

EE23BTECH11217 - Prajwal M*

EE 16

The steady state output V_{out} of the circuit shown below, will

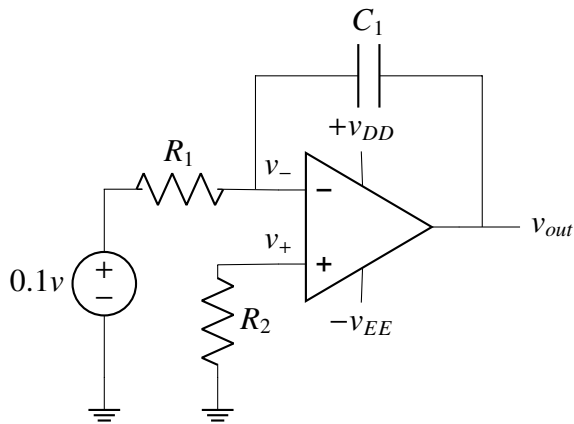


Fig. 0. circuit

- 1) saturate to $+V_{DD}$
- 2) saturate to $-V_{EE}$
- 3) become equal to $0.1V$
- 4) become equal to $-0.1V$

Solution:

Parameters	Description
v_{out}	Steady State Output Voltage
V_{out}	Laplace Transform of v_{out}

TABLE 4

PARAMETER DESCRIPTION

for an ideal OP amp,

$$V_+ = 0V \quad (1)$$

$$V_- = 0V \quad (2)$$

using KVL,

$$0 = \frac{V_- - 0.1}{R_1} + C_1 s (V_- - V_{out}) \quad (3)$$

$$V_{out} = \frac{V_- - 0.1}{R_1 C_1 s} + V_- \quad (4)$$

$$= -\frac{0.1}{R_1 C_1 s} \quad \text{using (2)} \quad (5)$$

$$V_{out} \xrightarrow{\mathcal{L}^{-1}} v_{out} \quad (6)$$

$$v_{out} = -\frac{0.1}{R_1 C_1} t \quad (7)$$

$$v_{out} = \max \left\{ -v_{EE}, -\frac{1}{R_1 C_1} t \right\} \quad (8)$$

Hence, v_{out} saturates to $-v_{EE}$

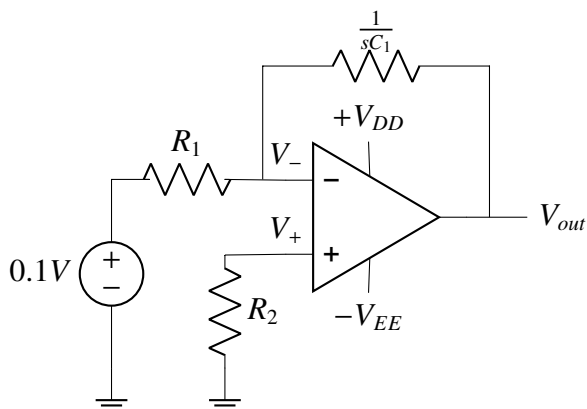


Fig. 4. s-domain circuit