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CS 20 Laboratory 7: Sequential Circuit Components

1. (0.25pt) From your circuit in 2.1.1, describe the LED's behavior in relation to the clock

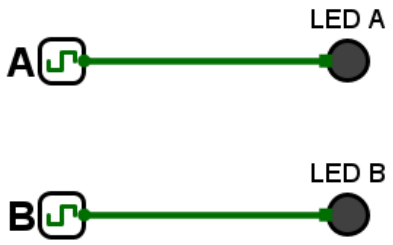
   As the clock ticks once, the LED lights up. Another tick will make the light turn off. For every tick in continuous ticking, the state of the LED changes – it transitions from off to on or on to off, continuing the pattern. This means that the LED is dependent on the state of the clock.

2. (0.75pt) Refer to your circuit in 2.1.2 for these questions

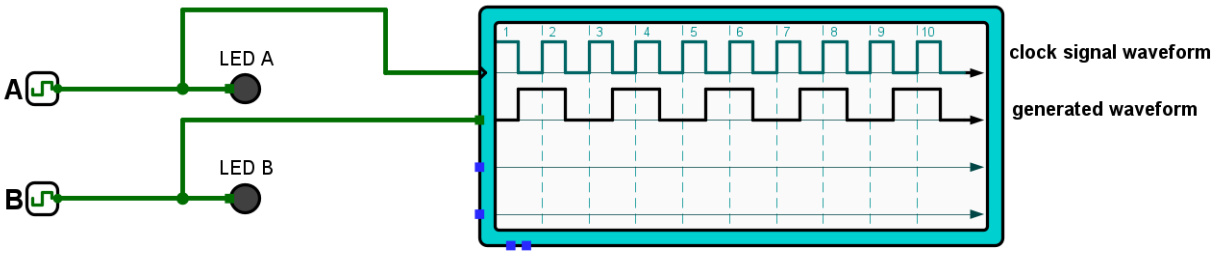
   a. (0.5pt) Is there a difference in the behavior of the two LEDs? Explain.

      Yes, there is a difference in the timing of the two LEDs. Since clock A and clock B have different durations (1 tick and 2 ticks, respectively), the time it takes for the LEDs to change state varies. In the first tick, LED A is already on, but LED B is still off – this is because LED B will only change every 2 ticks. By the second tick, LED A is already off, and LED B just turned on. At the third tick, LED A will turn on again while LED B is still turned on. By the fourth tick, LED A will now turn off together with LED B. This cycle continues for the continuous ticking.

   b. (0.25pt) Attach a picture of your circuit, make sure that the components are properly labelled



3. (1.5pts) Attach a picture of the oscilloscope reading of your circuit and do the following:



a. (0.25pt) Describe the shape of the generated waveform (triangular, square, sinusoidal, etc.).

The shape of the waveform is square since the width of the positive half is the same as the width of the negative half.

b. (0.25pt) Describe which part (edge, level, or others) of the generated waveform does the LED light up.

In reference to clock A's waveform, LED B lights up at the levels. In the 2nd tick, clock A is in low level while LED B lights up, and it remains lit as clock A shifts to high level. Once clock A shifts back to low level, LED B turns off.

c. (0.5pt) With respect with the clock signal waveform, what is the period of the generated waveform? Why? Answer in terms of the clock signal's period.

For the next items, let us assume that 1 tick is equivalent to 1 second. The clock signal waveform takes 2 seconds to complete a cycle. As for the generated waveform, its period is 4 seconds or 2 periods of the clock signal. Since one period of the clock signal is just one clock width for the generated waveform, it takes up 2 periods of the clock signal to complete the cycle.

d. (0.5pt) With respect with the clock signal waveform, what is the frequency of the generated waveform? Why? Answer in terms of the clock signal's frequency.

Since the clock signal waveform has a period of 2 seconds, its frequency is 0.5 Hz. This means that only half of the cycle is done in one tick or second. As for the generated waveform, its frequency is 0.25 Hz. In relation to the clock signal, the generated waveform takes up twice as much to complete the cycle, so its frequency is twice as less as well.

4. (2pts) The waveform that you must have observed will have portions that are high and portions that are low in every cycle. The percentage of the waveform's period which it spends at the HIGH state is called the duty cycle. Therefore, 75% duty cycle means that within a period, the amount of time the signal is HIGH is three times as much as it is in LOW.

a. (1pt) Compute for the duty cycle of the generated waveform

To compute for the duty cycle, we have the formula

$$duty\ cycle = \frac{clock\ width\ of\ HIGH}{period} \times 100\% = \frac{1}{2} \times 100\% = 50\%$$

Hence, the duty cycle of the generated waveform is 50%

b. (1pt) What is the relationship of the Clock's High and Low Duration with the duty cycle?

The duty cycle represents the percentage of the period spent at high duration. Since the computed duty cycle is 50%, this means that the clock spends half of the period in high duration, and we can infer that the other half is spent on low duration. We can also say that in a period, the low and high duration of the generated waveform is equal.

5. (4pts) Include a video (cs20labrep7.mp4) showing state transitions for the JK flip-flop for all possible input combinations for J, K and Qn−1. Ensure that the Pins for J and K can be clearly distinguished by either editing the video or putting labels on the circuit. Also ensure that the Digital Oscilloscope is clear and labelled in presenting the waveform of the components (clock, J, K, and Qn−1). No point will be given if any of the input or output components is missing. The video file must be under 50 MB (UVLE limit). 0.5 point each for each input combination for J, K, Qn−1 (during rising clock edges) (4pts). Note that you can change the High and Low Duration of your clock signal to have more time to change inputs just make sure that they are equal. Submit your Logisim circuit as cs20lab7 2.circ.