CS 20 Project 1: Adder and Comparator with base conversion

DOCUMENTATION

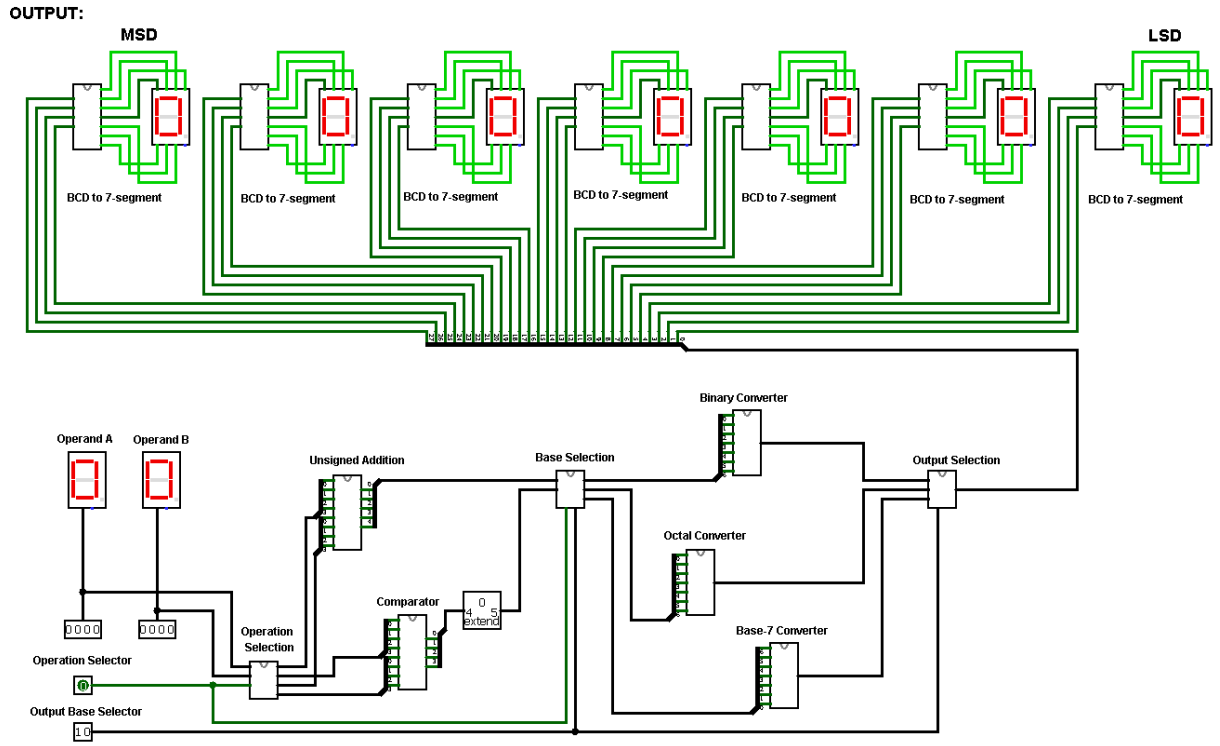

Fig 1. Schematic Diagram of the whole system

The system is composed of 4 user inputs: Operand A, Operand B, Operation Selector, and Output Base Selector. Both Operand A and B each have 4 bits and are displayed using a hex display.

The Operation Selector pin has 1 bit that selects the operation to be performed. It is connected to the Operation Selection subcircuit which depicts whether the operands are going to be inputted in the Unsigned Addition or Comparator subcircuits, depending on the input of the Operation Selector pin.

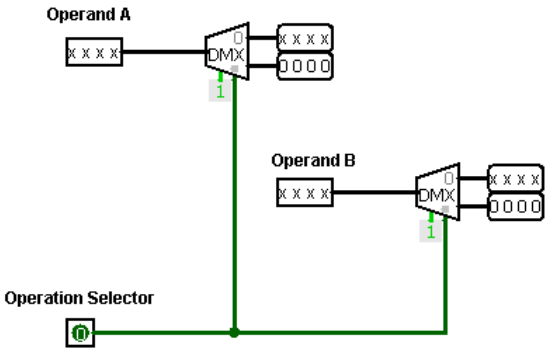

Fig 2. Schematic Diagram of the Output Selection Subcircuit

Each operand is connected to a demultiplexer with the source destination dependent on the Operation Selector pin. When 0 is selected, Output 1 and 3 of the Operation Selection subcircuit will be passed to the Unsigned Addition subcircuit. Conversely, if 1 is selected, Output 2 and 4 of the Operation Selection subcircuit will be passed to the Comparator subcircuit.

When Operation Selector Pin is 0: Unsigned Addition

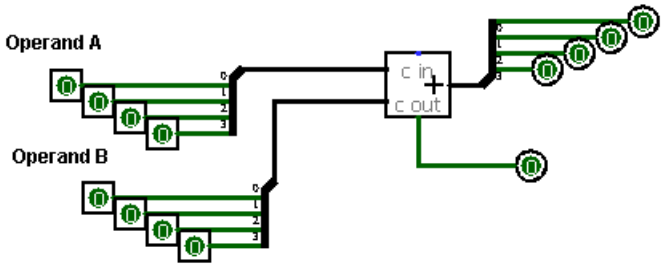

Fig 3. Schematic Diagram of the Unsigned Addition Subcircuit

Since the inputs for the Unsigned Addition subcircuit are 2 sets of 4 bits, a splitter is used to input both operands in the 4-bit adder. Because of the carry, there is a possibility of 5 outputs so there are 5 output pins.

When Operation Selector Pin is 1: Comparator

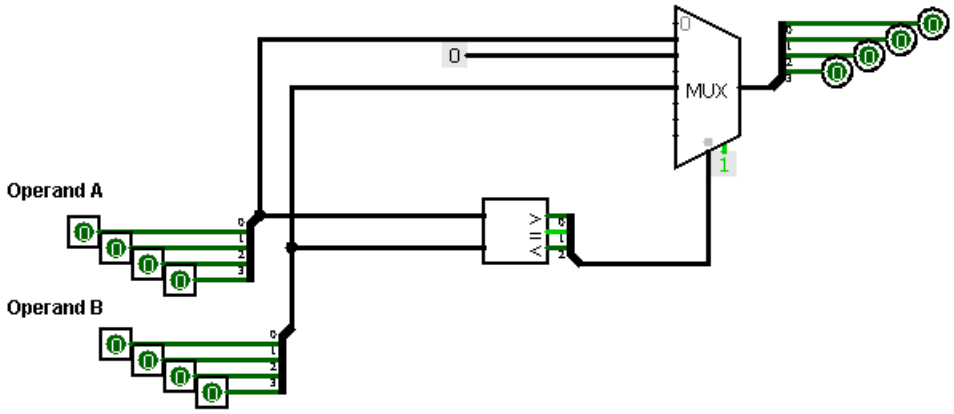

Fig 4. Schematic Diagram of the Comparator Subcircuit

Like in the Unsigned Addition, a splitter is used for the inputs which are connected to a 4-bit comparator and a multiplexer. Operand A is connected to 001, Operand B is connected to 100, and a constant 0000 is connected to 010. With the comparator as the source address, if the result is A>B, the output is 001 so the multiplexer will pass Operand A as output. Similar process will happen for A=B with 010 to output 0000, and A<B with 100 to output Operand B.

Since the output of the Unsigned Addition subcircuit has 5 bits, a bit extender is attached to the output of the Comparator subcircuit to match the number of bits. Results of both operations are then passed to the Base Selection Subcircuit.

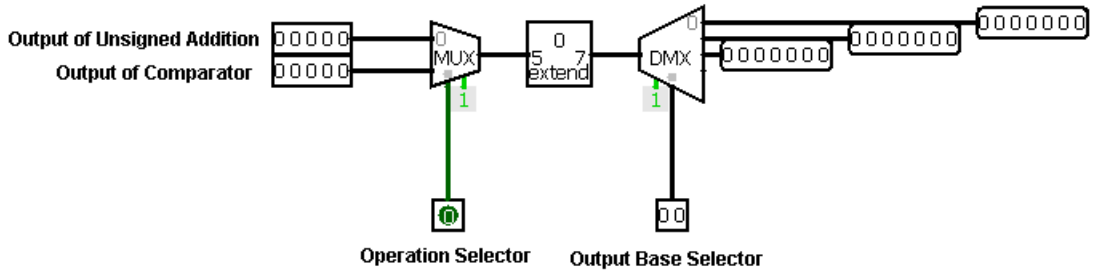

Fig 5. Schematic Diagram of the Base Selection Subcircuit

The outputs of the operations are connected to a multiplexer with the source address dependent on the Operation Selector pin. If the pin is 0, the output of the Unsigned Addition is passed; if the pin is 1, the output of the Comparator is passed. The result is extended to 7 bits corresponding to the 7 7-segment displays and is connected to a demultiplexer. The destination address of the demultiplexer is dependent on the Output Base Selector pin: 00 for Binary, 01 for Octal and 10 for Mystery base.

When Output Base Selector Pin is 00: Binary

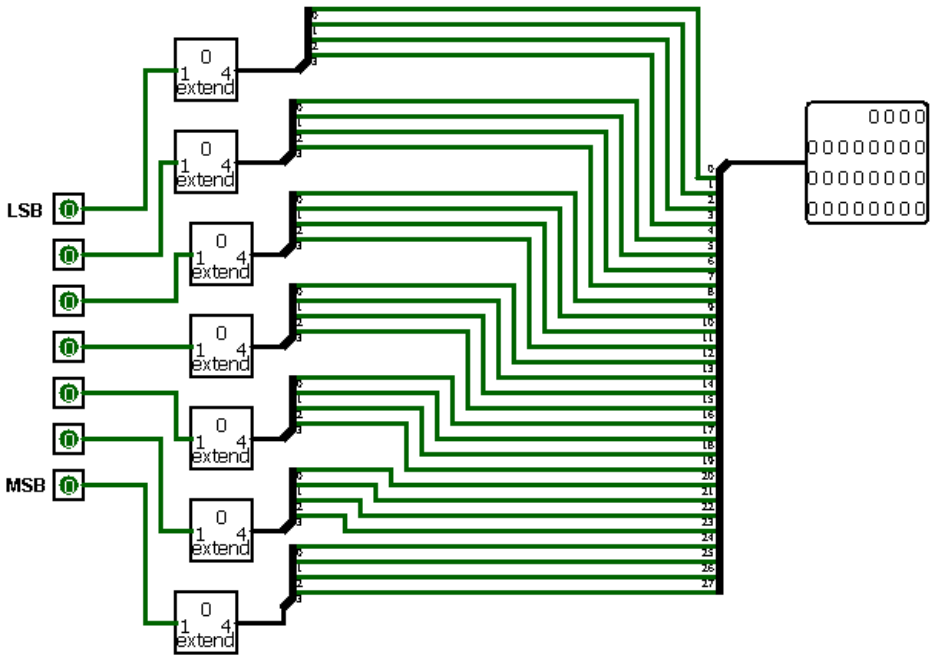

Fig 6. Schematic Diagram of the Binary Converter Subcircuit

Since the result of the operation has already 7 bits, each bit can be connected to a single 7-segment display. The BCD to 7-segment converter needs 4 bits so each bit of the operation result is extended to 4 bits with a total of 28 output bits.

When Output Base Selector Pin is 01: Octal

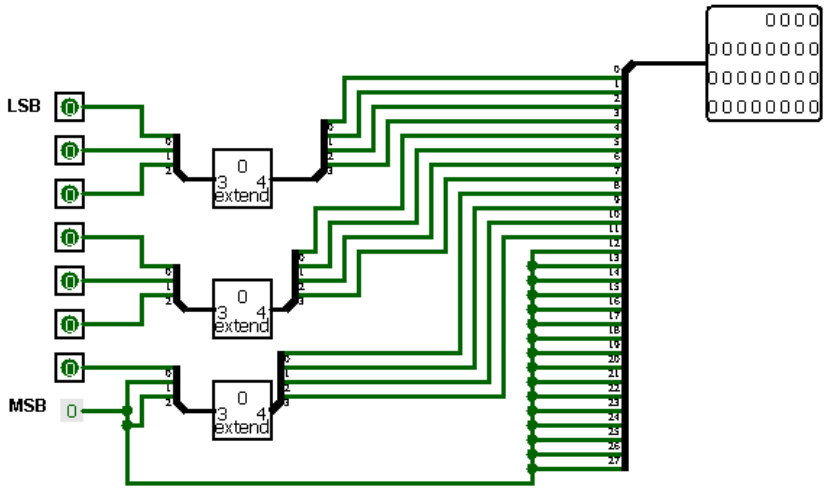

Fig 7. Schematic Diagram of the Octal Converter Subcircuit

The 7-bit result of the operation is divided by 3s, with the MSB grouped with 2 zeroes. The first 3 bits (from the LSB) will now correspond to the LSD in the 7-segment display, so it is extended to 4 bits. The next 3 bits will now be the next digit from the right, and so on. For the last 4 digits, it is padded to zero. We can confirm that the maximum result of all the operations (F_{16} + F_{16} or 1111_2 + 1111_2) only needs 2 digits for octal (36_8) so we do not need to worry about the other values.

When Output Base Selector Pin is 10: Mystery Base

The last 4 digits of my student number is 6676 so the result of the computation is (6+6+7+6)%3 = 1 which corresponds to base-7.

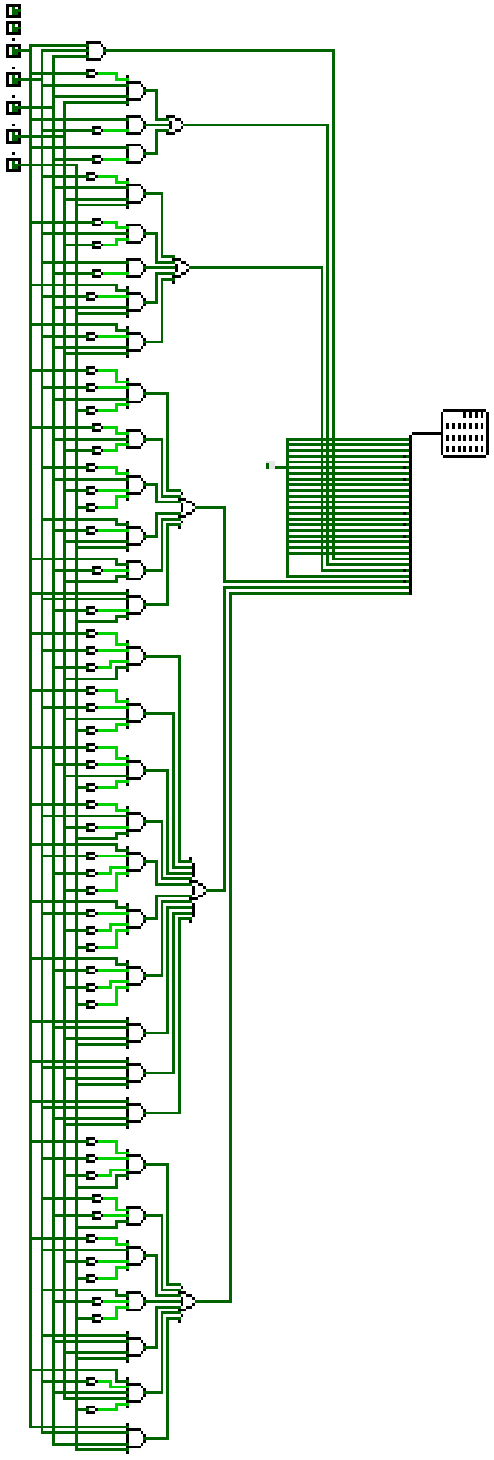

Fig 8. Schematic Diagram of the Base-7 Converter Subcircuit

The maximum result of all the operations (F_{16} + F_{16} or 1111_2 + 1111_2) only uses 5 bits in binary (11110_2) so we only need to convert those bits into base-7 and ignore the 2 bits from the MSB. Furthermore, the conversion of the maximum to base-7 only needs 2 digits (42_7) so we do not need to worry about the other values for the converted output.

The circuit is made using Logisim's combinational analysis function with the following truth table:

E	D	C	B	A	b_2	b_1	b_0	a_2	a_1	a_0
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	1	0
0	0	0	1	1	0	0	0	0	1	1
0	0	1	0	0	0	0	0	1	0	0
0	0	1	0	1	0	0	0	1	0	1
0	0	1	1	0	0	0	0	1	1	0
0	0	1	1	1	0	0	1	0	0	0
0	1	0	0	0	0	0	1	0	0	1
0	1	0	0	1	0	0	1	0	1	0
0	1	0	1	0	0	0	1	0	1	1
0	1	0	1	1	0	0	1	1	0	0
0	1	1	0	0	0	0	1	1	0	1
0	1	1	0	1	0	0	1	1	1	0
0	1	1	1	0	0	1	0	0	0	0
0	1	1	1	1	0	1	0	0	0	1
1	0	0	0	0	0	1	0	0	1	0
1	0	0	0	1	0	1	0	0	1	1
1	0	0	1	0	0	1	0	1	0	0
1	0	0	1	1	0	1	0	1	0	1
1	0	1	0	0	0	1	0	1	1	0
1	0	1	0	1	0	1	1	0	0	0
1	0	1	1	0	0	1	1	0	0	1
1	0	1	1	1	0	1	1	0	1	0
1	1	0	0	0	0	1	1	0	1	1
1	1	0	0	1	0	1	1	1	0	0
1	1	0	1	0	0	1	1	1	0	1
1	1	0	1	1	0	1	1	1	1	0
1	1	1	0	0	1	0	0	0	0	0
1	1	1	0	1	1	0	0	0	0	1
1	1	1	1	0	1	0	0	0	1	0
1	1	1	1	1	1	0	0	0	1	1

Table 1. Truth Table of the Base-7 Converter Subcircuit

Where E is the MSB and A is the LSB. Each digit output, b and a, has 3 bits ($b_{-2}b_{-1}b_{-0}$ and $a_{-2}a_{-1}a_{-0}$) until 110_2 (6_{10}). When the desired digit is 7_{10} and above, base-7 uses 2 digits to represent it.

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2020-06676

Here is the k-map of each output of the truth table together with its SOP:

b_2:

DC \ BA	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

E = 0

DC \ BA	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	0	0

E = 1

SOP: EDC

b_1:

DC \ BA	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	1	1
10	0	0	0	0

E = 0

DC \ BA	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

E = 1

SOP: E'DCB + ED' + EC'

b_0:

DC \ BA	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	1	1	0	0
10	1	1	1	1

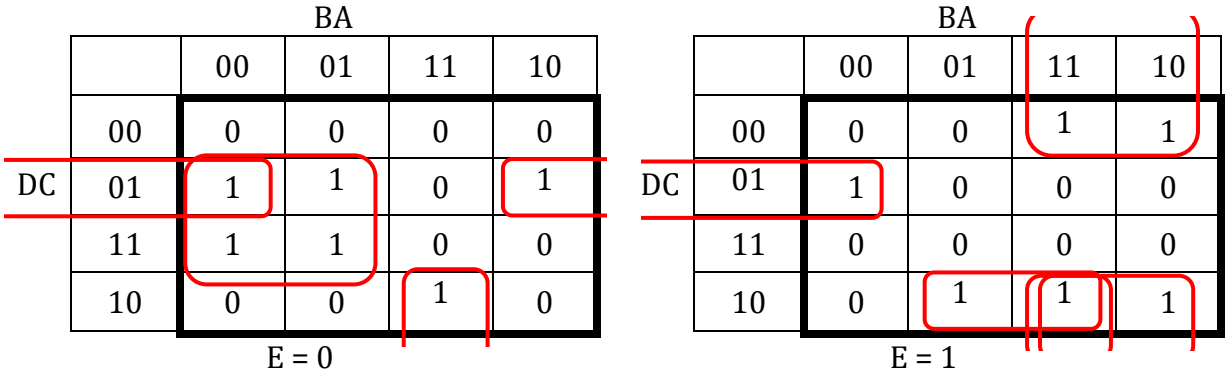
E = 0

DC \ BA	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	0	0	0	0
10	1	1	1	1

E = 1

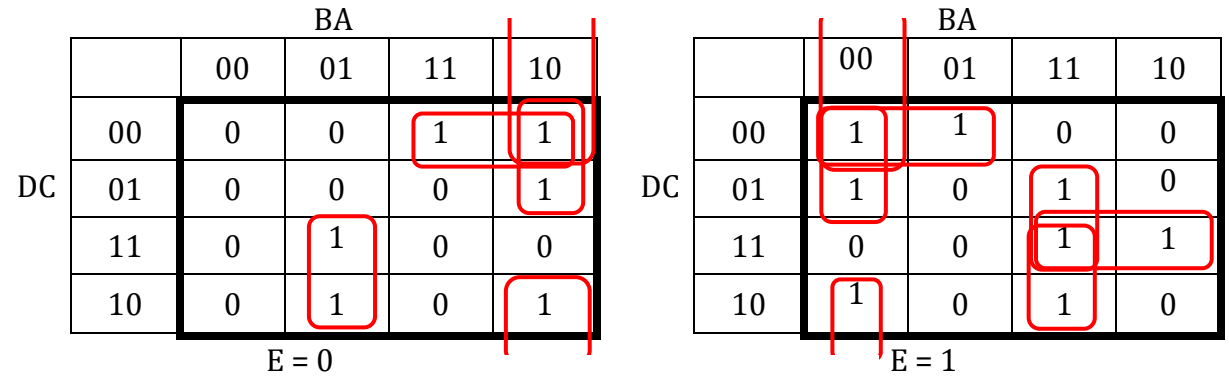
SOP: E'DB' + DC' + D'CBA + ED'CA + ED'CB

a_2:



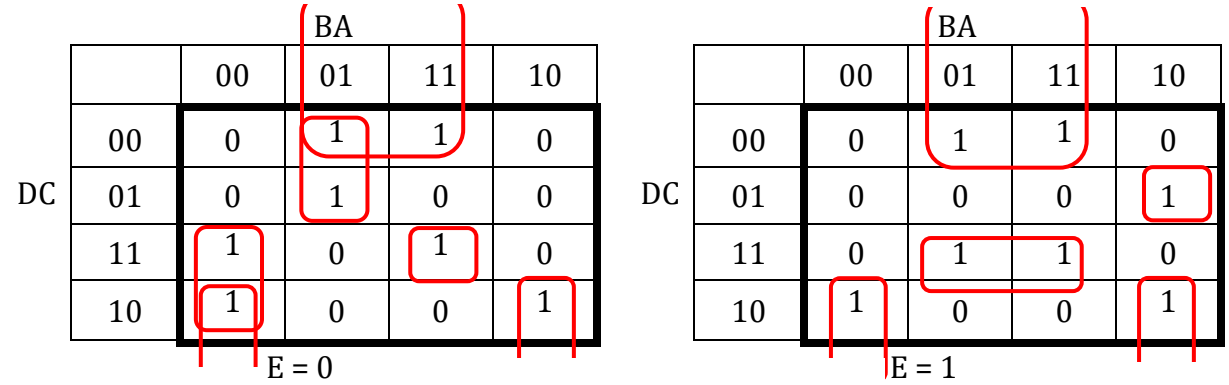
SOP: E'CB' + DC'BA + EC'B + EDC'A + D'CB'A' + E'D'CA'

a_1:



SOP: E'DB'A + E'D'C'B + E'BA' + E'C'BA' + ED'B'A' + EC'B'A' + ED'C'B' + ECBA + EDCB + EDBA

a_0:



SOP: E'D'B'A + E'DB'A' + D'C'A + DC'A' + DCBA + EDCA + ED'CBA'

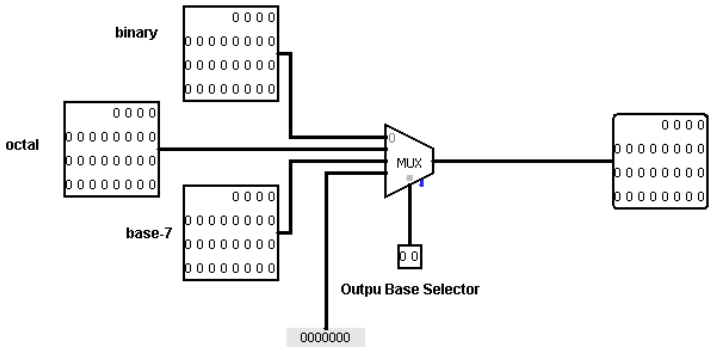


Fig 9. Schematic Diagram of the Output Selection Subcircuit

The result of the 3 base conversions, along with a 28-bit 0, are connected to a multiplexer. The source address is dependent on the Output Base Selector pin. When the pin is 00, it passes the converted output in binary, 01 for octal, 10 for base-7, and 11 for the zeroes.

The output of the Output Selection Subcircuit is then connected to a 28-bit splitter to deliver 4 bits each to the 7-segment displays. These 4 bits correspond to BCD and are converted using a BCD to 7-segment Converter Subcircuit.

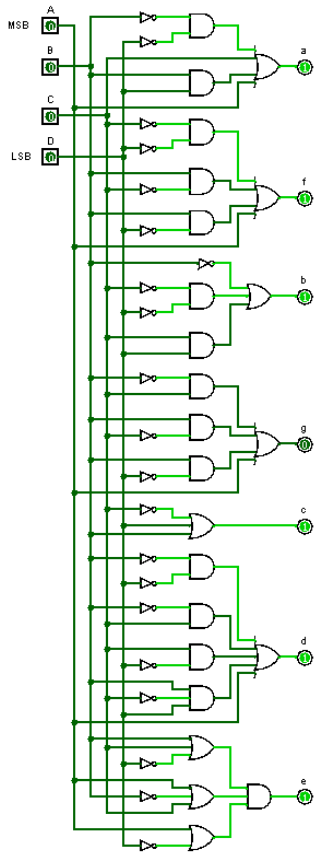


Fig 10. Schematic Diagram of the BCD to 7-segment Converter Subcircuit

The circuit is made using Logisim's combinational analysis function with the following truth table:

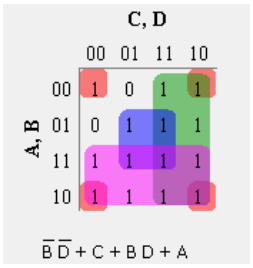
A	B	C	D	a	f	b	g	c	d	e
0	0	0	0	1	1	1	0	1	1	1
0	0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	0
0	1	0	0	0	1	1	1	1	0	0
0	1	0	1	1	1	0	1	1	1	0
0	1	1	0	1	1	0	1	1	1	1
0	1	1	1	1	0	1	0	1	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	0	1	1
1	0	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1
1	1	0	1	1	1	0	1	1	1	1
1	1	1	0	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1

Table 2. Truth Table of the BCD to 7-segment Converter Subcircuit

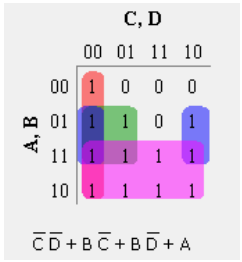
Where A is the MSB and D is the LSB of the 4-bit input. Each part of the 7-segment display is represented by the outputs a-g.

Here is the k-map of each output of the truth table together with its SOP:

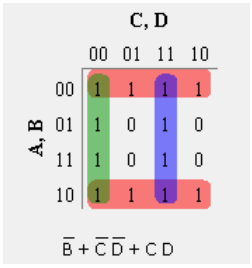
a:



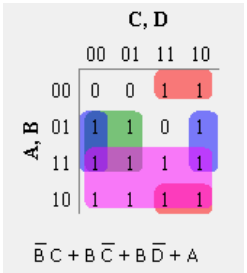
f:



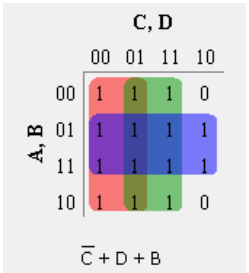
b:



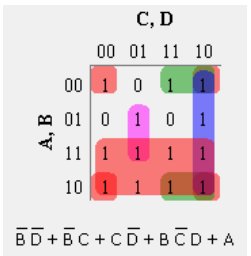
g:



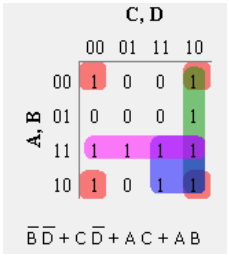
c:



d:



e:



With each of the 4 bits in the 28-bit result corresponding to a digit in the 7 7-segment displays, the results of the operations selected converted into the base selected is shown as the output of the system.

LINK FOR THE DOCUMENTATION VIDEO:

https://drive.google.com/file/d/1dGvWeHc_pKiugjfJNb7M_PG3HmL6hRR8/view?usp=sharing