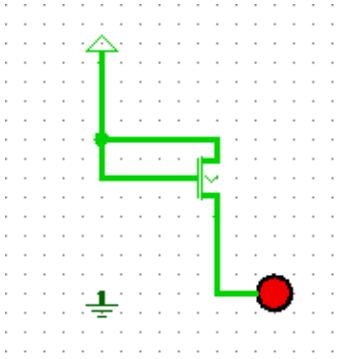
CS 20 Laboratory 3: Transistors as Digital Logic Building Blocks

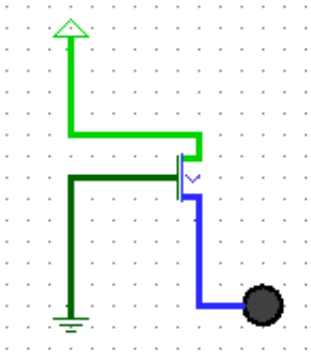
1. Transistor as Switches

   In the experiment done in Section 2.1, describe what happens to the LED when you connect the gate pin to the power source. How about when you connect the gate pin to ground? Provide pictures for both instances

   When the gate pin is connected to the power source, the LED lights up.



   Conversely, when the gate pin is connected to the ground, the LED does not light up.

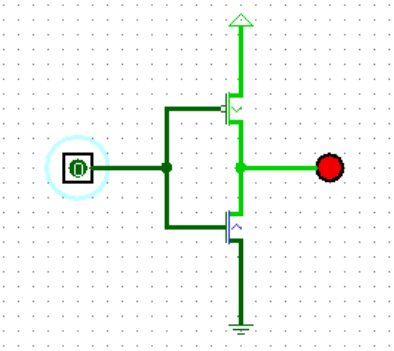


2. NOT GATE

   In the experiment done in Section 2.2.1, what is V out of the circuit:

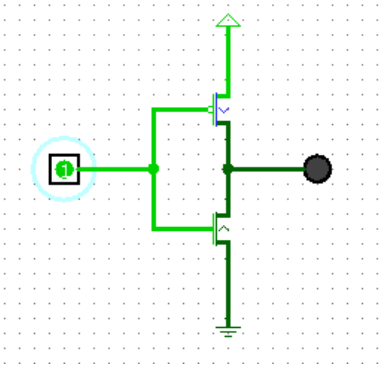
   a. when V in is 0? Explain why the circuit gave that output. Include the states (closed/open switch) of the nMOS and pMOS

      When V in is 0, V out is 1 (high). Since the input is equivalent to GND, the current can't flow in the nMOS and it becomes an open switch (turned off). Conversely, the pMOS becomes a closed switch (turned on) so the power source flows through the drain and outputs 1 (high) characterized by the light in the LED.



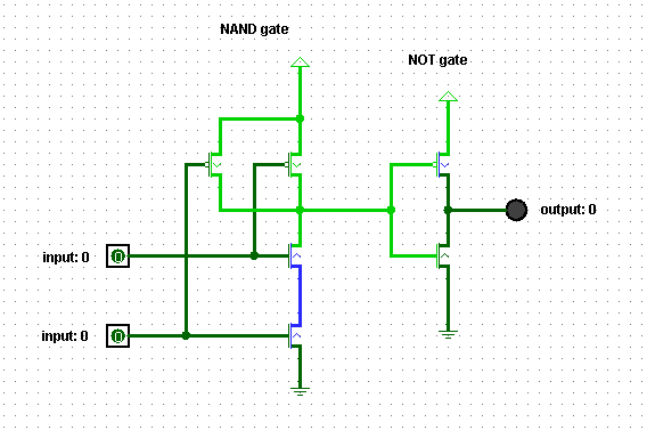
b. when V in is 1? Explain why the circuit gave that output. Include the states (closed/open switch) of the nMOS and pMOS.

When V in is 1, V out is 0 (low). Since the input is equivalent to VDD, the current can't flow in the pMOS and it becomes an open switch (turned off). Conversely, the nMOS becomes a closed switch (turned on) so the ground connects through the drain and outputs 0 (low) characterized by the absence of light in the LED.

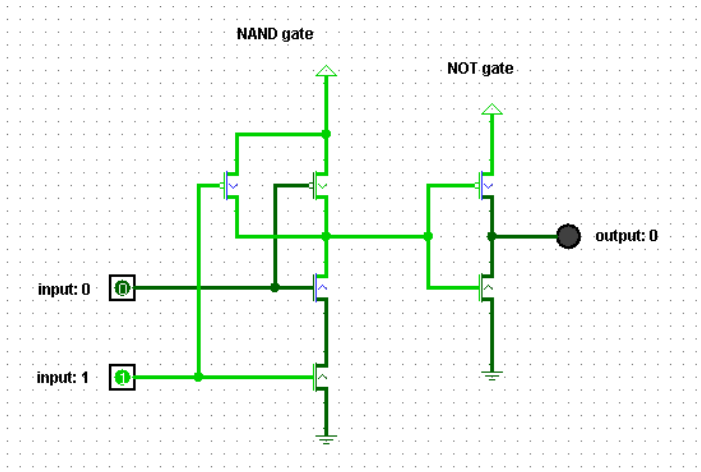


3. Using the NAND gate in Figure 4 and NOT gate in Figure 3, create an AND gate in Logisim and save it as cs20labrep3b.circ. Provide a screenshot of the simulator for each input combination possible of the circuit created. Have input labels in all of the screenshots. Clearly show the input and the output of the circuit.

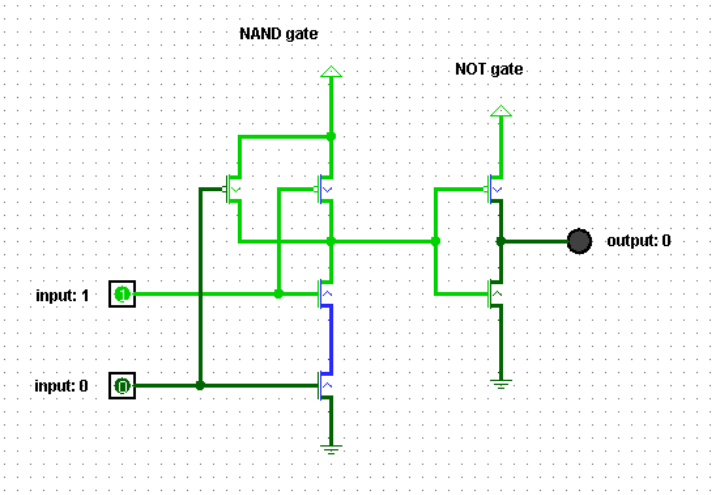
a. Input: 0, 0 Output: 0



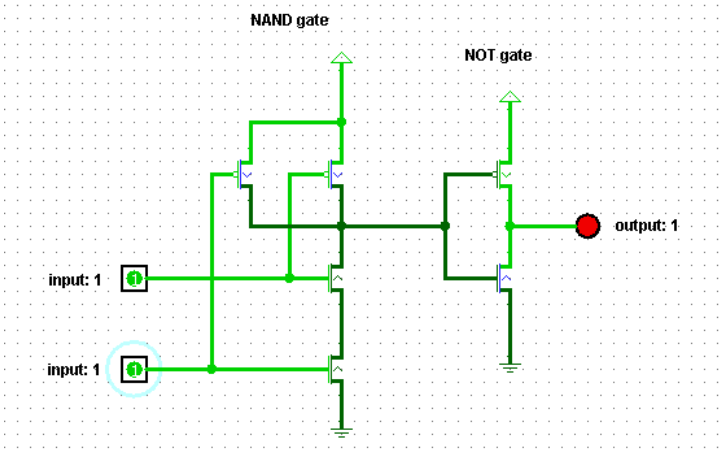
b. Input: 0, 1 Output: 0



c. Input: 1, 0 Output: 0

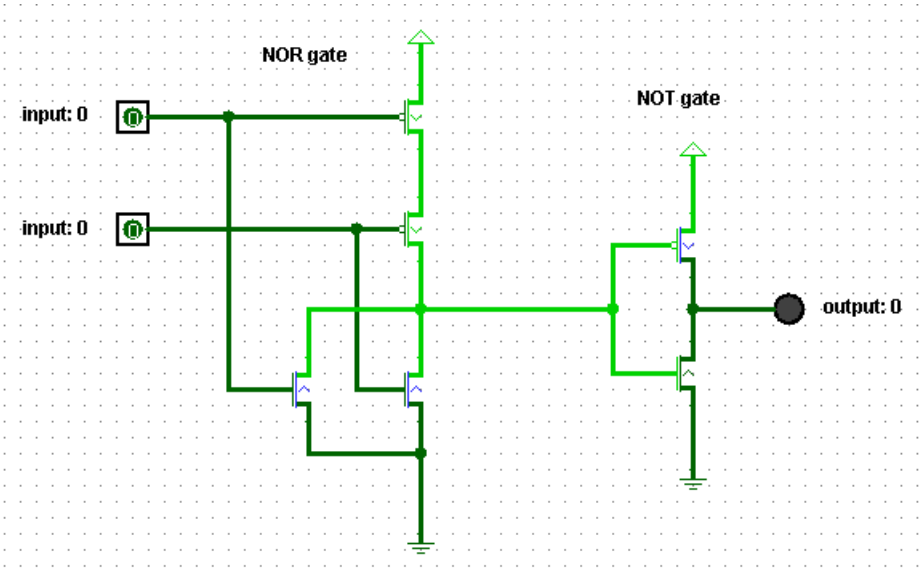


d. Input: 1, 1 Output: 1

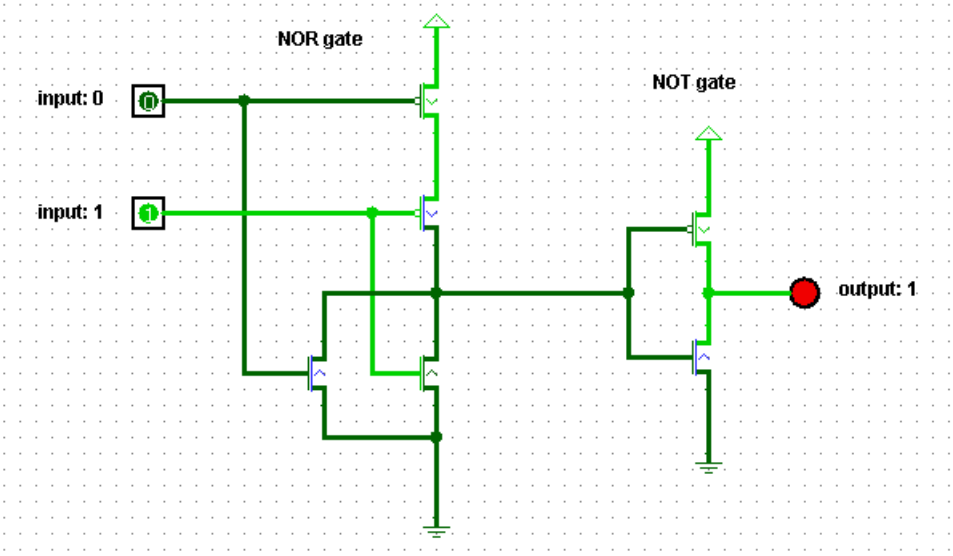


4. Using the NOR gate in Figure 5 and NOT gate in Figure 3, create an OR gate in Logisim and save it as cs20labrep3c.circ. Provide a screenshot of the simulator for each input combination possible of the circuit created. Have input labels in all of the screenshots. Clearly show the input and the output of the circuit.

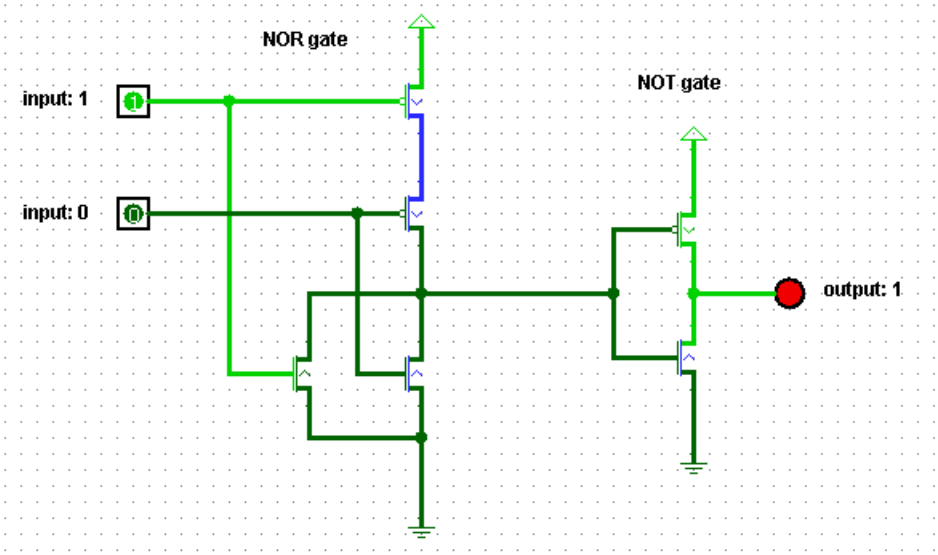
   a. Input: 0, 0 Output: 0



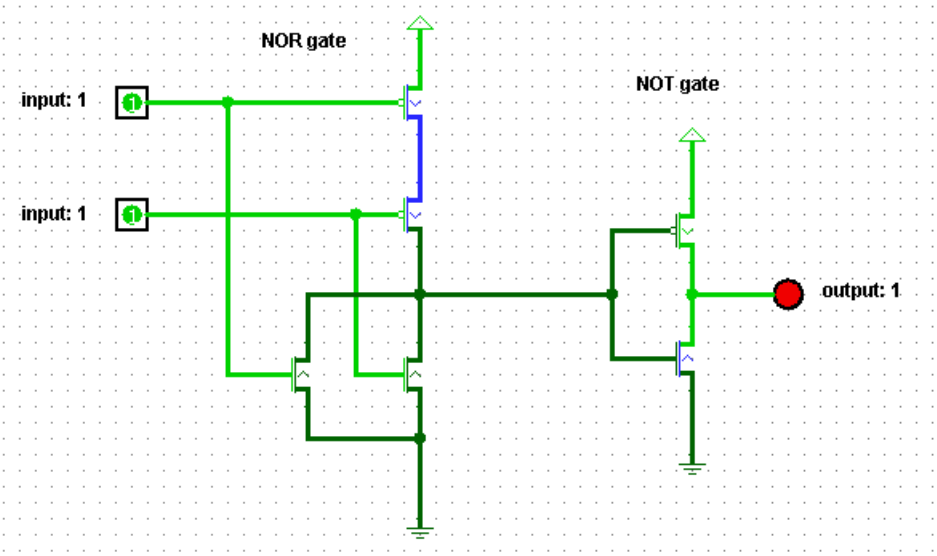
   b. Input: 0, 1 Output: 1



c. Input: 1, 0 Output: 1



d. Input: 1, 1 Output: 1



5. Show a schematic diagram (i.e., diagram with pMOS and nMOS symbols) of your CMOS logic circuit done in Section 2.3.

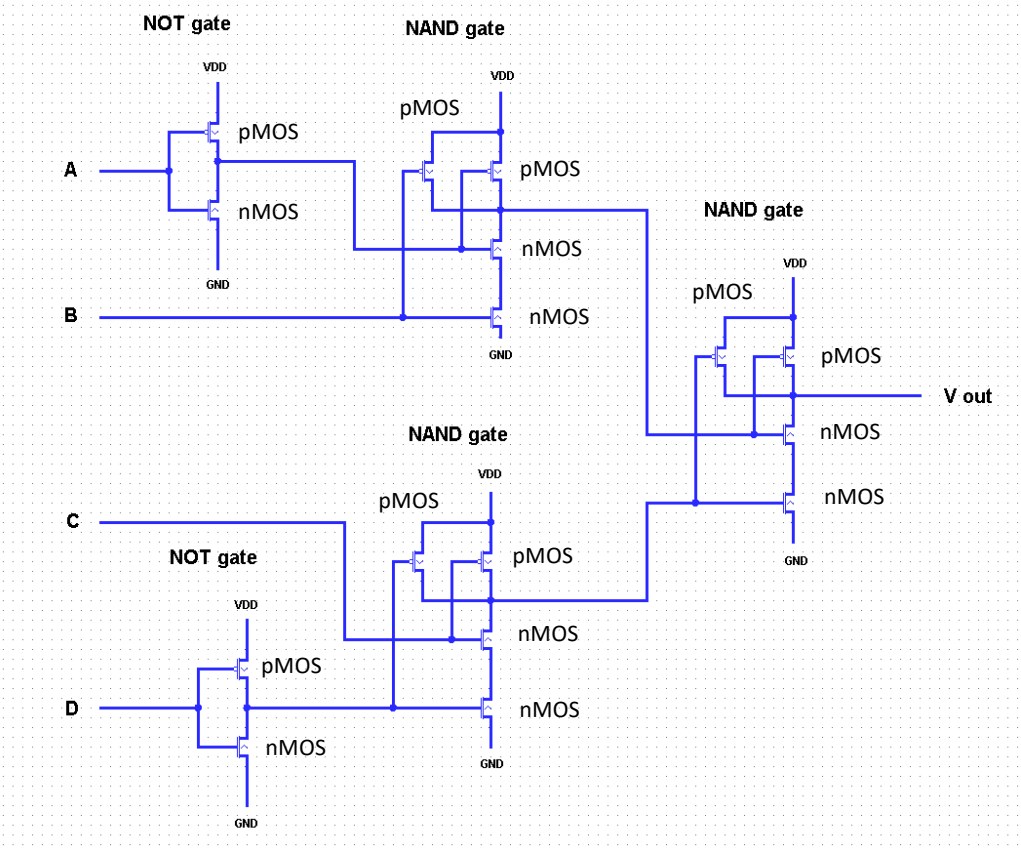
$\bar{A}B + C\bar{D}$

$\overline{\overline{\bar{A}B}} + C\bar{D}$ Involution

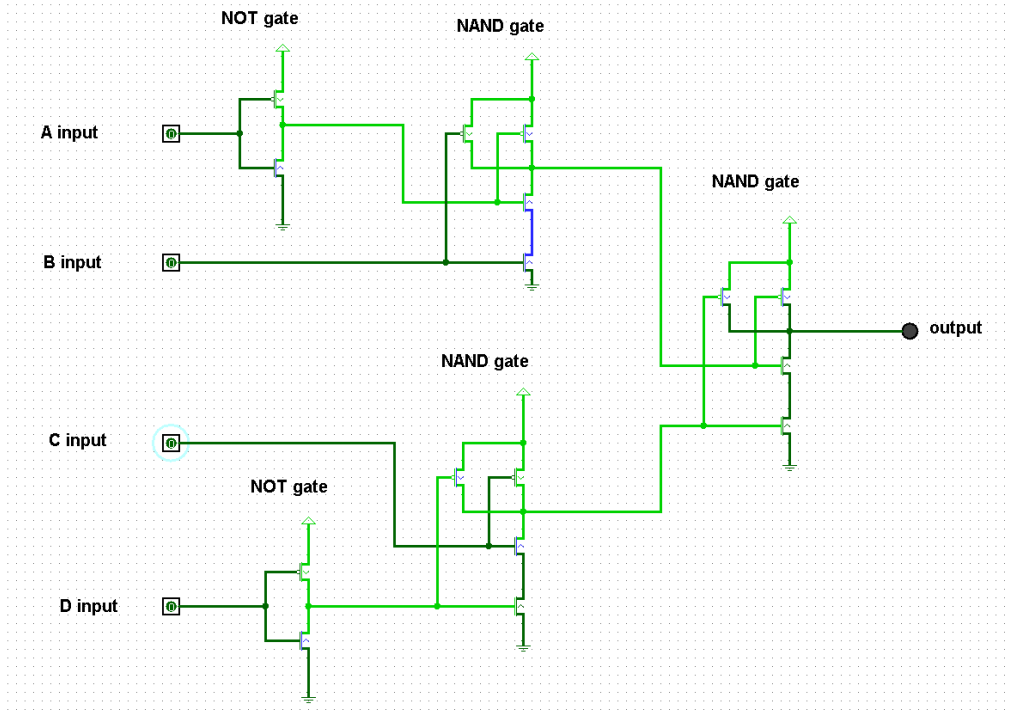
$\overline{\overline{\bar{A}B}} + \overline{\overline{C\bar{D}}}$ Involution

$\overline{(\overline{\bar{A}B})(\overline{C\bar{D}})}$ De Morgan's Laws

Schematic Diagram:



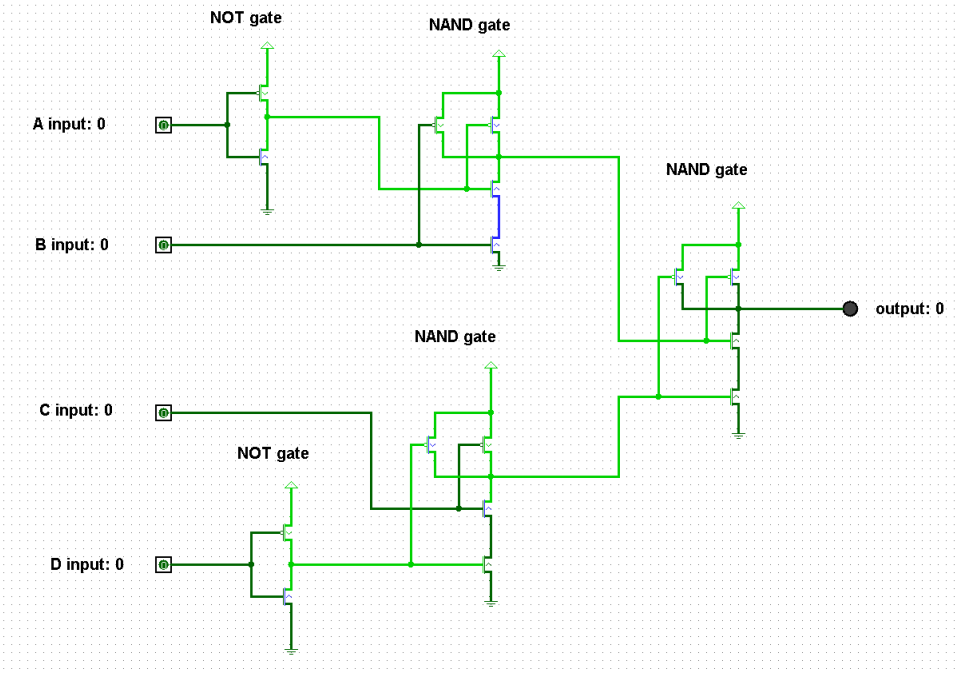
Implementation in Logisim:



6. Provide a picture for each input combination possible (in standard order; 16 total, 0.5 pts each) of your CMOS logic circuit in Logisim as defined in Section 2.3. Have input labels in the screenshot. Ensure that the LED clearly reflects the output.

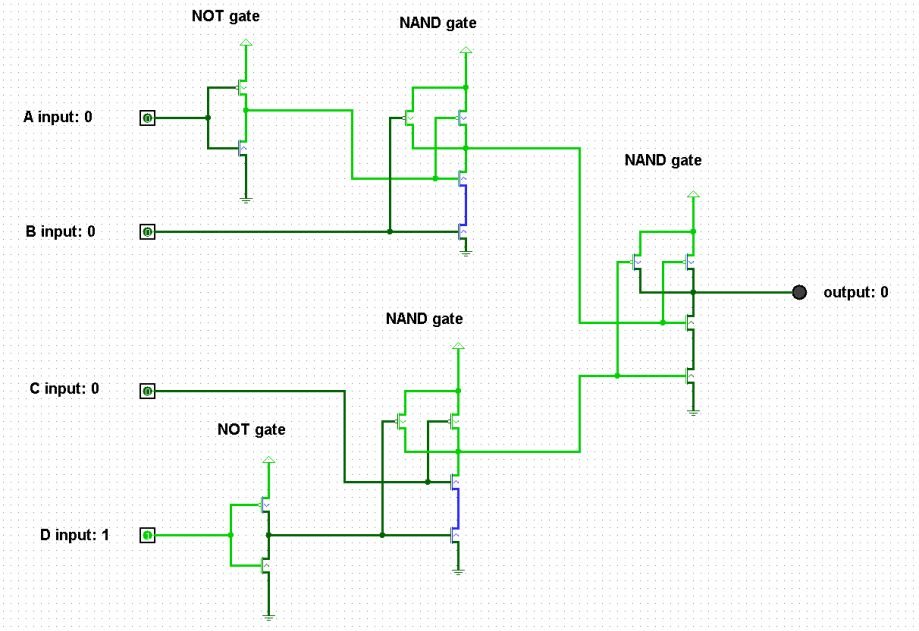
   i. A input: 0 C input: 0 Output: 0

   B input: 0 D input: 0



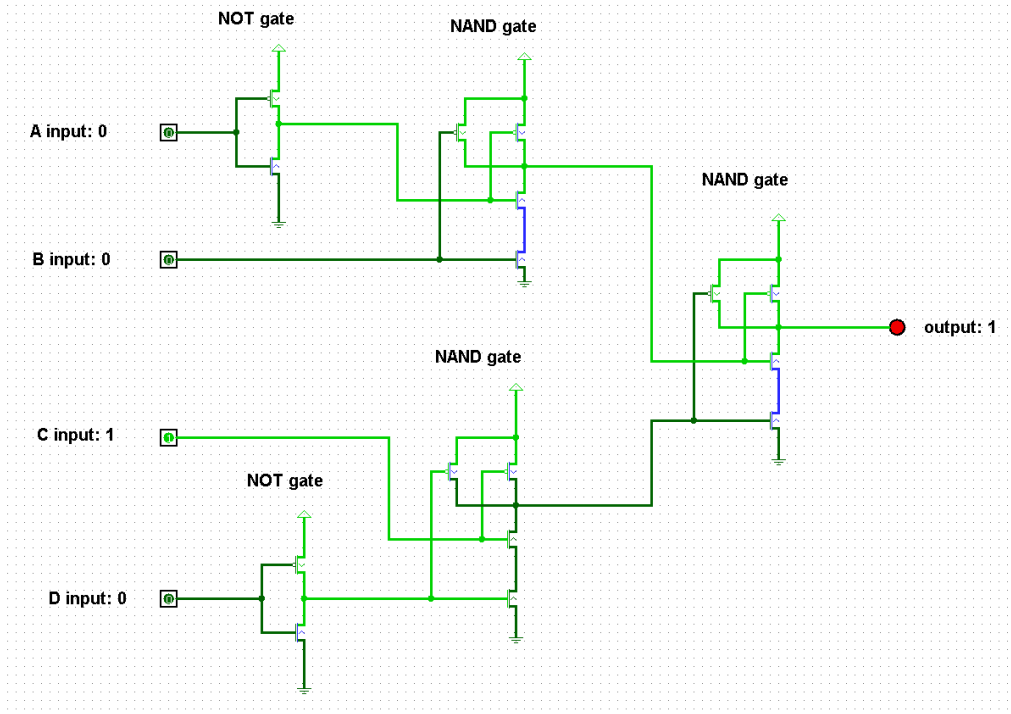
   ii. A input: 0 C input: 0 Output: 0

   B input: 0 D input: 1



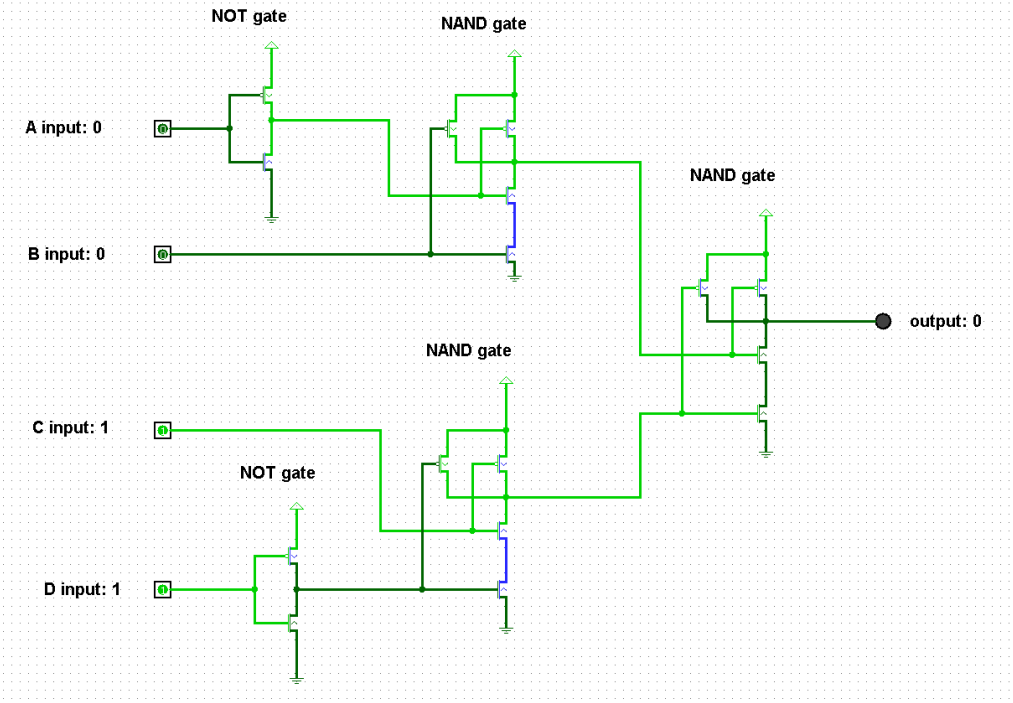
iii. A input: 0 C input: 1 Output: 1

B input: 0 D input: 0



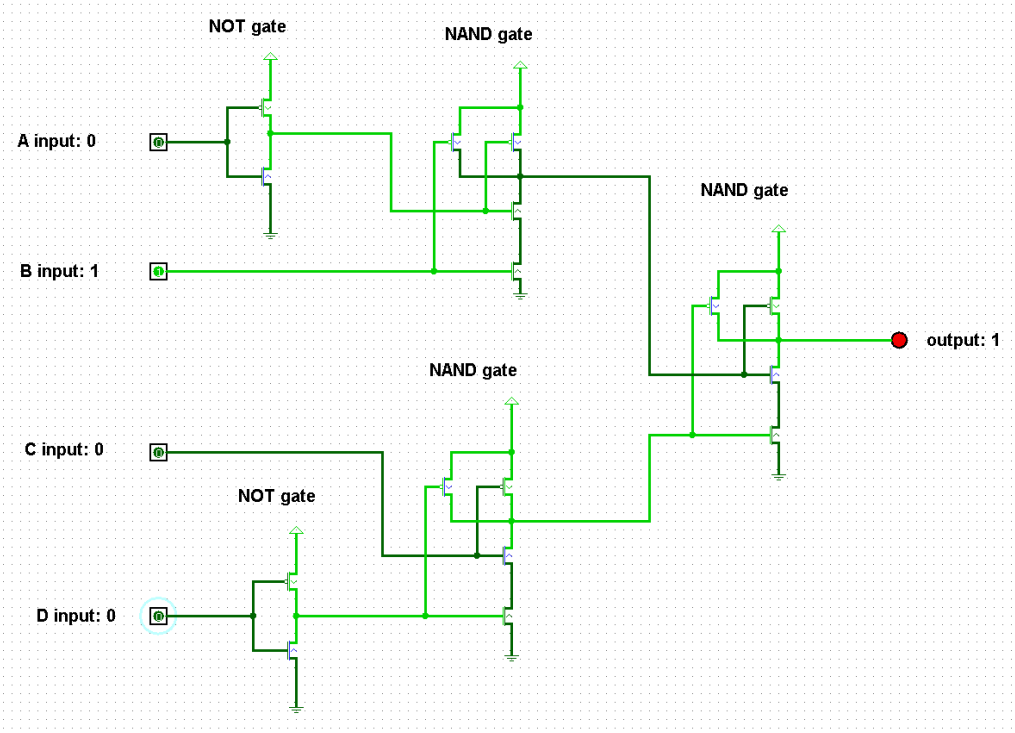
iv. A input: 0 C input: 1 Output: 0

B input: 0 D input: 1



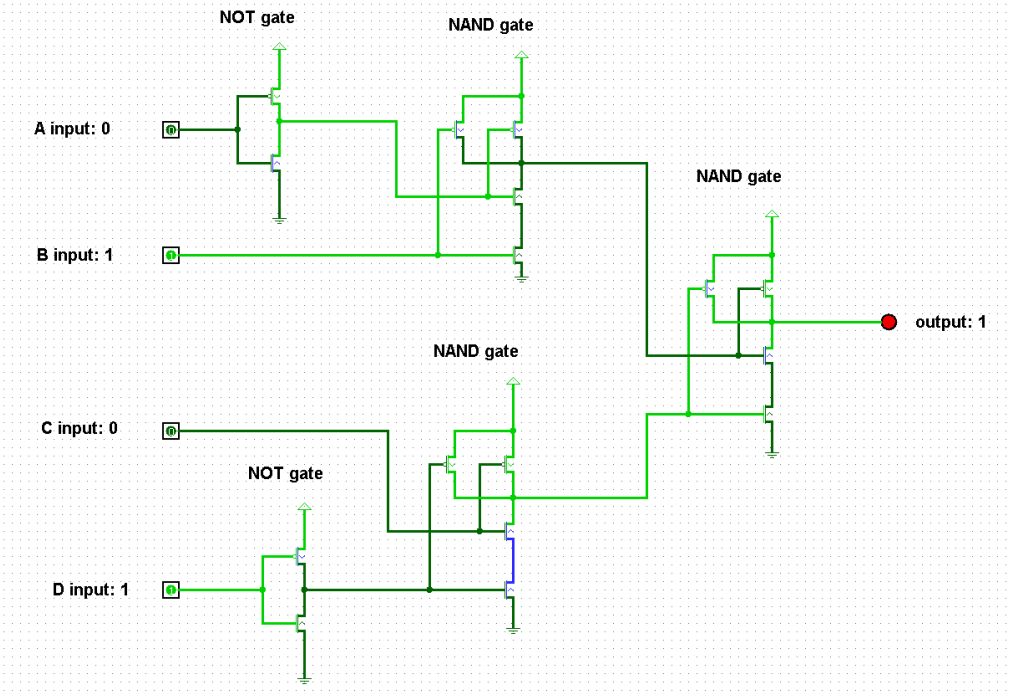
v. A input: 0 C input: 0 Output: 1

B input: 1 D input: 0



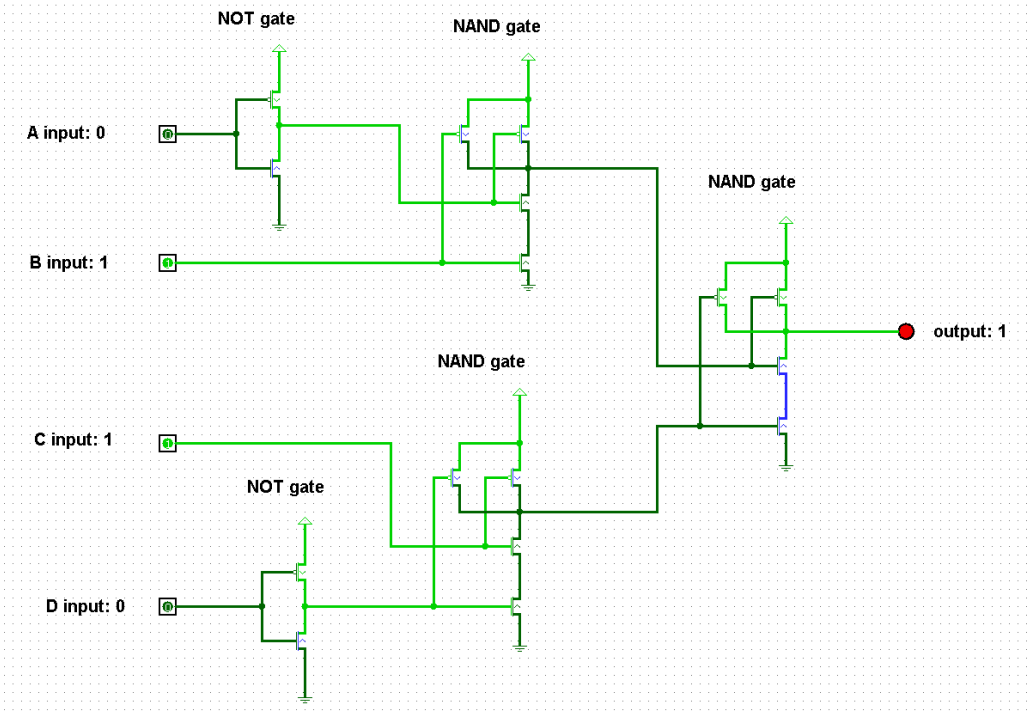
vi. A input: 0 C input: 0 Output: 1

B input: 1 D input: 1



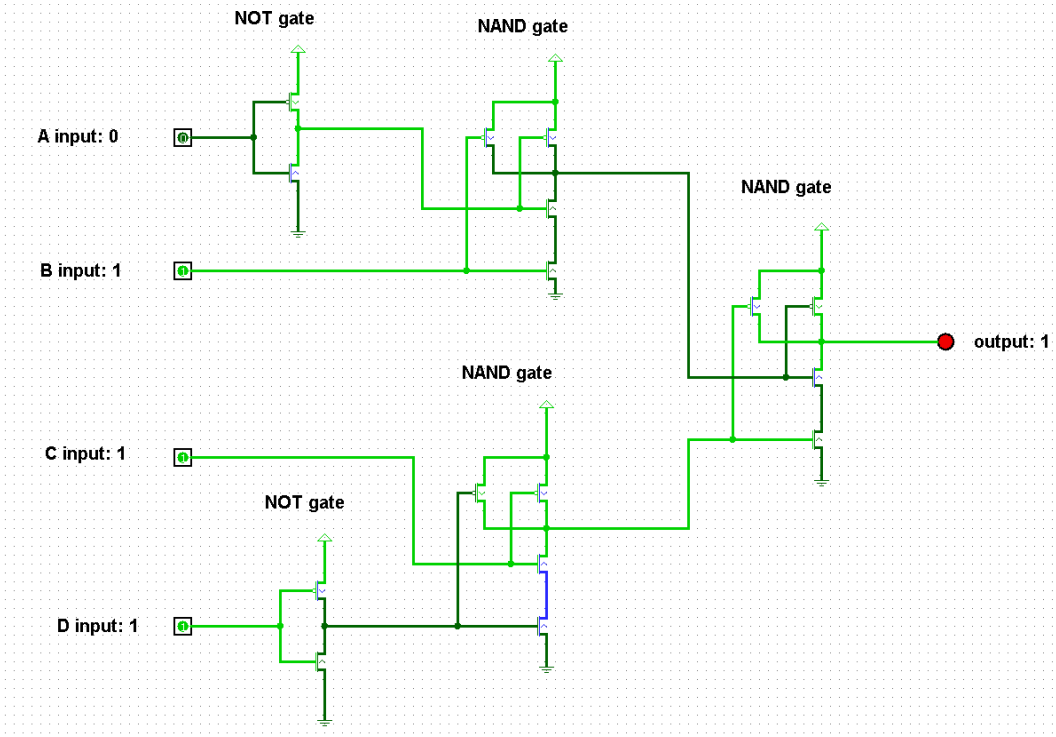
vii. A input: 0 C input: 1 Output: 1

B input: 1 D input: 0



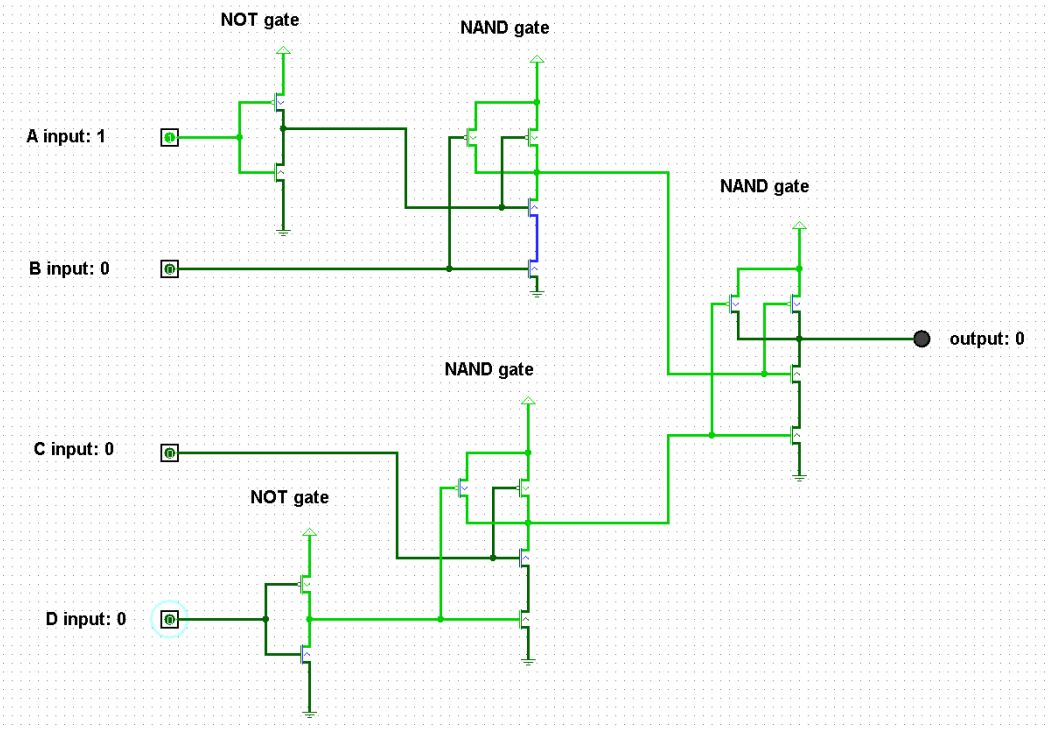
viii. A input: 0 C input: 1 Output: 1

B input: 1 D input: 1



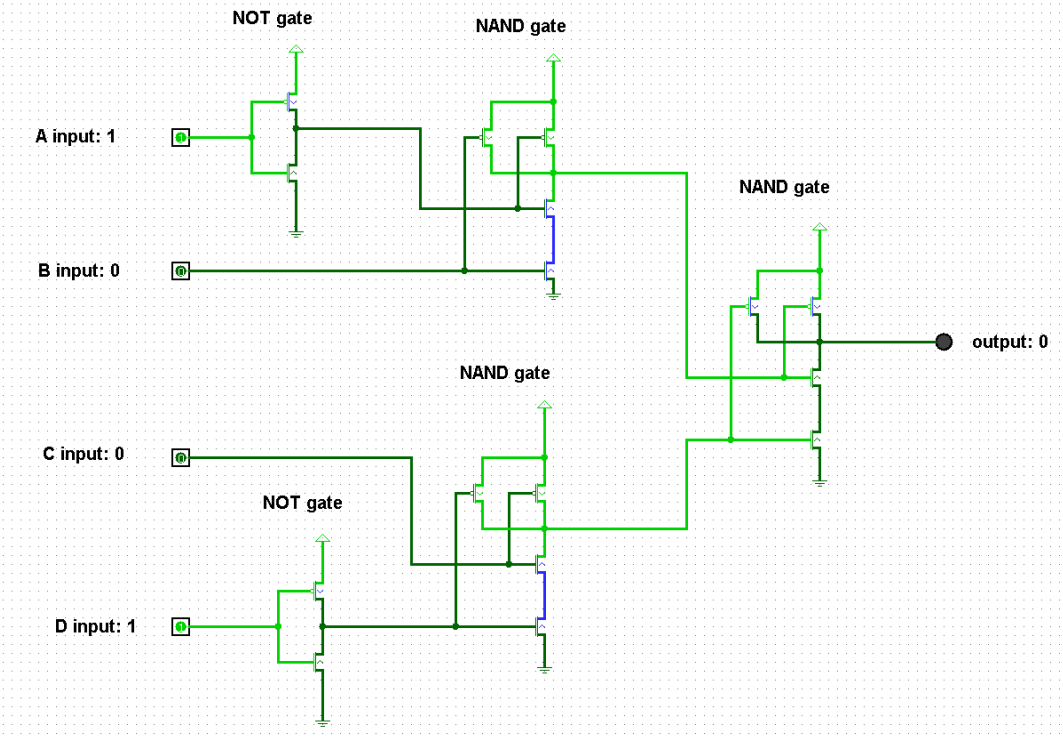
ix. A input: 1 C input: 0 Output: 0

B input: 0 D input: 0



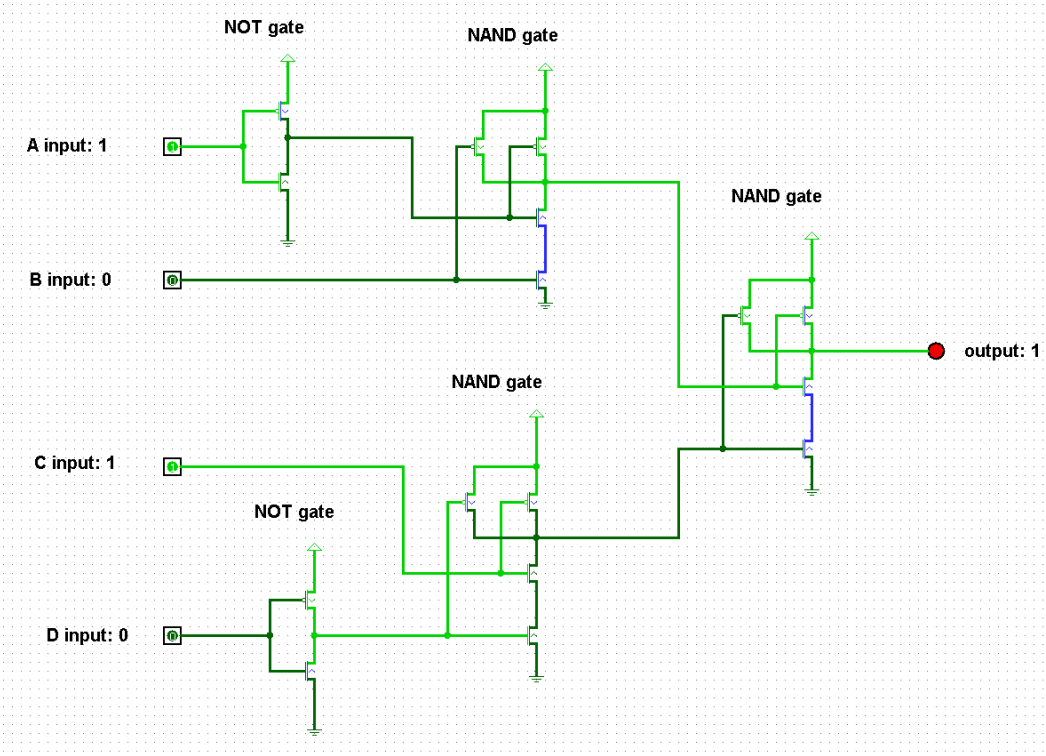
x. A input: 1 C input: 0 Output: 0

B input: 0 D input: 1



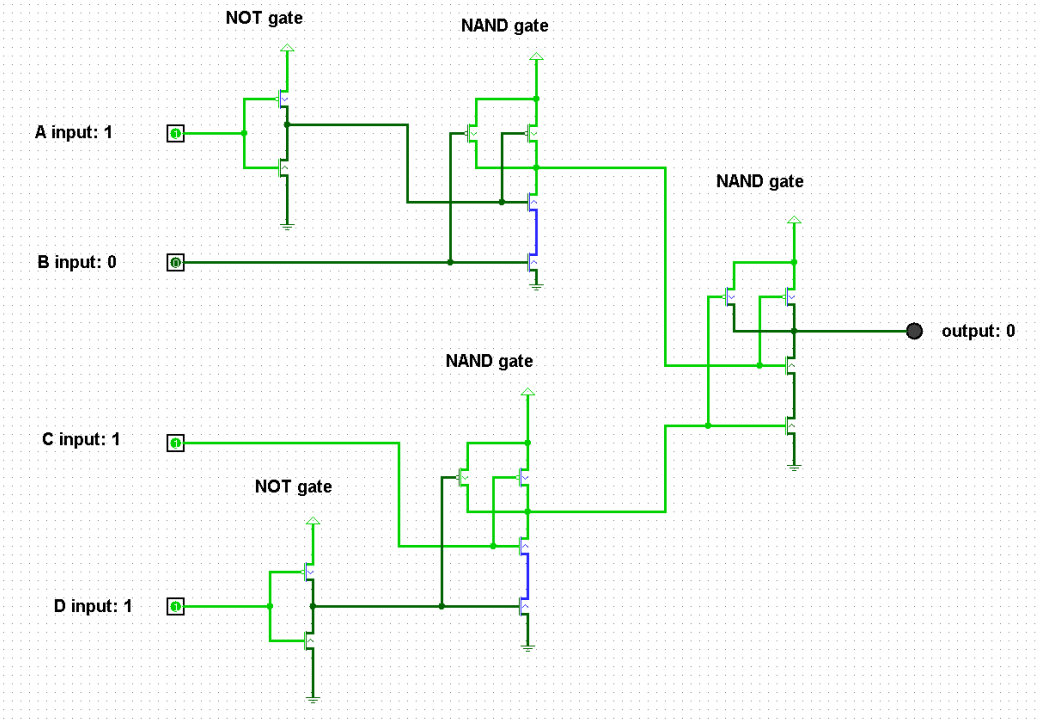
xi. A input: 1 C input: 1 Output: 1

B input: 0 D input: 0



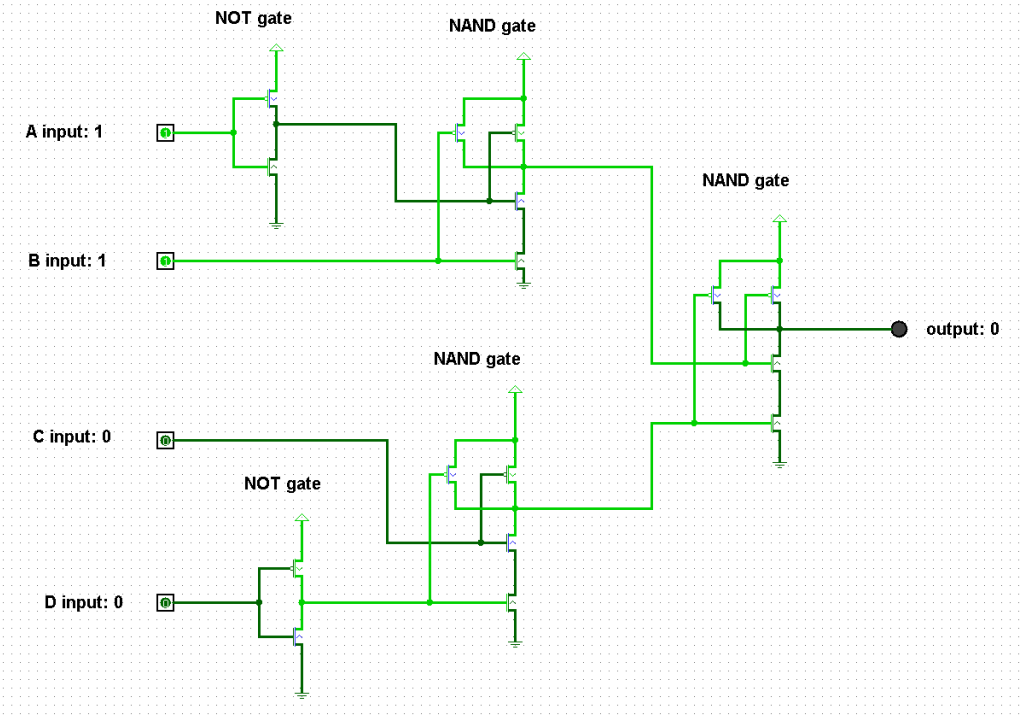
xii. A input: 1 C input: 1 Output: 0

B input: 0 D input: 1



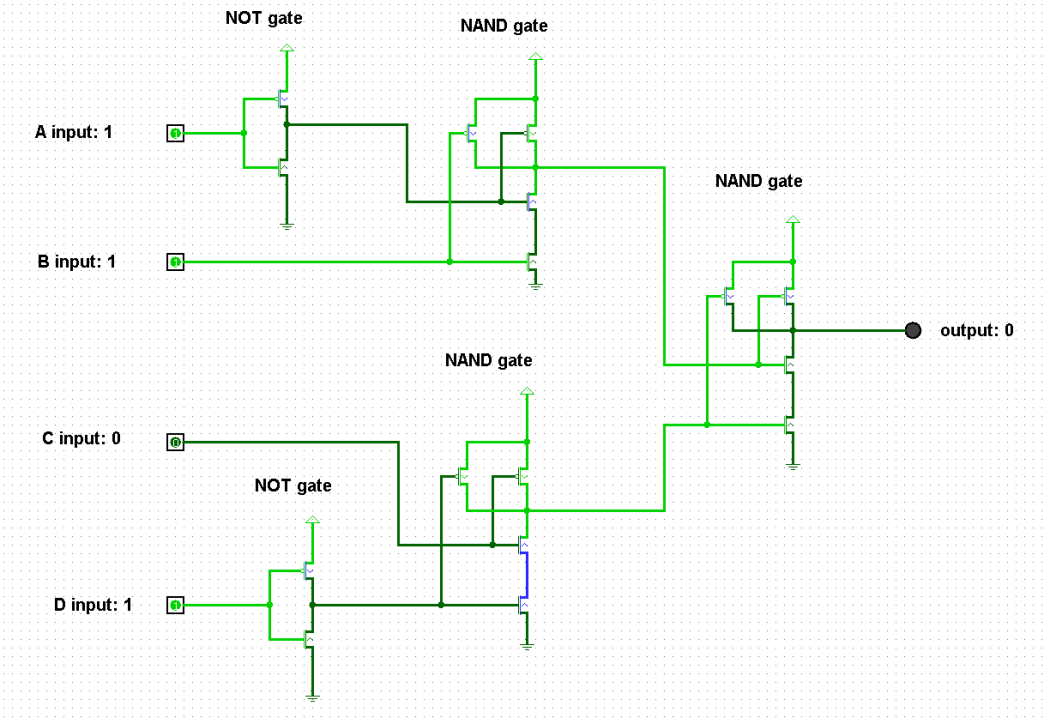
xiii. A input: 1 C input: 0 Output: 0

B input: 1 D input: 0



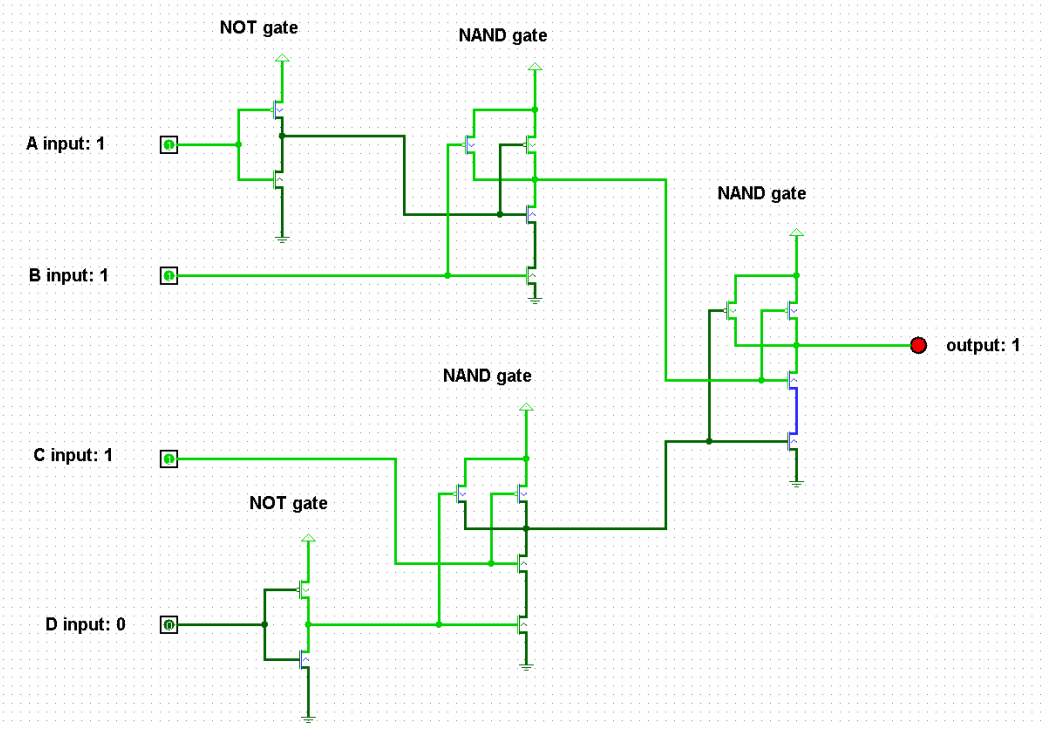
xiv. A input: 1 C input: 0 Output: 0

B input: 1 D input: 1



xv. A input: 1 C input: 1 Output: 1

B input: 1 D input: 0



xvi. A input: 1 C input: 1 Output: 0

B input: 1 D input: 1