# nanoML for Human Activity Recognition

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#### **ABSTRACT**

Human Activity Recognition (HAR) is critical for applications in healthcare, fitness, and IoT, but deploying accurate models on resource-constrained devices remains challenging due to high energy and memory demands. This paper demonstrates the application of Differentiable Weightless Neural Networks (DWNs) to HAR, achieving competitive accuracies of 96.34% and 96.67% while consuming only 56nJ and 104nJ per sample, with an inference time of just 5ns per sample. The DWNs were implemented and evaluated on an FPGA, showcasing their pratical feasibility for energy-efficient hardware deployment. DWNs achieve up to 926,000x energy savings and 260x memory reduction compared to state-of-the-art deep learning methods. These results position DWNs as a nano-machine learning (nanoML) model for HAR, setting a new benchmark in energy efficiency and compactness for edge and wearable devices, paving the way for ultra-efficient edge AI.

#### **KEYWORDS**

nanoML, human activity recognition, energy-efficient machine learning, weightless neural networks

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# 1 INTRODUCTION

Human activity recognition (HAR) is a pivotal area of research with applications spanning healthcare, fitness, and workplace monitoring. By enabling the automated identification of activities such as walking, running, or sitting, HAR systems have significantly enhanced our ability to monitor and improve human health and well-being. These advancements are particularly valuable in healthcare, where HAR plays a critical role in early disease detection, rehabilitation monitoring, and elder care. Furthermore, HAR facilitates the development of personalized fitness programs and ensures

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workplace safety by monitoring posture and movement patterns. With the rapid proliferation of digital health solutions, the demand for accurate, efficient, and scalable HAR systems has grown exponentially.

Wearable devices, such as smartwatches, fitness bands, and IoT-enabled sensors, serve as the primary platforms for HAR. These devices are equipped with sensors like accelerometers and gyroscopes, which continuously collect rich data streams about users' activities. However, the constrained hardware capabilities of wearables pose significant challenges, especially in terms of energy efficiency. As wearables are often battery-powered and expected to operate for extended periods without frequent charging, developing low-energy models for HAR becomes crucial. Energy-efficient models not only extend device battery life but also enable seamless, real-time activity recognition, ensuring their adoption in resource-constrained environments.

Several recent models for HAR have demonstrated impressive accuracy [9–11, 13, 14], leveraging advancements in deep learning and other machine learning approaches. These models, however, often rely on architectures with massive computational demands, requiring millions of floating-point operations (FLOPs), or computationally expensive preprocessing steps. Unfortunately, these energy-intensive aspects are frequently overlooked or insufficiently addressed in the presentation of results, creating a disconnect between reported performance and their practical deployment on resource-constrained wearable devices. The mismatch between the energy-efficient hardware of edge devices and the computational needs of these models poses a significant barrier to their widespread adoption in real-world applications.

Recently, Differentiable Weightless Neural Networks (DWNs) have emerged as a promising solution for edge devices [4], offering energy-efficient models. DWNs are capable of performing inference with minimal energy consumption—often measured in nanojoules (nJ)—and executing in just nanoseconds (ns). While DWNs have demonstrated significant potential in other domains, their application to human activity recognition has not yet been explored.

In this paper, we address the critical gap in energy-efficient HAR solutions by showcasing DWNs as a nano-machine learning approach for human activity recognition (HAR). We demonstrate their ability to achieve accurate recognition with extremely low energy consumption, deploying them on FPGA and highlighting their performance for edge devices. Additionally, we estimate the energy costs of recent state-of-the-art convolutional neural networks (CNNs) [10, 14] and Transformers [9, 13]. By comparing

these implementations to DWNs, this work not only underscores the potential of DWNs for HAR but also paves the way for further exploration of ultra-efficient models for edge AI applications.

The remainder of the paper is organized as follows - Section 2 introduces existing Deep Neural Network based works on Human Activity Recognition, and Section 3 introduces DWNs. In Section 4 we elucidate our experimental methodology and results, and Section 5 concludes the paper.

# 2 DEEP NEURAL NETWORKS MODELS FOR HUMAN ACTIVITY RECOGNITION

Deep neural networks (DNNs) have been extensively explored for human activity recognition (HAR), spannig various architectures, including multi-layer perceptrons (MLPs), Convolutional Neural Networks (CNNs), Transformers, and Hybrid Models. While DNNs have achieved high accuracy on benchmark datasets, including UCI-HAR, their practical deployment on wearable devices remains challenging due to their reliance on computationally expensive preprocessing pipelines and hardware-intensive architectures.

# 2.1 Preprocessing in Neural Network-Based HAR

Many HAR approaches rely on extensive preprocessing steps to extract high-level statistical and spectral features from raw sensor signals. Commonly used features include mean, standard deviation, energy, entropy, and correlation, alongside frequency-domain representations obtained via Fast Fourier Transform (FFT) or wavelet transforms. These preprocessing steps enhance the input data's representation for neural network models, enabling superior accuracy but at a substantial computational cost. For instance, FFT operations require  $O(N\log N)$  complexity, which is resource-intensive for edge devices like FPGAs and ASICs. Similarly, the calculation of entropy and correlation involves non-linear operations that are impractical for real-time, low-power environments.

The UCI-HAR dataset [2, 8], a widely used benchmark, exemplifies this dependency on preprocessing. The highest reported accuracy for CNNs on UCI-HAR, 97.62%, is achieved by elaborate preprocessing pipelines [11]. While effective, such approaches are unsuitable for edge deployment due to their significant preprocessing and computational overhead.

#### 2.2 State-of-the-art Models

Recent studies have demonstrated the feasibility of deploying HAR models directly on raw sensor data without preprocessing. For instance, CNNs applied to raw UCI-HAR data achieved an accuracy of 96.27% [14]. However, this approach incurs a significant computational cost, requiring 33.7 million floating-point operations (FLOPs) per inference. This substantial demand translates to high energy consumption, as quantified in the experimental section of this paper. These findings highlight the trade-off between eliminating preprocessing and managing model complexity, underscoring the need for lightweight, energy-efficient alternatives for resource-constrained environments.

In addition to CNNs, transformers have been explored for HAR due to their ability to model long-term dependencies in sequential

data. HARMamba, a transformer-based model, achieved a state-of-the-art accuracy of 97.65% on UCI-HAR by leveraging self-attention mechanisms [13]. However, the model still relies on some preprocessing, and its large parameter count and complex operations result in significant energy and memory requirements, limiting its suitability for edge devices. Similarly, TSLANet, another transformer-based architecture, tailored for time series, achieved 96.06% accuracy [9]. Despite their strong performance, transformer models remain computationally intensive, necessitating millions of FLOPs per inference. These challenges underscore the demand for more energy-efficient architectures to meet the constraints of edge and wearable devices.

# 3 DIFFERENTIABLE WEIGHTLESS NEURAL NETWORKS (DWN)

Weightless Neural Networks (WNNs) [1] are a class of neural architectures that uses lookup tables (LUTs) as neurons instead of weighted connections and dot products used by DNNs. The expressive power of a neural network neuron is characterized by its Vapnik-Chervonenkis (VC) dimension, which quantifies the model's capacity to distinguish complex patterns. Notably, the VC dimension of a LUT scales exponentially with the number of inputs *n*, as  $2^n$  [7], whereas, for a conventional deep neural network (DNN) neuron with n inputs, the VC dimension is limited to n + 1. For example, to accurately model a simple XOR pattern of 2 bits, a WNN requires only one LUT with 4 entries. In contrast, a DNN would need 3 neurons, resulting in 6 weights and 3 biases, totalizing 9 parameters. This stark difference highlights the efficiency of LUT-based models in representing complex patterns within a single computational unit compared to the relatively parameter-intensive approach of DNNs.

Despite their theoretical advantages, traditional WNNs have primarily been confined to single-layer architectures and random connections of inputs to LUTs. This limitation arises from the non-differentiable nature of LUTs, which has historically posed challenges for gradient-based optimization techniques, impeding the development of multi-layer architectures.

Recently, Differentiable Weightless Neural Networks (DWNs) [4] have been proposed to address this limitation by introducing differentiability to LUT-based architectures, thereby enabling the training of multi-layer WNNs. These networks achieve up to a  $286\times$  reduction in energy costs and a  $60\times$  reduction in latency compared to FINN [15], the state-of-the-art Binary Neural Network (BNN) framework, under iso-accuracy scenarios.

#### 3.1 DWN Architecture and Training

DWN architecture is built entirely from LUTs, routing connections, and a final population count (popcount) operation.

As illustrated in Figure 1, DWNs operate on binary inputs, which are routed to form the addresses for the first layer of LUTs. Each LUT indexes trainable binary values corresponding to these addresses, producing binary outputs. These outputs serve as inputs for the next layer, propagating through the network without any intermediate arithmetic operations. The outputs from the final layer of LUTs are aggregated using a popcount operation, which calculates the total

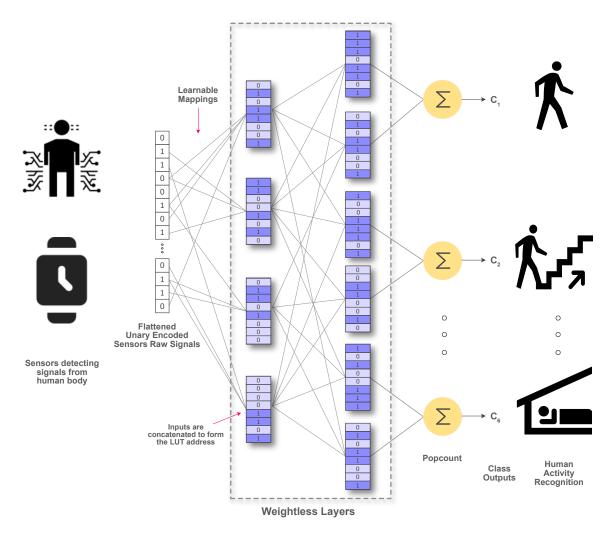


Figure 1: A simple example of a DWN with two layers of LUT-3s. DWNs compute entirely using multiple layers of directly chained lookup tables. Input features are concatenated to form addresses for the first-layer LUTs, whose binary outputs are combined to address the LUTs in subsequent layers. The outputs of the final layer are aggregated to produce activations for each class, without any intermediate arithmetic operations.

number of binary "1s" across the outputs. This aggregated value determines the activations for each class.

To address the challenge of training discrete LUT-based networks, DWNs propose the Extended Finite Difference (EFD) technique. EFD introduces differentiability to LUTs by approximating gradients for the discrete entries and indexing operations within the tables. This enables LUT values to be optimized through gradient-based learning, allowing DWNs to be trained end-to-end like traditional neural networks.

Another critical innovation of DWNs is the concept of Learnable Mapping, which enables the connections between inputs and LUTs, and between layers of LUTs, to be learned during training. Importantly, these learned connections are fixed at inference time, introducing no additional overhead as routing becomes a static

design. This ensures that DWNs remain computationally efficient during deployment.

The minimalistic design of DWNs—comprising LUTs, routing, and a final popcount operation—makes them highly suitable for hardware implementation. On FPGAs, LUTs directly map to hardware primitives, and routing leverages the programmable interconnects of the device. On ASICs, the simplicity of DWNs ensures a compact design with minimal area and power requirements. These characteristics enable DWNs to achieve real-time inference in energy-constrained environments, such as wearable devices and IoT applications.

## 3.2 Thermometer Unary Encoding

Weightless Neural Networks (WNNs) require binary inputs, making the method of binarizing continuous sensor data critical for

performance [12]. Among the available strategies, thermometer encoding is the state-of-the-art approach.

Thermometer encoding [3, 6] represents numerical values as unary binary vectors, where the number of consecutive "1s" corresponds to the magnitude of the value. For instance, a reading of 3 in a range of 5 would be encoded as '[1, 1, 1, 0, 0]'.

Importantly, thermometer encoding is not part of the DWN model itself and can be implemented directly at the sensor level. This allows the sensor to output thermometer-encoded binary values, avoiding additional binarization steps. Its simplicity and lightweight implementation make it an ideal choice for deployment on resource-constrained hardware. Furthermore, sensors designed to output thermometer-encoded values need only recognize a small, discrete set of values rather than full precision (e.g., FP32), significantly reducing sensor complexity and cost.

#### 4 EXPERIMENTAL EVALUATION

#### 4.1 Dataset Description

The UCI Human Activity Recognition (HAR) Dataset [2] is a widely used benchmark for evaluating human activity recognition models. The dataset was collected from 30 participants aged between 19 and 48 years as they performed six basic activities: walking, walking upstairs, walking downstairs, sitting, standing, and lying down. Each participant carried a smartphone (Samsung Galaxy S II) on their waist, which recorded sensor data from a 3-axis accelerometer and a 3-axis gyroscope.

Raw Signals. The raw sensor data consists of 128 samples per activity segment, corresponding to a window of 2.56 seconds sampled at 50 Hz. These raw signals capture the accelerometer and gyroscope readings along three spatial axes (X, Y, Z), providing a direct representation of the participants' movements.

Hand-Crafted Features. In addition to the raw signals, the dataset includes 561 hand-crafted features derived from the time and frequency domains. These features, used by many traditional models, include statistical metrics such as mean, standard deviation, skewness, and kurtosis, as well as frequency-domain features obtained via the Fast Fourier Transform (FFT). While these features enhance the representational power of the data, their extraction is computationally and energetically expensive, posing significant challenges for deployment on hardware-constrained wearable devices.

In this work, we deploy our model exclusively on the raw 128-sample signals, excluding the hand-crafted signals and without using any preprocessing on the signals. By eliminating the need for feature extraction, we demonstrate the feasibility of achieving accurate human activity recognition while adhering to the strict energy constraints of real-world wearable devices.

Data Splits. The dataset is pre-divided into training and testing sets in an inter-patient fashion, where data from 70% of the participants are used for training, and the remaining 30% are reserved for testing. This ensures that the model is evaluated on entirely unseen participants, providing a robust assessment of its ability to generalize to new users.

### 4.2 Thermometer Encoding

Each of the 9 raw sensor signals in the dataset is converted to unary encoding using a 20-bit Distributive Thermometer Encoding scheme [3], as described in section 3.2.

# 4.3 Model Configurations and Training Details

To identify the optimal DWN configuration, we split the training set into a training subset (80% of the training data) and a validation subset (20%) for hyperparameter search and Neural Architecture Search (NAS). The search explored the following ranges:

- Number of Layers: [1, 2, 3, 4]
- LUT Size: [2, 3, 4, 5, 6, 7, 8]
- Softmax Temperature  $(\tau)$ :  $\left[\frac{1}{0.5}, \frac{1}{0.3}, \frac{1}{0.1}, \frac{1}{0.05}, \frac{1}{0.03}, \frac{1}{0.01}\right]$

The best-performing architecture consists of a single layer of LUT-4 with a softmax temperature of  $\tau = \frac{1}{0.03}$ .

4.3.1 Data Augmentation. To enhance generalization, we applied a range of standard 1D signal augmentations to the training data. Each augmentation was applied with a probability of p=0.3, including:

- Time Shift: Randomly shifts signals along the time axis by up to 10 steps.
- Scaling: Multiplies signals by a random scaling factor uniformly sampled from [0.9, 1.1].
- Jitter: Adds Gaussian noise with a standard deviation of 0.05 to simulate signal variability.
- **Time Masking**: Masks a random section of the signal (up to 10 time steps) by setting it to zero.
- Axis Flip: Randomly inverts one or more signal axes.
- Rotation: Applies a small rotation (up to 10°) to the first three axes, simulating spatial transformations.
- Low-Pass Filtering: Smoothens the signal using a low-pass Butterworth filter with a cutoff frequency of 20 Hz.
- 4.3.2 *Training Procedure.* The DWN was trained using the Adam optimizer with the following settings:
  - Batch Size: 100
  - Learning Rate: 0.01, decayed by a factor of 0.1 every 14 epochs.
  - Total Training Epochs: 32

We trained two DWN models for evaluation: one with 10,000 LUTs and another with 20,000 LUTs. The training process was conducted using the full training set, and the final models were obtained after completing all 32 epochs. This ensures the model fully leverages the available training data to achieve optimal performance.

#### 4.4 FPGA Board Deployment

We deployed the DWN models on the Xilinx XC7Z020CLG400 FPGA, operating in out-of-context mode. This configuration allows us to isolate and demonstrate the model's computational capabilities independently of specific data transfer constraints. We write SystemVerilog RTL codes for the design using make templating scripts [5] based on the hardware architecture proposed by the authors of DWN [4]. The design is synthesized on the target FPGA using the Xilinx Vivado 2022.1 tool, with a target clock of 200 MHz.

Table 1: Comparison of state-of-the-art models for Human Activity Recognition (HAR) on the UCI-HAR dataset on the Xilinx
XC7Z020CLG400 FPGA. DWNs achieve significant energy efficiency compared to CNN and Transformer-based architectures.

Model	Accuracy	F1 Score	Model Size (KiB)	FLOPs	Energy/Sample
TSLANet [9]	96.06%	-	-	69M	52mJ
Channel-Equalization-HAR [10]	97.35%	97.12%	1600	44M	33mJ
CNN [14]	96.27%	96.27%	5100	35M	26mJ
HARMamba [13]	97.65%	97.01%	1300	11M	8mJ
DWN	96.34%	96.30%	19	0	0.000056mJ
DWN	96.67%	96.68%	39	0	0.000104mJ

This enables us to determine the maximum achievable frequency for the design by observing the reported Worst Negative Slack (WNS). The DWN architecture, implemented with pipelining, achieves one inference per clock cycle, ensuring maximal throughput under ideal conditions. Any bottlenecks in real-world deployment would arise solely from data transfer rates, not the model's computation.

We evaluate the energy consumption for DWN models by performing a vectorless power estimation of the synthesized design on our target FPGA with a default switching activity of 12.5%. We report the energy per sample inference of these models as the energy spent in operating the deployment for an amount of time corresponding to the latency of execution.

# 4.5 Energy Estimation for Other Models

To compare DWN's energy efficiency with other models, we estimated the energy consumption of prior work based on the FLOP counts reported in their respective papers. We consider Verilog-based RTL designs for individual floating-point operation units and synthesize these on the same target Xilinx XC7Z020CLG400 FPGA with Xilinx Vivado 2022.1 to report vectorless power estimation for a 12.5% switching activity. With this approach, the energy per floating-point operation (FLOP) on the FPGA was determined as:

- Multiplication (FP32): 0.928nJ
- Addition (FP32): 0.594nJ

On average, a FLOP in neural network architectures involves roughly equal proportions of multiplications and additions, as a DNN neuron with n inputs performs n multiplications and n additions. Using this assumption, we estimated the energy per FLOP as the average of the two operations: 0.761nJ.

The total energy consumption of other models was calculated by multiplying the reported FLOP counts from their respective papers with this estimated energy per FLOP. It is important to note that we do not know whether the reported FLOP counts include only the model computations or also account for any preprocessing steps required for those architectures. If preprocessing FLOPs are excluded, it puts these models at an advantage over DWNs in our comparison.

#### 4.6 Results

The application of Differentiable Weightless Neural Networks (DWNs) to Human Activity Recognition (HAR) underscores their unparalleled energy efficiency and suitability for edge deployment compared to state-of-the-art methods.

Accuracy and Energy Efficiency. The DWN models achieve accuracies of 96.34% and 96.67%, closing the gap with the state-of-theart HAR methods while consuming just 56nJ and 104nJ per sample. These energy consumption levels represent a dramatic 77,000x to 926,000x reduction compared to other models, which require between 8mJ and 52mJ per inference.

Model Size and Compactness. The DWN models are significantly smaller than traditional state-of-the-art solutions. With sizes of 19.5KiB and 39.1KiB, they achieve a 33x to 260x reduction compared to models such as CNN and HARMamba, which range from 1.3MiB to 5.1MiB. This compactness, combined with their hardware-friendly design, supports their deployment on resource-constrained devices.

Hardware Performance. Unlike traditional neural networks, DWNs operate without any floating-point operations (FLOPs). Instead, they rely entirely on LUTs, routing, and a final population count (popcount) operation, which drastically reduces computation overhead. The DWN models perform **one inference per clock cycle**, resulting in a total processing time of **5ns per sample** on the Xilinx XC7Z020CLG400 FPGA, running at **199MHz**. This fully pipelined design ensures consistently low inference times, further emphasizing their potential for real-time HAR applications.

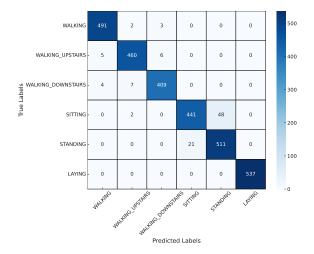
## 5 CONCLUSION AND FUTURE WORK

This study demonstrates that Differentiable Weightless Neural Networks (DWNs) embody the principles of nano-machine learning (nanoML), achieving unprecedented levels of energy efficiency and compactness in Human Activity Recognition (HAR). DWNs deliver competitive accuracies of 96.34% and 96.67% while consuming just 56nJ and 104nJ per sample, setting a new benchmark for energy-efficient HAR systems.

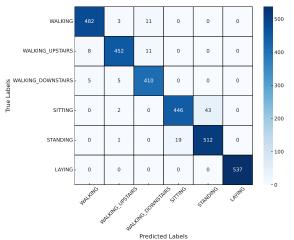
In comparison to state-of-the-art models, DWNs achieve up to 926,000x energy savings and a 260x reduction in memory size, while maintaining low latency with a processing time of 5ns per sample. Furthermore, DWNs can be directly converted into logic

Table 2: Detailed performance of DWNs for HAR on the Xilinx XC7Z020CLG400 FPGA deployed in out-of-context mode. The 'Time/Sample' metric is calculated as the reciprocal of throughput, and 'Latency' represents the end-to-end processing time of the model.

Model	Accuracy	Model Size	#LUTs	#FFs	FMax	Latency	Time/Sample	Energy/Sample
DWN	96.34%	19.5KiB	20444	13948	199MHz	40ns	5ns	56nJ
DWN	96.67%	39.1KiB	41252	27861	199MHz	45ns	5ns	104nJ



#### (a) Confusion matrix for the DWN model with a F1 of 96.30%



(b) Confusion matrix for the DWN model with a F1 of 96.68%

Figure 2: Confusion matrices for Differentiable Weightless Neural Network (DWN) models evaluated on the UCI-HAR dataset.

gates [4] and implemented as custom ASICs, making them ready for immediate integration into wearable devices.

Future work will investigate the extension of DWNs to multimodal sensor data and explore their scalability for more complex HAR scenarios. Additionally, efforts will focus on designing custom ASICs for DWNs to further enhance their efficiency in wearable applications, optimizing DWNs for diverse hardware platforms, and expanding their applications beyond HAR.

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