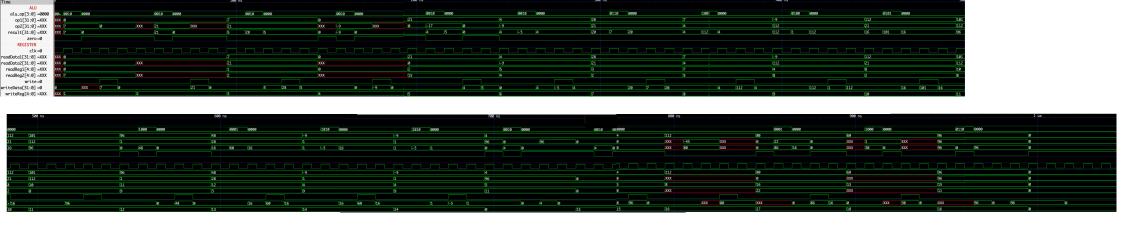


| | 3 | | | | | | | | 100 n | 15 | | | | | | | | | 200 | ıs | | | | | | | | 3 | 00 ns | | | | | | | | | 400 n | 5 | | | | | | |
|---------------------------------|------------|--|------------------------------|----------|-------------|--------------|------------|-------|--------|-----------|---------------------------|----------|---------|----------|-------------------------------|-----------|---------|--------|-----------|-----------|--------------------------------|----------|---------|------------|---|--|-------|---------|--|----------|------------|------|------------|----------|---|---|---------|--------|------------|--|----------|----------|--------------|------------|-----------|
| DATAPATH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ALUCtrl[3:0] =0 | 6 00+ 0010 | 9966 | | | 98 | 10 0000 | | | | 9919 | 6666 | | | | 0010 | 6669 | | | | 9919 | 8888 | | |) | 9919 | 0000 | | | 0110 | 90 | 800 | | | 100 | 0000 |) | | | 8166 | 8888 | | | (8) | 181 (8 | 999 |
| ALUSrc => | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| EX_MEM[31:0] =0 | Ø XXX | 7 | 0 | | | 21 | 0 | | |)5 | 28 |)5 | | | 0 | (-9 | 8 | | | | 4 |)5 | 8 | | \$ | -5 / / | 1 | | 20 |)7 | 20 | | | + | 112 |)4 | | | 112 | 1 | 112 | |)16 | 6 (1) | .01)1 |
| MEM_WB[31:0] =0 | | XXX | 7 | 9 | | | 21 | Ø | | | /5 | 28 | 5 | | | 0 | -9 | 0 | | | | 4 |)5 | 0 | | 4) | -5 4 | | | 26 | 7 | 20 | | |)4 | 112 | 4 | | | 112 |)1 | 112 | | (1) | .6)1 |
| MemToReg =€ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PCSrc =€ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PC[31:0] =0 | | | | 99499984 | | | | 98480 | 8000 | | | | 0840000 | | | | | 084006 | 910 | | | | 8848881 | 4 | | |)(| 6400018 | | | | 98 | 40001C | | | | 0840002 | 3 | | | | 00400024 | | | |
| RegWrite =€ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BackData[31:0] =0 | | XXX | 7 | 9 | | | /21 | 9 | | | /5 | 28 | 5 | | | 0 | /-9 | 0 | | | | 4 |)5 | 0 |) | 4) | -5)4 | | | 26 | 7 7 | 28 | | | 4 | 112 |)4 | | | 112 |)1 | 112 | | (1) | .6)1 |
| Zero=€ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| alu_op1[31:0] => | | | | | | | | | /7 | | | | | 0 | | | | | 21 | | | | |)4 | | | | 28 | | | | | 7 | | | | |)-9 | | | | | 112 | | |
| alu_op2[31:0] => | | | 0 | | XXX 21 | | XXX | | 21 | | | | | XXX | -9 | | XXX | | 0 | /-17 | | 0 | |)-9 | | | | 21 | | | | | | | | | | 112 | | | | | 21 | | |
| _result[31:0] => | | | | |)21 | | | | /5 | 28 | (5 | | | 0 | (-9 | 0 | | | | 4 | | 0 | | | -5 | 4 | | 20 | 7 | 26 |) | | | 113 | 4 | | | 112 | (1 | 112 | | | 16 10 | ð1 (1) | 6 |
| clk=€ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| currentPC[31:0] =0 | | | | 00400004 | | | | 99490 | 8000 | | | | 0840000 | | | | | 084006 | 010 | | | | 0040001 | 4 | | | | 0400018 | | | | 00 | 40001C | | | | 0040002 | 0 | | | | 00400024 | | | |
| dAddress[31:0] =0 | | 7 | (0 | | | /21 |)Ø | | |)5 | 28 |)5 | | | 8 | (-9 |)8 | | | | |)5 |)8 | ^ | (| -5 / | | | 20 |)7 | 20 | | | |)112 |)4 | | | 112 | <u>,1</u> | 112 | |)16 | 6 (1) |)1)1 |
| ReadData[31:0] => | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 7.0 | | | | | | | |
| riteData[31:0] => | | | | | XXX | | | | 21 | | 000000000 | | | XXX | | | | | | | | | | <u>, 9</u> | | 0000000000 | | /21 | | | | | | | | 000000000000000000000000000000000000000 | | 112 | | 00000000000 | | | Z1 | | |
| imm[31:0] => | | | | | | | | | 000000 | 00000000 | 10000000000 1000001000 | 00000010 | | | 1111111111 | | | | | | 11111111111 | | | 00000000 | ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,, | 000000000 | 00100 | | 9999999999 | | | | ,000 | | | 900000000101 90000001000 | | | | 9000000000000 90000010000 | | | 000000000000 | | |
| imm_B[31:0] => imm_I_L[31:0] => | | | 198698888888 198698819988 | | 99999999999 | 000000000000 | | | | | 10000001000 | | | | 1111111111111 111111111111 | | | | | | 1111111111111 1111111111111 | | | | | 0000000000 000000000 | | | 9969999999 | | | | | | | 900000001000 90000000100 | | | | 99999999999999999999999999999999999999 | | | 00000000000 | | |
| imm_S[31:0] => | | 30000000000000000000000000000000000000 | | | | 000000000000 | | | | | 000000000 | | | | 111111111111 | | | | | | | | | | | 000000000 | | | 00000000000 | | | | | | | 90000000001000 900000001000 | | | | 100000000000 1000000000000 | | | | 2002000000 | |
| instr[31:0] => | | | | 0000000 | 0000000000 | | 000000000 | | 000000 | 00000000 | 010000000 | 00000011 | | | 1011100000 | | | | | | 1000000101 | | | | | 60000000000000000000000000000000000000 | | | 00000000000000000000000000000000000000 | **** | | | ,000 | 0000000 | ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,, | 1000011001 | | | | 10001001001 | | | 00000000000 | 00000000 | |
| loadPC => | | 00000111000 | 000000000 | 10010011 | 00000001010 | 10000000000 | 0100010011 | | 000000 | 000010000 | 010000001 | 10110011 | | ,1111111 | 1011100000 | ACOUCOTOR | 0010011 | | A (11111) | 101111000 | 1000000101 | .0010011 | | 000000000 | 100001010 | 000011001 | 10011 | 01 | 00000000100 | 00011000 | 9001110110 | 1011 | 000 | coocoao. | 1001110010. | 10000110011 | | 000000 | 3010000010 | 000100100 | 10110011 | | 30000000001 | 100100010 | 001010011 |
| readData1[31:0] => | | | | | | | | | /7 | | | | | a | | | | | (21 | | | | | Ya | | | | 95(| | | | | 17 | | | | | Y_9 | | | | | 112 | | |
| readData2[31:0] => | | | | | XXX | | | | 21 | | | | | XXX | | | | | 0 | | | | | /-9 | | | |)21 | | | | | 7 <u>4</u> | | | | | 112 | | | | | 21 | | |
| readReg1[4:0] => | | | | | 7000 | | | | /1 | | | | | a | | | | | 2 | | | | |), | | | |)3 | | | | | 7 | | | | | 14 | | | | | 8 | | |
| readReg2[4:0] => | | | | | XXX | | | | 2 | | | | | XXX | | | | | (15 | | | | | 4 | | | |)2 | | | | | 15 | | | | | 8 | | | | | 2 | | |
| rst=1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| writeReg[4:0] => | | | | | 2 | | | | 13 | | | | | A | | | | | 15 | | | | | \6 | | | | 17 | | | | | /8 | | | | | 9 | | | | | 10 | | |

| XXXX 1 | | | /2 | |)3 | | | | | (4 | | | | (5 | | | |)6 | | | |)7 | | | | /8 | | | | |)9 | | |
|---|-------------|-----|------------|--|---------|---------|------------------------------|------|----|----------|--------------|------|-----|----------|----------|---------------|-----|----------|--------------------------|--------|-----|----------|-------------|---------|----|--------|-----|------|----------------------------|-----|----------|------|--|
| | | | | 500 ns | | | | | | | 00 ns | | | | | | | | 700 ns | | | | | | | | 800 | or. | | | | | |
| | | | | | | | | | | | | | | | | | | | 100 113 | | | | | | | | 000 | | | | | | |
| 0000 0101 | 6666 | | | | | | 1999 | 9966 | | | 0001 | 8888 | | | | 810 0000 |) | | .00 | 10 000 | 3 | | 00 | 10 0000 | , | | | | | | | 98 | 0000 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 112 16 | |)16 | |)96 | | | | | 0 | | 16 | | (16 | |)1 | .)-5 | (1 | | 0 | /4 | 0 | | | 4 | 0 | | | XXX | | | XXX | 9 | ,86 |
| 112 | (16 | 101 | 16 |)96 | | | | 9 | 48 | 0 | | 16 | 60 | 16 | |)1 | (-5 |)1 | | 0 | | 0 | | | | (0 | | | XXX | 80 | | XXX | 0 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00400024 | | | 00400028 | | 0040002 | c | | | | 00400030 | | | | 00400034 | | | | 00400038 | | | | 9849883C | | | | 894699 | 148 | | | | 99499944 | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ١ |
| 112 | (16 | 101 | 16 | 96 | | | | 9 | 48 | 0 | | (16 | 60 | 16 | |)1 | (-5 |)1 | |)8 | /4 | 9 | | | 96 | (0 | | | XXX | 80 | | XXX | (e) |
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| 7,10 ,101 | , <u>10</u> | | | | | | ,40 | , e | | 7,10 | ,00 | ,10 | | | | | | | | | | | | | | | *** | - 00 | | | | 0 80 | |
| 00400024 | | | 00400028 | | 9849882 | c | | | | 00400030 | | | | 00400034 | | | | 00400038 | | | | 0040003C | | | | 004000 | 148 | | | | 98499844 | | |
| 112 16 | 101 |)16 | |)96 | | | 8 | 48 | 0 | | /16 | 60 | (16 | | (1 |)-5 | (1 | | 0(| /4 | 0 | | | /4 | 0 | | | XXX | 80 | | XXX | 0 | (86 |
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| + 000000000010010 | | | | 0000000100001010111010110110 | | | 010010101 | | | | 000000001101 | | | | | 01001001010 | | | 80000000101 | | | | 89869869868 | | | | | | 00011110000 | | | | 9100001101000100 |
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| 8)2 | | | 8 | | |)9 | | | | 3 | | | | |) | | | | 11 | | | | 0 | | | | XXX | | | | | 22 | |
| 0/10 | | | X1: | | | 112 | | | |)13 | | | | | 14 | | | | а | | | | 15 | | | |)16 | | | | | 17 | |
| 3/10 | | | Ņž. | | | - Maria | | | | 1.3 | | | | | | | | | | | | | 120 | | | | -20 | | | | | 100 | |





Συμπεράσματα

Οι κυματομορφές έχουν την αναμενόμενη μορφή, γεγονός που σημαίνει ότι ο επεξεργαστής λειτουργεί κανονικά. Οι καταστάσεις αλλάζουν όπως πρέπει και τα αποτελέσματα της ALU αποθηκεύονται στην σωστή θέση κάθε φορά.

Οι στόχοι περιλάμβαναν τη δημιουργία και τη σύνδεση των βασικών μονάδων του επεξεργαστή, όπως ο καταχωρητής του προγράμματος (PC), το αρχείο καταχωρητών, η μονάδα αριθμητικής λογικής (ALU), η γεννήτρια άμεσων τιμών $(Immediate\ Generation)$ και η μονάδα μνήμης. Ο επεξεργαστής σχεδιάστηκε για να εκτελεί τις βασικές εντολές του RISC-V, περιλαμβανομένων των εντολών καταχωρητή-καταχωρητή, καταχωρητή-άμεσης τιμής, εντολών μνήμης, καθώς και των εντολών διακλάδωσης. Το σύστημα αναπτύχθηκε χρησιμοποιώντας μία αρχιτεκτονική με πολλαπλά στάδια εκτέλεσης, και περιλαμβάνει τις φάσεις της εντολής, αποκωδικοποίησης, εκτέλεσης, μνήμης και της εγγραφής. Η σωστή λειτουργία του επεξεργαστή διασφαλίστηκε μέσω της υλοποίησης των απαραίτητων σημάτων ελέγχου για κάθε φάση, και η απόδοσή του αξιολογήθηκε με τη χρήση κατάλληλων εντολών και παραμέτρων. Οι βασικές έννοιες της αρχιτεκτονικής RISC-V εφαρμόστηκαν πλήρως και το σύστημα λειτουργεί όπως απαιτείται στην εκφώνηση της άσκησης.