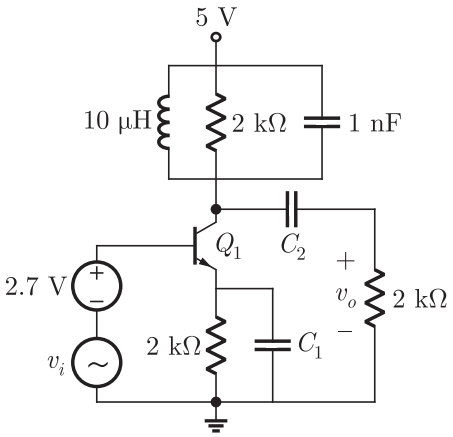
UNIT 4
Analog Circuits

2011 **ONE MARK**

MCQ 4.1

In the circuit shown below, capacitors C_1 and C_2 are very large and are shorts at the input frequency. v_i is a small signal input. The gain magnitude $\left|\frac{v_o}{v_i}\right|$ at 10 M rad/s is



(A) maximum

(B) minimum

(C) unity

(D) zero

MCQ 4.2

The circuit below implements a filter between the input current i_i and the output voltage v_o. Assume that the op-amp is ideal. The filter implemented is a

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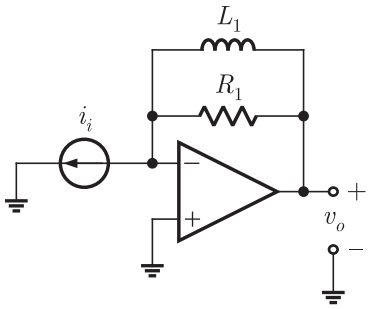
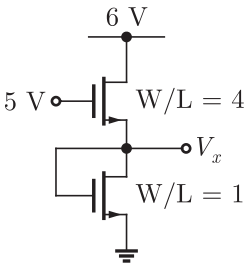


(A) low pass filter
(B) band pass filter
(C) band stop filter
(D) high pass filter

2011 TWO MARKS

MCQ 4.3

In the circuit shown below, for the MOS transistors, $\mu_n C_{ox} = 100\ \mu A/V^2$ and the threshold voltage $V_T = 1$ V. The voltage V_x at the source of the upper transistor is



(A) 1 V
(B) 2 V
(C) 3 V
(D) 3.67 V

MCQ 4.4

For a BJT, the common base current gain $\alpha = 0.98$ and the collector base junction reverse bias saturation current $I_{CO} = 0.6\,\mu A$. This BJT is connected in the common emitter mode and operated in the active region with a base drive current $I_B = 20\,\mu A$. The collector current I_C for this mode of operation is

(A) 0.98 mA
(B) 0.99 mA
(C) 1.0 mA
(D) 1.01 mA

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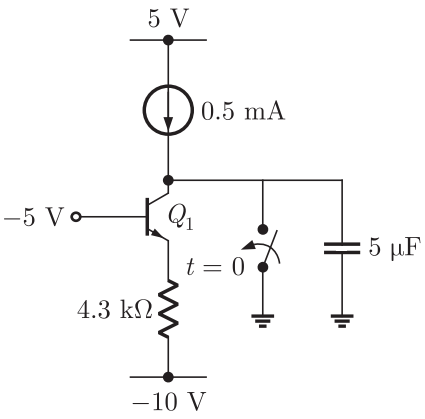
MCQ 4.5

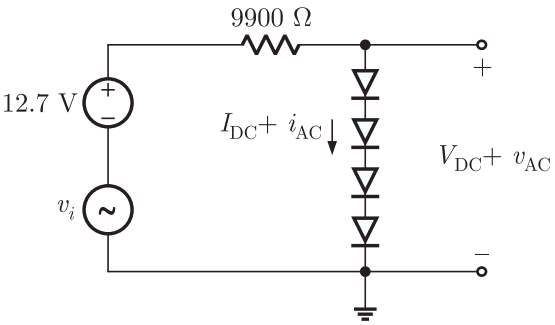
For the BJT, Q_1 in the circuit shown below, $\beta = \infty$, $V_{BEon} = 0.7$ V, $V_{CEsat} = 0.7$ V. The switch is initially closed. At time $t = 0$, the switch is opened. The time t at which Q_1 leaves the active region is



(A) 10 ms (B) 25 ms
(C) 50 ms (D) 100 ms

Statement for Linked Answer Questions: 4.6 & 4.7

In the circuit shown below, assume that the voltage drop across a forward biased diode is 0.7 V. The thermal voltage $V_t = kT/q = 25$ mV . The small signal input $v_i = V_p \cos(\omega t)$ where $V_p = 100$ mV.



MCQ 4.6

The bias current I_{DC} through the diodes is

(A) 1 mA (B) 1.28 mA
(C) 1.5 mA (D) 2 mA

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MCQ 4.7

The ac output voltage v_{ac} is

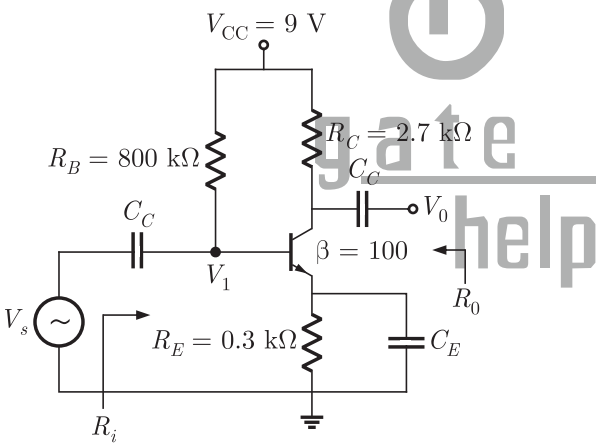
(A) $0.25\cos(\omega t)$ mV (B) $1\cos(\omega t)$ mV

(C) $2\cos(\omega t)$ mV (D) $22\cos(\omega t)$ mV

2010 **ONE MARK**

MCQ 4.8

The amplifier circuit shown below uses a silicon transistor. The capacitors C_C and C_E can be assumed to be short at signal frequency and effect of output resistance r_0 can be ignored. If C_E is disconnected from the circuit, which one of the following statements is true



(A) The input resistance R_i increases and magnitude of voltage gain A_V decreases

(B) The input resistance R_i decreases and magnitude of voltage gain A_V increases

(C) Both input resistance R_i and magnitude of voltage gain A_V decreases

(D) Both input resistance R_i and the magnitude of voltage gain A_V increases

MCQ 4.9

In the silicon BJT circuit shown below, assume that the emitter area of transistor Q_1 is half that of transistor Q_2

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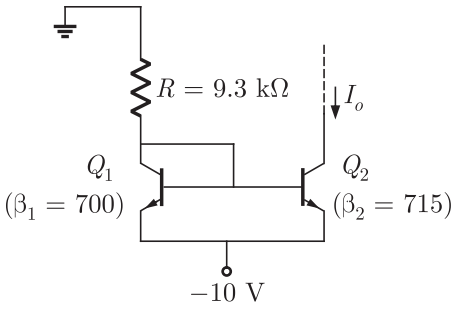


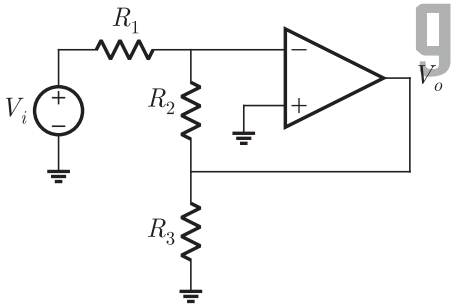
The value of current I_o is approximately

(A) 0.5 mA (B) 2 mA

(C) 9.3 mA (D) 15 mA

MCQ 4.10

Assuming the OP-AMP to be ideal, the voltage gain of the amplifier shown below is



(A) $-\frac{R_2}{R_1}$ (B) $-\frac{R_3}{R_1}$

(C) $-\frac{R_2 \,||\, R_3}{R_1}$ (D) $-\left(\frac{R_2 + R_3}{R_1}\right)$

2010 **TWO MARKS**

Common Data Questions: 4.11 & 4.12 :

Consider the common emitter amplifier shown below with the following circuit parameters:

$\beta = 100, g_m = 0.3861\ \text{A/V}, r_0 = 259\ \Omega, R_S = 1\ \text{k}\Omega, R_B = 93\ \text{k}\Omega,$

$R_C = 250\ \text{k}\Omega, R_L = 1\ \text{k}\Omega, C_1 = \infty$ and $C_2 = 4.7\ \mu\text{F}$

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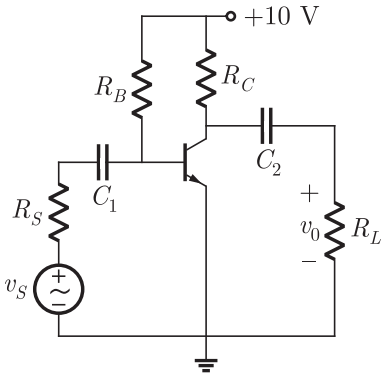


MCQ 4.11

The resistance seen by the source v_S is

(A) 258 Ω (B) 1258 Ω

(C) 93 kΩ (D) ∞

MCQ 4.12

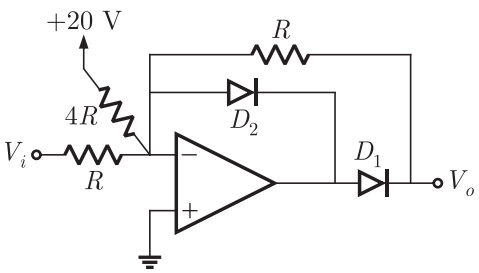
The lower cut-off frequency due to C_2 is

(A) 33.9 Hz (B) 27.1 Hz

(C) 13.6 Hz (D) 16.9 Hz

MCQ 4.13

The transfer characteristic for the precision rectifier circuit shown below is (assume ideal OP-AMP and practical diodes)



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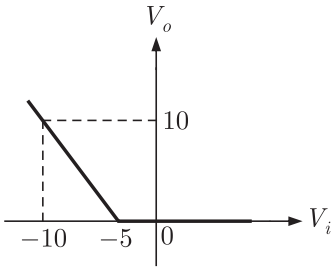
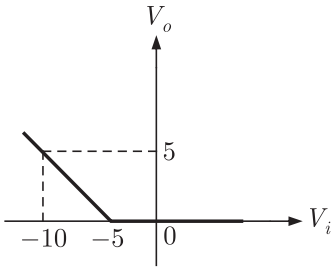
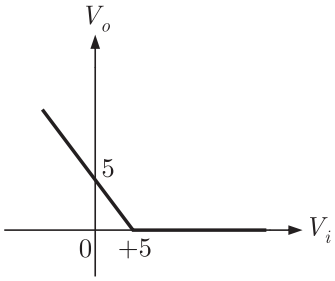
(A)



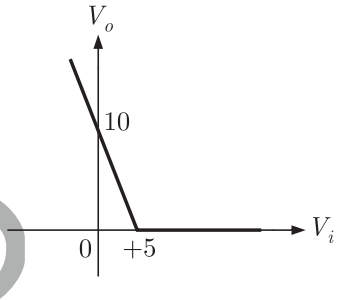
(B)



(C)



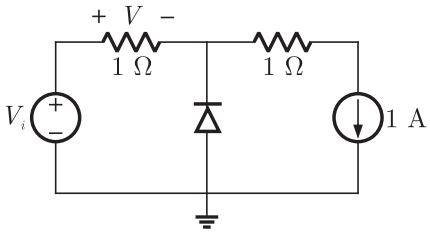
(D)



2009 **TWO MARKS**

MCQ 4.14

In the circuit below, the diode is ideal. The voltage V is given by



(A) min $(V_i, 1)$

(B) max $(V_i, 1)$

(C) min $(-V_i, 1)$

(D) max $(-V_i, 1)$

MCQ 4.15

In the following a stable multivibrator circuit, which properties of $v_0(t)$ depend on R_2?

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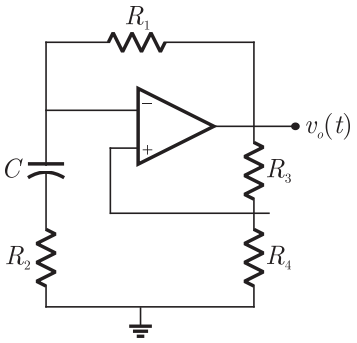


(A) Only the frequency

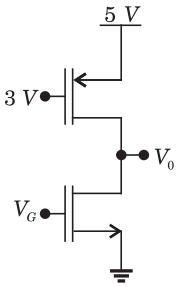
(B) Only the amplitude

(C) Both the amplitude and the frequency

(D) Neither the amplitude nor the frequency

Statement for Linked Answer Question 4.16 and 4.17

Consider for CMOS circuit shown, where the gate voltage v_0 of the n-MOSFET is increased from zero, while the gate voltage of the $p-$ MOSFET is kept constant at 3 V. Assume, that, for both transistors, the magnitude of the threshold voltage is 1 V and the product of the trans-conductance parameter is 1mA. V^{-2}



MCQ 4.16

For small increase in V_G beyond 1V, which of the following gives the correct description of the region of operation of each MOSFET

(A) Both the MOSFETs are in saturation region

(B) Both the MOSFETs are in triode region

(C) n-MOSFETs is in triode and $p-$MOSFET is in saturation region

(D) n- MOSFET is in saturation and $p-$MOSFET is in triode region

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MCQ 4.17

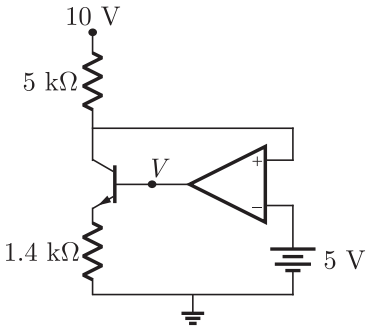
Estimate the output voltage V_0 for $V_G = 1.5$ V. [Hints : Use the appropriate current-voltage equation for each MOSFET, based on the answer to Q.4.16]

(A) $4 - \frac{1}{\sqrt{2}}$ (B) $4 + \frac{1}{\sqrt{2}}$

(C) $4 - \frac{\sqrt{3}}{2}$ (D) $4 + \frac{\sqrt{3}}{2}$

MCQ 4.18

In the circuit shown below, the op-amp is ideal, the transistor has $V_{BE} = 0.6$ V and $\beta = 150$. Decide whether the feedback in the circuit is positive or negative and determine the voltage V at the output of the op-amp.



(A) Positive feedback, $V = 10$ V. (B) Positive feedback, $V = 0$ V

(C) Negative feedback, $V = 5$ V (D) Negative feedback, $V = 2$ V

MCQ 4.19

A small signal source $V_i(t) = A\cos 20t + B\sin 10^6 t$ is applied to a transistor amplifier as shown below. The transistor has $\beta = 150$ and $h_{ie} = 3\Omega$. Which expression best approximate $V_0(t)$

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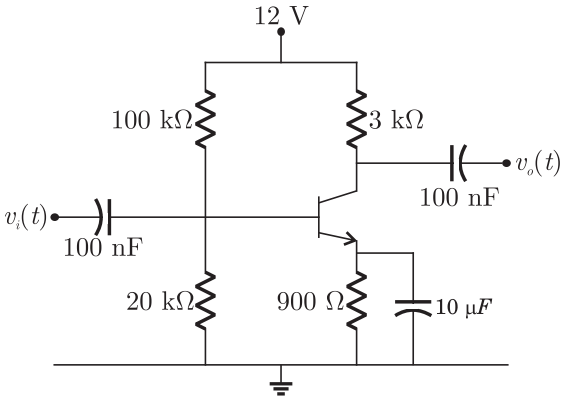


(A) $V_0(t) = -1500(A\cos 20t + B\sin 10^6 t)$

(B) $V_0(t) = -1500(A\cos 20t + B\sin 10^6 t)$

(C) $V_0(t) = -1500B\sin 10^6 t$

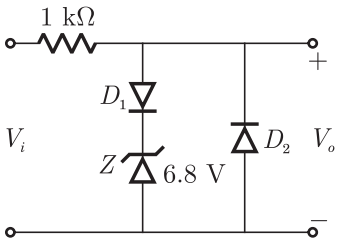
(D) $V_0(t) = -150B\sin 10^6 t$

2008 **ONE MARK**

MCQ 4.20

In the following limiter circuit, an input voltage $V_i = 10\sin 100\pi t$ is applied. Assume that the diode drop is 0.7 V when it is forward biased. When it is forward biased. The zener breakdown voltage is 6.8 V

The maximum and minimum values of the output voltage respectively are



(A) 6.1 V, – 0.7 V

(B) 0.7 V, – 7.5 V

(C) 7.5 V, – 0.7 V

(D) 7.5 V, – 7.5 V

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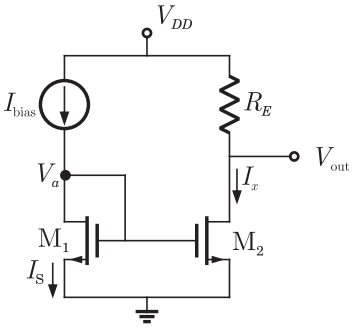
MCQ 4.21

For the circuit shown in the following figure, transistor $M1$ and $M2$ are identical $NMOS$ transistors. Assume the $M2$ is in saturation and the output is unloaded.



The current I_x is related to I_{bias} as

(A) $I_x = I_{bias} + I_s$

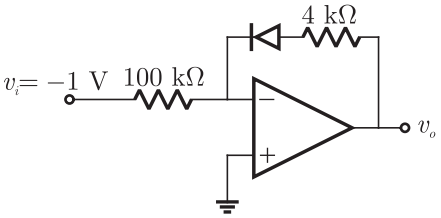
(B) $I_x = I_{bias}$

(C) $I_x = I_{bias} - \left(V_{DD} - \frac{V_{out}}{R_E}\right)$

(D) $I_x = I_{bias} - I_s$

MCQ 4.22

Consider the following circuit using an ideal OPAMP. The I-V characteristic of the diode is described by the relation $I = I_0\left(e^{\frac{V}{V_t}-1}\right)$ where $V_T = 25$ mV, $I_0 = 1\mu$A and V is the voltage across the diode (taken as positive for forward bias). For an input voltage $V_i = -1$ V, the output voltage V_0 is



(A) 0 V

(B) 0.1 V

(C) 0.7 V

(D) 1.1 V

MCQ 4.23

The OPAMP circuit shown above represents a

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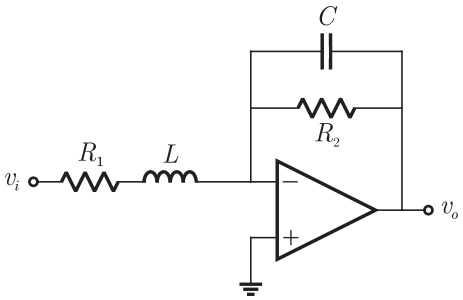
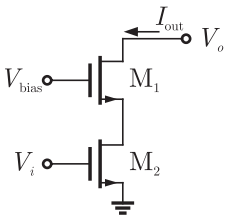


(A) high pass filter
(B) low pass filter
(C) band pass filter
(D) band reject filter

MCQ 4.24

Two identical NMOS transistors $M1$ and $M2$ are connected as shown below. V_{bias} is chosen so that both transistors are in saturation. The equivalent g_m of the pair is defied to be $\frac{\partial I_{out}}{\partial V_i}$ at constant V_{out}

The equivalent g_m of the pair is



(A) the sum of individual g_m's of the transistors
(B) the product of individual g_m's of the transistors
(C) nearly equal to the g_m of $M1$
(D) nearly equal to $\frac{g_m}{g_0}$ of $M2$

MCQ 4.25

Consider the Schmidt trigger circuit shown below

A triangular wave which goes from -12 to 12 V is applied to the inverting input of OPMAP. Assume that the output of the OPAMP swings from +15 V to -15 V. The voltage at the non-inverting input switches between

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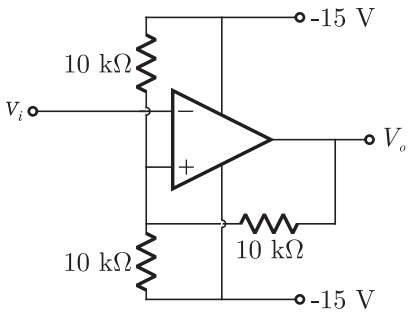


(A) $-12V$ to +12 V

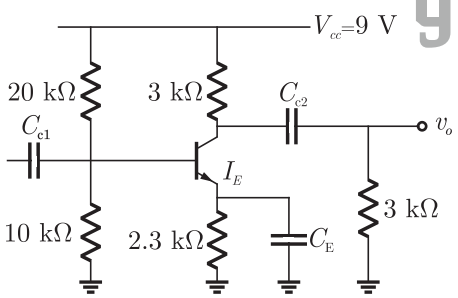
(B) -7.5 V to 7.5 V

(C) -5 V to +5 V

(D) 0 V and 5 V

Statement for Linked Answer Question 3.26 and 3.27:

In the following transistor circuit, $V_{BE} = 0.7$ V, $r_3 = 25$ mV/I_E, and β and all the capacitances are very large



MCQ 4.26

The value of DC current I_E is

(A) 1 mA

(B) 2 mA

(C) 5 mA

(D) 10 mA

MCQ 4.27

The mid-band voltage gain of the amplifier is approximately

(A) -180

(B) -120

(C) -90

(D) -60

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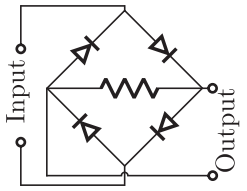
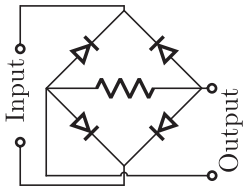
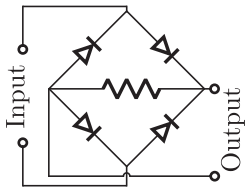
2007 **ONE MARK**

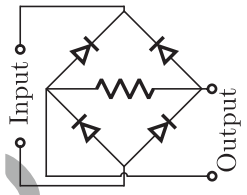
MCQ 4.28

The correct full wave rectifier circuit is

(A)


(B)


(C)


(D)


MCQ 4.29

In a transconductance amplifier, it is desirable to have

(A) a large input resistance and a large output resistance

(B) a large input resistance and a small output resistance

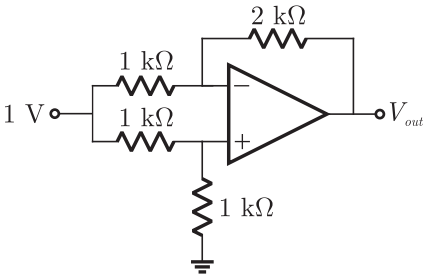
(C) a small input resistance and a large output resistance

(D) a small input resistance and a small output resistance

2007 **TWO MARKS**

MCQ 4.30

For the Op-Amp circuit shown in the figure, V_0 is



(A) -2 V

(B) -1 V

(C) -0.5 V

(D) 0.5 V

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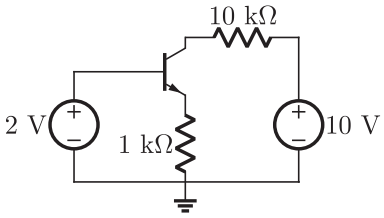
MCQ 4.31

For the BJT circuit shown, assume that the β of the transistor is very large and $V_{BE} = 0.7$ V. The mode of operation of the BJT is



(A) cut-off

(B) saturation

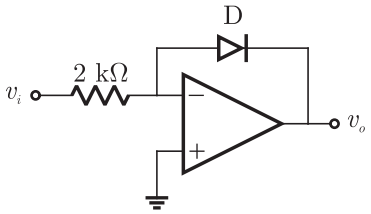
(C) normal active

(D) reverse active

MCQ 4.32

In the Op-Amp circuit shown, assume that the diode current follows the equation $I = I_s \exp(V/V_T)$. For $V_i = 2\,V$, $V_0 = V_{01}$, and for $V_i = 4\,V$, $V_0 = V_{02}$.

The relationship between V_{01} and V_{02} is



(A) $V_{02} = \sqrt{2}\ V_{o1}$

(B) $V_{o2} = e^2\, V_{o1}$

(C) $V_{o2} = V_{o1} 1\text{n}2$

(D) $V_{o1} - V_{o2} = V_T 1\text{n}2$

MCQ 4.33

In the CMOS inverter circuit shown, if the trans conductance parameters of the NMOS and PMOS transistors are

$$k_n = k_p = \mu_n C_{ox} \frac{W_n}{L_n} = \mu C_{ox} \frac{W_p}{L_p} = 40\mu A/V^2$$

and their threshold voltages ae $V_{THn} = |V_{THp}| = 1$ V the current I is

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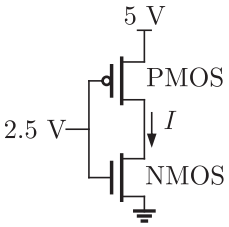
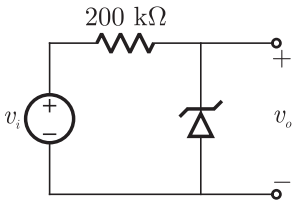


(A) 0 A
(B) 25 μA
(C) 45 μA
(D) 90 μA

MCQ 4.34

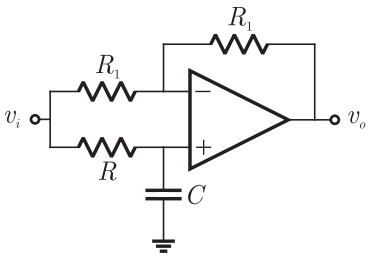
For the Zener diode shown in the figure, the Zener voltage at knee is 7 V, the knee current is negligible and the Zener dynamic resistance is 10 Ω. If the input voltage (V_i) range is from 10 to 16 V, the output voltage (V_0) ranges from



(A) 7.00 to 7.29 V
(B) 7.14 to 7.29 V
(C) 7.14 to 7.43 V
(D) 7.29 to 7.43 V

Statement for Linked Answer Questions 4.35 & 4.36:

Consider the Op-Amp circuit shown in the figure.



MCQ 4.35

The transfer function $V_0(s)/\ V_i(s)$ is

(A) $\dfrac{1-sRC}{1+sRC}$
(B) $\dfrac{1+sRC}{1-sRC}$

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(C) $\frac{1}{1-sRC}$ (D) $\frac{1}{1+sRC}$

MCQ 4.36

If $V_i = V_1 \sin(\omega t)$ and $V_0 = V_2 \sin(\omega t + \phi)$, then the minimum and maximum values of ϕ (in radians) are respectively

(A) $-\frac{\pi}{2}$ and $\frac{\pi}{2}$ (B) 0 and $\frac{\pi}{2}$

(C) $-\pi$ and 0 (D) $-\frac{\pi}{2}$ and 0

2006 ONE MARK

MCQ 4.37

The input impedance (Z_i) and the output impedance (Z_0) of an ideal trans-conductance (voltage controlled current source) amplifier are

(A) $Z_i = 0, Z_0 = 0$ (B) $Z_i = 0, Z_0 = \infty$

(C) $Z_i = \infty, Z_0 = 0$ (D) $Z_i = \infty, Z_0 = \infty$

MCQ 4.38

An n-channel depletion MOSFET has following two points on its $I_D - V_{Gs}$ curve:

(i) $V_{GS} = 0$ at $I_D = 12$ mA and

(ii) $V_{GS} = -6$ Volts at $I_D = 0$ mA

Which of the following Q point will given the highest trans conductance gain for small signals?

(A) $V_{GS} = -6$ Volts (B) $V_{GS} = -3$ Volts

(C) $V_{GS} = 0$ Volts (D) $V_{GS} = 3$ Volts

2006 TWO MARKS

MCQ 4.39

For the circuit shown in the following figure, the capacitor C is initially uncharged. At $t = 0$ the switch S is closed. The V_c across the capacitor at $t = 1$ millisecond is

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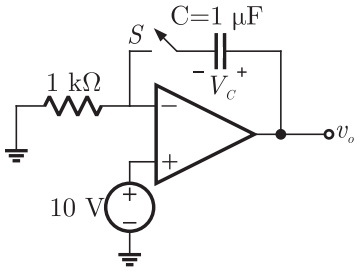
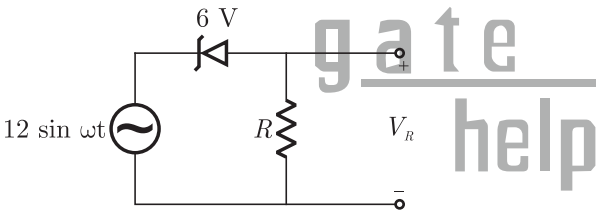
In the figure shown above, the OP-AMP is supplied with $\pm 15\,V$.

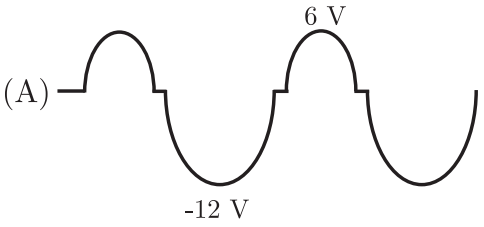


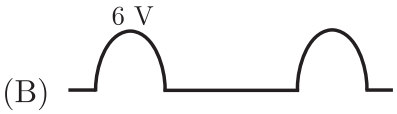
(A) 0 Volt
(B) 6.3 Volt
(C) 9.45 Volts
(D) 10 Volts

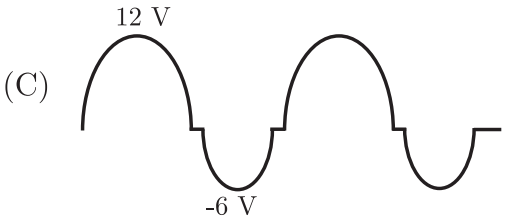
MCQ 4.40

For the circuit shown below, assume that the zener diode is ideal with a breakdown voltage of 6 volts. The waveform observed across R is









Common Data for Questions 4.41, 4.42 and 4.43 :

In the transistor amplifier circuit shown in the figure below, the

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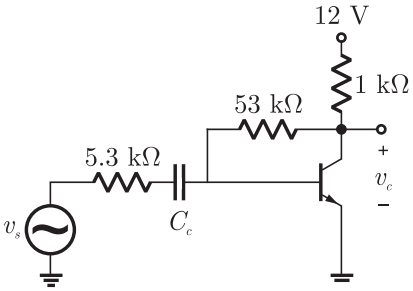
transistor has the following parameters:

$$\beta_{DC} = 60,\ V_{BE} = 0.7\,V, h_{ie} \to \infty$$

The capacitance C_C can be assumed to be infinite.

In the figure above, the ground has been shown by the symbol ∇



MCQ 4.41

Under the DC conditions, the collector-or-emitter voltage drop is

(A) 4.8 Volts (B) 5.3 Volts

(C) 6.0 Volts (D) 6.6 Volts

MCQ 4.42

If β_{DC} is increased by 10%, the collector-to-emitter voltage drop

(A) increases by less than or equal to 10%

(B) decreases by less than or equal to 10%

(C) increase by more than 10%

(D) decreases by more than 10%

MCQ 4.43

The small-signal gain of the amplifier $\frac{v_c}{v_s}$ is

(A) -10 (B) -5.3

(C) 5.3 (D) 10

Common Data for Questions 4.44 & 4.45:

A regulated power supply, shown in figure below, has an unregulated input (UR) of 15 Volts and generates a regulated output V_{out}. Use the component values shown in the figure.

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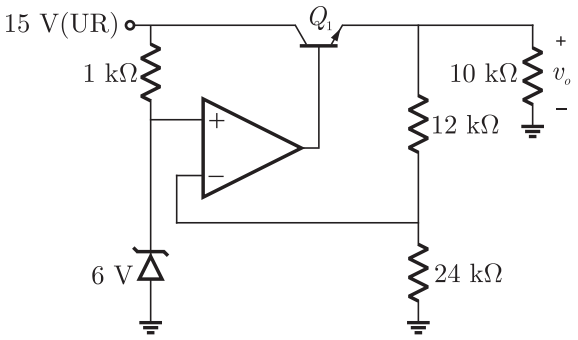


MCQ 4.44

The power dissipation across the transistor Q1 shown in the figure is

(A) 4.8 Watts (B) 5.0 Watts

(C) 5.4 Watts (D) 6.0 Watts

MCQ 4.45

If the unregulated voltage increases by 20%, the power dissipation across the transistor Q1

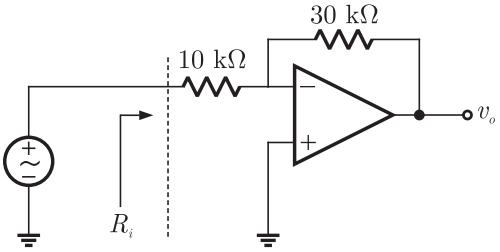
(A) increases by 20% (B) increases by 50%

(C) remains unchanged (D) decreases by 20%

2005 ONE MARK

MCQ 4.46

The input resistance R_i of the amplfier shown in the figure is



(A) $\frac{30}{4}$ kΩ (B) 10 kΩ

(C) 40 kΩ (D) infinite

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MCQ 4.47

The effect of current shunt feedback in an amplifier is to

(A) increase the input resistance and decrease the output resistance

(B) increases both input and output resistance

(C) decrease both input and output resistance

(D) decrease the input resistance and increase the output resistance

MCQ 4.48

The cascade amplifier is a multistage configuration of

(A) CC – CB (B) CE – CB

(C) CB – CC (D) CE – CC

2005 TWO MARKS

MCQ 4.49

In an ideal differential amplifier shown in the figure, a large value of (R_E).

(A) increase both the differential and common - mode gains.

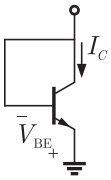
(B) increases the common mode gain only.

(C) decreases the differential mode gain only.

(D) decreases the common mode gain only.

MCQ 4.50

For an npn transistor connected as shown in figure $V_{BE} = 0.7$ volts. Given that reverse saturation current of the junction at room temperature 300 K is 10^{-13} A, the emitter current is



(A) 30 mA (B) 39 mA

(C) 49 mA (D) 20 mA

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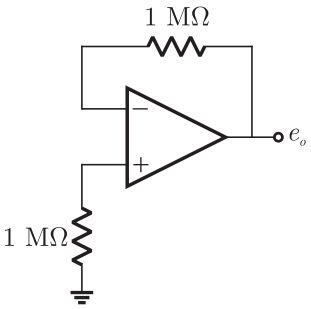
MCQ 4.51

The voltage e_0 is indicated in the figure has been measured by an ideal voltmeter. Which of the following can be calculated ?



(A) Bias current of the inverting input only

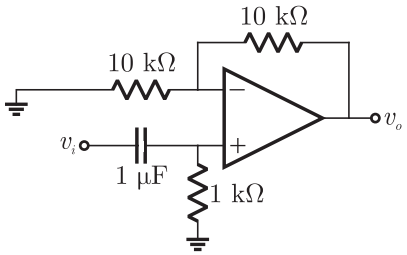
(B) Bias current of the inverting and non-inverting inputs only

(C) Input offset current only

(D) Both the bias currents and the input offset current

MCQ 4.52

The Op-amp circuit shown in the figure is filter. The type of filter and its cut. Off frequency are respectively



(A) high pass, 1000 rad/sec.

(B) Low pass, 1000 rad/sec

(C) high pass, 1000 rad/sec

(D) low pass, 10000 rad/sec

MCQ 4.53

The circuit using a BJT with $\beta = 50$ and $V_{BE} = 0.7\,V$ is shown in the figure. The base current I_B and collector voltage by V_C and respectively

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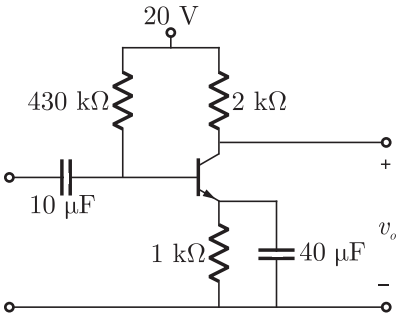
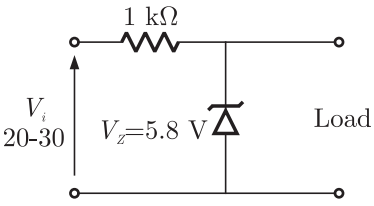


(A) 43 μA and 11.4 Volts
(B) 40 μA and 16 Volts
(C) 45 μA and 11 Volts
(D) 50 μA and 10 Volts

MCQ 4.54

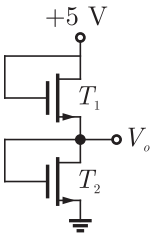
The Zener diode in the regulator circuit shown in the figure has a Zener voltage of 5.8 volts and a zener knee current of 0.5 mA. The maximum load current drawn from this current ensuring proper functioning over the input voltage range between 20 and 30 volts, is



(A) 23.7 mA
(B) 14.2 mA
(C) 13.7 mA
(D) 24.2 mA

MCQ 4.55

Both transistors T_1 and T_2 show in the figure, have a $\beta = 100$, threshold voltage of 1 Volts. The device parameters K_1 and K_2 of T_1 and T_2 are, respectively, 36 $\mu A/V^2$ and 9 μA/V^2. The output voltage V_o i s



(A) 1 V
(B) 2 V
(C) 3 V
(D) 4 V

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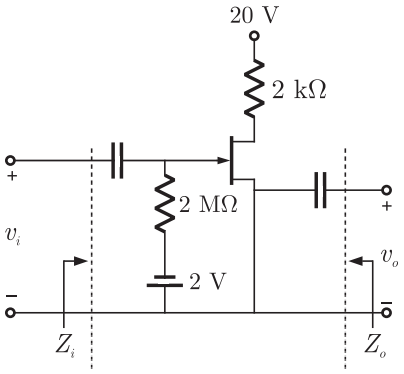
Common Data Questions 4.58, 4.59 and 4.60 :

Given, $r_d = 20k\Omega$, $I_{DSS} = 10$ mA, $V_p = -8$ V



MCQ 4.56

Z_i and Z_0 of the circuit are respectively

(A) 2 MΩ and 2 kΩ

(B) 2 MΩ and $\frac{20}{11}$ kΩ

(C) infinity and 2 MΩ

(D) infinity and $\frac{20}{11}$kΩ

MCQ 4.57

I_D and V_{DS} under DC conditions are respectively

(A) 5.625 mA and 8.75 V

(B) 1.875 mA and 5.00 V

(C) 4.500 mA and 11.00 V

(D) 6.250 mA and 7.50 V

MCQ 4.58

Transconductance in milli-Siemens (mS) and voltage gain of the amplifier are respectively

(A) 1.875 mS and 3.41

(B) 1.875 ms and -3.41

(C) 3.3 mS and -6

(D) 3.3 mS and 6

MCQ 4.59

Given the ideal operational amplifier circuit shown in the figure indicate the correct transfer characteristics assuming ideal diodes with zero cut-in voltage.

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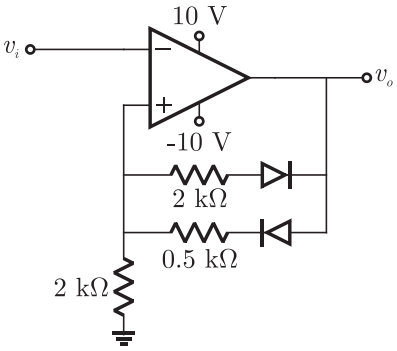
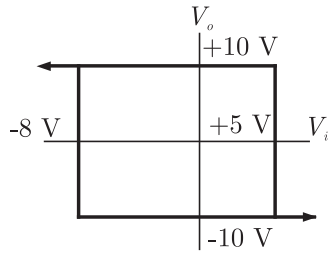
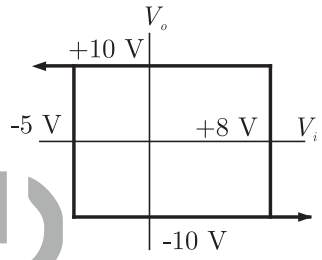
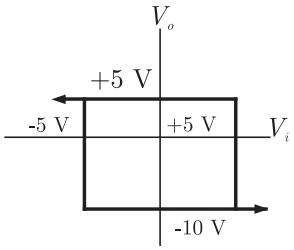
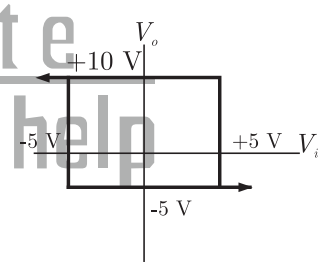


(A)


(B)


(C)


(D)


2004 ONE MARK

MCQ 4.60

An ideal op-amp is an ideal

(A) voltage controlled current source

(B) voltage controlled voltage source

(C) current controlled current source

(D) current controlled voltage source

MCQ 4.61

Voltage series feedback (also called series-shunt feedback) results in

(A) increase in both input and output impedances

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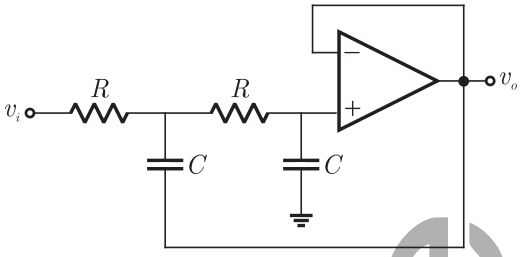
(B) decrease in both input and output impedances

(C) increase in input impedance and decrease in output impedance

(D) decrease in input impedance and increase in output impedance

MCQ 4.62

The circuit in the figure is a



(A) low-pass filter (B) high-pass filter

(C) band-pass filter (D) band-reject filter

2004 **TWO MARKS**

MCQ 4.63

A bipolar transistor is operating in the active region with a collector current of 1 mA. Assuming that the β of the transistor is 100 and the thermal voltage (V_T) is 25 mV, the transconductance (g_m) and the input resistance (r_π) of the transistor in the common emitter configuration, are

(A) $g_m = 25$ mA/V and $r_\pi = 15.625\,\text{k}\Omega$

(B) $g_m = 40$ mA/V and $r_\pi = 4.0\ \text{k}\Omega$

(C) $g_m = 25$ mA/V and $r_\pi = 2.5\ \text{k}\ \Omega$

(D) $g_m = 40$ mA/V and $r_\pi = 2.5\ \text{k}\Omega$

MCQ 4.64

The value of C required for sinusoidal oscillations of frequency 1 kHz in the circuit of the figure is

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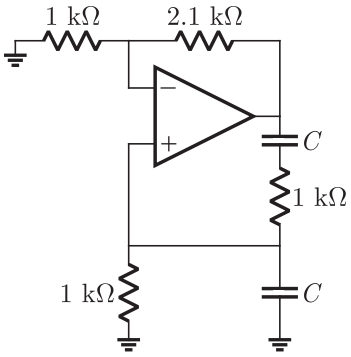


(A) $\frac{1}{2\pi}$ μF

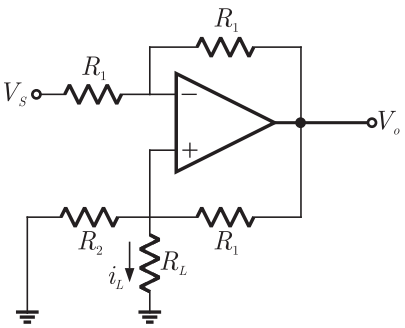
(B) 2π μF

(C) $\frac{1}{2\pi\sqrt{6}}$ μF

(D) $2\pi\sqrt{6}$ μF

MCQ 4.65

In the op-amp circuit given in the figure, the load current i_L is



(A) $-\frac{V_s}{R_2}$

(B) $\frac{V_s}{R_2}$

(C) $-\frac{V_s}{R_L}$

(D) $\frac{V_s}{R_1}$

MCQ 4.66

In the voltage regulator shown in the figure, the load current can vary from 100 mA to 500 mA. Assuming that the Zener diode is ideal (i.e., the Zener knee current is negligibly small and Zener resistance is zero in the breakdown region), the value of R is

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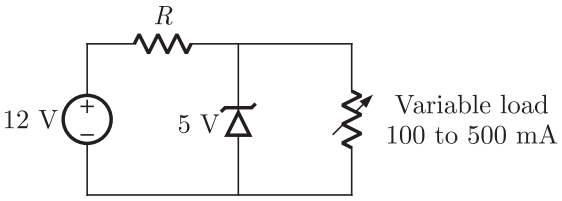


(A) $7\,\Omega$ (B) $70\,\Omega$

(C) $\frac{70}{3}\,\Omega$ (D) $14\ \Omega$

MCQ 4.67

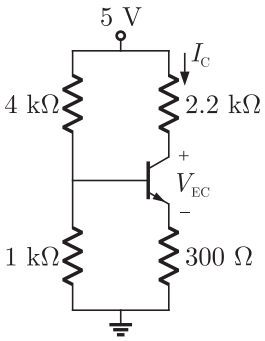
In a full-wave rectifier using two ideal diodes, V_{dc} and V_m are the dc and peak values of the voltage respectively across a resistive load. If PIV is the peak inverse voltage of the diode, then the appropriate relationships for this rectifier are

(A) $V_{dc} = \frac{V_m}{\pi},\ PIV = 2V_m$ (B) $I_{dc} = 2\frac{V_m}{\pi},\ PIV = 2\,V_m$

(C) $V_{dc} = 2\frac{V_m}{\pi},\ PIV = V_m$ (D) $V_{dc}\frac{V_m}{\pi},\ PIV = V_m$

MCQ 4.68

Assume that the β of transistor is extremely large and $V_{BE} = 0.7\,V, I_C$ and V_{CE} in the circuit shown in the figure



(A) $I_C = 1\,\text{mA}, V_{CE} = 4.7\ \text{V}$ (B) $I_C = 0.5\ \text{mA}, V_{CE} = 3.75\ \text{V}$

(C) $I_C = 1\ \text{mA}, V_{CE} = 2.5\ \text{V}$ (D) $I_C = 0.5\ \text{mA}, V_{CE} = 3.9\ \text{V}$

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MCQ 4.69

Choose the correct match for input resistance of various amplifier configurations shown below :

Configuration	Input resistance
CB : Common Base	LO : Low
CC : Common Collector	MO : Moderate
CE : Common Emitter	HI : High

(A) CB – LO, CC – MO, CE – HI

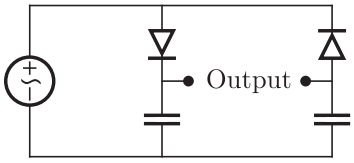
(B) CB – LO, CC – HI, CE – MO

(C) CB – MO, CC – HI, CE – LO

(D) CB – HI, CC – LO, CE – MO

MCQ 4.70

The circuit shown in the figure is best described as a

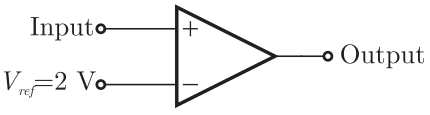


(A) bridge rectifier (B) ring modulator

(C) frequency discriminator (D) voltage double

MCQ 4.71

If the input to the ideal comparators shown in the figure is a sinusoidal signal of 8 V (peak to peak) without any DC component, then the output of the comparators has a duty cycle of



(A) 1/2 (B) 1/3

(C) 1/6 (D) 1/2

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MCQ 4.72

If the differential voltage gain and the common mode voltage gain of a differential amplifier are 48 dB and 2 dB respectively, then common mode rejection ratio is

(A) 23 dB (B) 25 dB

(C) 46 dB (D) 50 dB

MCQ 4.73

Generally, the gain of a transistor amplifier falls at high frequencies due to the

(A) internal capacitances of the device

(B) coupling capacitor at the input

(C) skin effect

(D) coupling capacitor at the output

2003 TWO MARKS

MCQ 4.74

An amplifier without feedback has a voltage gain of 50, input resistance of 1 k Ω and output resistance of 2.5 kΩ. The input resistance of the current-shunt negative feedback amplifier using the above amplifier with a feedback factor of 0.2, is

(A) $\frac{1}{11}$ kΩ (B) $\frac{1}{5}$kΩ

(C) 5 kΩ (D) 11 kΩ

MCQ 4.75

In the amplifier circuit shown in the figure, the values of R_1 and R_2 are such that the transistor is operating at $V_{CE} = 3$ V and $I_C = 1.5$ mA when its β is 150. For a transistor with β of 200, the operating point (V_{CE}, I_C) is

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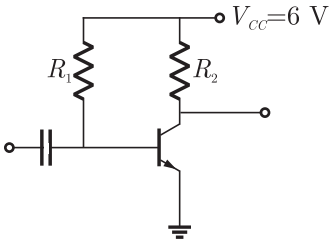
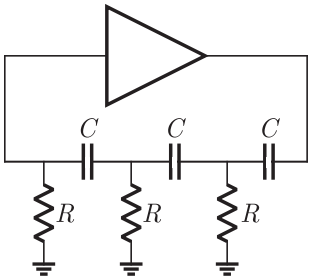


(A) (2 V, 2 mA)
(B) (3 V, 2 mA)
(C) (4 V, 2 mA)
(D) (4 V, 1 mA)

MCQ 4.76

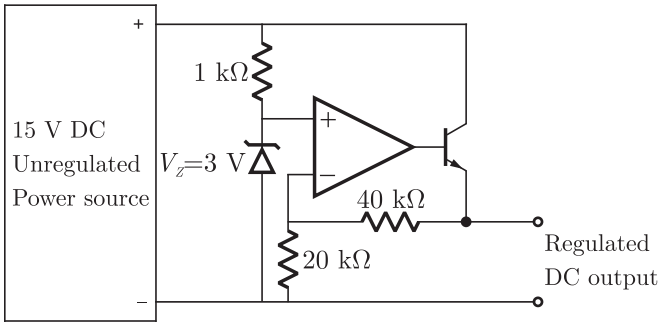
The oscillator circuit shown in the figure has an ideal inverting amplifier. Its frequency of oscillation (in Hz) is



(A) $\frac{1}{(2\pi\sqrt{6}\,RC)}$
(B) $\frac{1}{(2\pi RC)}$
(C) $\frac{1}{(\sqrt{6}\,RC)}$
(D) $\frac{\sqrt{6}}{(2\pi RC)}$

MCQ 4.77

The output voltage of the regulated power supply shown in the figure is



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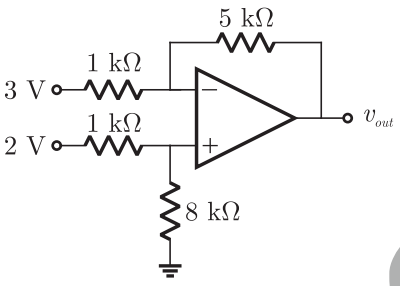
(A) 3 V (B) 6 V

(C) 9 V (D) 12 V

MCQ 4.78

If the op-amp in the figure is ideal, the output voltage V_{out} will be equal to



(A) 1 V (B) 6 V

(C) 14 V (D) 17 V

MCQ 4.79

Three identical amplifiers with each one having a voltage gain of 50, input resistance of 1 kΩ and output resistance of 250 Ω are cascaded. The opened circuit voltages gain of the combined amplifier is

(A) 49 dB (B) 51 dB

(C) 98 dB (D) 102 dB

MCQ 4.80

An ideal sawtooth voltages waveform of frequency of 500 Hz and amplitude 3 V is generated by charging a capacitor of 2 μF in every cycle. The charging requires

(A) Constant voltage source of 3 V for 1 ms

(B) Constant voltage source of 3 V for 2 ms

(C) Constant voltage source of 1 mA for 1 ms

(D) Constant voltage source of 3 mA for 2 ms

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MCQ 4.81

In a negative feedback amplifier using voltage-series (i.e. voltage-sampling, series mixing) feedback.

(A) R_i decreases and R_0 decreases

(B) R_i decreases and R_0 increases

(C) R_i increases and R_0 decreases

(D) R_i increases and R_0 increases

(R_i and R_0 denote the input and output resistance respectively)

MCQ 4.82

A 741-type opamp has a gain-bandwidth product of 1 MHz. A non-inverting amplifier suing this opamp and having a voltage gain of 20 dB will exhibit a -3 dB bandwidth of

(A) 50 kHz

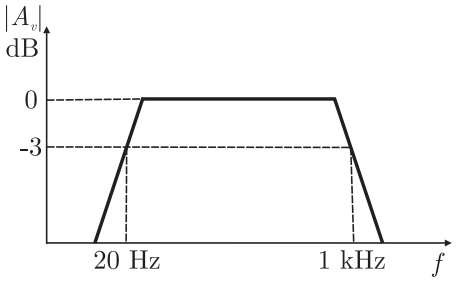
(B) 100 kHz

(C) $\frac{1000}{17}$ kHz

(D) $\frac{1000}{7.07}$ kHz

MCQ 4.83

Three identical RC-coupled transistor amplifiers are cascaded. If each of the amplifiers has a frequency response as shown in the figure, the overall frequency response is as given in



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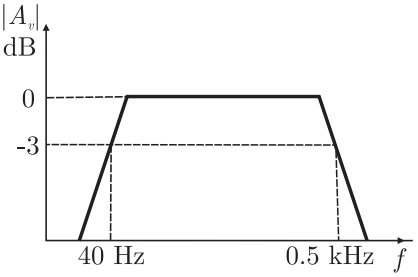
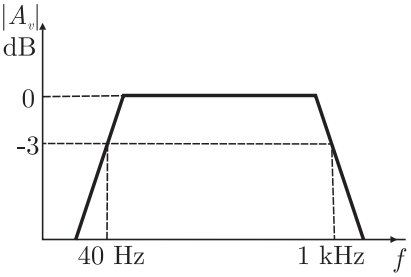
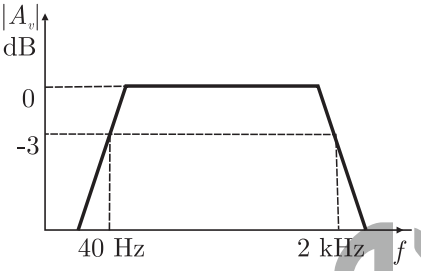
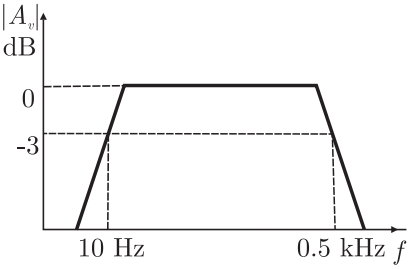
(A)


(B)


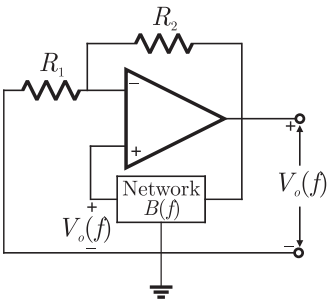
(C)


(D)


2002 TWO MARKS

MCQ 4.84

The circuit in the figure employs positive feedback and is intended to generate sinusoidal oscillation. If at a frequency $f_0, B(f) = \Delta\dfrac{V_f(f)}{V_0(f)} = \dfrac{1}{6}\angle 0°$, then to sustain oscillation at this frequency



(A) $R_2 = 5R_1$

(B) $R_2 = 6R_1$

(C) $R_2 = \dfrac{R_1}{6}$

(D) $R_2 = \dfrac{R_1}{5}$

MCQ 4.85

An amplifier using an opamp with a slew-rate $SR = 1\ V/\mu$ sec has

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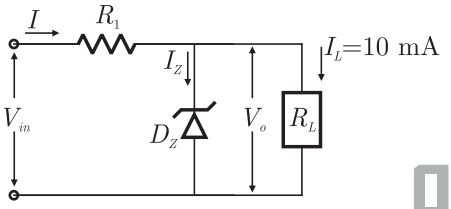
a gain of 40 dB. If this amplifier has to faithfully amplify sinusoidal signals from dc to 20 kHz without introducing any slew-rate induced distortion, then the input signal level must not exceed.

(A) 795 mV (B) 395 mV

(C) 79.5 mV (D) 39.5 mV

MCQ 4.86

A zener diode regulator in the figure is to be designed to meet the specifications: $I_L = 10$ mA $V_0 = 10$ V and V_{in} varies from 30 V to 50 V. The zener diode has $V_z = 10$ V and I_{zk} (knee current) =1 mA. For satisfactory operation

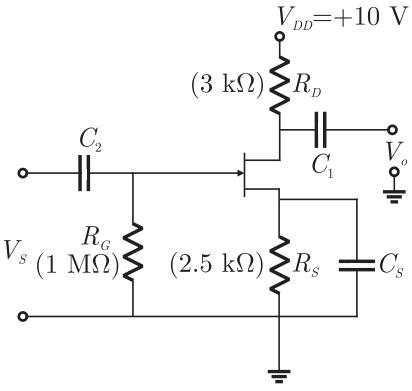


(A) $R \leq 1800\Omega$ (B) $2000\Omega \leq R \leq 2200\Omega$

(C) $3700\Omega \leq R \leq 4000\Omega$ (D) $R \geq 4000\Omega$

MCQ 4.87

The voltage gain $A_v = \frac{v_0}{v_i}$ of the JFET amplifier shown in the figure is $I_{DSS} = 10$ mA $V_p = -5$ V(Assume C_1, C_2 and C_s to be very large



(A) +16 (B) -16

(C) +8 (D) -6

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2001 **ONE MARK**

MCQ 4.88

The current gain of a BJT is

(A) $g_m r_0$ (B) $\frac{g_m}{r}$

(C) $g_m r_\pi$ (D) $\frac{g_m}{r_\pi}$

MCQ 4.89

Thee ideal OP-AMP has the following characteristics.

(A) $R_i = \infty,\ A = \infty,\ R_0 = 0$ (B) $R_i = 0,\ A = \infty,\ R_0 = 0$

(C) $R_i = \infty,\ A = \infty,\ R_0 = \infty$ (D) $R_i = 0,\ A = \infty,\ R_0 = \infty$

MCQ 4.90

Consider the following two statements :

Statement 1 :

A stable multi vibrator can be used for generating square wave.

Statement 2:

Bistable multi vibrator can be used for storing binary information.

(A) Only statement 1 is correct

(B) Only statement 2 is correct

(C) Both the statements 1 and 2 are correct

(D) Both the statements 1 and 2 are incorrect

2001 **TWO MARKS**

MCQ 4.91

An *npn* BJT has $g_m = 38$ mA/V, $C_\mu = 10^{-14}$ F, $C_\pi = 4 \times 10^{-13}$ F, and DC current gain $\beta_0 = 90$. For this transistor f_T and f_β are

(A) $f_T = 1.64 \times 10^8$ Hz and $f_\beta = 1.47 \times 10^{10}$ Hz

(B) $f_T = 1.47 \times 10^{10}$ Hz and $f_\beta = 1.64 \times 10^8$ Hz

(C) $f_T = 1.33 \times 10^{12}$ Hz and $f_\beta = 1.47 \times 10^{10}$ Hz

(D) $f_T = 1.47 \times 10^{10}$ Hz and $f_\beta = 1.33 \times 10^{12}$ Hz

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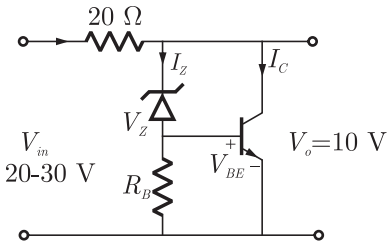
MCQ 4.92

The transistor shunt regulator shown in the figure has a regulated output voltage of 10 V, when the input varies from 20 V to 30 V. The relevant parameters for the zener diode and the transistor are : $V_z = 9.5$, $V_{BE} = 0.3$ V, $\beta = 99$, Neglect the current through R_B. Then the maximum power dissipated in the zener diode (P_z) and the transistor (P_T) are



(A) $P_z = 75$ mW, $P_T = 7.9$ W

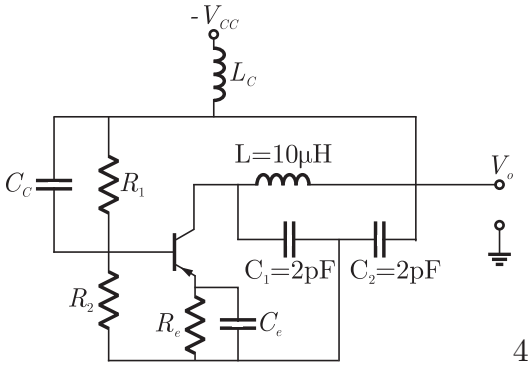
(B) $P_z = 85$ mW, $P_T = 8.9$ W

(C) $P_z = 95$ mW, $P_T = 9.9$ W

(D) $P_z = 115$ mW, $P_T = 11.9$ W

MCQ 4.93

The oscillator circuit shown in the figure is



4

(A) Hartely oscillator with $f_{oscillation} = 79.6$ MHz

(B) Colpitts oscillator with $f_{oscillation} = 50.3$ MHz

(C) Hartley oscillator with $f_{oscillation} = 159.2$ MHz

(D) Colpitts oscillator with $f_{oscillation} = 159.3$ MHz

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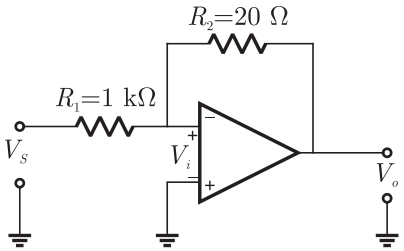
MCQ 4.94

The inverting OP-AMP shown in the figure has an open-loop gain of 100.



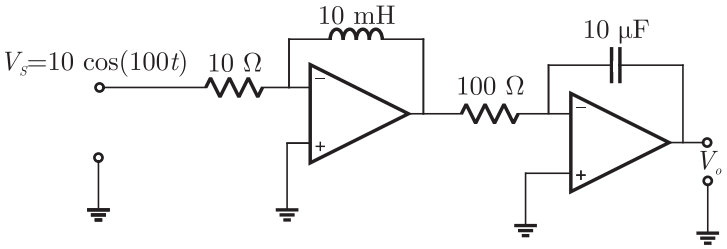
The closed-loop gain $\frac{V_0}{V_s}$ is

(A) -8 (B) -9

(C) -10 (D) -11

MCQ 4.95

In the figure assume the OP-AMPs to be ideal. The output v_0 of the circuit is



(A) $10\cos(100t)$ (B) $10\int_0^t \cos(100\tau)\,d\tau$

(C) $10^{-4}\int_0^t \cos(100\tau)\,d\tau$ (D) $10^{-4}\frac{d}{dt}\cos(100t)$

2000 **ONE MARK**

MCQ 4.96

In the differential amplifier of the figure, if the source resistance of the current source I_{EE} is infinite, then the common-mode gain is

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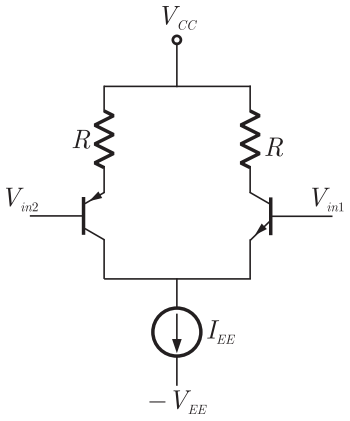
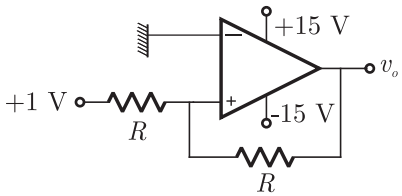


(A) zero
(B) infinite
(C) indeterminate
(D) $\frac{V_{in1} + V_{in2}}{2\,V_T}$

MCQ 4.97

In the circuit of the figure, V_0 is



(A) -1 V
(B) 2 V
(C) +1 V
(D) +15 V

MCQ 4.98

Introducing a resistor in the emitter of a common amplifier stabilizes the dc operating point against variations in

(A) only the temperature
(B) only the β of the transistor
(C) both temperature and β
(D) none of the above

MCQ 4.99

The current gain of a bipolar transistor drops at high frequencies because of

(A) transistor capacitances
(B) high current effects in the base
(C) parasitic inductive elements
(D) the Early effect

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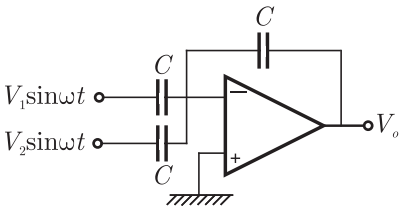
MCQ 4.100

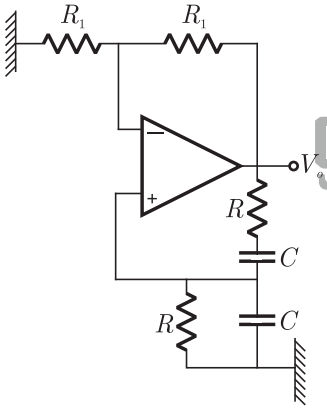
If the op-anp in the figure, is ideal, then v_0 is



(A) zero
(B) $(V_1 - V_2)\sin\omega t$
(C) $-(V_1 + V_2)\sin\omega t$
(D) $(V_1 + V_2)\sin\omega t$

MCQ 4.101

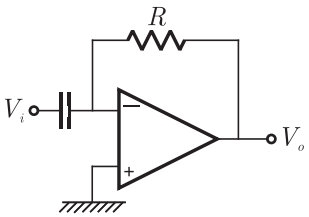
The configuration of the figure is a



(A) precision integrator
(B) Hartely oscillator
(C) Butterworth high pass filter
(D) Wien-bridge oscillator

MCQ 4.102

Assume that the op-amp of the figure is ideal. If v_i is a triangular wave, then v_0 will be



(A) square wave
(B) triangular wave
(C) parabolic wave
(D) sine wave

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MCQ 4.103

The most commonly used amplifier is sample and hold circuits is

(A) a unity gain inverting amplifier

(B) a unity gain non-inverting amplifier

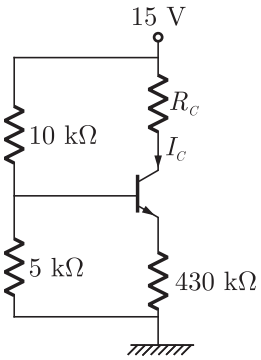
(C) an inverting amplifier with a gain of 10

(D) an inverting amplifier with a gain of 100

2000 TWO MARKS

MCQ 4.104

In the circuit of figure, assume that the transistor is in the active region. It has a large β and its base-emitter voltage is 0.7 V. The value of I_c is

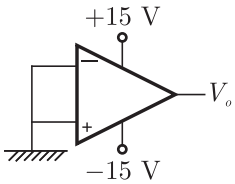


(A) Indeterminate since R_c is not given (B) 1 mA

(C) 5 mA (D) 10 mA

MCQ 4.105

If the op-amp in the figure has an input offset voltage of 5 mV and an open-loop voltage gain of 10000, then v_0 will be



(A) 0 V (B) 5 mV

(C) + 15 V or -15 V (D) +50 V or -50 V

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1999 **ONE MARK**

MCQ 4.106

The first dominant pole encountered in the frequency response of a compensated op-amp is approximately at

(A) 5 Hz (B) 10 kHz

(C) 1 MHz (D) 100 MHz

MCQ 4.107

Negative feedback in an amplifier

(A) reduces gain

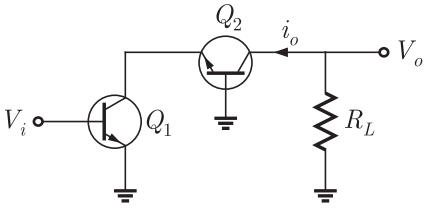
(B) increases frequency and phase distortions

(C) reduces bandwidth

(D) increases noise

MCQ 4.108

In the cascade amplifier shown in the given figure, if the common-emitter stage (Q_1) has a transconductance gm_1, and the common base stage (Q_2) has a transconductance gm_2, then the overall transconductance $g(= i_0/v_i)$ of the cascade amplifier is



(A) g_{m1} (B) g_{m2}

(C) $\frac{g_{m1}}{2}$ (D) $\frac{g_{m2}}{2}$

MCQ 4.109

Crossover distortion behavior is characteristic of

(A) Class A output stage (B) Class B output stage

(C) Class AB output stage (D) Common-base output stage

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1999 **TWO MARK**

MCQ 4.110

An amplifier has an open-loop gain of 100, an input impedance of 1 kΩ,and an output impedance of 100 Ω. A feedback network with a feedback factor of 0.99 is connected to the amplifier in a voltage series feedback mode. The new input and output impedances, respectively, are

(A) 10 Ω and 1Ω (B) 10 Ω and 10 kΩ

(C) 100 kΩ and 1 Ω (D) 100 kΩ and 1 kΩ

MCQ 4.111

A dc power supply has a no-load voltage of 30 V, and a full-load voltage of 25 V at a full-load current of 1 A. Its output resistance and load regulation, respectively, are

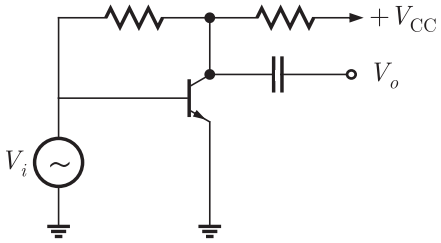
(A) 5 Ω and 20% (B) 25 Ω and 20%

(C) 5 Ω and 16.7% (D) 25 Ω and 16.7%

1998 **ONE MARK**

MCQ 4.112

The circuit of the figure is an example of feedback of the following type



(A) current series (B) current shunt

(C) voltage series (D) voltage shunt

MCQ 4.113

In a differential amplifier, CMRR can be improved by using an increased

(A) emitter resistance (B) collector resistance

(C) power supply voltages (D) source resistance

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MCQ 4.114

From a measurement of the rise time of the output pulse of an amplifier whose is a small amplitude square wave, one can estimate the following parameter of the amplifier

(A) gain-bandwidth product (B) slow rate

(C) upper 3–dB frequency (D) lower 3–dB frequency

MCQ 4.115

The emitter coupled pair of BJT's given a linear transfer relation between the differential output voltage and the differential output voltage and the differential input voltage V_{id} is less α times the thermal voltage, where α is

(A) 4 (B) 3

(C) 2 (D) 1

MCQ 4.116

In a shunt-shunt negative feedback amplifier, as compared to the basic amplifier

(A) both, input and output impedances decrease

(B) input impedance decreases but output impedance increases

(C) input impedance increase but output

(D) both input and output impedances increases.

1998 TWO MARKS

MCQ 4.117

A multistage amplifier has a low-pass response with three real poles at $s = -\omega_1 - \omega_2$ and ω_3. The approximate overall bandwidth B of the amplifier will be given by

(A) $B = \omega_1 + \omega_2 + \omega_3$ (B) $\frac{1}{B} = \frac{1}{\omega_1} + \frac{1}{\omega_2} + \frac{1}{\omega_3}$

(C) $B = (\omega_1 + \omega_2 + \omega_3)^{1/3}$ (D) $B = \sqrt{\omega_1^2 + \omega_2^2 + \omega_3^2}$

MCQ 4.118

One input terminal of high gain comparator circuit is connected to ground and a sinusoidal voltage is applied to the other input. The

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output of comparator will be

(A) a sinusoid
(B) a full rectified sinusoid
(C) a half rectified sinusoid
(D) a square wave

MCQ 4.119

In a series regulated power supply circuit, the voltage gain A_v of the 'pass' transistor satisfies the condition

(A) $A_v \to \infty$
(B) $1 << A_v < \infty$
(C) $A_v \approx 1$
(D) $A_v << 1$

MCQ 4.120

For full wave rectification, a four diode bridge rectifier is claimed to have the following advantages over a two diode circuit :

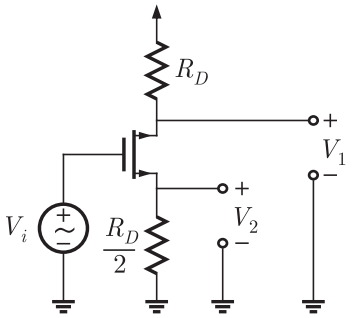
(A) less expensive transformer,
(B) smaller size transformer, and
(C) suitability for higher voltage application.

Of these,

(A) only (1) and (2) are true
(B) only (1) and (3) are true
(C) only (2) and (3) are true
(D) (1), (2) as well as (3) are true

MCQ 4.121

In the MOSFET amplifier of the figure is the signal output V_1 and V_2 obey the relationship



(A) $V_1 = \frac{V_2}{2}$
(B) $V_1 = -\frac{V_2}{2}$
(C) $V_1 = 2\,V_2$
(D) $V_1 = -\,2\,V_2$

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MCQ 4.122

For small signal ac operation, a practical forward biased diode can be modelled as

(A) a resistance and a capacitance in series

(B) an ideal diode and resistance in parallel

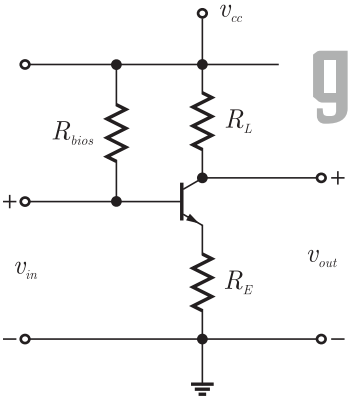
(C) a resistance and an ideal diode in series

(D) a resistance

1997 **ONE MARK**

MCQ 4.123

In the BJT amplifier shown in the figure is the transistor is based in the forward active region. Putting a capacitor across R_E will



(A) decrease the voltage gain and decrease the input impedance

(B) increase the voltage gain and decrease the input impedance

(C) decrease the voltage gain and increase the input impedance

(D) increase the voltage gain and increase the input impedance

MCQ 4.124

A cascade amplifier stags is equivalent to

(A) a common emitter stage followed by a common base stage

(B) a common base stage followed by an emitter follower

(C) an emitter follower stage followed by a common base stage

(D) a common base stage followed by a common emitter stage

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MCQ 4.125

In a common emitter BJT amplifier, the maximum usable supply voltage is limited by

(A) Avalanche breakdown of Base-Emitter junction

(B) Collector-Base breakdown voltage with emitter open (BV_{CBO})

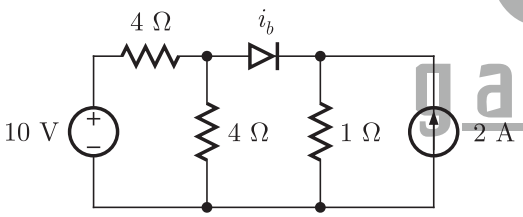
(C) Collector-Emitter breakdown voltage with base open (BV_{CBO})

(D) Zener breakdown voltage of the Emitter-Base junction

1997 **TWO MARKS**

MCQ 4.126

In the circuit of in the figure is the current i_D through the ideal diode (zero cut in voltage and forward resistance) equals



(A) 0 A

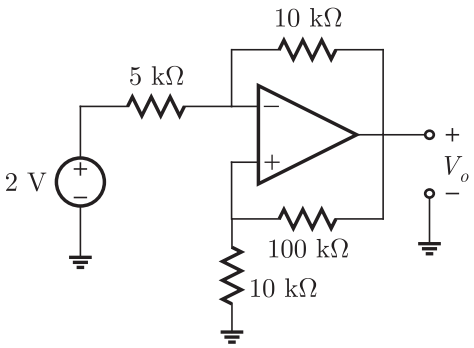
(B) 4 A

(C) 1 A

(D) None of the above

MCQ 4.127

The output voltage V_0 of the circuit shown in the figure is



(A) −4 V

(B) 6 V

(C) 5 V

(D) −5.5 V

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MCQ 4.128

A half wave rectifier uses a diode with a forward resistance Rf. The voltage is $V_m \sin \omega t$ and the load resistance is R_L. The DC current is given by

(A) $\dfrac{V_m}{\sqrt{2}\,R_L}$

(B) $\dfrac{V_m}{\pi (R_f + R_L)}$

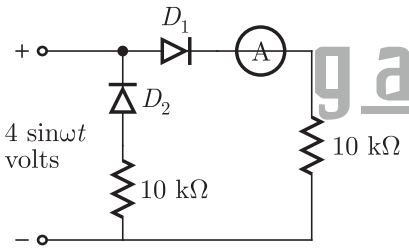
(C) $\dfrac{2\,V_m}{\sqrt{\pi}}$

(D) $\dfrac{V_m}{R_L}$

1996 **ONE MARK**

MCQ 4.129

In the circuit of the given figure, assume that the diodes are ideal and the meter is an average indicating ammeter. The ammeter will read



(A) $0.4\sqrt{2}$ A

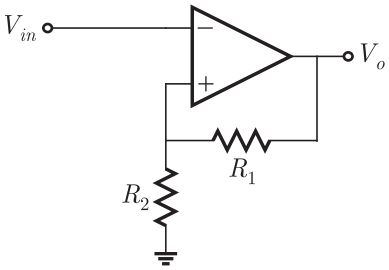
(B) 0.4 A

(C) $\dfrac{0.8}{\pi}$ A

(D) $\dfrac{0.4}{\pi}$ mamp

MCQ 4.130

The circuit shown in the figure is that of



(A) a non-inverting amplifier

(B) an inverting amplifier

(C) an oscillator

(D) a Schmitt trigger

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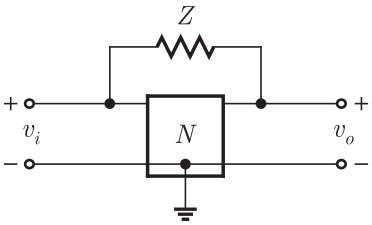
MCQ 4.131

In the circuit shown in the given figure N is a finite gain amplifier with a gain of k, a very large input impedance, and a very low output impedance. The input impedance of the feedback amplifier with the feedback impedance Z connected as shown will be

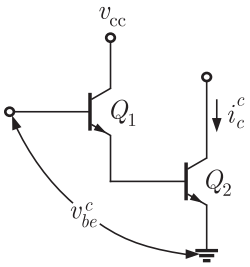


(A) $Z\left(1-\frac{1}{k}\right)$ (B) $Z(1-k)$

(C) $\frac{Z}{(k-1)}$ (D) $\frac{Z}{(1-k)}$

MCQ 4.132

A Darlington stage is shown in the figure. If the transconductance of Q_1 is g_{m1} and Q_2 is g_{m2}, then the overall transconductance $g_{mc}\left[\triangleq \frac{i_c^c}{v_{be}^c}\right]$ is given by



(A) g_{m1} (B) $0.5\, g_{m1}$

(C) g_{m2} (D) $0.5\, g_{m2}$

MCQ 4.133

Value of R in the oscillator circuit shown in the given figure, so chosen that it just oscillates at an angular frequency of ω. The value of ω and the required value of R will respectively be

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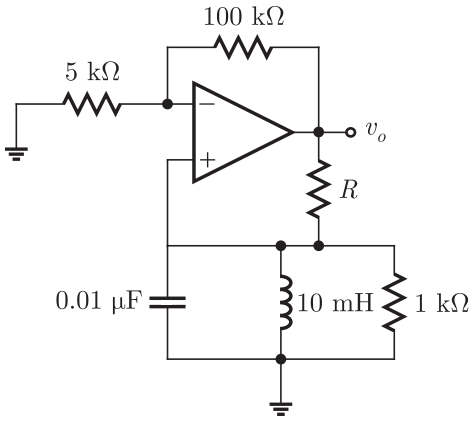
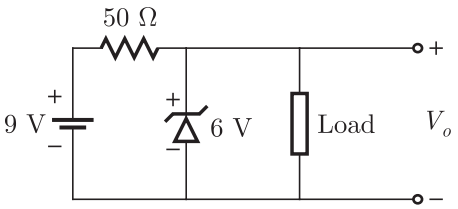


(A) 10^5 rad/sec, $2 \times 10^4\ \Omega$
(B) 2×10^4 rad/sec, $2 \times 10^4\ \Omega$
(C) 2×10^4 rad/sec, $10^5\ \Omega$
(D) 10^5 rad/sec, $10^5\ \Omega$

MCQ 4.134

A zener diode in the circuit shown in the figure is has a knee current of 5 mA, and a maximum allowed power dissipation of 300 mW. What are the minimum and maximum load currents that can be drawn safely from the circuit, keeping the output voltage V_0 constant at 6 V?



(A) 0 mA, 180 mA
(B) 5 mA, 110 mA
(C) 10 mA, 55 mA
(D) 60 mA, 180 mA

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SOLUTIONS

SOL 4.1

For the parallel RLC circuit resonance frequency is,

$$\omega_r = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{10 \times 10^{-6} \times 1 \times 10^{-9}}} = 10\,\text{M rad/s}$$

Thus given frequency is resonance frequency and parallel RLC circuit has maximum impedance at resonance frequency

Gain of the amplifier is $g_m \times (Z_C \| R_L)$ where Z_C is impedance of parallel RLC circuit.

At $\omega = \omega_r$, $Z_C = R = 2\,\text{k}\Omega = Z_{C\max}$.

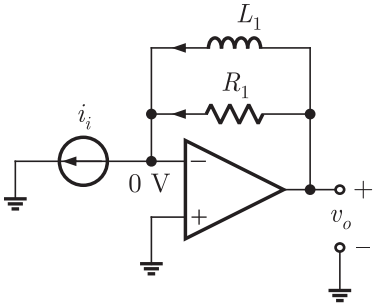
Hence at this frequency (ω_r), gain is

$\text{Gain}\big|_{\omega=\omega_r} = g_m(Z_C \| R_L) = g_m(2\text{k} \| 2\text{k}) = g_m \times 10^3$ which is maximum. Therefore gain is maximum at $\omega_r = 10\,\text{M rad/sec}$.

Hence (A) is correct option.

SOL 4.2

The given circuit is shown below :



From diagram we can write

$$I_i = \frac{V_o}{R_1} + \frac{V_o}{sL_1}$$

Transfer function

$$H(s) = \frac{V_o}{I_1} = \frac{sR_1L_1}{R_1 + sL_1}$$

or $$H(j\omega) = \frac{j\omega R_1 L_1}{R_1 + j\omega L_1}$$

At $\omega = 0$ $\quad H(j\omega) = 0$

At $\omega = \infty$ $\quad H(j\omega) = R_1 = \text{constant}.$ Hence HPF.

Hence (D) is correct option.

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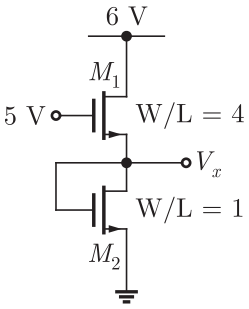
SOL 4.3

Given circuit is shown below.



For transistor M_2,

$$V_{GS} = V_G - V_S = V_x - 0 = V_x$$

$$V_{DS} = V_D - V_S = V_x - 0 = V_x$$

Since $V_{GS} - V_T = V_x - 1 < V_{DS}$, thus M_2 is in saturation.
By assuming M_1 to be in saturation we have

$$I_{DS(M_1)} = I_{DS(M_2)}$$

$$\frac{\mu_n C_{0x}}{2}(4)(5 - V_x - 1)^2 = \frac{\mu_n C_{0x}}{2}1(V_x - 1)^2$$

$$4(4 - V_x)^2 = (V_x - 1)^2$$

or $$2(4 - V_x) = \pm (V_x - 1)$$

Taking positive root,

$$8 - 2V_x = V_x - 1$$

$$V_x = 3\text{ V}$$

At $V_x = 3$ V for $M_1, V_{GS} = 5 - 3 = 2\text{ V} < V_{DS}$. Thus our assumption is true and $V_x = 3$ V.
Hence (C) is correct option.

SOL 4.4

We have $\alpha = 0.98$

Now $$\beta = \frac{\alpha}{1 - \alpha} = 4.9$$

In active region, for common emitter amplifier,

$$I_C = \beta I_B + (1 + \beta) I_{CO} \qquad ...(1)$$

Substituting $I_{CO} = 0.6\,\mu\text{A}$ and $I_B = 20\,\mu\text{A}$ in above eq we have,

$$I_C = 1.01\,\text{mA}$$

Hence (D) is correct option.

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SOL 4.5

In active region $V_{BEon} = 0.7\text{ V}$

Emitter voltage $V_E = V_B - V_{BEon} = -5.7\text{ V}$

Emitter Current $I_E = \dfrac{V_E - (-10)}{4.3\text{k}} = \dfrac{-5.7 - (-10)}{4.3\text{k}} = 1\text{ mA}$

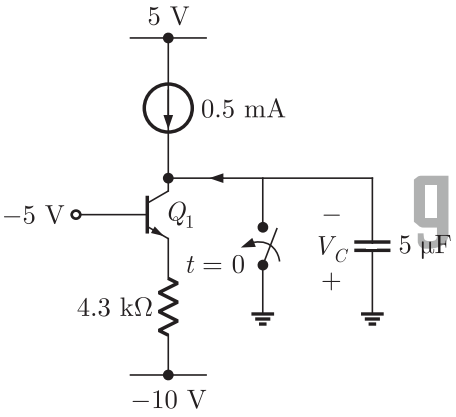
Now $I_C \approx I_E = 1\text{ mA}$

Applying KCL at collector

$$i_1 = 0.5\text{ mA}$$

Since $i_1 = C\dfrac{dV_C}{dt}$

or $V_C = \dfrac{1}{C}\int i_1\,dt = \dfrac{i_1}{C}t$ ...(1)



with time, the capacitor charges and voltage across collector changes from 0 towards negative.

When saturation starts, $V_{CE} = 0.7 \Rightarrow V_C = +5\text{ V}$ (across capacitor)

Thus from (1) we get, $+5 = \dfrac{0.5\text{ mA}}{5\,\mu\text{A}}\,T$

or $T = \dfrac{5 \times 5 \times 10^{-6}}{0.5 \times 10^{-3}} = 50\text{ m sec}$

Hence (C) is correct option.

SOL 4.6

The current flows in the circuit if all the diodes are forward biased. In forward biased there will be 0.7 V drop across each diode.

Thus $I_{DC} = \dfrac{12.7 - 4(0.7)}{9900} = 1\text{ mA}$

Hence (A) is correct option.

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SOL 4.7

The forward resistance of each diode is

$$r = \frac{V_T}{I_C} = \frac{25\,\text{mV}}{1\,\text{mA}} = 25\,\Omega$$

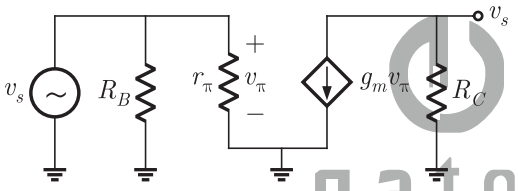
Thus $$V_{ac} = V_i \times \left(\frac{4(r)}{4(r)+9900}\right)$$

$$= 100\,\text{mV}\cos(\omega t)\,0.01 = 1\cos(\omega t)\,\text{mV}$$

Hence (B) is correct option.

SOL 4.8

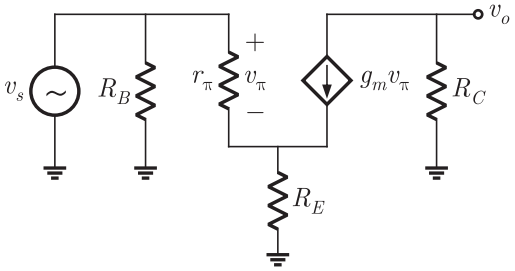
The equivalent circuit of given amplifier circuit (when C_E is connected, R_E is short-circuited)



Input impedance $R_i = R_B \,||\, r_\pi$

Voltage gain $A_V = g_m R_C$

Now, if C_E is disconnected, resistance R_E appears in the circuit



Input impedance $R_{\text{in}} = R_B \,||\, [r_\pi + (\beta+1)]\, R_E$

Input impedance increases

Voltage gain $A_V = \dfrac{g_m R_C}{1 + g_m R_E}$ Voltage gain decreases.

Hence (A) is correct option.

SOL 4.9

Since, emitter area of transistor Q_1 is half of transistor Q_2, so current

$$I_{E_1} = \frac{1}{2} I_{E_2} \text{ and } I_{B_1} = \frac{1}{2} I_{B_2}$$

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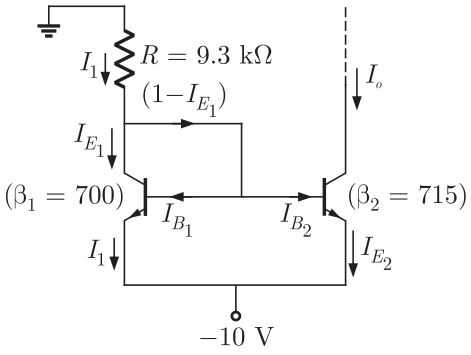
The circuit is as shown below :



$$V_B = -10 - (-0.7) = -9.3\ \text{V}$$

Collector current

$$I_1 = \frac{0-(-9.3)}{(9.3\,\text{k}\Omega)} = 1\,\text{mA}$$

$$\beta_1 = 700 \text{ (high)}, \text{ So } I_C \approx I_{E_1}$$

Applying KCL at base we have

$$1 - I_E = I_{B_1} + I_{B_2}$$

$$1 - (\beta_1 + 1)\, I_{B_1} = I_{B_1} + I_{B_2}$$

$$1 = (700 + 1 + 1)\frac{I_{B_2}}{2} + I_{B_2}$$

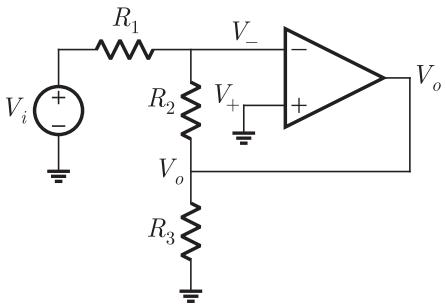
$$I_{B_2} \approx \frac{2}{702}$$

$$I_0 = I_{C_2} = \beta_2 \cdot I_{B_2} = 715 \times \frac{2}{702} \approx 2\,\text{mA}$$

Hence (B) is correct option.

SOL 4.10

The circuit is as shown below :



So, $$\frac{0 - V_i}{R_1} + \frac{0 - V_o}{R_2} = 0$$

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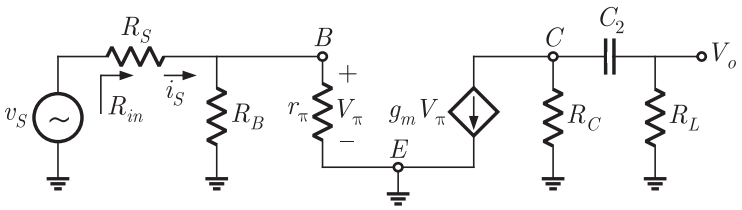
or $$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

Hence (A) is correct option.

SOL 4.11

By small signal equivalent circuit analysis



Input resistance seen by source v_s

$$R_{\text{in}} = \frac{v_s}{i_s} = R_s + R_s \,||\, r_s$$

$$= (1000\,\Omega) + (93\,\text{k}\Omega \,||\, 259\,\Omega) = 1258\,\Omega$$

Hence (B) is correct option.

SOL 4.12

Cut-off frequency due to C_2

$$f_o = \frac{1}{2\pi (R_C + R_L)\, C_2}$$

$$f_o = \frac{1}{2 \times 3.14 \times 1250 \times 4.7 \times 10^{-6}} = 271\,\text{Hz}$$

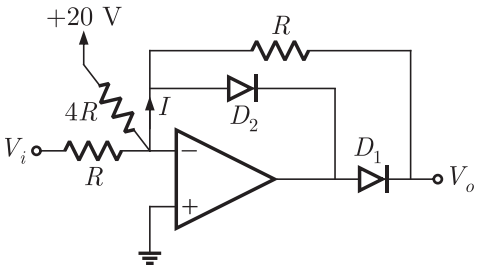
Lower cut-off frequency

$$f_L \approx \frac{f_o}{10} = \frac{271}{10} = 27.1\,\text{Hz}$$

Hence (B) is correct option.

SOL 4.13

The circuit is as shown below



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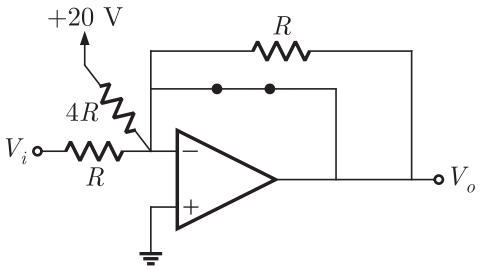
Current $I = \frac{20-0}{4R} + \frac{V_i - 0}{R} = \frac{5+V_i}{R}$

If $I > 0$, diode D_2 conducts

So, for $\frac{5+V_I}{2} > 0 \Rightarrow V_I > -5, D_2$ conducts

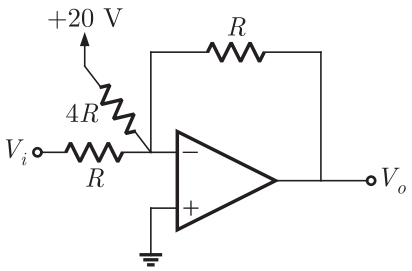
Equivalent circuit is shown below



Output is $V_o = 0$. If $I < 0$, diode D_2 will be off

$$\frac{5+V_I}{R} < 0 \Rightarrow V_I < -5, D_2 \text{ is off}$$

The circuit is shown below



$$\frac{0-V_i}{R} + \frac{0-20}{4R} + \frac{0-V_o}{R} = 0$$

or $V_o = -V_i - 5$

At $V_i = -5$ V, $V_o = 0$

At $V_i = -10$ V, $V_o = 5$ V

Hence (B) is correct option.

SOL 4.14

Let diode be OFF. In this case 1 A current will flow in resistor and voltage across resistor will be $V = 1.\text{V}$

Diode is off, it must be in reverse biased, therefore

$V_i - 1 > 0 \rightarrow V_i > 1$

Thus for $V_i > 1$ diode is off and $V = 1\,V$

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Option (B) and (C) doesn't satisfy this condition.
Let $V_i < 1$. In this case diode will be on and voltage across diode will be zero and $V = V_i$
Thus $V = \min(V_i, 1)$
Hence (A) is correct option.

SOL 4.15

The R_2 decide only the frequency.
Hence (A) is correct option

SOL 4.16

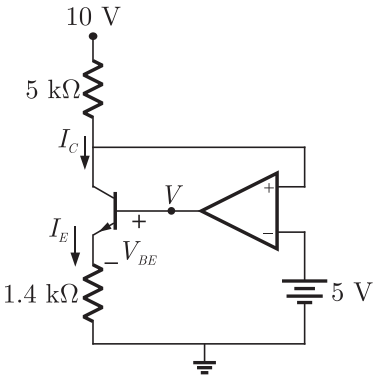
For small increase in V_G beyond 1 V the $n-$ channel MOSFET goes into saturation as $V_{GS} \rightarrow +\ ive$ and $p-$ MOSFET is always in active region or triode region.
Hence (D) is correct option.

SOL 4.17

Hence (C) is correct option.

SOL 4.18

The circuit is shown in fig below



The voltage at non inverting terminal is 5 V because OP AMP is ideal and inverting terminal is at 5 V.

Thus $I_C = \dfrac{10-5}{5k} = 1\text{ mA}$

$V_E = I_E R_E = 1m \times 1.4k = 1.4\,V$ $\qquad I_E = I_C$

$= 0.6 + 1.4 = 2\,V$

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Thus the feedback is negative and output voltage is $V = 2\,V$.
Hence (D) is correct option.

SOL 4.19

The output voltage is

$$V_0 = A_r\, V_i \approx -\frac{h_{fe} R_C}{h_{ie}}\, V_i$$

Here $R_C = 3\,\Omega$ and $h_{ie} = 3\,\text{k}\Omega$

Thus $$V_0 \approx -\frac{150 \times 3\text{k}}{3\text{k}}\, V_i$$

$$\approx -150\,(A\cos 20t + B\sin 10^6 t)$$

Since coupling capacitor is large so low frequency signal will be filtered out, and best approximation is

$$V_0 \approx -150B\sin 10^6 t$$

Hence (D) is correct option.

SOL 4.20

For the positive half of V_i, the diode D_1 is forward bias, D_2 is reverse bias and the zener diode is in breakdown state because $V_i > 6.8$.
Thus output voltage is

$$V_0 = 0.7 + 6.8 = 7.5\ \text{V}$$

For the negative half of V_i, D_2 is forward bias thus

Then $$V_0 = -0.7\ \text{V}$$

Hence (C) is correct option.

SOL 4.21

By Current mirror,

$$I_x = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{bias}$$

Since MOSFETs are identical,

Thus $$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_2$$

Hence $$I_x = I_{bias}$$

Hence (B) is correct option.

SOL 4.22

The circuit is using ideal OPAMP. The non inverting terminal of OPAMP is at ground, thus inverting terminal is also at virtual ground.

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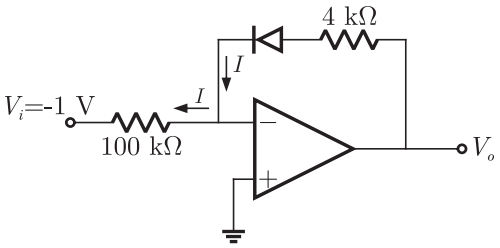


Thus current will flow from -ive terminal (0 Volt) to -1 Volt source. Thus the current I is

$$I = \frac{0-(-1)}{100k} = \frac{1}{100k}$$

The current through diode is

$$I = I_0\left(e^{\frac{V}{V_t}} - 1\right)$$

Now $V_T = 25$ mV and $I_0 = 1$ μA

Thus $$I = 10^{-6}\left[e^{\frac{V}{25\times 10^{-3}}} - 1\right] = \frac{1}{10^5}$$

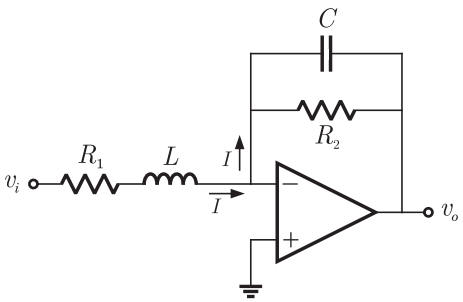
or $$V = 0.06 \text{ V}$$

Now $$V_0 = I\times 4\text{k} + V = \frac{1}{100k}\times 4k + 0.06 = 0.1 \text{ V}$$

Hence (B) is correct option.

SOL 4.23

The circuit is using ideal OPAMP. The non inverting terminal of OPAMP is at ground, thus inverting terminal is also at virtual ground.



Thus we can write

$$\frac{v_i}{R_1 + sL} = \frac{-v}{\frac{R_2}{sR_2C_2+1}}$$

or $$\frac{v_0}{v_i} = -\frac{R_2}{(R_1+sL)(sR_2C_2+1)}$$

and from this equation it may be easily seen that this is the standard form of T.F. of low pass filter

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$$H(s) = \frac{K}{(R_1 + sL)(sR_2C_2 + 1)}$$

and form this equation it may be easily seen that this is the standard form of T.F. of low pass filter

$$H(s) = \frac{K}{as^2 + bs + b}$$

Hence (B) is correct option.

SOL 4.24

The current in both transistor are equal. Thus g_m is decide by M_1. Hence (C) is correct option.

SOL 4.25

Let the voltage at non inverting terminal be V_1, then after applying KCL at non inverting terminal side we have

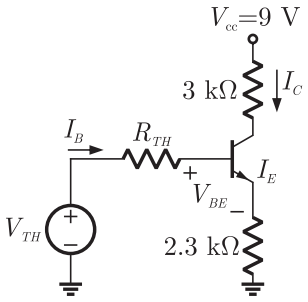
$$\frac{15 - V_1}{10} + \frac{V_0 - V_1}{10} = \frac{V_1 - (-15)}{10}$$

or $$V_1 = \frac{V_0}{3}$$

If V_0 swings from -15 to +15 V then V_1 swings between -5 V to +5 V. Hence (C) is correct option.

SOL 4.26

For the given DC values the Thevenin equivalent circuit is as follows



The thevenin resistance and voltage are

$$V_{TH} = \frac{10}{10 + 20} \times 9 = 3 \text{ V}$$

and total $$R_{TH} = \frac{10\text{k} \times 20\text{k}}{10\text{k} + 20\text{k}} = 6.67 \text{ k}\Omega$$

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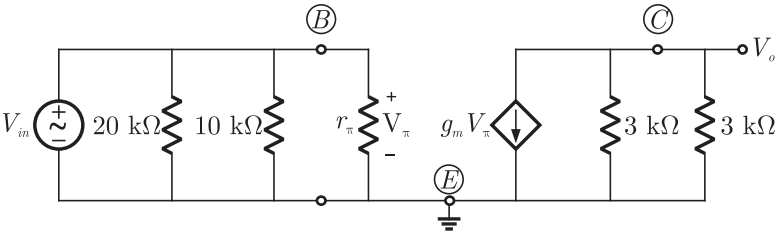
Since β is very large, therefore I_B is small and can be ignored

Thus $$I_E = \frac{V_{TH} - V_{BE}}{R_E} = \frac{3 - 0.7}{2.3k} = 1 \text{ mA}$$

Hence (A) is correct option.

SOL 4.27

The small signal model is shown in fig below



$$g_m = \frac{|I_C|}{V_T} = \frac{1\text{m}}{25\text{m}} = \frac{1}{25} \text{ A/V} \qquad I_C \approx I_E$$

$$V_o = -\, g_m V_\pi \times (3k \,\|\, 3k)$$

$$= -\frac{1}{25} V_{in} (1.5k) \qquad V_\pi = V_{in}$$

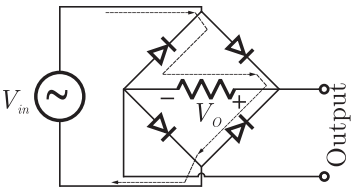
$$= -\, 60\, V_{in}$$

or $$A_m = \frac{V_o}{V_{in}} = -\, 60$$

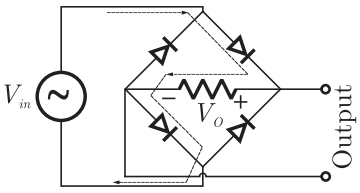
Hence (D) is correct option.

SOL 4.28

The circuit shown in (C) is correct full wave rectifier circuit.



During Negative Cycle



During Positive Cycle

Hence (C) is correct option.

SOL 4.29

In the transconductance amplifier it is desirable to have large input resistance and large output resistance.

Hence (A) is correct option.

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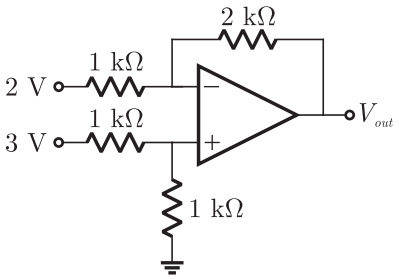
SOL 4.30

We redraw the circuit as shown in fig.



Applying voltage division rule

$$v_+ = 0.5 \text{ V}$$

We know that $v_+ = v_-$

Thus $v_- = 0.5$ V

Now $$i = \frac{1 - 0.5}{1k} = 0.5 \text{ mA}$$

and $$i = \frac{0.5 - v_0}{2k} = 0.5 \text{ mA}$$

or $$v_0 = 0.5 - 1 = -0.5 \text{ V}$$

Hence (C) is correct option.

SOL 4.31

If we assume β very large, then $I_B = 0$ and $I_E = I_C$; $V_{BE} = 0.7$ V. We assume that BJT is in active, so applying KVL in Base-emitter loop

$$I_E = \frac{2 - V_{BE}}{R_E} = \frac{2 - 0.7}{1k} = 1.3 \text{ mA}$$

Since β is very large, we have $I_E = I_C$, thus

$$I_C = 1.3 \text{ mA}$$

Now applying KVL in collector-emitter loop

$$10 - 10I_C - V_{CE} - I_C = 0$$

or $$V_{CE} = -4.3 \text{ V}$$

Now $$V_{BC} = V_{BE} - V_{CE}$$
$$= 0.7 - (-4.3) = 5 \text{ V}$$

Since $V_{BC} > 0.7$ V, thus transistor in saturation.

Hence (B) is correct option.

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SOL 4.32

Here the inverting terminal is at virtual ground and the current in resistor and diode current is equal i.e.

$$I_R = I_D$$

or $$\frac{V_i}{R} = I_s e^{V_D/V_T}$$

or $$V_D = V_T \ln \frac{V_i}{I_s R}$$

For the first condition

$$V_D = 0 - V_{o1} = V_T \ln \frac{2}{I_s R}$$

For the first condition

$$V_D = 0 - V_{o1} = V_T \ln \frac{4}{I_s R}$$

Subtracting above equation

$$V_{o1} - V_{o2} = V_T \ln \frac{4}{I_s R} - V_T \ln \frac{2}{I_s R}$$

or $$V_{o1} - V_{o2} = V_T \ln \frac{4}{2} = V_T \ln 2$$

Hence (D) is correct option.

SOL 4.33

We have $$V_{thp} = V_{thp} = 1 \text{ V}$$

and $$\frac{W_P}{L_P} = \frac{W_N}{L_N} = 40 \mu\text{A/V}^2$$

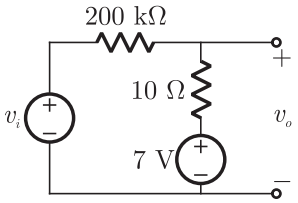
From figure it may be easily seen that V_{as} for each NMOS and PMOS is 2.5 V

Thus $$I_D = K(V_{as} - V_T)^2 = 40 \frac{\mu\text{A}}{\text{V}^2} (2.5 - 1)^2 = 90 \, \mu\text{A}$$

Hence (D) is correct option.

SOL 4.34

We have $V_Z = 7$ volt, $V_K = 0, R_Z = 10\Omega$
Circuit can be modeled as shown in fig below



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Since V_i is lies between 10 to 16 V, the range of voltage across 200 kΩ

$$V_{200} = V_i - V_Z = 3 \text{ to } 9 \text{ volt}$$

The range of current through 200 kΩ is

$$\frac{3}{200k} = 15 \text{ mA to } \frac{9}{200k} = 45 \text{ mA}$$

The range of variation in output voltage

$$15\text{m} \times R_Z = 0.15 \text{ V to } 45\text{m} \times R_Z = 0.45$$

Thus the range of output voltage is 7.15 Volt to 7.45 Volt

Hence (C) is correct option.

SOL 4.35

The voltage at non-inverting terminal is

$$V_+ = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_i = \frac{1}{1 + sCR} V_i$$

Now $$V_- = V_+ = \frac{1}{1 + sCR} V_i$$

Applying voltage division rule

$$V_+ = \frac{R_1}{R_1 + R_1}(V_0 + V_i) = \frac{(V_o + V_i)}{2}$$

or $$\frac{1}{1 + sCR} V_i = \frac{(V_o + V_i)}{2}$$

or $$\frac{V_o}{V_i} = -1 + \frac{2}{1 + sRC}$$

$$\frac{V_0}{V_i} = \frac{1 - sRC}{1 + sRC}$$

Hence (A) is correct option.

SOL 4.36

$$\frac{V_0}{V_i} = H(s) = \frac{1 - sRC}{1 + sRC}$$

$$H(j\omega) = \frac{1 - j\omega RC}{1 + j\omega RC}$$

$$\angle H(j\omega) = \phi = -\tan^{-1}\omega RC - \tan^{-1}\omega RC$$

$$= -2\tan^{-2}\omega RC$$

Minimum value, $\phi_{\min} = -\pi (\text{at } \omega \to \infty)$

Maximum value, $\phi_{\max} = 0 (\text{at } \omega = 0)$

Hence (C) is correct option.

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SOL 4.37

In the transconductance amplifier it is desirable to have large input impedance and large output impedance.
Hence (D) is correct option.

SOL 4.38

Hence (C) is correct option.

SOL 4.39

The voltage at inverting terminal is

$$V_- = V_+ = 10 \text{ V}$$

Here note that current through the capacitor is constant and that is

$$I = \frac{V_-}{1\text{k}} = \frac{10}{1\text{k}} = 10 \text{ mA}$$

Thus the voltage across capacitor at $t = 1$ msec is

$$V_C = \frac{1}{C}\int_0^{1m} I dt = \frac{1}{1\mu}\int_0^{1m} 10 m dt = 10^4 \int_0^{\text{Im}} dt = 10 \text{ V}$$

Hence (D) is correct option.

SOL 4.40

In forward bias Zener diode works as normal diode.
Thus for negative cycle of input Zener diode is forward biased and it conducts giving $V_R = V_{in}$.
For positive cycle of input Zener diode is reversed biased
when $0 < V_{in} < 6$, Diode is OFF and $V_R = 0$
when $V_{in} > 6$ Diode conducts and voltage across diode is 6 V. Thus voltage across is resistor is

$$V_R = V_{in} - 6$$

Only option (B) satisfy this condition.
Hence (A) is correct option.

SOL 4.41

The circuit under DC condition is shown in fig below

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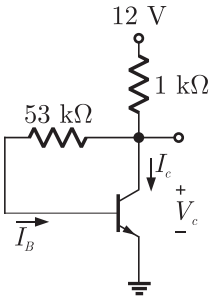

Applying KVL we have

$$V_{CC} - R_C(I_C + I_B) - V_{CE} = 0 \quad ...(1)$$

and $$V_{CC} - R_B I_B - V_{BE} = 0 \quad ...(2)$$

Substituting $I_C = \beta I_B$ in (1) we have

$$V_{CC} - R_C(\beta I_B + I_B) - V_{CE} = 0 \quad ...(3)$$

Solving (2) and (3) we get

$$V_{CE} = V_{CC} - \frac{V_{CC} - V_{BE}}{1 + \frac{R_B}{R_C(1+\beta)}} \quad ...(4)$$

Now substituting values we get

$$V_{CE} = 12 - \frac{12 - 0.7}{1 + \frac{53}{1 + (1 + 60)}} = 5.95 \text{ V}$$

Hence (C) is correct option.

SOL 4.42

We have $$\beta' = \frac{110}{100} \times 60 = 66$$

Substituting $\beta' = 66$ with other values in (iv) in previous solutions

$$V_{CE} = 12 - \frac{12 - 0.7}{1 + \frac{53}{1 + (1 + 66)}} = 5.29 \text{ V}$$

Thus change is $$= \frac{5.29 - 59.5}{5.95} \times 100 = -4.3\%$$

Hence (B) is correct option.

SOL 4.43

Hence (A) is correct option.

SOL 4.44

The Zener diode is in breakdown region, thus

$$V_+ = V_Z = 6 \text{ V} = V_{in}$$

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We know that $V_o = V_{in}\left(1 + \frac{R_f}{R_1}\right)$

or $V_{out} = V_o = 6\left(1 + \frac{12k}{24k}\right) = 9 \text{ V}$

The current in 12 kΩ branch is negligible as comparison to 10 Ω. Thus Current

$$I_C \approx I_E \approx = \frac{V_{out}}{R_L} = \frac{9}{10} = 0.9 \text{ A}$$

Now $V_{CE} = 15 - 9 = 6 \text{ V}$

The power dissipated in transistor is

$$P = V_{CE} I_C = 6 \times 0.9 = 5.4 \text{ W}$$

Hence (C) is correct option.

SOL 4.45

If the unregulated voltage increase by 20%, them the unregulated voltage is 18 V, but the $V_Z = V_{in} = 6$ remain same and hence V_{out} and I_C remain same. There will be change in V_{CE}

Thus, $V_{CE} = 18 - 9 = 9 \text{ V}$

$I_C = 0.9 \text{ A}$

Power dissipation $P = V_{CE} I_C = 9 \times 0.9 = 8.1 \text{ W}$

Thus % increase in power is

$$\frac{8.1 - 5.4}{5.4} \times 100 = 50\%$$

Hence (B) is correct option.

SOL 4.46

Since the inverting terminal is at virtual ground, the current flowing through the voltage source is

$$I_s = \frac{V_s}{10\text{k}}$$

or $$\frac{V_s}{I_s} = 10 \text{ k}\Omega = R_{in}$$

Hence (B) is correct option.

SOL 4.47

The effect of current shunt feedback in an amplifier is to decrease the input resistance and increase the output resistance as :

$$R_{if} = \frac{R_i}{1 + A\beta}$$

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$$R_{of} = R_0(1 + A\beta)$$

where $R_i \rightarrow$ Input resistance without feedback

$R_{if} \rightarrow$ Input resistance with feedback.

Hence (D) is correct option.

SOL 4.48

The CE configuration has high voltage gain as well as high current gain. It performs basic function of amplifications. The CB configuration has lowest R_i and highest R_o. It is used as last step to match a very low impedance source and to drain a high impedance load

Thus cascade amplifier is a multistage configuration of CE-CB

Hence (B) is correct option

SOL 4.49

Common mode gain

$$A_{CM} = -\frac{R_C}{2R_E}$$

And differential mode gain

$$A_{DM} = -\, g_m R_C$$

Thus only common mode gain depends on R_E and for large value of R_E it decreases.

Hence (D) is correct option.

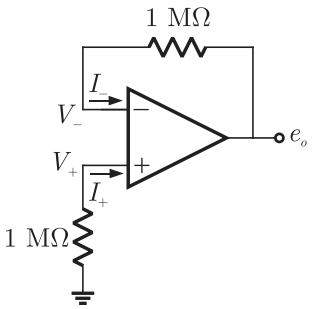
SOL 4.50

$$I_E = I_s\left(e^{\frac{V_{BE}}{nV_T}} - 1\right) = 10^{-13}\left(\frac{0.7}{e^{1\times 26\times 10^{-3}}} - 1\right) = 49 \text{ mA}$$

Hence (C) is correct option.

SOL 4.51

The circuit is as shown below



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Writing equation for I_- have

$$\frac{e_0 - V_-}{1\text{M}} = I_-$$

or $$e_0 = I_-(1\text{M}) + \text{V}_- \quad ...(1)$$

Writing equation for I_+ we have

$$\frac{0 - V_+}{1\text{M}} = I_+$$

or $$V_+ = -\, I_+(1\text{M}) \quad ...(2)$$

Since for ideal OPAMP $V_+ = V_-$, from (1) and (2) we have

$$e_0 = I_-(1\text{M}) - \text{I}_+(1\text{M})$$
$$= (I_- - I_+)(1\text{M}) = I_{OS}(1\text{M})$$

Thus if e_0 has been measured, we can calculate input offset current I_{OS} only.

Hence (C) is correct option.

SOL 4.52

At low frequency capacitor is open circuit and voltage acr s non-inverting terminal is zero. At high frequency capacitor act as short circuit and all input voltage appear at non-inverting terminal. Thus, this is high pass circuit.

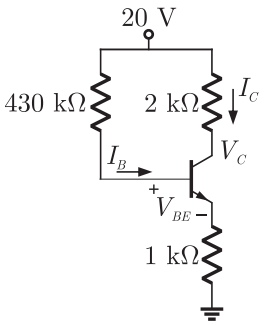
The frequency is given by

$$\omega = \frac{1}{RC} = \frac{1}{1\times10^3\times1\times10^{-6}} = 1000 \text{ rad/sec}$$

Hence (C) is correct option.

SOL 4.53

The circuit under DC condition is shown in fig below



Applying KVL we have

$$V_{CC} - R_B I_B - V_{BE} - R_E I_E = 0$$

or $$V_{CC} - R_B I_B - V_{BE} - R_E(\beta+1) I_B = 0 \quad \text{Since } I_E = I_B + \beta I_B$$

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or $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$= \frac{20 - 0.7}{430\text{k} + (50 + 1)1\,\text{k}} = 40\mu\text{A}$$

Now $$I_C = \beta I_B = 50 \times 40\mu = 2 \text{ mA}$$

$$V_C = V_{CC} - R_C I_C = 20 - 2\text{m} \times 2\text{k} = 16 \text{ V}$$

Hence (B) is correct option.

SOL 4.54

The maximum load current will be at maximum input voltage i.e.

$$V_{\max} = 30 \text{ V i.e.}$$

$$\frac{V_{\max} - V_Z}{1\text{k}} = I_L + I_Z$$

or $$\frac{30 - 5.8}{1\text{k}} = I_L = 0.5 \text{ m}$$

or $$I_L = 24.2 - 0.5 = 23.7 \text{ mA}$$

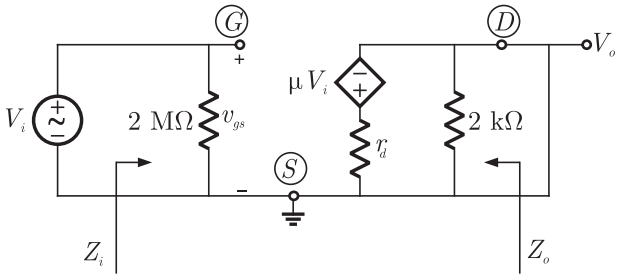
Hence (A) iscorrect option.

SOL 4.55

Hence (D) is correct option.

SOL 4.56

The small signal model is as shown below



From the figure we have

$$Z_{in} = 2\,\text{M}\Omega$$

and $$Z_0 = r_d \| R_D = 20\text{k} \| 2\text{k} = \frac{20}{11}\,\text{k}\Omega$$

Hence (B) is correct option.

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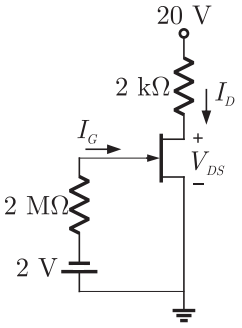
SOL 4.57

The circuit in DC condition is shown below



Since the FET has high input resistance, gate current can be neglect and we get $V_{GS} = -2$ V

Since $V_P < V_{GS} < 0$, FET is operating in active region

Now $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\left(1 - \frac{(-2)}{(-8)}\right)^2 = 5.625 \text{ mA}$$

Now $$V_{DS} = V_{DD} - I_D R_D = 20 - 5.625\text{m} \times 2\text{k} = 8.75 \text{ V}$$

Hence (A) is correct option.

SOL 4.58

The transconductance is

$$g_m = \frac{2}{|V_P|\sqrt{I_D I_{DSS}}}$$

or, $$= \frac{2}{8}\sqrt{5.625\text{mA} \times 10\text{mA}} = 1.875 \text{ mS}$$

The gain is $$A = -g_m(r_d \| R_D)$$

So, $$= 1.875\text{ms} \times \frac{20}{11}K = -3.41$$

Hence (B) is correct option.

SOL 4.59

Only one diode will be in ON conditions

When lower diode is in ON condition, then

$$V_u = \frac{2\text{k}}{2.5\text{k}} V_{sat} = \frac{2}{2.5}10 = 8 \text{ V}$$

when upper diode is in ON condition

$$V_u = \frac{2\text{k}}{2.5\text{k}} V_{sat} = \frac{2}{4}(-10) = -5 \text{ V}$$

Hence (B) is correct option.

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SOL 4.60

An ideal OPAMP is an ideal voltage controlled voltage source.
Hence (B) is correct option.

SOL 4.61

In voltage series feed back amplifier, input impedance increases by factor $(1 + A\beta)$ and output impedance decreases by the factor $(1 + A\beta)$.

$$R_{if} = R_i(1 + A\beta)$$
$$R_{of} = \frac{R_o}{(1 + A\beta)}$$

Hence (C) is correct option.

SOL 4.62

This is a Low pass filter, because

At $\omega = \infty$ $\quad \dfrac{V_0}{V_{in}} = 0$

and at $\omega = 0$ $\quad \dfrac{V_0}{V_{in}} = 1$

Hence (A) is correct option.

SOL 4.63

When $|I_C| >> |I_{CO}|$

$$g_m = \frac{|I_C|}{V_T} = \frac{1\text{mA}}{25\text{mV}} = 0.04 = 40 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{40 \times 10^{-3}} = 2.5 \text{ k}\Omega$$

Hence (D) is correct option.

SOL 4.64

The given circuit is wein bridge oscillator. The frequency of oscillation is

$$2\pi f = \frac{1}{RC}$$

or $$C = \frac{1}{2\pi Rf} = \frac{1}{2\pi \times 10^3 \times 10^3} = \frac{1}{2\pi}\mu$$

Hence (A) is correct option.

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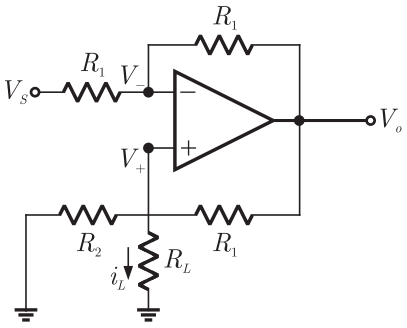
SOL 4.65

The circuit is as shown below



We know that for ideal OPAMP

$$V_- = V_+$$

Applying KCL at inverting terminal

$$\frac{V_- - V_s}{R_1} + \frac{V_- - V_0}{R_1} = 0$$

or $$2V_- - V_o = V_s \qquad ...(1)$$

Applying KCL at non-inverting terminal

$$\frac{V_+}{R_2} + I_L + \frac{V_+ - V_o}{R_2} = 0$$

or $$2V_+ - V_o + I_L R_2 = 0 \qquad ...(2)$$

Since $V_- = V_+$, from (1) and (2) we have

$$V_s + I_L R_2 = 0$$

or $$I_L = -\frac{V_s}{R_2}$$

Hence (A) is correct option.

SOL 4.66

If I_Z is negligible the load current is

$$\frac{12 - V_z}{R} = I_L$$

as per given condition

$$100 \text{ mA} \le \frac{12 - V_Z}{R} \le 500 \text{ mA}$$

At $I_L = 100$ mA $\dfrac{12-5}{R} = 100$ mA $\qquad V_Z = 5$ V

or $$R = 70\Omega$$

At $I_L = 500$ mA $\dfrac{12-5}{R} = 500$ mA $\qquad V_Z = 5$ V

or $$R = 14\,\Omega$$

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Thus taking minimum we get

$$R = 14\,\Omega$$

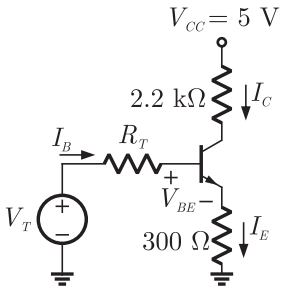
Hence (D) is correct option.

SOL 4.67

Hence (B) is correct option.

SOL 4.68

The thevenin equivalent is shown below



$$V_T = \frac{R_1}{R_1 + R_2} V_C = \frac{1}{4+1} \times 5 = 1 \quad \text{V}$$

Since β is large is large, $I_C \approx I_E$, $I_B \approx 0$ and

$$I_E = \frac{V_T - V_{BE}}{R_E} = \frac{1 - 0.7}{300} = 3 \text{ mA}$$

Now
$$\begin{aligned} V_{CE} &= 5 - 2.2\text{k}I_C - 300I_E \\ &= 5 - 2.2\text{k} \times 1\text{m} - 300 \times 1\text{m} \\ &= 2.5 \text{ V} \end{aligned}$$

Hence (C) is correct option

SOL 4.69

For the different combinations the table is as follows

CE	*CE*	*CC*	*CB*
A_i	High	High	Unity
A_v	High	Unity	High
R_i	Medium	High	Low
R_o	Medium	Low	High

Hence (B) is correct option.

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SOL 4.70

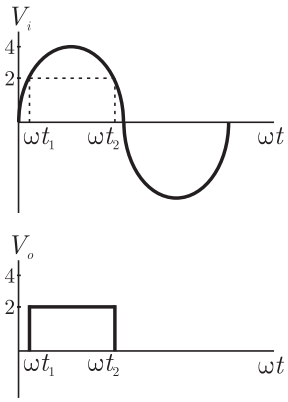
This circuit having two diode and capacitor pair in parallel, works as voltage doubler.
Hence (D) is correct option.

SOL 4.71

If the input is sinusoidal signal of 8 V (peak to peak) then

$$V_i = 4\sin\omega t$$

The output of comparator will be high when input is higher than $V_{ref} = 2$ V and will be low when input is lower than $V_{ref} = 2$ V. Thus the waveform for input is shown below



From fig, first crossover is at ωt_1 and second crossover is at ωt_2 where

$$4\sin\omega t_1 = 2V$$

Thus

$$\omega t_1 = \sin^{-1}\frac{1}{2} = \frac{\pi}{6}$$

$$\omega t_2 = \pi - \frac{\pi}{6} = \frac{5\pi}{6}$$

$$\text{Duty Cycle} = \frac{\frac{5\pi}{6} - \frac{\pi}{6}}{2\pi} = \frac{1}{3}$$

Thus the output of comparators has a duty cycle of $\frac{1}{3}$.

Hence (B) is correct option.

SOL 4.72

$$CMMR = \frac{A_d}{A_c}$$

or

$$20\log CMMR = 20\log A_d - 20\log A_c$$
$$= 48 - 2 = 46 \text{ dB}$$

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Where $A_d \rightarrow$Differential Voltage Gain
and $A_C \rightarrow$ Common Mode Voltage Gain
Hence (C) is correct option.

SOL 4.73

The gain of amplifier is

$$A_i = \frac{-g_m}{g_b + j\omega C}$$

Thus the gain of a transistor amplifier falls at high frequencies due to the internal capacitance that are diffusion capacitance and transition capacitance.
Hence (B) is correct option.

SOL 4.74

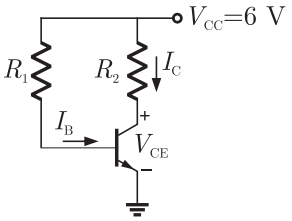
We have $R_i = 1\text{k}\Omega, \beta = 0.2, A = 50$

Thus, $$R_{if} = \frac{R_i}{(1 + A\beta)} = \frac{1}{11}\text{k}\Omega$$

Hence (A) is correct option.

SOL 4.75

The DC equivalent circuit is shown as below. This is fixed bias circuit operating in active region.



In first case

$$V_{CC} - I_{C1}R_2 - V_{CE1} = 0$$

or $$6 - 1.5\text{m}R_2 - 3 = 0$$

or $$R_2 = 2k\Omega$$

$$I_{B1} = \frac{I_{C1}}{\beta_1} = \frac{1.5\text{m}}{150} = 0.01 \text{ mA}$$

In second case I_{B2} will we equal to I_{B1} as there is no in R_1.

Thus $$I_{C2} = \beta_2 I_{B2} = 200 \times 0.01 = 2 \text{ mA}$$

$$V_{CE2} = V_{CC} - I_{C2}R_2 = 6 - 2\text{m} \times 2\,\text{k}\Omega = 2 \text{ V}$$

Hence (A) is correct option.

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SOL 4.76

The given circuit is a $R-C$ phase shift oscillator and frequency of its oscillation is

$$f = \frac{1}{2\pi\sqrt{6}\,RC}$$

Hence (A) is correct option.

SOL 4.77

If we see th figure we find that the voltage at non-inverting terminal is 3 V by the zener diode and voltage at inverting terminal will be 3 V. Thus V_o can be get by applying voltage division rule, i.e.

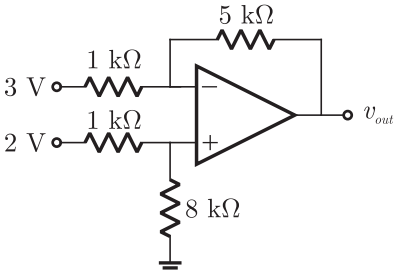
$$\frac{20}{20+40}V_o = 3$$

or $$V_0 = 9 \text{ V}$$

Hence (C) is correct option.

SOL 4.78

The circuit is as shown below



$$V_+ = \frac{8}{1+8}(3) = \frac{8}{3}\text{k}\Omega$$

$$V_+ = V_- = \frac{8}{3}V$$

Now applying KCL at inverting terminal we get

$$\frac{V_- - 2}{1} + \frac{V_- - V_o}{5} = 0$$

or $$V_o = 6V_- - 10$$
$$= 6 \times \frac{8}{3} - 10 = 6 \text{ V}$$

Hence (B) is correct option.

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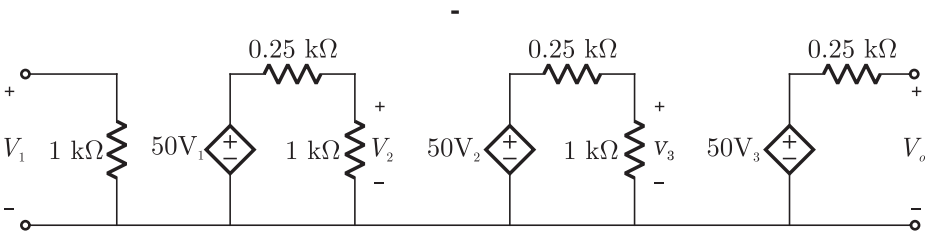
SOL 4.79

The equivalent circuit of 3 cascade stage is as shown in fig.



$$V_2 = \frac{1k}{1k + 0.25k} 50\, V_1 = 40\, V_1$$

Similarly $$V_3 = \frac{1k}{1k + 0.25k} 50\, V_2 = 40\, V_2$$

or $$V_3 = 40 \times 40\, V_1$$

$$V_o = 50\, V_3 = 50 \times 40 \times 40\, V_1$$

or $$A_V = \frac{V_o}{V_1} = 50 \times 40 \times 40 = 8000$$

or $$20 \log A_V = 20 \log 8000 = 98 \text{ dB}$$

Hence (C) is correct option.

SOL 4.80

If a constant current is made to flow in a capacitor, the output voltage is integration of input current and that is sawtooth waveform as below :

$$V_C = \frac{1}{C} \int_0^t i dt$$

The time period of wave form is

$$T = \frac{1}{f} = \frac{1}{500} = 2 \text{ m sec}$$

Thus $$3 = \frac{1}{2 \times 10^6} \int_0^{20 \times 10^{-3}} i dt$$

or $$i(2 \times 10^{-3} - 0) = 6 \times 10^{-6}$$

or $$i = 3 \text{ mA}$$

Thus the charging require 3 mA current source for 2 msec.

Hence (D) is correct option.

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SOL 4.81

In voltage-amplifier or voltage-series amplifier, the R_i increase and R_o decrease because

$$R_{if} = R_i(1 + A\beta)$$
$$R_{of} = \frac{R_o}{(1 + A\beta)}$$

Hence (C) is correct option.

SOL 4.82

Let x be the gain and it is 20 db, therefore

$$20 \log x = 20$$

or $$x = 10$$

Since Gain band width product is 10^6 Hz, thus

So, bandwidth is $$BW = \frac{10^6}{\text{Gain}} = \frac{10^6}{10} = 10^5 \text{ Hz} = 100 \text{ kHz}$$

Hence (B) is correct option.

SOL 4.83

In multistage amplifier bandwidth decrease and overall gain increase. From bandwidth point of view only options (A) may be correct because lower cutoff frequency must be increases and higher must be decreases. From following calculation we have

We have $f_L = 20$ Hz and $f_H = 1$ kHz

For n stage amplifier the lower cutoff frequency is

$$f_{Ln} = \frac{f_L}{\sqrt{2^{\frac{1}{n}} - 1}} = \frac{20}{\sqrt{2^{\frac{1}{3}} - 1}} = 39.2 \approx 40 \text{ Hz}$$

The higher cutoff frequency is

$$f_{Hn} = f_H \sqrt{2^{\frac{1}{2}} - 1} = 0.5 \text{ kHz}$$

Hence (A) is correct option.

SOL 4.84

As per Barkhousen criterion for sustained oscillations $|A\beta| \geq 1$ and phase shift must be or $2\pi n$.

Now from circuit $$A = \frac{V_O(f)}{V_f(f)} = 1 + \frac{R_2}{R_1}$$

$$\beta(f) = \frac{1}{6} \angle 0 = \frac{V_f(f)}{V_O(f)}$$

Thus from above equation for sustained oscillation

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$$6 = 1 + \frac{R_2}{R_1}$$

or $$R_2 = 5R_1$$

Hence (A) is correct option.

SOL 4.85

Let the gain of OPAMP be A_V then we have

$$20 \log A_V = 40 \text{ dB}$$

or $$A_V = 100$$

Let input be $V_i = V_m \sin \omega t$ then we have

$$V_O = V_V V_i = V_m \sin \omega t$$

Now $$\frac{dV_O}{dt} = A_V V_m \omega \cos \omega t$$

Slew Rate $$\left(\frac{dV_O}{dt}\right)_{\max} = A_V V_m \omega = A_V V_m 2\pi f$$

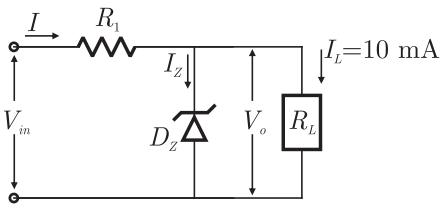
or $$V_m = \frac{SR}{A_V V 2\pi f} = \frac{1}{10^{-6} \times 100 \times 2\pi \times 20 \times 10^3}$$

or $$V_M = 79.5 \text{ mV}$$

Hence (C) is correct option.

SOL 4.86

The circuit is shown as below



$$I = I_Z + I_L$$

For satisfactory operations

$$\frac{V_{in} - V_0}{R} > I_Z + I_L \qquad [I_Z + I_L = I]$$

When $V_{in} = 30$ V,

$$\frac{30 - 10}{R} \geq (10 + 1) \text{ mA}$$

or $$\frac{20}{R} \geq 11 \text{ mA}$$

or $$R \leq 1818\ \Omega$$

when $V_{in} = 50$ V

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$$\frac{50-10}{R} \geq (10+1)\ \text{mA}$$

$$\frac{40}{R} \geq 11\times10^{-3}$$

or $$R \leq 3636\Omega$$

Thus $R \leq 1818\Omega$

Hence (A) is correct option.

SOL 4.87

We have

$$I_{DSS} = 10\ \text{mA and } V_P = -5\ \text{V}$$

Now $$V_G = 0$$

and $$V_S = I_D R_S = 1\times2.5\Omega = 2.5\ \text{V}$$

Thus $$V_{GS} = V_G - V_S = 0 - 2.5 = -2.5\ \text{V}$$

Now $$g_m = \frac{2I_{DSS}}{|V_P|}\left[1-\left(\frac{-2.5}{-5}\right)\right] = 2\ \text{mS}$$

$$A_V = \frac{V_0}{V_i} = -g_m R_D$$

So, $$= -2ms\times3k = -6$$

Hence (D) is correct option.

SOL 4.88

The current gain of a BJT is

$$h_{fe} = g_m r_\pi$$

Hence (C) is correct option.

SOL 4.89

The ideal op-amp has following characteristic :

$$R_i \to \infty$$

$$R_0 \to 0$$

and $$A \to \infty$$

Hence (A) is correct option.

SOL 4.90

Both statements are correct because

(1) A stable multivibrator can be used for generating square wave, because of its characteristic

(2) Bi-stable multivibrator can store binary information, and this

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multivibrator also give help in all digital kind of storing.
Hence (C) is correct option.

SOL 4.91

If f_T is the frequency at which the short circuit common emitter gain attains unity magnitude then

$$f_T = \frac{g_m}{2\pi(C_\mu + C_\pi)} = \frac{38\times10^{-3}}{2\pi\times(10^{-14}+4\times10^{-13})}$$

or $$= 1.47\times10^{10} \text{ Hz}$$

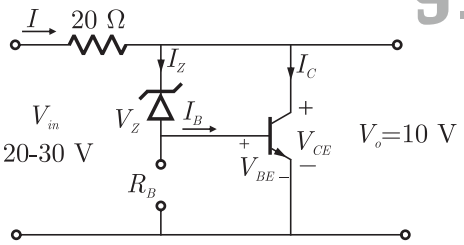
If f_B is bandwidth then we have

$$f_B = \frac{f_T}{\beta} = \frac{1.47\times10^{10}}{90} = 1.64\times10^{8} \text{ Hz}$$

Hence (B) is correct option.

SOL 4.92

If we neglect current through R_B then it can be open circuit as shown in fig.



Maximum power will dissipate in Zener diode when current through it is maximum and it will occur at $V_{in} = 30$ V

$$I = \frac{V_{in} - V_o}{20} = \frac{30-10}{20} = 1 \text{ A}$$

$$I \quad I_C + I_Z = \beta I_B + I_Z \qquad \text{Since } I_C = \beta I_B$$

$$= \beta I_Z + I_Z = (\beta+1) I_Z \qquad \text{since } I_B = I_Z$$

or $$I_Z = \frac{I}{\beta+1} = \frac{1}{99+1} = 0.01 \text{ A}$$

Power dissipated in zener diode is

$$P_Z = V_Z I_Z = 9.5\times0.01 = 95 \text{ mW}$$

$$I_C = \beta I_Z = 99\times0.1 = 0.99 \text{ A}$$

$$V_{CE} = V_o = 10 \text{ V}$$

Power dissipated in transistor is

$$P_T = V_C I_C = 10\times0.99 = 9.9 \text{ W}$$

Hence (C) is correct option.

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SOL 4.93

From the it may be easily seen that the tank circuit is having 2-capacitors and one-inductor, so it is colpits oscillator and frequency is

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

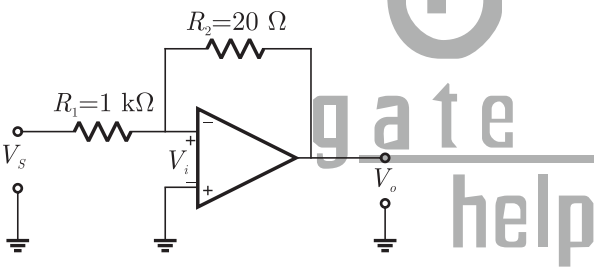
$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{2\times 2}{4} = 1 \text{ pF}$$

$$f = \frac{1}{2\pi\sqrt{10\times 10^{-6}\times 10^{-12}}} = \frac{1\times 10^{9}}{2\pi\sqrt{10}} = 50.3 \text{ MHz}$$

Hence (B) is correct option.

SOL 4.94

The circuit is as shown below



Let V_- be the voltage of inverting terminal, since non inverting terminal a at ground, the output voltage is

$$V_o = A_{OL} V_- \qquad ...(1)$$

Now applying KCL at inverting terminal we have

$$\frac{V_- - V_s}{R_1} + \frac{V_- - V_0}{R_2} = 0 \qquad ...(2)$$

From (1) and (2) we have

$$\frac{V_O}{V_s} = A_{CL} = \frac{-R_2}{R - \dfrac{R_2 + R_1}{R_{OL}}}$$

Substituting the values we have

$$A_{CL} = \frac{-10\text{k}}{1k - \dfrac{10\text{k} + 1\text{k}}{100\text{k}}} = -\frac{1000}{89} \approx -11$$

Hence (D) is correct option.

SOL 4.95

The first OPAMP stage is the differentiator and second OPAMP stage is integrator. Thus if input is cosine term, output will be also

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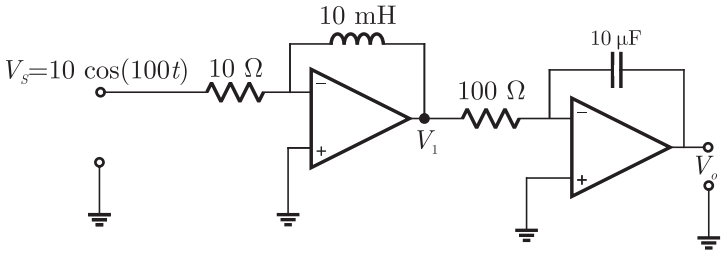
cosine term. Only option (A) is cosine term. Other are sine term. However we can calculate as follows. The circuit is shown in fig



Applying KCL at inverting terminal of first OP AMP we have

$$\frac{V_1}{V_S} = \frac{-\omega jL}{R} = \frac{-100 \times 10 \times 10^{-3}}{10} = \frac{-1}{10}$$

or $$V_1 = \frac{-jV_S}{10} = j\cos 100t$$

Applying KCL at inverting terminal of second OP AMP we have

$$\frac{V_O}{V_1} = \frac{-1/j\omega C}{100}$$

$$= -\frac{1}{j100 \times 10 \times 10^{-6} \times 100} = j10$$

or $$V_0 = j10\, V_2 = j10\,(-j\cos 100t)$$

$$V_0 = 10\cos 100t$$

Hence (A) is correct option.

SOL 4.96

Common mode gain is

$$A_C = \frac{\alpha R_C}{R_{EE}}$$

Since source resistance of the current source is infinite $R_{EE} = \infty$, common mode gain $A_C = 0$

Hence (A) is correct option.

SOL 4.97

In positive feed back it is working as OP-AMP in saturation region, and the input applied voltage is +ve.

So, $$V_0 = +\, V_{sat} = 15 \text{ V}$$

Hence (D) is correct option.

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SOL 4.98

With the addition of R_E the DC abis currents and voltages remain closer to the point where they were set by the circuit when the outside condition such as temperature and transistor parameter β change.
Hence (C) is correct option.

SOL 4.99

At high frequency

$$A_i = -\frac{g_m}{g_{bc}' + j\omega(C)}$$

or, $$A_i \propto \frac{1}{\text{Capacitance}}$$

and $$A_i \ \alpha \frac{1}{\text{frequency}}$$

Thus due to the transistor capacitance current gain of a bipolar transistor drops.
Hence (A) is correct option.

SOL 4.100

As OP-AMP is ideal, the inverting terminal at virtual ground due to ground at non-inverting terminal. Applying KCL at inverting terminal

$$sC(v_1 \sin\omega t - 0) + sC(V_2 \sin\omega t - 0) + sC(V_o - 0) = 0$$

or $$V_o = -(V_1 + V_2)\sin\omega t$$

Hence (C) is correct option.

SOL 4.101

There is $R-C$, series connection in parallel with parallel $R-C$ combination. So, it is a wein bridge oscillator because two resistors R_1 and R_2 is also in parallel with them.
Hence (D) is correct option.

SOL 4.102

The given circuit is a differentiator, so the output of triangular wave will be square wave.
Hence (A) is correct option.

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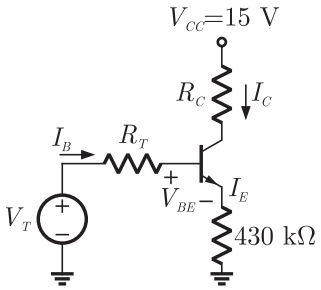
SOL 4.103

In sampling and hold circuit the unity gain non-inverting amplifier is used.

Hence (B) is correct option.

SOL 4.104

The thevenin equivalent is shown below



$$V_T = \frac{R_1}{R_1 + R_2} V_C = \frac{5}{10+5} \times 15 = 5 \text{ V}$$

Since β is large is large, $I_C \approx I_E, I_B \approx 0$ and

$$I_E = \frac{V_T - V_{BE}}{R_E}$$

$$= \frac{5 - 0.7}{0.430k\Omega} = \frac{4.3}{0.430K\Omega} = 10 \text{ mA}$$

Hence (D) is correct option.

SOL 4.105

The output voltage will be input offset voltage multiplied by open by open loop gain. Thus

So $V_0 = 5\text{mV} \times 10,000 = 50 \text{ V}$

But $V_0 = \pm 15 \text{ V}$ in saturation condition

So, it can never be exceeds ± 15 V

So, $V_0 = \pm V_{set} = \pm 15 V$

Hence (C) is correct option.

SOL 4.106

Hence (A) is correct option.

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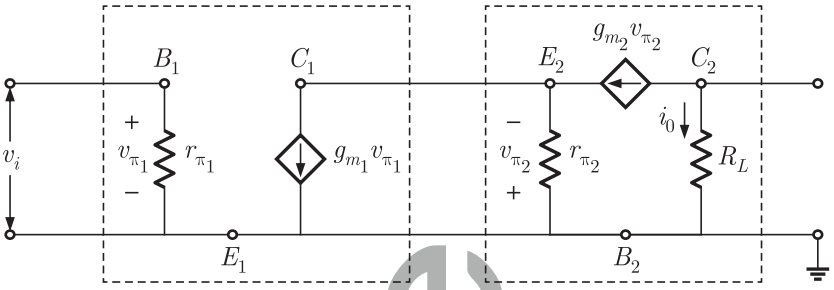
SOL 4.107

Negative feedback in amplifier reduces the gain of the system.
Hence (A) is correct option.

SOL 4.108

By drawing small signal equivalent circuit



by applying KCL at E_2

$$g_{m1} V_{\pi_1} - \frac{V_{\pi_2}}{r_{\pi_2}} = g_{m2} V_{\pi_2}$$

at C_2 $\quad i_0 = - g_{m2} V_{\pi_2}$

from eq (1) and (2)

$$g_{m1} V_{\pi_1} + \frac{i_0}{g_{m2} r_{\pi_2}} = - i_0$$

$$g_{m1} V_{\pi_1} = - i_0 \left[1 + \frac{1}{g_{m2} r_{\pi_2}}\right]$$

$$g_{m2} r_{\pi_2} = \beta >> 1$$

so $\quad g_{m1} V_{\pi_1} = - i_0$

$$\frac{i_0}{V_{\pi_1}} = - g_{m1}$$

$$\left|\frac{i_0}{V_i}\right| = g_{m1} \qquad \because \quad V_{\pi_1} = V_i$$

Hence (A) is correct option.

SOL 4.109

Crossover behavior is characteristic of calss B output stage. Here 2 transistor are operated one for amplifying +ve going portion and other for -ve going portion.
Hence (B) is correct option.

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SOL 4.110

In Voltage series feedback mode input impedance is given by

$$R_{\text{in}} = R_i(1 + \beta_v A_v)$$

where $\beta_v =$ feedback factor,

$A_v =$ openloop gain

and $R_i =$ Input impedance

So, $R_{\text{in}} = 1 \times 10^3(1 + 0.99 \times 100) = 100\,\text{k}\Omega$

Similarly output impedance is given by

$$R_{\text{OUT}} = \frac{R_0}{(1 + \beta_v A_v)} \qquad R_0 = \text{output impedance}$$

Thus $$R_{\text{OUT}} = \frac{100}{(1 + 0.99 \times 100)} = 1\,\Omega$$

Hence (C) is correct option.

SOL 4.111

$$\text{Regulation} = \frac{V_{\text{no-load}} - V_{\text{fuel-load}}}{V_{\text{full-load}}}$$

$$= \frac{30 - 25}{25} \times 100 = 20\%$$

$$\text{Output resistance} = \frac{25}{1} = 25\,\Omega$$

Hence (B) is correct option.

SOL 4.112

This is a voltage shunt feedback as the feedback samples a portion of output voltage and convert it to current (shunt).

Hence (D) is correct option.

SOL 4.113

In a differential amplifier CMRR is given by

$$\text{CMRR} = \frac{1}{2}\left[1 + \frac{(1 + \beta)\, I_Q R_0}{V_T \beta}\right]$$

So where R_0 is the emitter resistance. So CMRR can be improved by increasing emitter resistance.

Hence (A) is correct option.

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SOL 4.114

We know that rise time (t_r) is

$$t_r = \frac{0.35}{f_H}$$

where f_H is upper 3 dB frequency. Thus we can obtain upper 3 dB frequency it rise time is known.
Hence (C) is correct option.

SOL 4.115

In a BJT differential amplifier for a linear response $V_{id} < V_T$.
Hence (D) is correct option.

SOL 4.116

In a shunt negative feedback amplifier.
Input impedance

$$R_{\text{in}} = \frac{R_i}{(1+\beta A)}$$

where R_i = input impedance of basic amplifier
β = feedback factor
A = open loop gain

So, $R_{\text{in}} < R_i$
Similarly

$$R_{\text{OUT}} = \frac{R_0}{(1+\beta A)}$$

$R_{\text{OUT}} < R_0$
Thus input & output impedances decreases.
Hence (D) is correct option.

SOL 4.117

Hence (A) is correct option.

SOL 4.118

Comparator will give an output either equal to $+V_{\text{supply}}$ or $-V_{\text{supply}}$.
So output is a square wave.
Hence (D) is correct option.

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SOL 4.119

In series voltage regulator the pass transistor is in common collector configuration having voltage gain close to unity.
Hence (C) is correct option.

SOL 4.120

In bridge rectifier we do not need central tap transformer, so its less expensive and smaller in size and its PIV (Peak inverse voltage) is also greater than the two diode circuit, so it is also suitable for higher voltage application.
Hence (D) is correct option.

SOL 4.121

In the circuit we have

$$V_2 = I_S \times \frac{R_D}{2}$$

and

$$V_1 = I_S \times R_D$$

$$\frac{V_2}{V_1} = \frac{1}{2}$$

$$V_1 = 2\,V_2$$

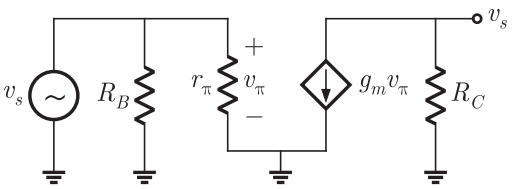
Hence (C) is correct option.

SOL 4.122

Hence (C) is correct option.

SOL 4.123

The equivalent circuit of given amplifier circuit (when C_E is connected, R_E is short-circuited)



Input impedance $R_i = R_B \,||\, r_\pi$
Voltage gain $A_V = g_m R_C$
Now, if C_E is disconnected, resistance R_E appears in the circuit

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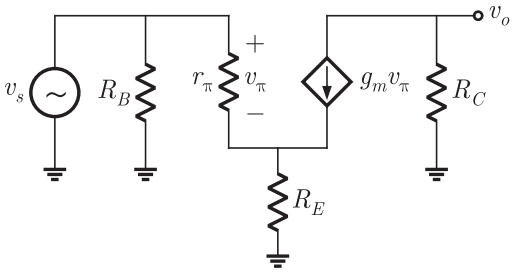


Input impedance $R_{\text{in}} = R_B \,||\, [r_\pi + (\beta + 1)] R_E$

Input impedance increases

Voltage gain $A_V = \dfrac{g_m R_C}{1 + g_m R_E}$ Voltage gain decreases.

Hence (C) is correct option.

SOL 4.124

In common emitter stage input impedance is high, so in cascaded amplifier common emitter stage is followed by common base stage.
Hence (A) is correct option.

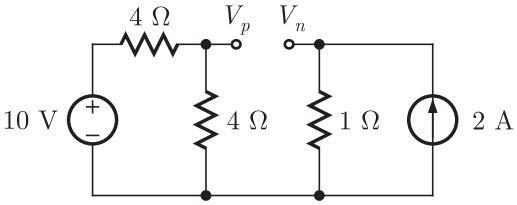
SOL 4.125

We know that collect-emitter break down voltage is less than compare to collector base breakdown voltage.

$$BV_{\text{CEO}} < BV_{\text{CBO}}$$

both avalanche and zener break down. Voltage are higher than BV_{CEO} .So BV_{CEO} limits the power supply.
Hence (C) is correct option.

SOL 4.126



If we assume consider the diode in reverse bias then V_n should be greater than V_P.

$$V_P < V_n$$

by calculating

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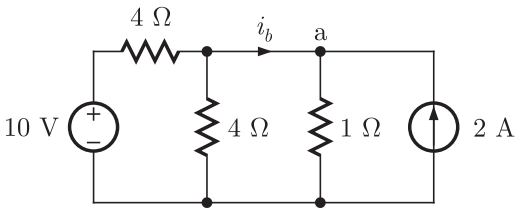
$$V_P = \frac{10}{4+4} \times 4 = 5 \text{ Volt}$$

$$V_n = 2 \times 1 = 2 \text{ Volt}$$

here $V_P > V_n$ (so diode cannot be in reverse bias mode).



apply node equation at node a

$$\frac{V_a - 10}{4} + \frac{V_a}{4} + \frac{V_a}{1} = 2$$

$$6V_a - 10 = 8$$

$$V_a = 3 \text{ Volt}$$

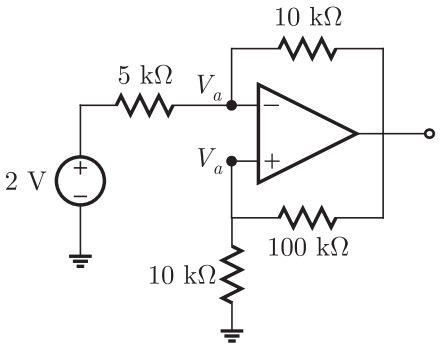
so current $$I_b = \frac{0-3}{4} + \frac{10-3}{4}$$

$$I_b = \frac{10-6}{4} = 1 \text{ amp}$$

Hence (C) is correct option.

SOL 4.127

By applying node equation at terminal (2) and (3) of *OP*-amp



$$\frac{V_a - Q}{5} + \frac{V_a - V_0}{10} = 0$$

$$2V_a - 4 + V_a - V_0 = 0$$

$$V_0 = 3V_a - 4$$

$$\frac{V_a - V_0}{100} + \frac{V_a - 0}{10} = 0$$

$$V_a - V_0 + 10V_a = 0$$

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$$11\,V_a = V_0$$

$$V_a = \frac{V_0}{11}$$

So
$$V_0 = \frac{3\,V_0}{11} - 4$$

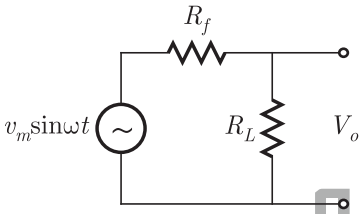
$$\frac{8\,V_0}{11} = -4$$

$$V_0 = -5.5\ \text{Volts}$$

Hence (D) is correct option.

SOL 4.128

Circuit with diode forward resistance looks



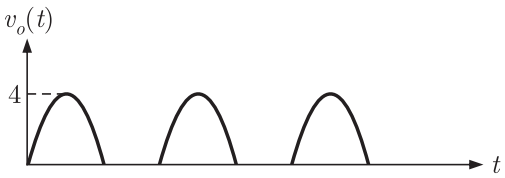
So the DC current will

$$I_{DC} = \frac{V_m}{\pi\,(R_f + R_L)}$$

Hence (B) is correct option.

SOL 4.129

For the positive half cycle of input diode D_1 will conduct & D_2 will be off. In negative half cycle of input D_1 will be off & D_2 conduct so output voltage wave from across resistor $(10\,\text{k}\Omega)$ is –



Ammeter will read rms value of current

so
$$I_{\text{rms}} = \frac{V_m}{\pi R}\,(\text{half wave rectifier})$$

$$= \frac{4}{(10\,\text{k}\Omega)\,\pi} = \frac{0.4}{\pi}\ \text{mA}$$

Hence (D) is correct option.

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SOL 4.130

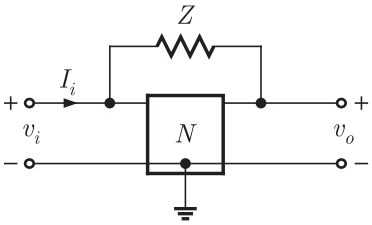
In given circuit positive feedback is applied in the op-amp., so it works as a Schmitt trigger.
Hence (D) is correct option.

SOL 4.131

Gain with out feedback factor is given by

$$V_0 = kV_i$$

after connecting feedback impedance Z



given input impedance is very large, so after connecting Z we have

$$I_i = \frac{V_i - V_0}{Z} \qquad V_0 = kV_i$$

$$I_i = \frac{V_i - kV_i}{Z}$$

input impedance $Z_{in} = \dfrac{V_i}{I_i} = \dfrac{Z}{(1-k)}$

Hence (D) is correct option

SOL 4.132

Hence (A) is correct option.

SOL 4.133

For the circuit, In balanced condition It will oscillated at a frequency

$$\omega = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{10 \times 10^{-3} \times .01 \times 10^{-6}}} = 10^5 \text{rad/sec}$$

In this condition

$$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$

$$\frac{5}{100} = \frac{R}{1}$$

$$R = 20\,\text{k}\Omega = 2 \times 10^4\,\Omega$$

Hence (A) is correct option.

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SOL 4.134

V_0 kept constant at $V_0 = 6$ volt

so current in $50\,\Omega$ resistor $I = \dfrac{9-6}{50\,\Omega}$

$$I = 60 \text{ m amp}$$

Maximum allowed power dissipation in zener

$$P_Z = 300\,\text{mW}$$

Maximum current allowed in zener

$$P_Z = V_Z (I_Z)_{\max} = 300 \times 10^{-3}$$

$$\Rightarrow \quad = 6\,(I_Z)_{\max} = 300 \times 10^{-3}$$

$$\Rightarrow \quad = (I_Z)_{\max} = 50 \text{ m amp}$$

Given knee current or minimum current in zener

$$(I_Z)_{\min} = 5 \text{ m amp}$$

In given circuit $I = I_Z + I_L$

$$I_L = I - I_Z$$

$$(I_L)_{\min} = I - (I_Z)_{\max}$$

$$= (60 - 50) \text{ m amp} = 10 \text{ m amp}$$

$$(I_L)_{\max} = I - (I_Z)_{\min}$$

$$= (60 - 5) = 55 \text{ m amp}$$

Hence (C) is correct option.

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