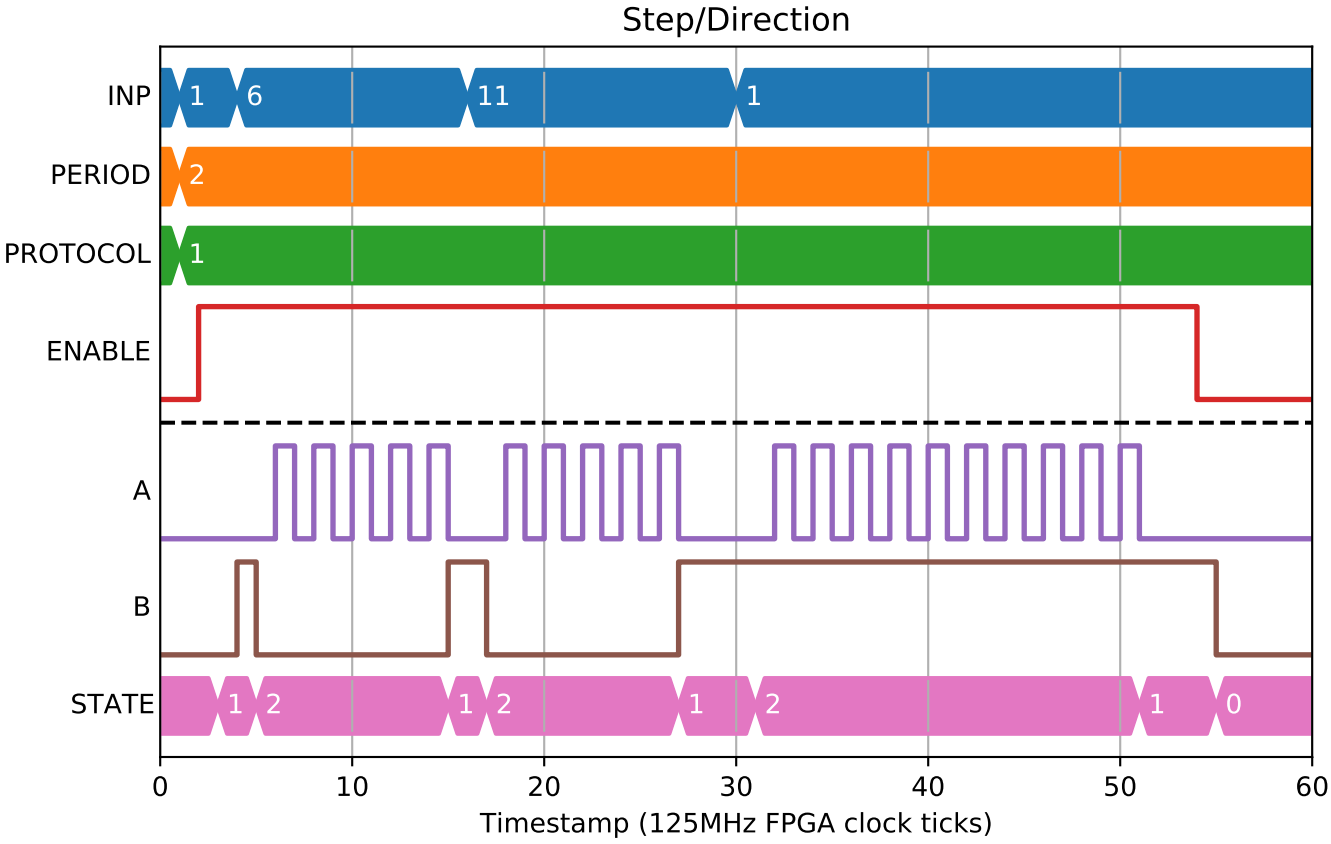
Step/Direction
INP
PERIOD
PROTOCOL
ENABLE
A
B
STATE
1
6
11
1
2
1
1
2
1
2
1
2
1
0
0
10
20
30
40
50
60
Timestamp (125MHz FPGA clock ticks)