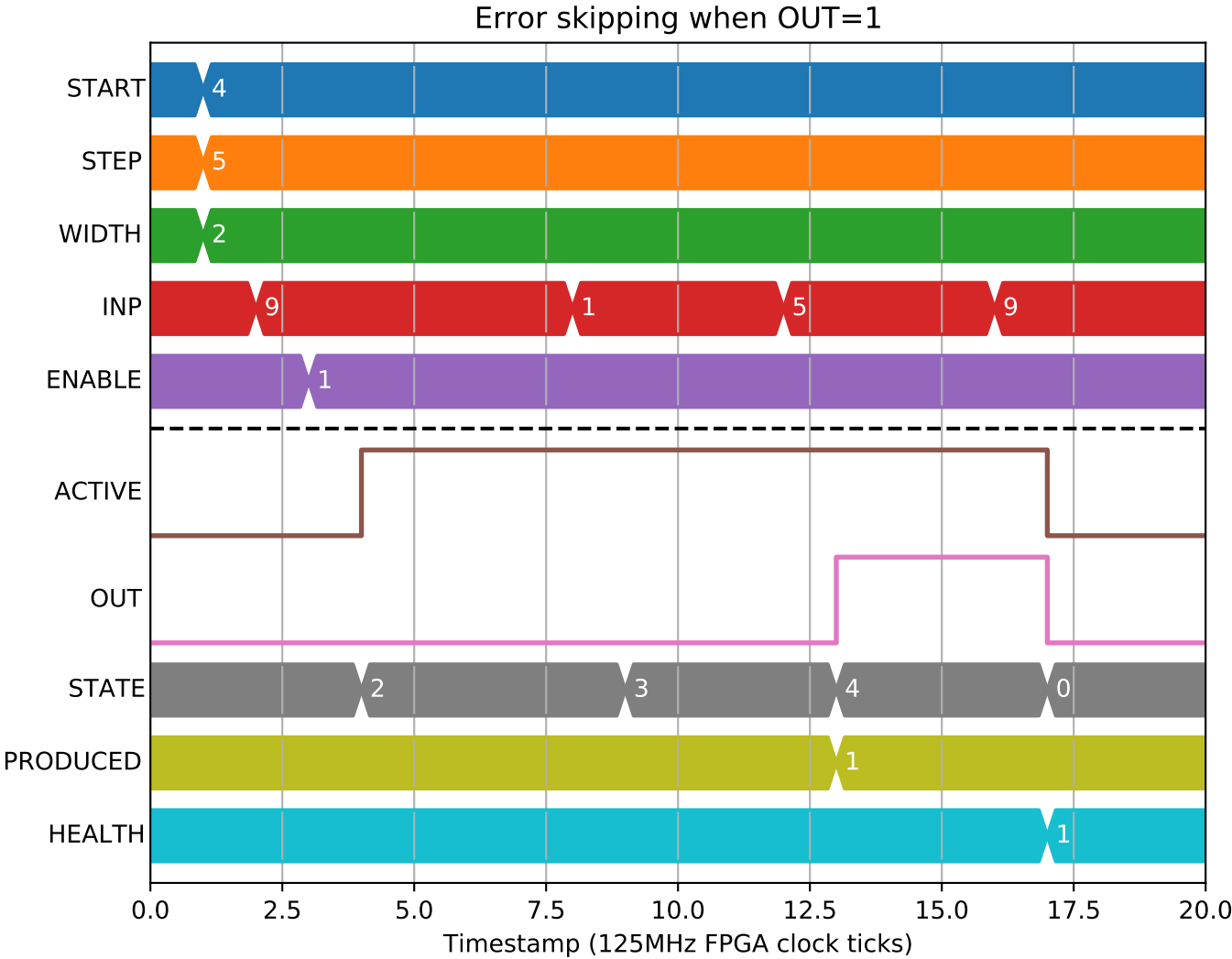
Error skipping when OUT=1
START
STEP
WIDTH
INP
ENABLE
ACTIVE
OUT
STATE
PRODUCED
HEALTH
4
5
2
9
1
5
9
1
2
3
4
0
1
1
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
Timestamp (125MHz FPGA clock ticks)