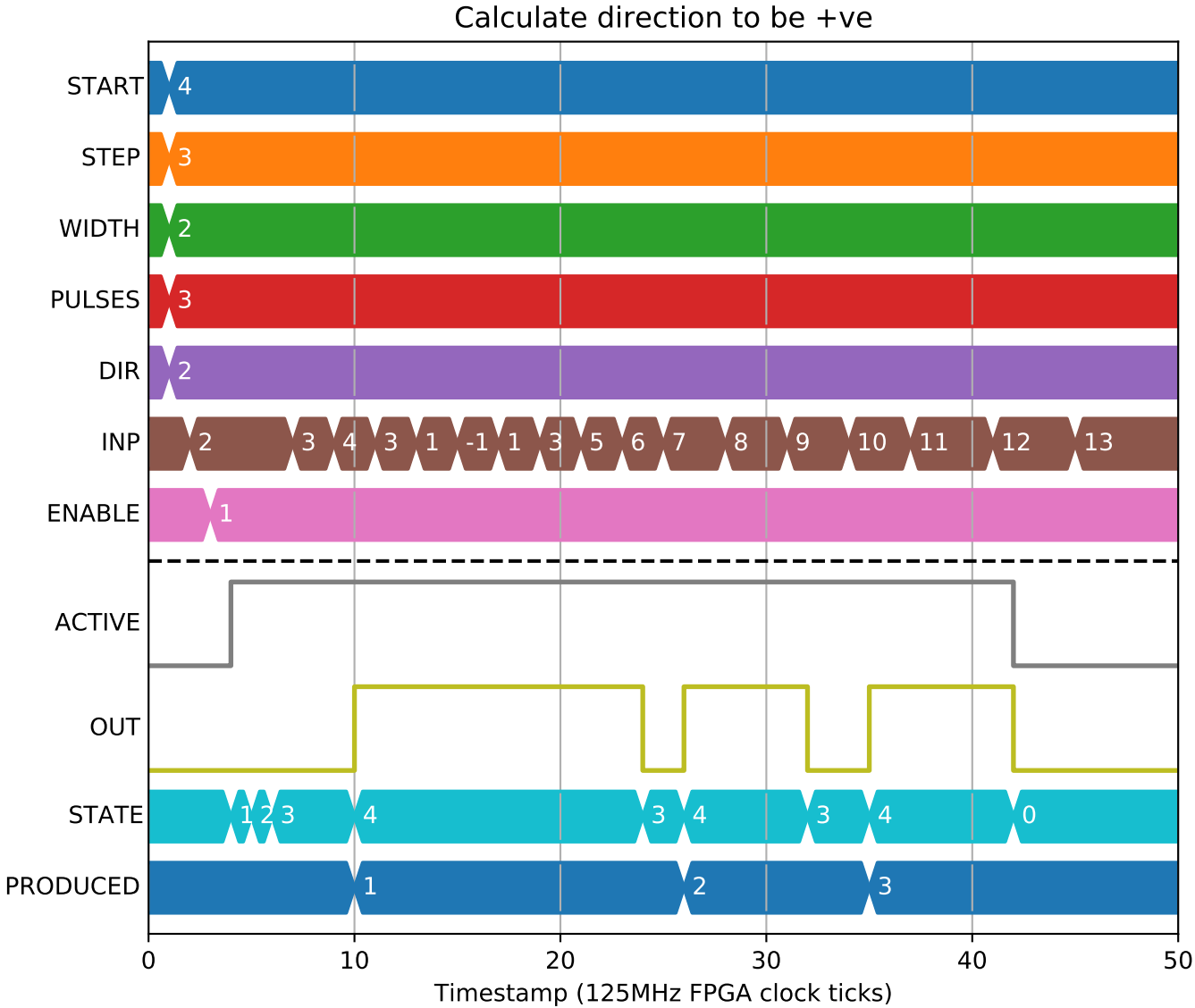
Calculate direction to be +ve
START
STEP
WIDTH
PULSES
DIR
INP
ENABLE
ACTIVE
OUT
STATE
PRODUCED
4
3
2
3
2
2 3 4 3 1 -1 1 3 5 6 7 8 9 10 11 12 13
1
1 2 3 4 3 4 3 4 0
1 2 3
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)