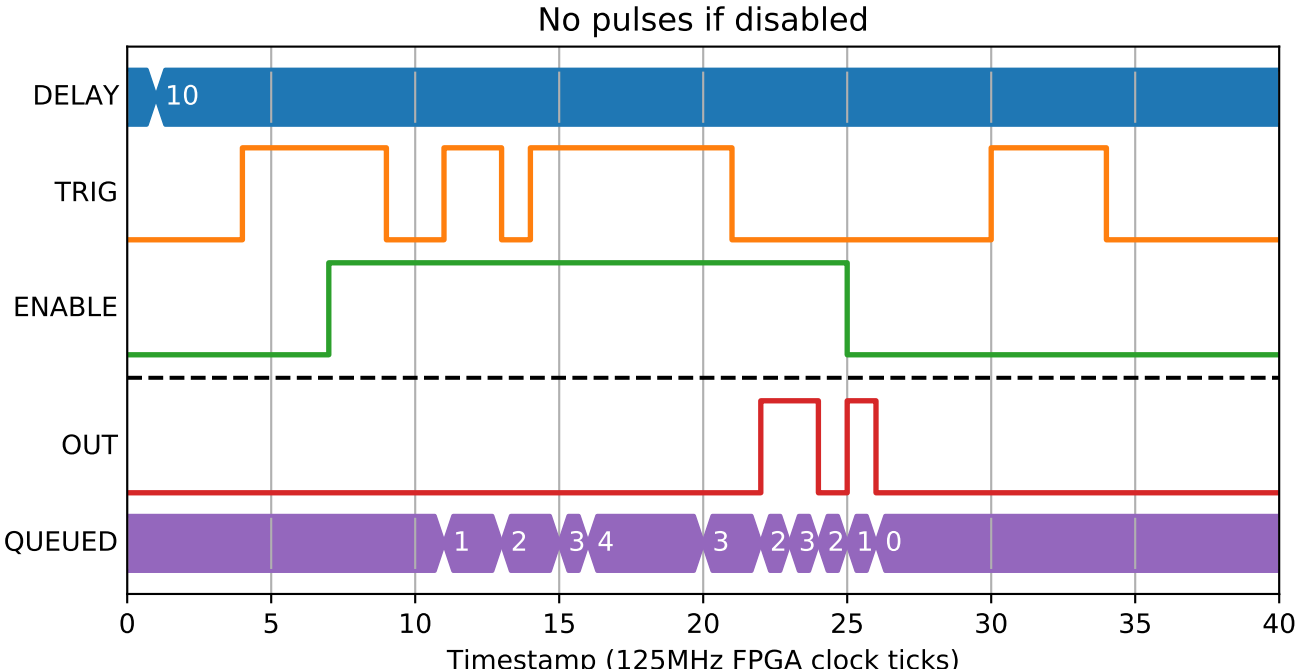
No pulses if disabled
DELAY
10
TRIG
ENABLE
OUT
QUEUED
1
2
3
4
3
2
3
2
1
0
0
5
10
15
20
25
30
35
40
Timestamp (125MHz FPGA clock ticks)