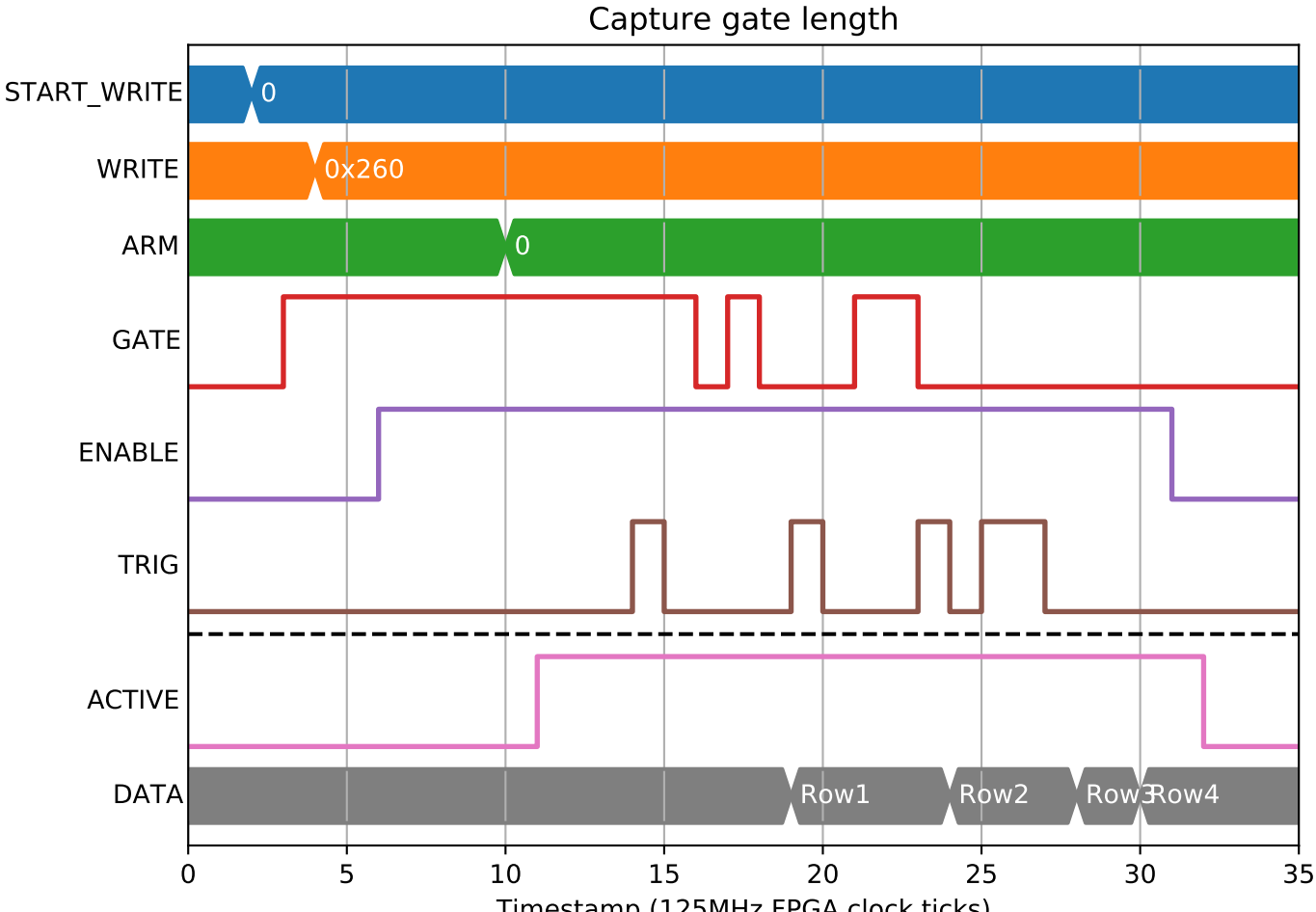
Capture gate length
START_WRITE
0
WRITE
0x260
ARM
0
GATE
ENABLE
TRIG
ACTIVE
DATA
Row1
Row2
Row3
Row4
0
5
10
15
20
25
30
35
Timestamp (125MHz FPGA clock ticks)