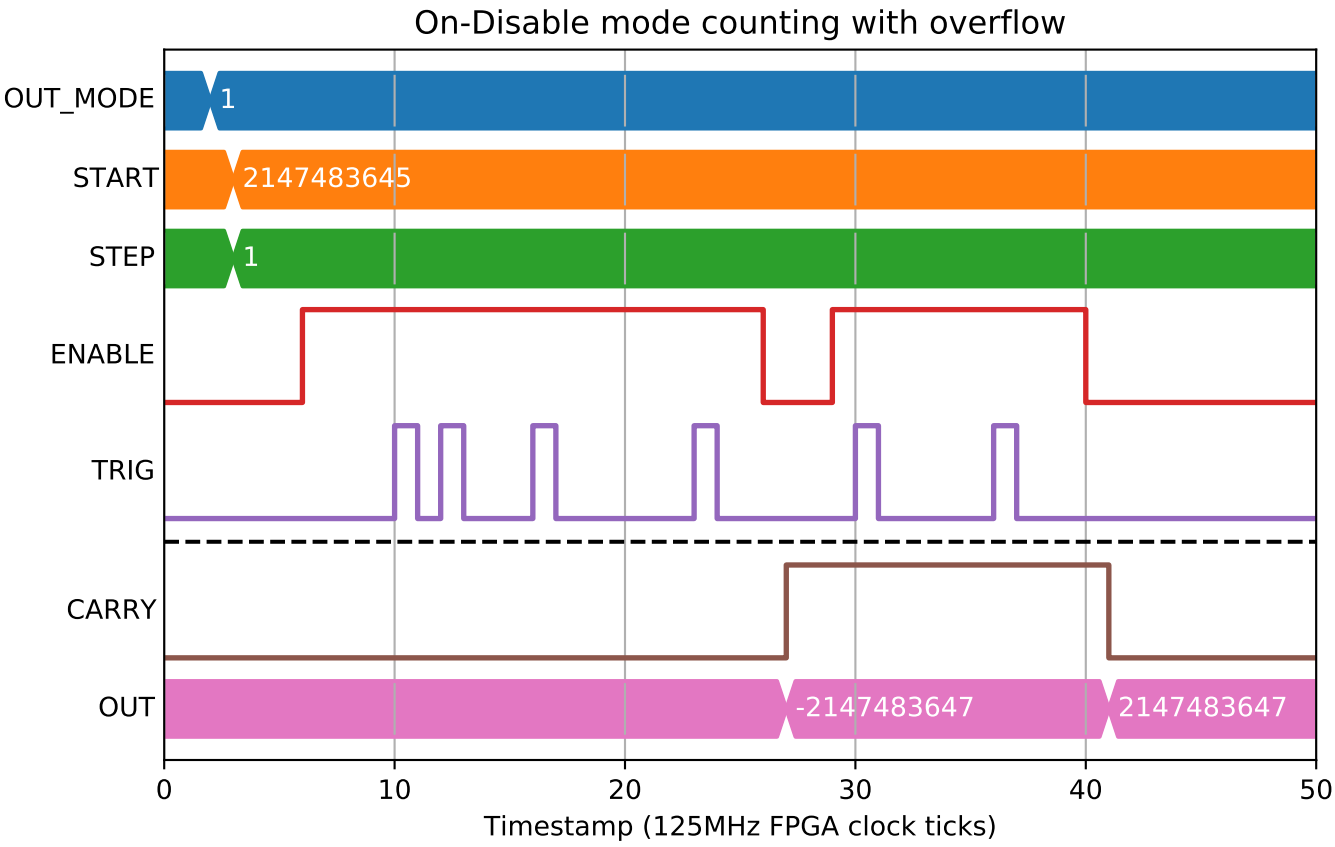
On-Disable mode counting with overflow
OUT_MODE
START
STEP
ENABLE
TRIG
CARRY
OUT
1
2147483645
1
-2147483647
2147483647
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)