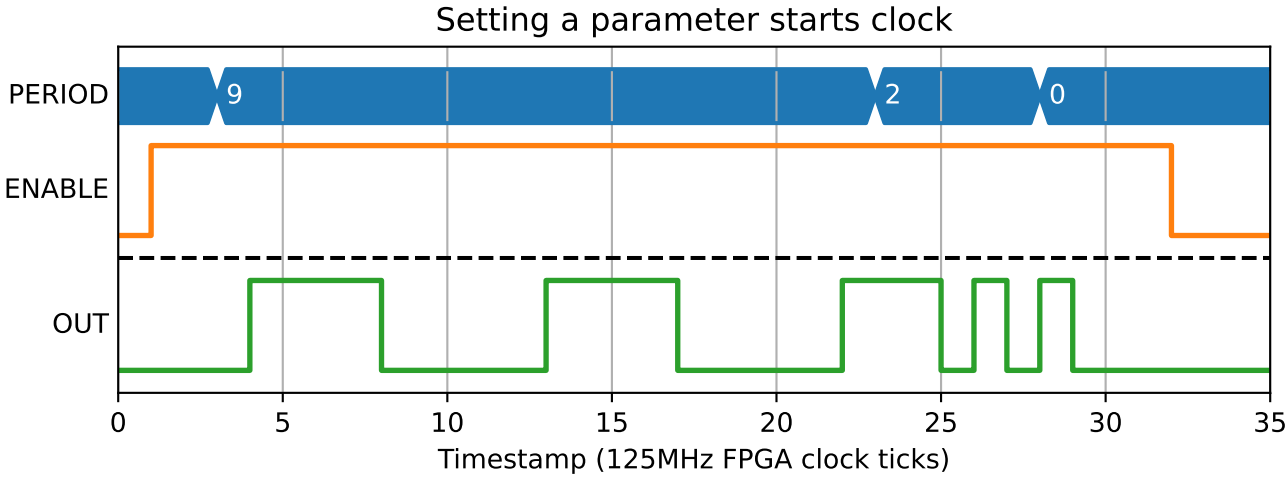
Setting a parameter starts clock
PERIOD
ENABLE
OUT
9
2
0
0
5
10
15
20
25
30
35
Timestamp (125MHz FPGA clock ticks)