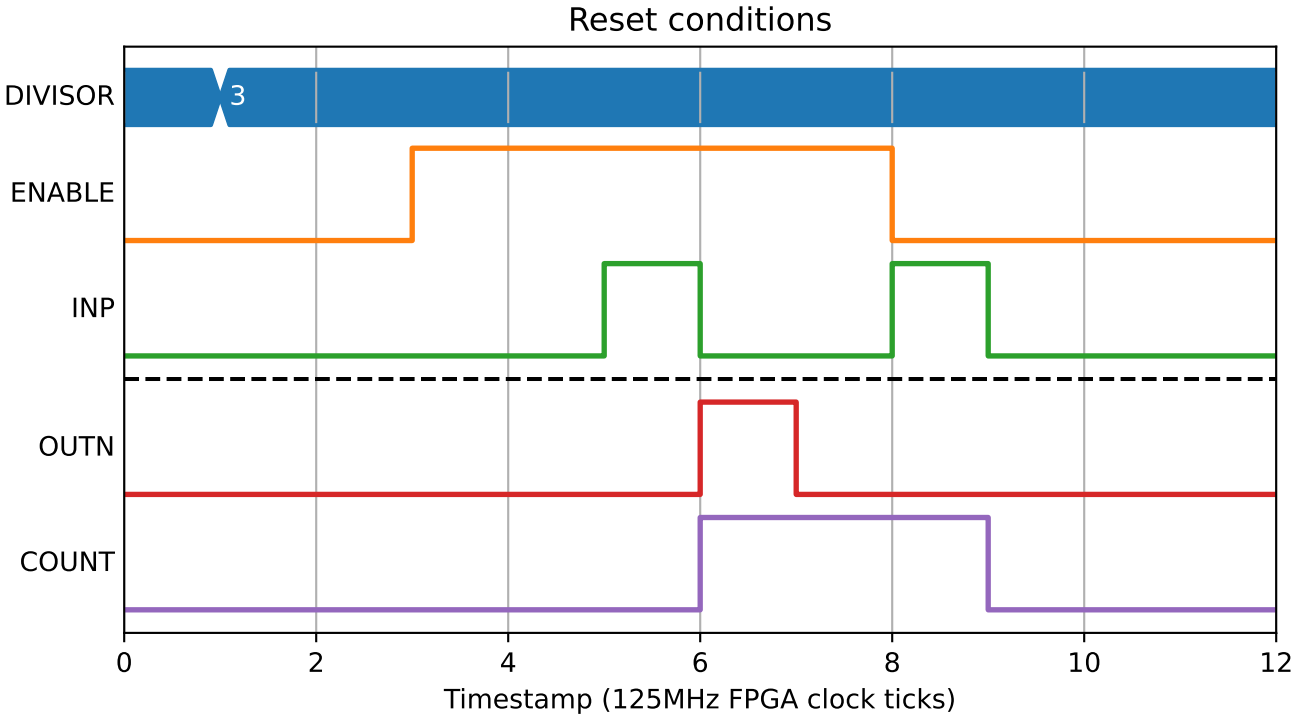
Reset conditions
DIVISOR
3
ENABLE
INP
OUTN
COUNT
0
2
4
6
8
10
12
Timestamp (125MHz FPGA clock ticks)