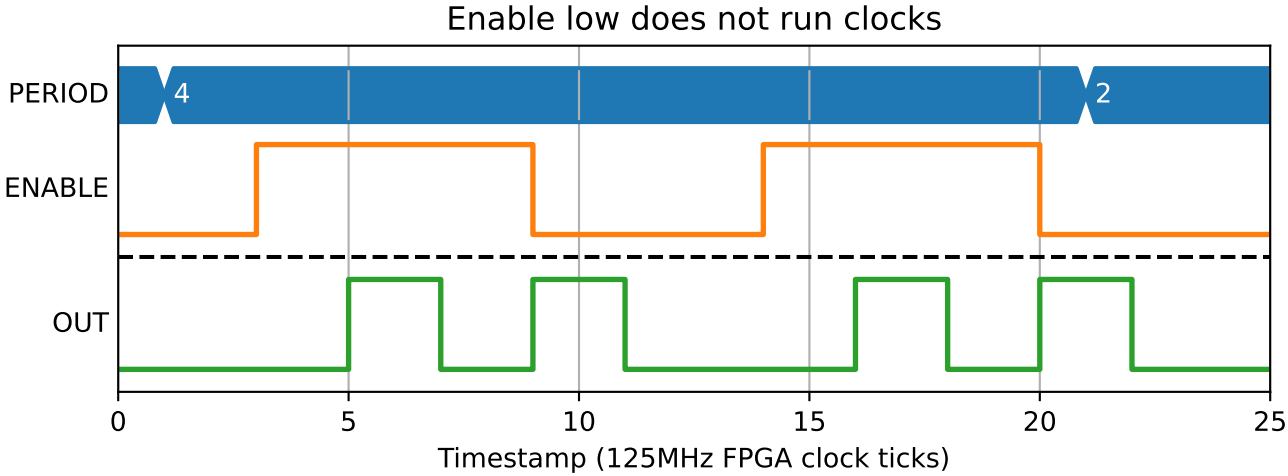
Enable low does not run clocks
PERIOD
4
2
ENABLE
OUT
0
5
10
15
20
25
Timestamp (125MHz FPGA clock ticks)