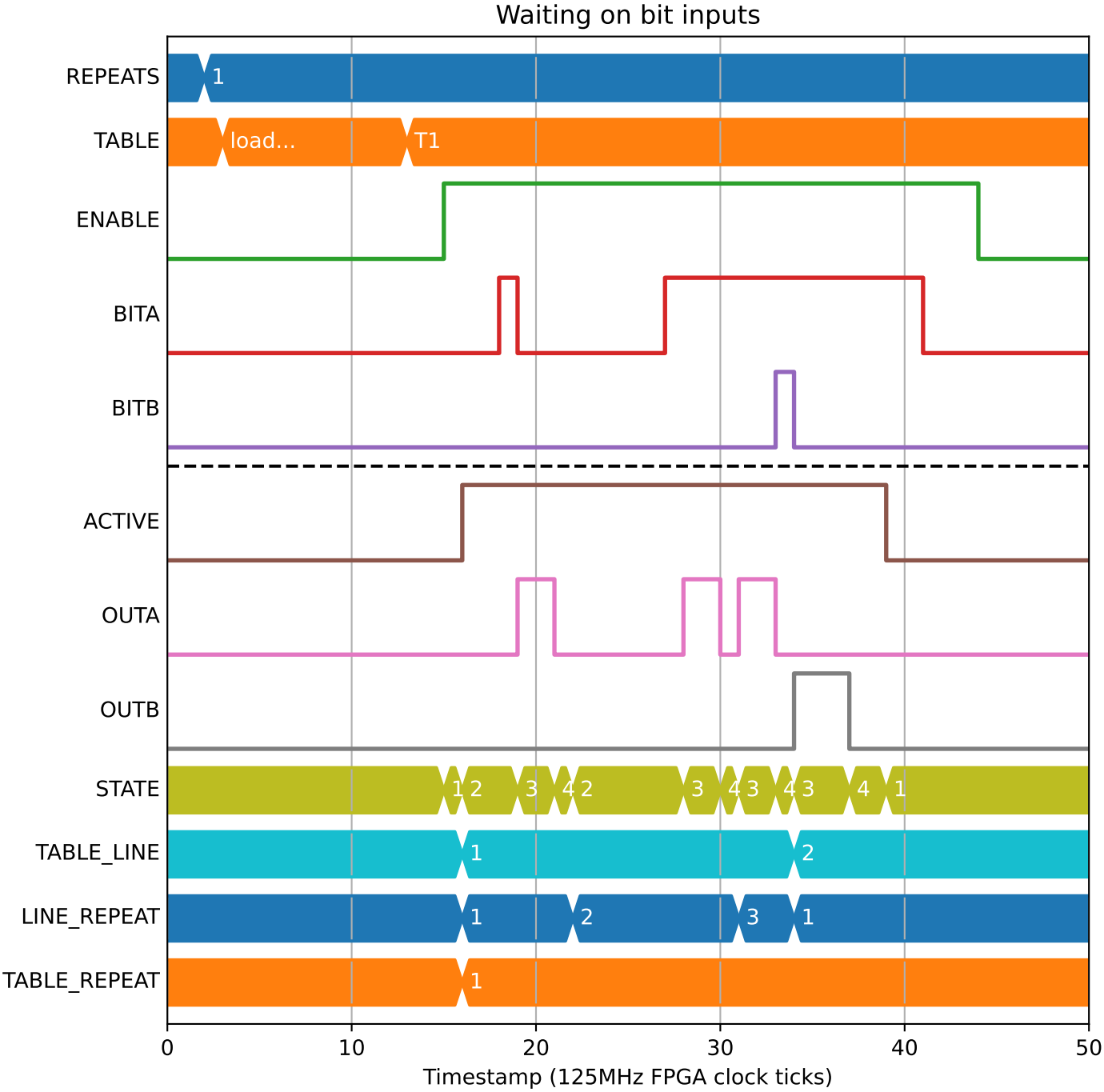
Waiting on bit inputs
REPEATS
TABLE
ENABLE
BITA
BITB
ACTIVE
OUTA
OUTB
STATE
TABLE_LINE
LINE_REPEAT
TABLE_REPEAT
1
load...
T1
1 2 3 4 2 3 4 3 4 3 4 1
1 2
1 2 3 1
1
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)