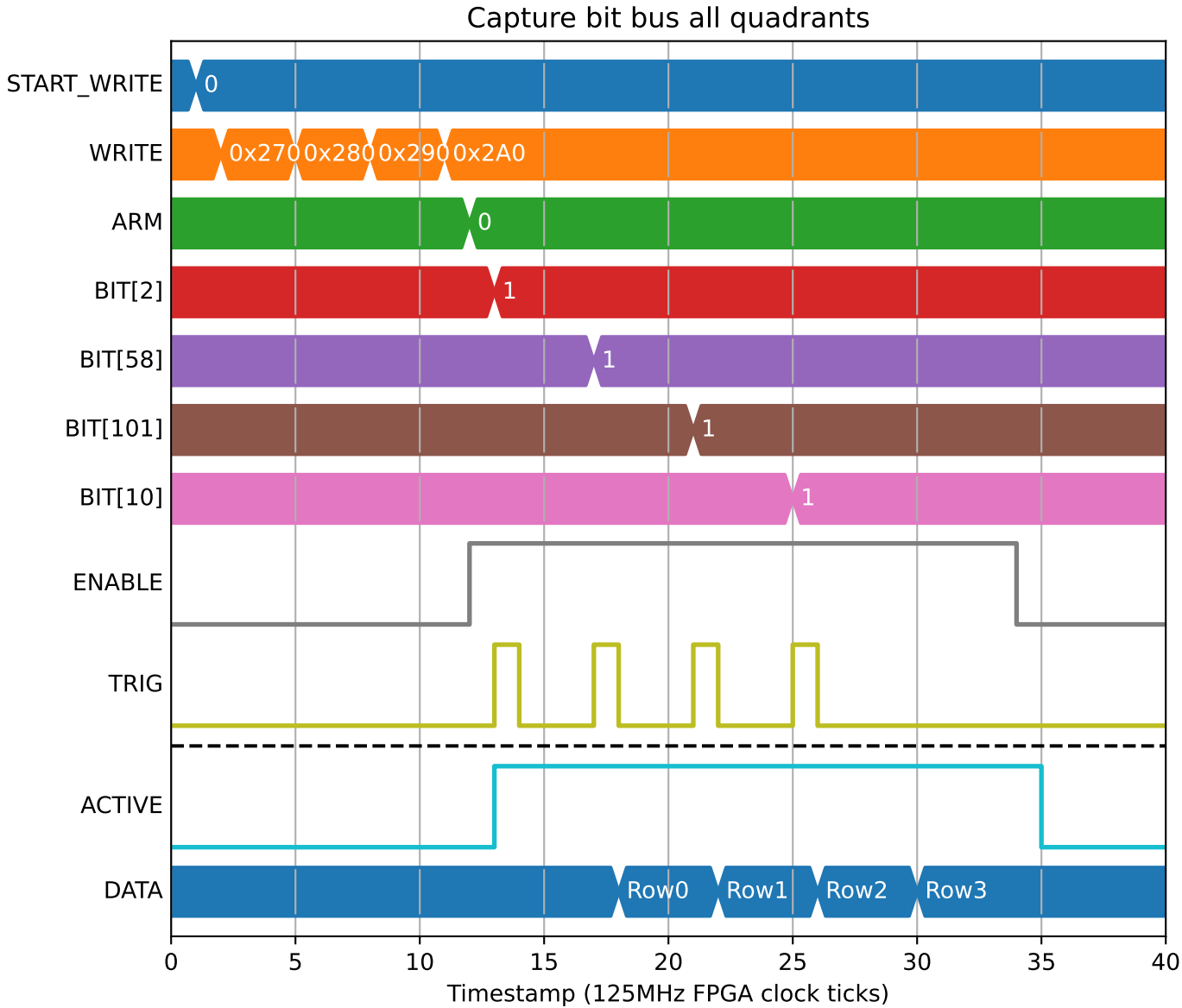
Capture bit bus all quadrants
START_WRITE
0
WRITE
0x270
0x280
0x290
0x2A0
ARM
0
BIT[2]
1
BIT[58]
1
BIT[101]
1
BIT[10]
1
ENABLE
TRIG
ACTIVE
DATA
Row0
Row1
Row2
Row3
0
5
10
15
20
25
30
35
40
Timestamp (125MHz FPGA clock ticks)