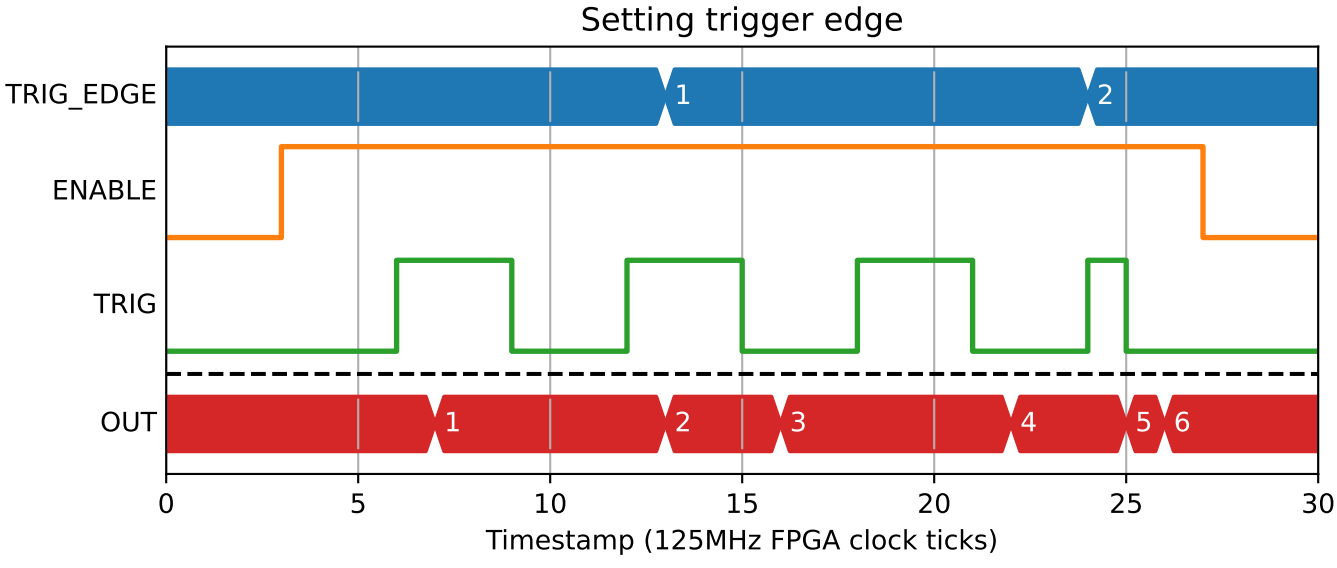
Setting trigger edge
TRIG_EDGE
ENABLE
TRIG
OUT
1
2
1
2
3
4
5
6
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)