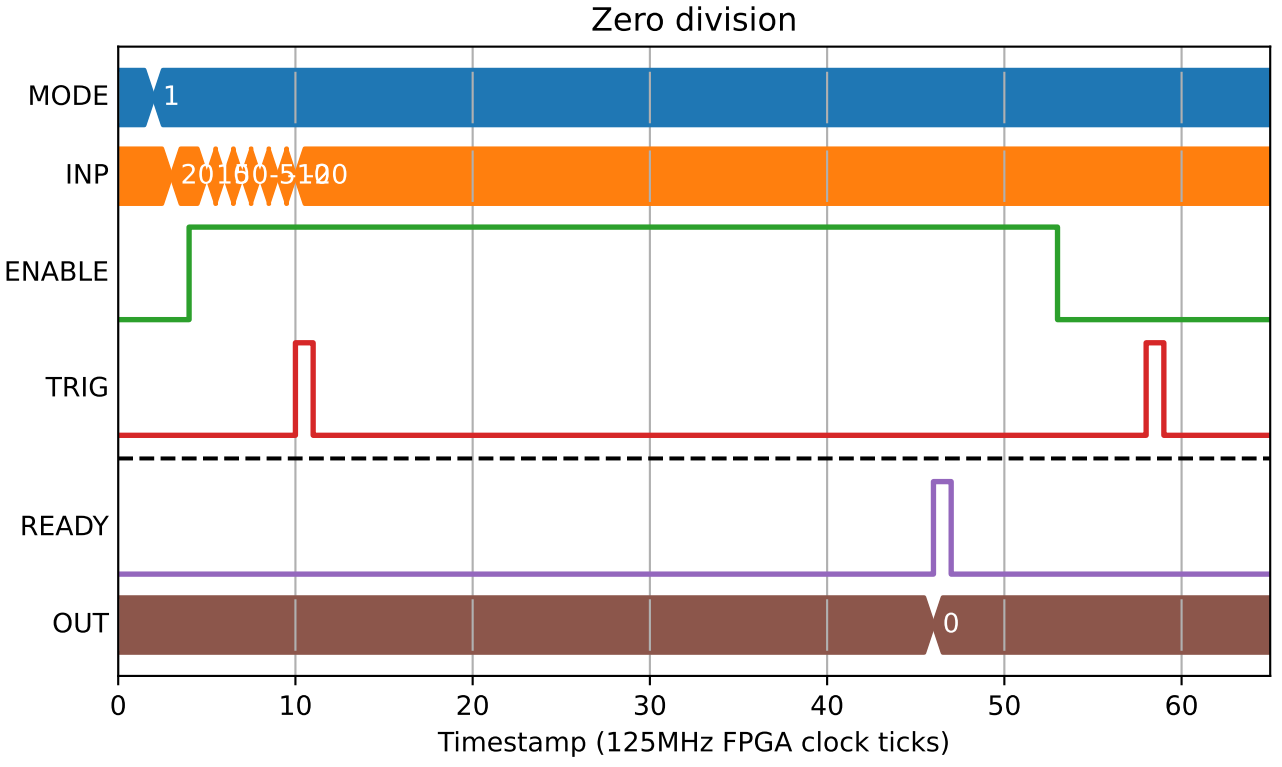
Zero division
MODE
INP
ENABLE
TRIG
READY
OUT
1
20100-5100
0
0
10
20
30
40
50
60
Timestamp (125MHz FPGA clock ticks)