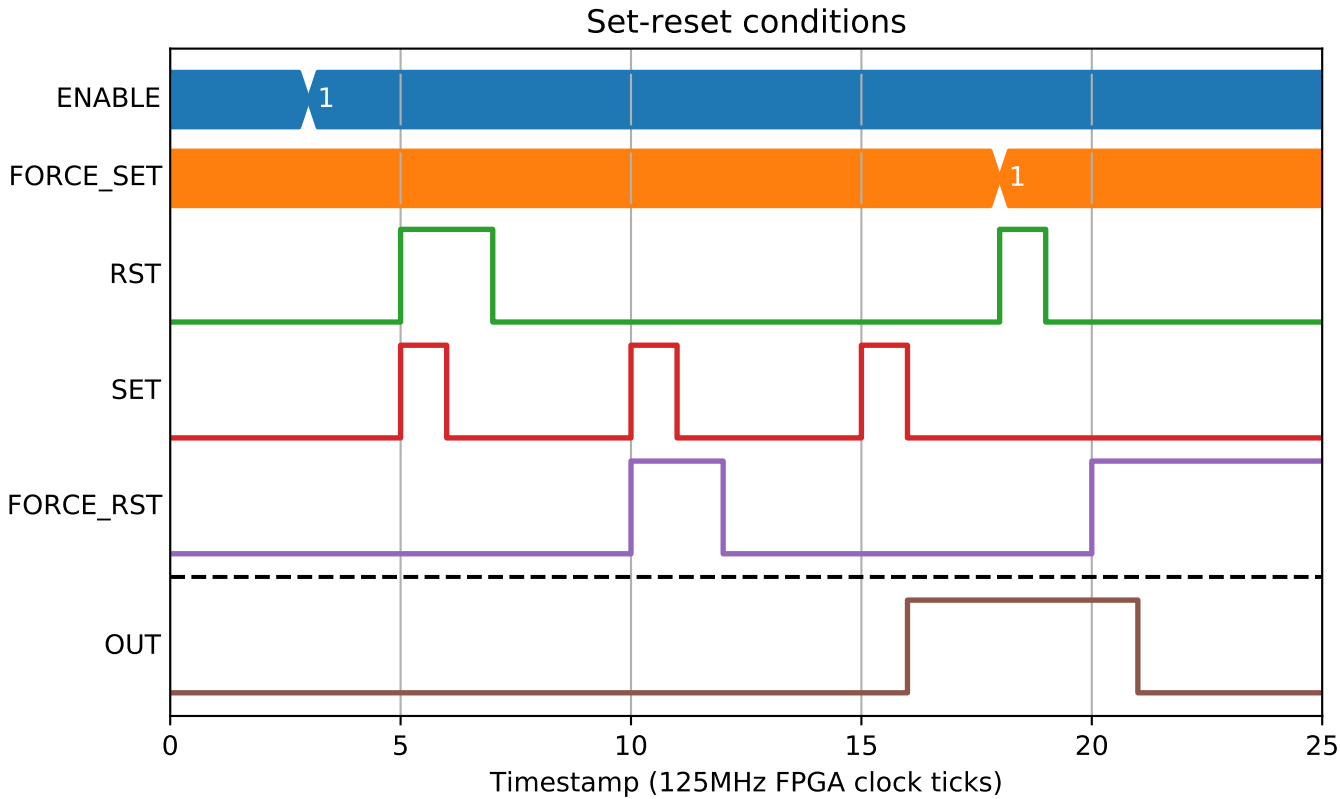
Set-reset conditions
ENABLE
1
FORCE_SET
1
RST
SET
FORCE_RST
OUT
0
5
10
15
20
25
Timestamp (125MHz FPGA clock ticks)