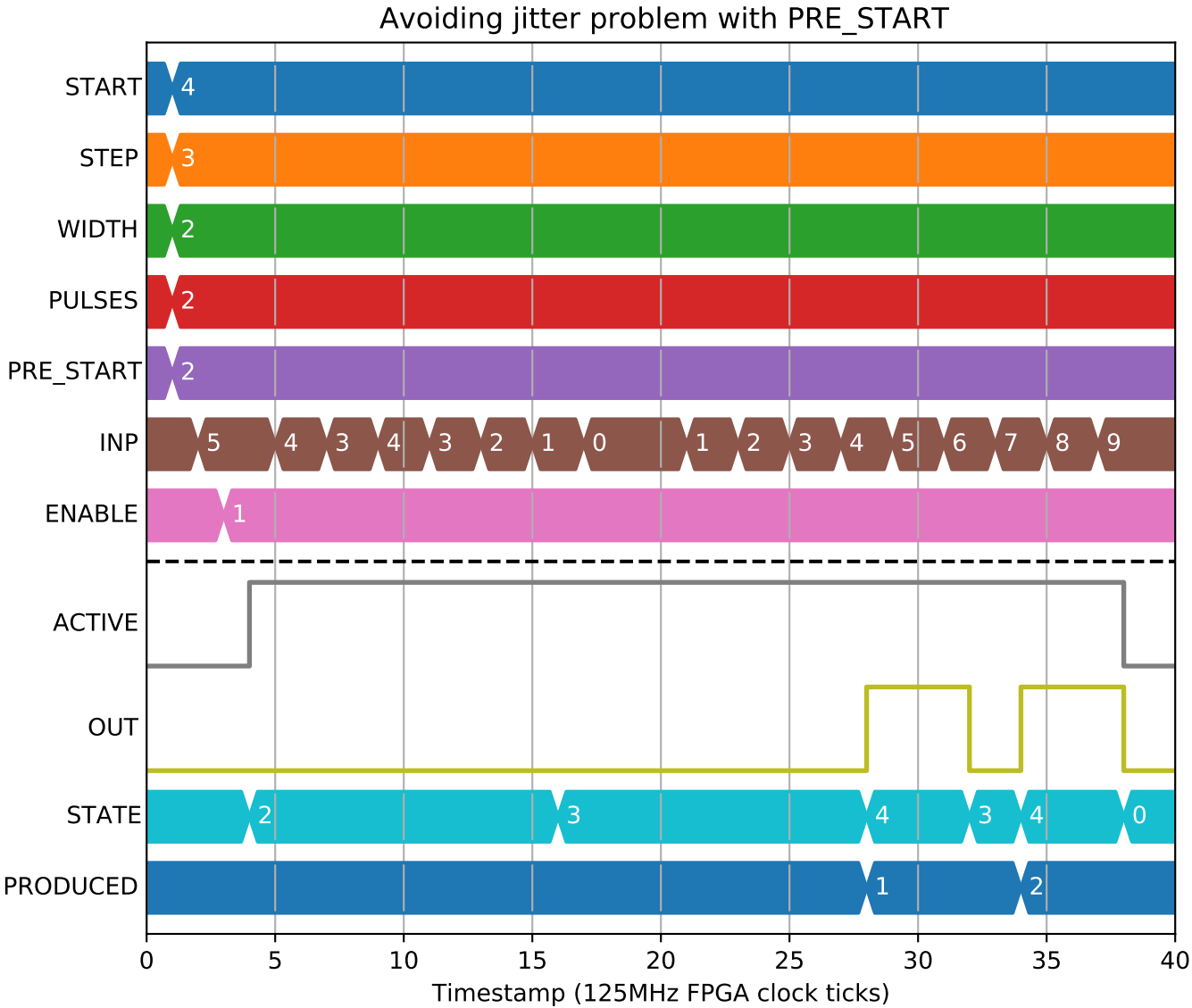
Avoiding jitter problem with PRE_START
START
STEP
WIDTH
PULSES
PRE_START
INP
ENABLE
ACTIVE
OUT
STATE
PRODUCED
4
3
2
2
2
5 4 3 4 3 2 1 0 1 2 3 4 5 6 7 8 9
1
2 3 4 3 4 0
1 2
0 5 10 15 20 25 30 35 40
Timestamp (125MHz FPGA clock ticks)