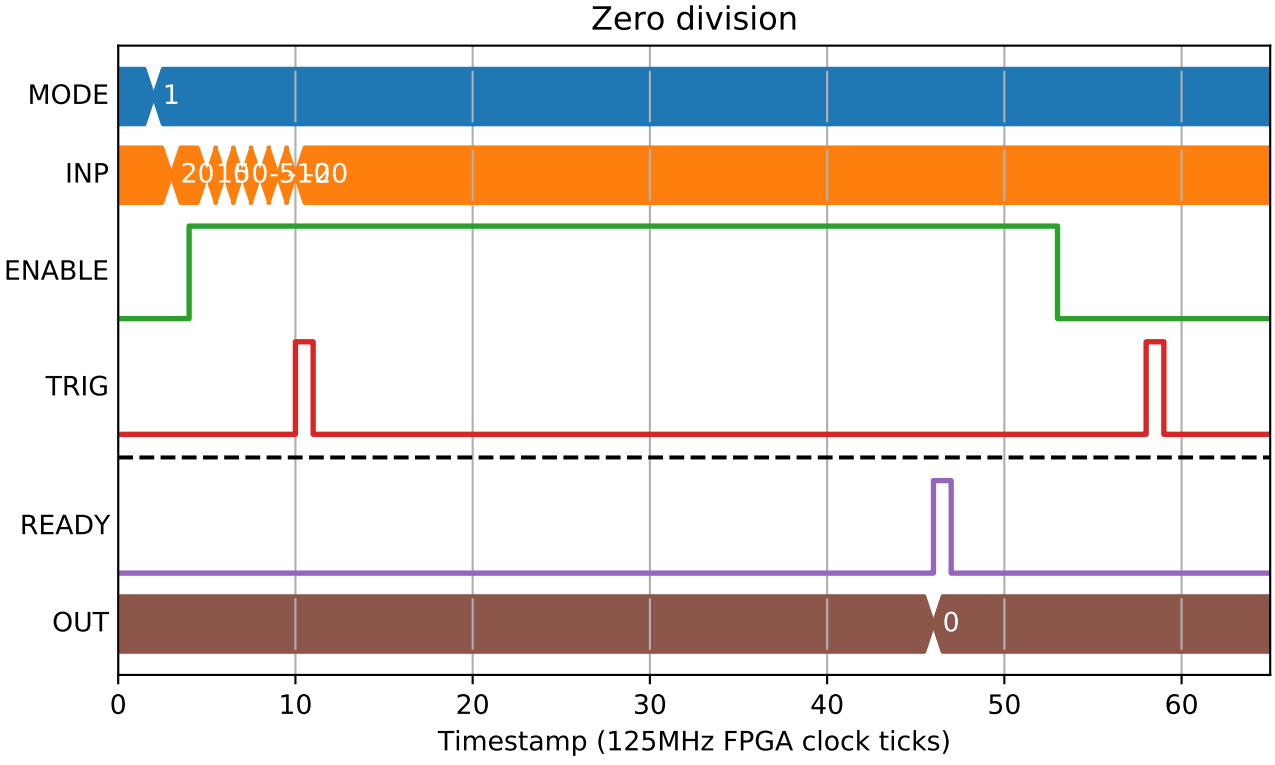
Zero division
MODE
1
INP
20160-5100
ENABLE
TRIG
READY
OUT
0
0
10
20
30
40
50
60
Timestamp (125MHz FPGA clock ticks)