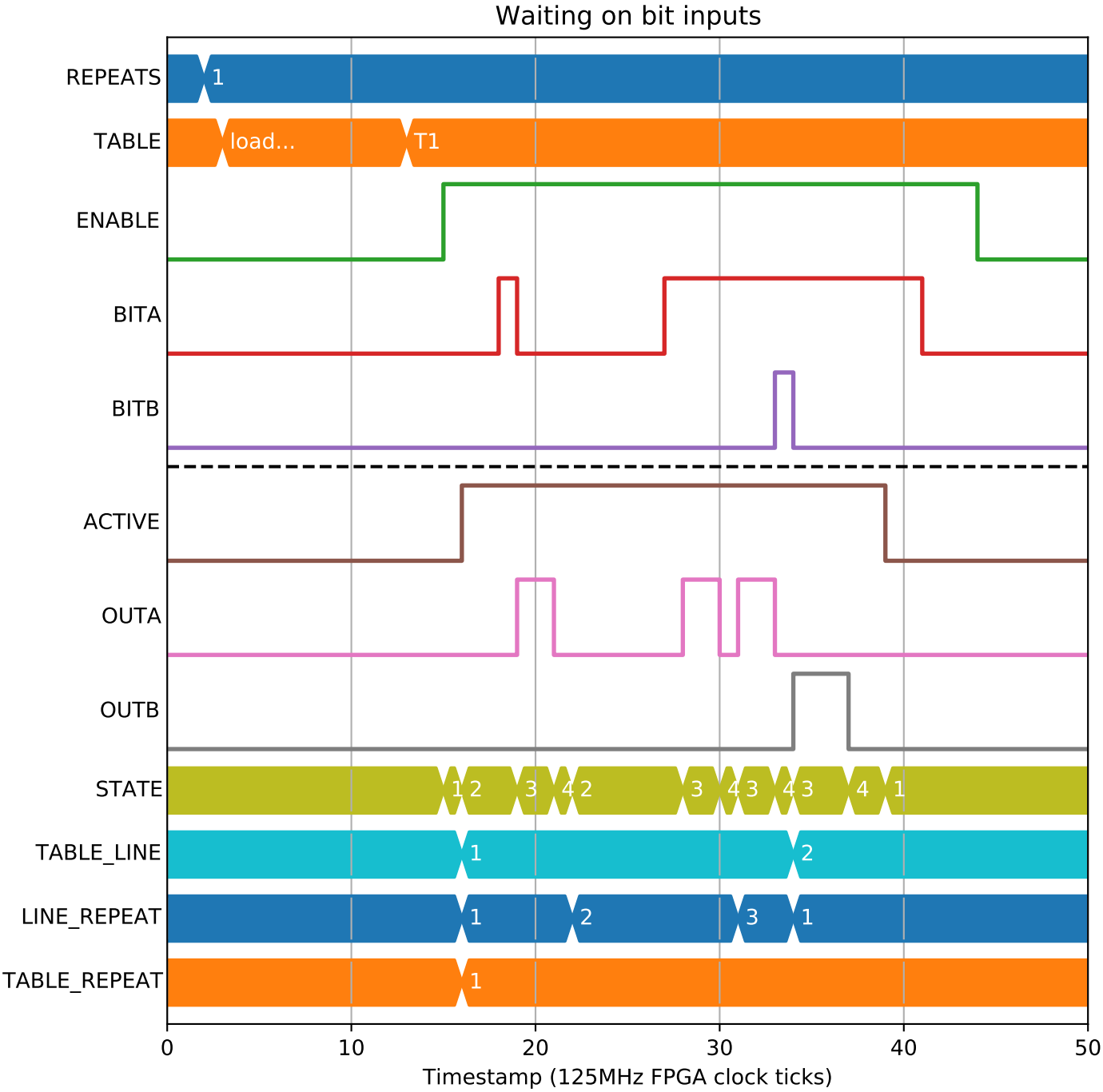
Waiting on bit inputs
REPEATS
1
TABLE
load...
T1
ENABLE
BITA
BITB
ACTIVE
OUTA
OUTB
STATE
1 2 3 4 2 3 4 3 4 3 4 1
TABLE_LINE
1
2
LINE_REPEAT
1
2
3
1
TABLE_REPEAT
1
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)