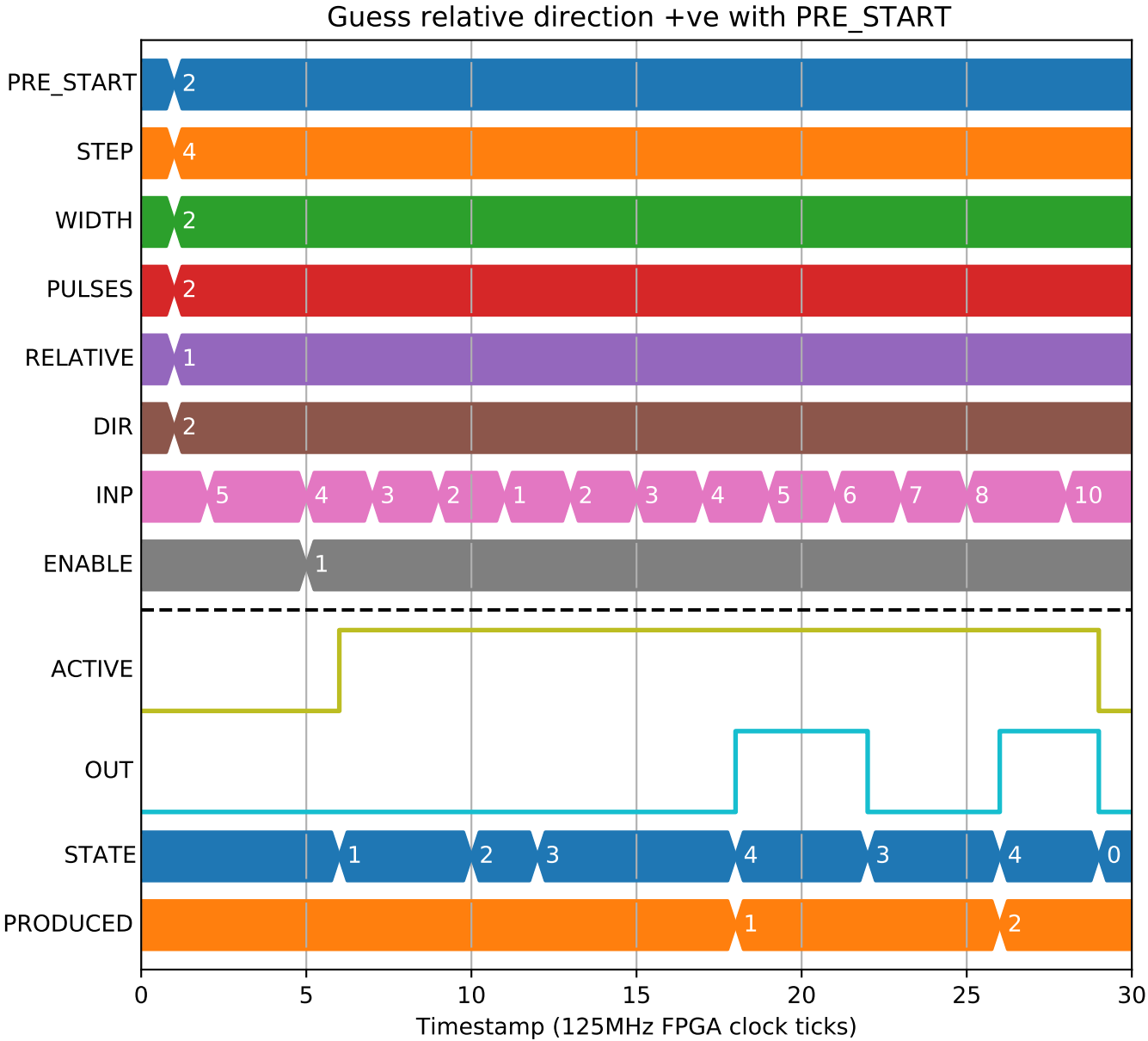
Guess relative direction +ve with PRE_START
PRE_START
STEP
WIDTH
PULSES
RELATIVE
DIR
INP
ENABLE
ACTIVE
OUT
STATE
PRODUCED
2
4
2
2
1
2
5 4 3 2 1 2 3 4 5 6 7 8 10
1
1 2 3 4 3 4 0
1 2
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)