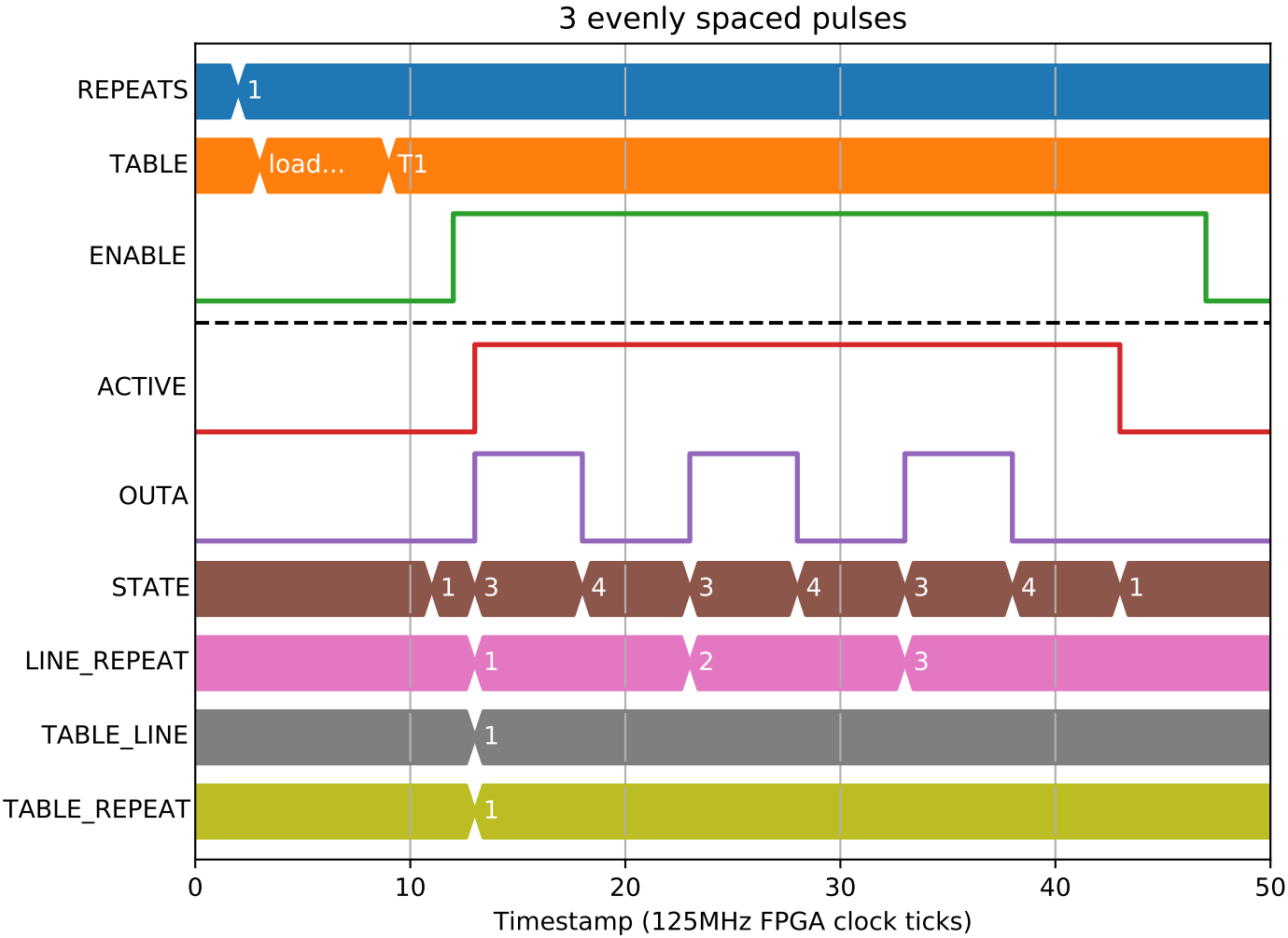
3 evenly spaced pulses
REPEATS
TABLE
ENABLE
ACTIVE
OUTA
STATE
LINE_REPEAT
TABLE_LINE
TABLE_REPEAT
1
load...
T1
1
3
4
3
4
3
4
1
1
2
3
1
1
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)