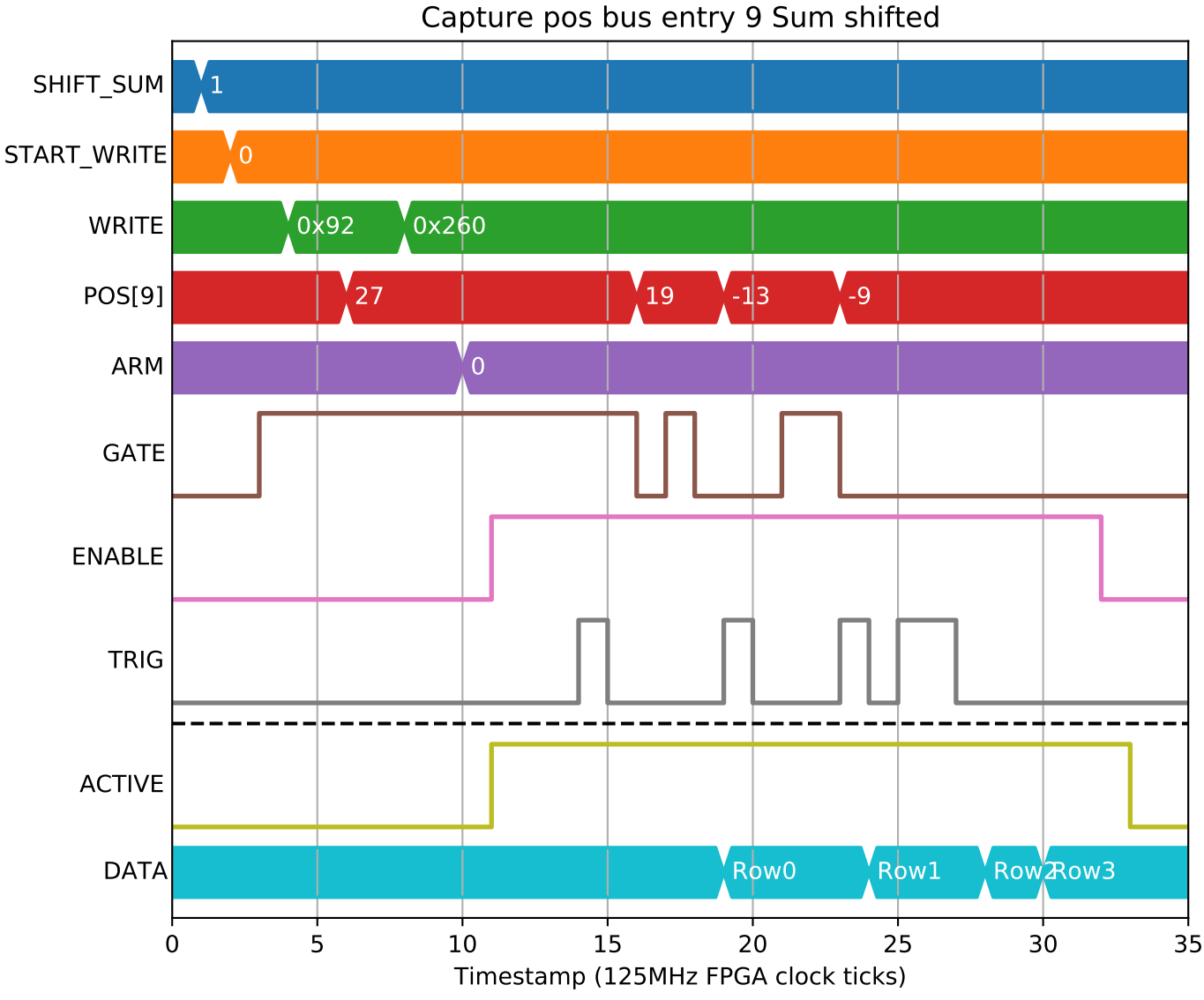
Capture pos bus entry 9 Sum shifted
SHIFT_SUM
1
START_WRITE
0
WRITE
0x92
0x260
POS[9]
27
19
-13
-9
ARM
0
GATE
ENABLE
TRIG
ACTIVE
DATA
Row0
Row1
Row2
Row3
0
5
10
15
20
25
30
35
Timestamp (125MHz FPGA clock ticks)