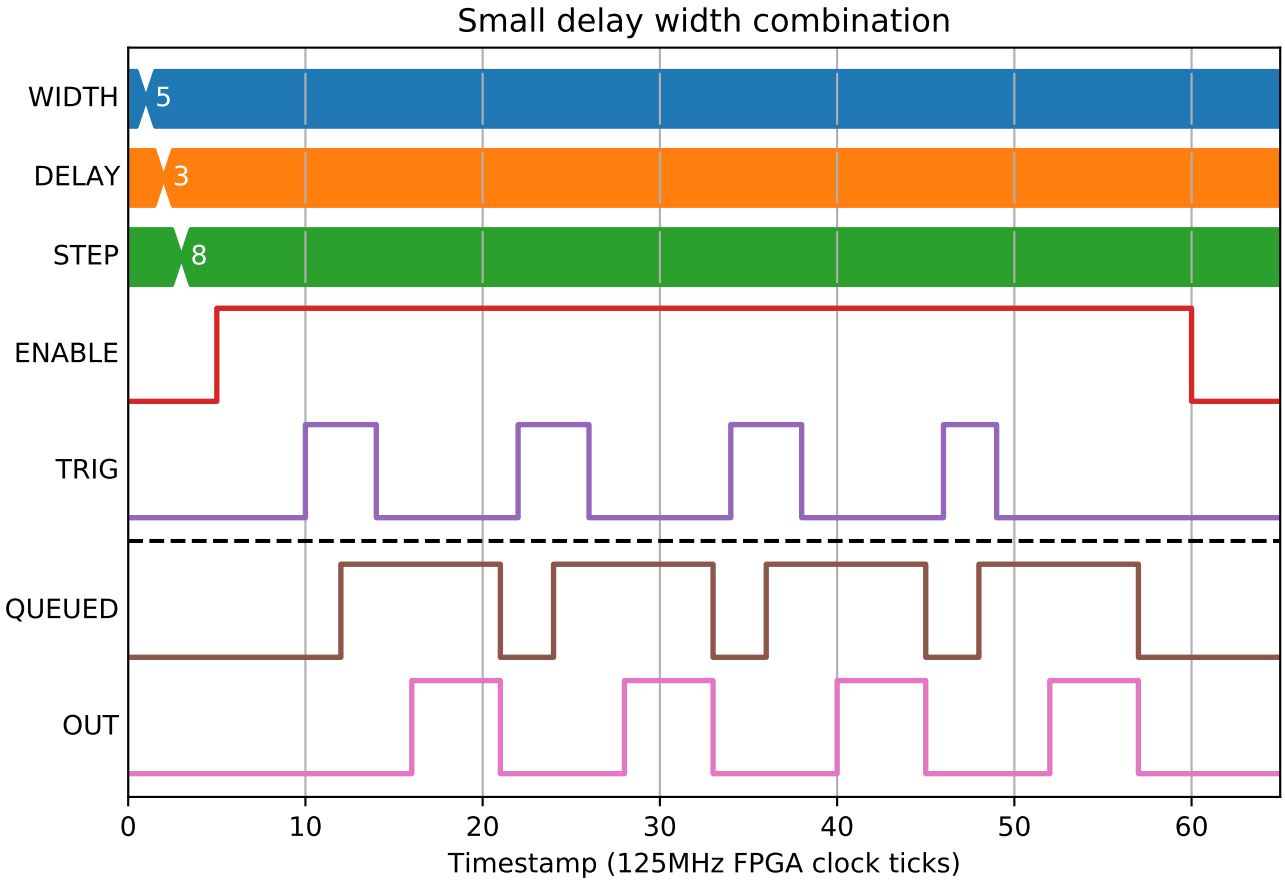
Small delay width combination
WIDTH
5
DELAY
3
STEP
8
ENABLE
TRIG
QUEUED
OUT
0
10
20
30
40
50
60
Timestamp (125MHz FPGA clock ticks)