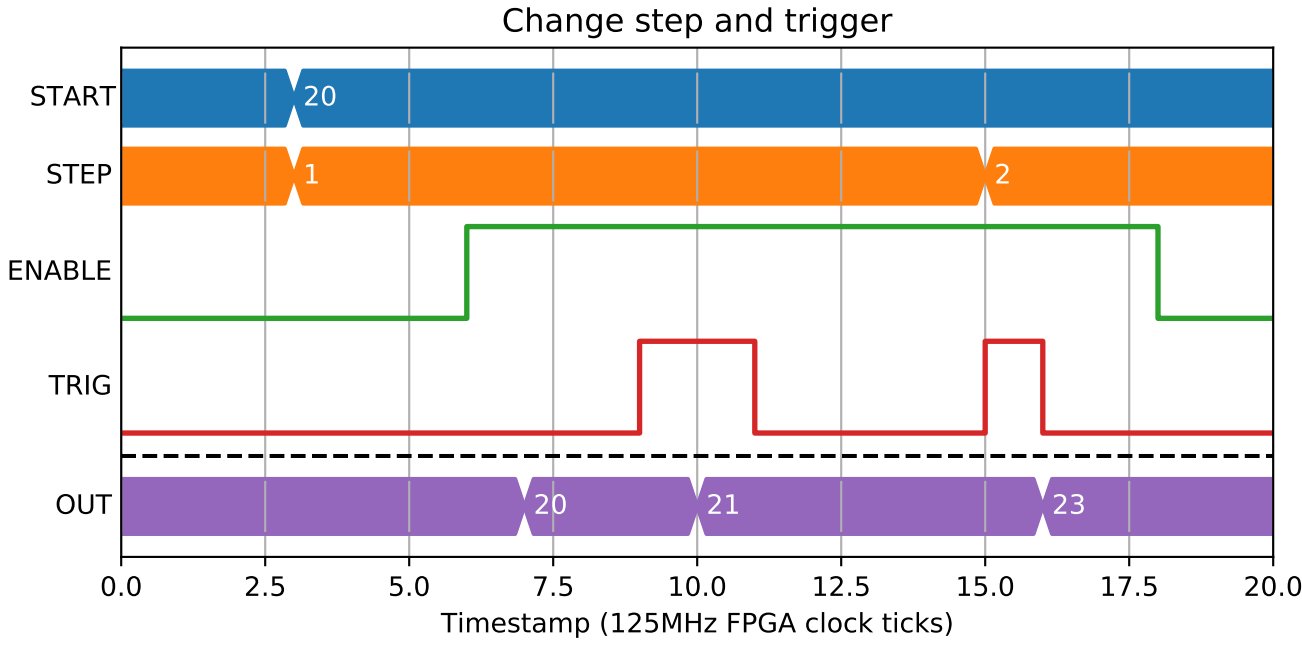
Change step and trigger
START
STEP
ENABLE
TRIG
OUT
20
1
2
20
21
23
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
Timestamp (125MHz FPGA clock ticks)