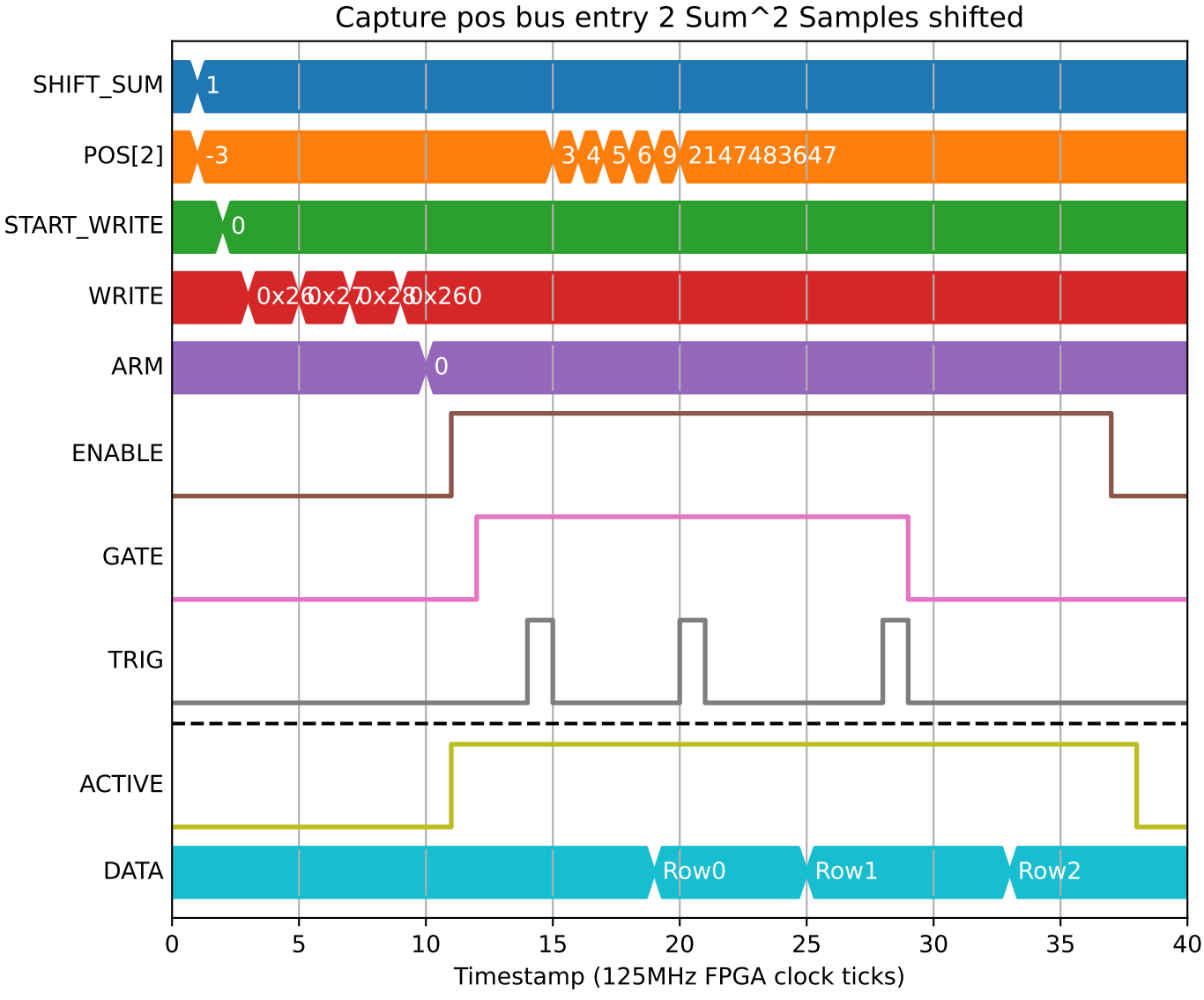
Capture pos bus entry 2 Sum^2 Samples shifted
SHIFT_SUM
1
POS[2]
-3
3
4
5
6
9
2147483647
START_WRITE
0
WRITE
0x260
0x260
0x280
0x260
ARM
0
ENABLE
GATE
TRIG
ACTIVE
DATA
Row0
Row1
Row2
0
5
10
15
20
25
30
35
40
Timestamp (125MHz FPGA clock ticks)