

The diagram illustrates the timing of the INPA, INPB, INPC, INPD, INPE, and OUT signals. The INPA signal is high from tick 5 to 8 and 11 to 14. The INPB signal is high from tick 5 to 10. The INPC signal is high from tick 5 to 10. The INPD signal is high from tick 5 to 10. The INPE signal is high from tick 5 to 10. The OUT signal is high from tick 2 to 6 and 11 to 12. A dashed line indicates the output is high when all inputs are high.

INPA

INPB

INPC

INPD

INPE

OUT

0

2

6

1:

14

Timestamp (125MHz FPGA clock ticks)