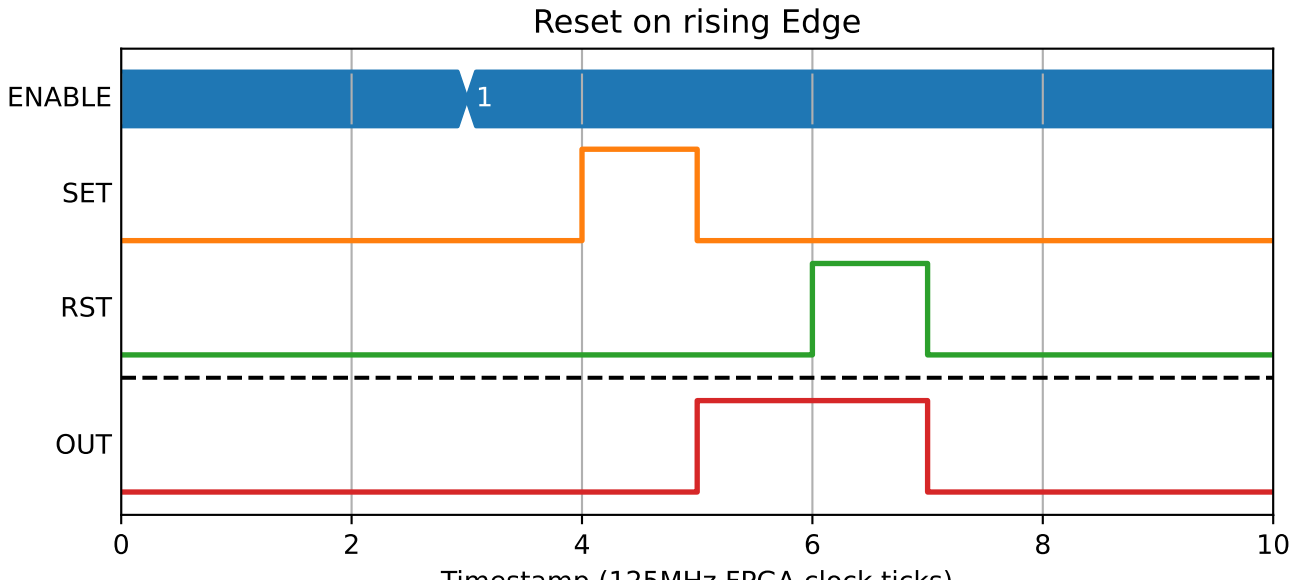
Reset on rising Edge
ENABLE
1
SET
RST
OUT
0
2
4
6
8
10
Timestamp (125MHz FPGA clock ticks)