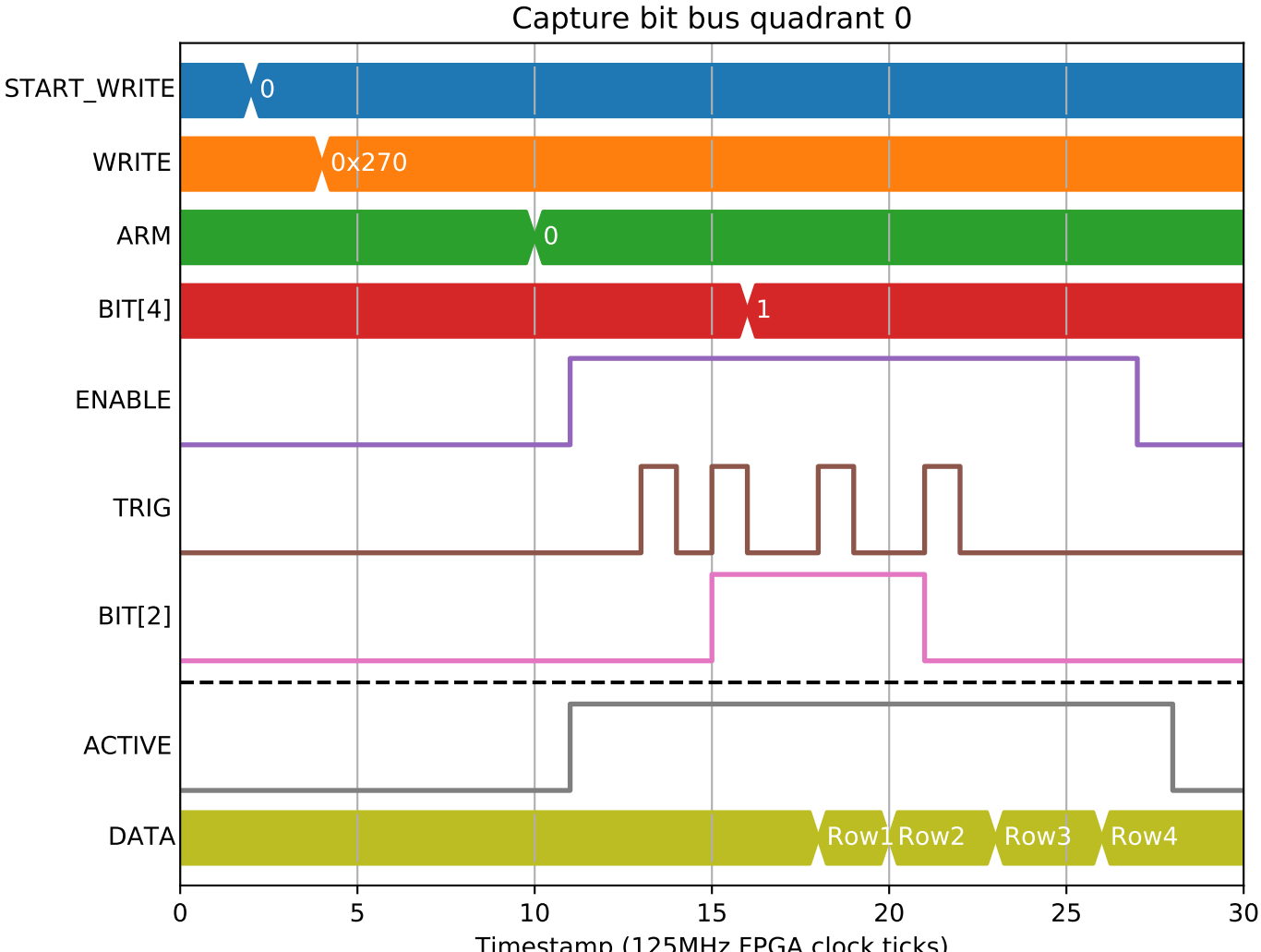
Capture bit bus quadrant 0
START_WRITE
0
WRITE
0x270
ARM
0
BIT[4]
1
ENABLE
TRIG
BIT[2]
ACTIVE
DATA
Row1
Row2
Row3
Row4
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)