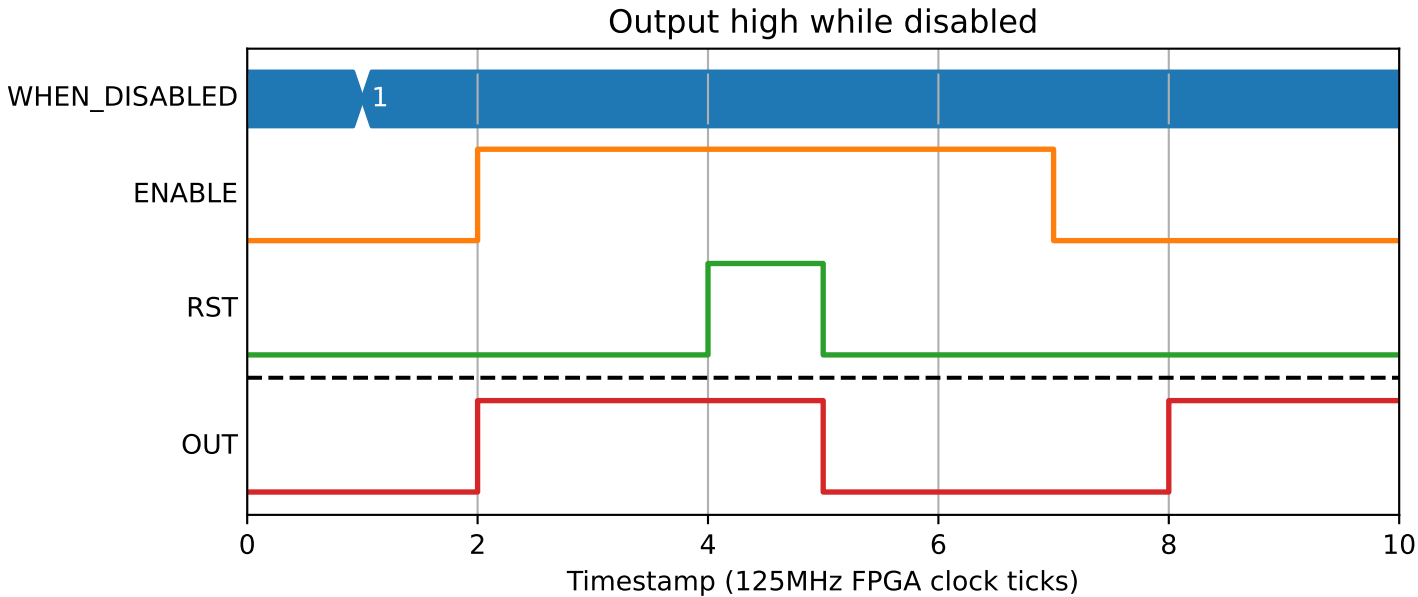
Output high while disabled
WHEN_DISABLED
1
ENABLE
RST
OUT
0
2
4
6
8
10
Timestamp (125MHz FPGA clock ticks)