

The timing diagram illustrates the operation of a 4-bit adder over 40 clock cycles. The signals shown are:

- Input A (Blue):** A constant high signal (1).
- Input B (Orange):** A constant high signal (2147483645).
- Input C (Green):** A constant high signal (1).
- Carry (Red):** A signal that starts at 0, rises to 1 at cycle 6, and remains at 1 until cycle 26. It then drops to 0 at cycle 27, rises to 1 at cycle 29, and remains at 1 until cycle 40. It then drops to 0.
- Sum (Purple):** A signal that is 0 for most of the time, but has narrow pulses at cycles 10, 12, 16, 23, 30, and 36.
- Overflow Flag (Brown):** A signal that is 0 until cycle 27, rises to 1 at cycle 27, and remains at 1 until cycle 40. It then drops to 0.
- Output Y (Pink):** A signal that is 0 until cycle 27, rises to 1 at cycle 27, and remains at 1 until cycle 40. It then drops to 0.

The diagram also includes a dashed horizontal line at the 0 level and a vertical line at cycle 40.

Timestamp (125MHz FPGA clock ticks)