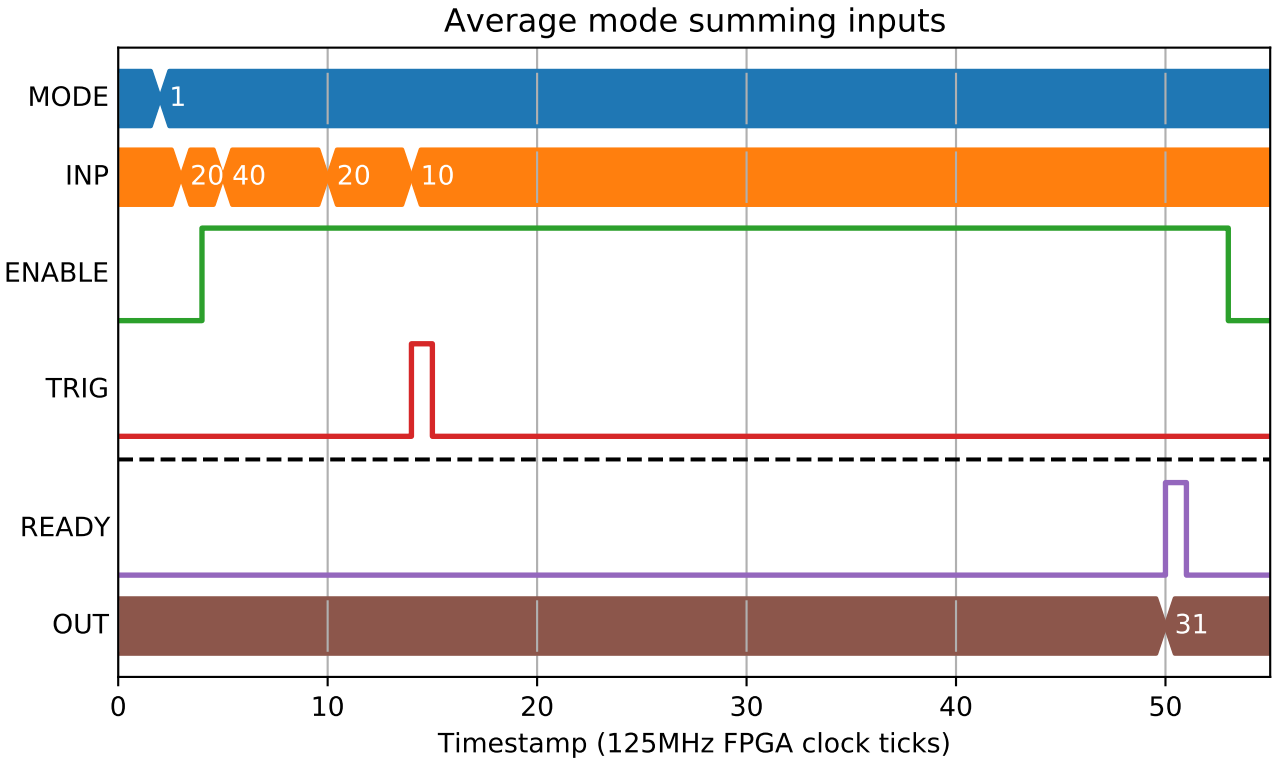
Average mode summing inputs
MODE
INP
ENABLE
TRIG
READY
OUT
1
20
40
20
10
31
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)