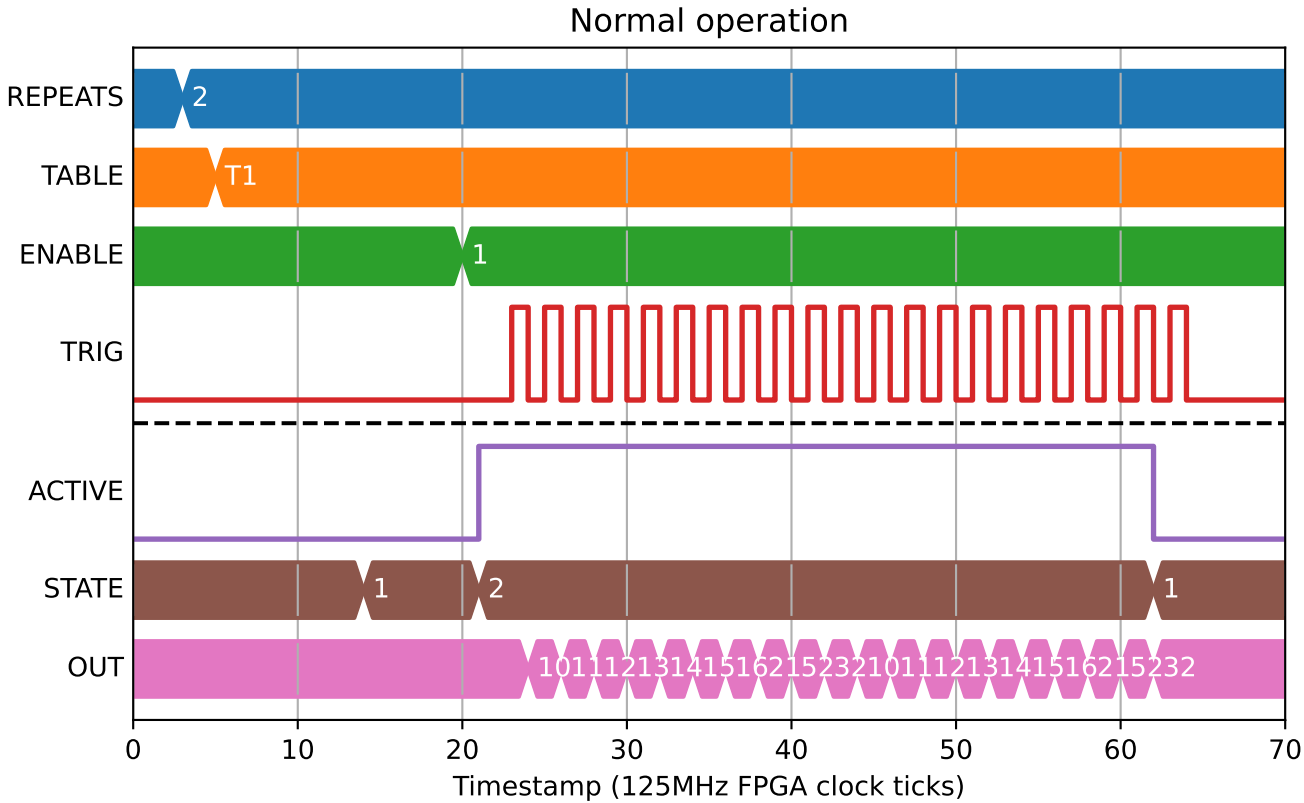
Normal operation
REPEATS
2
TABLE
T1
ENABLE
1
TRIG
ACTIVE
STATE
1
2
1
OUT
1011121314151621523210111213141516215232
0
10
20
30
40
50
60
70
Timestamp (125MHz FPGA clock ticks)