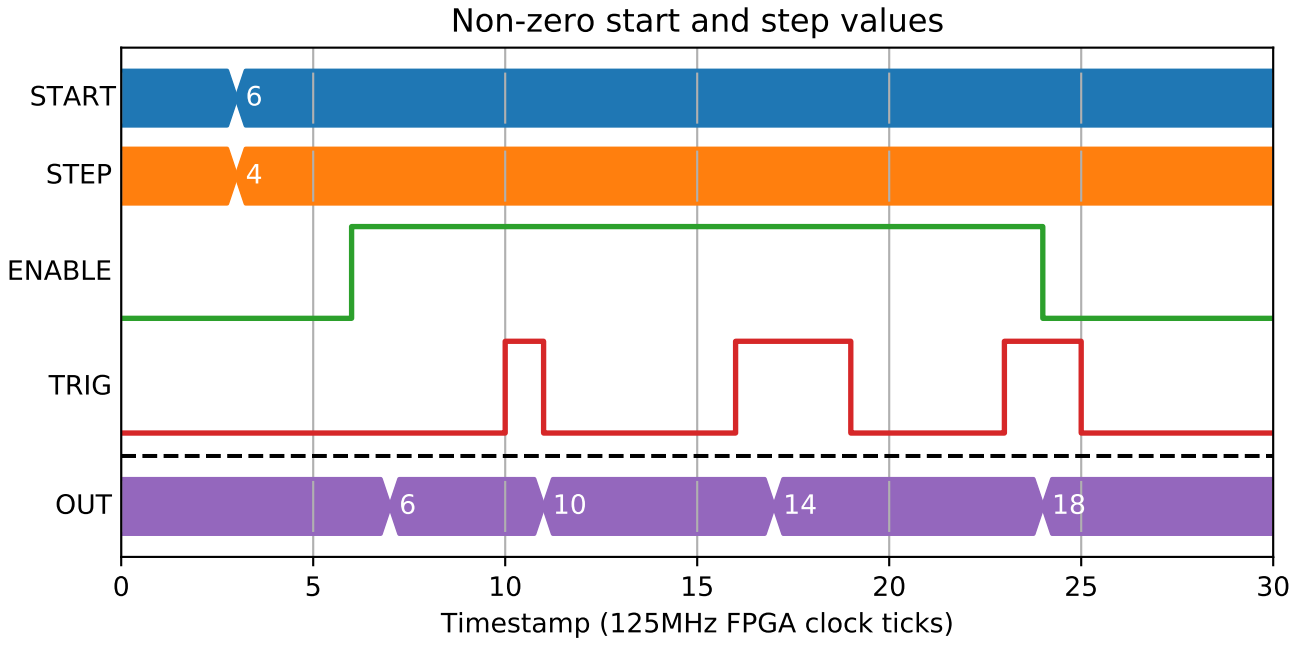
Non-zero start and step values
START
STEP
ENABLE
TRIG
OUT
6
4
6
10
14
18
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)