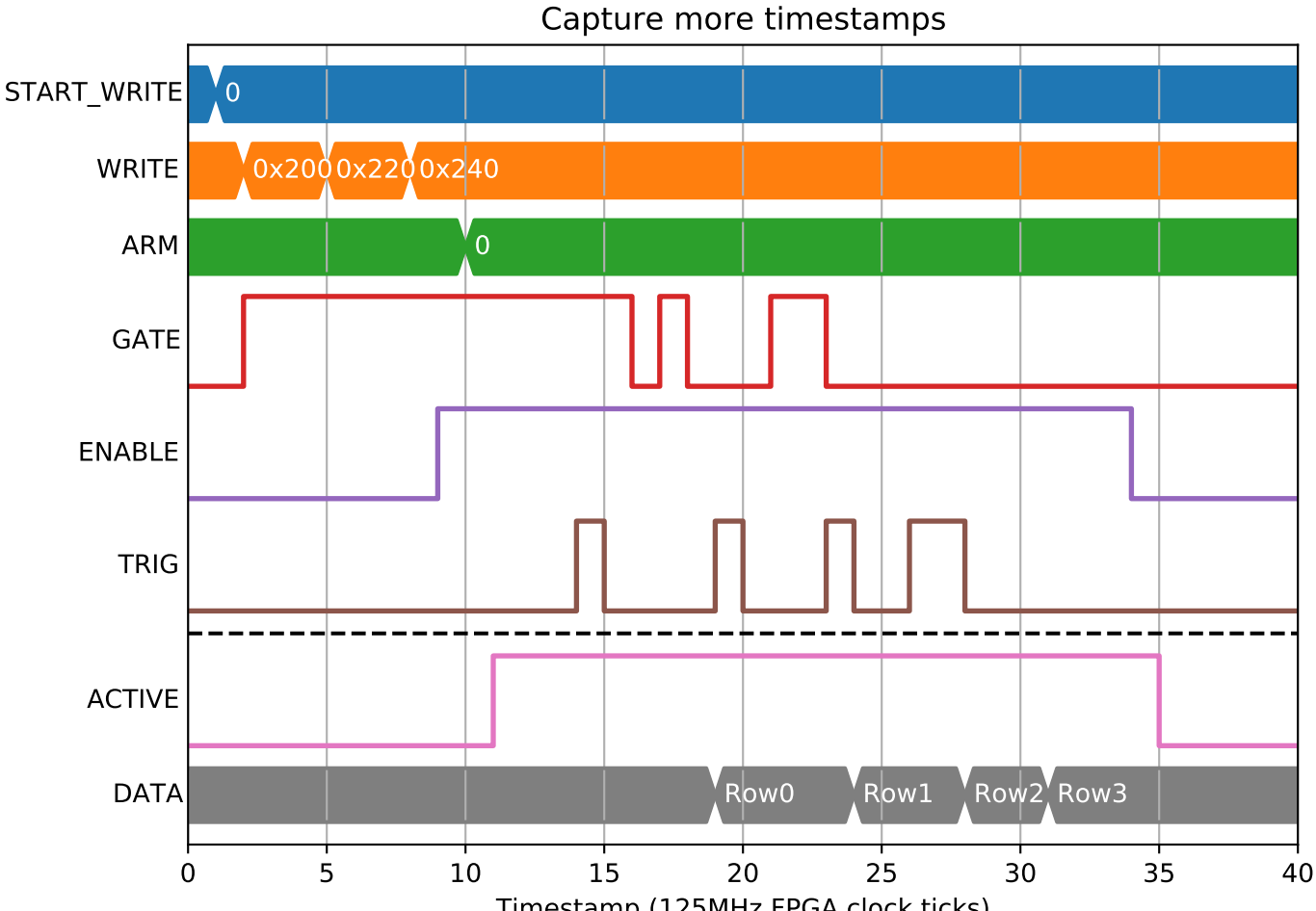
Capture more timestamps
START_WRITE
0
WRITE
0x200
0x220
0x240
ARM
0
GATE
ENABLE
TRIG
ACTIVE
DATA
Row0
Row1
Row2
Row3
0
5
10
15
20
25
30
35
40
Timestamp (125MHz FPGA clock ticks)