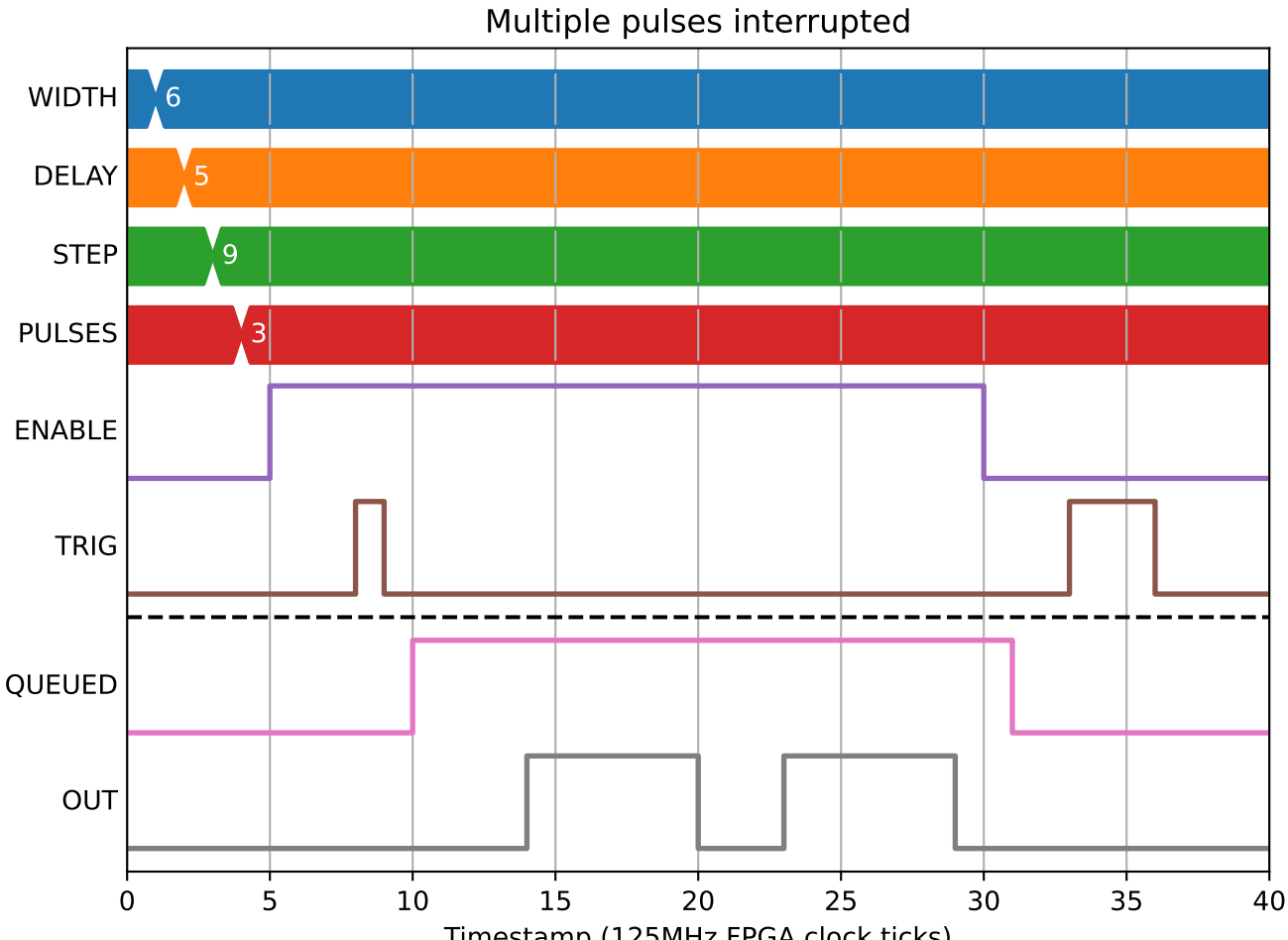
Multiple pulses interrupted
WIDTH
DELAY
STEP
PULSES
ENABLE
TRIG
QUEUED
OUT
6
5
9
3
0
5
10
15
20
25
30
35
40
Timestamp (125MHz FPGA clock ticks)