

The diagram shows three signals over a 30-tick period:

- ENABLE (Blue):** High from tick 3 to 28, low otherwise.
- TRIG (Orange):** High during four intervals: [8, 10), [13, 17), [18, 20), and [29, 30).
- OUT (Green):** A continuous stream of data blocks. The first four blocks are labeled 1, 2, 3, and 4, corresponding to the TRIG intervals.

TRIG

OUT

Timestamp (125MHz FPGA clock ticks)