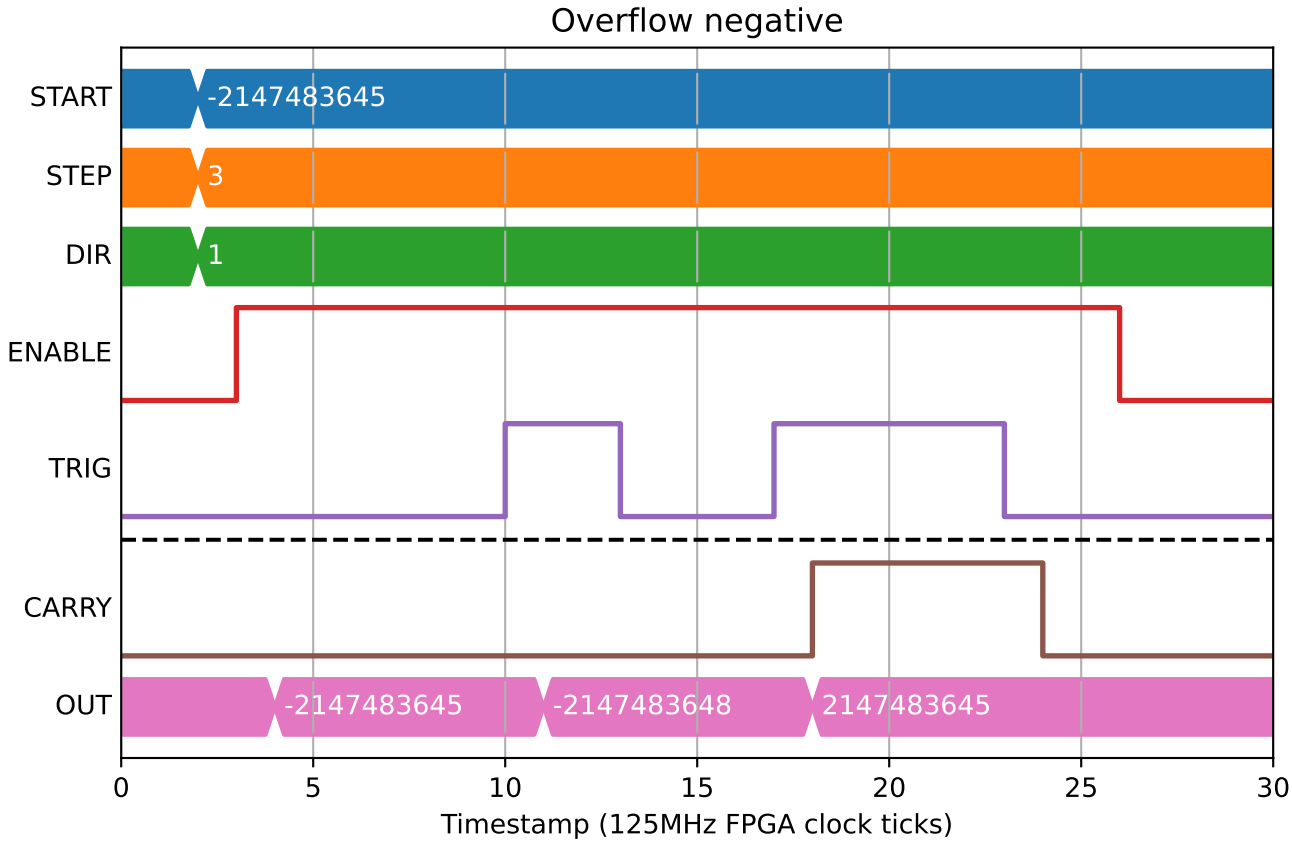
Overflow negative
START
STEP
DIR
ENABLE
TRIG
CARRY
OUT
-2147483645
3
1
-2147483645
-2147483648
2147483645
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)