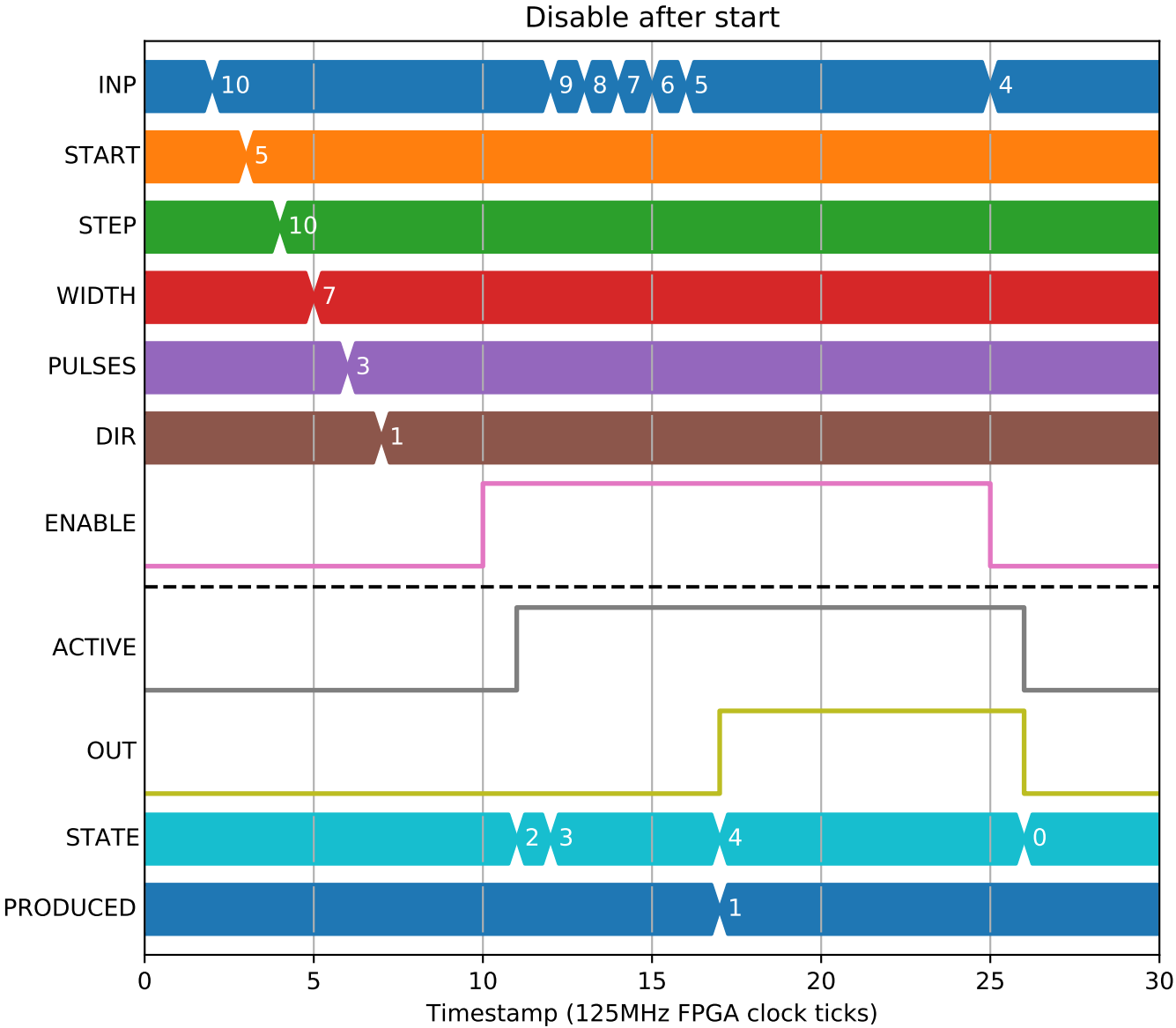
Disable after start
INP
START
STEP
WIDTH
PULSES
DIR
ENABLE
ACTIVE
OUT
STATE
PRODUCED
10
9
8
7
6
5
4
5
10
7
3
1
2
3
4
0
1
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)