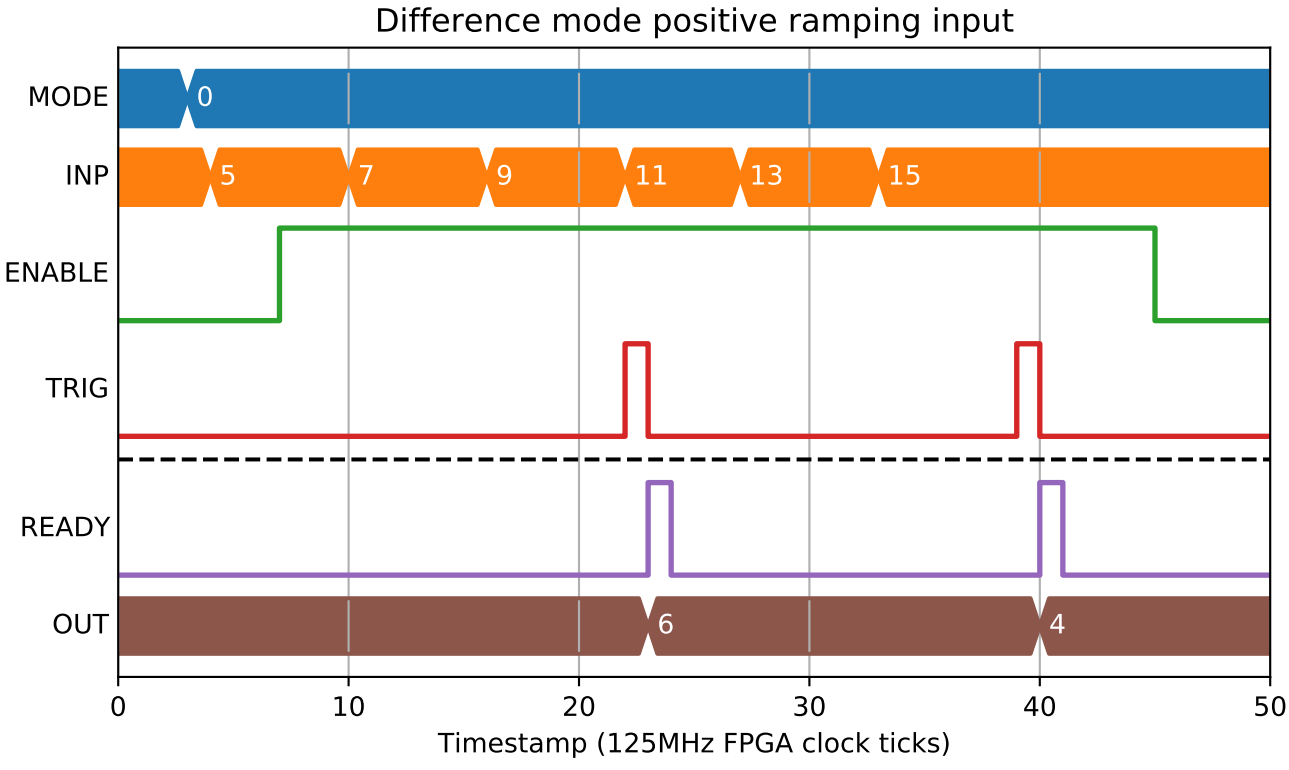
Difference mode positive ramping input
MODE
INP
ENABLE
TRIG
READY
OUT
0
5
7
9
11
13
15
6
4
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)