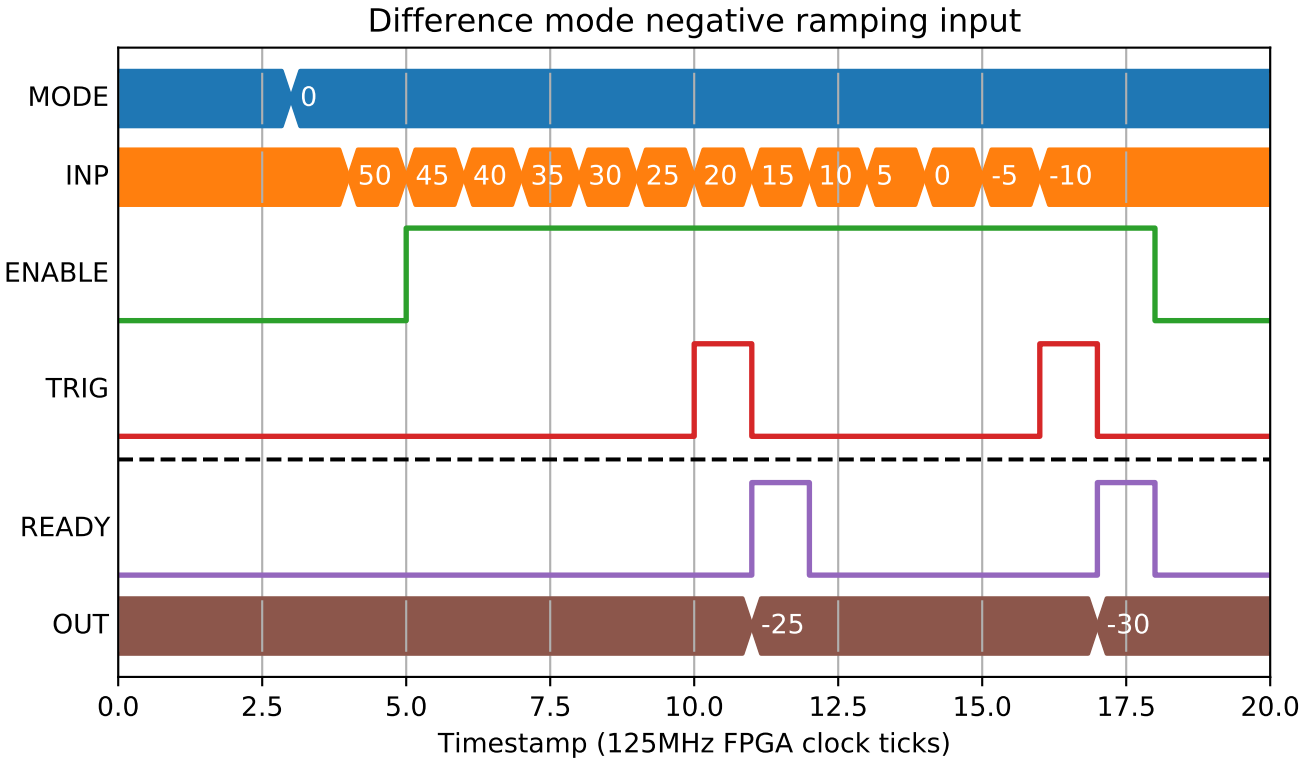
Difference mode negative ramping input
MODE
INP
ENABLE
TRIG
READY
OUT
0
50
45
40
35
30
25
20
15
10
5
0
-5
-10
-25
-30
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
Timestamp (125MHz FPGA clock ticks)