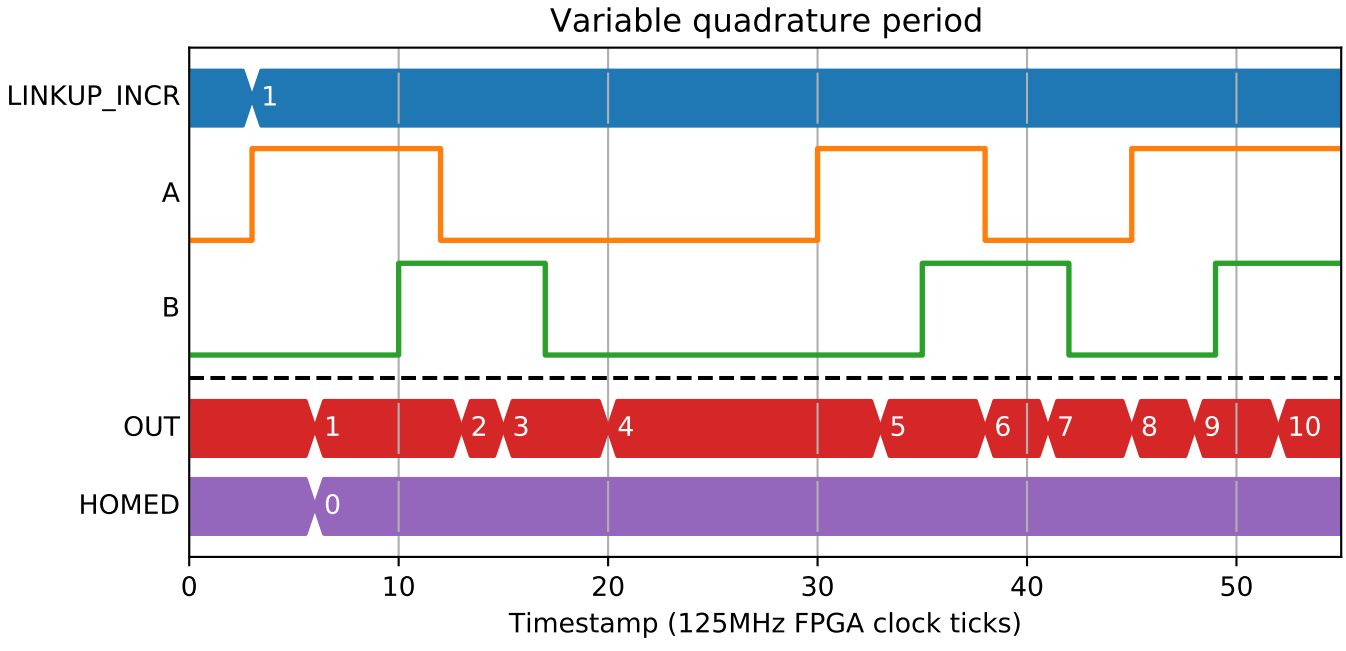
Variable quadrature period
LINKUP_INCR
A
B
OUT
HOMED
1
1
2
3
4
5
6
7
8
9
10
0
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)