

The timing diagram illustrates the operation of a 4-bit ripple-carry adder. The signals are as follows:

- Blue Signal (1):** A constant high signal, likely representing a clock or enable.
- Orange Signal (1987 6542):** The input values being added. The value 1987 is shown in the first 10 ns, and 6542 is shown in the next 10 ns. The signal then transitions to a sequence of 4-bit values: 8, 4, 0, -4, -8, and -10.
- Green Signal:** The carry-in signal, which is high from 10 ns to 58 ns and low otherwise.
- Red Signal:** The carry-out signal, which is high during the first 10 ns, the next 10 ns, and the last 10 ns, and low otherwise.
- Purple Signal:** The sum signal, which is high during the first 10 ns, the next 10 ns, and the last 10 ns, and low otherwise.

The sum of 1987 and 6542 is 8531. The diagram shows the carry-in and carry-out signals for each 4-bit ripple-carry stage. The carry-in is high for the first two stages (10 ns each) and the last stage (10 ns). The carry-out is high for the first two stages and the last stage. The sum is 8531.

Timestamp (125MHz FPGA clock ticks)