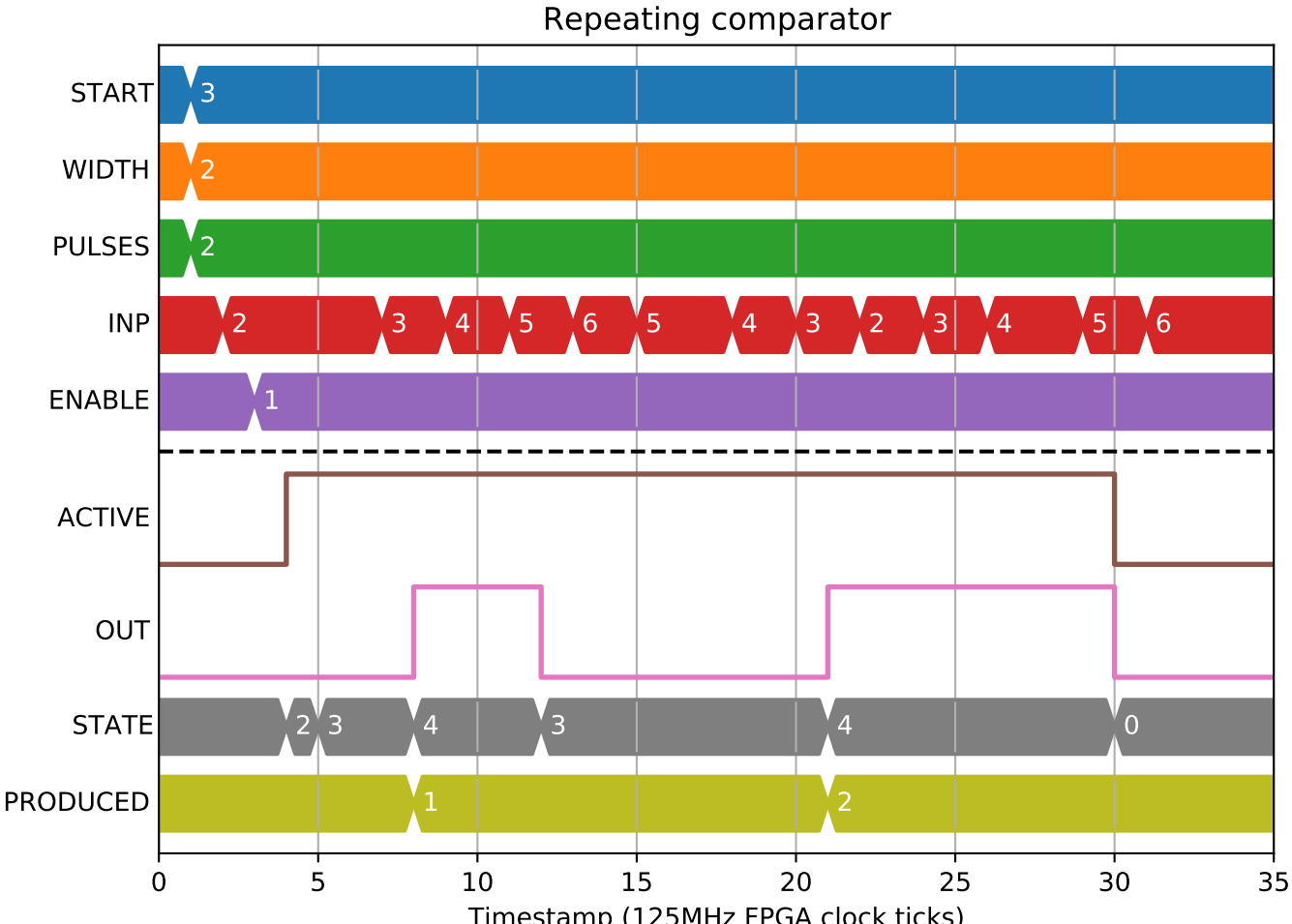
Repeating comparator
START
WIDTH
PULSES
INP
ENABLE
ACTIVE
OUT
STATE
PRODUCED
3
2
2
2 3 4 5 6 5 4 3 2 3 4 5 6
1
2 3 4 3 4 0
1 2
0 5 10 15 20 25 30 35
Timestamp (125MHz FPGA clock ticks)