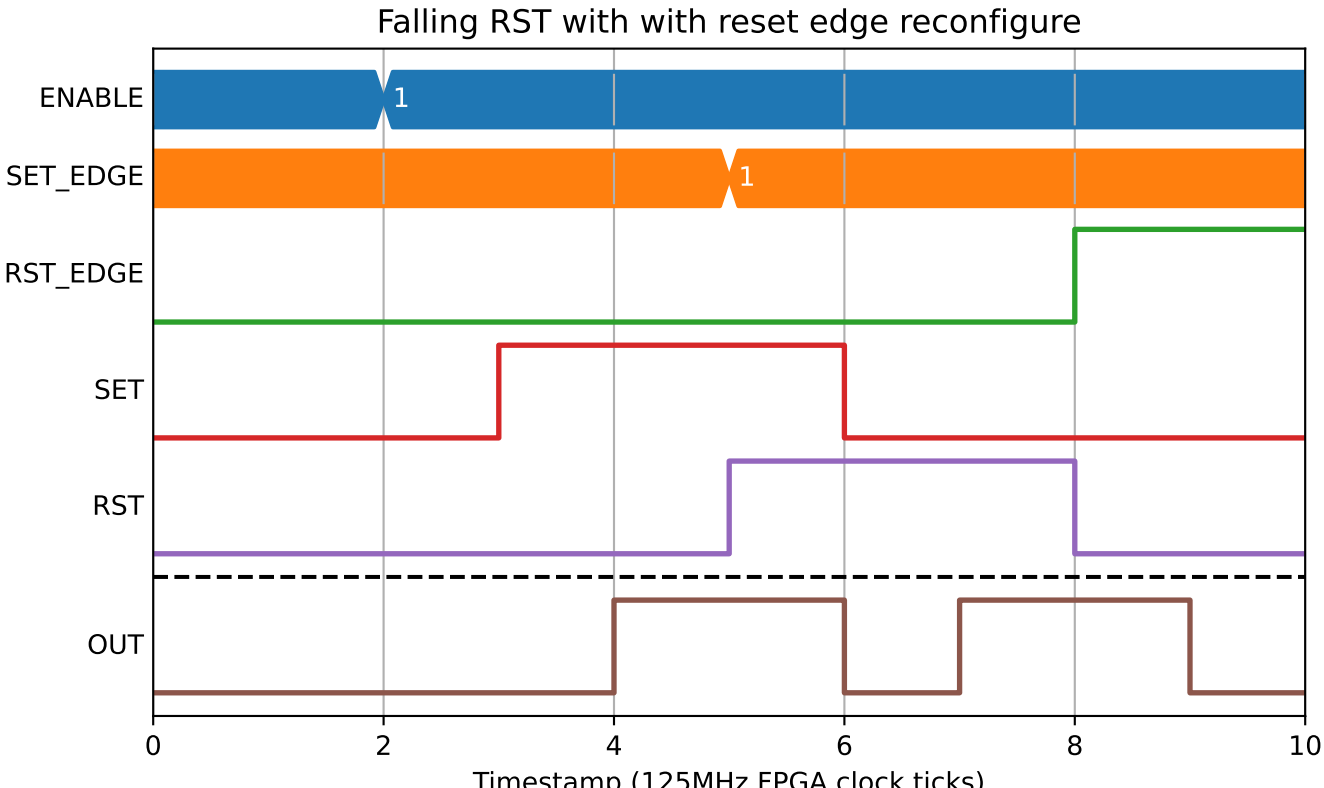
Falling RST with with reset edge reconfigure
ENABLE
1
SET_EDGE
1
RST_EDGE
SET
RST
OUT
0
2
4
6
8
10
Timestamp (125MHz FPGA clock ticks)