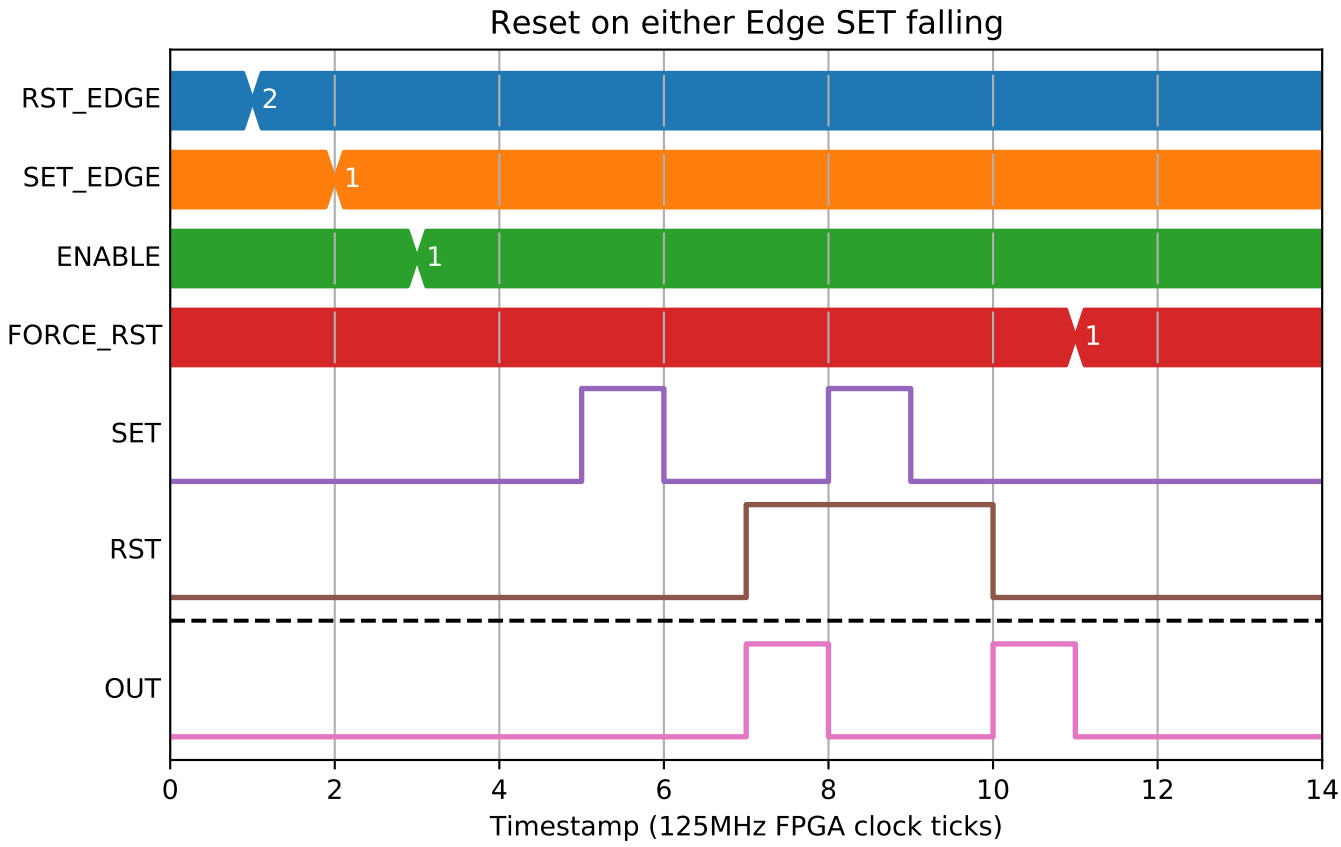
Reset on either Edge SET falling
RST_EDGE
SET_EDGE
ENABLE
FORCE_RST
SET
RST
OUT
2
1
1
1
0
2
4
6
8
10
12
14
Timestamp (125MHz FPGA clock ticks)