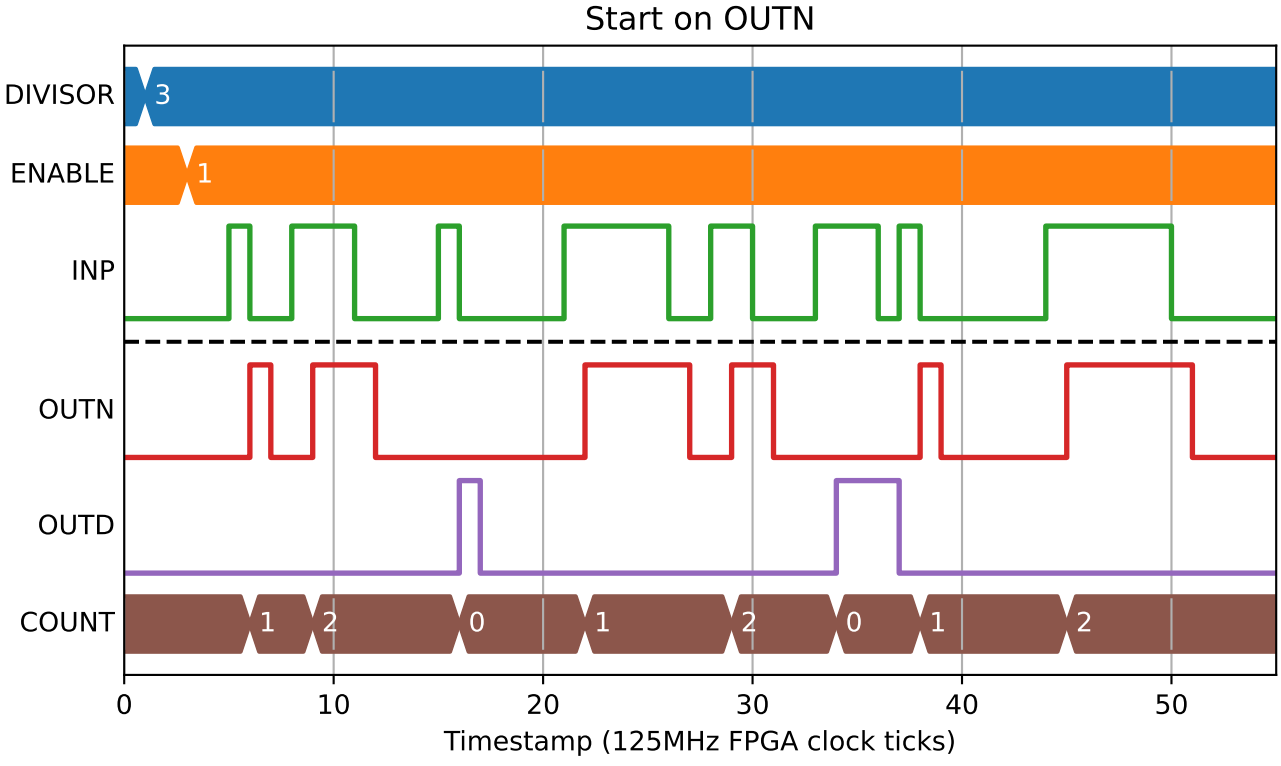
Start on OUTN
DIVISOR
3
ENABLE
1
INP
OUTN
OUTD
COUNT
1
2
0
1
2
0
1
2
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)