

The timing diagram illustrates the operation of a 4-bit ripple-carry adder. The x-axis represents time in clock cycles, from 0 to 9. The y-axis represents the signal level, with a dashed line indicating the zero level.

- Input 1 (Blue):** A constant high signal (1) across all clock cycles.
- Input 2 (Orange):** A sequence of 4-bit values: 10, 11, 12, 8, 4, 0, -4, -8, -10. These are represented by a series of pulses with varying widths and positions.
- Carry (Green):** A signal that starts at 0, rises to 1 at clock cycle 5, and returns to 0 at clock cycle 6.
- Sum (Red):** A signal that starts at 0, rises to 1 at clock cycle 10, and returns to 0 at clock cycle 11.
- Sum (Purple):** A signal that starts at 0, rises to 1 at clock cycle 15, and returns to 0 at clock cycle 16.
- Sum (Brown):** A signal that starts at 0, rises to 1 at clock cycle 20, and returns to 0 at clock cycle 21.

Timestamp (125MHz FPGA clock ticks)