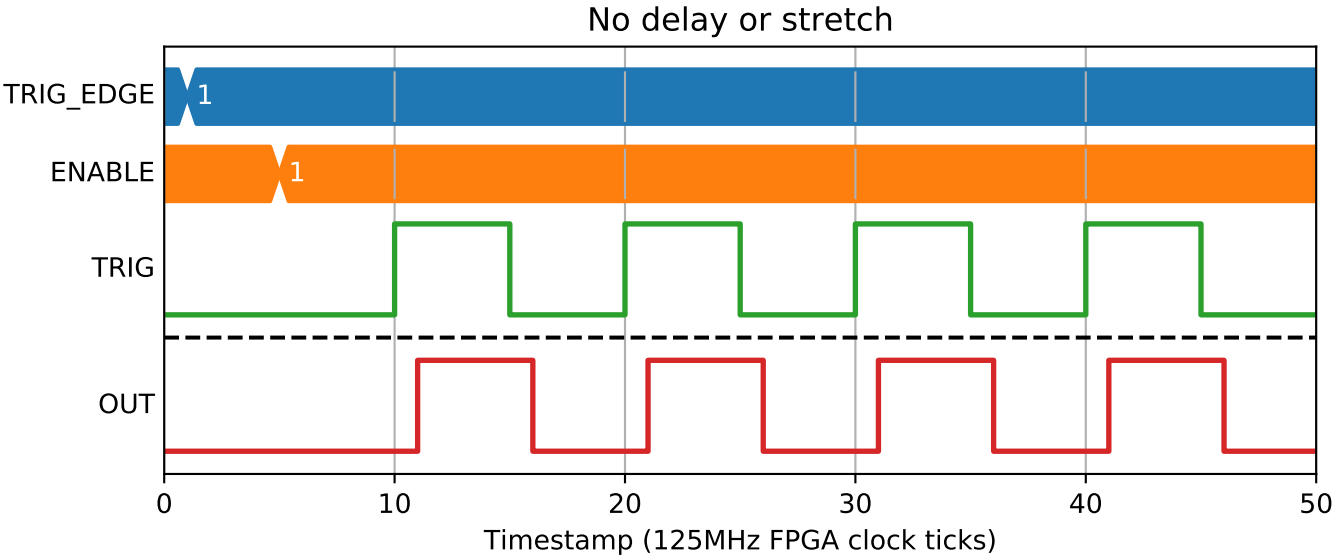
No delay or stretch
TRIG_EDGE
1
ENABLE
1
TRIG
OUT
0
10
20
30
40
50
Timestamp (125MHz FPGA clock ticks)