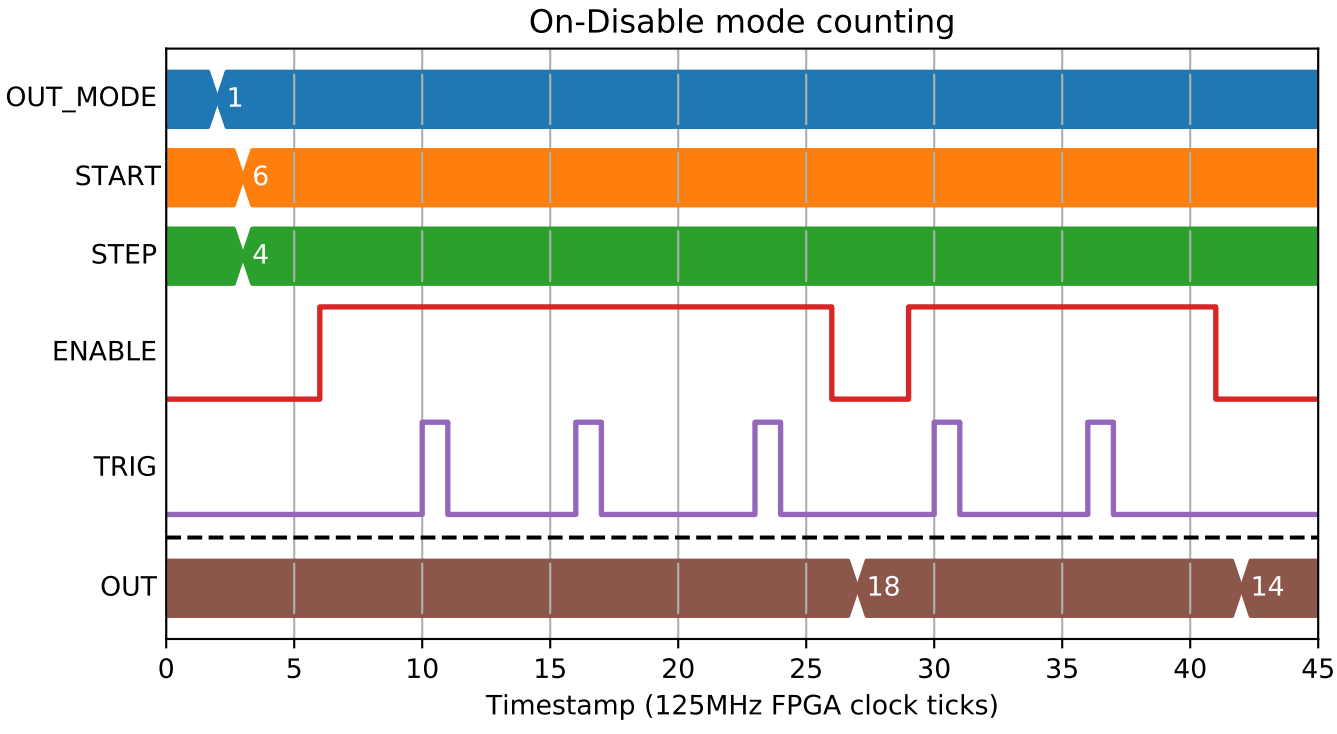
On-Disable mode counting
OUT_MODE
START
STEP
ENABLE
TRIG
OUT
1
6
4
18
14
0
5
10
15
20
25
30
35
40
45
Timestamp (125MHz FPGA clock ticks)