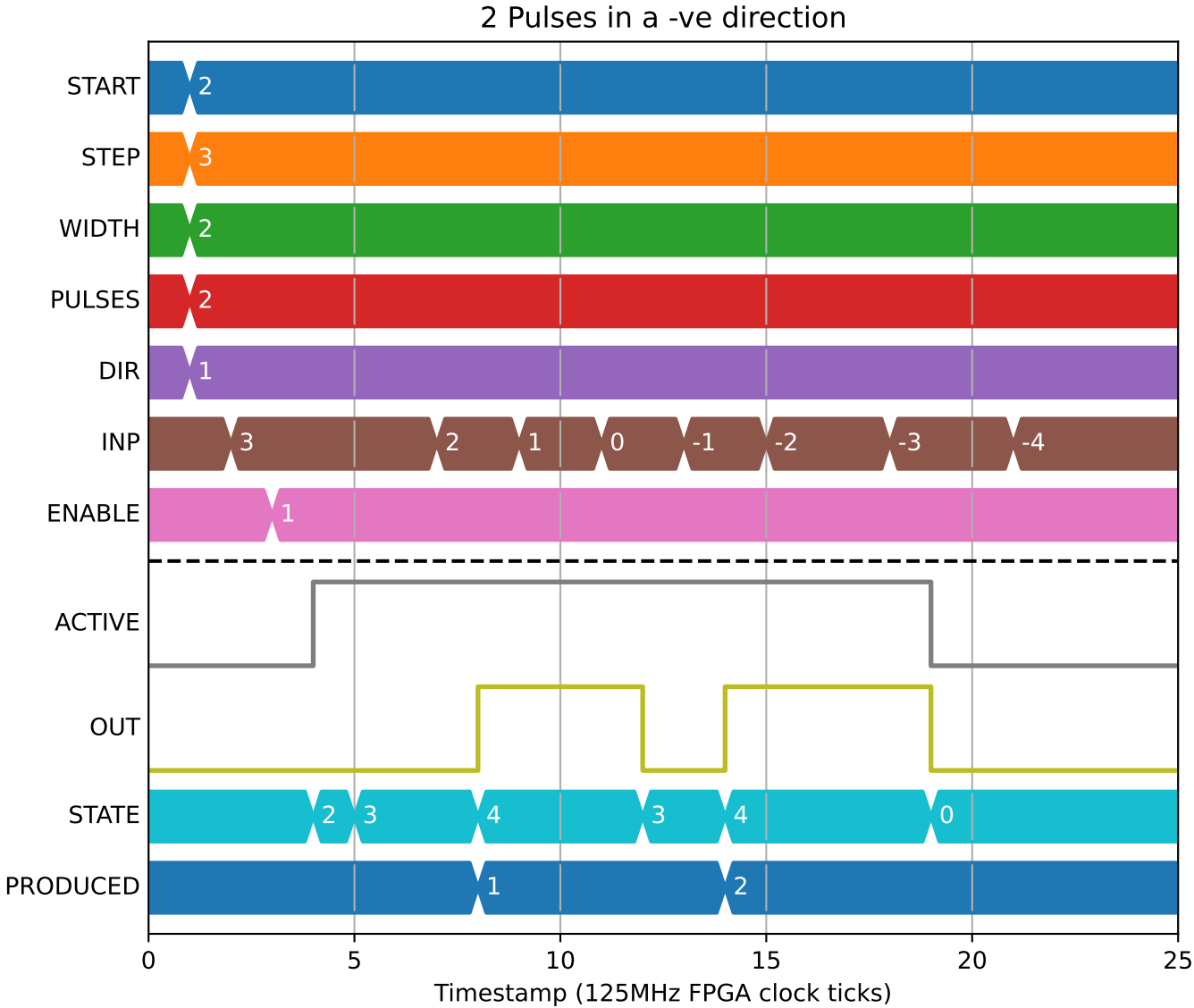
2 Pulses in a -ve direction
START
STEP
WIDTH
PULSES
DIR
INP
ENABLE
ACTIVE
OUT
STATE
PRODUCED
2
3
2
2
1
3
2
1
0
-1
-2
-3
-4
1
2
3
4
3
4
0
1
2
0
5
10
15
20
25
Timestamp (125MHz FPGA clock ticks)