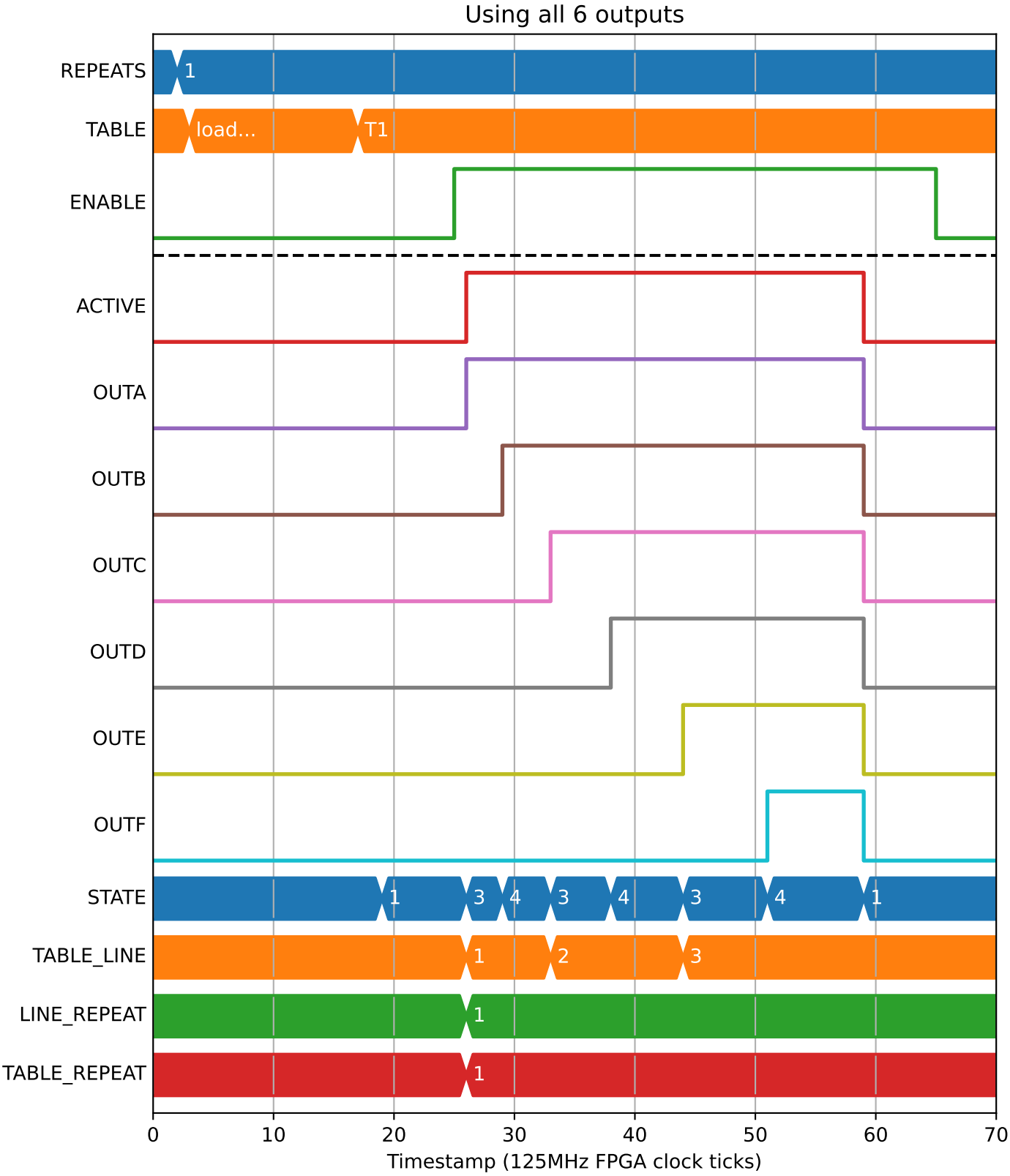
Using all 6 outputs
REPEATS
1
TABLE
load...
T1
ENABLE
ACTIVE
OUTA
OUTB
OUTC
OUTD
OUTE
OUTF
STATE
1
3
4
3
4
3
4
1
TABLE_LINE
1
2
3
LINE_REPEAT
1
TABLE_REPEAT
1
0
10
20
30
40
50
60
70
Timestamp (125MHz FPGA clock ticks)