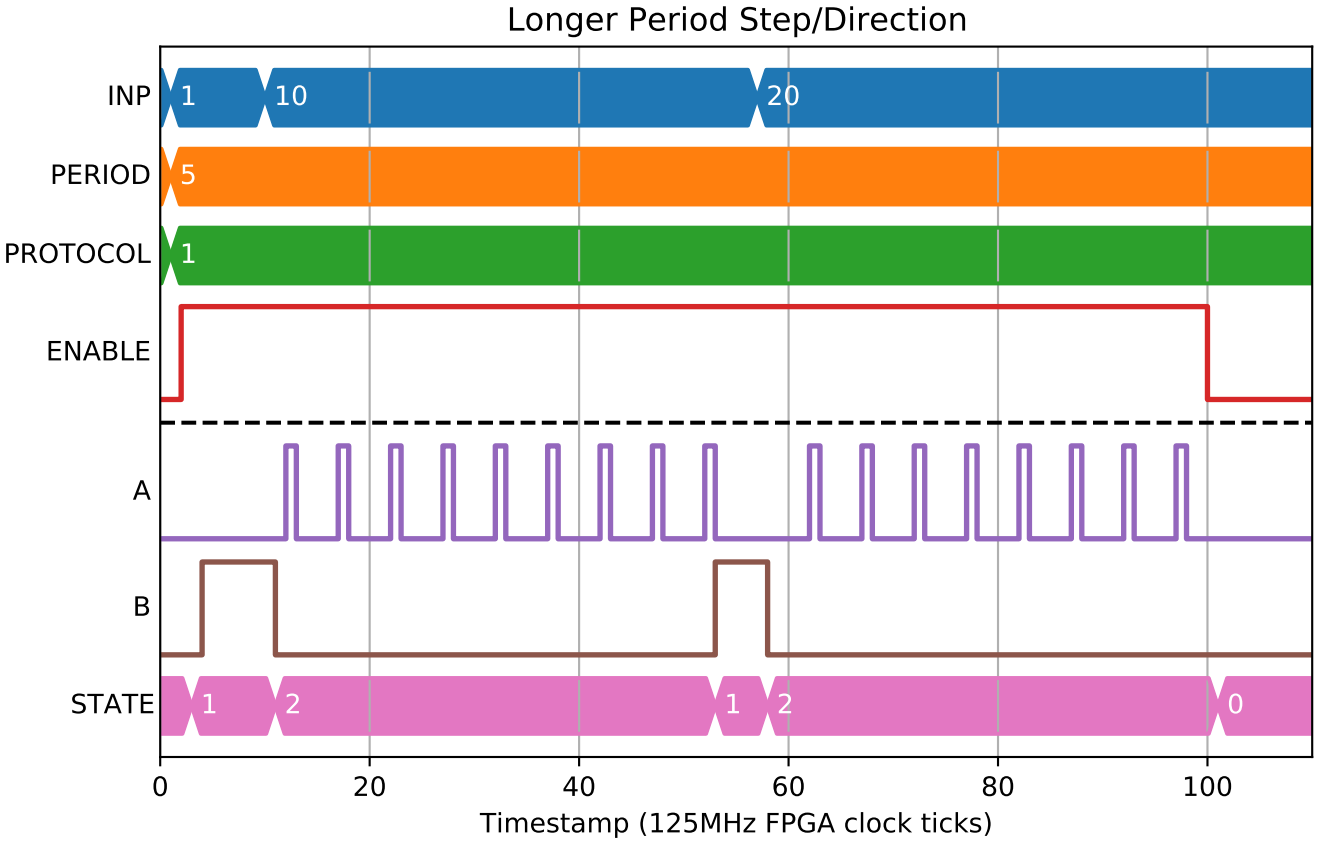
Longer Period Step/Direction
INP
PERIOD
PROTOCOL
ENABLE
A
B
STATE
1
10
20
5
1
1
2
1
2
0
0
20
40
60
80
100
Timestamp (125MHz FPGA clock ticks)