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Rev. 0, 15 October 2018

QorIQ LS1046A Reference Design Board Errata

This document lists and describes all known errata for the LS1046ARDB. It also provides available workaround with detailed explanation, wherever required, for each erratum.

The table below lists the revision history of this document.

Table 1. Revision history

Revision	Date	Description
Rev. 0	10/2018	Initial public release

This table summarizes all known errata and their workarounds for the LS1046ARDB.

Table 2. LS1046ARDB errata summary

Errata	Name	Workaround	Applicable PCB revision	Applicable schematics (SCH-29142) revision
E-00001	AQR107-ES2 MDIO voltage configuration changed as per ES2 part requirements	Remove R70 (0 Ω) and populate R69 (4.99 KΩ)	Rev. B	Rev. B
E-00002	When SFP+ module is inserted, its I2C address conflicts with that of SPD	Cut SFP cage's I2C traces	Rev. B	Rev. B
E-00003	FA_VL pin is connected to VDD	Remove the J13 shunt	Rev. B	Rev. B or B1

The table below lists the additional documents that you can refer to, for more information about the LS1046ARDB. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to such documents, contact your local field applications engineer or sales representative.

Table 3. Related documentation

Document	Description	Web link
QorIQ LS1046A Reference Design Board Reference Manual (LS1046ARDBRM)	Explains the LS1046ARDB interfaces and configuration	LS1046ARDB product summary page - Documentation tab
QorIQ LS1046A Reference Design Board Getting Started Guide (LS1046ARDBGSG)	Describes the LS1046ARDB hardware kit, provides settings for the onboard switches, connectors, jumpers, and LEDs, and explains the basic board operations in a step-by-step manner	
Updating SDK Images on QorIQ LS1046ARDB Application Note (AN5340)	Describes how to deploy U-Boot, Linux kernel, and root file system on the QorIQ LS1046ARDB using QorIQ SDK images	
QorIQ LS1046A BSP v0.4 (QORIQ-LS1046A-BSP)	Provides detailed information about QorIQ LS1046A BSP v0.4	
QorIQ LS1046ARDB Schematics (SCH-29142)	Provides detailed information about the LS1046ARDB circuitry	LS1046ARDB product summary page - Software and Tools tab (bundled with the LS1046ARDB design file package)
QorIQ LS1046A Reference Manual (LS1046ARM)	Provides a detailed description of the LS1046A multicore processor and its features, such as the memory map, serial interfaces, power supply, chip features, and clock information	LS1046A product summary page
QorIQ LS1046A Data Sheet (LS1046A)	Contains information on LS1046A pin assignments, electrical characteristics, hardware design considerations, package information, and ordering information	
QorIQ LS1046A Design Checklist (AN5252)	Provides recommendations for new designs based on the LS1046A/LS1026A processor	This document is currently under NDA. After it becomes public, it will be posted at the LS1046A product summary page.

NOTE

In case of any mismatch between the board schematics and SoC datasheet, the SoC datasheet is recommended to be followed.

E-00001: AQR107-ES2 MDIO voltage configuration changed as per ES2 part requirements

Description: As per AQR107-ES2 revision A0, the polarity of MDIO_1P2_SELECT_N is inverted as follows:

- When pulled low, the voltage level is 1.8 V - 2.1 V
- When pulled high, the voltage level is 2.5 V - 3.3 V

Impact: AQR107 firmware cannot be programmed and MDIO cannot work.

Workaround: Remove R70 (0 Ω) and populate R69 (4.99 KΩ).

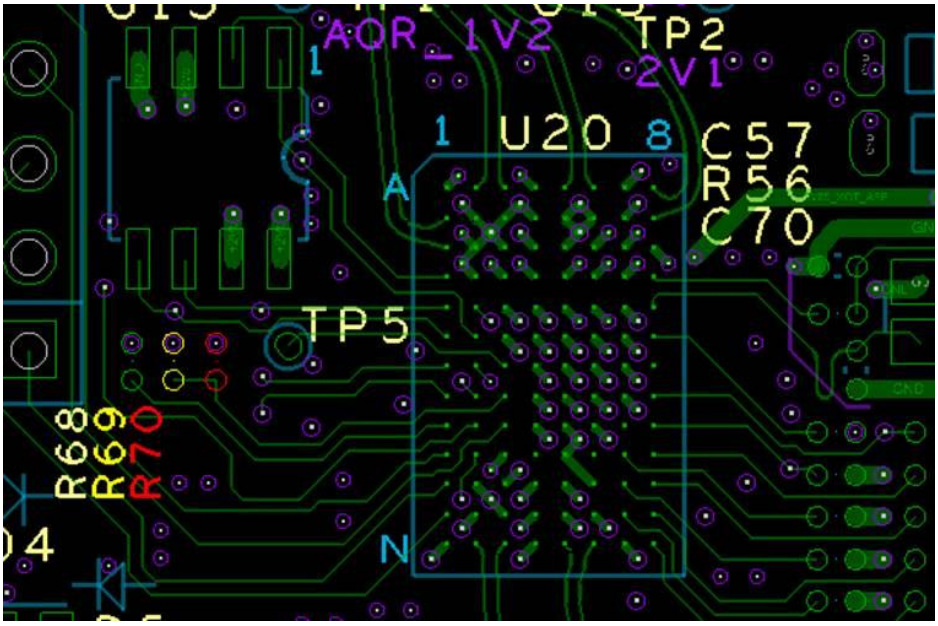

Figure 1. E-00001 workaround

Fix plan: The above mentioned rework has been implemented on all revision B boards. Starting board revision B1, no rework is needed.

E-00002: When SFP+ module is inserted, its I2C address conflicts with that of SPD

Description: When SFP+ module is inserted into the LS1046ARDB, then an I2C address conflict happens between SFP+ module and SPD.

Impact: Board stops booting if SFP+ module is inserted.

Workaround: Follow these steps:

1. Cut off top layer trace I2C1_SDA and I2C1_SCL before and after vertical interconnect access (via) (1900.60 4402.20) and via (1947.42 4375.42).
2. Fly wire from via (2100.20 3702.90) to pin 5 of U22.
3. Fly wire from via (2065.00 3748.60) to pin 4 of U22.

E-00002: When SFP+ module is inserted, its I2C address conflicts with that of SPD

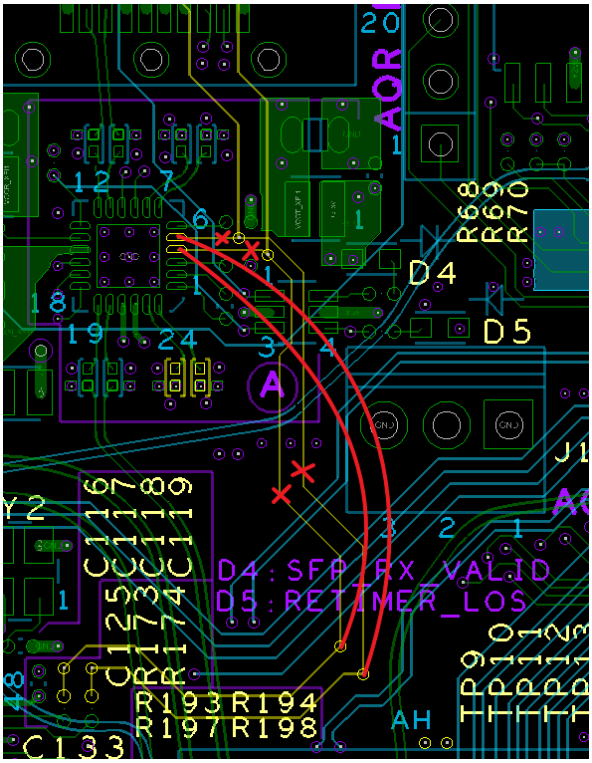

Figure 2. Rework demonstrated on PCB layout

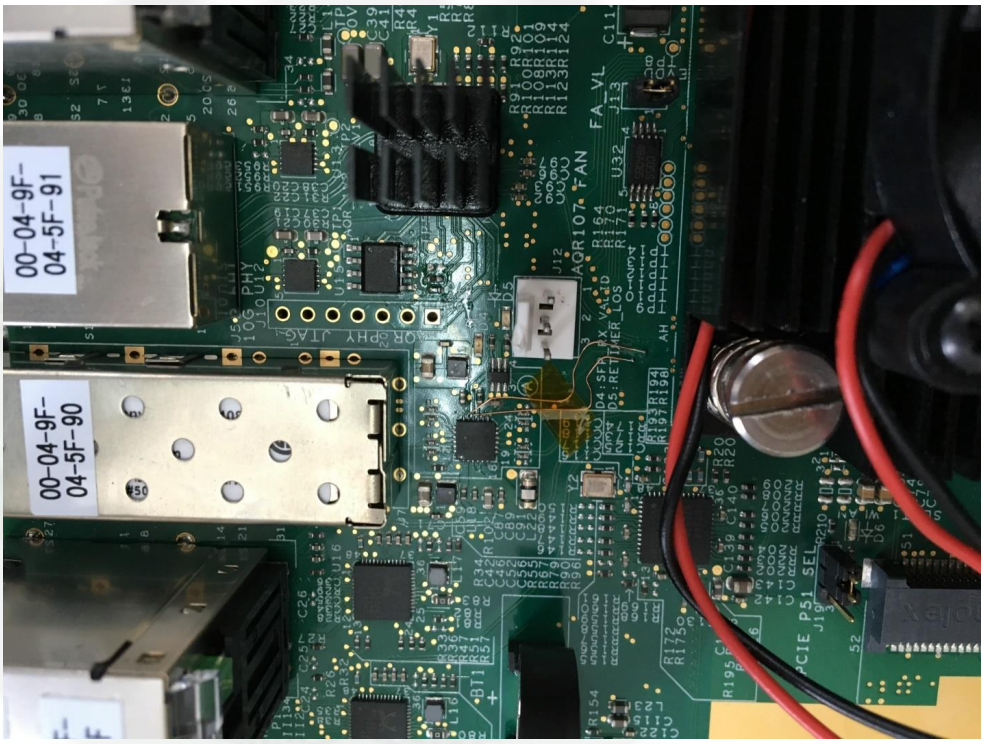

Figure 3. Rework implemented on PCB assembly (PCBA)

After the rework, SFP+ module cannot be accessed through I2C1.

Fix plan: The above mentioned rework needs to be implemented on all revision B boards. Starting board revision B1, no rework is needed. On the PCB Gerber file, I2C connection is disconnected from the SFP slot.

E-00003: FA_VL pin is connected to VDD

Description: The FA_VL pin has a jumper (J13) to select GND or VDD. On some early-shipped boards, J13 is shorted. The J13 shunt needs to be removed to select GND.

Impact: This may impact Linux kernel stability.

Workaround: Remove the J13 shunt.

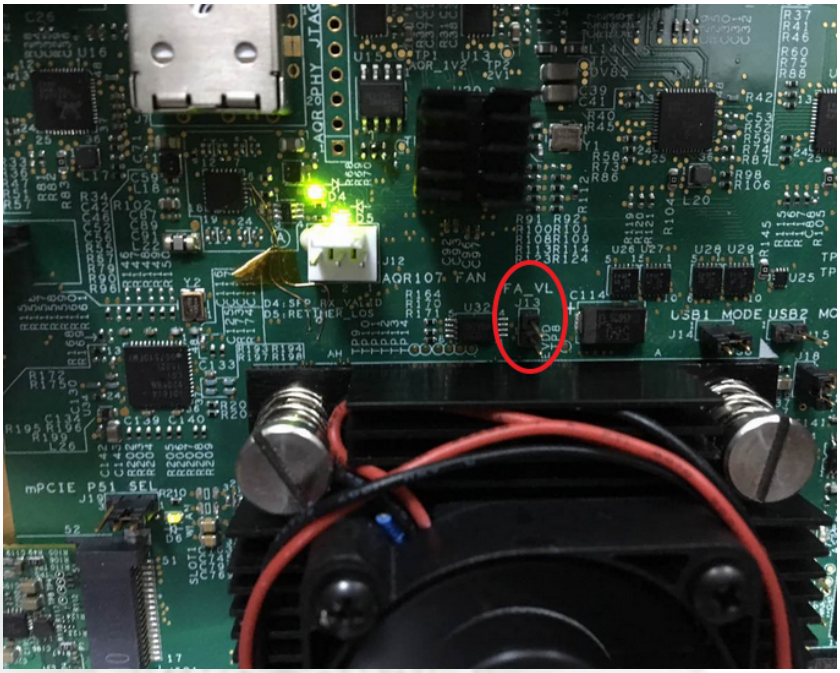

Figure 4. E-00003 workaround

Fix plan: The J13 shunt must be removed from all boards with revision B or later.

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