Σχεδίαση Ψηφιακών Συστημάτων

ΕΞΑΜΗΝΙΑΙΑ ΑΣΚΗΣΗ ΘΕΩΡΙΑΣ

ΜΕΡΟΣ 02

Τμήμα Μηχανικών Πληροφορικής

& Υπολογιστών

(Καθηγητής: Ιωάννης Βογιατζής)

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ALU Control Unit

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3
4  ENTITY ALU_Control IS PORT (
5      OP_5to0: IN STD_LOGIC_VECTOR(5 DOWNTO 0);
6      ALU_op: IN STD_LOGIC_VECTOR(1 DOWNTO 0);
7      Operation: OUT STD_LOGIC_VECTOR(3 DOWNTO 0));
8  END ALU_Control;
9
10 architecture behavioural of ALU_Control is
11     signal OP_5to0_sig: STD_LOGIC_VECTOR(3 downto 0);
12     signal ALU_op_sig: STD_LOGIC_VECTOR(3 downto 0);
13 begin
14 with OP_5to0(3 downto 0) select
15 OP_5to0_sig <=
16     "0010" when "0000",
17     "0110" when "0010",
18     "0000" when "0100",
19     "0001" when "0101",
20         "0111" when "1010",
21     "1111" when others;
22 with ALU_op select
23 ALU_op_sig <=
24     "0010" when "00",
25     "0110" when "01",
26     "1111" when others;
27 with ALU_op select
28 Operation <=
29     OP_5to0_sig when "10",
30     ALU_op_sig  when others;
31 end behavioural;
```

Εικ2.1.1: Κώδικας αρχείου VHDL κυκλώματος ελεγκτή Αριθμητικής και Λογικής μονάδας.

```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all;
3
4   entity ALU_Control_tb is
5   end ALU_Control_tb;
6
7   architecture test_b of ALU_Control_tb is
8   signal OP_5to0_1: STD_LOGIC_VECTOR(5 DOWNTO 0);
9   signal ALU_op1 : STD_LOGIC_VECTOR(1 DOWNTO 0);
10  signal Operation1   : STD_LOGIC_VECTOR(3 DOWNTO 0);
11
12  component ALU_Control PORT (
13      OP_5to0: IN STD_LOGIC_VECTOR(5 DOWNTO 0);
14      ALU_op: IN STD_LOGIC_VECTOR(1 DOWNTO 0);
15      Operation: OUT STD_LOGIC_VECTOR(3 DOWNTO 0));
16  end component;
17
18  BEGIN
19  M1: ALU_Control port map (OP_5to0 => OP_5to0_1, ALU_op => ALU_op1, Operation => Operation1);
20  process
21  begin
22      ALU_op1 <= "00";
23      OP_5to0_1 <= "001001";
24      wait for 50 ps;
25
26      ALU_op1 <= "00";
27      OP_5to0_1 <= "001010";
28      wait for 50 ps;
29
30      ALU_op1 <= "01";
31      OP_5to0_1 <= "100111";
32      wait for 50 ps;
33
34      ALU_op1 <= "10";
35      OP_5to0_1 <= "100000";
36      wait for 50 ps;
37
38      ALU_op1 <= "10";
39      OP_5to0_1 <= "100010";
40      wait for 50 ps;
41
42      ALU_op1 <= "10";
43      OP_5to0_1 <= "100100";
44      wait for 50 ps;
45
46      ALU_op1 <= "10";
47      OP_5to0_1 <= "100101";
48      wait for 50 ps;
49
50      ALU_op1 <= "10";
51      OP_5to0_1 <= "101010";
52      wait for 50 ps;
53  end process;
54  end test_b;
```

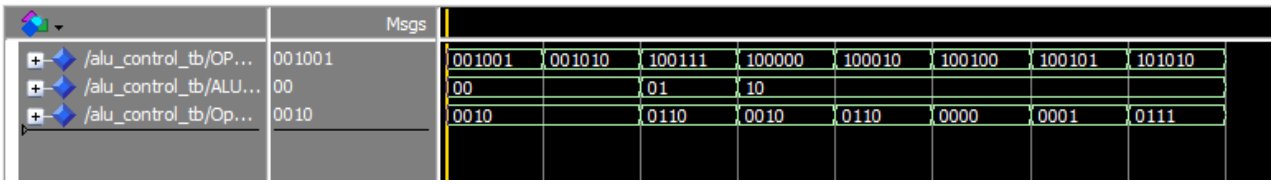
Εικ2.1.2: Κώδικας αρχείου VHDL testbench κυκλώματος ελεγκτή Αριθμητικής και Λογικής μονάδας.

2.2

Πίν2.2: Πίνακας ζητούμενων τιμών για ALU Control.

ALUOp	OP 5to0	Operation (Λειτουργία)
00	001001	0010
00	001010	0010
01	100111	0110
10	100000	0010
10	100010	0110
10	100100	0000
10	100101	0001
10	101010	0111

Οι τιμές που παίρνει έξοδος “Operation” στον παραπάνω πίνακα του ελεγκτή ALU επαληθεύονται στην κυματομορφή της Εικόνας 2.3.



Εικ2.1.3: Παράδειγμα λειτουργίας κυκλώματος ελεγκτή Αριθμητικής και Λογικής μονάδας μέσω κυματομορφής.

2.3

```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all;
3
4   ENTITY ALU_Control IS PORT (
5       OP_5to0: IN STD_LOGIC_VECTOR(5 DOWNTO 0);
6       ALU_op: IN STD_LOGIC_VECTOR(1 DOWNTO 0);
7       Operation: OUT STD_LOGIC_VECTOR(3 DOWNTO 0));
8   END ALU_Control;
9
10  architecture behavioural of ALU_Control is
11      signal OP_5to0_sig: STD_LOGIC_VECTOR(3 downto 0);
12      signal ALU_op_sig: STD_LOGIC_VECTOR(3 downto 0);
13  begin
14  with OP_5to0(3 downto 0) select
15  OP_5to0_sig <=
16      "0010" when "0000",
17      "0110" when "0010",
18      "0000" when "0100",
19      "0001" when "0101",
20      "0111" when "1010",
21      "1111" when others;
22  with ALU_op select
23  ALU_op_sig <=
24      "0010" when "00",
25      "0110" when "01",
26      "1111" when others;
27  with ALU_op select
28  Operation <=
29      OP_5to0_sig when "10",
30      ALU_op_sig  when others;
31  end behavioural;
```

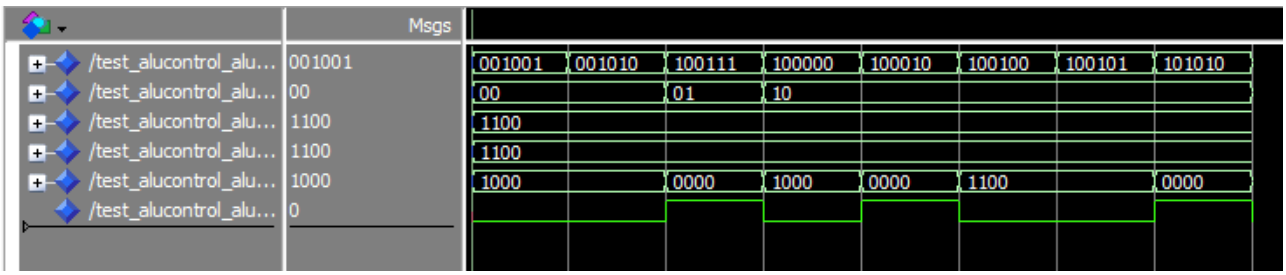
Εικ2.3.1: Κώδικας αρχείου VHDL κυκλώματος “TEST_ALUCONTROL_ALU”.

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  entity TEST_ALUCONTROL_ALU_tb is
4  end TEST_ALUCONTROL_ALU_tb;
5
6  architecture test_b of TEST_ALUCONTROL_ALU_tb is
7  component TEST_ALUCONTROL_ALU port(
8      OP_5to0: IN STD_LOGIC_VECTOR(5 DOWNTO 0);
9      ALU_op: IN STD_LOGIC_VECTOR(1 DOWNTO 0);
10     ALUin1: in std_logic_vector(3 downto 0);
11     ALUin2: in std_logic_vector(3 downto 0);
12     ALUout1: out std_logic_vector(3 downto 0);
13     zero: out std_logic);
14 end component;
15
16 signal OP_5to0_tb:  STD_LOGIC_VECTOR(5 DOWNTO 0);
17 signal ALU_op_tb :  STD_LOGIC_VECTOR(1 DOWNTO 0);
18 signal ALUin1_tb :  std_logic_vector(3 downto 0);
19 signal ALUin2_tb :  std_logic_vector(3 downto 0);
20 signal ALUout1_tb:  std_logic_vector(3 downto 0);
21 signal zero_tb   :  std_logic;
22
23 begin
24 M1: TEST_ALUCONTROL_ALU port map(
25 OP_5to0=>OP_5to0_tb, ALU_op=>ALU_op_tb, ALUin1=>ALUin1_tb,
26 ALUin2=>ALUin2_tb, ALUout1=>ALUout1_tb, zero=>zero_tb);
27 process
28 begin
29     ALUin1_tb<="1100";
30     ALUin2_tb<="1100";
31     ALU_op_tb<="00";
32     OP_5to0_tb<="001001";
33     wait for 50 ps;
34
35     ALU_op_tb<="00";
36     OP_5to0_tb<="001010";
37     wait for 50 ps;
```

```
38
39      ALU_op_tb<="01";
40      OP_5to0_tb<="100111";
41      wait for 50 ps;
42
43      ALU_op_tb<="10";
44      OP_5to0_tb<="100000";
45      wait for 50 ps;
46
47      ALU_op_tb<="10";
48      OP_5to0_tb<="100010";
49      wait for 50 ps;
50
51      ALU_op_tb<="10";
52      OP_5to0_tb<="100100";
53      wait for 50 ps;
54
55      ALU_op_tb<="10";
56      OP_5to0_tb<="100101";
57      wait for 50 ps;
58
59      ALU_op_tb<="10";
60      OP_5to0_tb<="101010";
61      wait for 50 ps;
62  end process;
63  end test_b;
```

Εικ2.3.2: Κώδικας αρχείου VHDL για το κύκλωμα “TEST_ALUCONTROL_ALU”.

2.4



Εικ2.4.1: Παράδειγμα λειτουργίας κυκλώματος “TEST_ALUCONTROL_ALU” μέσω κυματομορφής με τις ζητούμενες τιμές εισόδου.

Από τη παραπάνω κυματομορφή επαληθεύονται οι τιμές που δώσαμε στον πίνακα της άσκησης για τις εξόδους ALUOUT1 και Zero (βλ. Πίν 2.4).

Πίν2.4: Πίνακας τιμών εισόδων-εξόδων κυκλώματος “TEST_ALUCONTROL_ALU”.

ALUop	OP 5to0	ALUin1	ALUin2	ALUOUT1	Zero
00	001001	1100	1100	1000	0
00	001010	1100	1100	1000	0
01	100111	1100	1100	0000	1
10	100000	1100	1100	1000	0
10	100010	1100	1100	0000	1
10	100100	1100	1100	1100	0
10	100101	1100	1100	1100	0
10	101010	1100	1100	0000	1