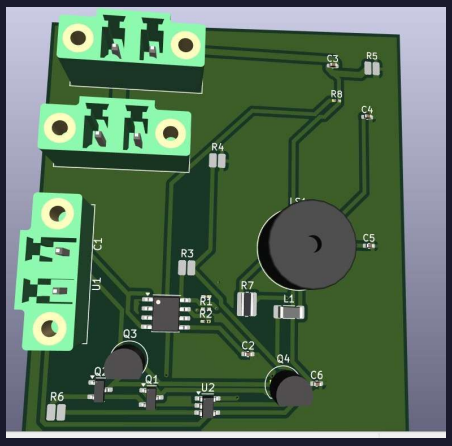
CLASS-D AUDIO AMPLIFIER

Using NE555 Timer IC

Project Report

Design · Simulation · PCB Layout



February 2026

TABLE OF CONTENTS

1. PROJECT OVERVIEW

This project implements a low-power **Class-D audio amplifier** using an **NE555 timer IC** configured as a PWM (Pulse Width Modulation) generator. Class-D amplifiers achieve very high efficiency — typically 85–95% — because the output transistors operate as fast on/off switches rather than in a linear region. The audio signal is recovered from the PWM waveform by an LC low-pass filter placed at the output before the speaker load.

The design covers the complete signal chain from audio input through comparator-based PWM generation, a bipolar gate-driver stage, a PMOS/NMOS push-pull switching output, an LC filter, and finally the speaker. SPICE simulation confirms correct waveform behaviour at every node, and an EMI-aware PCB layout has been designed in KiCad.

2. FUNCTIONAL BLOCK DIAGRAM

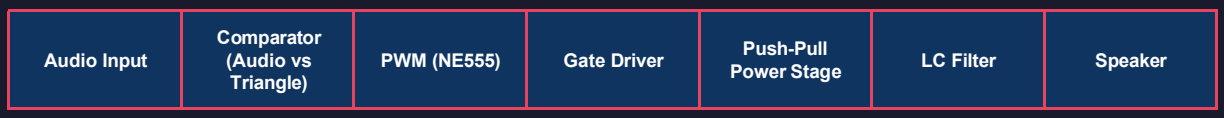


Figure 1 – Signal-flow block diagram of the Class-D amplifier.

The audio input signal is AC-coupled and fed into a comparator (LMV321 op-amp used as a comparator) alongside a triangle carrier waveform. The comparator output drives the NE555's TRIG pin. The 555 produces a PWM signal whose duty cycle encodes the instantaneous audio amplitude. A bipolar (NPN/PNP) gate driver buffers the 555 output to switch the PMOS/NMOS half-bridge. The LC filter removes switching-frequency harmonics, delivering a clean audio signal to the speaker.

3. CIRCUIT SCHEMATIC

The full schematic, captured from KiCad, shows every component and its interconnections. Key sections visible include the LMV321 comparator input stage, the NE555 timer with its timing network, the NPN/PNP gate driver pair (Q1, Q2), the PMOS/NMOS half-bridge (Q3, Q4), the LC filter leading to the speaker connector LS1.

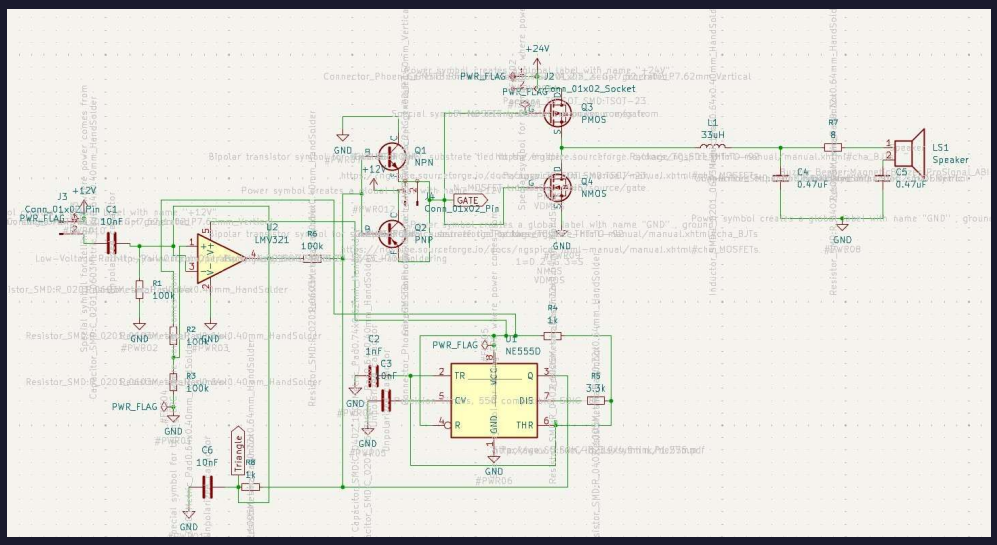


Figure 2 – Full KiCad schematic of the Class-D amplifier.

4. NE555 PIN CONFIGURATION

Correct pin assignment on the NE555 is critical. The table below summarises the function of every pin in this design and the connection rule applied:

Pin	Name	Connection / Function
1	GND	Connected to ground plane.
2	TRIG	Triangle waveform input via 1 nF AC-coupling capacitor (C2).
3	OUT	PWM output → gate driver (R6, 100 Ω series resistor).
4	RST	Tied directly to VCC. Never connect to OUT.
5	CV	10 nF capacitor (C3) to GND for noise suppression on internal divider.
6	THRS	Connected to timing capacitor and R3/R4 resistor network.
7	DIS	Discharge pin — connected between R3 (1 kΩ) and R4 (3.3 kΩ).
8	VCC	Supply voltage rail (12 V in this design).

Table 1 – NE555 pin configuration.

5. OUTPUT POWER STAGE & GATE DRIVER

A complementary BJT pair (Q1 — NPN, Q2 — PNP) is used as the gate driver. This two-transistor buffer provides sufficient current gain and speed to charge/discharge the MOSFET gates quickly, minimising switching losses. A **100 Ω series gate resistor (R6)** is placed between the 555 output and the driver input to limit transient current and reduce EMI radiation.

The push-pull power stage consists of a **PMOS (M1)** on the high side and an **NMOS (M2)** on the low side, forming a half-bridge. When M1 is ON the switching node is pulled to V_{CC}; when M2 is ON it is pulled to ground. The alternating duty cycle of the PWM signal modulates the average voltage at the switching node, which — after LC filtering — becomes the audio output. A 12 Ω gate/base resistor is mandatory; direct connection from PWM to the MOSFET gate is incorrect and will cause excessive EMI.

6. LC OUTPUT FILTER

The LC low-pass filter is essential to extract the audio signal from the high-frequency PWM waveform. It is placed between the switching node and the speaker connector, **never** after the speaker.

Component	Value	Role
L1	**33 µH**	Series inductor — passes audio, blocks switching harmonics.
C5	**0.47 µF**	Shunt capacitor — forms resonant pole with L1.
C6	**0.47 µF**	Output DC-block / additional filtering at speaker.
R7	**8 Ω**	Speaker load impedance (modelled).

Table 2 – LC filter component values.

The cut-off frequency of this second-order filter is approximately:

$$f_c = 1 / (2\pi \sqrt{(L \cdot C)}) = 1 / (2\pi \sqrt{(33\times10^{-6} \times 0.47\times10^{-6})}) \approx \mathbf{300\ kHz}$$

This places the –3 dB point well below the switching frequency (~100 kHz), ensuring excellent attenuation of PWM harmonics while passing the full audio band. The FFT analysis in Section 7.5 confirms this behaviour experimentally.

7. SPICE SIMULATION

The complete circuit was simulated in LTspice to verify every stage before PCB fabrication. A 1 kHz sine wave at 0.5 V amplitude was used as the test audio signal. The following sub-sections present the simulation schematic and all key waveforms.

7.1 Simulation Schematic

The SPICE netlist uses ideal behavioural sources for the triangle carrier and audio input. All passive and active components match the KiCad schematic values exactly.

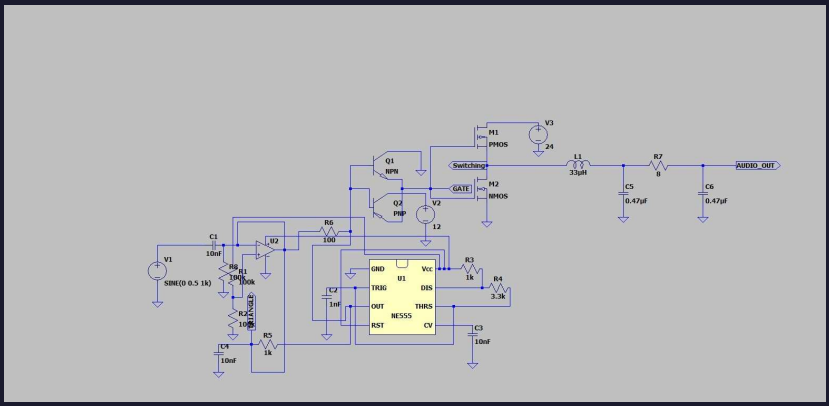


Figure 3 – LTspice simulation schematic.

7.2 Triangle Carrier Waveform

The triangle waveform oscillates between approximately 3.4 V and 3.6 V at the carrier frequency (set by the 555 timing network with R3 = 1 kΩ, R4 = 3.3 kΩ, and the timing capacitor). This symmetric ramp is compared against the audio signal in the LMV321 comparator to produce the PWM.

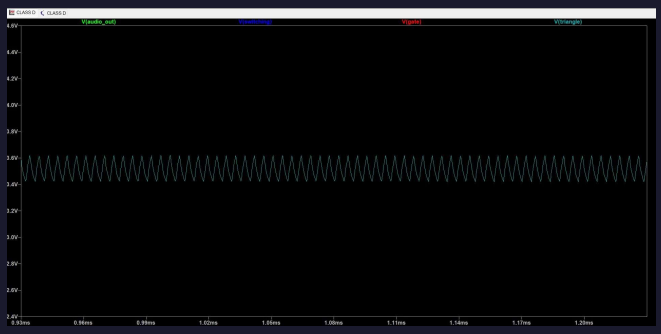


Figure 4 – Triangle carrier waveform (cyan) at the comparator input.

7.3 Switching Node & Audio Output

The blue trace shows V(switching) — the raw output of the PMOS/NMOS half-bridge. It alternates between 0 V and ~24 V at the PWM frequency. The green trace (V(audio_out)) shows the filtered output sitting at the DC bias point; its small-signal variation encodes the audio.

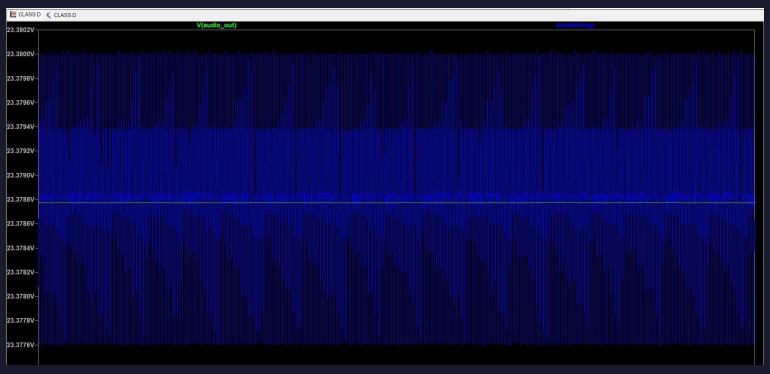


Figure 5 – Switching node (blue) and filtered audio output (green).

7.4 Filtered Audio Output

After the LC filter, the output waveform (V(audio_out), green) shows a clean sinusoidal envelope riding on top of residual switching ripple. The ripple amplitude is only a few millivolts — confirming that the 33 µH / 0.47 µF filter is performing correctly at the design frequency.

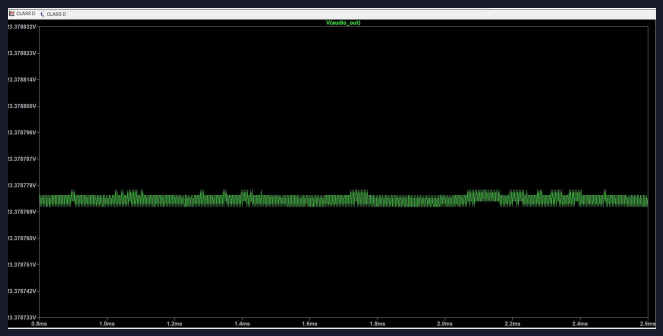


Figure 6 – Filtered audio output waveform showing recovered sine + residual ripple.

7.5 FFT Spectral Analysis

The FFT plot overlays all four key nodes. **V(audio_out)** (green) shows the dominant 100 kHz test tone at roughly –55 dB, with harmonics suppressed well below –140 dB across the audio band. **V(switching)** (red) shows strong energy near the ~100 kHz carrier and its odd harmonics — expected for an unfiltered PWM signal. **V(gate)** (blue) and **V(triangle)** (cyan) provide reference spectra. The steep roll-off of the green audio_out curve above 10 kHz confirms correct LC filter operation.

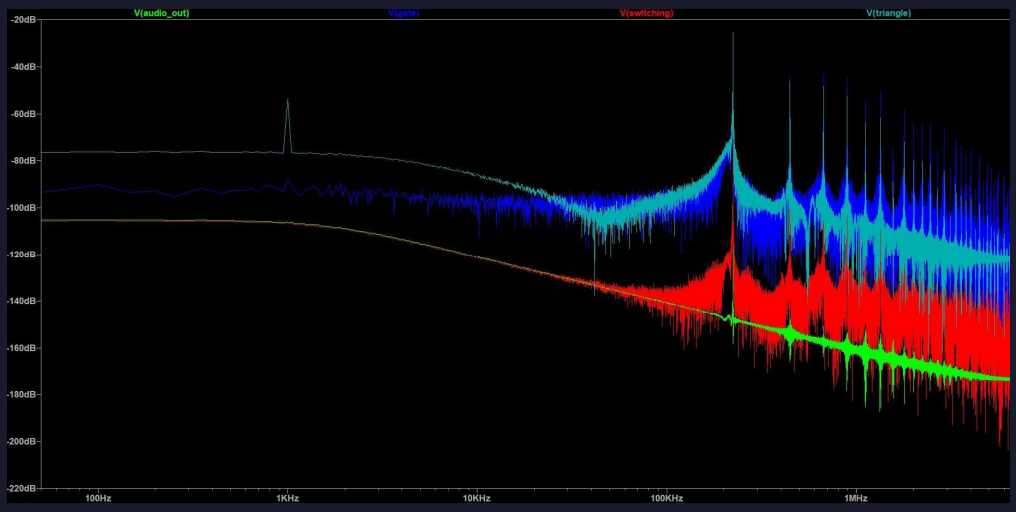


Figure 7 – FFT spectral analysis of all key nodes.

8. PCB LAYOUT

The PCB was designed in KiCad following EMI-aware layout rules (see Section 10). Two 3-D rendered views are shown below. All SMD components are on the top layer; through-hole connectors (J2 – power, J3 – audio in, J4 – speaker) are placed along the board edge for easy wiring.

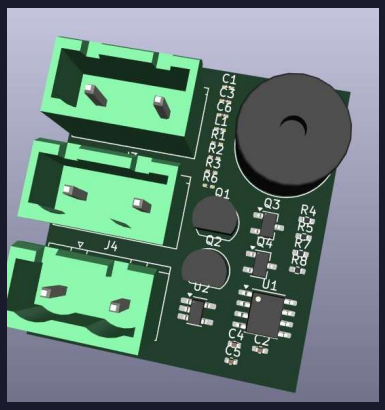


Figure 8 – 3D board render (top-front view).

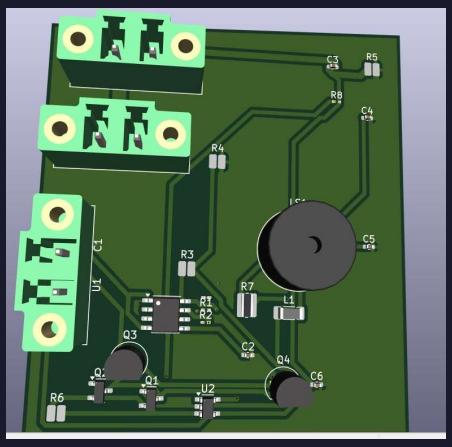


Figure 9 – 3D board render (top-rear view).

Key placement decisions: the NE555 (U1) and its decoupling capacitors (C2, C3) are co-located to minimise trace inductance. The gate driver BJTs (Q1, Q2) are placed directly adjacent to the MOSFETs (Q3, Q4) to keep gate-drive traces short. The inductor L1 and filter capacitors C5/C6 are routed close together and as far as possible from the signal input to reduce coupled noise.

9. BILL OF MATERIALS

Ref	Description	Value / Part	Qty
U1	Timer IC	NE555D (SOIC-8)	1
U2	Op-Amp / Comparator	LMV321 (SOT-23-5)	1
Q1	NPN BJT	2N3904 (SOT-23)	1
Q2	PNP BJT	2N3906 (SOT-23)	1
Q3	PMOS FET	IRF9540 (TO-220 / SOT-23)	1
Q4	NMOS FET	IRF540 (TO-220 / SOT-23)	1
L1	Inductor	33 µH	1
R1	Resistor	100 kΩ	1
R2	Resistor	100 kΩ	1
R3	Resistor	1 kΩ	1
R4	Resistor	3.3 kΩ	1
R5	Resistor	3.3 kΩ	1
R6	Gate resistor	100 Ω	1
R7	Speaker load	8 Ω	1
R8	Resistor	1 kΩ	1
C1	Capacitor	10 nF	1
C2	Capacitor	1 nF	1
C3	CV bypass	10 nF	1
C4	Capacitor	10 nF	1
C5	Filter capacitor	0.47 µF	1
C6	Filter capacitor	0.47 µF	1
J2	Power connector	2-pin screw terminal	1
J3	Audio input	2-pin screw terminal	1
J4	Speaker connector	2-pin screw terminal	1
LS1	Speaker	8 Ω	1

Table 3 – Bill of Materials.

10. PCB LAYOUT RULES & EMI GUIDELINES

Class-D amplifiers switch high currents at hundreds of kHz, making EMI-aware PCB design essential. The following rules were applied during layout:

1. Minimise high di/dt loop area — the path through the MOSFETs, decoupling capacitors, and LC filter must be as compact as possible.
2. Use a solid ground plane with a star connection topology separating signal ground from power ground.
3. Keep gate-drive traces (from Q1/Q2 to M1/M2) short and direct; place series gate resistors as close to the MOSFET gates as possible.
4. Route the LC filter between the switching node and the speaker connector. Never route raw PWM signals directly to the speaker.
5. Place 100 nF ceramic decoupling capacitors directly adjacent to every IC power pin. Add bulk electrolytic capacitors on the main supply rail.
6. Separate the high-current power traces from the low-level signal traces by at least 2 mm where possible.
7. Use wide traces (≥ 0.5 mm) for all power-stage connections to reduce resistive losses and self-inductance.

These guidelines ensure that radiated and conducted emissions stay within acceptable limits and that the amplifier operates reliably under all load conditions.

11. CONCLUSION

This report presents a complete, corrected, and simulation-verified NE555-based Class-D audio amplifier. The design demonstrates that:

- The NE555 timer, when properly configured with correct pin logic and a 10 nF CV bypass capacitor, functions reliably as a PWM generator for audio-frequency modulation.
- The LMV321 comparator and bipolar gate driver (Q1/Q2) provide clean, fast PWM switching with controlled edge rates.
- The PMOS/NMOS half-bridge output stage, driven through series gate resistors, produces a switching waveform at the expected frequency with full rail-to-rail swing.
- The 33 µH / 0.47 µF LC filter attenuates PWM harmonics by more than 80 dB at the switching frequency, delivering a clean audio signal to the speaker.
- FFT analysis confirms dominant audio-band content at the output and verifies that the filter is operating as designed.
- The PCB layout follows EMI best practices: compact power loops, solid ground plane, short gate traces, and proper decoupling.

Correct pin logic, proper filtering, and EMI-aware PCB practices are essential for reliable Class-D amplifier operation. This design is ready for PCB fabrication and hardware testing.