Lab 2

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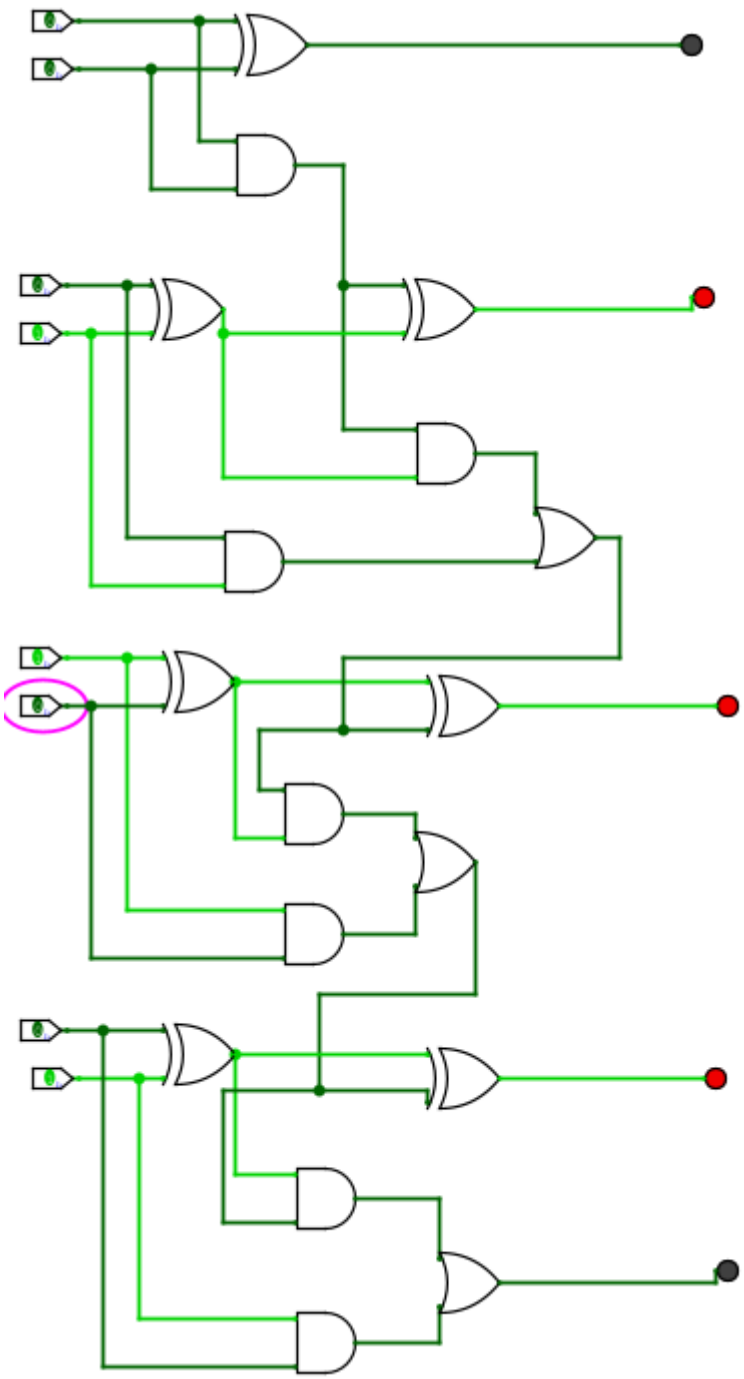
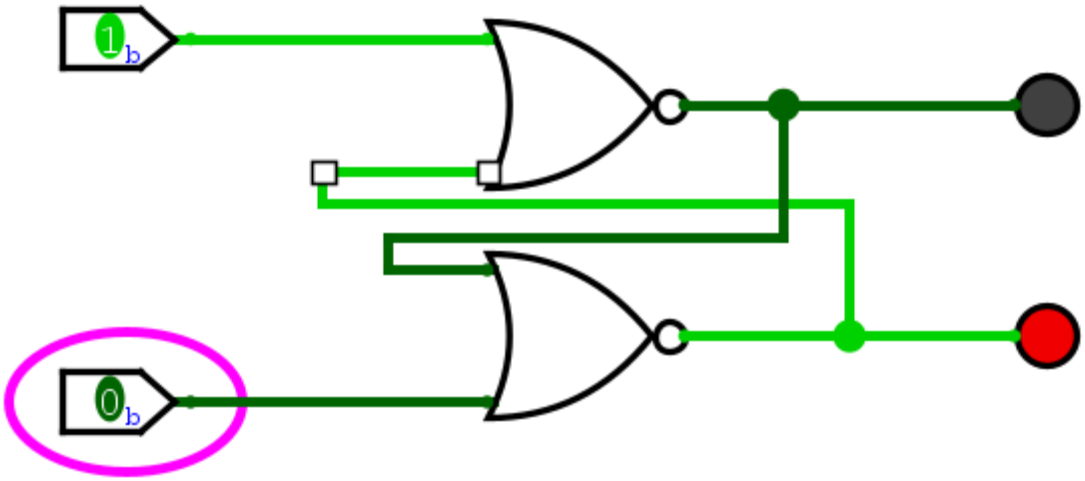
Exercise 1:

Input A	Input B	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000
0101	0100	1001
0101	0101	1010
0101	0110	1011
0101	0111	1100
0101	1000	1101
0101	1001	1110
0101	1010	1111
0101	1011	10000
0101	1100	10001
0101	1101	10010
0101	1110	10011
0101	1111	10100



Exercise 2:

Set	Reset	Q	Q’
1	0	0	1
1	1	0	0
0	1	1	0
1	1	0	0



11. Describe in a sentence, the behaviour of the circuit when one of the inputs is 1 (but not both) and why this is useful for digital circuit design.

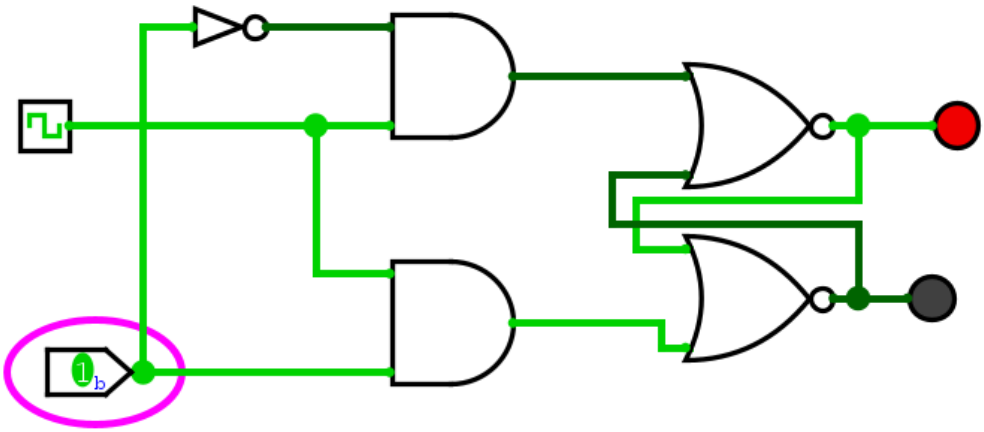
- If one of the inputs is 1 so the other output will be 1.

12. What do you notice about the two times you set both inputs to 1. Briefly explain what is happening here and why this is an issue for digital circuit design ?

- Both times the outputs are 0. Because all the 1s input will go through 2 NOR gates and it will turn into 0.

Exercise 3:

Clock	Pin	Q	Q’
0	0	0	1
0	1	0	1
1	1	1	0
1	0	0	1



15. Briefly explain the behavior of a D flip flop and how it is useful for digital circuit design.

It normally used as part of memory storage parts and data processors. Because of its versatility, it is used for delay in timing circuit.

16. What is the role of the clock? how does it impact the changing of state of Q and Q'?

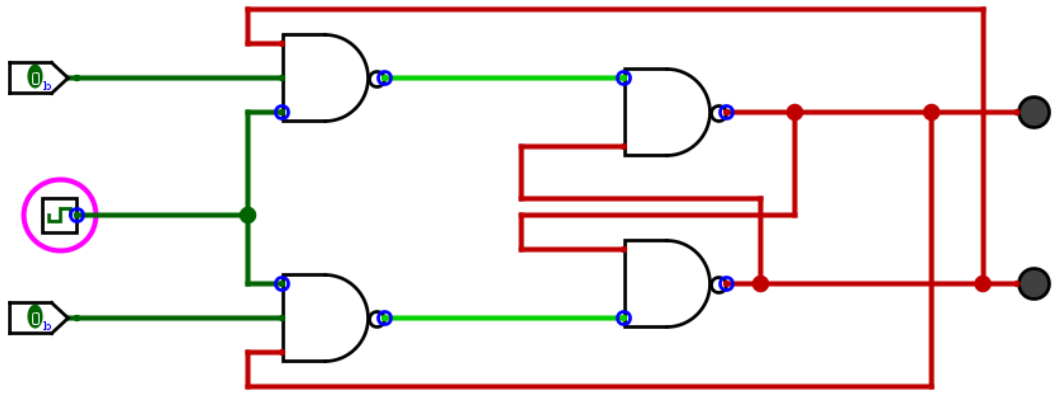
The role of the clock in D Flip Flop is keep the output stable even the input is low

17. Why is it generally preferred over the R-S flip flop?

D flip flop is simplicity, and both of the input and output can be identified easily.

Exercise 4:

J	K	Q (when clocked)	Q'(when clocked)
0	0	0	0
1	0	1	0
0	1	0	1
1	1	0	0



20. How can a J-K Flip Flop be made to behave like a D Flip Flop ?

The input pins of J-K flip flop can be drive with the D input and its negation

21. How can a J-K Flop Flop be made to behave like a toggle (T Flip Flop) ?

The J-K flip flop inputs (J input and K input) will need to connect together and both value of it need to set to 1.