



# EE457: Digital IC Design

## Spring 2024

### Final Report Cover Sheet

Submit on Blackboard by 11PM, 5/19/2024

Final Presentation on Monday 5/20/24 at 10:30AM (for section D) and 3:30PM (for section F).

**PROJECT TITLE:** 16 to 1 Multiplexer (TG Circuit and Static Circuit)

Group Name: Mux It

Student Names: Paniz Peiravani and Zackery Akira Wallach

Put Check marks for completion in this column	Topics ***DO NOT alter the order and shape of this table***	GRADES
Required	Section1: Executive Summary (1/2 page to 1 page)	
✓	Section 2: Introduction and Background	/5
✓	Section 3: Electric Circuit Schematics (only transistors)	/10
✓	Section 4: Detailed Electric Layouts ( <i>The entire layout should be on single page landscape form.</i> ) Provide detailed layouts of subcircuits with simulations.	/30
✓	Section 5: LTSPICE code and parasitic extractions with calculation analysis. Put only samples of code.	/15
✓	Section 6: IRSIM Logic Simulations and Measurements for Layout and Schematic ( <u>must provide comparisons between the two using tables</u> )	/10
✓	Section 7: Measurements in LTSPICE for delays for Layout and Schematic ( <u>must provide comparisons between the two using tables</u> )	/15
✓	Section 8: Measurements of <u>power, delay, chip area, timing, number of transistors</u> for the layout. (If you are using TG, static or dynamic CMOS, compare here using tables.)	/10
Required	Section 9: Conclusions and References	
Required	Presentation (Monday 5/20/24)	..... .... /5
	Late Report (-5pts per day until day 5/20/24)	
Yes	Does the project work? (-20pts for not functioning design) Y/N	
	<b>TOTAL</b>	<b>/100</b>

**Five points will be deducted for not following the directions.**

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## Section1: Executive Summary

The purpose of our final project was to implement a 16-to-1 Multiplexer using Electric software. For this project, we had to choose between two different circuit designs: Transmission Gate circuit, Static circuit, or Dynamix circuit. We implemented Transmission Gates and Static circuits using Electric software. The purpose of having different designs was to analyze and find the differences and similarities between them. We also used IRSIM and LTSpice to obtain the output waveform and verify our design with the 16-to-1 Mux truth table. Additionally, we compared the results from the TG and static circuits.

## Section 2: Introduction and Background

Multiplexing is the process of combining one or more signals and transmitting on a single channel. *Figure 1*, on the right, shows the block diagram of a multiplexer consisting with  $n$  input lines,  $m$  selection lines, and one output line. If there are  $m$  selection lines, there can be  $2^m$  possible input lines. In other words, if the number of input lines equals  $2^m$  (considering  $2^m = n$ ), then  $m$  selection lines are needed to choose one of the  $n$  input lines. This type of multiplexer is called a  $2^n \times 1$  multiplexer or a  $2^n$ -to-1 multiplexer.

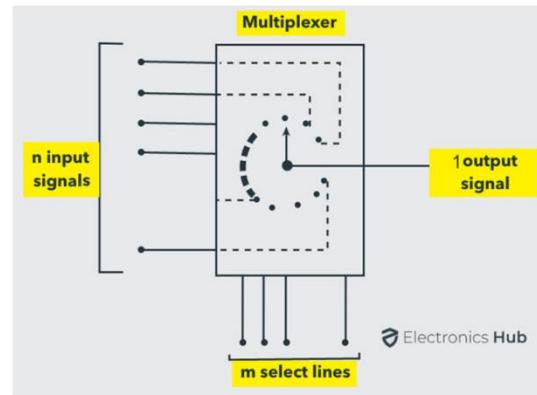


Figure 1 – General Multiplexer Diagram (Teja, 2024)

Generally, the number of data inputs to a multiplexer is a power of two such as 2, 4, 8, 16, etc. Some of the most frequently used multiplexers include 2-to-1, 4-to-1, 8-to-1, and 16-to-1 multiplexers. For our project, we are designing a 16-to-1 multiplexer.

As you can see in *Figure 2* on the right, 16-to-1 Multiplexer has sixteen data inputs  $D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_9, D_{10}, D_{11}, D_{12}, D_{13}, D_{14}$ , and  $D_{15}$ , four selection lines  $S_0, S_1, S_2$ , and  $S_3$ , and one output  $Y$ .

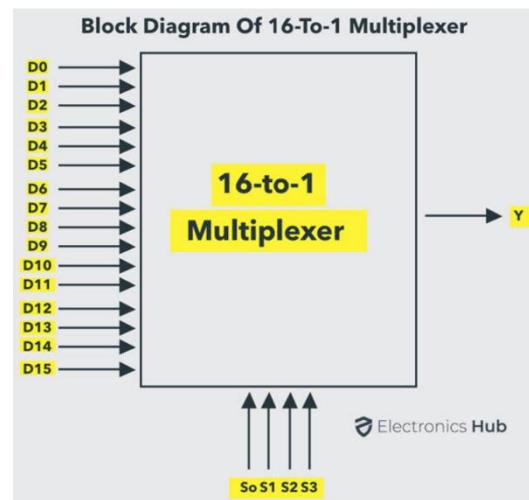
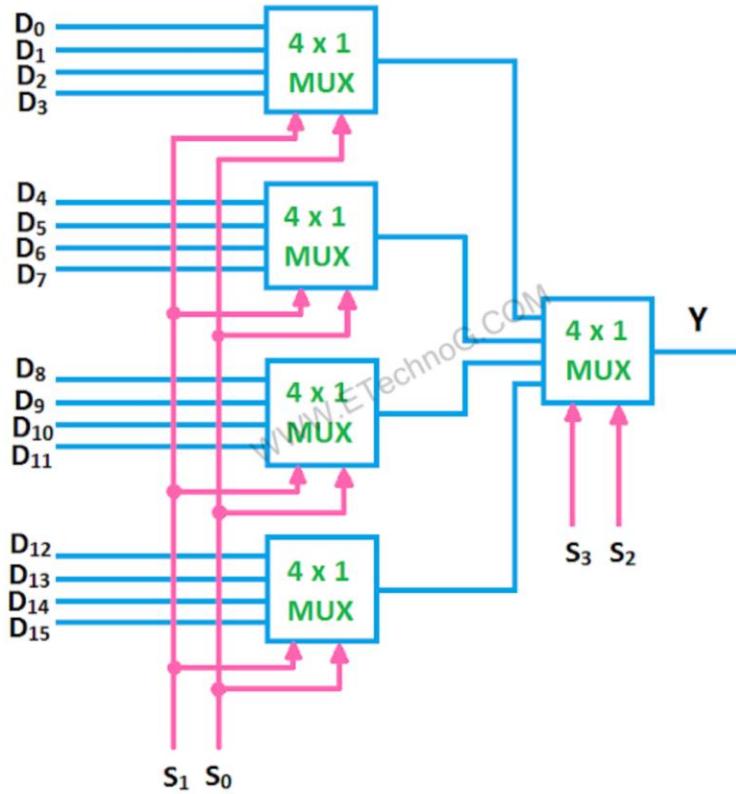


Figure 2 – 16-to-1 Multiplexer Diagram (Teja, 2024)

As you can see in *Figure 3*, to design a 16-to-1 multiplexer, we cascaded 4-to-1 multiplexer 5 times. Each 4-to-1 Mux has 4 inputs and one output which will be the input to our last 4-to-1 Mux. Lastly, our final 4-to-1 Mux has four inputs which are from our four 4-to-1 Mux and the last final indicates our output Y.



**16 to 1 Multiplexer**

*Figure 3 – 16-to-1 Mux (Nithin, 2022)*

Since we were cascading five 4-to-1 Mux, we needed to know the truth table for the 4-to-1 Mux to make sure our design worked properly. Below on *Table 1*, you can see the truth table for 4-to-1 Mux.

*Table 1 – 4-to-1 Mux Truth Table*

$S_0$	$S_1$	$D_0$	$D_1$	$D_2$	$D_3$	Y
0	0	0	x	x	x	0
0	0	1	x	x	x	1
0	1	x	0	x	x	0
0	1	x	1	x	x	1
1	0	x	x	0	x	0
1	0	x	x	1	x	1
1	1	x	x	x	0	0
1	1	x	x	x	1	1

Once we designed our 16-to-1 Mux, we compared our waveform from IRSIM and LTSpice to the 16-to-1 Mux truth table to make sure our design worked properly. Below on *Table 2*, you can see the 16-to-1 Mux truth table.

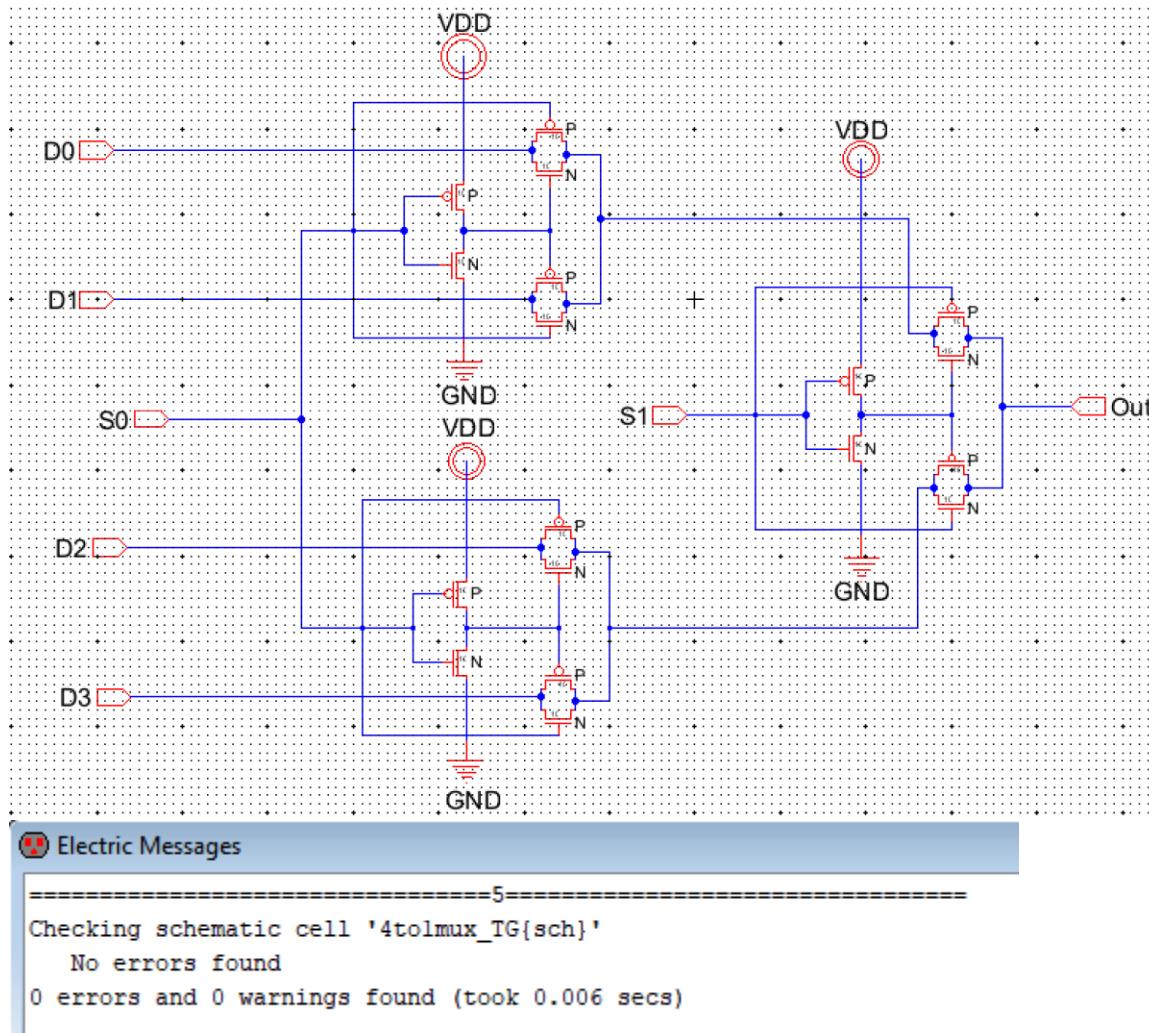
*Table 2 – 16-to-1 Mux Truth Table*

$S_0$	$S_1$	$S_2$	$S_3$	Y
0	0	0	0	$D_0$
0	0	0	1	$D_1$
0	0	1	0	$D_2$
0	0	1	1	$D_3$
0	1	0	0	$D_4$
0	1	0	1	$D_5$
0	1	1	0	$D_6$
0	1	1	1	$D_7$
1	0	0	0	$D_8$
1	0	0	1	$D_9$
1	0	1	0	$D_{10}$
1	0	1	1	$D_{11}$
1	1	0	0	$D_{12}$
1	1	0	1	$D_{13}$
1	1	1	0	$D_{14}$
1	1	1	1	$D_{15}$

After implementing our design, we find the rise time, fall time, propagation delay, power, and chip area for both layout and schematic for our 16-to-1 TG and 16-to-1 Static which you can see the details in other sections.

## Section 3: Electric Circuit Schematics

To design our 16-to-1 Mux we first needed to design 4-to-1 mux. Below you can see designs for 4-to-1 for TG and Static circuit. *Figure 4* shows the TG circuit for 4-to-1 Mux with DRC check.



*Figure 4 – 4-to-1 Mux – Transmission Gate Schematic with DRC check*

Figure 5 shows the Static circuit for 4-to-1 Mux with DRC check.

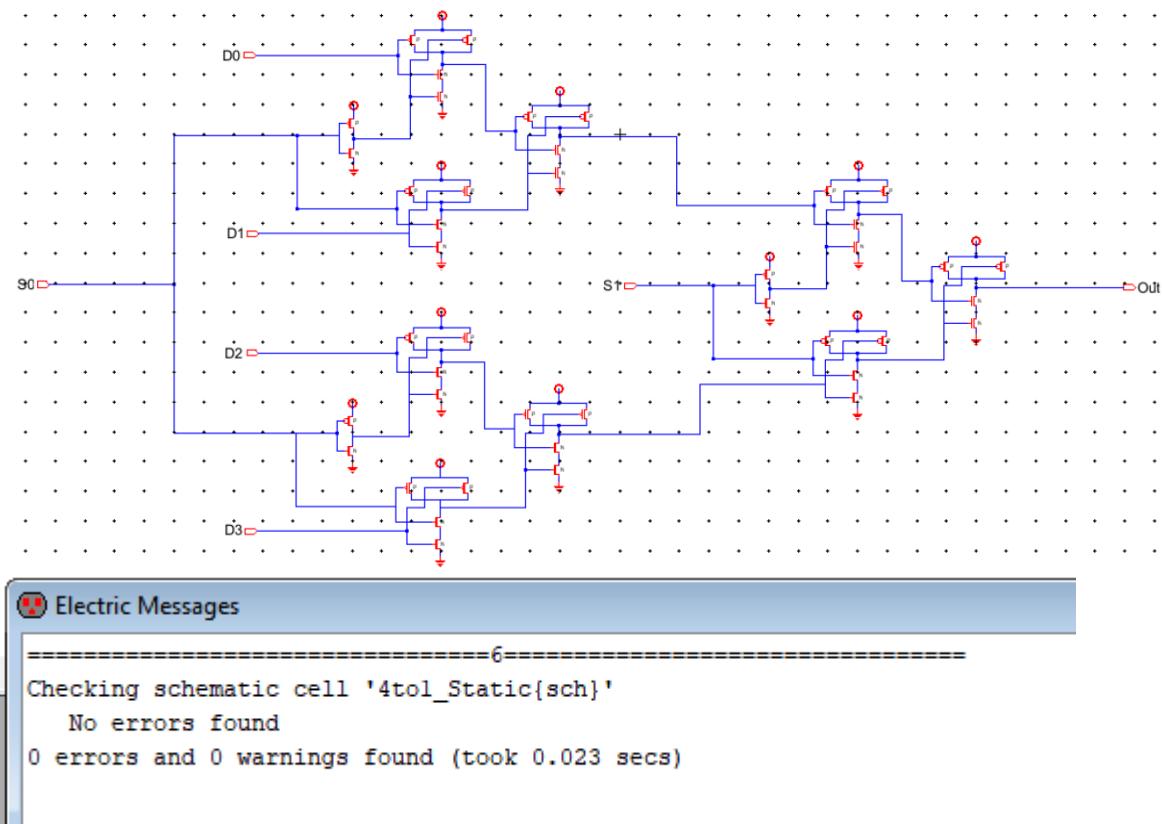


Figure 5 – 4-to-1 Mux – Static Circuit Schematic with DRC check

Once we had our 4-to-1 Mux and checked the waveform and saw that they worked properly, we moved forward to design our 16-to-1 Mux.

In *Figure 6* you can see our design for the TG circuit for 16-to-1 Mux with DRC check.

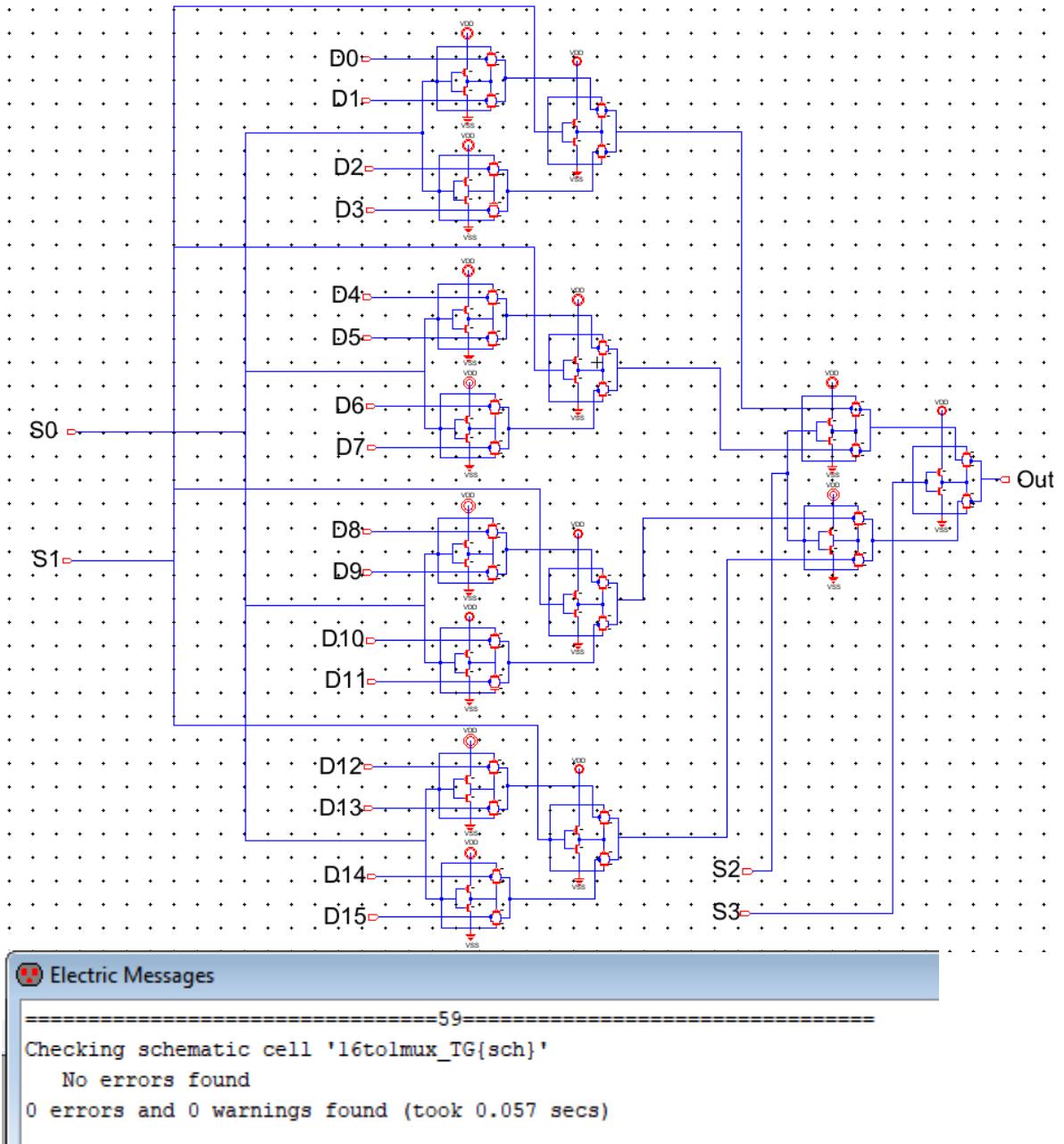


Figure 6– 16-to-1 Mux – TG Circuit Schematic with DRC check

In *Figure 7* you can see our design for Static CMOS circuit for 16-to-1 Mux with DRC.

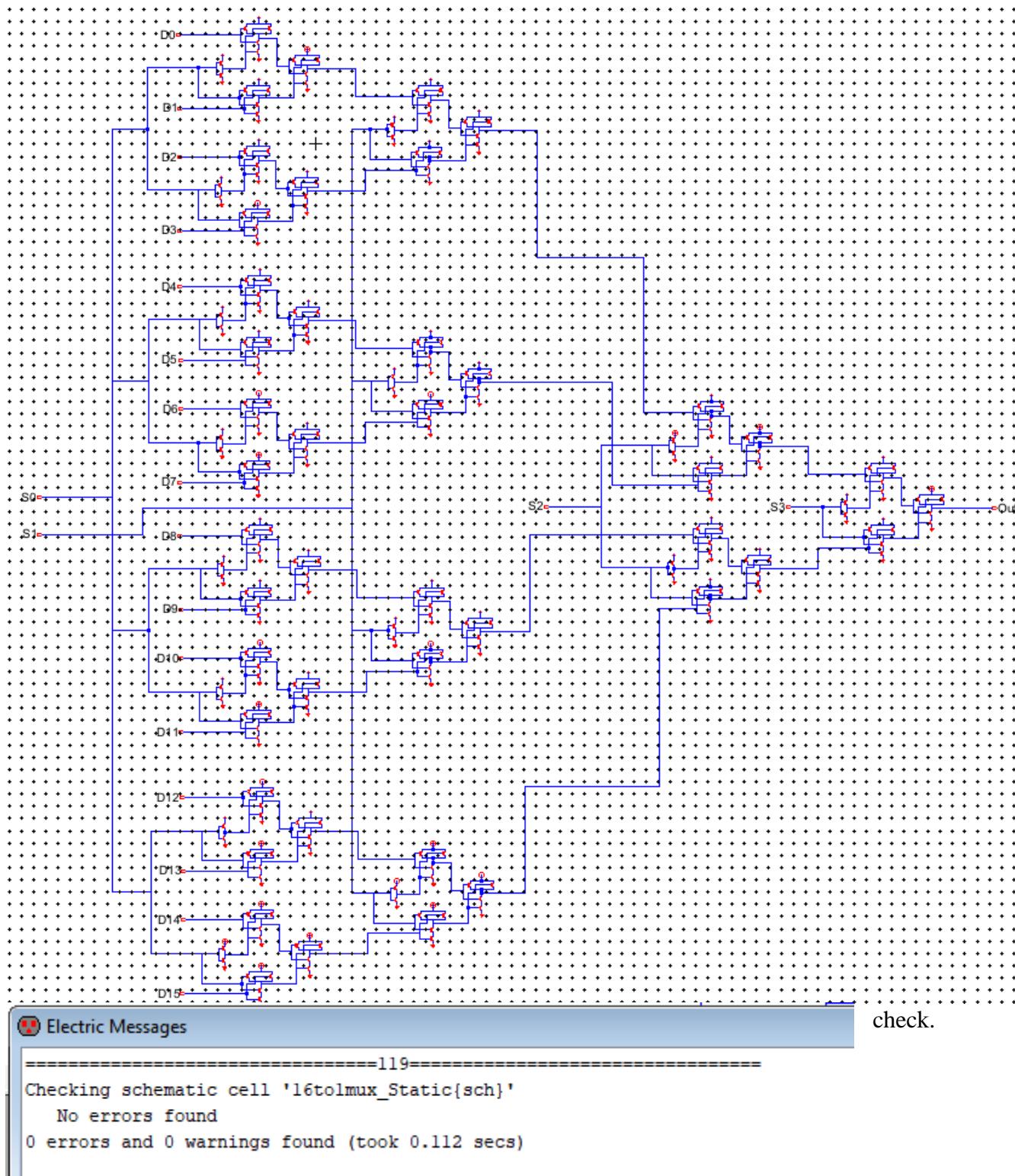


Figure 7– 16-to-1 Mux – Static CMOS Circuit Schematic with DRC check

## Section 4: Detailed Electric Layouts

To design our 16-to-1 Mux, first needed to design 4-to-1 mux. Below you can see our designs for 4-to-1 for TG and Static circuit.

Figure 8 shows the TG circuit for 4-to-1 Mux.

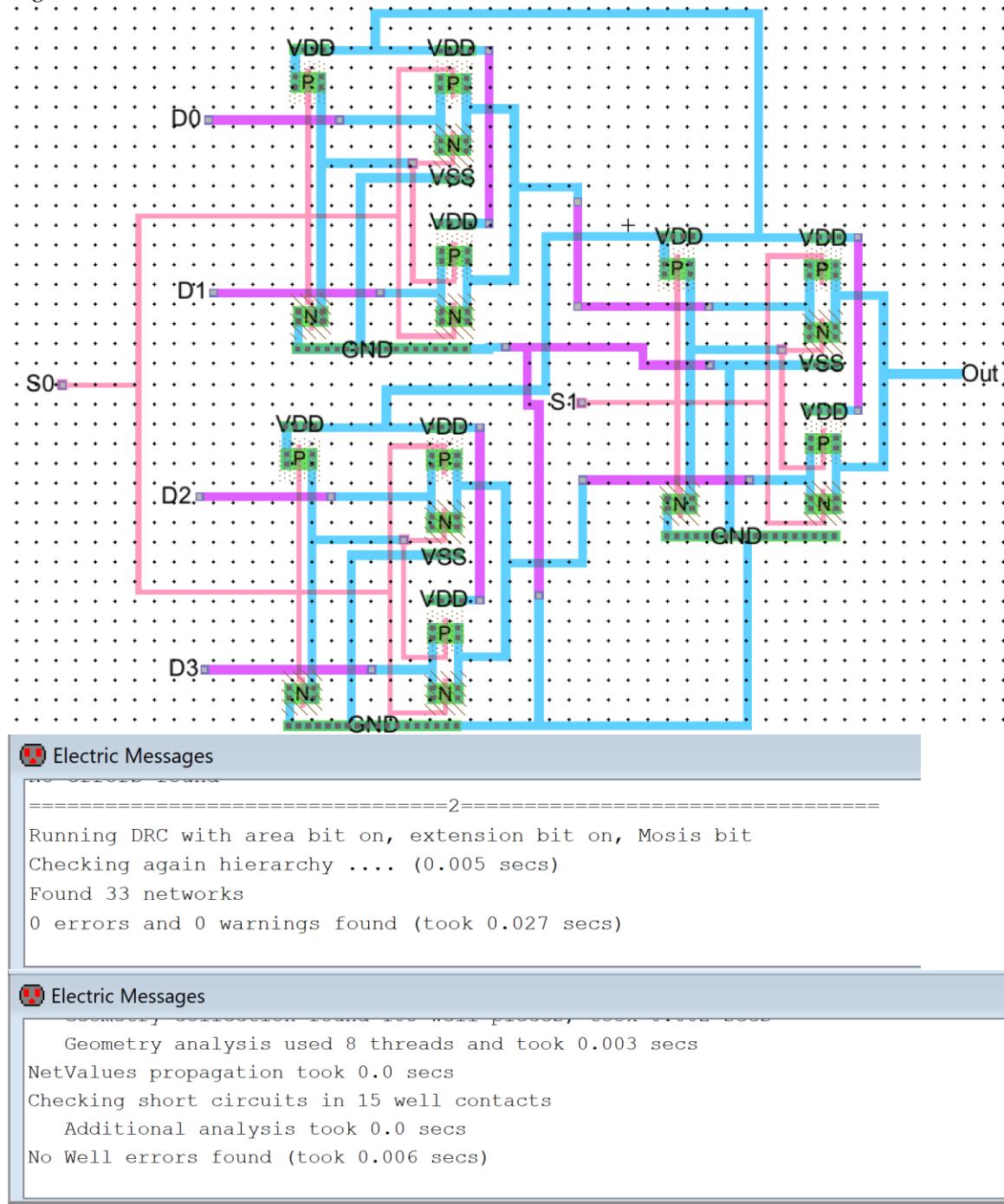


Figure 8 – 4-to-1 Mux – Transmission Gate Layout with DRC and Well Check

Figure 9 shows the Static circuit for 4-to-1 Mux with DRC and Well Check.

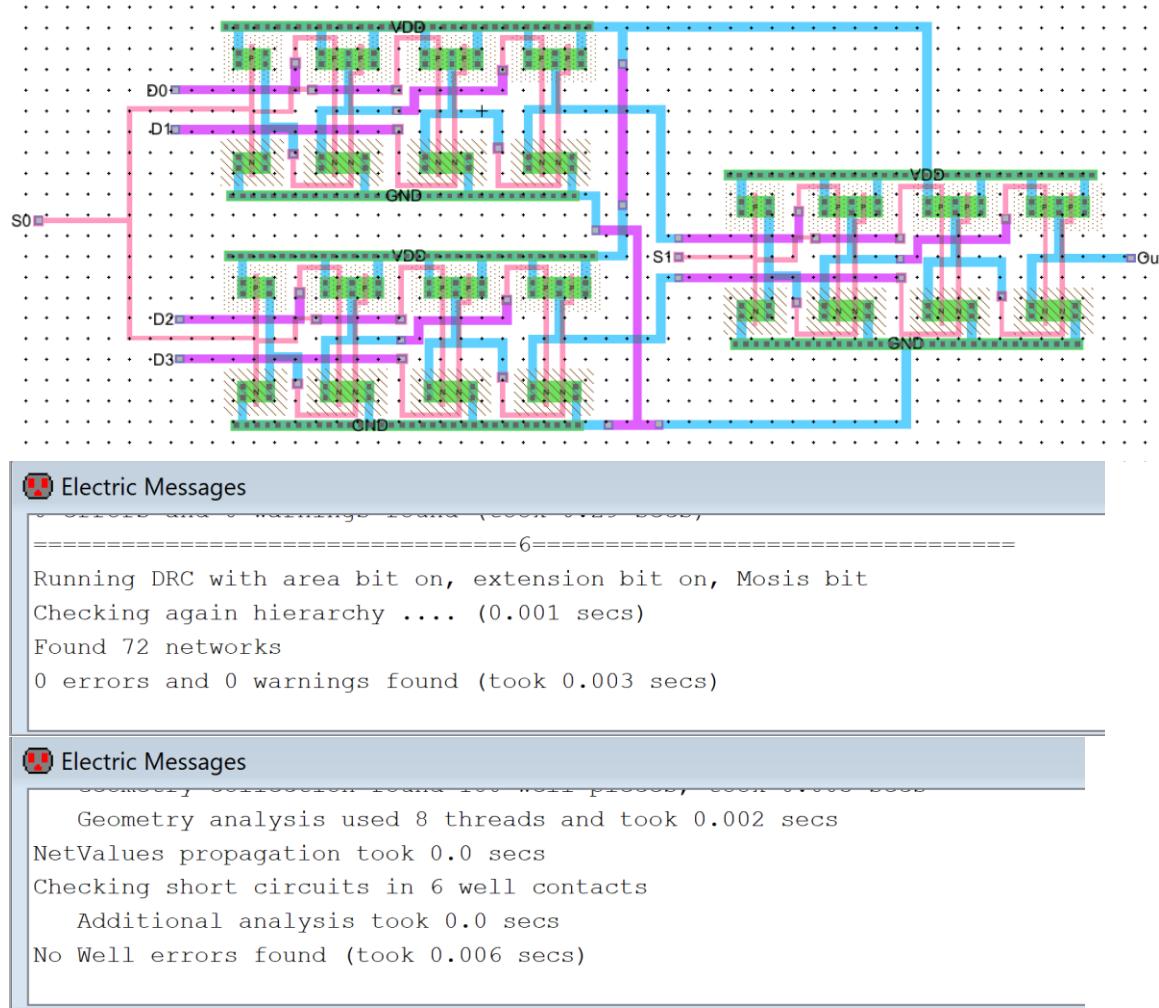


Figure 9 – 4-to-1 Mux – Static Circuit Layout with DRC and Well Check

Once we had our 4-to-1 Mux and checked the waveform and saw that they worked properly, we moved forward to design our 16-to-1 Mux.

Figure 10 shows the TG circuit for 16-to-1 Mux with DRC and Well Check.

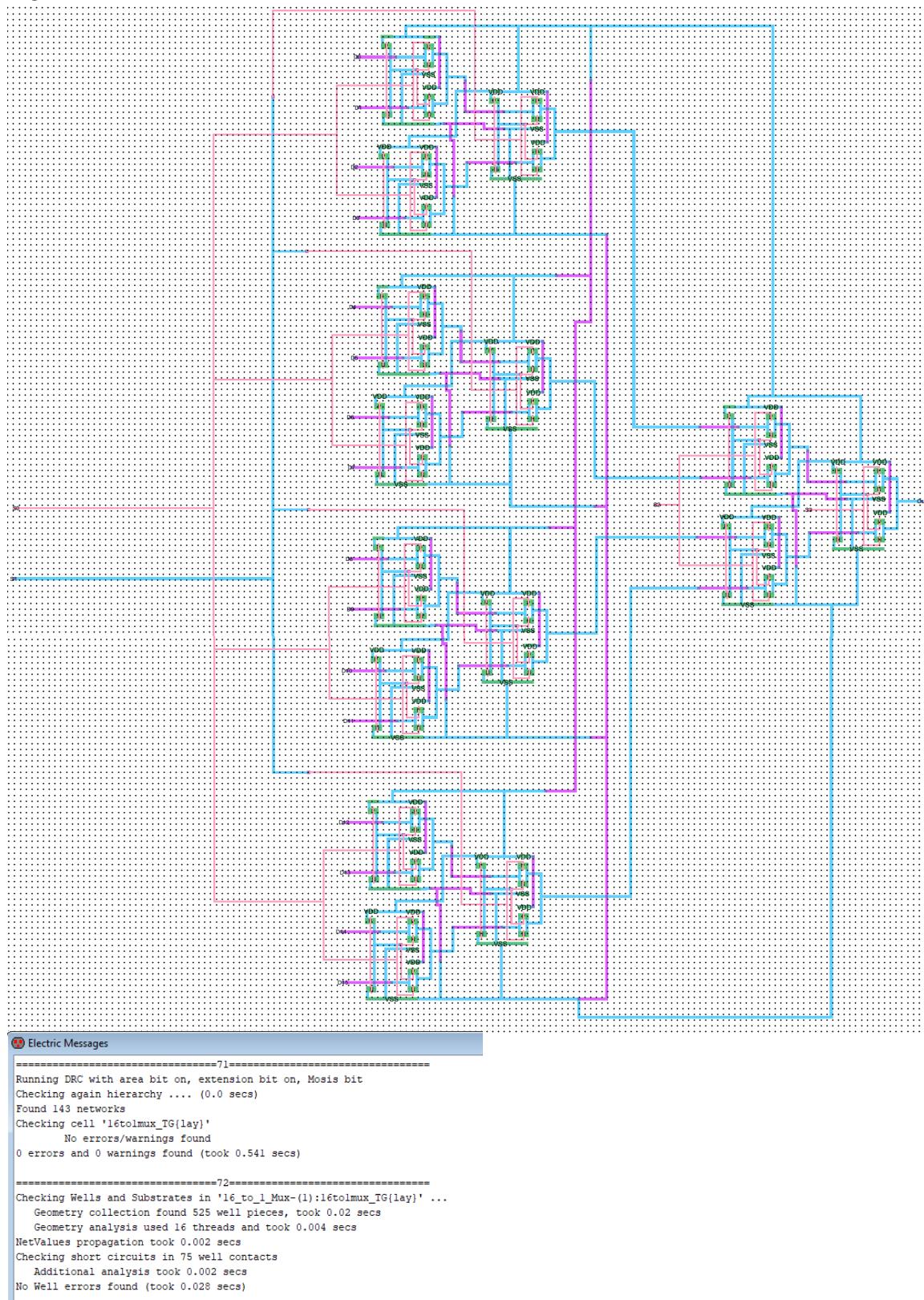
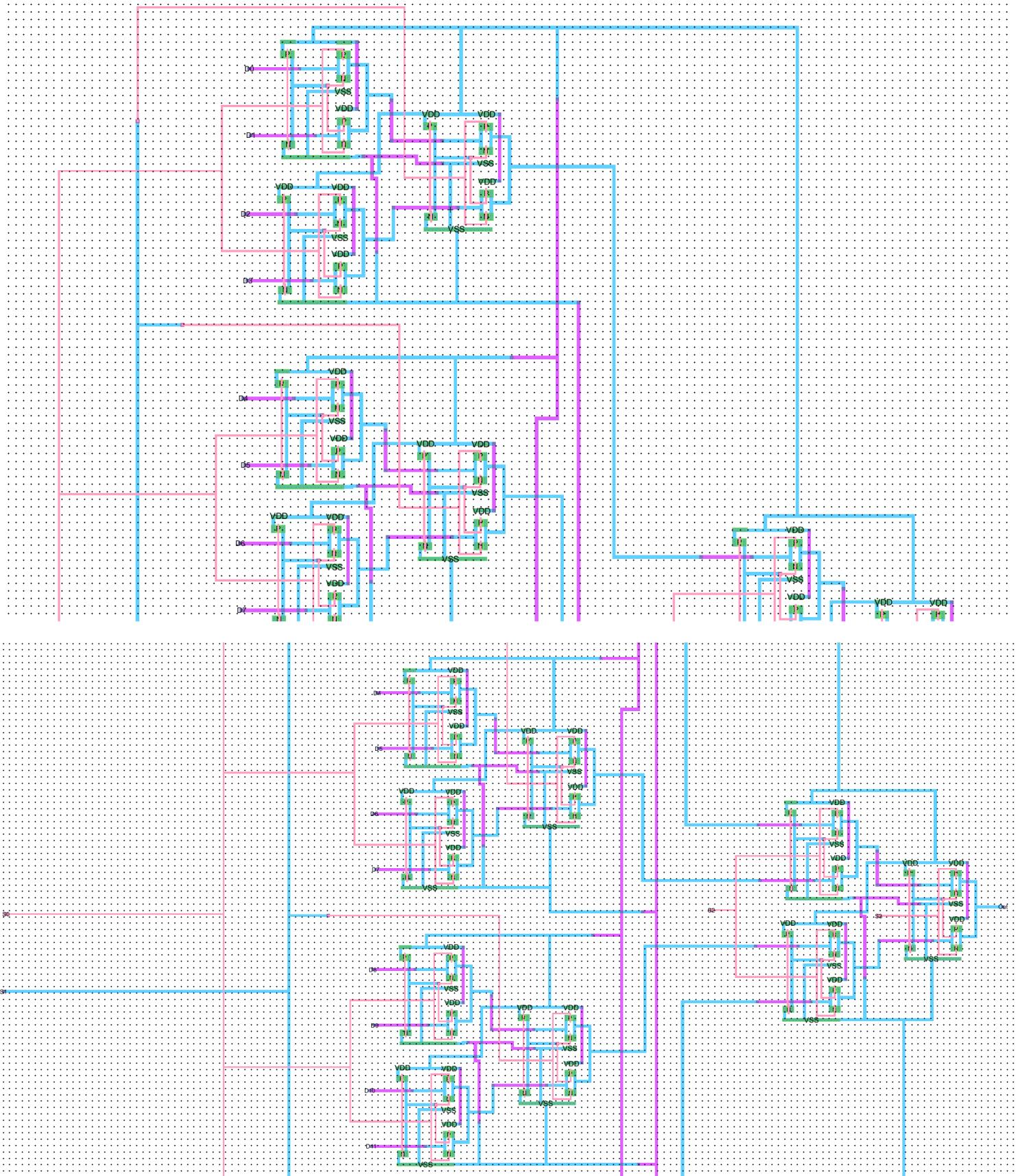


Figure 10 – 16-to-1 Mux – Transmission Gate Layout with DRC check

We also added a closer picture for our design for better visibility. Below you can see the Zoomed In of our 16-to-1 Mux TG.



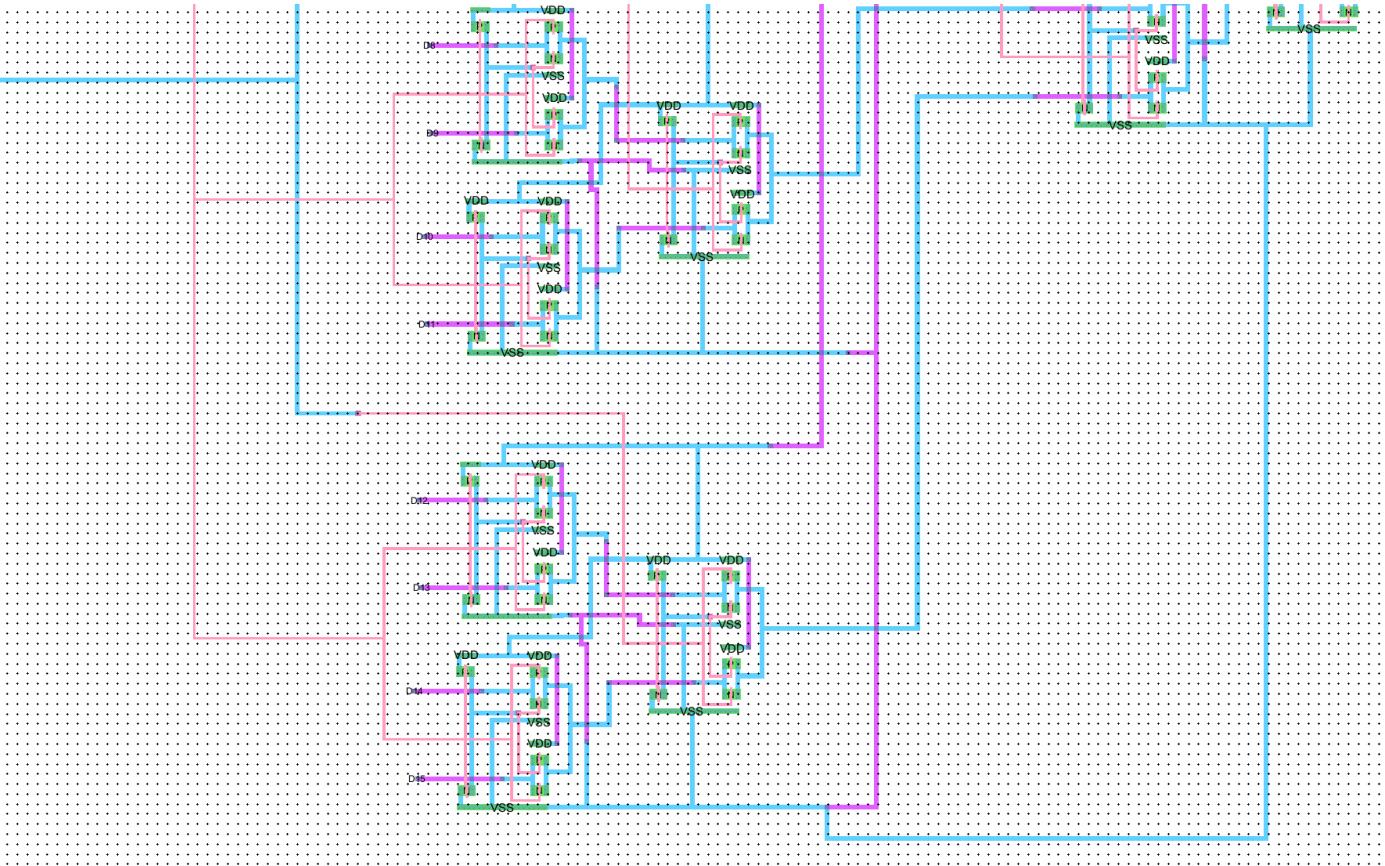


Figure 11 shows the Static CMOS circuit for 16-to-1 Mux with DRC and Well Check.

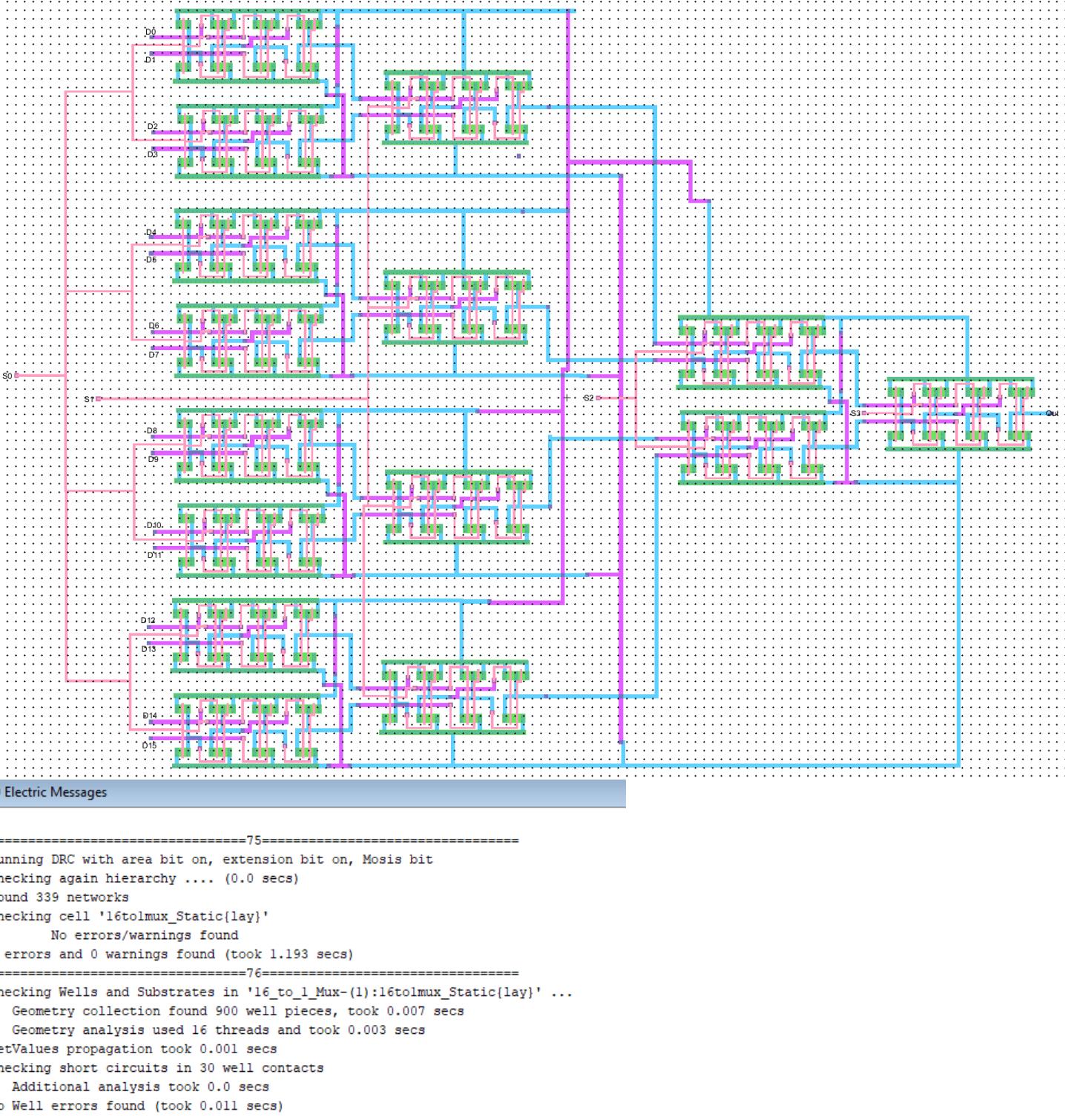
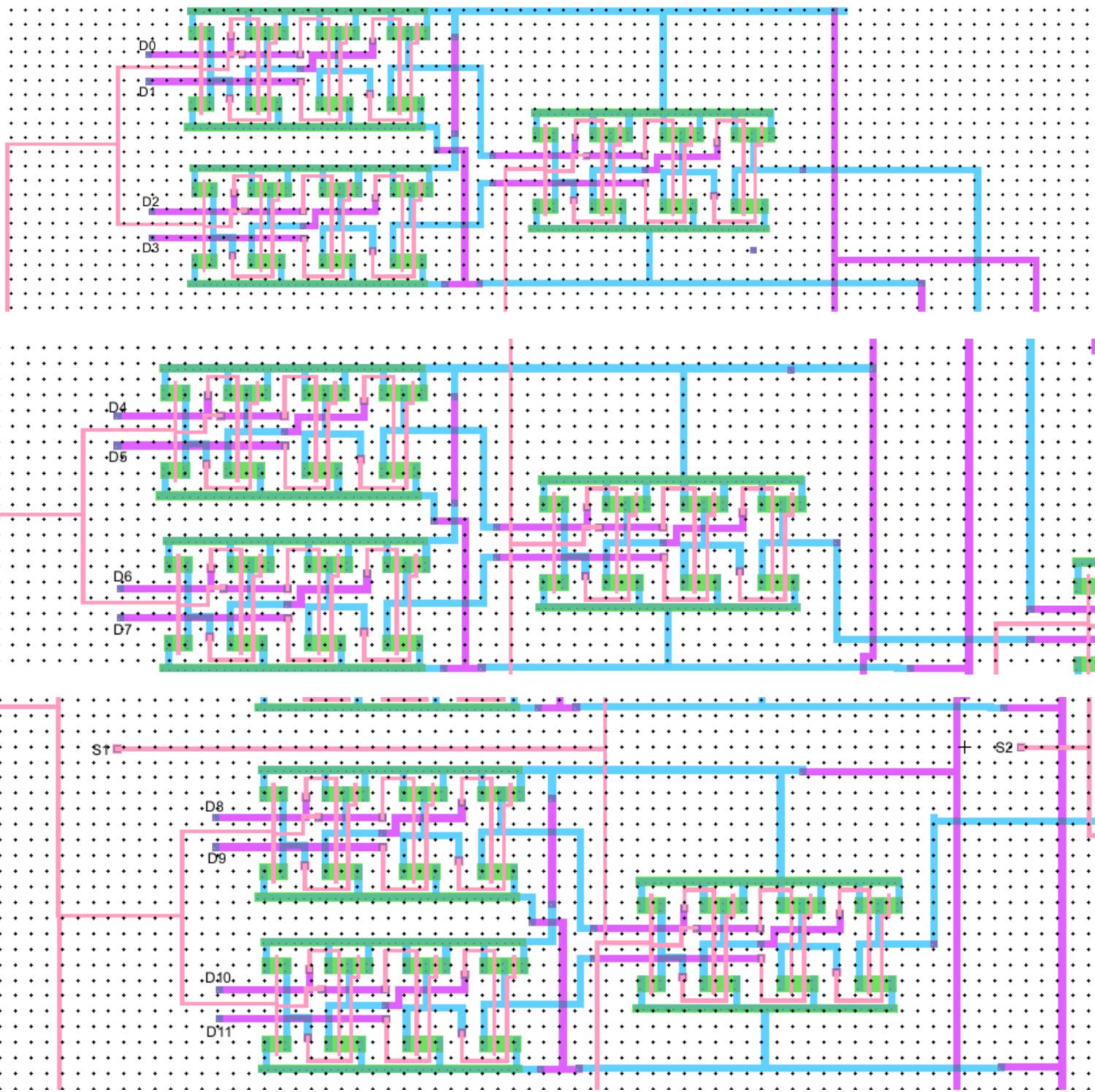
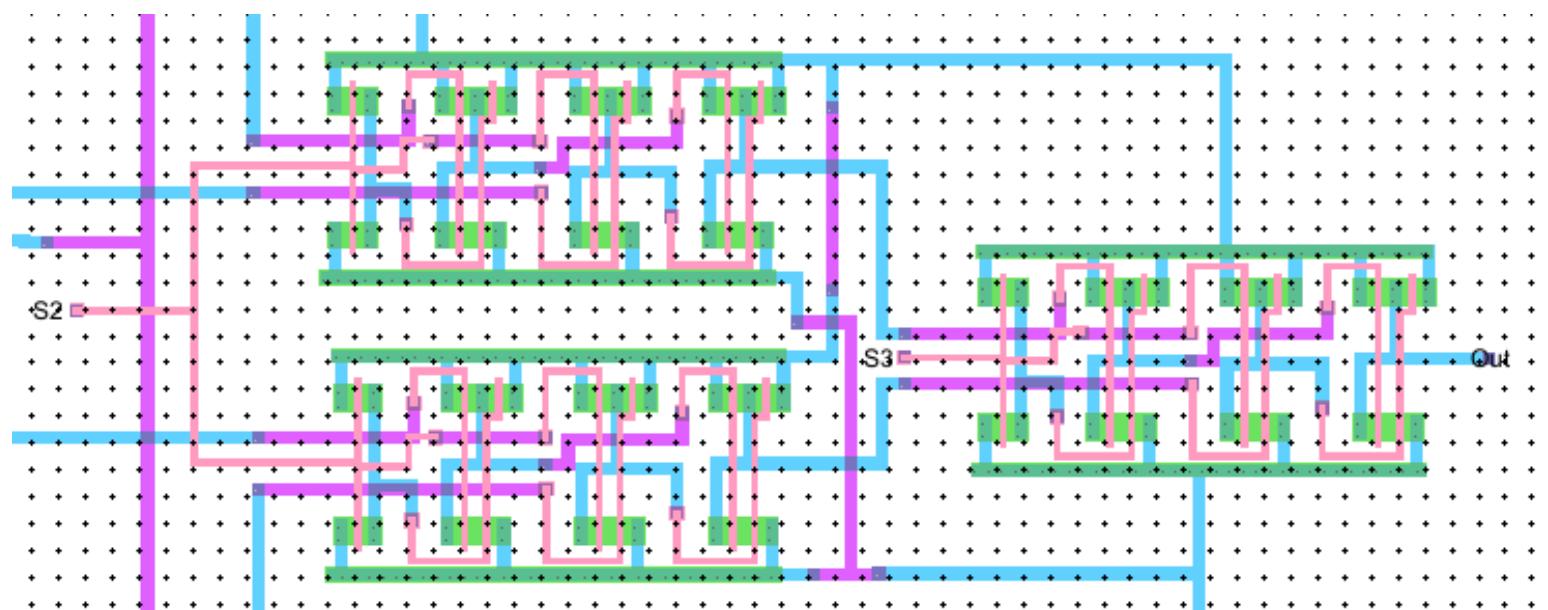
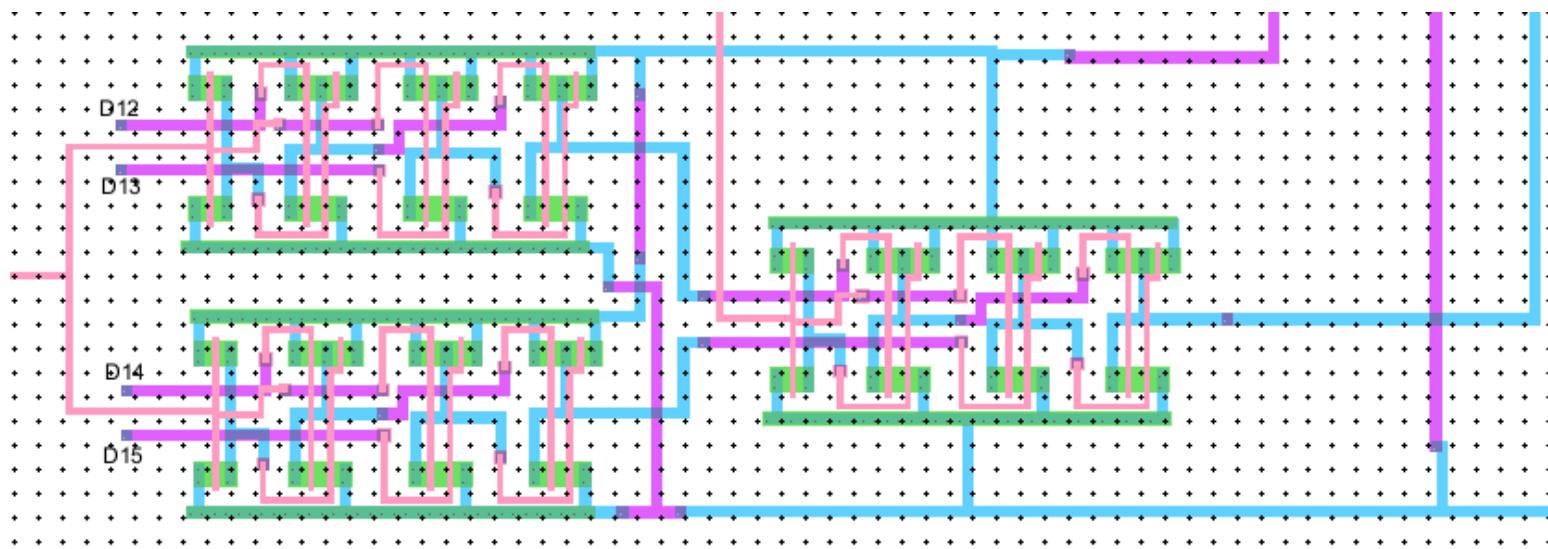


Figure 11 – 16-to-1 Mux – Static CMOS Layout with DRC check

We also added a closer pictures for our design for better visibility. Below you can see the Zoomed In of our 16-to-1 Mux Static Circuit.





## Section 5: LTSPICE code and parasitic extractions with calculation analysis.

Before we checked our 16-to-1 Mux LTSpice waveform, we checked our 4-to-1 to make sure our 4-to-1 works properly as well.

Below you can see our spice code for 4-to-1 Mux for the Transmission Gate schematic and layout. Figure 12 shows the spice code for our schematic and Figure 14 shows the spice code for our layout.

Below you can see our spice code for the TG 4-to-1 Mux for schematic.

```
* Spice Code nodes in cell cell '4to1mux_TG{sch}'
VDD VDD 0 DC 3.3
UVSS UVSS 0 DC 0
UD0 D0 0 PULSE(0 3.3 0n 5n 5n 50n 800n)
UD1 D1 0 PULSE(0 3.3 200n 5n 5n 50n 800n)
UD2 D2 0 PULSE(0 3.3 400n 5n 5n 50n 800n)
UD3 D3 0 PULSE(0 3.3 600n 5n 5n 50n 800n)
US0 S0 0 PULSE(3.3 0 0n 5n 5n 200n 400n)
US1 S1 0 PULSE(3.3 0 0n 5n 5n 400n 800n)
.tran 0 1600n
.include C:\Users\paniw\Downloads\EE457\Technology_MODEL.txt
.END
```

Figure 12 - 4-to-1 Mux TG Schematic

Below you can see our waveform for the 4-to-1 Mux for our transmission gate for schematic. We checked our waveform to the truth table, *Table 1*, to make sure we have correct results.

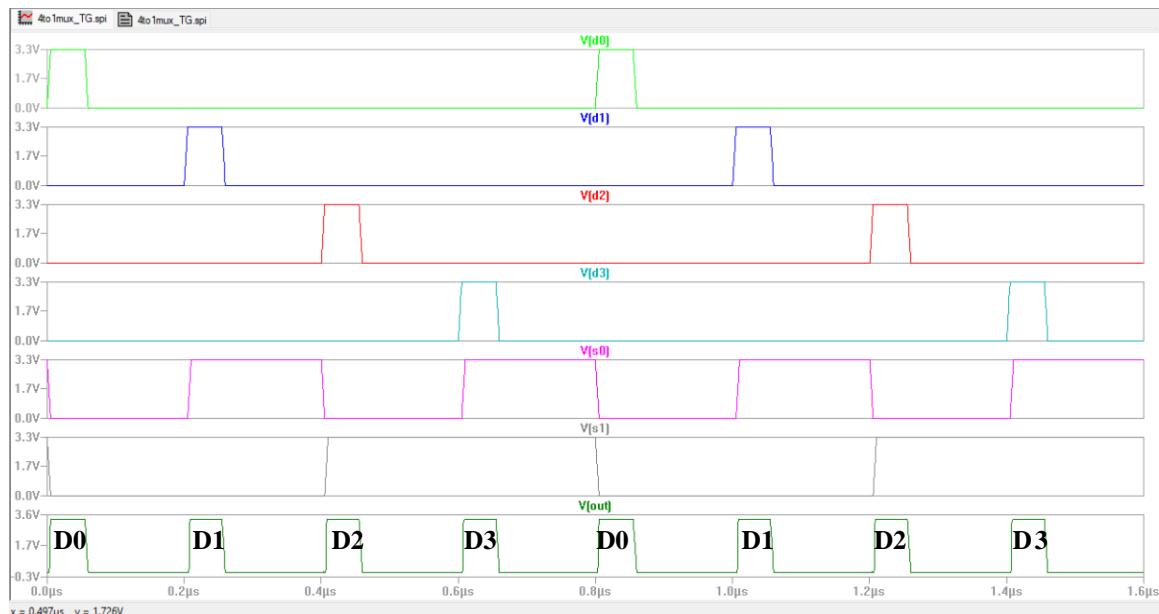


Figure 13 - LTSpice Waveform TG 4-to-1 Mux for Schematic

Below you can see our spice code for the TG 4-to-1 Mux for layout.

```
* Spice Code nodes in cell cell '4to1mux_TG{lay}'
VDD VDD 0 DC 3.3
VUSS VSS 0 DC 0
VD0 D0 0 PULSE(0 3.3 0n 5n 5n 50n 800n)
VD1 D1 0 PULSE(0 3.3 200n 5n 5n 50n 800n)
VD2 D2 0 PULSE(0 3.3 400n 5n 5n 50n 800n)
VD3 D3 0 PULSE(0 3.3 600n 5n 5n 50n 800n)
VS0 S0 0 PULSE(3.3 0 0n 5n 5n 200n 400n)
VS1 S1 0 PULSE(3.3 0 0n 5n 5n 400n 800n)
.tran 0 1600n
.include C:\Users\paniw\Downloads\EE457\Technology_MODEL.txt
.END
```

Figure 14 - 4-to-1 Mux TG Layout

Below you can see our waveform for the 4-to-1 Mux for our transmission gate for layout. We checked our waveform to the truth table, *Table 1*, to make sure we had correct results.

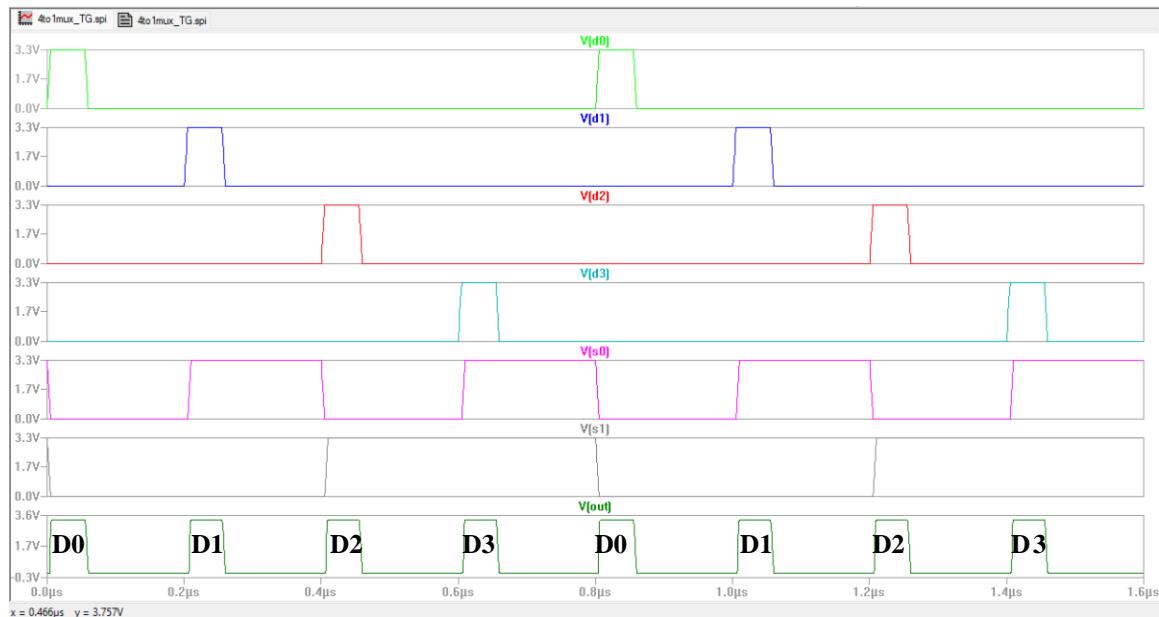


Figure 15 - LTSpice Waveform TG 4-to-1 Mux for Layout

Once we checked our Transmission Gate, we moved to check our LTSpice for Static CMOS.

Below you can see our spice code for the Static CMOS 4-to-1 Mux for schematic.

```
* Spice Code nodes in cell cell '4to1_Static{sch}'
UDD UDD 0 DC 3.3
UVSS UVSS 0 DC 0
UD0 D0 0 PULSE(0 3.3 0n 5n 5n 50n 800n)
UD1 D1 0 PULSE(0 3.3 200n 5n 5n 50n 800n)
UD2 D2 0 PULSE(0 3.3 400n 5n 5n 50n 800n)
UD3 D3 0 PULSE(0 3.3 600n 5n 5n 50n 800n)
US0 S0 0 PULSE(3.3 0 0n 5n 5n 200n 400n)
US1 S1 0 PULSE(3.3 0 0n 5n 5n 400n 800n)
.tran 0 1600n
.include C:\Users\Zack\Downloads\EE457\model.txt
.END
```

Figure 16 - LTSpice Waveform Static CMOS 4-to-1 Mux for Schematic

Below you can see our waveform for the 4-to-1 Mux for our Static CMOS for schematic. We checked our waveform to the truth table, *Table 1*, to make sure we had correct results.

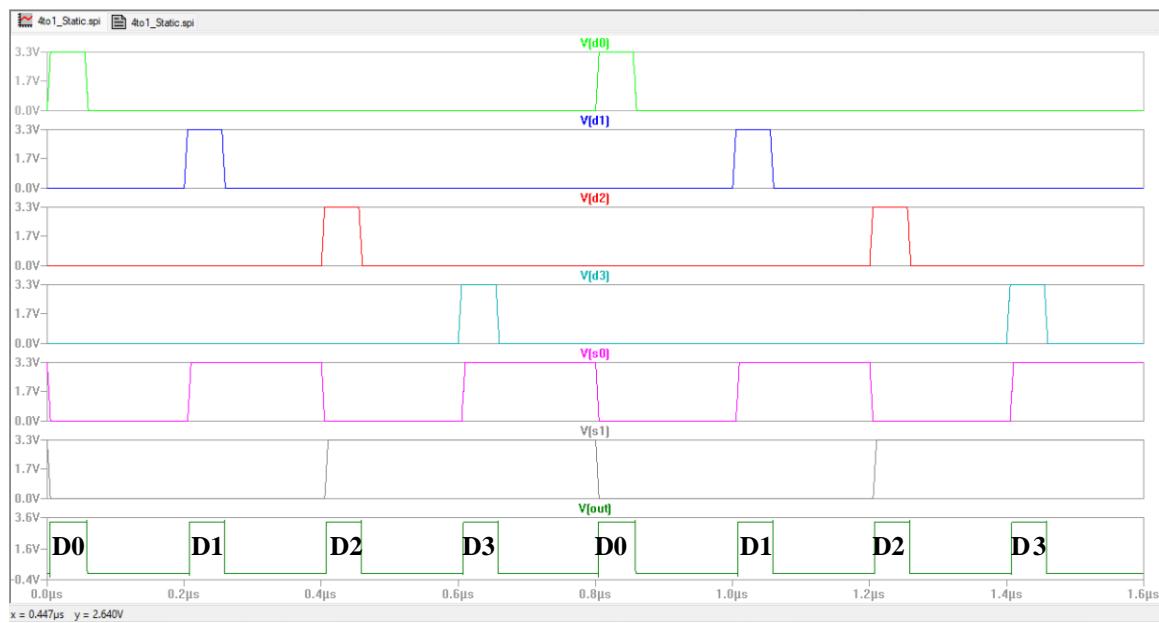


Figure 17 - LTSpice Waveform for Static CMOS 4-to-1 Mux for Schematic

Below you can see our spice code for the Static CMOS 4-to-1 Mux for layout.

```
* Spice Code nodes in cell cell '4to1_Static{lay}'
VDD VDD 0 DC 3.3
UVSS UVSS 0 DC 0
VD0 D0 0 PULSE(0 3.3 0n 5n 5n 50n 800n)
VD1 D1 0 PULSE(0 3.3 200n 5n 5n 50n 800n)
VD2 D2 0 PULSE(0 3.3 400n 5n 5n 50n 800n)
VD3 D3 0 PULSE(0 3.3 600n 5n 5n 50n 800n)
VS0 S0 0 PULSE(3.3 0 0n 5n 5n 200n 400n)
VS1 S1 0 PULSE(3.3 0 0n 5n 5n 400n 800n)
.tran 0 1600n
.include C:\Users\Zack\Downloads\EE457\model.txt
.END
```

Figure 18 - LTSpice Waveform Static CMOS 4-to-1 Mux for Layout

Below you can see our waveform for the 4-to-1 Mux for our Static CMOS for layout. We checked our waveform to the truth table, *Table 1*, to make sure we had correct results.

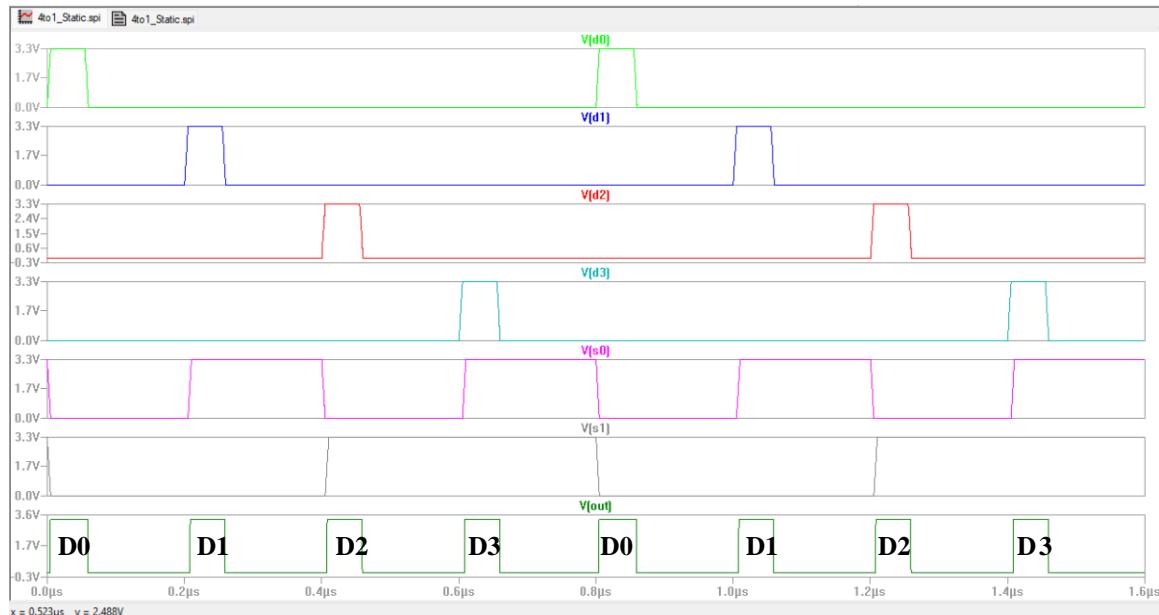


Figure 19 - LTSpice Waveform for Static CMOS 4-to-1 Mux for Layout

After we checked our design to make sure it does not have any errors, we started checking the waveform in LTSpice and comparing them to the truth table on *Table 2*. To use the IRSIM, first, we needed to figure the Spice Code out. You can see our Spice Code for the 16-to-1 Transmission Gate in *Figure 20* for schematic and *Figure 22* for Layout.

Below in *Figure 21* you can see the LTSpice waveform for our 16-to-1 Mux TG schematic and in *Figure 23*, you can see the LTSpice waveform for our 16-to-1 TG layout. We compared the waveform from Table 2 which is 16-to-1 truth table to make sure that our design worked properly.

Once we checked the Transmission Gate circuit for 16-to-1 Mux, we started to check the Static circuit for 16-to-1 Mux. You can see our Spice Code for the 16-to-1 Static Circuit in *Figure 24* for schematic and *Figure 26* for Layout.

Below in *Figure 25* you can see the LTSpice waveform for our 16-to-1 Mux Static schematic and in *Figure 27*, you can see the LTSpice waveform for our 16-to-1 Static layout. We compared the waveform from *Table 2* which is 16-to-1 truth table to make sure that our design worked properly.

```

* Spice Code nodes in cell cell '16to1mux_TG{sch}'
VDD VDD 0 DC 3.3
VUSS VSS 0 DC 0
UD0 D0 0 PULSE(0 3.3 0n 5n 5n 50n 1600n)
UD1 D1 0 PULSE(0 3.3 100n 5n 5n 50n 1600n)
UD2 D2 0 PULSE(0 3.3 200n 5n 5n 50n 1600n)
UD3 D3 0 PULSE(0 3.3 300n 5n 5n 50n 1600n)
UD4 D4 0 PULSE(0 3.3 400n 5n 5n 50n 1600n)
UD5 D5 0 PULSE(0 3.3 500n 5n 5n 50n 1600n)
UD6 D6 0 PULSE(0 3.3 600n 5n 5n 50n 1600n)
UD7 D7 0 PULSE(0 3.3 700n 5n 5n 50n 1600n)
UD8 D8 0 PULSE(0 3.3 800n 5n 5n 50n 1600n)
UD9 D9 0 PULSE(0 3.3 900n 5n 5n 50n 1600n)
UD10 D10 0 PULSE(0 3.3 1000n 5n 5n 50n 1600n)
UD11 D11 0 PULSE(0 3.3 1100n 5n 5n 50n 1600n)
UD12 D12 0 PULSE(0 3.3 1200n 5n 5n 50n 1600n)
UD13 D13 0 PULSE(0 3.3 1300n 5n 5n 50n 1600n)
UD14 D14 0 PULSE(0 3.3 1400n 5n 5n 50n 1600n)
UD15 D15 0 PULSE(0 3.3 1500n 5n 5n 50n 1600n)
US0 S0 0 PULSE(0 3.3 100n 5n 5n 100n 200n)
US1 S1 0 PULSE(0 3.3 200n 5n 5n 200n 400n)
US2 S2 0 PULSE(0 3.3 400n 5n 5n 400n 800n)
US3 S3 0 PULSE(0 3.3 800n 5n 5n 800n 1600n)
.tran 0 1600n
.include C:\Users\paniw\Downloads\EE457\Technology_MODEL.txt
.END

```

Figure 20 - Spice Code for TG Schematic for 16-to-1 Mux

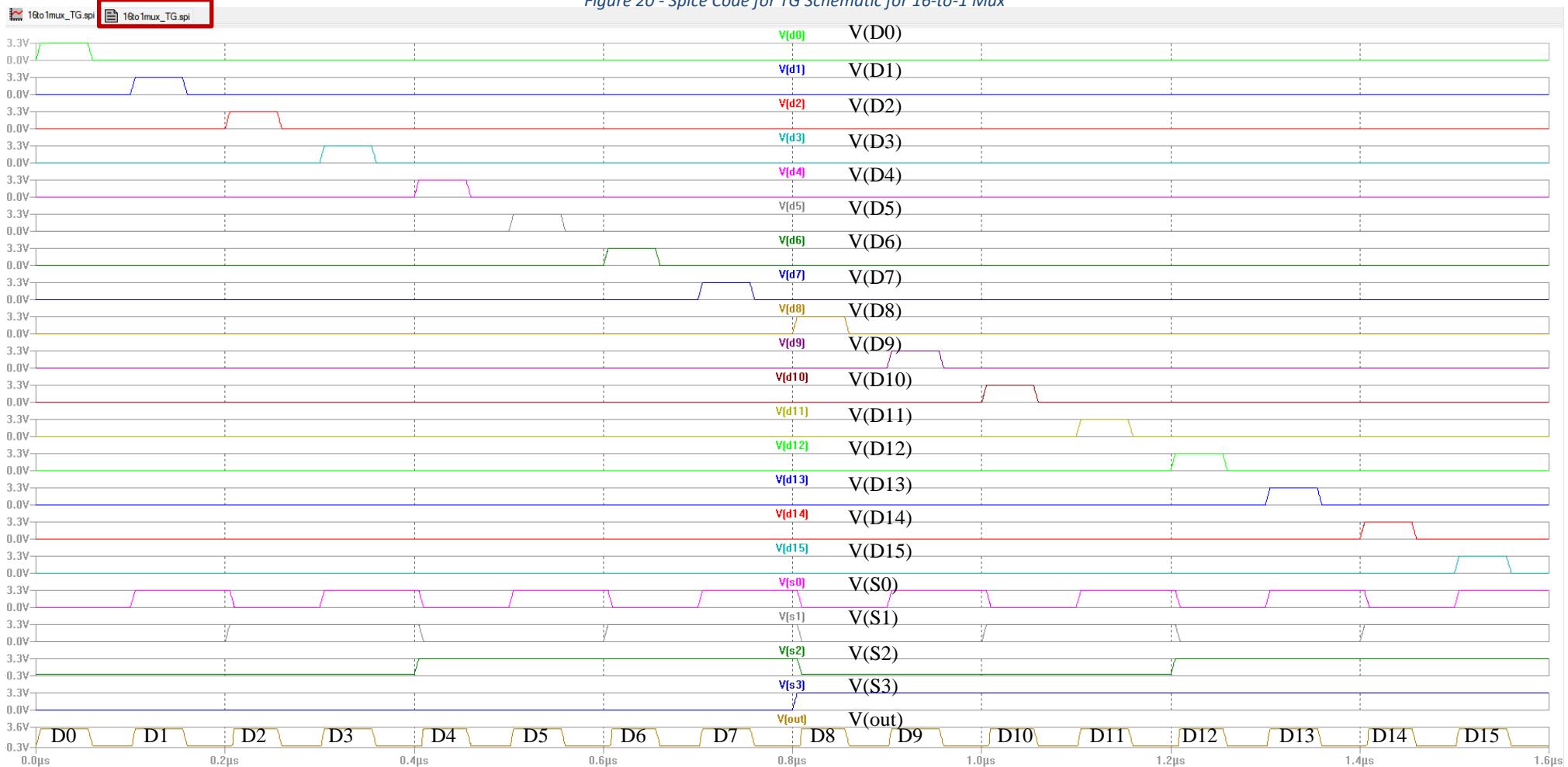


Figure 21 – Output TG Schematic for 16-to-1 Mux

```

* Spice Code nodes in cell cell '16to1mux_TG{lay}'
VDD VDD 0 DC 3.3
VUSS VUSS 0 DC 0
V00 D0 0 PULSE(0 3.3 0n 5n 5n 50n 1600n)
V01 D1 0 PULSE(0 3.3 100n 5n 5n 50n 1600n)
V02 D2 0 PULSE(0 3.3 200n 5n 5n 50n 1600n)
V03 D3 0 PULSE(0 3.3 300n 5n 5n 50n 1600n)
V04 D4 0 PULSE(0 3.3 400n 5n 5n 50n 1600n)
V05 D5 0 PULSE(0 3.3 500n 5n 5n 50n 1600n)
V06 D6 0 PULSE(0 3.3 600n 5n 5n 50n 1600n)
V07 D7 0 PULSE(0 3.3 700n 5n 5n 50n 1600n)
V08 D8 0 PULSE(0 3.3 800n 5n 5n 50n 1600n)
V09 D9 0 PULSE(0 3.3 900n 5n 5n 50n 1600n)
V010 D10 0 PULSE(0 3.3 1000n 5n 5n 50n 1600n)
V011 D11 0 PULSE(0 3.3 1100n 5n 5n 50n 1600n)
V012 D12 0 PULSE(0 3.3 1200n 5n 5n 50n 1600n)
V013 D13 0 PULSE(0 3.3 1300n 5n 5n 50n 1600n)
V014 D14 0 PULSE(0 3.3 1400n 5n 5n 50n 1600n)
V015 D15 0 PULSE(0 3.3 1500n 5n 5n 50n 1600n)
US0 S0 0 PULSE(0 3.3 100n 5n 5n 100n 200n)
US1 S1 0 PULSE(0 3.3 200n 5n 5n 200n 400n)
US2 S2 0 PULSE(0 3.3 400n 5n 5n 400n 800n)
US3 S3 0 PULSE(0 3.3 800n 5n 5n 800n 1600n)
.tran 0 1600n
.include C:\Users\paniv\Downloads\EE457\Technology_MODEL.txt
.END

```

Figure 22 - Spice Code for TG Layout for 16-to-1 Mux

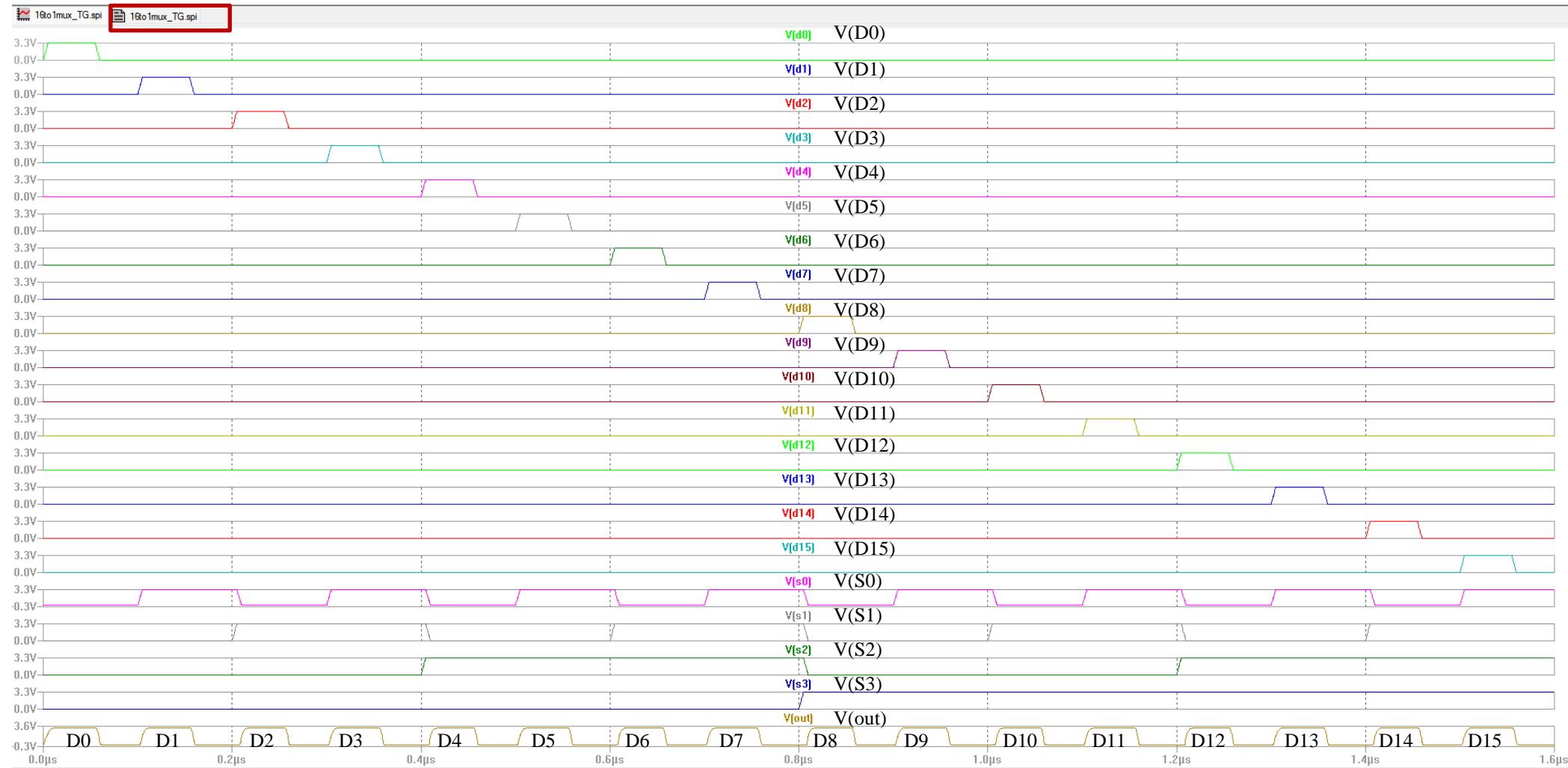


Figure 23 - Output for TG Layout for 16-to-1 Mux

```

* Spice Code nodes in cell cell '16to1mux_Static{sch}'
UDD UDD 0 DC 3.3
VUSS VSS 0 DC 0
UD0 D0 0 PULSE(0 3.3 0n 5n 5n 50n 1600n)
UD1 D1 0 PULSE(0 3.3 100n 5n 5n 50n 1600n)
UD2 D2 0 PULSE(0 3.3 200n 5n 5n 50n 1600n)
UD3 D3 0 PULSE(0 3.3 300n 5n 5n 50n 1600n)
UD4 D4 0 PULSE(0 3.3 400n 5n 5n 50n 1600n)
UD5 D5 0 PULSE(0 3.3 500n 5n 5n 50n 1600n)
UD6 D6 0 PULSE(0 3.3 600n 5n 5n 50n 1600n)
UD7 D7 0 PULSE(0 3.3 700n 5n 5n 50n 1600n)
UD8 D8 0 PULSE(0 3.3 800n 5n 5n 50n 1600n)
UD9 D9 0 PULSE(0 3.3 900n 5n 5n 50n 1600n)
UD10 D10 0 PULSE(0 3.3 1000n 5n 5n 50n 1600n)
UD11 D11 0 PULSE(0 3.3 1100n 5n 5n 50n 1600n)
UD12 D12 0 PULSE(0 3.3 1200n 5n 5n 50n 1600n)
UD13 D13 0 PULSE(0 3.3 1300n 5n 5n 50n 1600n)
UD14 D14 0 PULSE(0 3.3 1400n 5n 5n 50n 1600n)
UD15 D15 0 PULSE(0 3.3 1500n 5n 5n 50n 1600n)
US0 S0 0 PULSE(0 3.3 180n 5n 5n 100n 200n)
US1 S1 0 PULSE(0 3.3 200n 5n 5n 200n 400n)
US2 S2 0 PULSE(0 3.3 400n 5n 5n 400n 800n)
US3 S3 0 PULSE(0 3.3 800n 5n 5n 800n 1600n)
.tran 0 1600n
.include C:\Users\Zack\Downloads\EE457\model.txt
.END

```

Figure 24 - Spice Code for Static CMOS Schematic for 16-to-1 Mux

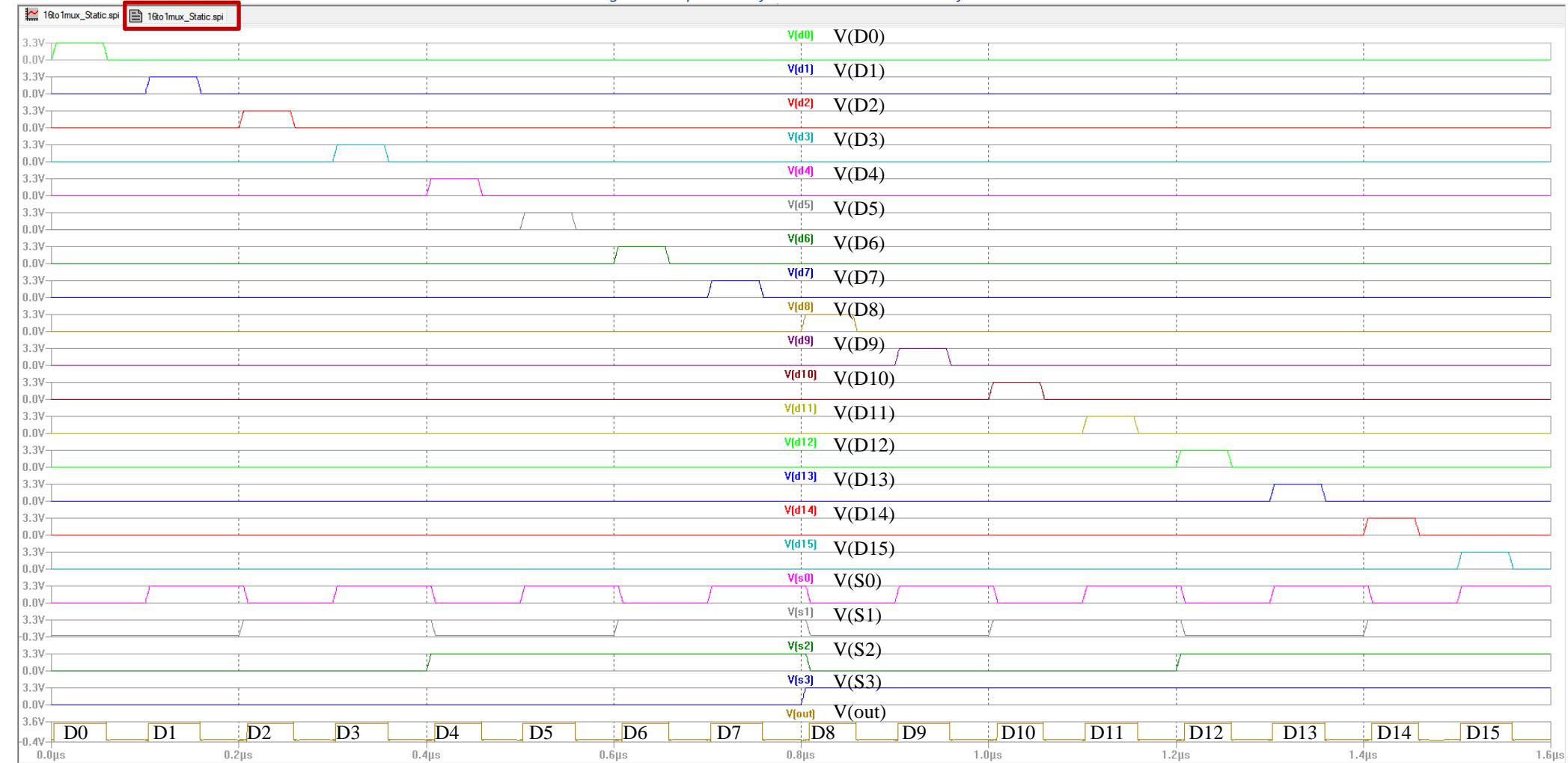


Figure 25 – Output for Static CMOS Schematic for 16-to-1 Mux

```

* Spice Code nodes in cell cell '16to1mux_Static{lay}'
UDD UDD 0 DC 3.3
USS USS 0 DC 0
UD0 D0 0 PULSE(0 3.3 0n 5n 5n 50n 1600n)
UD1 D1 0 PULSE(0 3.3 100n 5n 5n 50n 1600n)
UD2 D2 0 PULSE(0 3.3 200n 5n 5n 50n 1600n)
UD3 D3 0 PULSE(0 3.3 300n 5n 5n 50n 1600n)
UD4 D4 0 PULSE(0 3.3 400n 5n 5n 50n 1600n)
UD5 D5 0 PULSE(0 3.3 500n 5n 5n 50n 1600n)
UD6 D6 0 PULSE(0 3.3 600n 5n 5n 50n 1600n)
UD7 D7 0 PULSE(0 3.3 700n 5n 5n 50n 1600n)
UD8 D8 0 PULSE(0 3.3 800n 5n 5n 50n 1600n)
UD9 D9 0 PULSE(0 3.3 900n 5n 5n 50n 1600n)
UD10 D10 0 PULSE(0 3.3 1000n 5n 5n 50n 1600n)
UD11 D11 0 PULSE(0 3.3 1100n 5n 5n 50n 1600n)
UD12 D12 0 PULSE(0 3.3 1200n 5n 5n 50n 1600n)
UD13 D13 0 PULSE(0 3.3 1300n 5n 5n 50n 1600n)
UD14 D14 0 PULSE(0 3.3 1400n 5n 5n 50n 1600n)
UD15 D15 0 PULSE(0 3.3 1500n 5n 5n 50n 1600n)
US0 S0 0 PULSE(0 3.3 180n 5n 5n 100n 200n)
US1 S1 0 PULSE(0 3.3 200n 5n 5n 200n 400n)
US2 S2 0 PULSE(0 3.3 400n 5n 5n 400n 800n)
US3 S3 0 PULSE(0 3.3 800n 5n 5n 800n 1600n)
.tran 0 1600n
.include C:\Users\Zack\Downloads\EE457\model.txt
.END

```

Figure 26 - Spice Code for Static CMOS Layout for 16-to-1

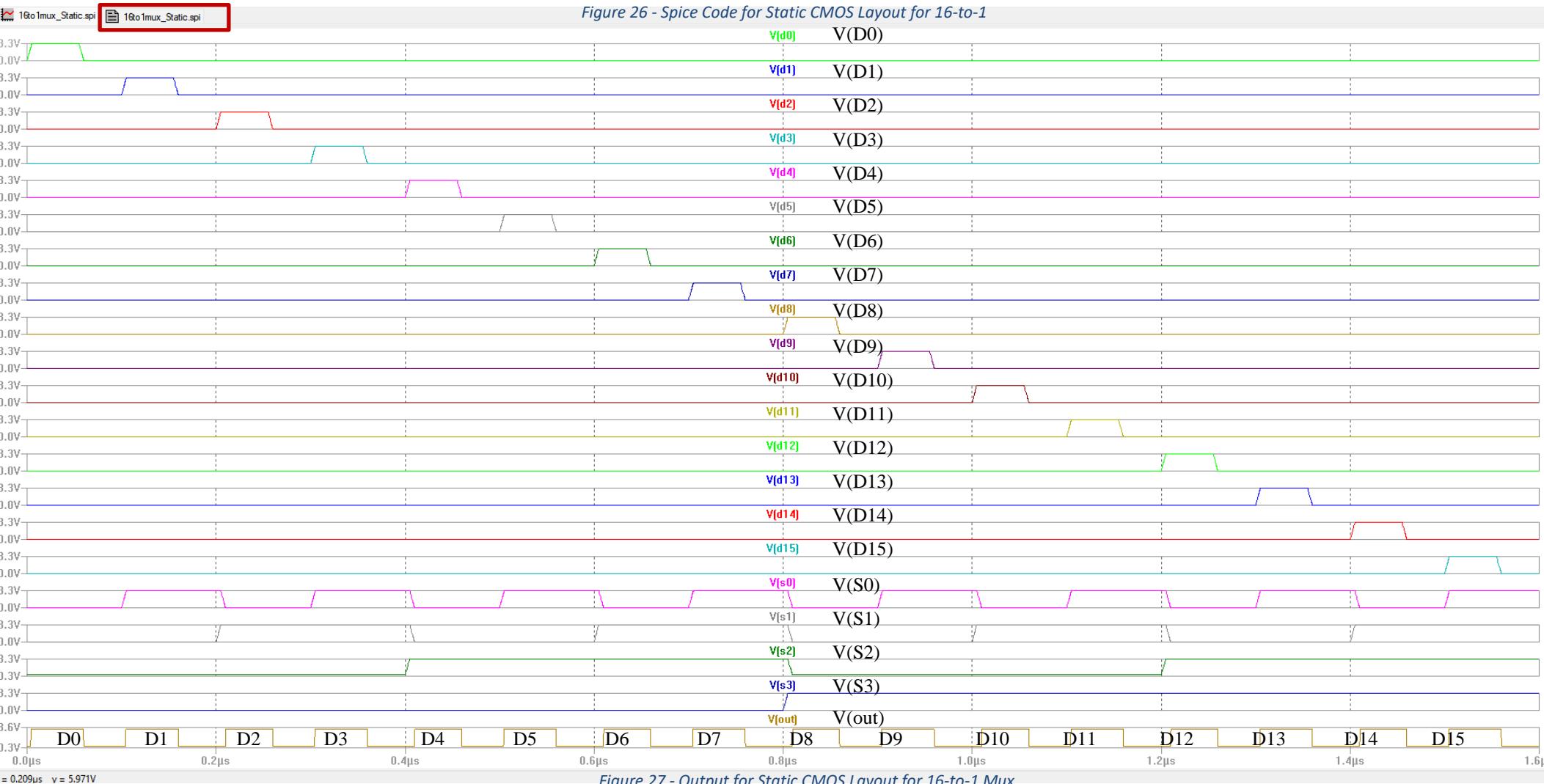


Figure 27 - Output for Static CMOS Layout for 16-to-1 Mux

Once we made sure our LTSpice had the correct waveform, we started to extract the Parasitic Extraction. Based on the requirement, we included screenshots of portions of the Parasitic extraction to show that we have been able to extract the data successfully. Below you can see our Parasitic Extraction for the Transmission Gate.

In *Figure 28*, you can see the NMOS characteristics we got from Parasitic Extraction for TG Layout.

```
*** TOP LEVEL CELL: 16to1mux_TG{lay}
Mnnos@0 net@0 S@#17nnos@0_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@1 net@2 S@#1nnos@1_poly-left D1 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@2 net@2 net@0#9nnos@2_poly-left D0 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@3 net@12 S@#8nnos@3_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@4 net@14 S@#5nnos@4_poly-left D3 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@5 net@14 net@12#9nnos@5_poly-left D2 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@6 net@70 S@#4nnos@6_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@7 net@72 S@#1nnos@7_poly-left net@0#14 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@8 net@72 net@7#9nnos@8_poly-left net@0#2 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@9 net@2#7 S@#3nnos@9_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@10 net@216 S@#38nnos@10_poly-left D5 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@11 net@216 net@2#7 S@#2#7nnos@11_poly-left D4 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@12 net@231 S@#39nnos@12_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@13 net@240 S@#27nnos@13_poly-left D7 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@14 net@240 net@2#4#23 S@#2#9nnos@14_poly-left D6 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@15 net@218 S@#1#8nnos@15_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@16 net@218 S@#18nnos@16_poly-left net@2#4#0 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@17 net@218#12nnos@17_poly-left net@2#16 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@18 net@414 S@#5#2nnos@18_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@19 net@423 S@#6#6nnos@19_poly-left D9 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@20 net@423 net@4#14#12nnos@20_poly-left D8 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@21 net@438 S@#6#1nnos@21_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@22 net@447 S@#4#9nnos@22_poly-left D11 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@23 net@447 net@4#38#9nnos@23_poly-left D10 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@24 net@425 S@#1#2#0nnos@24_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@25 net@417 S@#1#2#8nnos@25_poly-left net@4#47 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@26 net@417 net@4#25#12nnos@26_poly-left net@4#23 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@27 net@421 S@#0#7#4nnos@27_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@28 net@630 S@#0#8#2nnos@28_poly-left D13 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@29 net@630 net@6#21#12nnos@29_poly-left D12 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@30 net@645 S@#0#3#3nnos@30_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@31 net@654 S@#0#7#1nnos@31_poly-left D15 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@32 net@654 net@6#45#9nnos@32_poly-left D14 USS N L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mnnos@33 net@632 S@#1#3#0nnos@33_poly-right USS USS N L=0.35U W=1.75U AS=19.294P AD=2.373P PS=48.3U PD=6.212U
Mnnos@34 net@624 S@#1#3#8nnos@34_noin-left net@6#54 USS N I=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Figure 28 - Parasitic Extraction for NMOS characteristics for TG Layout
```

In *Figure 29*, you can see the PMOS characteristics we got from Parasitic Extraction for TG Layout.

```
Mpmos@0 net@0 S@#21pmos@0_poly-left vdd vdd P L=0.35U W=1.75U AS=11.638P AD=2.373P PS=32.55U PD=6.212U
Mpmos@1 net@2 net@0#7pmos@1_poly-left D1 vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@2 net@2 S@#3pmos@2_poly-right D0 vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@3 net@12 S@#8#12pmos@3_poly-left vdd vdd P L=0.35U W=1.75U AS=11.638P AD=2.373P PS=32.55U PD=6.212U
Mpmos@4 net@14 net@12#7pmos@4_poly-left D3 vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@5 net@14 S@#7#9pmos@5_poly-right D2 vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@6 net@70 S@#1#8pmos@6_poly-left vdd vdd P L=0.35U W=1.75U AS=11.638P AD=2.373P PS=32.55U PD=6.212U
Mpmos@7 net@72 net@7#8#7pmos@7_poly-left net@14 vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@8 net@72 S@#1#3pmos@8_poly-right net@2 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@9 net@2#7 S@#35pmos@9_poly-left vdd vdd P L=0.35U W=1.75U AS=11.638P AD=2.373P PS=32.55U PD=6.212U
Mpmos@10 net@216 net@2#7#9pmos@10_poly-left D5 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@11 net@216 S@#2#3pmos@11_poly-right D4 vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@12 net@231 S@#4#3pmos@12_poly-left vdd vdd P L=0.35U W=1.75U AS=11.638P AD=2.373P PS=32.55U PD=6.212U
Mpmos@13 net@240 net@2#4#23 S@#2#9pmos@13_poly-left D7 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@14 net@240 S@#3#7pmos@14_poly-right D6 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@15 net@218 S@#1#16pmos@15_poly-left vdd vdd P L=0.35U W=1.75U AS=11.638P AD=2.373P PS=32.55U PD=6.212U
Mpmos@16 net@218 net@2#18#10pmos@16_poly-left net@2#4#0 vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@17 net@210 S@#1#19pmos@17_poly-right net@2#16 vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@18 net@414 S@#5#7pmos@18_poly-left vdd vdd P L=0.35U W=1.75U AS=11.638P AD=2.373P PS=32.55U PD=6.212U
Mpmos@19 net@423 net@4#14#9pmos@19_poly-left D9 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@20 net@423 S@#4#5pmos@20_poly-right D8 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@21 net@438 S@#6#5pmos@21_poly-left vdd vdd P L=0.35U W=1.75U AS=11.638P AD=2.373P PS=32.55U PD=6.212U
Mpmos@22 net@447 net@4#38#7pmos@22_poly-left D11 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@23 net@447 S@#5#9pmos@23_poly-right D10 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@24 net@425 S@#1#2#6pmos@24_poly-left vdd vdd P L=0.35U W=1.75U AS=11.638P AD=2.373P PS=32.55U PD=6.212U
Mpmos@25 net@417 net@4#25#10pmos@25_poly-left net@4#47 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@26 net@417 S@#1#2#9pmos@26_poly-right net@4#23 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@27 net@621 S@#0#7#9pmos@27_poly-left vdd vdd P L=0.35U W=1.75U AS=11.638P AD=2.373P PS=32.55U PD=6.212U
Mpmos@28 net@630 net@6#21#9pmos@28_poly-left D13 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Mpmos@29 net@630 S@#6#7pmos@29_poly-right D12 vdd vdd P L=0.35U W=1.75U AS=2.45P AD=2.45P PS=6.3U PD=6.3U
Figure 29 - Parasitic Extraction for PMOS characteristics for TG Layout
```

In *Figure 30*, you can see the Parasitic Extraction of Capacitors TG Layout.

```
** Extracted Parasitic Capacitors ***
C0 net@0 0 9.059FF
C1 net@2 0 22.358FF
C2 D1 0 7.04FF
C3 D0 0 7.363FF
C4 net@12 0 9.059FF
C5 net@14 0 21.9FF
C6 D3 0 7.04FF
C7 D2 0 7.363FF
C8 net@78 0 9.059FF
C9 net@72 0 31.536FF
C10 net@207 0 9.059FF
C11 net@216 0 22.358FF
C12 D5 0 7.04FF
C13 D4 0 7.363FF
C14 net@231 0 9.059FF
C15 net@240 0 21.9FF
C16 D7 0 7.04FF
C17 D6 0 7.363FF
C18 net@218 0 9.059FF
C19 net@210 0 40.447FF
C20 net@414 0 9.059FF
C21 net@423 0 22.358FF
C22 D9 0 7.04FF
C23 D8 0 7.363FF
C24 net@438 0 9.059FF
C25 net@447 0 21.9FF
C26 D11 0 7.04FF
C27 D10 0 7.363FF
C28 net@425 0 9.059FF
C29 net@417 0 40.663FF
C30 net@621 0 9.059FF
C31 net@630 0 22.358FF
C32 D13 0 7.04FF
C33 D12 0 7.363FF
```

*Figure 30 - Parasitic Extraction of Capacitors for TG Layout*

In *Figure 31*, you can see Parasitic Extraction of Resistors for TG Layout.

```
** Extracted Parasitic Resistors ***
R0 S@#0pin@4_polysilicon-1 S@#1nmos@1_poly-left 9.3
R1 net@#2pin@0_polysilicon-1 net@#2pin@0_polysilicon-1##0 9.079
R2 net@#2pin@0_polysilicon-1##0 net@#2pin@0_polysilicon-1##1 9.079
R3 net@#2pin@0_polysilicon-1##1 net@#2pin@0_polysilicon-1##2 9.079
R4 net@#2pin@0_polysilicon-1##2 net@#2pin@0_polysilicon-1##3 9.079
R5 net@#2pin@0_polysilicon-1##3 net@#2pin@0_polysilicon-1##4 9.079
R6 net@#2pin@0_polysilicon-1##4 net@#2pin@0_polysilicon-1##5 9.079
R7 net@#2pin@0_polysilicon-1##5 net@0 9.079
R8 net@0 net@#0##0 9.708
R9 net@#0##1 net@#0##1 9.708
R10 net@#0##1 net@#0##2 9.708
R11 net@#0##2 net@#0##3 9.708
R12 net@#0##3 net@#0##4 9.708
R13 net@#0##4 net@#0##5 9.708
R14 net@#0##5 net@#0##6 9.708
R15 net@#0##6 net@#0##7 9.708
R16 net@#0##7 net@#0##8 9.708
R17 net@#0##8 net@#0##9 9.708
R18 net@#0##9 net@#0##10 9.708
R19 net@#0##10 net@#0##11 9.708
R20 net@#0##11 net@#0##12 9.708
R21 net@#0##12 net@#0##13 9.708
R22 net@#0##13 net@#0##14 9.708
R23 net@#0##14 net@#0##15 9.708
R24 net@#0##15 net@#0##16 9.708
R25 net@#0##16 net@#0##17 9.708
R26 net@#0##17 net@#0##4pin@10_polysilicon-1 9.708
R27 S@#2pin@11_polysilicon-1 S@#2pin@11_polysilicon-1##0 9.472
R28 S@#2pin@11_polysilicon-1##0 S@#2pin@11_polysilicon-1##1 9.472
R29 S@#2pin@11_polysilicon-1##1 S@#2pin@11_polysilicon-1##2 9.472
R30 S@#2pin@11_polysilicon-1##2 S@#2pin@11_polysilicon-1##3 9.472
R31 S@#2pin@11_polysilicon-1##3 S@#2pin@11_polysilicon-1##4 9.472
R32 S@#2pin@11_polysilicon-1##4 S@#2pin@11_polysilicon-1##5 9.472
R33 S@#2pin@11_polysilicon-1##5 S@#2pin@11_polysilicon-1##6 9.472
R34 S@#2pin@11_polysilicon-1##6 S@#2pin@11_polysilicon-1##7 9.472
R35 S@#2pin@11_polysilicon-1##7 S@#3pmos@2_poly-right 9.472
R36 S@#4pin@24_dolusilicon-1 S@#5nmos@4_poly-left 9.3
```

*Figure 31 - Parasitic Extraction of Resistors for TG Layout*

To find our resistors and capacitors values we used the methodology below. The Parasitic extraction generated 4307 lines of results. First, we needed to filter the extraction to be able to do the calculation.

To find the capacitor for  $V_{out}$ , we did the below methodology:

1. We copy the capacitor section in the Word documents to be able to use the search feature.
2. We found the capacitor for each signal.
3. Calculate the sum of total capacitance for each signal. Since the capacitors are more than likely to be in parallel, we added them all together.

To find the  $R_P$  (PMOS resistor) and  $R_n$  (NMOS resistor) for  $V_{out}$ , we did the below methodology:

1. Similar to the methodology for capacitors, first we copy the resistor section in the Word documents to be able to use the search feature.
2. First, we need to find whether the resistor is connected to a PMOS or a NMOS to know if we should count it for  $R_P$  or  $R_n$ .
  - a. If it is connected to both PMOS and NMOS, then we apply it to whichever is the source; for instance, the left side connection is the source of the resistor, and the right side is the destination.
  - b. If the source is something other than a PMOS or NMOS transistor something like polysilicon, but the destination is a NMOS or PMOS, we added the resistance to  $R_n$  or  $R_P$  since that NMOS or PMOS still shares that resistance.
3. Finally, we calculated the sum of values for each signal. We also needed to check if the transistor connects to it in parallel or series and add them accordingly.

Based on the Parasitic Extraction we found the following data for out  $V_{out}$  for Transmission Gate for 16-to-1 Mux.

*Table 3 - Parasitic Extraction Measurement for TG 16-to-1 Mux*

Signal	$R_P$ ( $\Omega$ )	$R_N$ ( $\Omega$ )	$C$ (fF)
$V_{out}$	301.965 $\Omega$	260.4 $\Omega$	12.828fF

Below you can see the Parasitic Extraction for our Static 16-to-1 Mux Layout.

In *Figure 32*, you can see the NMOS characteristics we got from Parasitic Extraction for Static Layout.

```
*** TOP LEVEL CELL: 16to1mux_Static(1ay)
Hnnos@0 net@146#2pmos@0_diff-bottom S@21nnos@0_poly-right gnd gnd N L=0.35U W=1.75U AS=8.958P AD=2.45P PS=21.612U PD=6.3U
Hnnos@1 net@294 D@48nnos@1_poly-right net@113#2contact@13_metal-1-n-act gnd N L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
Hnnos@2 gnd net@146 net@294 gnd N L=0.35U W=1.75U AS=0.919P AD=8.958P PS=2.8U PD=21.612U
Hnnos@3 net@327 S@0#1nnos@3_poly-right net@124#3pmos@3_diff-bottom gnd N L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
Hnnos@4 gnd D$#0#nnos@4_poly-right net@327 gnd N L=0.35U W=1.75U AS=0.919P AD=8.958P PS=2.8U PD=21.612U
Hnnos@5 net@2 net@113 net@0 gnd L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
Hnnos@6 gnd net@124 net@2 gnd N L=0.35U W=1.75U AS=0.919P AD=8.958P PS=2.8U PD=21.612U
Hnnos@7 net@15#6contact@58_metal-1-metal-2 S@0#3nnos@7_poly-right gnd gnd N L=0.35U W=1.75U AS=8.958P AD=2.45P PS=21.612U PD=6.3U
Hnnos@8 D$#0#nnos@8_poly-right net@10#2contact@49_metal-1-n-act gnd N L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
Hnnos@9 gnd net@45#net@25 gnd N L=0.35U W=1.75U AS=0.919P AD=8.958P PS=2.8U PD=21.612U
Hnnos@10 gnd net@011 S@0#8nnos@10_poly-right net@11#3contact@43_metal-1-p-act gnd N L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
Hnnos@11 gnd D7#0#nnos@11_poly-right net@11 gnd N L=0.35U W=1.75U AS=0.919P AD=8.958P PS=2.8U PD=21.612U
Hnnos@12 net@346 net@10 net@45 gnd N L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
Hnnos@13 gnd net@111#3contact@46_metal-1-metal-2 S@13nnos@14_poly-right gnd gnd N L=0.35U W=1.75U AS=8.958P AD=2.45P PS=21.612U PD=6.3U
Hnnos@14 net@134 net@0#3nnos@15_poly-right net@98 gnd N L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
Hnnos@15 gnd net@123#6contact@6_metal-1-n-act net@134#3pmos@14_poly-right gnd gnd N L=0.35U W=1.75U AS=8.958P AD=2.45P PS=21.612U PD=6.3U
Hnnos@16 gnd net@123 net@134 gnd N L=0.35U W=1.75U AS=0.919P AD=8.958P PS=2.8U PD=21.612U
Hnnos@17 net@174 S1#0#nnos@17_poly-right net@103 gnd N L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
Hnnos@18 gnd net@45#5nnos@18_poly-right net@174 gnd N L=0.35U W=1.75U AS=0.919P AD=8.958P PS=2.8U PD=21.612U
Hnnos@19 net@96 net@98#3nnos@19_poly-right net@94 gnd N L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
Hnnos@20 gnd net@103#3nnos@20_poly-right net@96 gnd N L=0.35U W=1.75U AS=0.919P AD=8.958P PS=2.8U PD=21.612U
Hnnos@21 net@06#2pmos@21_diff-bottom S@0#5nnos@21_poly-right gnd gnd N L=0.35U W=1.75U AS=8.958P AD=2.45P PS=21.612U PD=6.3U
Hnnos@22 net@654 D@0#nnos@22_poly-right net@47#2contact@131_metal-1-n-act gnd N L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
Hnnos@23 gnd net@056 net@54 gnd N L=0.35U W=1.75U AS=0.919P AD=8.958P PS=2.8U PD=21.612U
Hnnos@24 net@87 S@#4#nnos@24_poly-right net@48#3pmos@24_diff-bottom gnd N L=0.35U W=1.75U AS=1.889P AD=0.919P PS=4.492U PD=2.8U
```

*Figure 32 - Parasitic Extraction for NMOS characteristics for Static Layout*

In *Figure 33*, you can see the PMOS characteristics we got from Parasitic Extraction for Static Layout.

```
Hpnos@0 net@146#2pmos@0_diff-bottom S@0#3pmos@0_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=2.45P PS=15.05U PD=6.3U
Hpnos@1 net@113#2contact@13_metal-1-n-act D@4#1pmos@1_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
Hpnos@2 vdd net@146#4pmos@2_poly-left net@113#2contact@13_metal-1-n-act vdd P L=0.35U W=1.75U AS=1.889P AD=6.169P PS=4.492U PD=15.05U
Hpnos@3 net@124#3pmos@3_diff-bottom S@0#1pmos@3_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
Hpnos@4 vdd D$#2pmos@4_poly-left net@124#3pmos@3_diff-bottom vdd P L=0.35U W=1.75U AS=1.889P AD=6.169P PS=4.492U PD=15.05U
Hpnos@5 net@011#1pmos@5_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
Hpnos@6 vdd net@113#1pmos@5_poly-left net@08 vdd vdd P L=0.35U W=1.75U AS=1.889P AD=6.169P PS=4.492U PD=15.05U
Hpnos@7 net@15#6contact@58_metal-1-metal-2 S@12pmos@7_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=2.45P PS=15.05U PD=6.3U
Hpnos@8 net@10#2contact@49_metal-1-n-act D@6#1pmos@8_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
Hpnos@9 vdd net@1#2pmos@9_poly-left net@10#2contact@49_metal-1-n-act vdd P L=0.35U W=1.75U AS=1.889P AD=6.169P PS=4.492U PD=15.05U
Hpnos@10 net@11#3contact@43_metal-1-p-act S@0#1pmos@10_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
Hpnos@11 vdd D7#2pmos@11_poly-left net@11#3contact@43_metal-1-p-act vdd P L=0.35U W=1.75U AS=1.889P AD=6.169P PS=4.492U PD=15.05U
Hpnos@12 net@45 net@01#1pmos@12_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
Hpnos@13 vdd net@11#2pmos@13_poly-left net@45 vdd P L=0.35U W=1.75U AS=1.889P AD=6.169P PS=4.492U PD=15.05U
Hpnos@14 net@123#6contact@96_metal-1-metal-2 S@1#5pmos@14_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=2.45P PS=15.05U PD=6.3U
Hpnos@15 net@99 net@0#4pmos@15_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
Hpnos@16 vdd net@123#2pmos@16_poly-left net@98 vdd P L=0.35U W=1.75U AS=1.889P AD=6.169P PS=4.492U PD=15.05U
Hpnos@17 net@103 S1#1#pmos@17_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
Hpnos@18 vdd net@45#7pmos@18_poly-left net@103 vdd P L=0.35U W=1.75U AS=1.889P AD=6.169P PS=4.492U PD=15.05U
Hpnos@19 net@94 net@98#4pmos@19_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
Hpnos@20 vdd net@103#5pmos@20_poly-left net@94 vdd P L=0.35U W=1.75U AS=1.889P AD=6.169P PS=4.492U PD=15.05U
Hpnos@21 net@06#2pmos@21_diff-bottom S@#7pmos@21_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=2.45P PS=15.05U PD=6.3U
Hpnos@22 net@47#2contact@131_metal-1-n-act D@8#1pmos@22_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
Hpnos@23 vdd net@05#64pmos@23_poly-left net@47#2contact@131_metal-1-n-act vdd P L=0.35U W=1.75U AS=1.889P AD=6.169P PS=4.492U PD=15.05U
Hpnos@24 net@48#3pmos@24_diff-bottom S@#4#9pmos@24_poly-left vdd vdd P L=0.35U W=1.75U AS=6.169P AD=1.889P PS=15.05U PD=4.492U
```

*Figure 33 - Parasitic Extraction for PMOS characteristics for Static Layout*

In *Figure 34*, you can see the Parasitic Extraction of Capacitors for the Static 16-to-1 Mux Layout.

```
** Extracted Parasitic Capacitors ***
C0 net@146#2pmos@0_diff-bottom 0 4.165FF
C1 net@113#2contact@13_metal-1-n-act 0 7.833FF
C2 net@124#3pmos@3_diff-bottom 0 5.53FF
C3 net@0 0 13.088FF
C4 D4 0 3.226FF
C5 S@30contact@24_metal-1-metal-2 0 1.966FF
C6 D5 0 4.81FF
C7 net@15#6contact@58_metal-1-metal-2 0 4.165FF
C8 net@10#2contact@49_metal-1-n-act 0 7.833FF
C9 net@11#3contact@43_metal-1-p-act 0 5.53FF
C10 net@45 0 12.828FF
C11 D6 0 3.226FF
C12 S@7contact@68_metal-1-metal-2 0 1.966FF
C13 D7 0 4.81FF
C14 net@123#6contact@96_metal-1-metal-2 0 4.165FF
C15 net@98 0 7.833FF
C16 net@103 0 5.53FF
C17 net@94 0 19.99FF
C18 S@7contact@98_metal-1-metal-2 0 1.966FF
C19 net@506#2pmos@21_diff-bottom 0 4.165FF
C20 net@473#2contact@131_metal-1-n-act 0 7.833FF
C21 net@484#3pmos@24_diff-bottom 0 5.53FF
C22 net@360 0 13.088FF
C23 D8 0 3.226FF
C24 S@68contact@142_metal-1-metal-2 0 1.966FF
C25 D1 0 4.81FF
C26 net@375#6contact@176_metal-1-metal-2 0 4.165FF
C27 net@370#2contact@167_metal-1-n-act 0 7.833FF
C28 net@371#3contact@161_metal-1-p-act 0 5.53FF
C29 net@405 0 12.828FF
C30 D2 0 3.226FF
C31 S@45contact@178_metal-1-metal-2 0 1.966FF
C32 D3 0 4.81FF
C33 net@483#6contact@214_metal-1-metal-2 0 4.165FF
C34 net@458 0 7.833FF
C35 net@463 0 5.53FF
C36 net@454 0 19.189FF
```

*Figure 34 - Parasitic Extraction of Capacitors for Static Layout*

In *Figure 35*, you can see Parasitic Extraction of Resistors for our Static 16-to-1 Mux Layout.

```
** Extracted Parasitic Resistors ***
R0 D6#0nmos@8_poly-right D6#0nmos@8_poly-right##0 9.3
R1 D6#0nmos@8_poly-right##0 D6#0nmos@8_poly-right##1 9.3
R2 D6#0nmos@8_poly-right##1 D6#0nmos@8_poly-right##2 9.3
R3 D6#0nmos@8_poly-right##2 D6#0nmos@8_poly-right##3 9.3
R4 D6#0nmos@8_poly-right##3 D6#0nmos@8_poly-right##4 9.3
R5 D6#0nmos@8_poly-right##4 D6#0nmos@8_poly-right##5 9.3
R6 D6#0nmos@8_poly-right##5 D6#0nmos@8_poly-right##6 9.3
R7 D6#0nmos@8_poly-right##6 D6#0nmos@8_poly-right##7 9.3
R8 D6#0nmos@8_poly-right##7 D6#0nmos@8_poly-right##8 9.3
R9 D6#0nmos@8_poly-right##8 D6#0nmos@8_poly-right##9 9.3
R10 D6#0nmos@8_poly-right##9 D6#0nmos@8_poly-right##10 9.3
R11 D6#0nmos@8_poly-right##10 D6#1pmos@8_poly-left 9.3
R12 S@0nmos@10_poly-right S@0nmos@10_poly-right##0 9.3
R13 S@0nmos@10_poly-right##0 S@0nmos@10_poly-right##1 9.3
R14 S@0nmos@10_poly-right##1 S@0nmos@10_poly-right##2 9.3
R15 S@0nmos@10_poly-right##2 S@0nmos@10_poly-right##3 9.3
R16 S@0nmos@10_poly-right##3 S@0nmos@10_poly-right##4 9.3
R17 S@0nmos@10_poly-right##4 S@0nmos@10_poly-right##5 9.3
R18 S@0nmos@10_poly-right##5 S@0nmos@10_poly-right##6 9.3
R19 S@0nmos@10_poly-right##6 S@0nmos@10_poly-right##7 9.3
R20 S@0nmos@10_poly-right##7 S@0nmos@10_poly-right##8 9.3
R21 S@0nmos@10_poly-right##8 S@0nmos@10_poly-right##9 9.3
R22 S@0nmos@10_poly-right##9 S@0nmos@10_poly-right##10 9.3
R23 S@0nmos@10_poly-right##10 S@1pmos@10_poly-left 9.3
R24 D7#0nmos@11_poly-right D7#0nmos@11_poly-right##0 9.3
R25 D7#0nmos@11_poly-right##0 D7#0nmos@11_poly-right##1 9.3
R26 D7#0nmos@11_poly-right##1 D7#0nmos@11_poly-right##2 9.3
R27 D7#0nmos@11_poly-right##2 D7#0nmos@11_poly-right##3 9.3
R28 D7#0nmos@11_poly-right##3 D7#0nmos@11_poly-right##4 9.3
R29 D7#0nmos@11_poly-right##4 D7#0nmos@11_poly-right##5 9.3
```

*Figure 35 - Parasitic Extraction of Resistors for Static Layout*

To find our resistors and capacitors values we used the methodology below. The Parasitic extraction generated 4054 lines of results. First, we needed to filter the extraction to be able to do the calculation.

To find the capacitor for  $V_{out}$ , we did the below methodology:

4. We copy the capacitor section in the Word documents to be able to use the search feature.
5. We found the capacitor for each signal.
6. Calculate the sum of total capacitance for each signal. Since the capacitors are more than likely to be in parallel, we added them all together.

To find the  $R_P$  (PMOS resistor) and  $R_n$  (NMOS resistor) for  $V_{out}$ , we did the below methodology:

4. Similar to the methodology for capacitors, first we copy the resistor section in the Word documents to be able to use the search feature.
5. First, we need to find whether the resistor is connected to a PMOS or a NMOS to know if we should count it for  $R_P$  or  $R_n$ .
  - a. If it is connected to both PMOS and NMOS, then we apply it to whichever is the source; for instance, the left side connection is the source of the resistor, and the right side is the destination.
  - b. If the source is something other than a PMOS or NMOS transistor something like polysilicon, but the destination is a NMOS or PMOS, we added the resistance to  $R_n$  or  $R_P$  since that NMOS or PMOS still shares that resistance.
6. Finally, we calculated the sum of values for each signal. We also needed to check if the transistor connects to it in parallel or series and add them accordingly.

Based on the Parasitic Extraction we found the following data for out  $V_{out}$  for our Static 16-to-1 Mux.

*Table 4 - Parasitic Extraction Measurement for Static 16-to-1 Mux*

Signal	$R_P$ ( $\Omega$ )	$R_N$ ( $\Omega$ )	$C$ (fF)
$V_{out}$	534.23 $\Omega$	437.936 $\Omega$	5.238 fF

## Section 6: IRSIM Logic Simulations and Measurements for Layout and Schematic

Below you can see the waveform IRSIM for our 4-to-1 Transmission Gate Schematic. To make sure our design worked properly, we compared our design with *Table 1* which shows the truth table for 4-to-1 Mux.

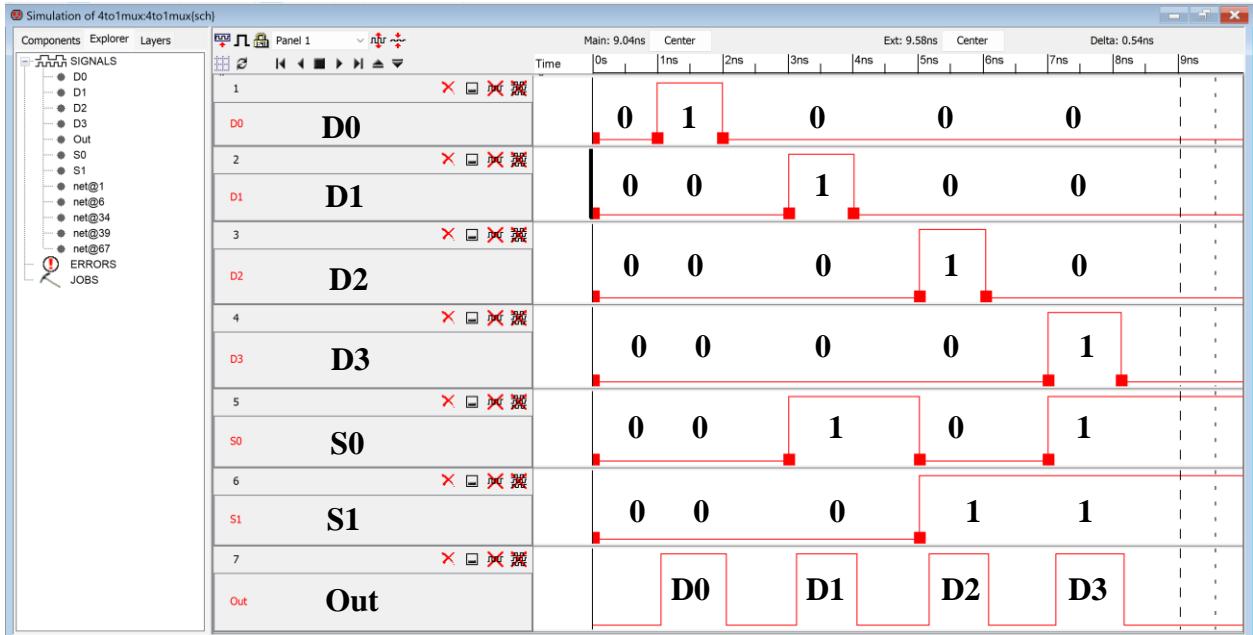


Figure 36 – TG 4-to-1 Schematic

Below you can see the IRSIM waveform for our 4-to-1 Transmission Gate Layout. To make sure our design worked properly, we compared our design with *Table 1* which shows the truth table for 4-to-1 Mux.

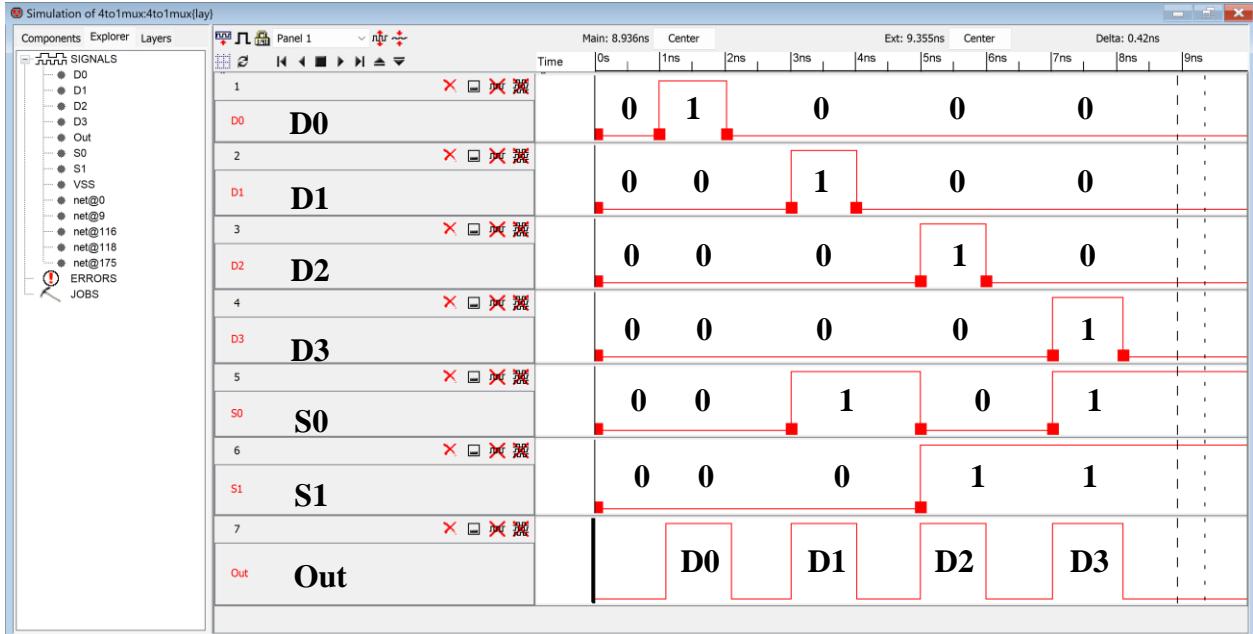


Figure 37 – TG 4-to-1 Layout

Below you can see the waveform for our 4-to-1 Static Circuit Schematic. To make sure our design worked properly, we compared our design with *Table 1* which shows the truth table for 4-to-1 Mux.

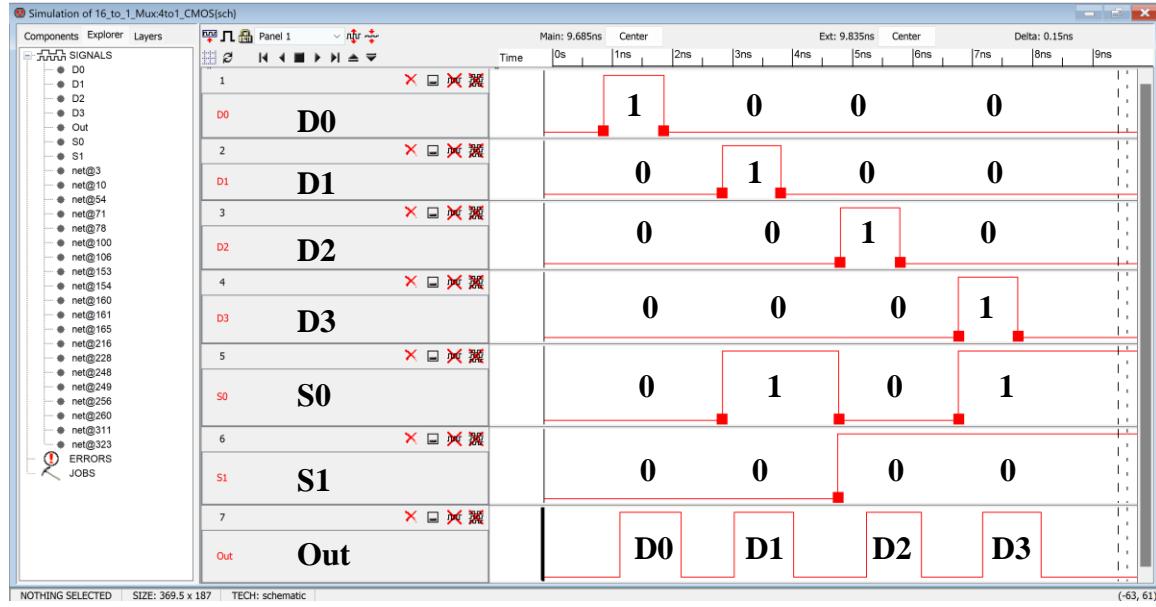


Figure 38 – 4-to-1 Static Circuit Schematic

Below you can see the waveform for our 4-to-1 Static Circuit Layout. To make sure our design worked properly, we compared our design with *Table 1* which shows the truth table for 4-to-1 Mux.

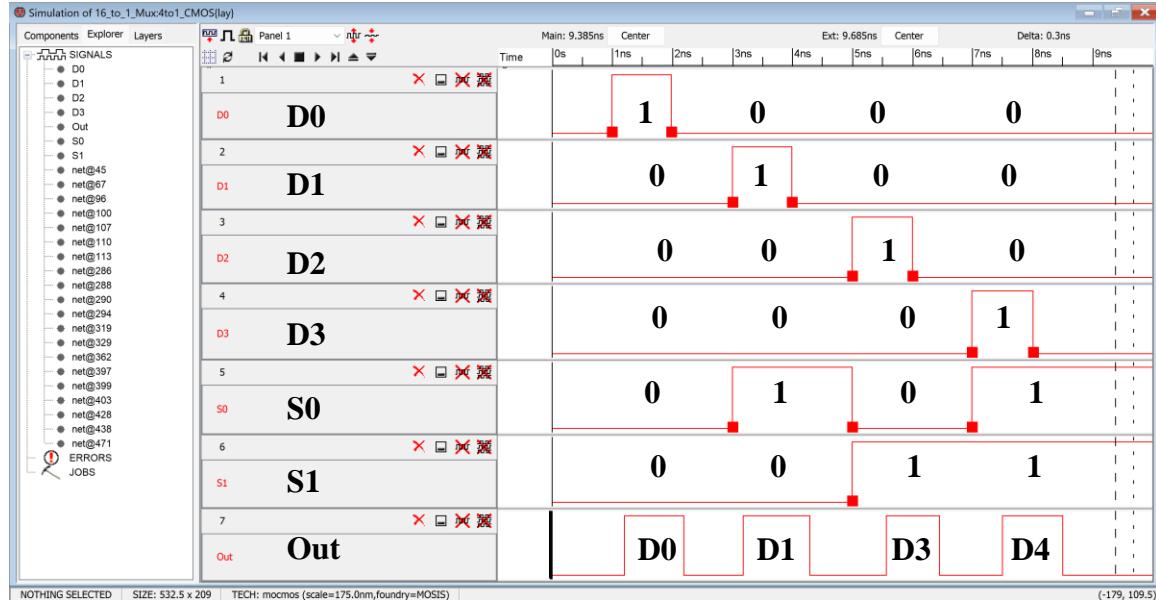


Figure 39 – 4-to-1 Static Circuit Layout

Once we had our 4-to-1 Mux and checked the waveform and saw that they worked properly, we moved forward to design our 16-to-1 Mux for both TG and Static.

Below you can see our IRSIM for 16-to-1 Transmission Gate Circuit for Schematic.

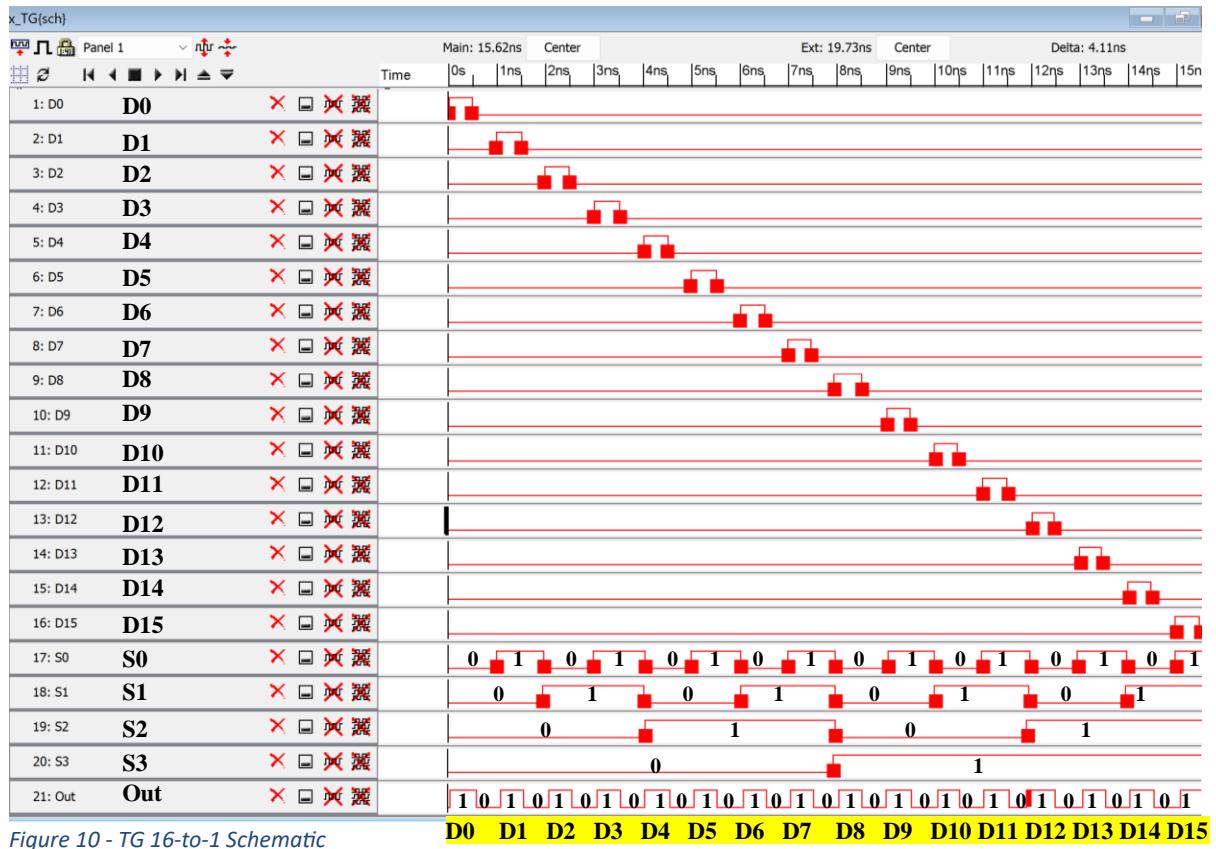


Figure 10 - TG 16-to-1 Schematic

Below you can see our IRSIM for 16-to-1 Transmission Gate Circuit for Layout.

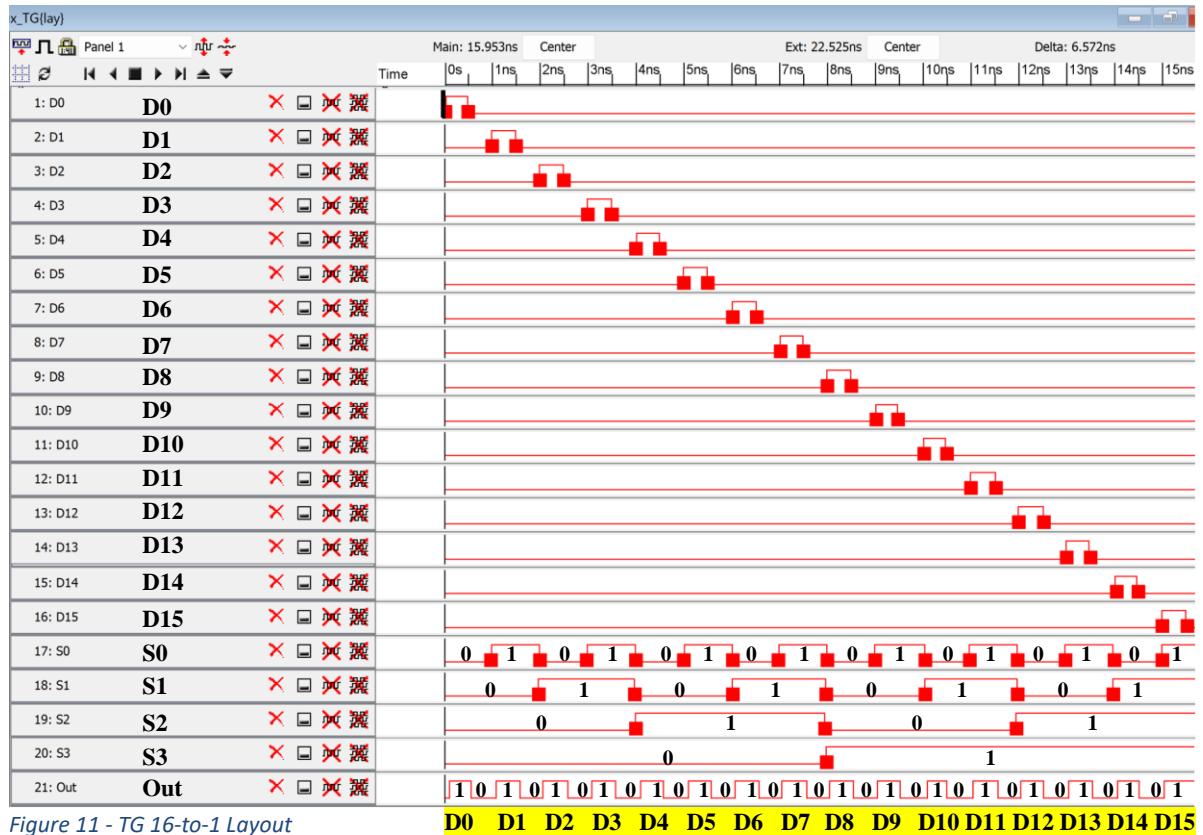


Figure 11 - TG 16-to-1 Layout

D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15

Below you can see our IRSIM for 16-to-1 Static CMOS Circuit for Schematic.

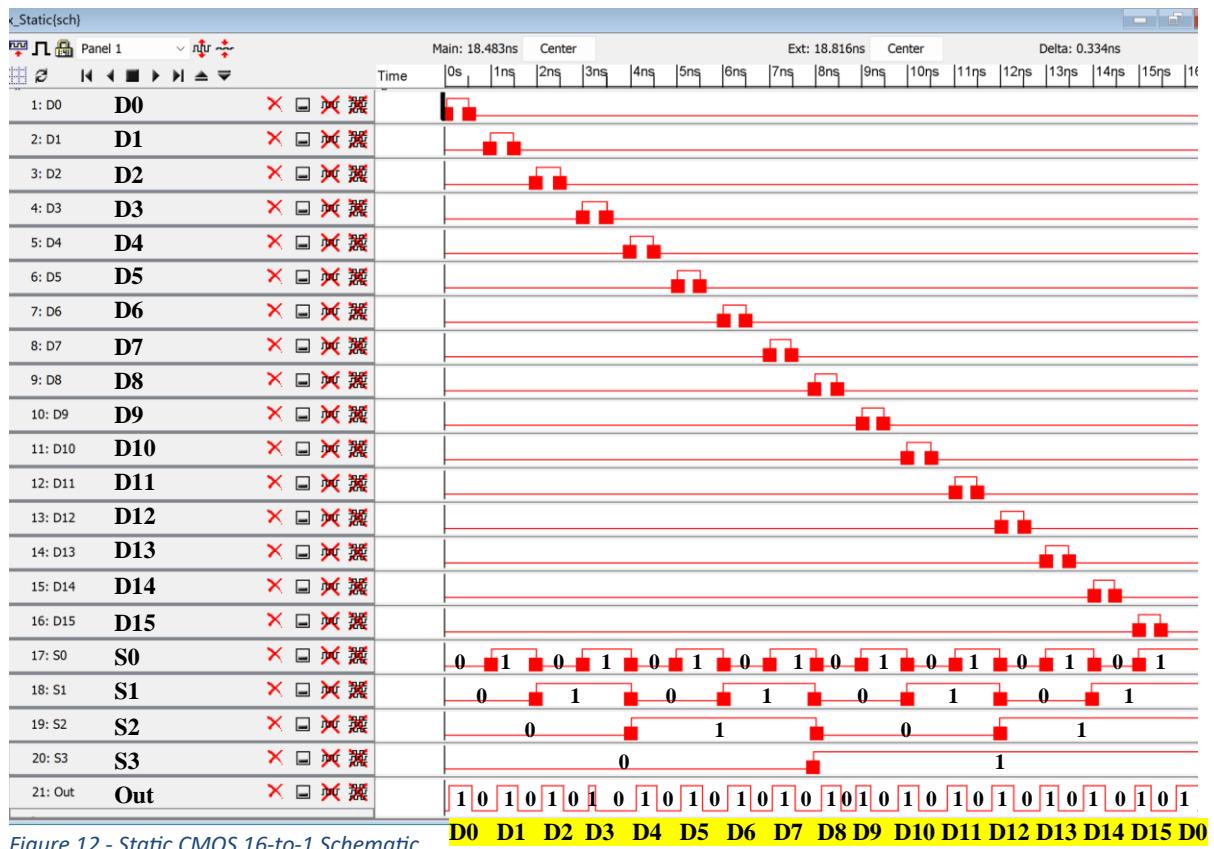
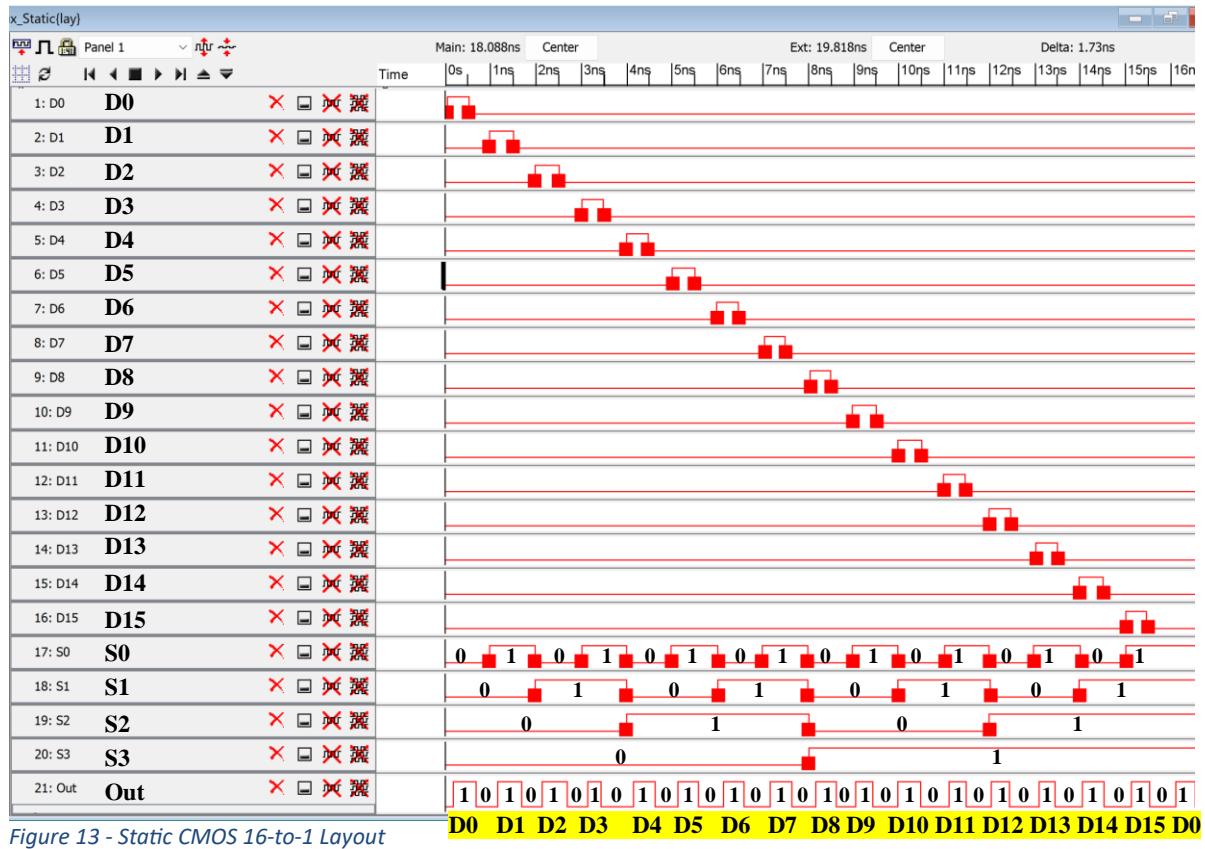


Figure 12 - Static CMOS 16-to-1 Schematic

Below you can see our IRSIM for 16-to-1 Static CMOS Circuit for Layout.



## Section 7: Measurements in LTSPICE for delays for Layout and Schematic

Now that we have verified that our design for the 16-to-1 Multiplexer created with both transmission gates, and with Static CMOS, we can now compare the performance of the two by adding the following SPICE code for running in LTSPICE.

```
.measure rs trig v(out) = 0.33 TD = 0 rise = 2 targ v(out) = 2.97 TD = 0 rise = 2
.measure f1 trig v(out) = 2.97 TD = 0 fall = 2 targ v(out) = 0.33 TD = 0 fall = 2
.measure TPHL trig v(D0) = 1.65 TD = 0 rise = 1 targ v(out) = 1.65 TD = 0 rise = 2
.measure TPLH trig v(D0) = 1.65 TD = 0 fall = 1 targ v(out) = 1.65 TD = 0 fall = 2
.measure propdelay param = (TPHL + TPLH)/2
```

We can then find these values in LTSPICE when the code is run.

```
SPICE Error Log: C:\Users\Zack\Downloads\16to1mux_TG.log
Circuit: *** SPICE deck for cell 16tolmux_TG(sch) from library 16_to_1_Mux-(1)
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
WARNING: Less than two connections to node VSS. This node is used by VVSS.
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

rs=2.59602e-009 FROM 1.02121e-007 TO 1.04717e-007
f1=3.84068e-009 FROM 1.55709e-007 TO 1.5955e-007
tphl=1.00635e-007 FROM 2.5e-009 TO 1.03135e-007
tplh=1.0016e-007 FROM 5.75e-008 TO 1.5766e-007
propdelay: (tphl + tplh)/2=1.00397e-007

Date: Thu May 16 13:22:41 2024
Total elapsed time: 1.260 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 7096

SPICE Error Log: C:\Users\Zack\Downloads\16to1mux_TG.log
Circuit: *** SPICE deck for cell 16tolmux_TG(lay) from library 16_to_1_Mux-(1)
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Direct Newton iteration for .op point succeeded.

rs=5.73812e-009 FROM 1.02871e-007 TO 1.08609e-007
f1=3.11125e-009 FROM 1.57092e-007 TO 1.60203e-007
tphl=1.02316e-007 FROM 2.5e-009 TO 1.04816e-007
tplh=1.01385e-007 FROM 5.75e-008 TO 1.58885e-007
propdelay: (tphl + tplh)/2=1.0185e-007

Date: Thu May 16 13:22:52 2024
Total elapsed time: 8.875 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 7171
traniter = 7155
tranpoints = 2530
accept = 2111
rejected = 419
matrix size = 3609
```

Figure 14 - TG 16-to-1 Schematic & Layout

```

SPICE Error Log: C:\Users\Zack\Downloads\16to1mux_Static.log
Circuit: *** SPICE deck for cell 16tolmux_Static{sch} from library 16_to_1_Mux

Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
WARNING: Less than two connections to node VSS. This node is used by VVSS.
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

rs=4.55214e-011 FROM 1.03133e-007 TO 1.03178e-007
fl=4.96493e-011 FROM 1.58769e-007 TO 1.58819e-007
tphl=1.00652e-007 FROM 2.5e-009 TO 1.03152e-007
tplh=1.0129e-007 FROM 5.75e-008 TO 1.5879e-007
propdelay: (tplh + tphl)/2=1.00971e-007

Date: Thu May 16 13:20:01 2024
Total elapsed time: 3.169 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 13395

SPICE Error Log: C:\Users\Zack\Downloads\16to1mux_Static.log
Circuit: *** SPICE deck for cell 16tolmux_Static{lay} from library 16_to_1_Mux

Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
WARNING: Less than two connections to node VSS. This node is used by VVSS.
Direct Newton iteration for .op point succeeded.

rs=2.50148e-010 FROM 1.04314e-007 TO 1.04564e-007
fl=1.75954e-010 FROM 1.59819e-007 TO 1.59995e-007
tphl=1.01912e-007 FROM 2.5e-009 TO 1.04412e-007
tplh=1.02411e-007 FROM 5.75e-008 TO 1.59911e-007
propdelay: (tplh + tphl)/2=1.02162e-007

Date: Thu May 16 13:51:35 2024
Total elapsed time: 16.127 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 12056
traniter = 12045
tranpoints = 3927
accept = 3043
rejected = 884

```

Figure 45 – Static CMOS 16-to-1 Schematic & Layout

We could find the rise and fall times by using the values that we found in section 7 from our Spice code. Below you can find the rise and the fall times:

Table 5 – Rise and Fall Time for TG 16-to-1 Mux

16-to-1 TG	Schematic	Layout
Rise Time	2.596 ns	5.74 ns
Fall Time	3.84 ns	3.11 ns

Table 6 - Rise and Fall Time for Static 16-to-1 Mux

16-to-1 Static CMOS	Schematic	Layout
Rise Time	0.0456 ns	0.25 ns
Fall Time	0.0496 ns	0.175 ns

As you can see the layout's rise and fall times are much higher. Since the layout is closer to a real-world implementation than the schematic this difference is expected. Additionally, the timing for the Static CMOS is shorter than the transmission gate.

To find the delay we added the TPHL and TPLH and then divided them by 2.

$$T_P = \frac{T_{PHL} + T_{PLH}}{2}$$

*Table 7 - Delay Table for TG*

16-to-1 TG	Schematic	Layout
High to Low (TPHL)	100.635 ns	102.316 ns
Low to High (TPLH)	100.16 ns	101.385 ns
Propagation Delay	100.397 ns	101.85 ns

*Table 8 - Delay Table for Static*

16-to-1 Static CMOS	Schematic	Layout
High to Low (TPHL)	100.625 ns	101.912 ns
Low to High (TPLH)	101.29ns	102.411 ns
Propagation Delay	100.97 ns	102.162 ns

As you can see the layout propagation delay is slightly longer than schematic. Due to the physical characteristics of the circuit being considered, the difference in the delays makes sense. Additionally, the delay for the Static CMOS is slightly longer than the transmission gate.

## Section 8: Measurements of power, delay, chip area, timing, number of transistors for the layout

### Power

To find the power, we used the measurements that we found from Parasitic Extraction from our  $V_{OUT}$ .

We used the power formula which is  $P = CV^2f$ .

- C = Capacitors
- V = VDD
- F = frequency

$$\text{Power for TG} = (12.828 \times 10^{-13}F) \times (3.3^2) \times (10^7 \text{Hz}) = 1.3973352 \times 10^{-4} \text{ W}$$

$$\text{Power for Static} = (5.238 \times 10^{-13}F) \times (3.3^2) \times (10^7 \text{Hz}) = 5.703042 \times 10^{-5} \text{ W}$$

### Delay

To find the delay we added the TPHL and TPLH and then divided them by 2. We can refer to Figures 44 and 45.

To find the delay we added the TPHL and TPLH and then divided them by 2.

$$T_p = \frac{T_{PHL} + T_{PLH}}{2}$$

Table 9 - Delay Table for TG

16-to-1 TG	Schematic	Layout
High to Low (TPHL)	100.635 ns	102.316 ns
Low to High (TPLH)	100.16 ns	101.385 ns
Propagation Delay	100.397 ns	101.85 ns

Table 10 - Delay Table for Static

16-to-1 Static CMOS	Schematic	Layout
High to Low (TPHL)	100.625 ns	101.912 ns
Low to High (TPLH)	101.29ns	102.411 ns
Propagation Delay	100.97 ns	102.162 ns

As you can see the layout propagation delay is slightly longer than the schematic. Due to the physical characteristics of the circuit being considered, the difference in the delays makes sense. Additionally, the delay for the Static CMOS is slightly longer than the transmission gate.

## Chip Area

To find the chip area, we first needed to find the measurement of the layout. Below you can see the measurements for our TG 16-to-1 Mux circuit.

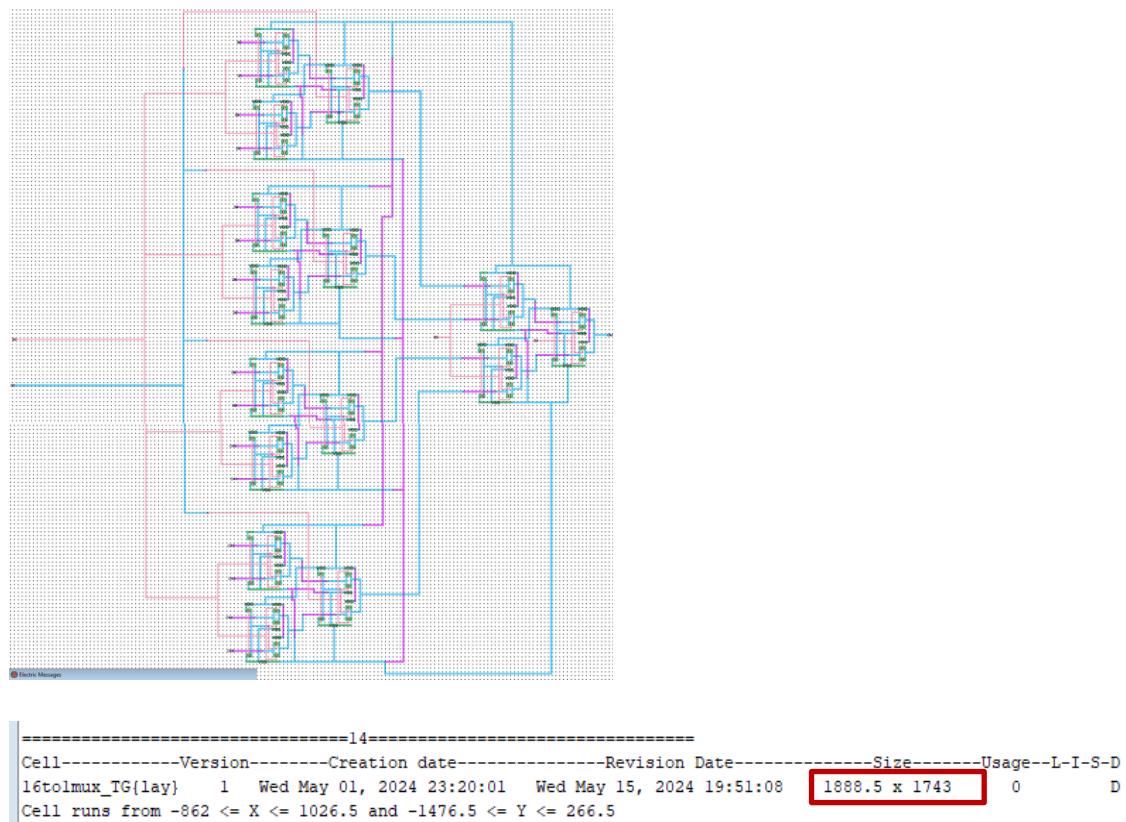


Figure 15 - Layout Measurement TG Circuit

**Width: 1743  $\lambda$**

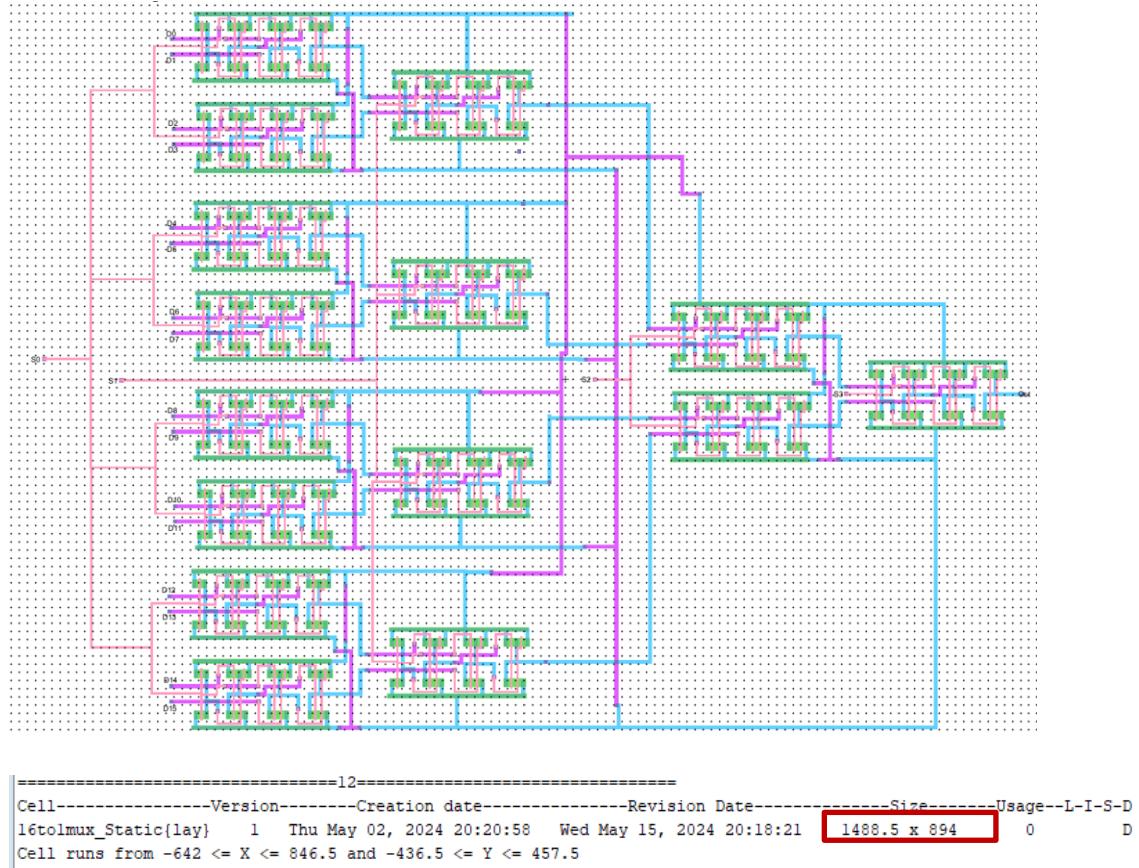
**Length: 1888.5  $\lambda$**

$$1743 \times 175 \text{ nm} = 305,025 \text{ nm} = \frac{305025 \text{ nm}}{1000 \mu\text{m}} = 305.025 \mu\text{m}$$

$$1888.5 \times 175 \text{ nm} = 330,487.5 \text{ nm} = \frac{330487.5 \text{ nm}}{1000 \mu\text{m}} = 330.4875 \mu\text{m}$$

**Total Chip Area TG 16-to-1Mux =  $305.025 \mu\text{m} \times 330.4875 \mu\text{m} = 100807.0107 \mu\text{m}^2$**

Below you can see the measurements for our Static 16-to-1 Mux circuit.



*Figure 16 - Layout Measurement Static Circuit*

**Width:**  $894 \lambda$

**Length:**  $1488.5 \lambda$

$$894 \times 175 \text{ nm} = 156,450 \text{ nm} = \frac{156,450 \text{ nm}}{1000 \mu\text{m}} = 156.45 \mu\text{m}$$

$$1488.5 \times 175 \text{ nm} = 260,487.5 \text{ nm} = \frac{260487.5 \text{ nm}}{1000 \mu\text{m}} = 260.4875 \mu\text{m}$$

$$\text{Total Chip Area for Static 16-to-1Mux} = 156.45 \mu\text{m} \times 260.4875 \mu\text{m} = 40753.2694 \mu\text{m}^2$$

## Timing

We could find the rise and fall times by using the values that we found in section 7 from our Spice code. Below you can find the rise and the fall times:

Table 11 – Rise and Fall Time for TG 16-to-1 Mux

16-to-1 TG	Schematic	Layout
Rise Time	2.596 ns	5.74 ns
Fall Time	3.84 ns	3.11 ns

Table 12 - Rise and Fall Time for Static 16-to-1 Mux

16-to-1 Static CMOS	Schematic	Layout
Rise Time	0.0456 ns	0.25 ns
Fall Time	0.0496 ns	0.175 ns

As you can see the layout's rise and fall times are much higher. Since the layout is closer to a real-world implementation than the schematic this difference is expected. Additionally, the timing for the Static CMOS is shorter than the transmission gate.

## Number of transistors for layout

To find the number of transistors for the schematic we could go to Cell => Cell Info => Number of Transistors. To find the number of transistors for the layout we could go to Cell => Cell Info => Summarize Cell Contents.

## Number of Transistor for 16-to-1 Mux Transmission Gate:

Below in *Figure 48* you can see the Number of Transistors for our TG 16-to-1 Mux Schematic.

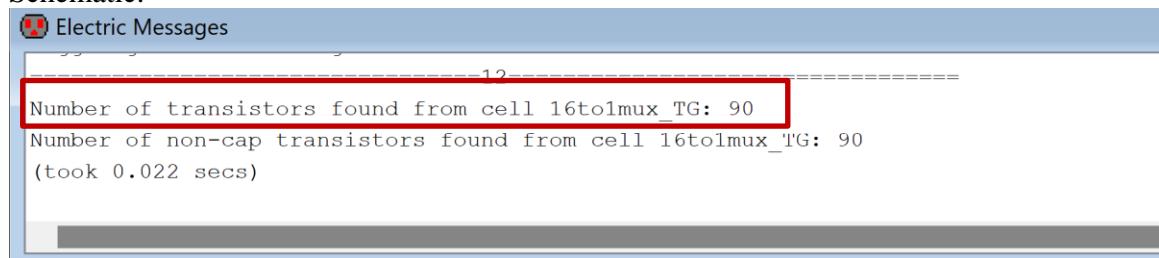


Figure 17 - Number of Transistor for Schematic for TG 16-to-1 Mux

Below in Figure 49 you can see the Number of Transistors for our TG 16-to-1 Mux Layout.

```
Layer Usage
*****
Count    Layer
255      mocmos:Active-Cut
1235     mocmos:Metal-1
274      mocmos:Metal-2
270      mocmos:N-Active
270      mocmos:N-Select
270      mocmos:N-Well
225      mocmos:P-Active
30       mocmos:P-Active-Well
255      mocmos:P-Select
255      mocmos:P-Well
22       mocmos:Poly-Cut
444      mocmos:Polysilicon-1
90       mocmos:Transistor-Poly
142      mocmos:Vial
----- Total: 4037 -----
*****
```

Figure 18 - Number of Transistor for Layout for TG 16-to-1 Mux

#### Number of Transistor for 16-to-1 Mux Static Circuit:

Below in *Figure 50* you can see the Number of Transistors for our Static Circuit 16-to-1 Mux Schematic.

```
-----14-----
Number of transistors found from cell 16tolmux_Static: 210
Number of non-cap transistors found from cell 16tolmux_Static: 210
(took 0.015 secs)
```

Figure 19 - Number of Transistor for Schematic for Static Circuit 16-to-1 Mux

Below in *Figure 51* you can see the Number of Transistors for our TG 16-to-1 Mux Layout.

Layer Usage	
Count	Layer
315	mocmos:Active-Cut
1538	mocmos:Metal-1
589	mocmos:Metal-2
405	mocmos:N-Active
405	mocmos:N-Select
495	mocmos:N-Well
480	mocmos:P-Active
15	mocmos:P-Active-Well
495	mocmos:P-Select
405	mocmos:P-Well
109	mocmos:Poly-Cut
1026	mocmos:Polysilicon-1
210	mocmos:Transistor-Poly
195	mocmos:Via1
----- Total: 6682 -----	

*Figure 20 - Number of Transistor for Layout for Static Circuit 16-to-1 Mux*

## Section 9: Conclusions

In conclusion, this project successfully designed, simulated, and analyzed 16-to-1 Multiplexer. We designed both the schematic and layouts for it using both the Static CMOS design and the Transmission Gate. Throughout the design process, we adhered to a structured approach and verified the functionality at each stage.

The initial phase involved designing and implementing the schematic of a 4-to-1 Multiplexer for both Static CMOS and the Transmission Gate. Following that, we verified the design by simulating the design in both LTSPICE and IRSIM. We were able to verify that our results were correct as both LTSPICE and IRSIM have the same output.

Afterwards, knowing that our design was correct, we then designed the 16-to-1 Multiplexer using. We saw that the functionality of the designs was working as intended and we obtained the correct results. Overall, this project demonstrates the successful design and verification of a 16-to-1 Multiplexer.

## Section 10: References

- [1] R. Teja, "Multiplexer (MUX) and multiplexing - complete guide," ElectronicsHub USA, <https://www.electronicshub.org/multiplexerandmultiplexing/> (accessed Apr. 29, 2024).
- [2] "Digital Circuits - Multiplexers - Tutorialspoint," Tutorialspoint.com, 2019. [https://www.tutorialspoint.com/digital\\_circuits/digital\\_circuits\\_multiplexers.html](https://www.tutorialspoint.com/digital_circuits/digital_circuits_multiplexers.html) (accessed Apr. 30, 2024).