Problem Statement: Panjugala Shashikala

Design a digital circuit using RTL and HLS for a FIR Interpolator.

🎯 Requirements

- The interpolator circuit should perform a 2X interpolation.
- Use the below co-efficient structure.
    - [1,0,2,0,3,4,3,0,2,0,1]
- The Interpolator circuit should give the output samples continuously for every clock cycle as long as the inputs are continuous.
- Let's say if an input vector length of 100 given to the Interpolator, conventionally we should get (100*2)+((11-1)/2) = 205 samples as output and out of them only 200 are valid.
    - But, the circuit should remove the invalid samples internally and send only the valid samples out.
    - Also, If the input vector is ended, all the valid output samples should be flushed out.
    - If the input vectors are continuous, the valid output samples also should be continuous, **there must not be any gap at all.**
- The design implementation should be targeted on the ZCU111 FPGA board.
- The implementation should use as minimum resources as possible.
- The minimum Fmax required for the circuit is 200MHz.
- Write a MATLAB reference code and compare the RTL outputs with it.

💼 Considerations

- Use AXIS interface for both the input and output data buses.
- The input sampling rate is 100 Msps.
- Use clock frequency of 100MHz.
- An input vector can have an **'N'** number of IQ samples and every vector end should be indicated with the help of the **'last'** signal in the AXIS interface.
- Use 16 bits signed integers for each real and imaginary portion of the data.

🚚 Deliverables

- Source code implementation of the design.
- Simulation results.
- Resource utilization report analysis.
- Timing report which contains the latency, interval, throughput and the Fmax of the circuit.
- Documentation detailing the design choices, and performance evaluation.