NPTEL Summer Workshop - (Beh.)

Wadhwani Electronics Lab, IIT Bombay

Monday 5th July, 2021

Duration: 2 hrs **Total Marks: 25**

Important instructions

1. This assignment is expected to be attempted using "structural style of modelling" only.
2. Spend enough time to make it compact so that it will be easy for you to describe and debug.
3. You are allowed to use only the components in **Gates.vhdl** and your **own** VHDL descriptions in the experiments/ homework problems so far.
4. Demonstrate your RTL and gate level simulation to your TA using the given tracefile for overall design. You are encouraged to break down your design conveniently (you may have to generate your own tracefiles for sub-parts) to demonstrate the working of the sub parts if necessary. This will help you get partial credits.

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1. Design the logic circuit to meet the specifications as follows (Refer the block schematic on Page 2):
   (a) The circuit has two four bit inputs A(a3a2a1a0) and B(b3b2b1b0) and six bits: $Y(y_5y_4y_3y_2y_1y_0)$ represent the output Y. The Tracefile format is : $A_3A_2A_1A_0B_3B_2B_1B_0 < space > Y_5Y_4Y_3Y_2Y_1Y_0 < space > 111111$
   (b) The unused most significant bits of the output should be made 0 as the case may be.
   (c) Design blocks MUL3, DIV 3,5, XOR AB, INR A, and MUX for the functionalities described as follows:
   - MUL3: Multiply A*3 Marks: 3
   - DIV 3,5: This block outputs the 4-bit input number A that are divisible by 3 **or** 5 **or by both**. The output should be (0000) otherwise. Marks: 2
   - XOR AB: A ExOR B Marks: 1
   - INR A: Increment A(4-bit) by 1. e.g.: INR(1111) = 0000 Marks: 1
   - MUX: selects one of $(I_0, I_1, I_2 and I_3)$ depending on the select lines S_1 and S_0) to the output Y. Note that I_0, I_1, I_2, I_3 and Y are all 6-bit wide. Marks: 2
   - **Note:** Here b_3b_2 are used as select lines for mux are also MSB bits of input B to the functional blocks.
2. Write VHDL description for these blocks. Marks: 12
3. Demonstrate the RTL and Gate Level simulation for **complete** design to your TA using the generic Testbench and the given Tracefile. Marks: 4
4. Upload the zipped handwritten design and Quartus project directory on the website.

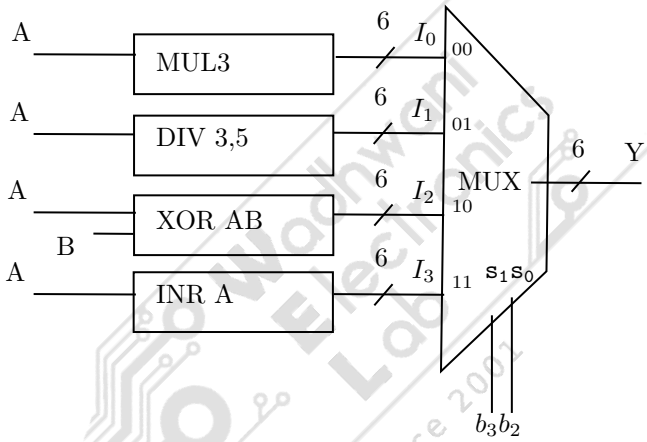

Figure 1: This is a simple block diagram for your understanding.