Homework Probelm:

Design and implement (structural and behavioral) following mealy(overlap) sequence detector

Given input symbols is Σ ={a,b}
output symbols is Λ ={Y,N}

The FSM should outputs a Y at a time instance k only if the last 4 inputs were ***aabb or bbaa***.
Note: On reset input the state should be RST state and output is don't care.

Hints:
step1: Identify different states
step2: Draw state diagram
step3: Use binary encoding of states and write state table
step4: Obtain next state and output equations
step5: Implement Using D flip flops and logic gates (you can use any logic gates)
step6: Write VHDL code in structural
step7: Verify the FSM using simulation
step:8 Verify the same using Virtual Jtag
step9: Implement the VHDL code in behavioral style (from the state diagram) and repeat steps 7 and 8 and Confirm the FSM inferred from the Quartus tool is correct

TRACEFILE format: reset input clock output mask