BANDGAP CURRENT REFERENCE CIRCUIT

TEAM:- ANALOG EDGE

TEAM MEMBERS

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PROBLEM STATEMENT

BGCR-1. Design a Band Gap Current Reference Circuit Using 90nm CMOS Technology with a Nominal Output Current of 100µA.

SPECIFICATIONS

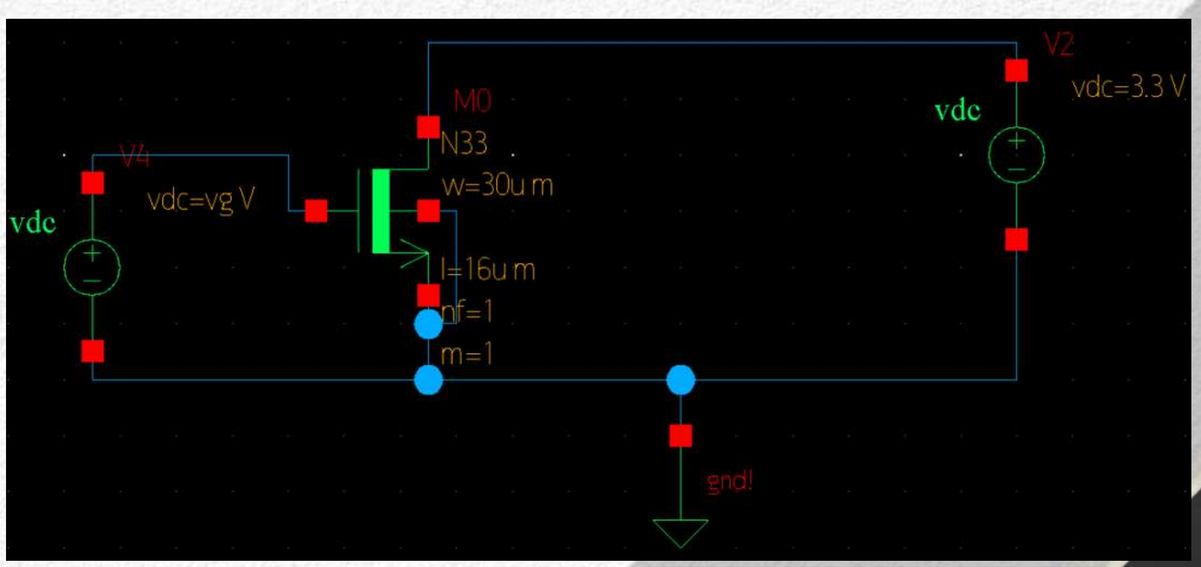
Output Current: 100µA ± 5% across the temperature range of -40°C to 125°C.
Technology: 90nm CMOS process.
Power Supply: 1.8V to 3.3V.
Power Consumption: Less than 50µW for the entire current reference circuit.
Temperature Coefficient: Less than 50 ppm/°C for the output current.
Load Regulation: Output current should remain stable within ±2% when the load voltage varies from 0 to 1V.
Design Considerations: Use a band gap voltage reference to set the bias current and design a current mirror to generate the output current. Explain how process variations, transistor matching, and temperature stability can be managed in the 90nm process.

DESIGN FLOW

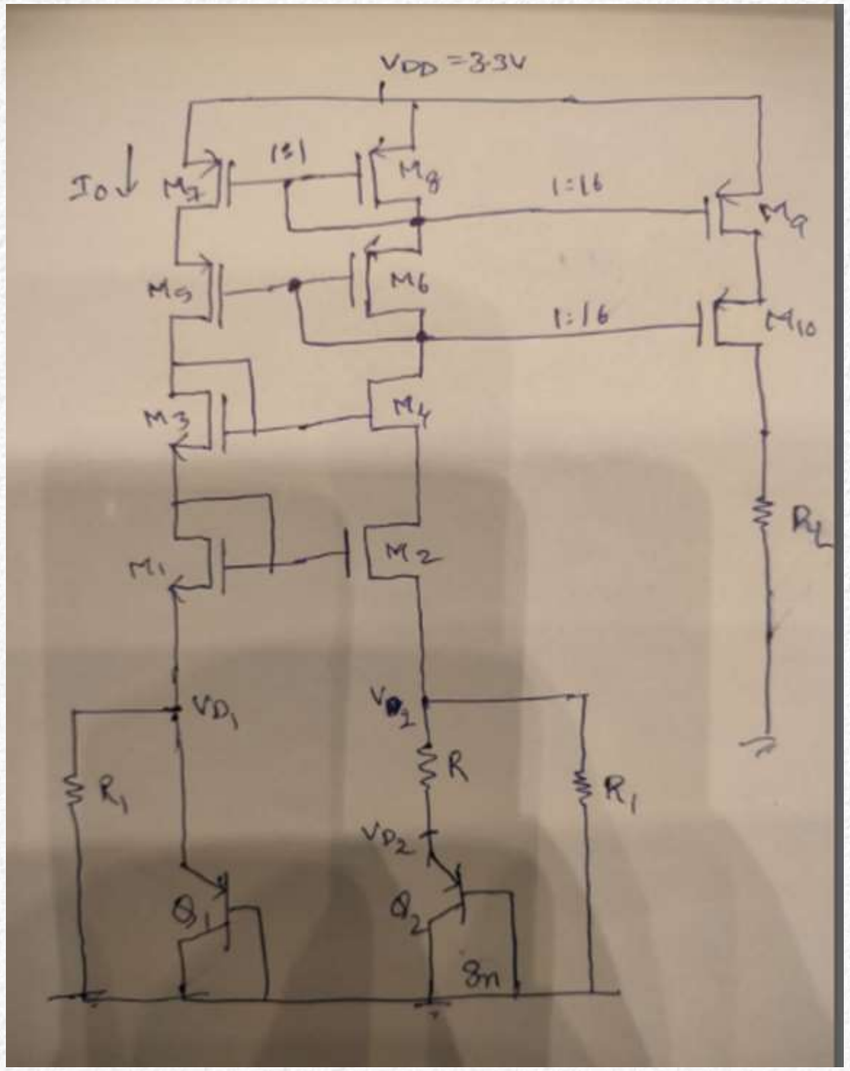
- 1.Charactrization of MOSFET
- 2.Basic premise of PTAT and CTAT
- 3.Schematic and Calculations
- 4.Circuit without startup
- 5.Circuit with startup

Characterization of MOSFET

NMOS_33 Charecterization		
Vthn	0.213146	0.213146
VGsn	1.65	1.65
VGsn-VTH	VOV	1.436854
VOV^2		2.06454942
W	20u	0.00002
L	2u	0.000002
W/L		10
Id	3.95628m	0.00395628
2id		0.00791256
w/l*vov^2		20.6454942
uncox= 2id/{(w/l)vov^2)	383uA/v^2	0.00038326
VG = 1.65, VD = 3.3		



Proposed Circuit



$$Io = I1 + I2$$

$$Io = \frac{Vd1}{R1} + \frac{Vt * \ln(N)}{R} \quad \text{(i)}$$

CTAT PTAT

$$dI0/dT = dVd1/dT * 1/R1 + VT/T * \ln(N/R) = 0 \quad \text{(ii)}$$

The target power spec is 50µW so we targeted for 45µW thus the branch current is around 6.7µA.
To generate 100 µA output, we set each branch to 6.25 µA and use a current mirror to scale it accordingly. Thus we will equate I0 current to 6.25µA.

Now putting all the values and solving both equation (i) and (ii) we will get,

R = 20.413KΩ, R1 = 193.6KΩ

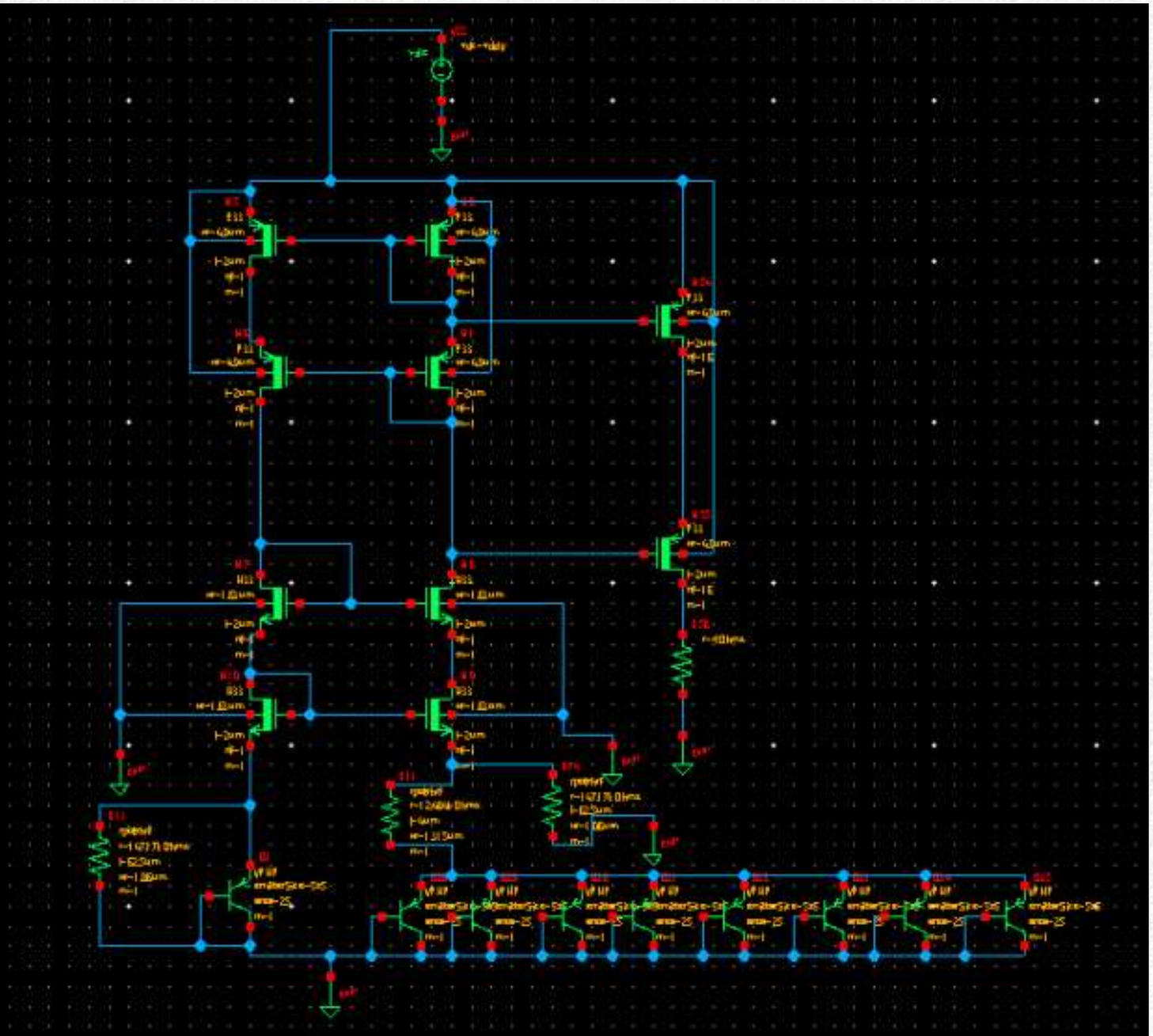
NOTE:-

Assuming M1-M2 ,M3-M4 , M5-M6 and M7-M8 are identic
For id1 =id2: VD1=V2
To make id1= id2 , we put M1 R1 gnd, M2 R1 gnd
why folded cascode? For strong current sources. Have high output impedance

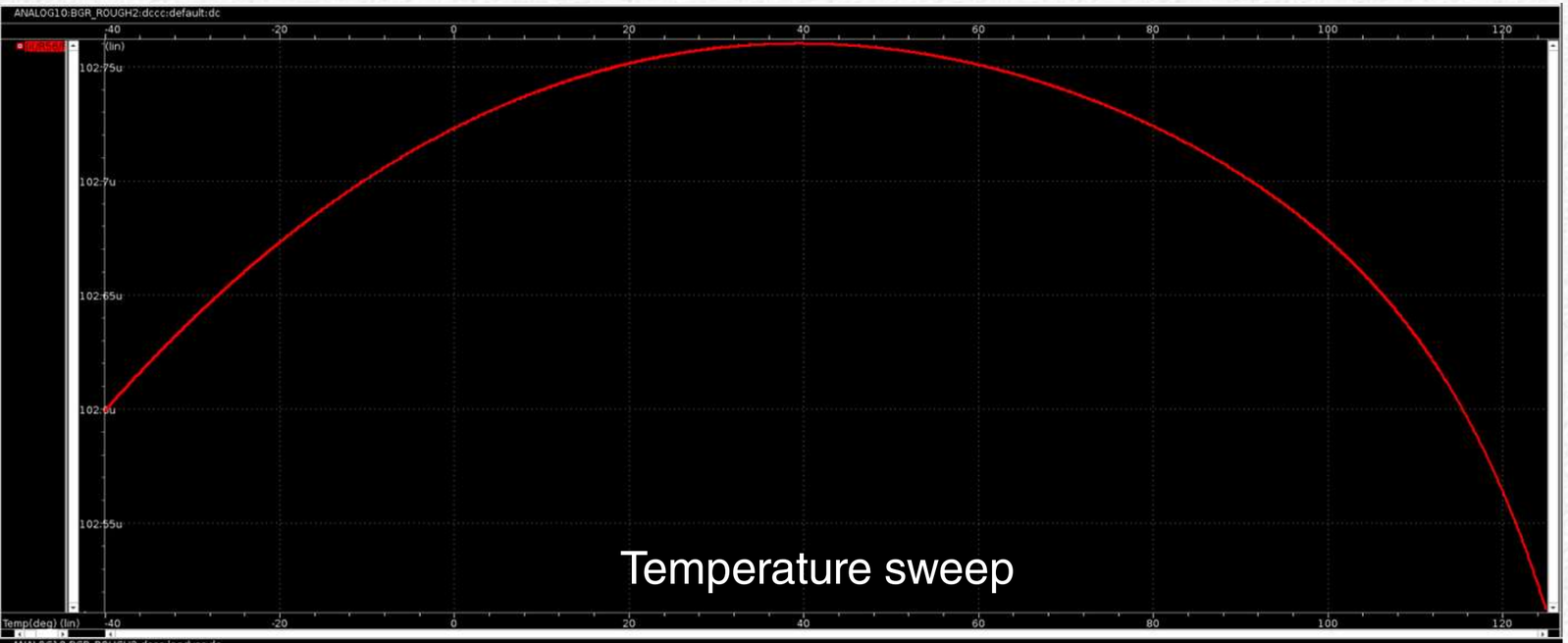
Calculation

Iout	100u	1.00E-04				
Io	Iout/16	6.25E-06				
VBE	0.47	0.47				
Io=I2,I4,I6,I8	I in R + I in R1					
6.25u	VBE1/R1+ VTln(n)/R		VBE1/(9.48*R)+VTln(n)/R= 6.25u			
dIo/dT=0	-1.7m * 1/R1 + k/q ln(n)/R					
	-1.7m * 1/R1 + VT/T ln(n)/R = 0		1.7m * 1/R1 = (VT/T) {ln(n)/R }			
VT	0.02586	0.02586				
T	300Kelvin	300				
n	8	8				
ln8		2.07944154				
VT/T		0.0000862	86u			
Why n=8? so that q2 will be around q1 in layout				IMIN	IMAX	Io(27)
VT/T * ln(n)						0.000103
R/R1	{VT/T} *{ln(n)/1.7m}	0.0814763		delta I	2.4391E-07	
R1/R		12.2735077		DELTAT	165	
VT*ln(n)		0.05377436		TC=	1.43512E-05	
R	VBE1/(9.48*6.25u)+VTln(n)/6.25u= R	1.47E+04	20.4K			
R1		1.81E+05	194k			
Assume Vov2,1		0.2				
L		0.000002				
vov^2		0.04				
uncox*Vov^2		0.00001532				
(w/l)1,2,3,4	(w/L)1,2= 2id/{(uncox)vov^2)	8.16E-01				
(w/l)5,6,7,8	(w/l)5,6,7,8= 3* (w/l)1,2,3,4	2.45E+00				
(w)1,2,3,4	w/l*L	1.63E-06				
(w)5,6,7,8	w/l*L	4.90E-06				
(w)9,10	16*(w)5,6,7,8	7.83E-05				
Assume RL	10K					

Circuit without Startup



SIMULATIONS



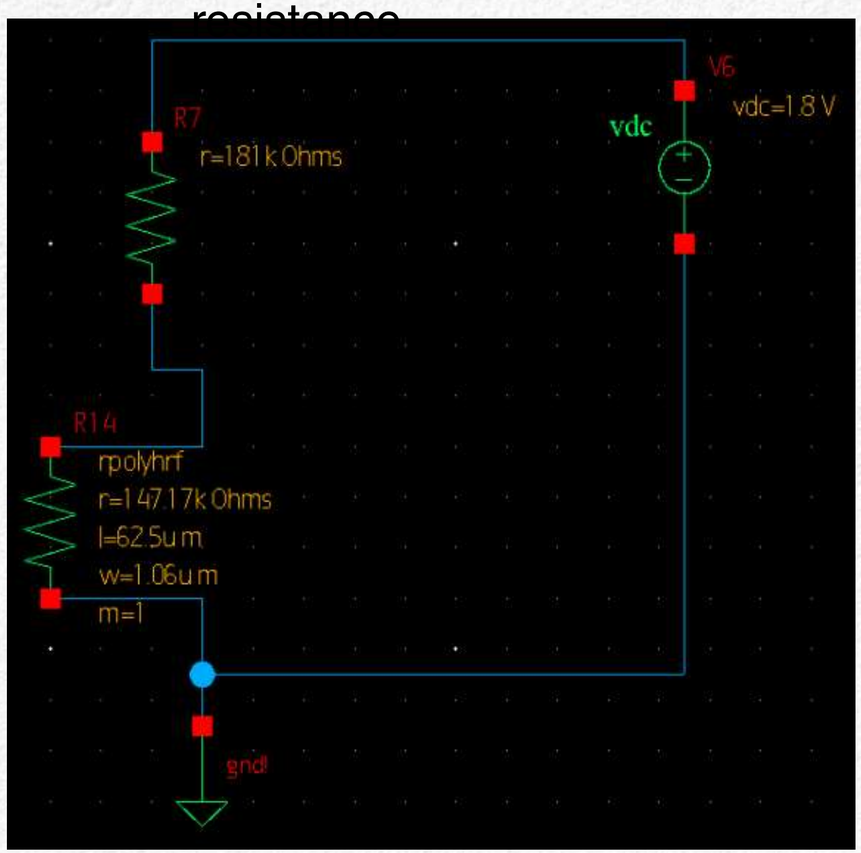
Temperature sweep

Load resistance sweep

Nominal value

i(/R5/PLUS) dc	i(/R56/PLUS) dc_op	PLUS, analysisN…e=dc))- ymin(i(, dc	dc	ppm dc
Filter	Filter	Filter	Filter	Filter
	102.757u	102.757u	248.03n	14.6289u

Matching foundry resistance



Nominal value

i(/R5...) dc	i(/R56/PLUS) dc_op	PLUS, analysisN...e=dc))- ymin(i(, dc	dc	ppm dc
Filter	Filter	Filter	Filter	Filter
	102.757u	102.757u	248.03n	14.6289u

Observations

(1) Given, to achieve 100 mA ± 5%, across -40°C to 125°C

Our spec → Iout = 102.757 mA ± 0.279 mA

(Nominal value @ 27°C)

= 102.757 mA ± 0.24%

(Imin = 102.5125 mA)

(Imax = 102.76 mA)

1.8V →

101.946 = Imax

96.6 = Imin

Tc = ΔI / (ΔT * Inominal)

(2) Temp. Coefficient (for 3.3V → 14.6289 ppm)

Tc = ΔI / (ΔT * Inominal)

(3) Load Regulation (@ 27°C)

1.8V → RL = 1Ω, VL = 0 → Iout = 100.918 mA

RL = 10kΩ, VL = 1V → Iout = 100.8 mA

3.3V → RL = 1Ω, VL = 0 → Iout = 102.901 mA

RL = 10kΩ, VL = 1V → Iout = 102.75+ mA

When load varies from 0V–1V (for 1.8V)

Iout varies from 100.918 mA to 100.8 mA

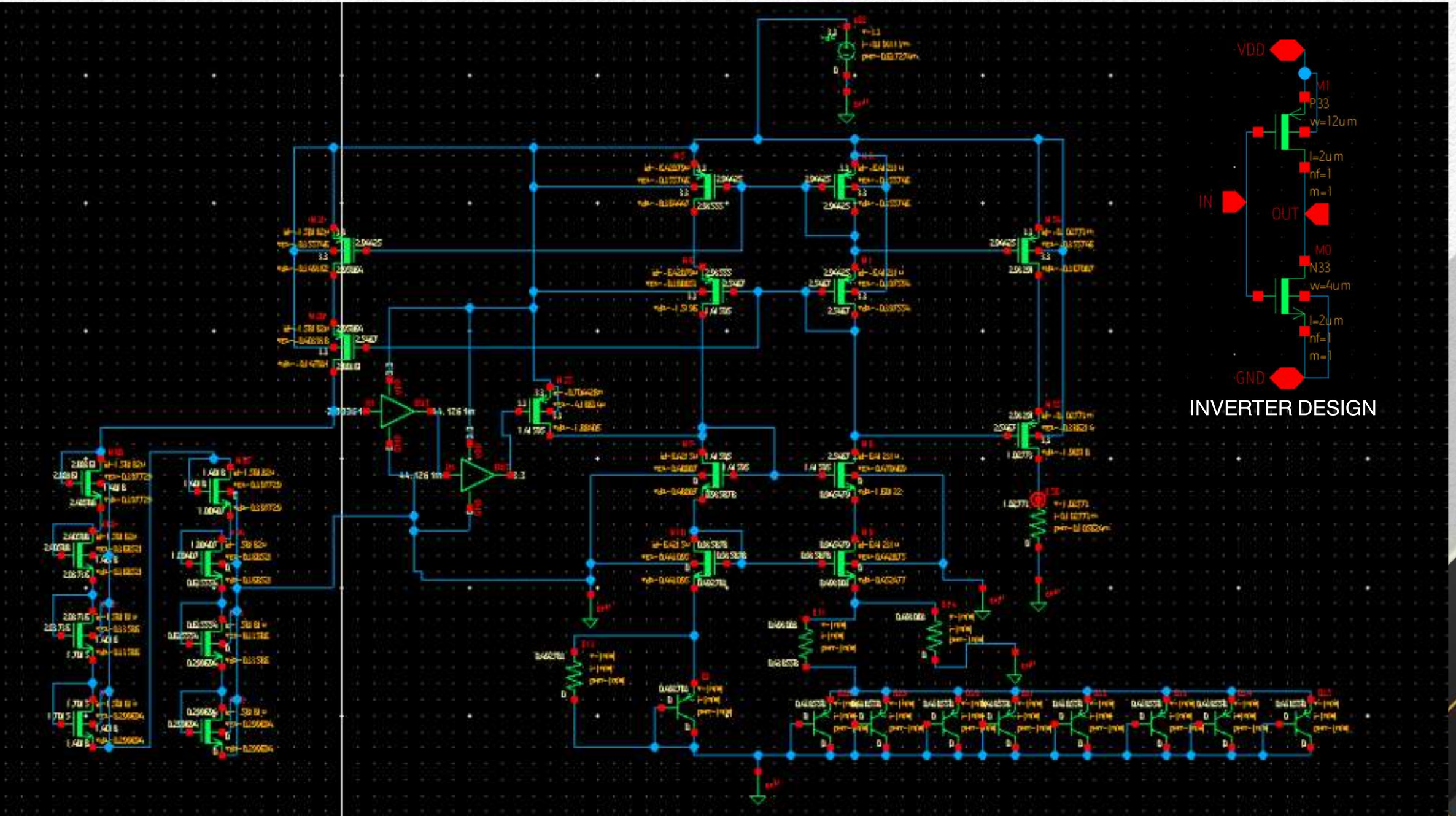
for (3.3V) → Iout varies from 102.901 mA to 102.757 mA

(4) Power Consumption

P = Vdd * (Id)

= 3.3 * (6.41974 * 2 * 10^-3) = 42.350244 mW< 50 mW

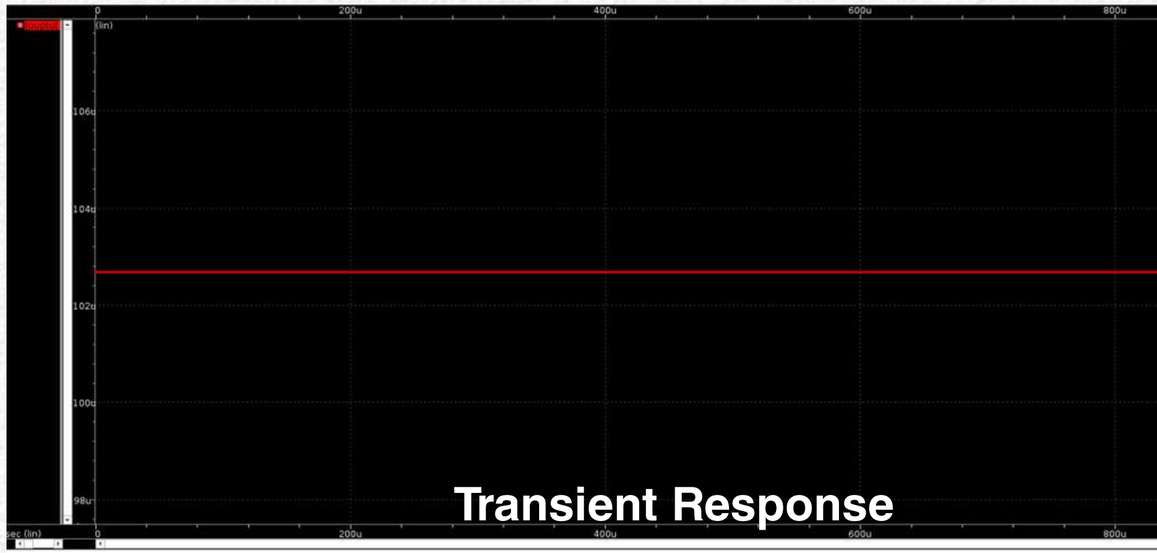
Circuit with Startup



INVERTER DESIGN

SIMULATIONS

Temperature sweep



Transient Response

Load resistance
sweep

THANK YOU