

# BANDGAP CURRENT REFERENCE CIRCUIT FOR ECG ACQUISITION SYSTEMS

TEAM:- ANALOG EDGE

## TEAM MEMBERS

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# PROBLEM STATEMENT

**BGCR-1. Design a Band Gap Current Reference Circuit Using 90nm CMOS Technology with a Nominal Output Current of 100 $\mu$ A.**

## SPECIFICATIONS

**Output Current:**  $100\mu\text{A} \pm 5\%$  across the temperature range of -40°C to 125°C.

**Technology:** 90nm CMOS process.

**Power Supply:** 1.8V to 3.3V.

**Power Consumption:** Less than 50 $\mu$ W for the entire current reference circuit.

**Temperature Coefficient:** Less than 50 ppm/°C for the output current.

**Load Regulation:** Output current should remain stable within  $\pm 2\%$  when the load voltage varies from 0 to 1V.

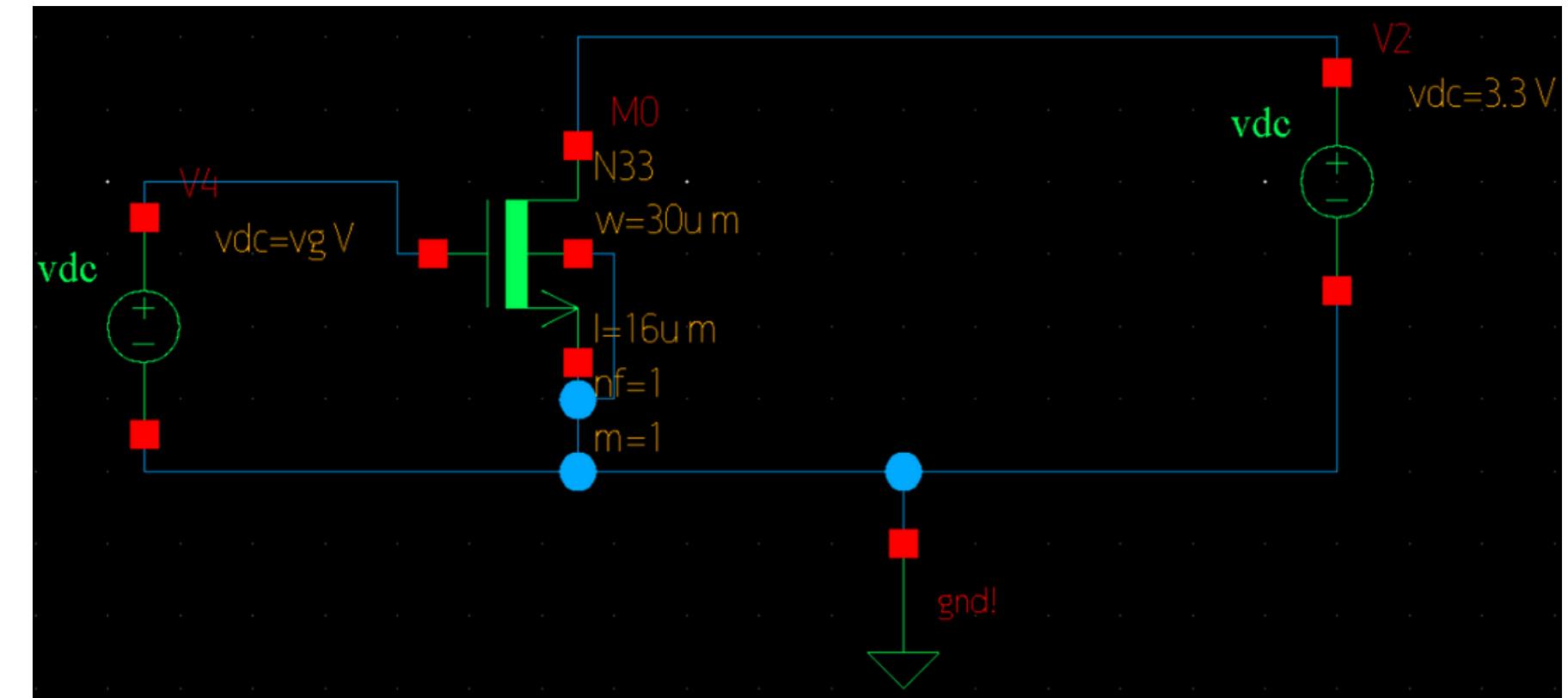
**Design Considerations:** Use a band gap voltage reference to set the bias current and design a current mirror to generate the output current. Explain how process variations, transistor matching, and temperature stability can be managed in the 90nm process.

# DESIGN FLOW OF PROPOSED CIRCUIT

1. Charactrization of MOSFET
2. Basic premise of PTAT and CTAT
3. Schematic and Calculations
4. Circuit without startup
5. Circuit with startup
6. Circuit w/o startup for layout optimization & Testing
7. Pre-Layout Simulation Layout Design
8. Post-Layout Simulation

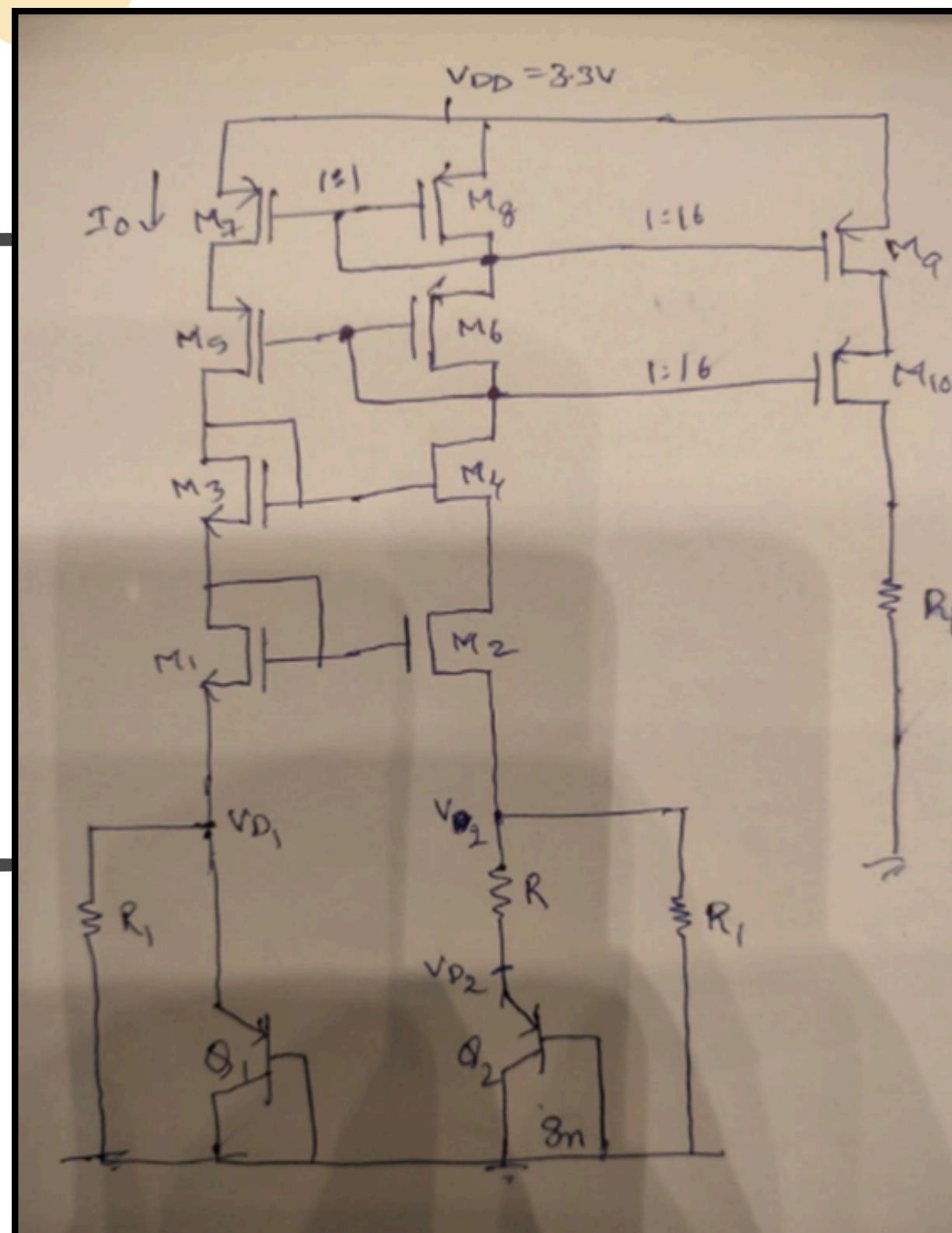
# Characterization of MOSFET

NMOS_33 Characterization			
V <sub>thn</sub>		0.213146	0.213146
V <sub>Gsn</sub>		1.65	1.65
V <sub>Gsn</sub> -V <sub>TH</sub>	V <sub>OV</sub>		1.436854
V <sub>OV</sub> <sup>2</sup>			2.0645494
W	20u		0.0000
L	2u		0.00000
W/L			10
I <sub>d</sub>	3.95628m		0.00395628
2I <sub>d</sub>			0.00791256
w/l*vov <sup>2</sup>			20.645494
uncox = 2id/{(w/l)vov <sup>2</sup> }	383uA/v <sup>2</sup>		0.00038326
VG = 1.65, VD = 3.3			



## Figure:- Schematic of NMOS

# Proposed Circuit



$$I_O = I_1 + I_2$$

$$I_O = \frac{V_{d1}}{R_1} + \frac{V_t * \ln(N)}{R} \quad (i)$$

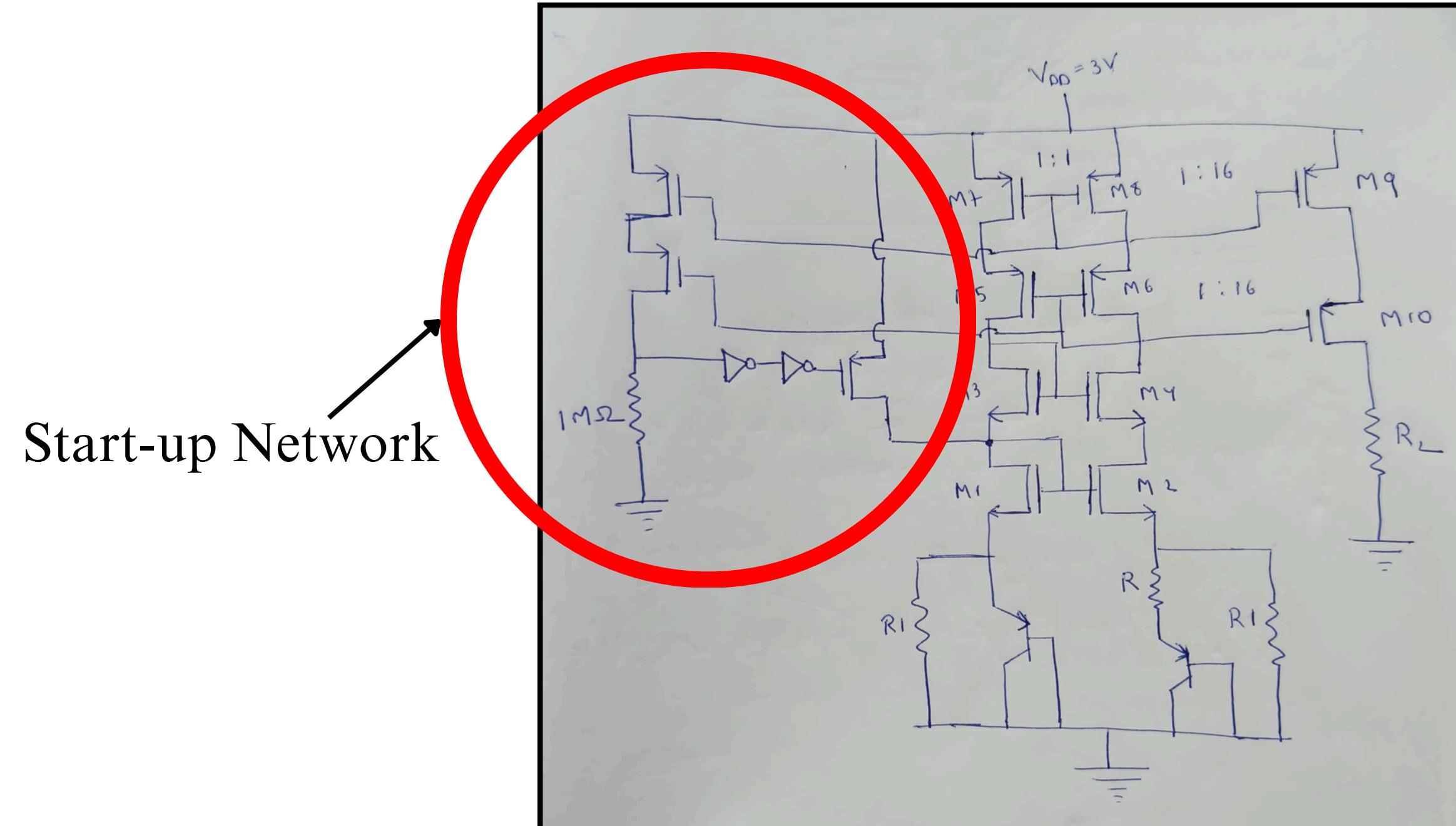
↑  
CTAT                            PTAT

$$\frac{dI_O}{dT} = \frac{dV_{d1}}{dT} * \frac{1}{R_1} + \frac{V_T}{T} * \ln\left(\frac{N}{R}\right) = 0 \quad (ii)$$

Why  $n=8$ ?

So, that  $q_1$  will be surrounded  $q_2$  in layout.

# Proposed Circuit with Start-up



# Calculations

Iout	100u	1.00E-04			
Io	Iout/16	6.25E-06			
VBE	0.47	0.47			
Io=I2,I4,I6,I8	I in R + I in R1				
6.25u	VBE1/R1+ VTln(n)/R	VBE1/(9.48*R)+VTln(n)/R= 6.25u			
dIo/dT=0	-1.7m * 1/R1 + k/q ln(n)/R				
	-1.7m * 1/R1 + VT/T ln(n)/R = 0	1.7m * 1/R1 = (VT/T) {ln(n)/R }			
VT	0.02586	0.02586			
T	300Kelvin	300			
n	8	8			
In8	2.07944154				
VT/T	0.0000862	86u			
Why n=8? so that q2 will be around q1 in layout			IMIN	IMAX	Io(27)
VT/T * ln(n)					0.000103
R/R1	{VT/T} *{ln(n)/1.7m}	0.0814763	delta I	2.4391E-07	
R1/R		12.2735077	DELTAT	165	
VT*ln(n)		0.05377436	TC=	1.43512E-05	
R	VBE1/(9.48*6.25u)+VTln(n)/6.25u= R	1.47E+04	20.4K		
R1		1.81E+05	194k		
Assume Vov2,1		0.2			
L		0.000002			
vov^2		0.04			
uncox*Vov^2		0.00001532			
(w/l)1,2,3,4	(w/L)1,2= 2id/{(uncox)vov^2}	8.16E-01			
(w/l)5,6,7,8	(w/l)5,6,7,8= 3* (w/l)1,2,3,4	2.45E+00			
(w)1,2,3,4	w/l*L	1.63E-06			
(w)5,6,7,8	w/l*L	4.90E-06			
(w)9,10	16*(w)5,6,7,8	7.83E-05			

**NOTE:-  $L = 2\mu m$**  choosen so, that our channel length modulation is negligible and high impedance.

The target power spec is  $50\mu\text{W}$  so we targeted for  $45\mu\text{W}$  thus the branch current is around  $6.25\mu\text{A}$ .

To generate  $100 \mu\text{A}$  output, we set each branch to  $6.25 \mu\text{A}$  and use a current mirror to scale it accordingly. Thus we will equate  $I_0$  current to  $6.25\mu\text{A}$ .

Now putting all the values and solving both equation (i) and (ii) we will get,

$$\mathbf{R = 20.413K\Omega, R1 = 193.6K\Omega}$$

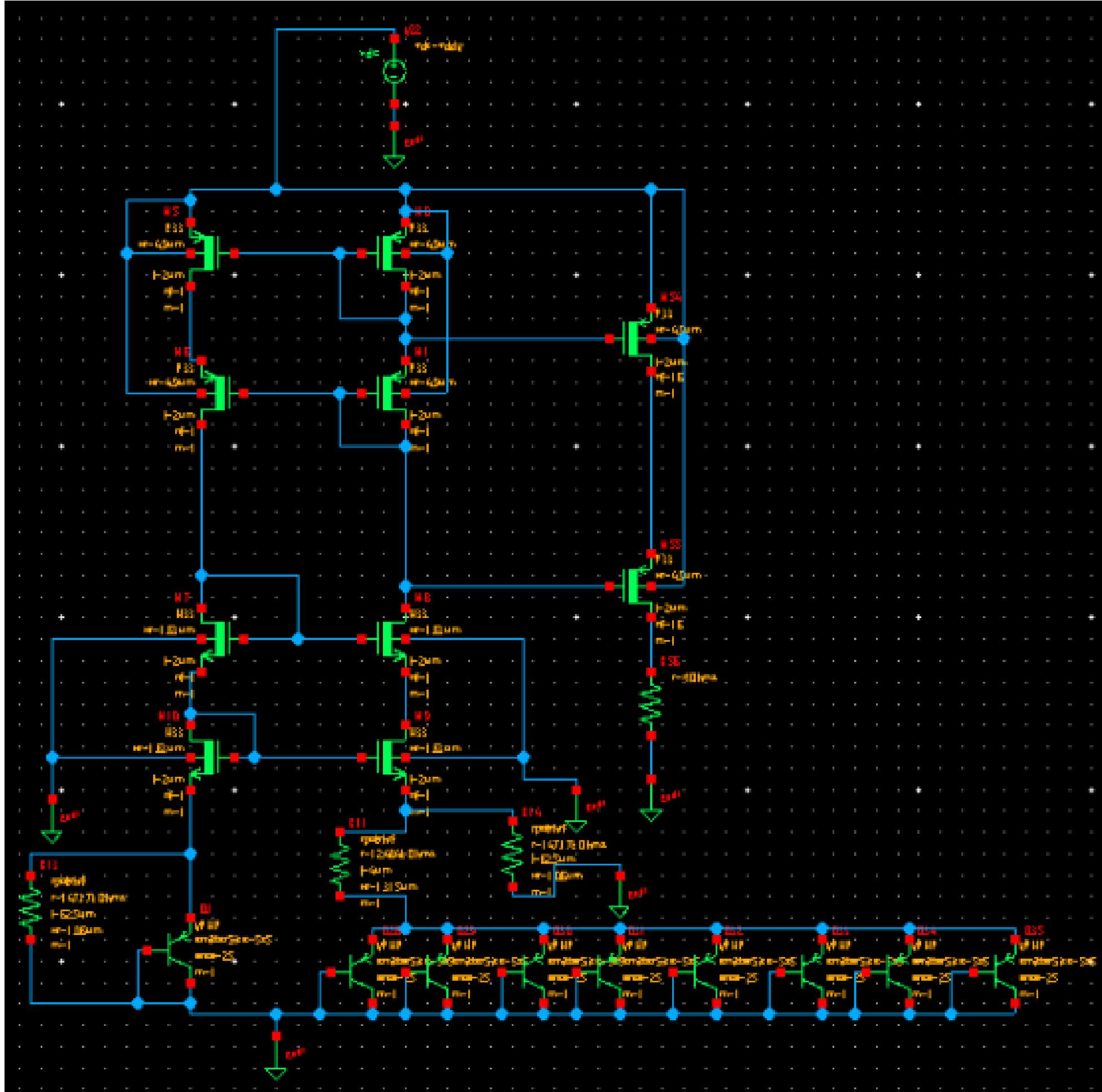
### NOTE:-

Assuming M1-M2 ,M3-M4 , M5-M6 and M7-M8 are identical

For  $i_{d1} = i_{d2}$ :  $V_{D1} = V_2$

To make  $i_{d1} = i_{d2}$ , we put M1 R1 gnd, M2 R1 gnd

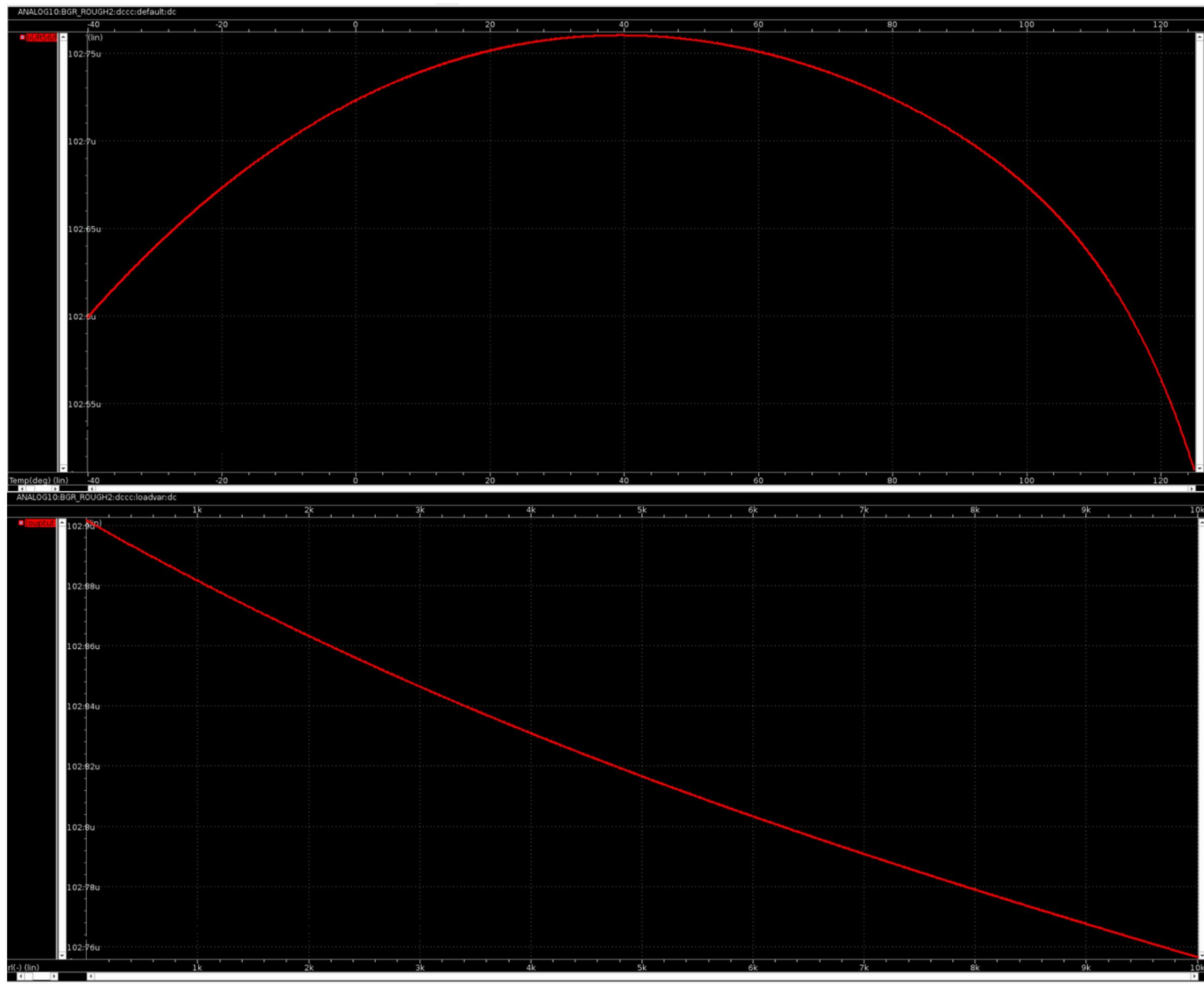
# Circuit without Startup



## Why folded cascoding structure used?

We use a folded cascode structure to achieve a nearly ideal current source by improving output resistance, enhancing gain, and allowing for a wider input common-mode range while maintaining low voltage operation.

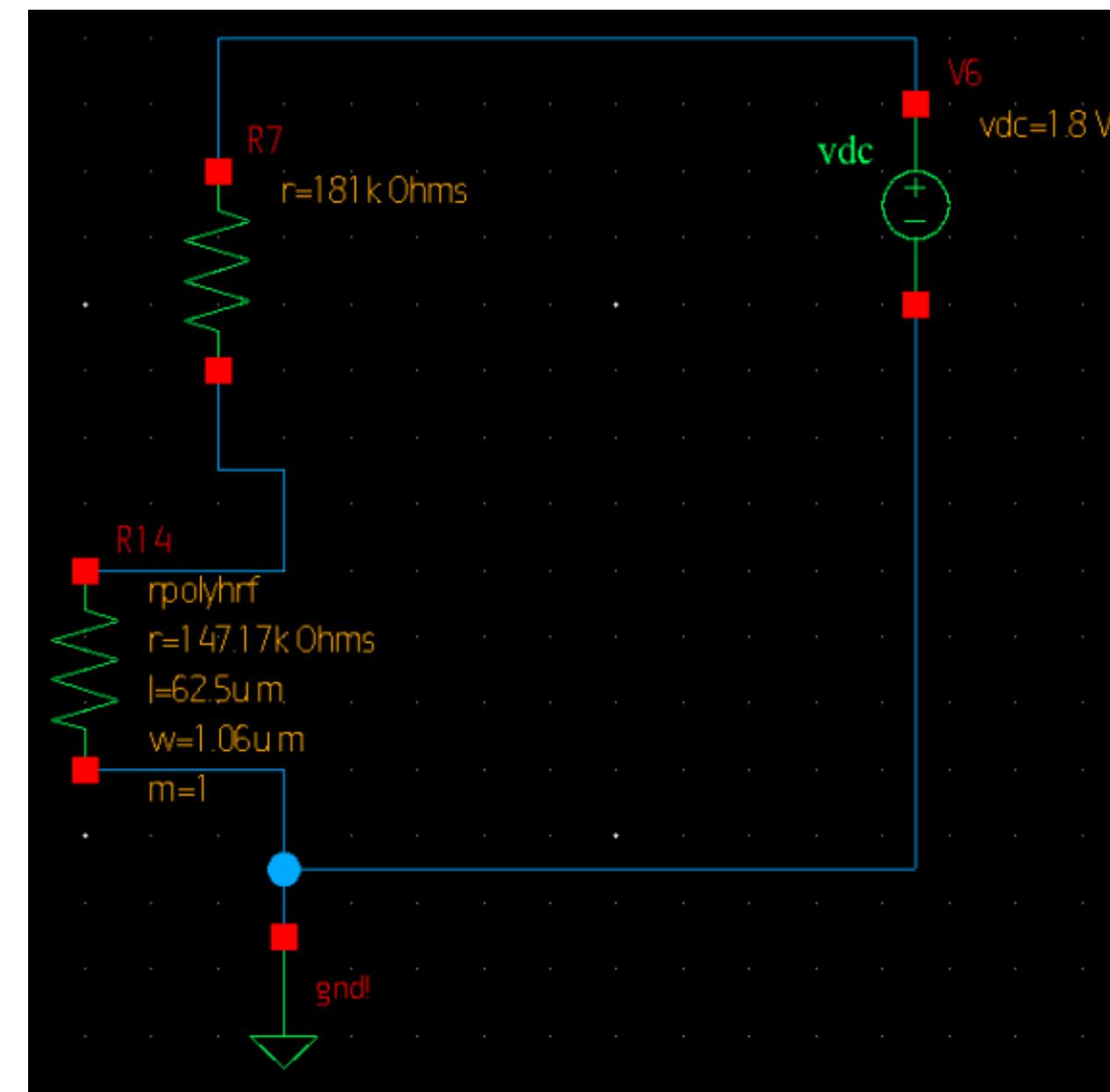
# SIMULATIONS



## Nominal value

i(R56/PLUS) dc	i(R56/PLUS) dc_op	PLUS, analysisN <i>i</i> e=dc))-ymin(i() dc	ppm dc
Filter 	102.757u	102.757u	248.03n 14.6289u

## Matching with foundry resistance



# Observations

(1)

Output Current		
Imin(µA)	Imax(µA)	Inominal(µA)
102.5125	102.76	102.757

$$T_c = \Delta I / (\Delta T * Inominal)$$

Temp Coefficient = 14.6289 ppm

(2)

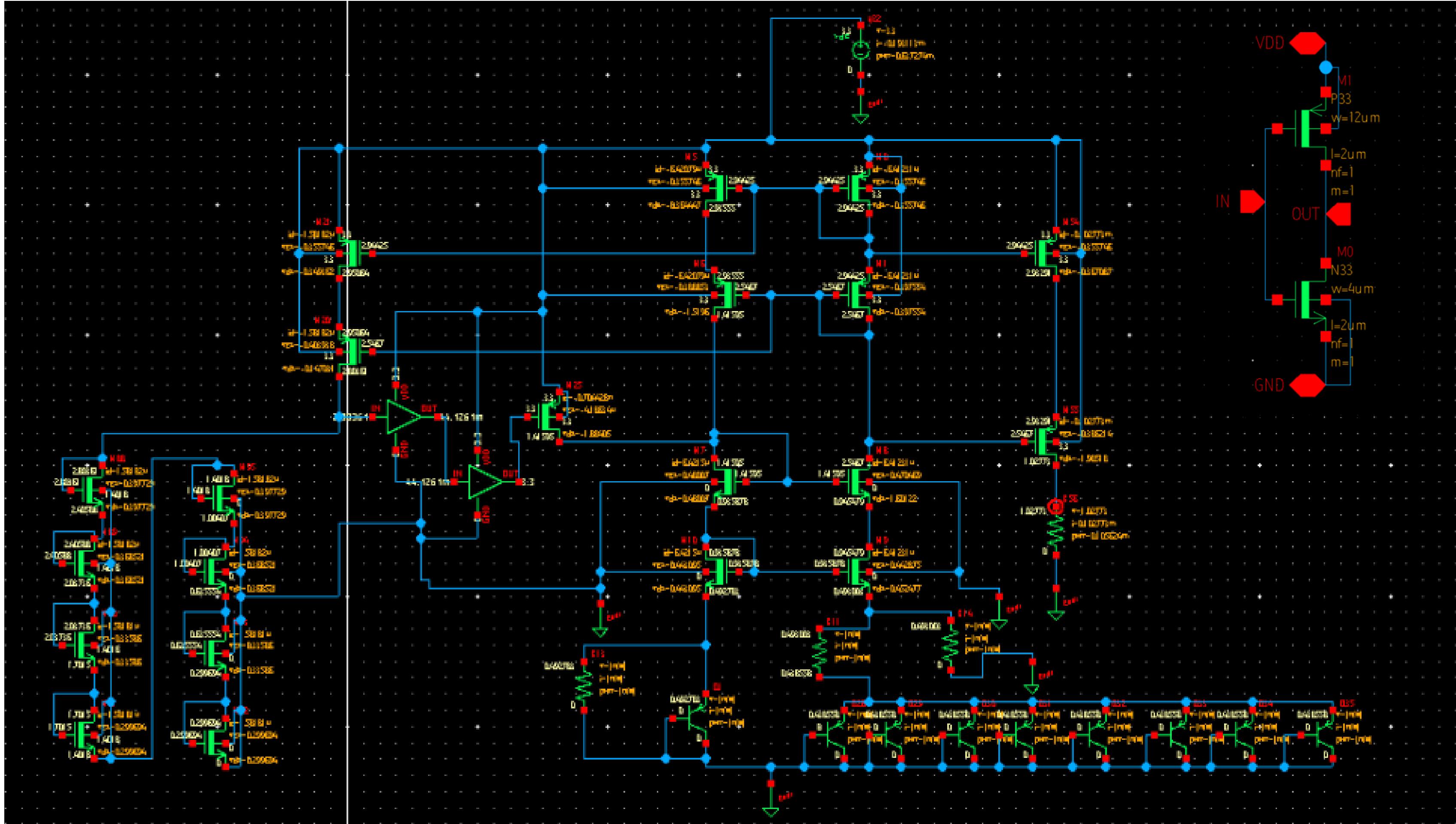
Load Regulation @ 3.3V	
RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)
Iout(max) = 102.901 µA	Iout(min) = 102.757 µA

(3) Power Consumption

$$P = Vdd * (Id)$$

$$= 3.3 * (6.41974 * 2 * 10^{-3}) = 42.350244 \mu W < 50 \mu W$$

# Schematic of Circuit with Startup



# Parameters of Different components

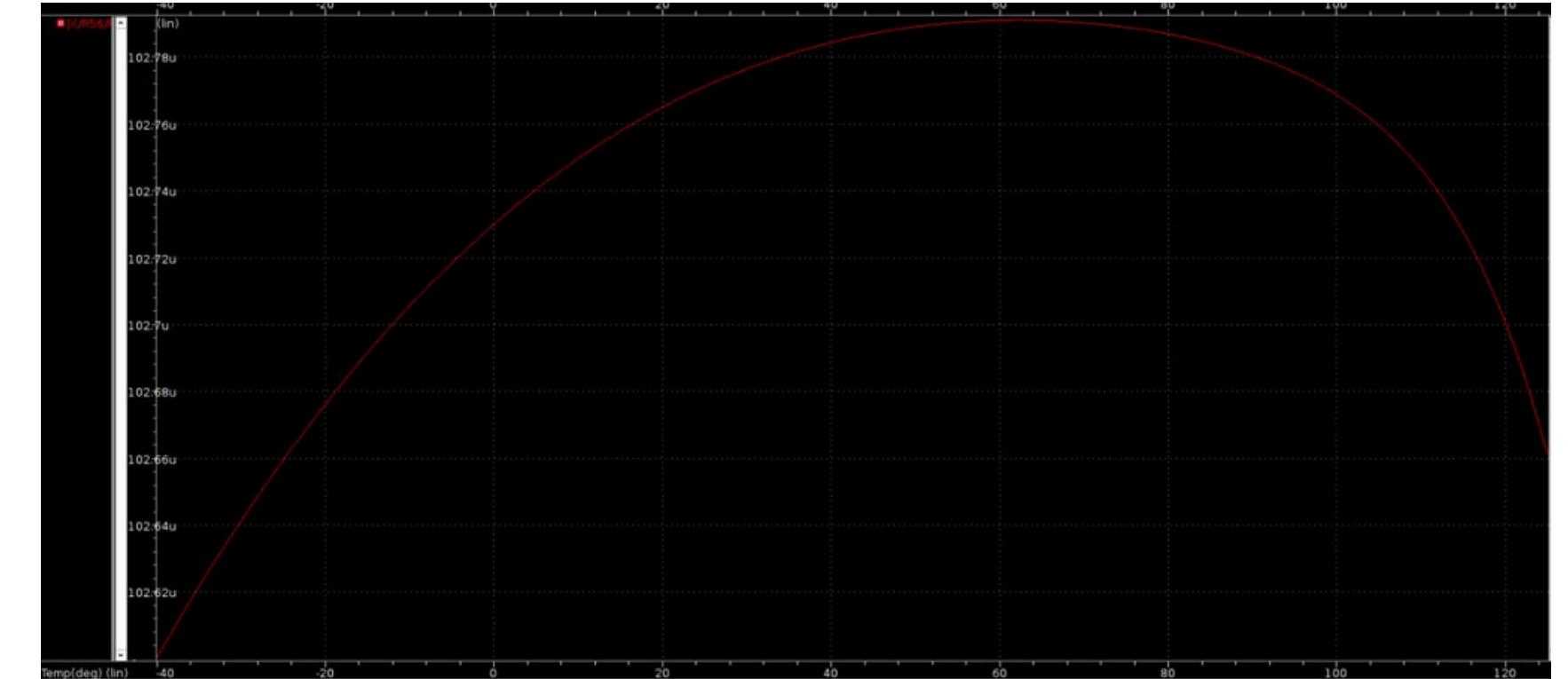
Component	W( $\mu\text{m}$ )	L( $\mu\text{M}$ )	Multiplier
M7, M8, M5, M6	2.45	2	2
M9, M10	2.45	2	32
M3, M4, M1, M2	0.815	2	2
M21, M20	1.63	2	1
M22 - M30	1.63	2	1
M31	4.9	2	1
R(rpoluhrf)	1.315	4	1
R1(rpoluhrf)	In multiples of $r = 12.484\text{k}\Omega$		
Q1 - Q9	5	5	1
Inverter			
M0	4	2	1
M1	12	2	1

INVERTER DESIGN

# SIMULATIONS

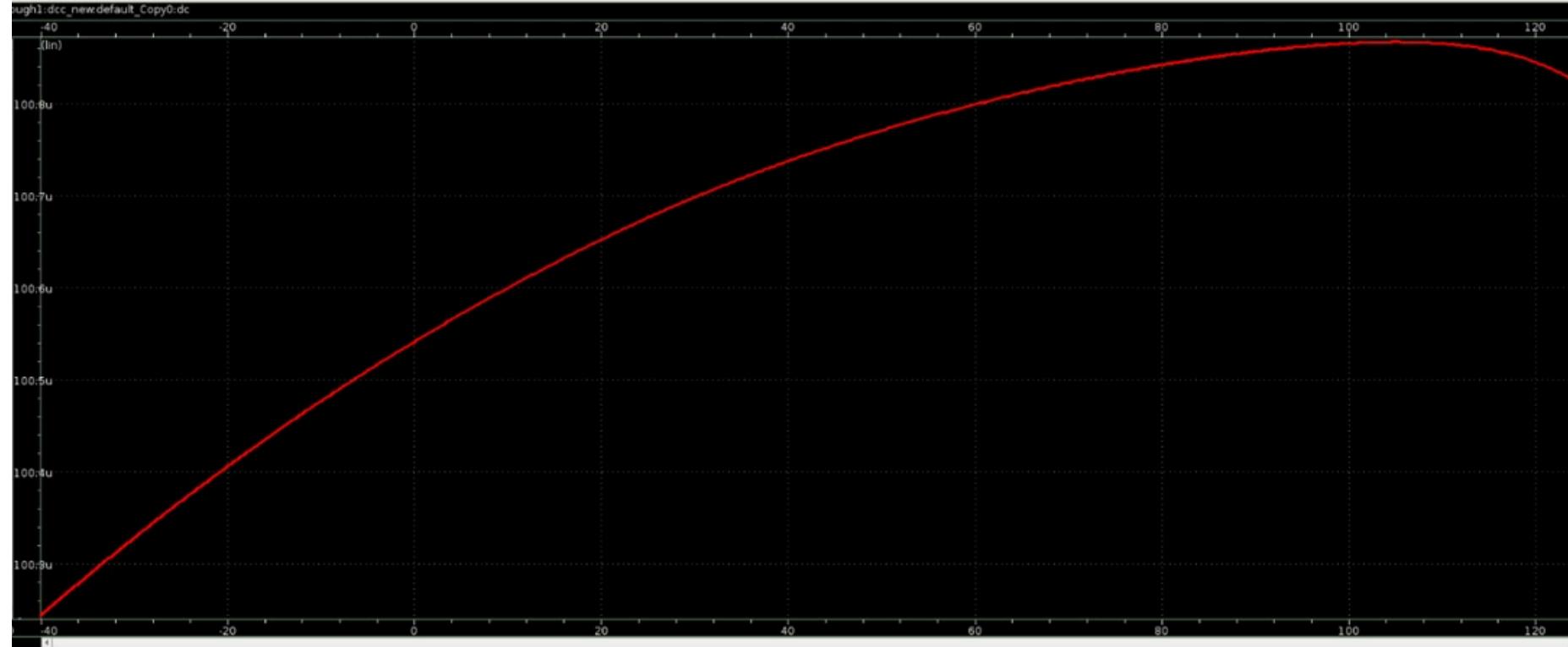
Pre Layout

Temperature sweep

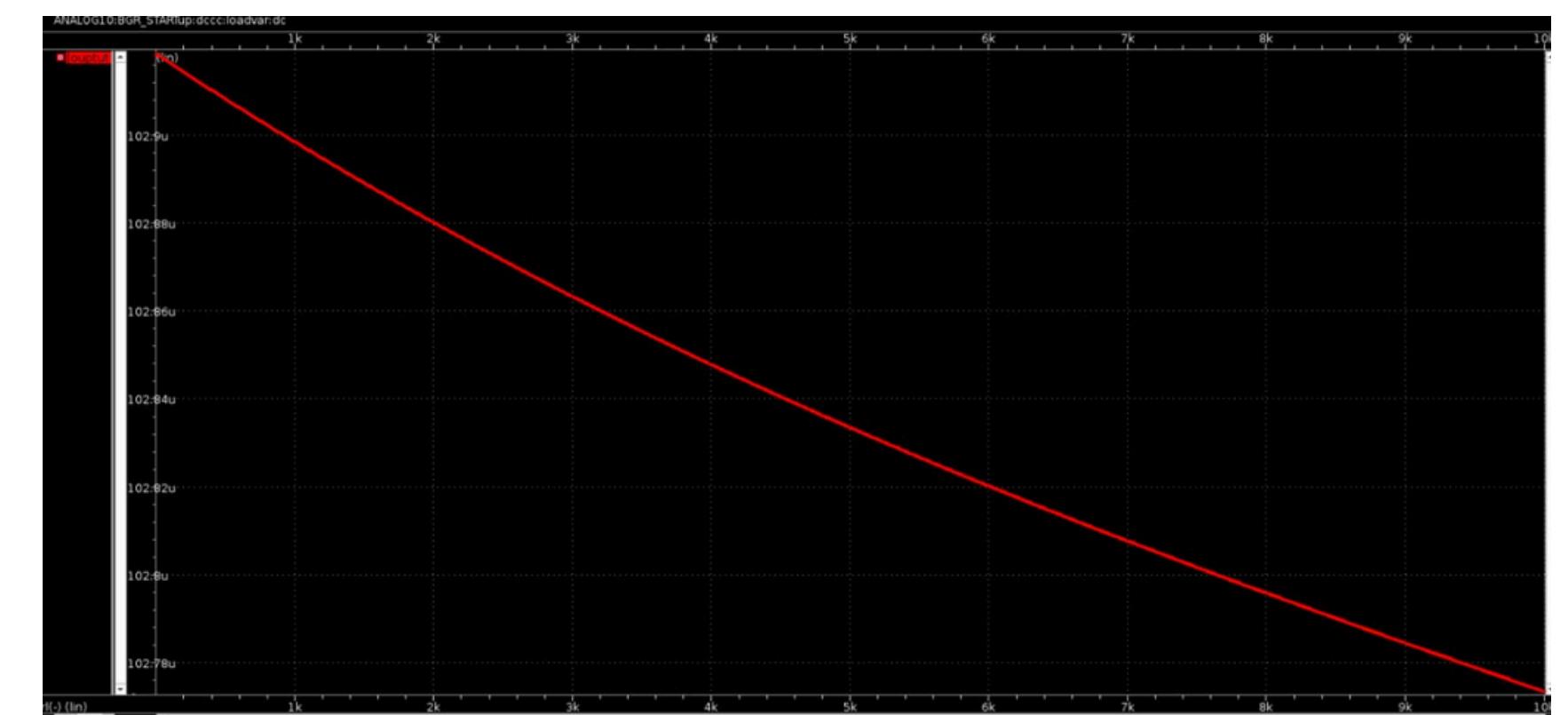


Post Layout

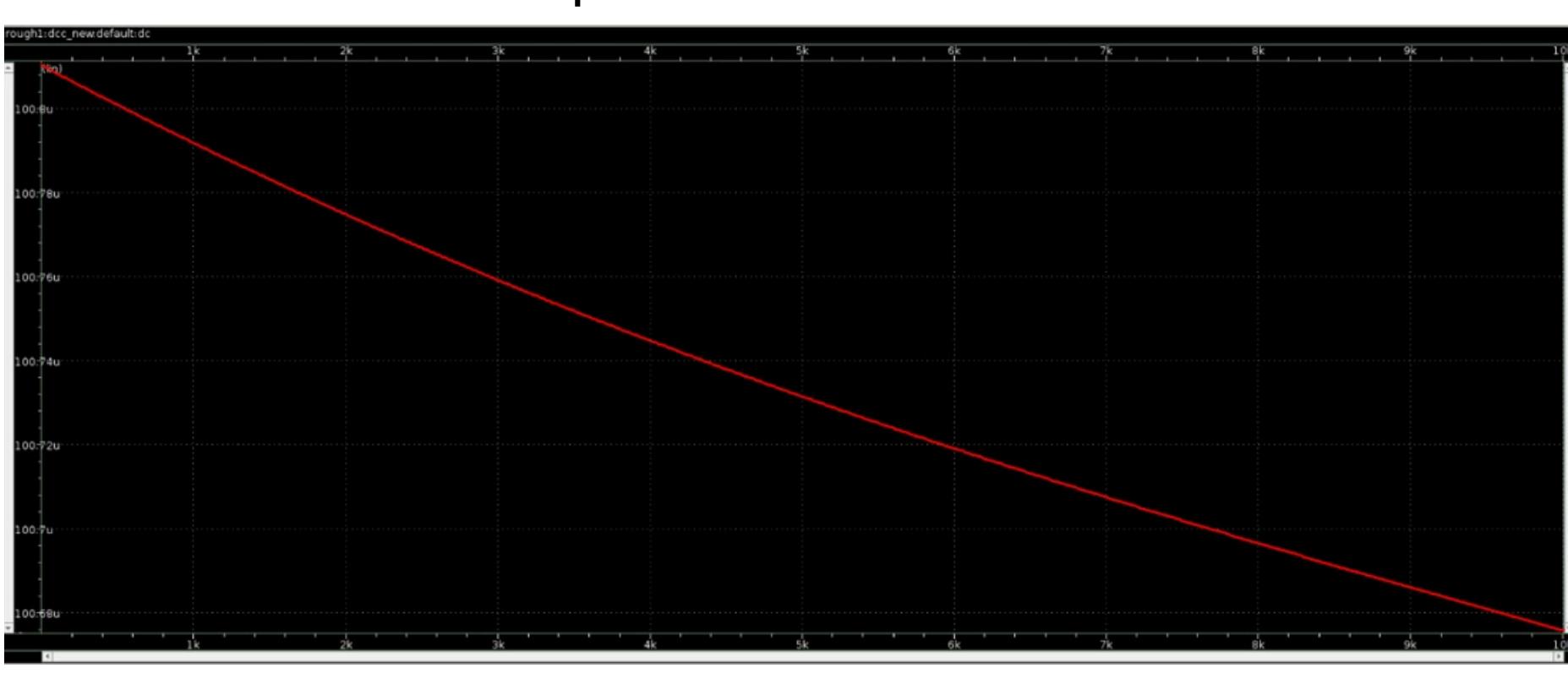
Temperature sweep



Load resistance sweep

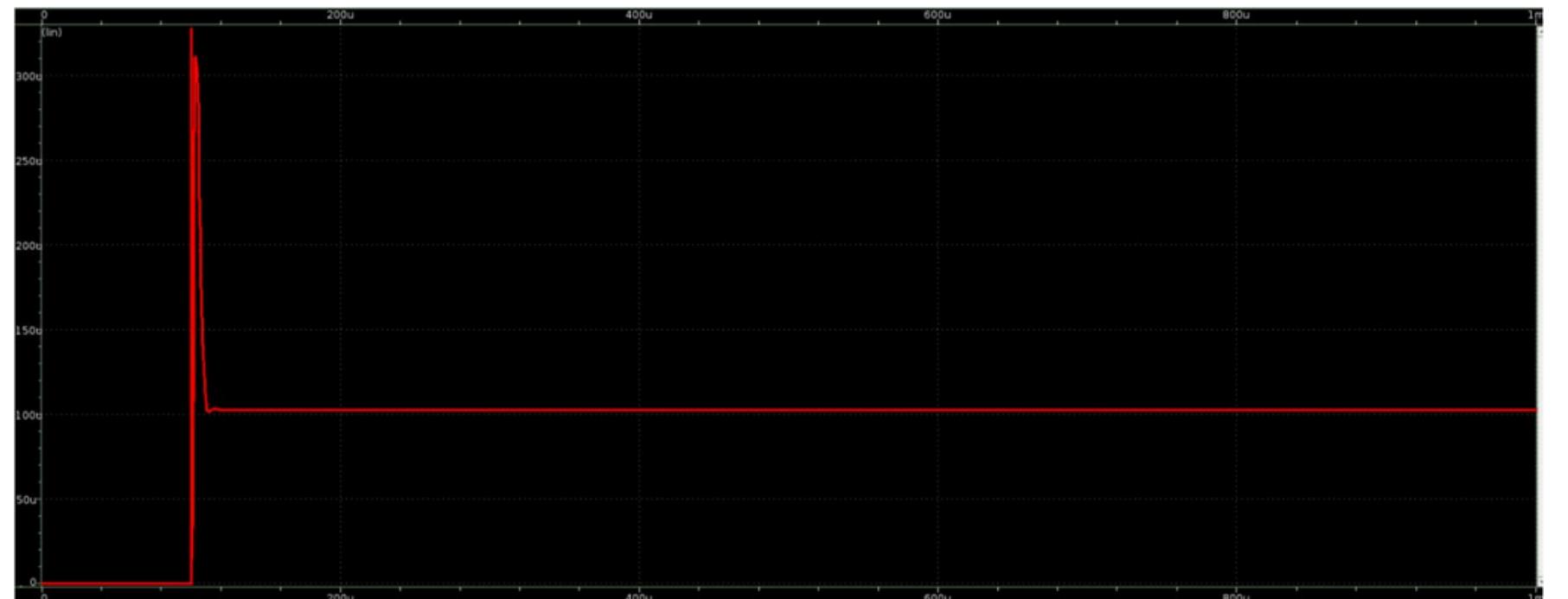


Load resistance sweep



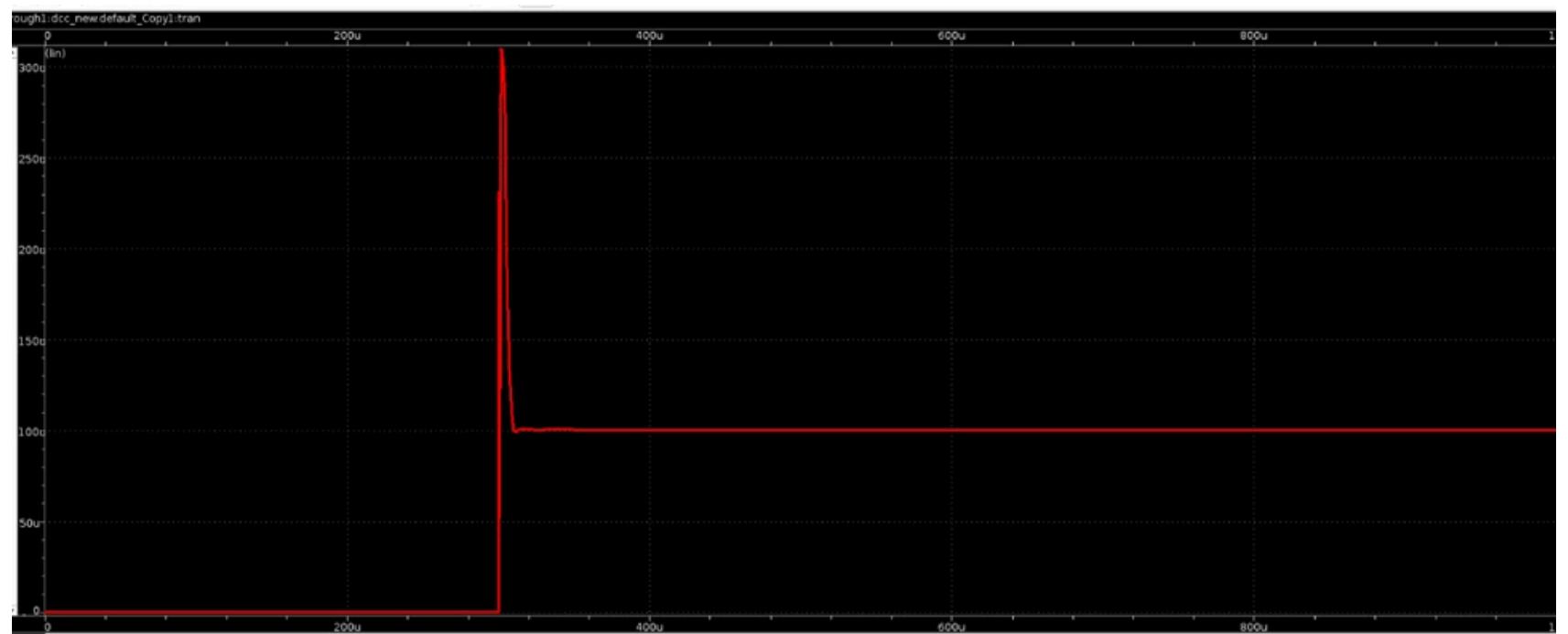
# Transient Analysis

Pre Layout



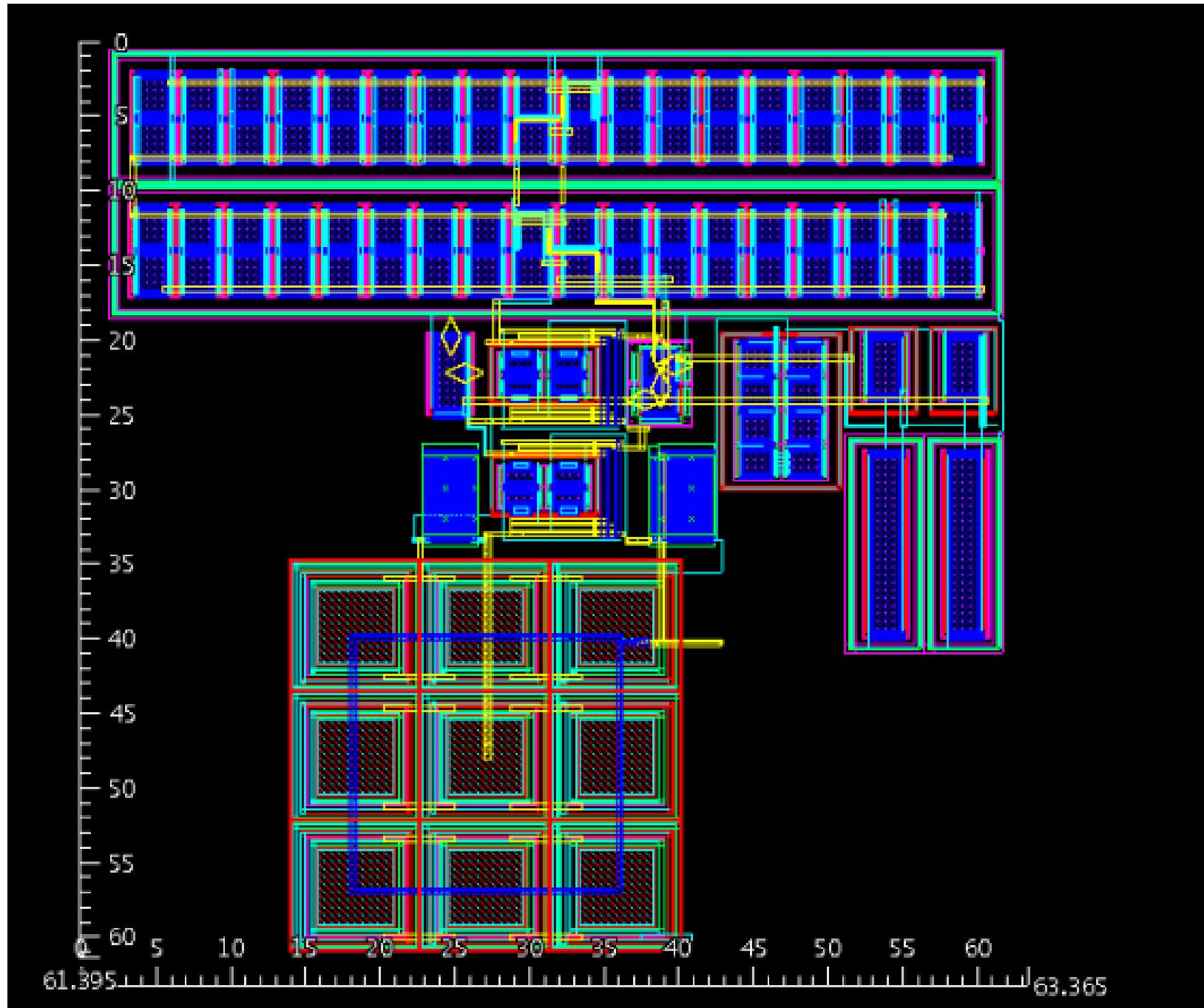
The settling time is  $11.768\mu$  sec.

Post Layout



The settling time is  $11.757\mu$  sec.

# LAYOUT



## Key Features of our Layout:-

1. Common centroid layout for BJT and MOSFET .  
-A common centroid layout minimizes mismatch due to process variations, thermal gradients, and stress effects. It ensures better device matching, improving accuracy in precision analog circuits.
2. Multiplier for MOSFET.
3. Area is less than  $(63 \times 63)\mu\text{m}^2$  with start -up.

Fig:- The Final Floorplanning of the Circuit with Start-up

# Observations

Pre Layout

Output Current		
Imin(µA)	Imax(µA)	Inominal(µA)
102.704	102.929	102.898

$$T_c = \Delta I / (\Delta T * Inominal)$$

Temp Coefficient = 13.36 ppm

Post Layout

Output Current		
Imin(µA)	Imax(µA)	Inominal(µA)
100.243	100.867	100.665

$$T_c = \Delta I / (\Delta T * Inominal)$$

Temp Coefficient = 37.5636 ppm

## Pre Layout

### Load Regulation

3.3V		1.8V	
RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)	RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)
Iout(max) = 102.804 μA	Iout(min) = 102.665 μA	Iout(max) = 100.103 μA	Iout(min) = 99.9887 μA

Regulation % = 0.14

Regulation % = 0.11

### Power Consumption

$$\begin{aligned}
 P &= Vdd * (Id) \\
 &= 3.3 * ((117.371 - 102.895) * 10^{-6}) \\
 &= 47.77 \mu W < 50 \mu W
 \end{aligned}$$

## Post Layout

### Load Regulation

3.3V		1.8V	
RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)	RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)
Iout(max) = 100.81 μA	Iout(min) = 100.676 μA	Iout(max) = 98.7875 μA	Iout(min) = 98.6332 μA

Regulation % = 0.13

Regulation % = 0.16

### Power Consumption

$$\begin{aligned}
 P &= Vdd * (Id) \\
 &= 3.3 * (115.9 - 101) * 10^{-6} \\
 &= 49.17 \mu W < 50 \mu W
 \end{aligned}$$

# APPLICATION

## OUR TARGET



LM4132, LM4132-Q1

SNVS372G – AUGUST 2005 – REVISED OCTOBER 2011

### LM4132, LM4132-Q1 SOT-23 Precision Low Dropout Voltage Reference

#### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
- Output Initial Voltage Accuracy: 0.05%
- Low Temperature Coefficient: 10 ppm/ $^{\circ}\text{C}$
- Low Supply Current: 60  $\mu\text{A}$
- Enable Pin Allowing a 3- $\mu\text{A}$  Shutdown Mode
- 20-mA Output Current
- Voltage Options: 1.8 V, 2.048 V, 2.5 V, 3 V, 3.3 V, 4.096 V
- Custom Voltage Options Available (1.8 V to 4.096 V)
- $V_{IN}$  Range of  $V_{REF} + 400 \text{ mV}$  to 5.5 V at 10 mA
- Stable With Low-ESR Ceramic Capacitors

#### 2 Applications

- Instrumentation and Process Control
- Test Equipment
- Data Acquisition Systems
- Base Stations
- Servo Systems
- Portable, Battery-Powered Equipment
- Automotive and Industrial
- Precision Regulators
- Battery Chargers
- Communications
- Medical Equipment

#### 3 Description

The LM4132 family of precision voltage references performs comparable to the best laser-trimmed bipolar references, but in cost-effective CMOS technology. The key to this breakthrough is the use of EEPROM registers for correction of curvature, temperature coefficient (tempco), and accuracy on a CMOS band-gap architecture allowing package-level programming to overcome assembly shift. The shifts in voltage accuracy and tempco during assembly of die into plastic packages limit the accuracy of references trimmed with laser techniques.

Unlike other LDO references, the LM4132 can deliver up to 20 mA and does not require an output capacitor or buffer amplifier. These advantages along with the SOT-23 packaging are important for space-critical applications.

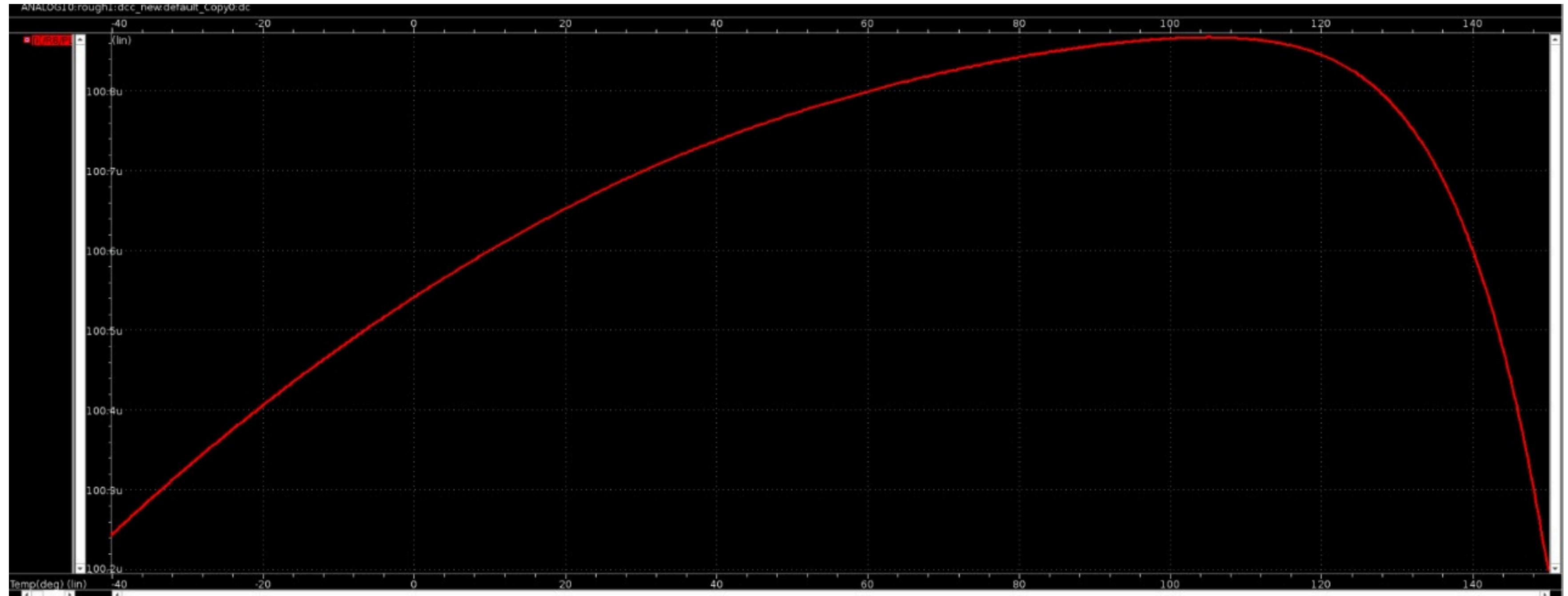
Series references provide lower power consumption than shunt references, because they do not have to idle the maximum possible load current under no-load conditions. This advantage, the low quiescent current (60  $\mu\text{A}$ ), and the low dropout voltage (400 mV) make the LM4132 ideal for battery-powered solutions.

The LM4132 is available in five grades (A, B, C, D and E) for greater flexibility. The best grade devices (A) have an initial accuracy of 0.05% with a specified temperature coefficient of 10 ppm/ $^{\circ}\text{C}$  or less, while the lowest grade devices (E) have an initial accuracy of 0.5% and a tempco of 30 ppm/ $^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM4132, LM4132-Q1	SOT-23 (5)	2.90 mm $\times$ 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



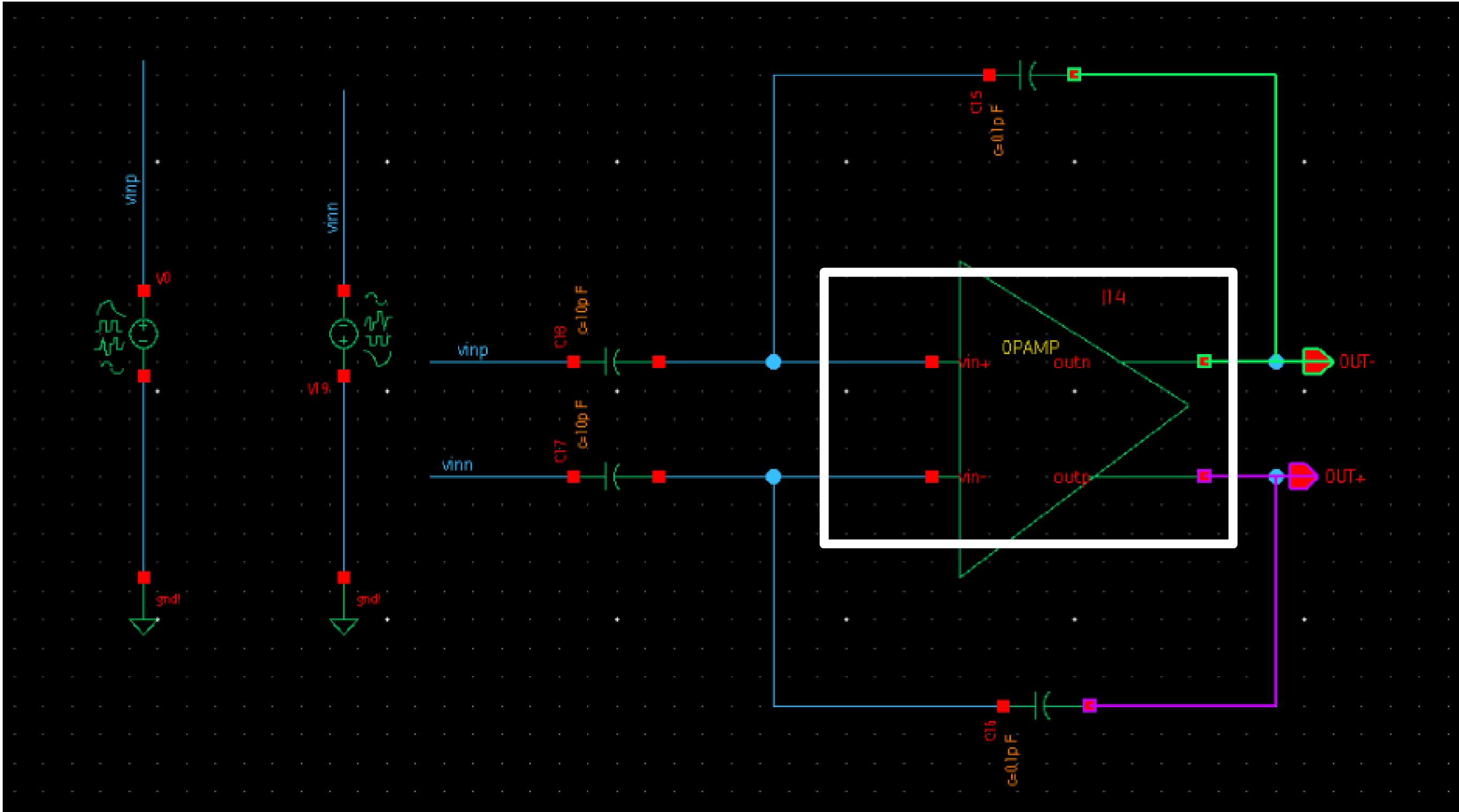
FOR -40 C to 150 C with 34.9 ppm TC

Testbench	Equations	Results
Filter	Filter	Filter
default_Copy0	i(R8/...	100.676u
	ppm:dc	34.9384u
	Nominal ...	100.685u

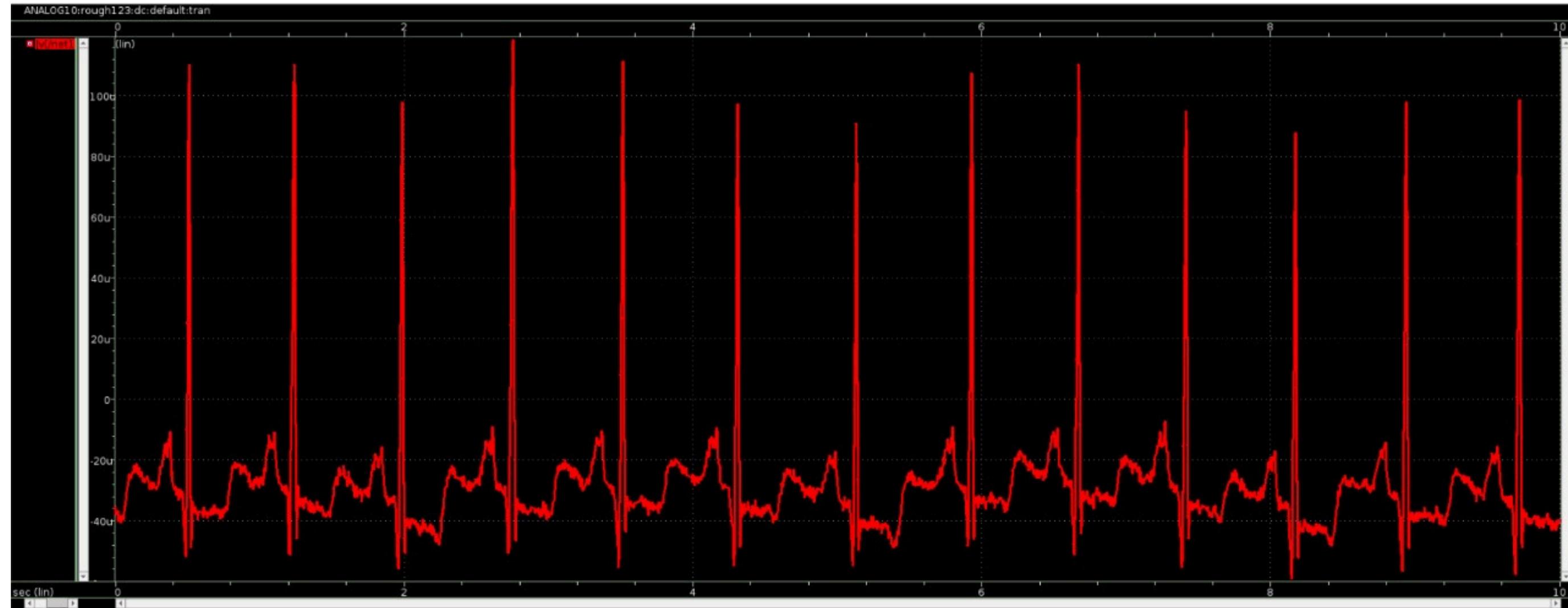
Here we are standing out with low TC within wide temperature range

## Implementation of application

## Data Acquisition System



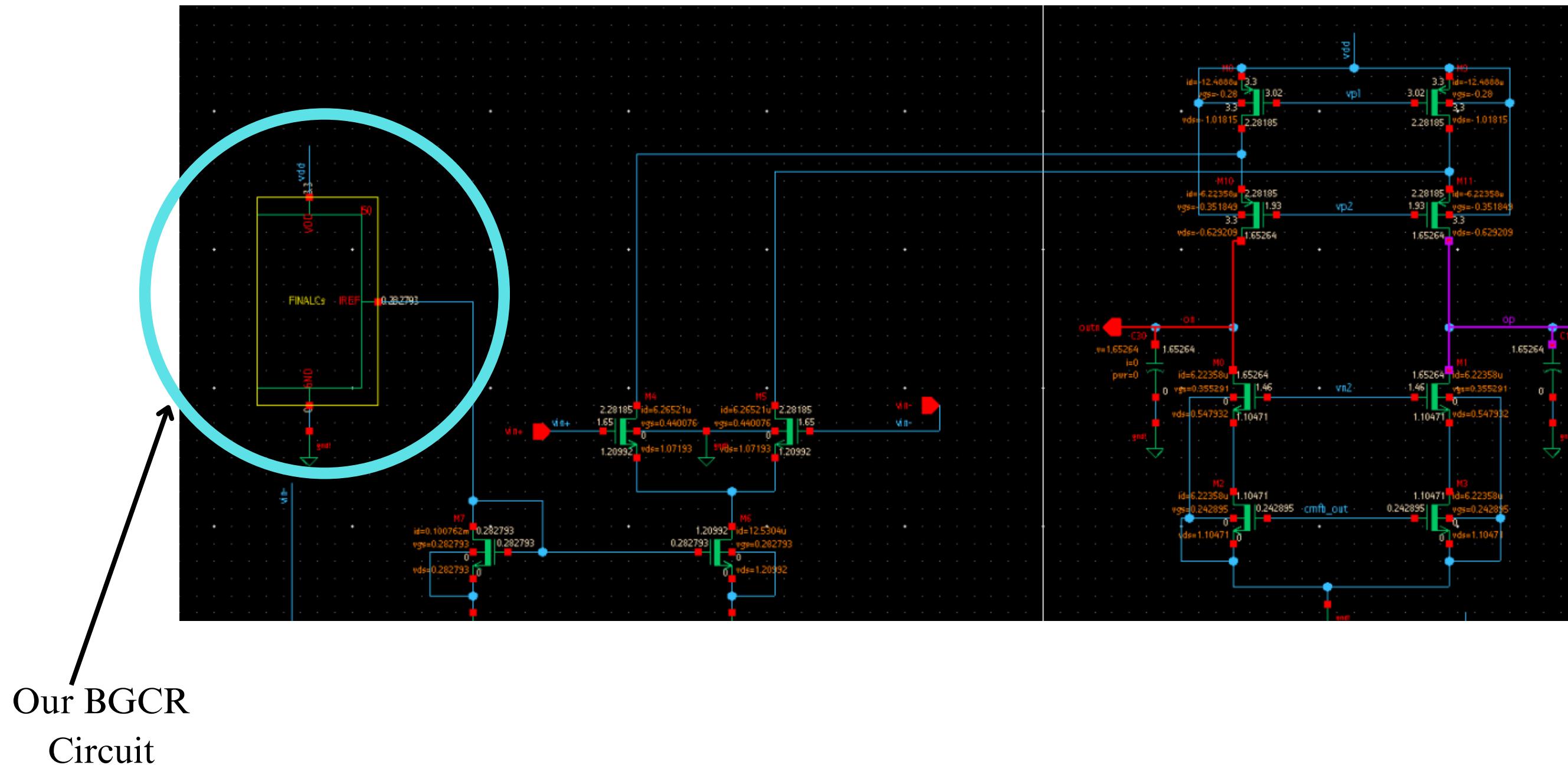
# ECG SIGNALS

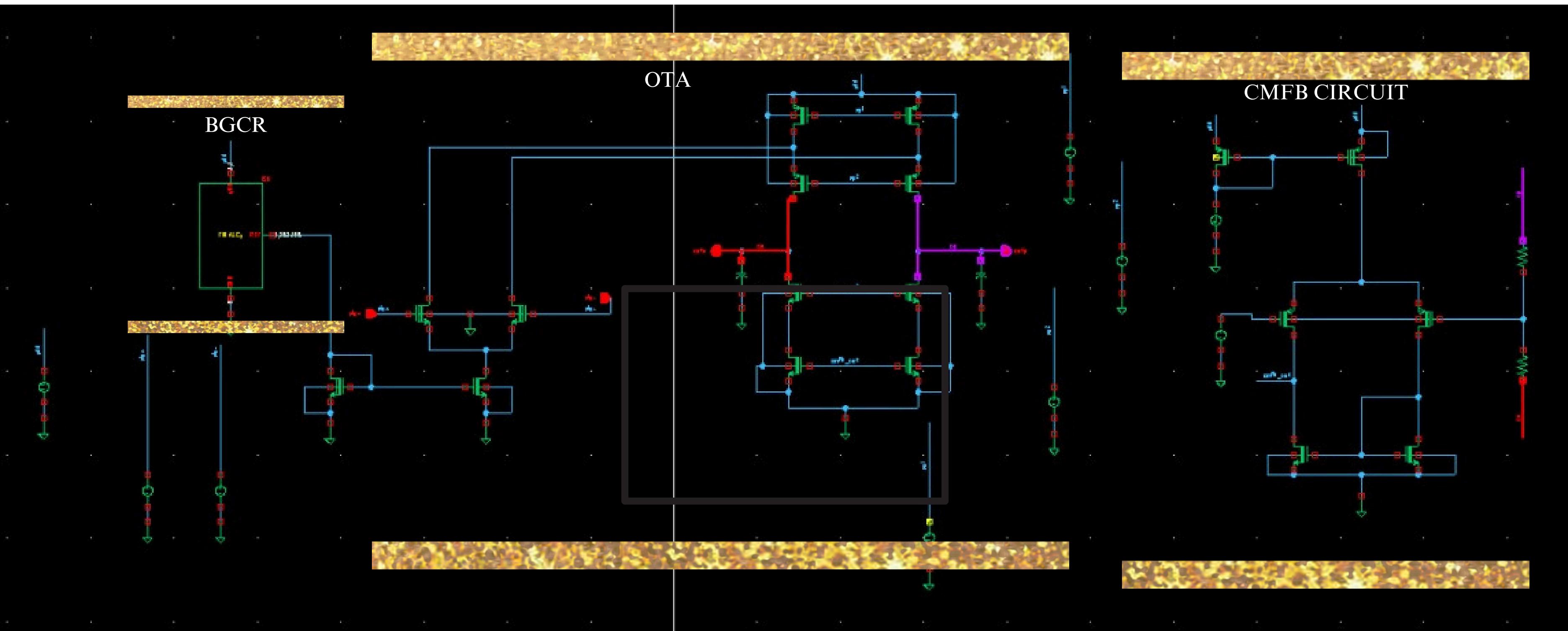


Vsource

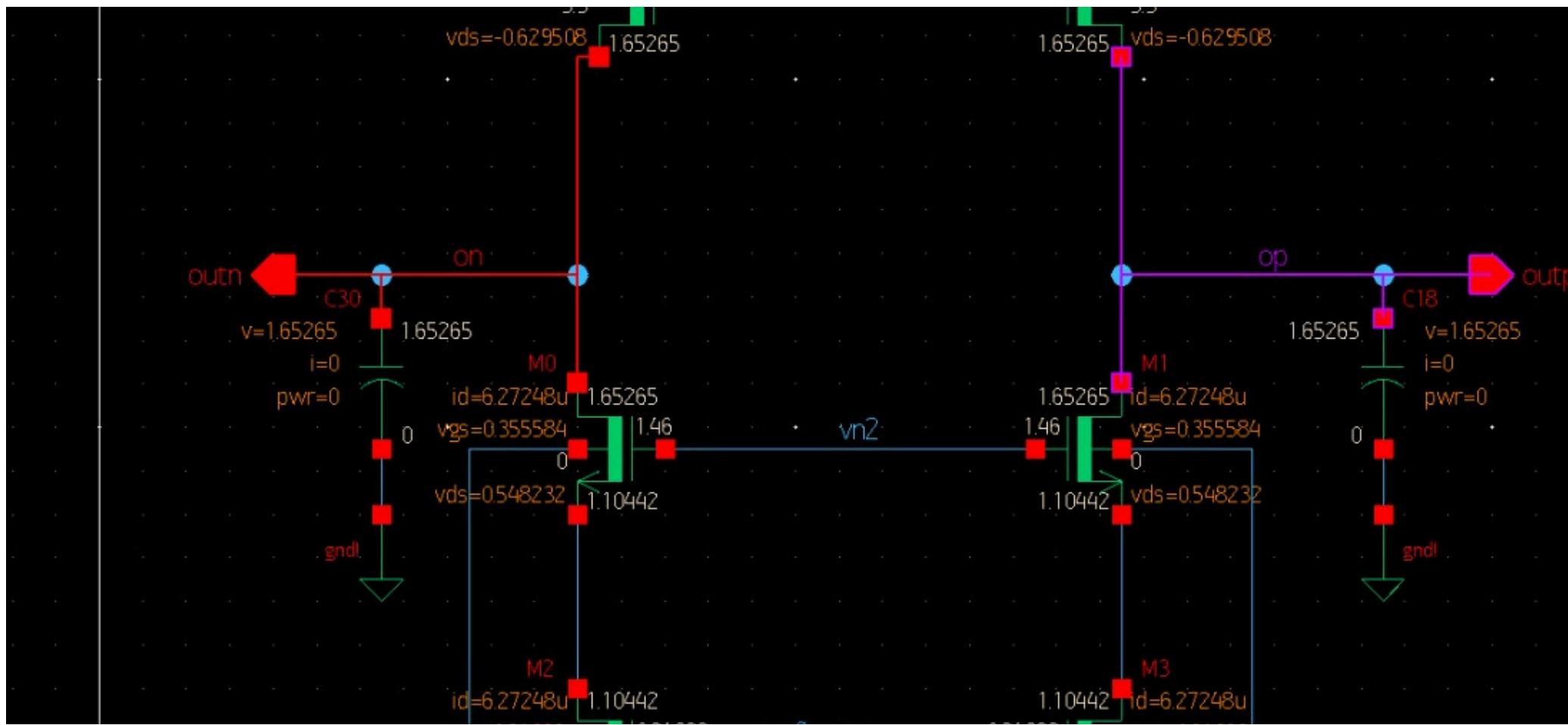
ecg2[t].txt		
File	Edit	View
0	-0.0000355	
0.002777778	-0.0000365	
0.005555556	-0.0000375	
0.008333333	-0.000038	
0.011111111	-0.000037	
0.013888889	-0.000037	
0.016666667	-0.0000365	
0.019444444	-0.000038	
0.022222222	-0.000039	
0.025	-0.00004	
0.027777778	-0.0000385	
0.030555556	-0.0000385	
0.033333333	-0.0000385	
0.036111111	-0.0000395	
0.038888889	-0.00004	
0.041666667	-0.0000405	
0.044444444	-0.0000405	
0.047222222	-0.00004	
0.05	-0.00004	
0.052777778	-0.0000385	
0.055555556	-0.000039	
0.058333333	-0.000039	
0.061111111	-0.0000395	
0.063888889	-0.000037	
0.066666667	-0.0000365	
0.069444444	-0.0000355	

At first we created a new OTA and tested our current reference circuit.

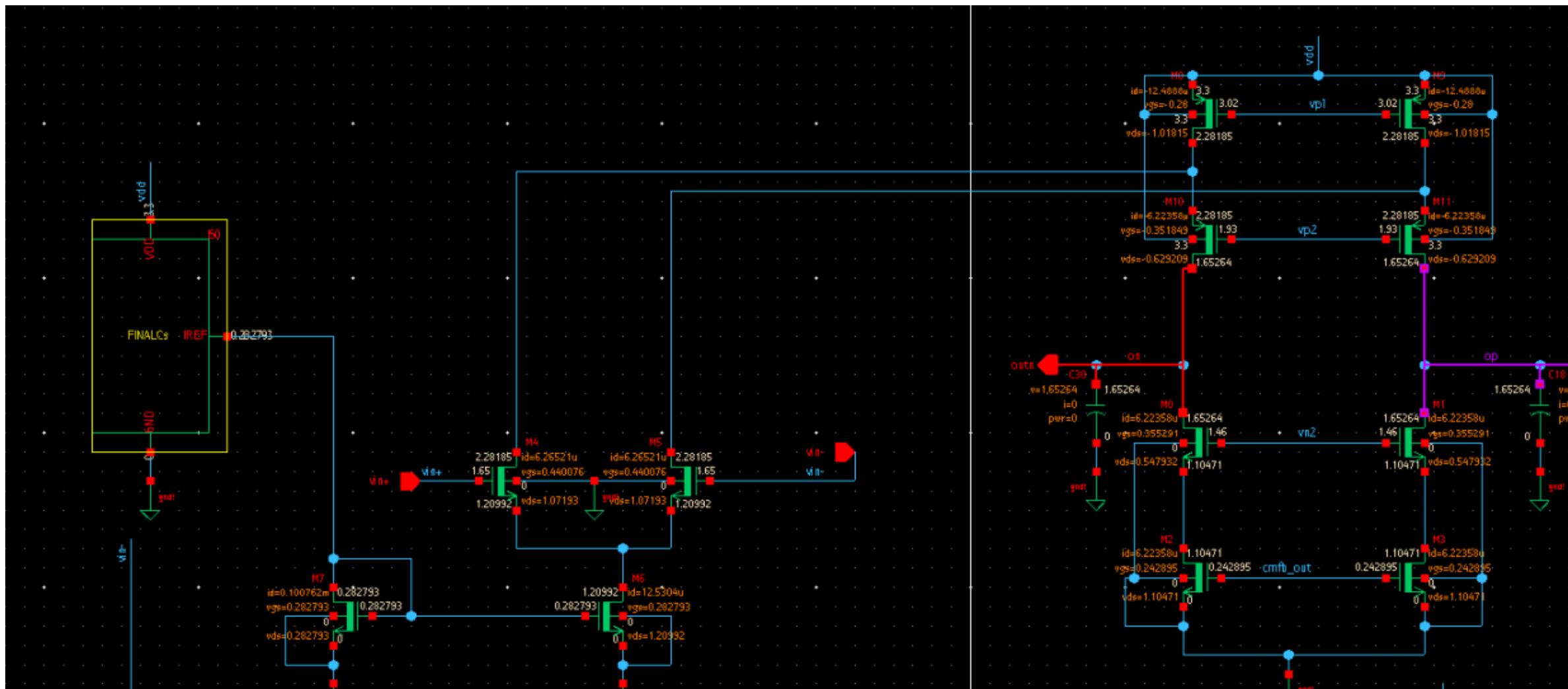




## PRE LAYOUT



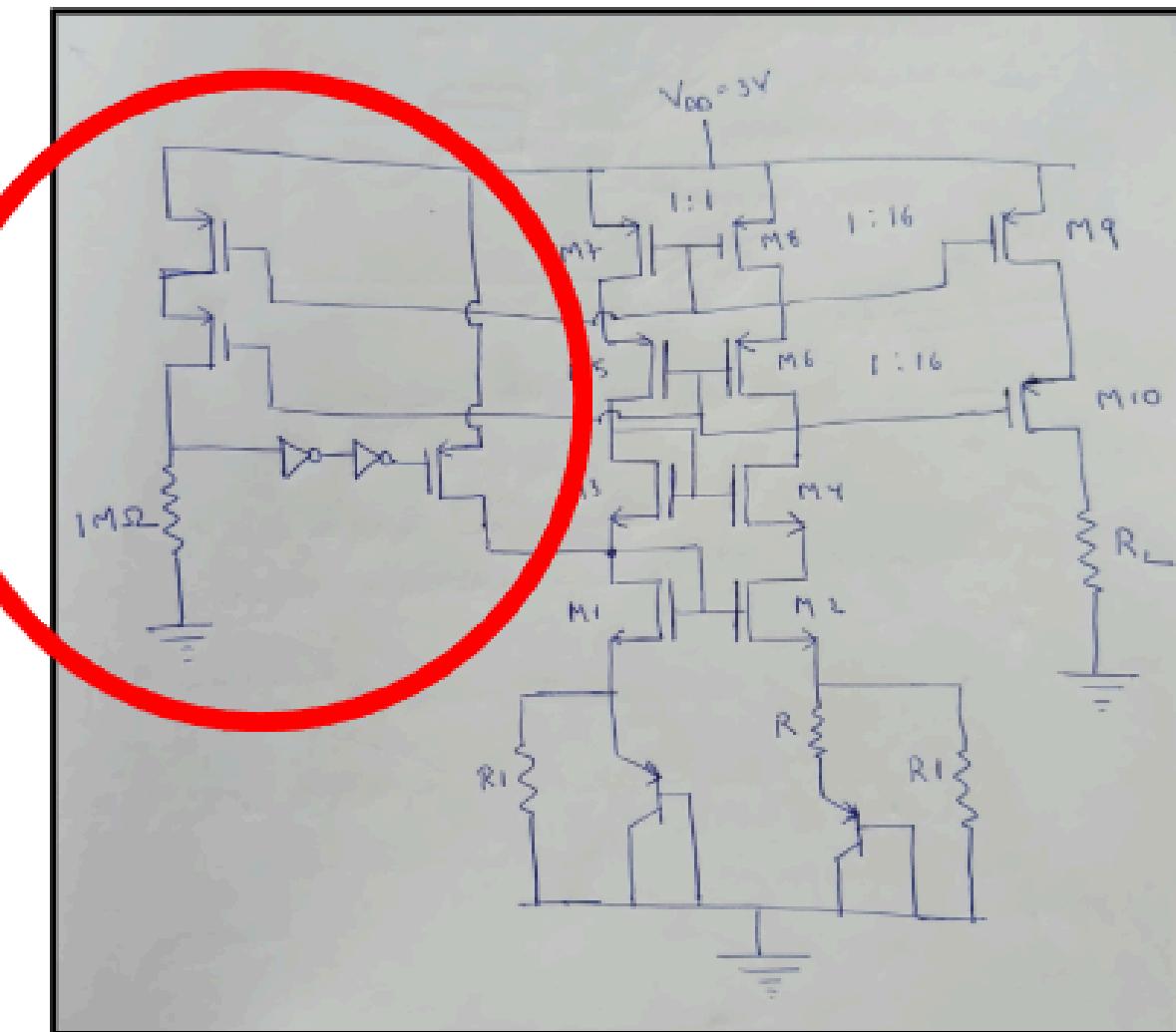
## POST LAYOUT SIMULATION



# Proposed Circuit with Start-up

Pre Layout					
Load Regulation					
3.3V		1.8V			
RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)	RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)		
Iout(max) = 102.804 μA	Iout(min) = 102.665 μA	Iout(max) = 100.103 μA	Iout(min) = 99.9887 μA		
Regulation % = 0.14		Regulation % = 0.11			
Power Consumption					
$P = V_{dd} * (I_d)$ $= 3.3 * ((6.41974+0.39+1.37) * 2 * 10^{-3})$ $= 48.114 \mu W < 50 \mu W$					

Start-up Network



## Load Regulation

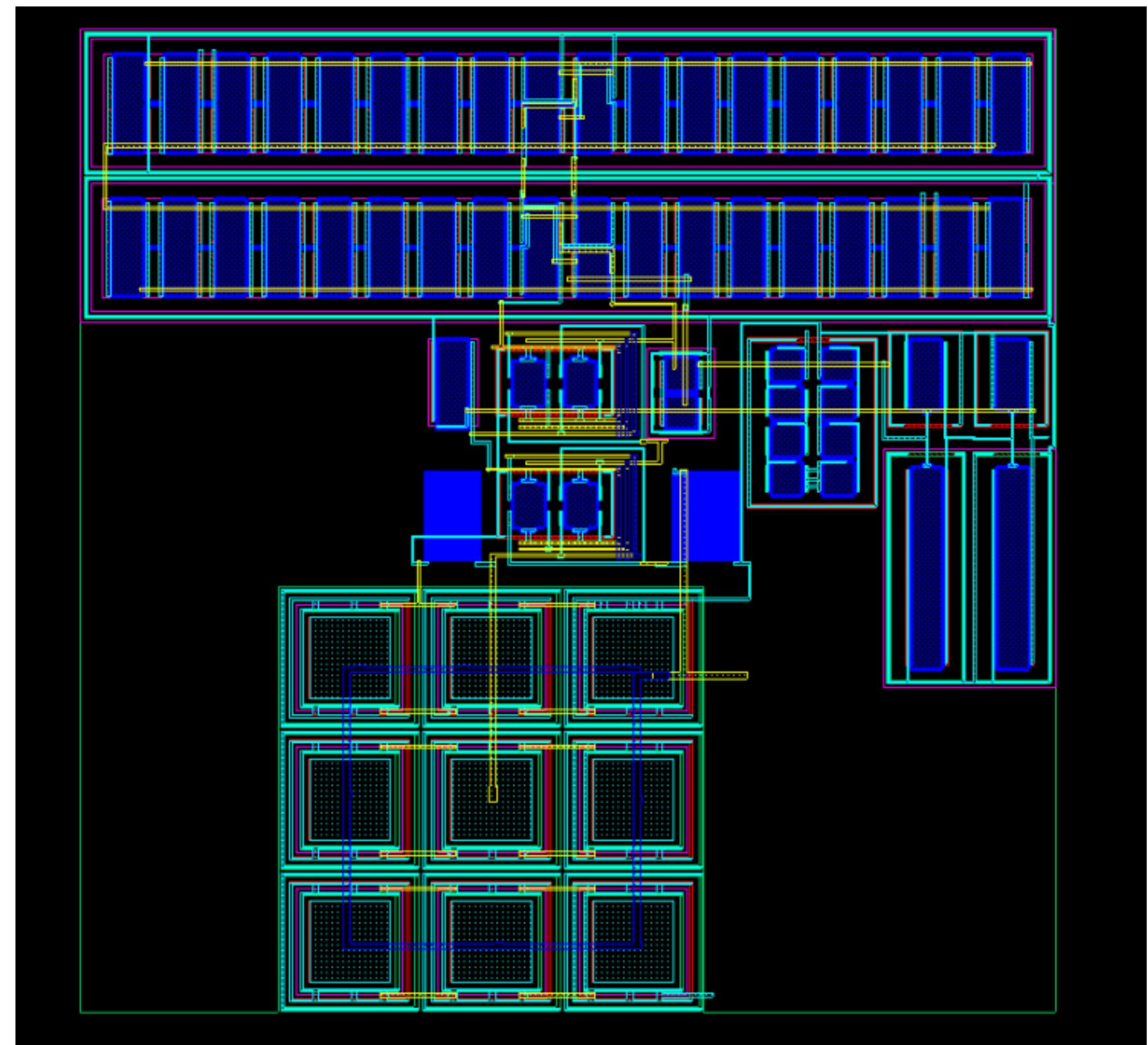
3.3V		1.8V	
RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)	RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)
Iout(max) = 100.81 μA	Iout(min) = 100.676 μA	Iout(max) = 98.7875 μA	Iout(min) = 98.6332 μA

Regulation % = 0.13      Regulation % = 0.16

Output Current		
Imin(μA)	Imax(μA)	Inominal(μA)
100.243	100.867	100.665

$$T_c = \Delta I / (\Delta T * Inominal)$$

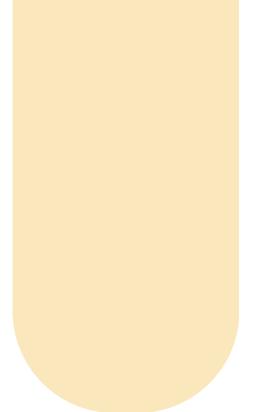
Temp Coefficient = 37.5636 ppm



POST LAYOUT EXTRACTION

Pre Layout				Post Layout			
<b>Load Regulation</b>							
3.3V		1.8V		3.3V		1.8V	
RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)	RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)	RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)	RL = 1 Ω (VL = 0V)	RL = 10 kΩ (VL = 1V)
Iout(max) = 102.804 μA	Iout(min) = 102.665 μA	Iout(max) = 100.103 μA	Iout(min) = 99.9887 μA	Iout(max) = 100.81 μA	Iout(min) = 100.676 μA	Iout(max) = 98.7875 μA	Iout(min) = 98.6332 μA
Regulation % = 0.14		Regulation % = 0.11		Regulation % = 0.13		Regulation % = 0.16	
<b>Power Consumption</b>				<b>Power Consumption</b>			
$P = Vdd * (Id)$ $= 3.3 * ((117.371 - 102.895) * 10^{-6})$ $= 47.77 \mu W < 50 \mu W$				$P = Vdd * (Id)$ $= 3.3 * (115.9 - 101) * 10^{-6}$ $= 49.17 \mu W < 50 \mu W$			

Observations			
Pre Layout			Post Layout
Output Current			Output Current
Imin(μA)	Imax(μA)	Inominal(μA)	Imin(μA)
102.704	102.929	102.898	100.243
Tc = ΔI / (ΔT * Inominal) Temp Coefficient = 13.36 ppm			Tc = ΔI / (ΔT * Inominal) Temp Coefficient = 37.5636 ppm



**THANK YOU**

