DESIGN OF AMPLIFIERS

4.1 CHARGE AMPLIFIER

4.1.1 Introduction

It is a current integrator, meaning that the integrated value of the input current or total injected charge determines the output voltage. Piezo sensors produce a charge, which is detected by charge amplifiers. They change this charge with the aid of the feedback capacitance. Since the charge is the parameter sensed, the cable's length has no effect on the system's performance. This is one of the main advantages of the charge amplifier configuration over the voltage amplifier configuration. Charge mode sensors might be better when the electronics system is linked far from the sensor.

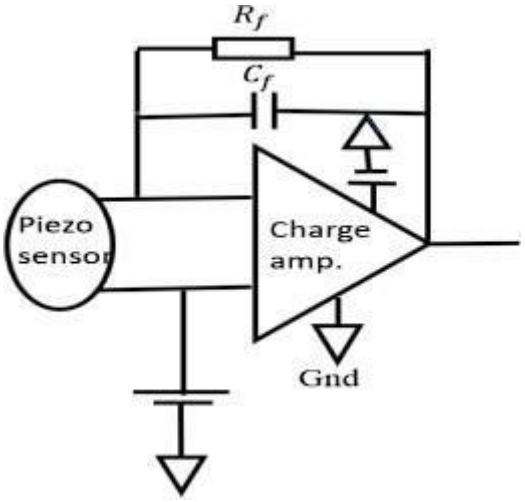

Fig.4.1 Diagram of featuring a piezo sensor connected to a charge amplifier

Fig shows the basic charge amplifier circuit in which C_f is the feedback capacitance and R_f is the feedback resistance. A voltage is created between the input pin of the amplifier whenever any charge from the piezoelectric sensor starts to charge its capacitance, that of the cable, or its input capacitance.

Gain expression for charge amplifier

The input charge, Qs, is applied to the inverting input of the amplifier. It is distributed to the cable capacitance, Cc, the amplifier input capacitance, C_{in}, and the feedback capacitor. So, by charge conservation principle:

$$C_f \cdot Q_s = QC_c + QC_{in} + QC_f \quad (1)$$

$$Q_s = V_{in} (C_c + Cin) + V_f \cdot C_f \quad (2)$$

The charge amplifier's gain expression makes it evident that gain is solely dependent on the feedback capacitance. The total gain of the system is unaffected by input capacitance, sensor capacitance, or cable capacitance. Stated differently, the system's sensitivity is unaffected by the capacitances of the sensor and connection. Because the bandwidth of the system is inversely proportional to its total capacitance, it has a high bandwidth. Because there is a direct correlation between the system's time constant and total capacitance, a lower time constant results in a higher system speed.

Equivalent circuit of piezoelectric sensor

To calculate the current that the piezoelectric sensor injects in order to produce a peak-to-peak output voltage of 270 mV. On Tina, a comparable system has been created by taking into account capacitance of 500 pF and resistance of 1 MΩ. The loading effect of the CRO, which has a resistance of 1 MΩ, lowers the piezoelectric's resistance to 1 MΩ even though it is 16 MΩ in its native condition.

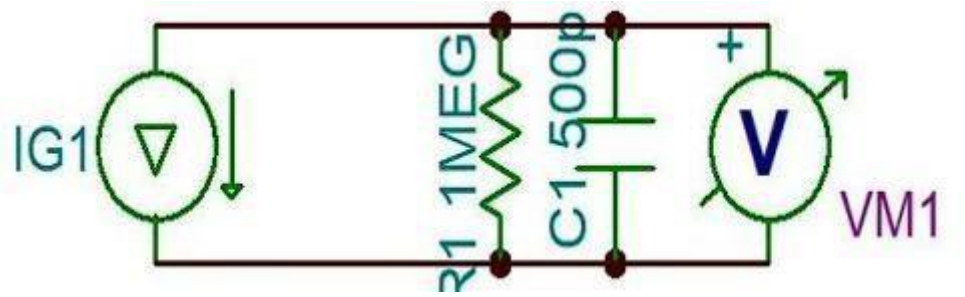

Fig.4.2 Calculation of voltage to charge gain of charge amplifier

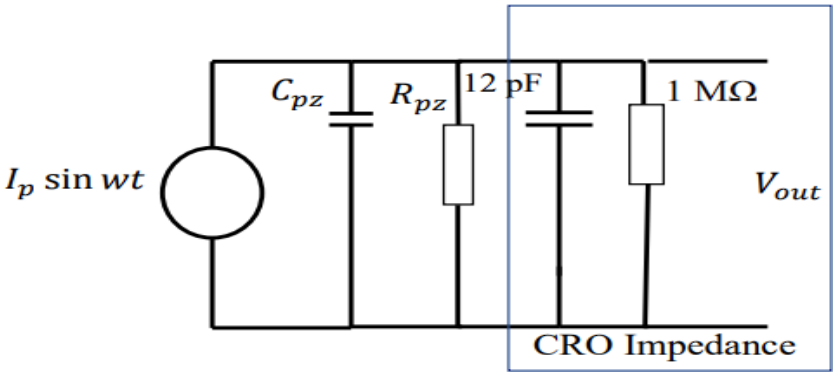

Fig.4.3 Impedance and Capacitance offered by CRO

The gain of the charge amplifier is ratio of output voltage and input charge, as
gain = $\boldsymbol{V_{out}}$ / $\boldsymbol{Q_{in}}$
So, we have to find out Qin of the overall amplifier circuit.

Let injected current by sensor is

$I = Ip \sin wt$= 140 nA

$Q = \int I\ dt = Ip/w \times \sin wt$

Q_{peak} = 140×10−9/30×2π

$Q_{peak-pak}$ = 2×(140×10−9)/(30×2π) = 1.48 nC

$V_{out}(p-p)$ = 700 mV = 700 × 10^−3

$V_{out}(p-p)/Qp-p$ = (700 × 10^−3)/ 2 * (140 × 10^−9) × (30 × 2π) = 4.71 × 10^8

$Gain$ = 4.71 × 10^8 V / C.

Hence, voltage to charge gain of system is 4.71 × 10^8 V / C

LTSPICE MODEL

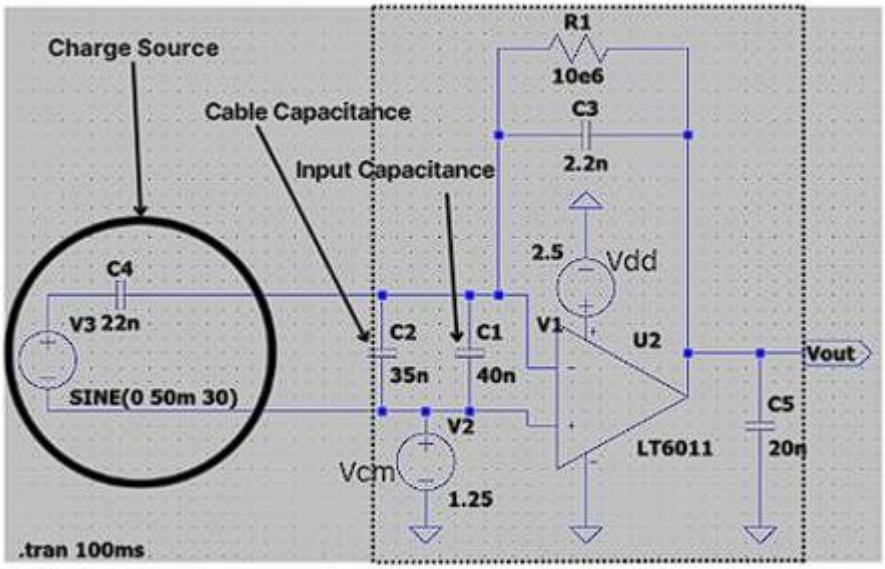

Fig.4.4 Circuit of sensor connected with Charge amplifier

Circuit Description

1.Input Signal and Coupling

- **V_3** is a sinusoidal input (50 mV peak, 30 Hz), simulating a signal source like a piezoelectric sensor.
- **C_4 (22nF)** blocks DC components and passes only AC signal to the amplifier input.

2.Biasing and Integration Node

- **C_2 (35nF)** and **C_1 (40nF)** form a capacitive voltage divider at the non-inverting input.
- **V_2 (1.25V)** sets the bias/reference voltage.

3.Operational Amplifier Stage

U2 is an LT6011 precision op-amp powered with a single supply (2.5V).

The feedback network consists of:

R1 = 10 MΩ: Provides DC stability and sets the low-frequency behavior.

C3 = 2.2nF: Forms a feedback integrator

C5 (20nF) is used for output AC decoupling.

4.Feedback Mechanism

The output voltage (Vout) is related to the integrated input charge on C3.
Since Vout=-Qin/C3, this topology is ideal for low-frequency, high-impedance signal sources.

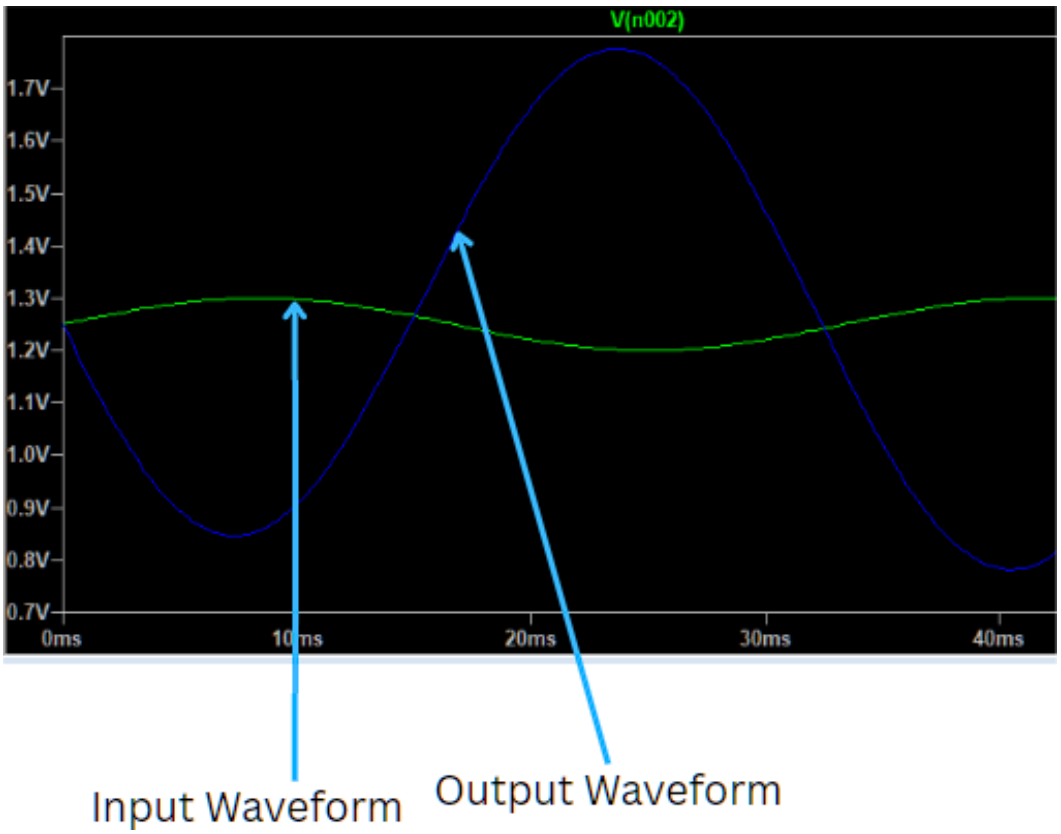

Fig.4.5 i/p waveform of Sensor and o/p waveform of Amplifier

Simulation Results Analysis

Graph 1 (Top): Output Voltage – V(vout)

- Shows amplified output waveform.
- Signal is centered around ~1.25 V with ~1 V peak-to-peak swing.
- Phase-inverted due to inverting configuration.

Graph 2 (Bottom): Input Reference Node – V(n002)

- Displays the voltage at the non-inverting input.
- Follows the input sine signal with smaller amplitude, showing capacitive division and DC bias behavior.
- Confirms proper AC coupling and low-frequency performance.

TINA model with proper devices

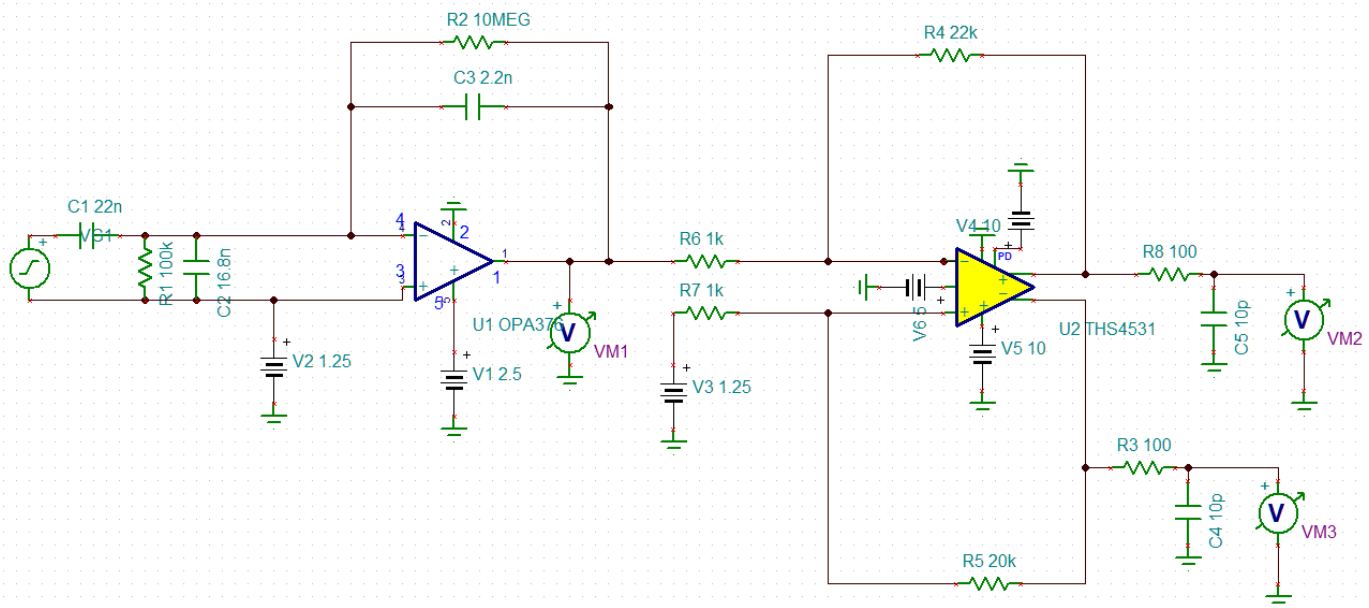

Fig.4.6 TINA Model

OPA376 (Single ended amplifier)

OPA376 is a low-noise operational amplifier with excellent dc precision and ac performance. It is very desirable for a variety of precise and portable rail-to-rail input and output applications due to its low noise (7.5 nV/Hz), maximum quiescent current of 950 uA and 5.5MHz bandwidth. This device also has a respectable single-supply operation and a wide supply range with good PSRR, which makes it appealing for applications that run unregulatedly directly from batteries. OPA376 is offered in the following packages: Micro-size SC70-5SOT23-5, SOT-23,VSSOP.

THS4531 (Differential amplifier)

THS4531A device is a low-power, fully differential amplifier. It is designed for low-power

data acquisition systems and high-density applications where power consumption and dissipation are crucial. While driving analog-to-digital converters (ADCs), the device possesses accurate output common-mode control, which permits DC coupling. It is manufactured in different packages like SOIC-8 (4.90 mm * 3.91 mm), VSSOP-8 (3.00 mm * 3.00 mm), and WQFN (10). Fig.3.6 shows the pin diagram of THS4531. This stage is mainly used for increasing the overall gain of the system and for enhancing its noise immunity.

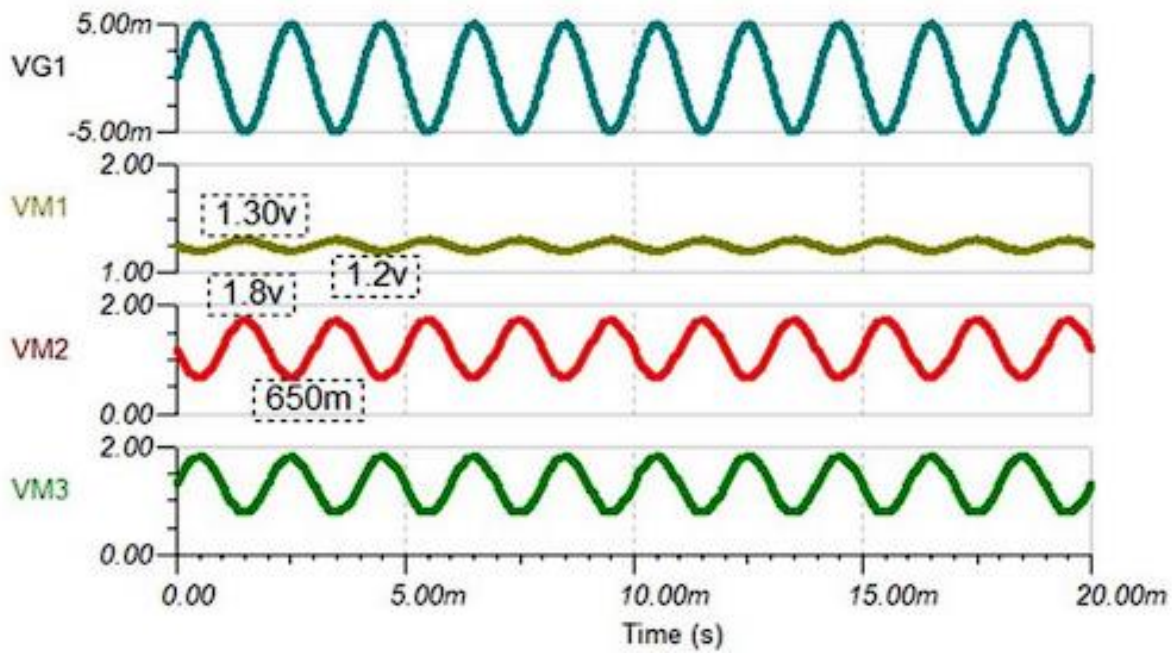

Fig.4.7 Transient Response of whole circuit

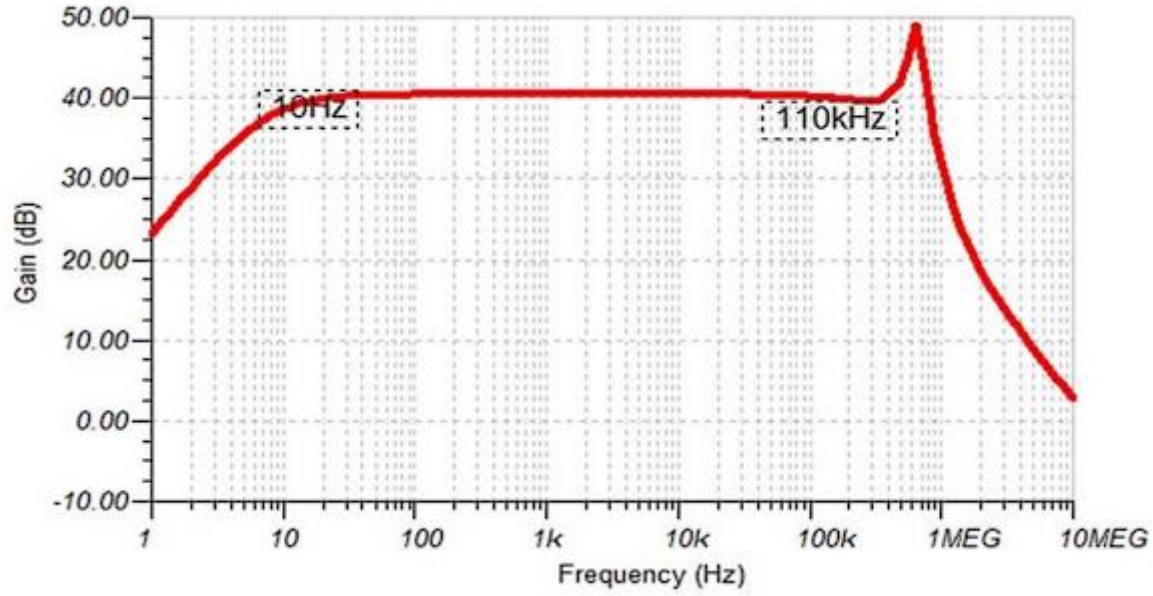

Fig.4.8 Frequency response of the signal conditioning unit (simulation)

In Fig. VG1 is the applied input voltage, VM1 is the output of the first stage, and VM2 and VM3 are the outputs of the second stage. The output of the first stage is in the opposite phase of the applied input signal, and the outputs of the differential amplifier are also out of phase.

From Fig., it can be inferred that the gain of the system is 40 dB, as per expectations.

Architecture of data acquisition unit

The signal processing, which can be analog or digital, is performed to extract relevant information. Analog signal processing is not preferred over digital signal processing because the latter offers much less flexibility and design complexity.
Since analog signals make up most of the signals acquired, an additional stage called an ADC is needed to carry out the transformation from analog to digital. ADC input range is fully utilised to reduce quantization error from sampling and a low pass filter is employed to remove unintentional frequency components from the collected signal.
Finally, after signal processing is complete, the extracted data can be sent to the user wirelessly or through a wire.

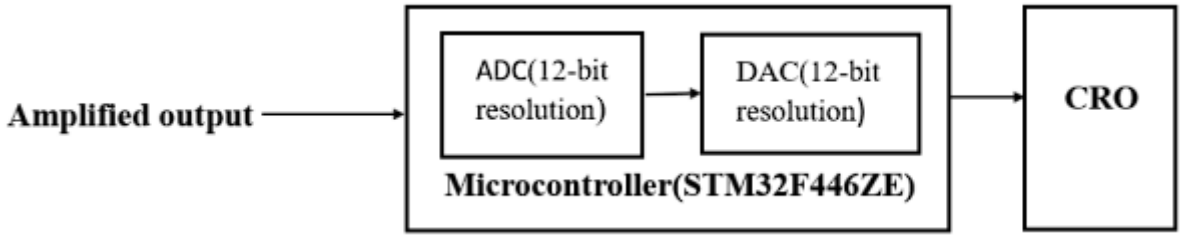

Fig.4.9 Architecture of the data acquisition system

Fig shows the architecture of data acquisition unit. Compared to analog signal processing, digital signal processing has several benefits, including lower noise sensitivity, greater design flexibility and the ability to implement complex digital filters, simpler data compression and storage, etc.The desire to digitize an analog signal as soon as possible in the signal acquisition module is motivated by all these benefits.
In this block diagram, amplified output is fed to a STM32 Microcontroller (STM32F446RE) having ADC of resolution 12 bit and this output is displayed on a STMCubeIDE software. For verification purpose the ADC output is again converted to analog domain using in built DAC of microcontroller. DAC output is displayed CRO screen along with amplified out.