Designing Digital Clock on Spartan-3 xc3s400

Aim of the project:

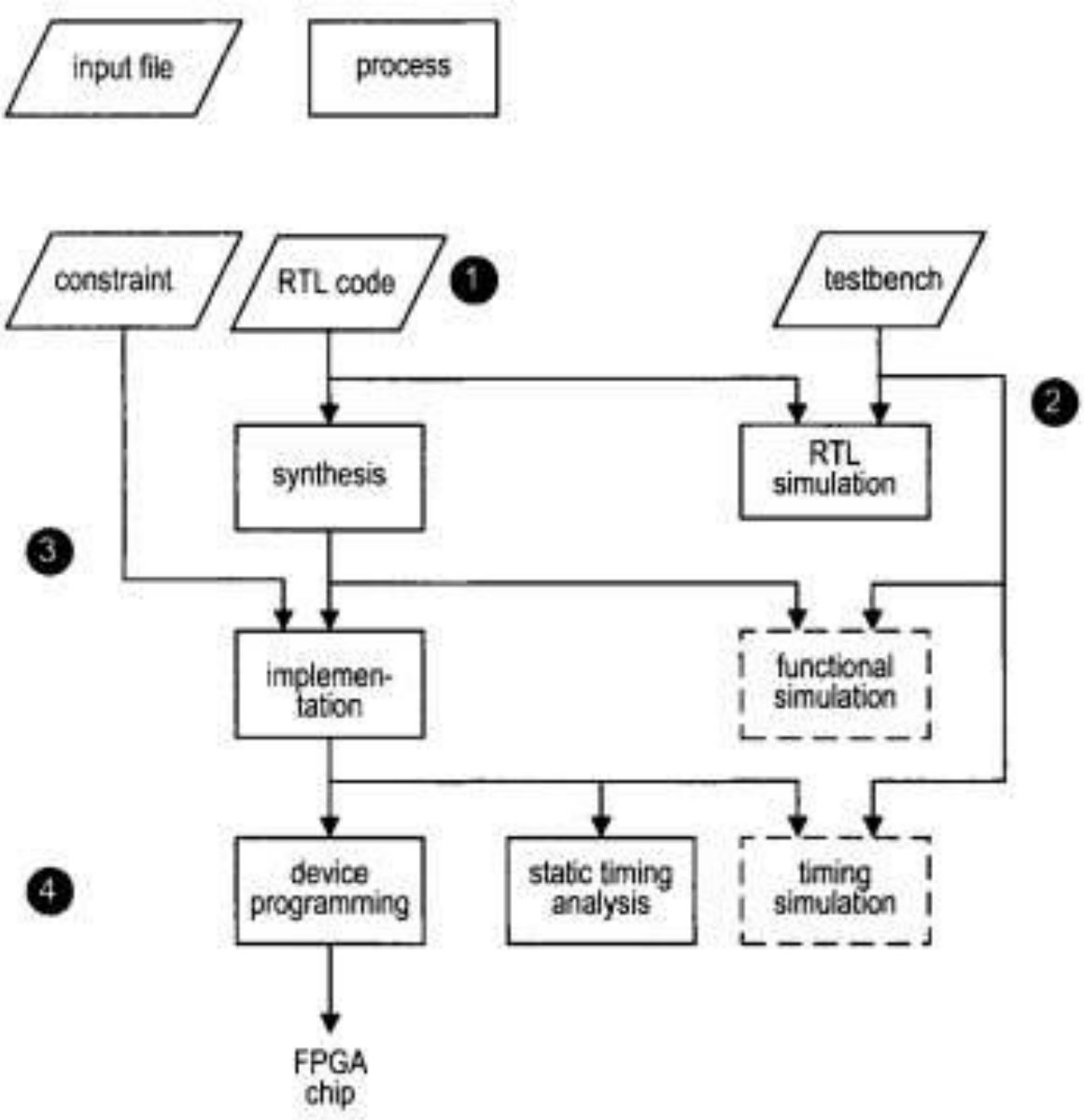
The main objective of the digital clock is to display the time digitally using 7-segment display on Spartan-3 FPGA Board. The digital clock by default displays the run time and time can be set by using time set assigned to switch on board. The digital clock designed is a 24-clock hour format. It displays the time in format of hours : minutes : seconds. Out of total 4MHz,it used only 1Hz frequency with 22 bit register. It uses the already existing blocks like counter.

Overview of Implementation of Digital Clock Using FPGA:

This project makes use of FPGA for the hardware implementation of digital clock. As soon as the FPGA is switched on, the clock starts. The FPGA and on board clock will generate the timing signals. One second signal is generated using the global clock and then this seconds clock is used to generate the timing signals. It consists of six registers in total which includes hr2,hr1,min2,min1,sec2,sec1. When sec1 is 9 and sec2 is 5, then sec2 and sec1 values are made to zero and min1 value is incremented. If min2 is 5 and min1 is 9 then min2 and min1 values are made to zero and hr1 is incremented. If hr2 is 2 and hr1 is 4 then hr2 and hr1 is made to zero and thus the count continues.

Development Flow:

The simplified development flow of an FPGA-based system is shown in the figure below.The left portion of design flow is the refinement and programming process in which a system is transformed from an abstract textual HDL description to a device cell-level configuration and then programmed to the FPGA device.The right portion is the validation process which checks whether the system meets the performance goals and functional specifications.



The major steps in the flow are:

1. Design of code and Addition of constrains:

Design the system and derive the HDL(Hardware Description Language) file. To specify certain implementation constraints, we may need to add a separate constraint file.

2. Development of testbench code for simulation:

Develop the testbench in HDL and perform RTL simulation. The RTL term proves the fact that the HDL code is done at the register transfer level.

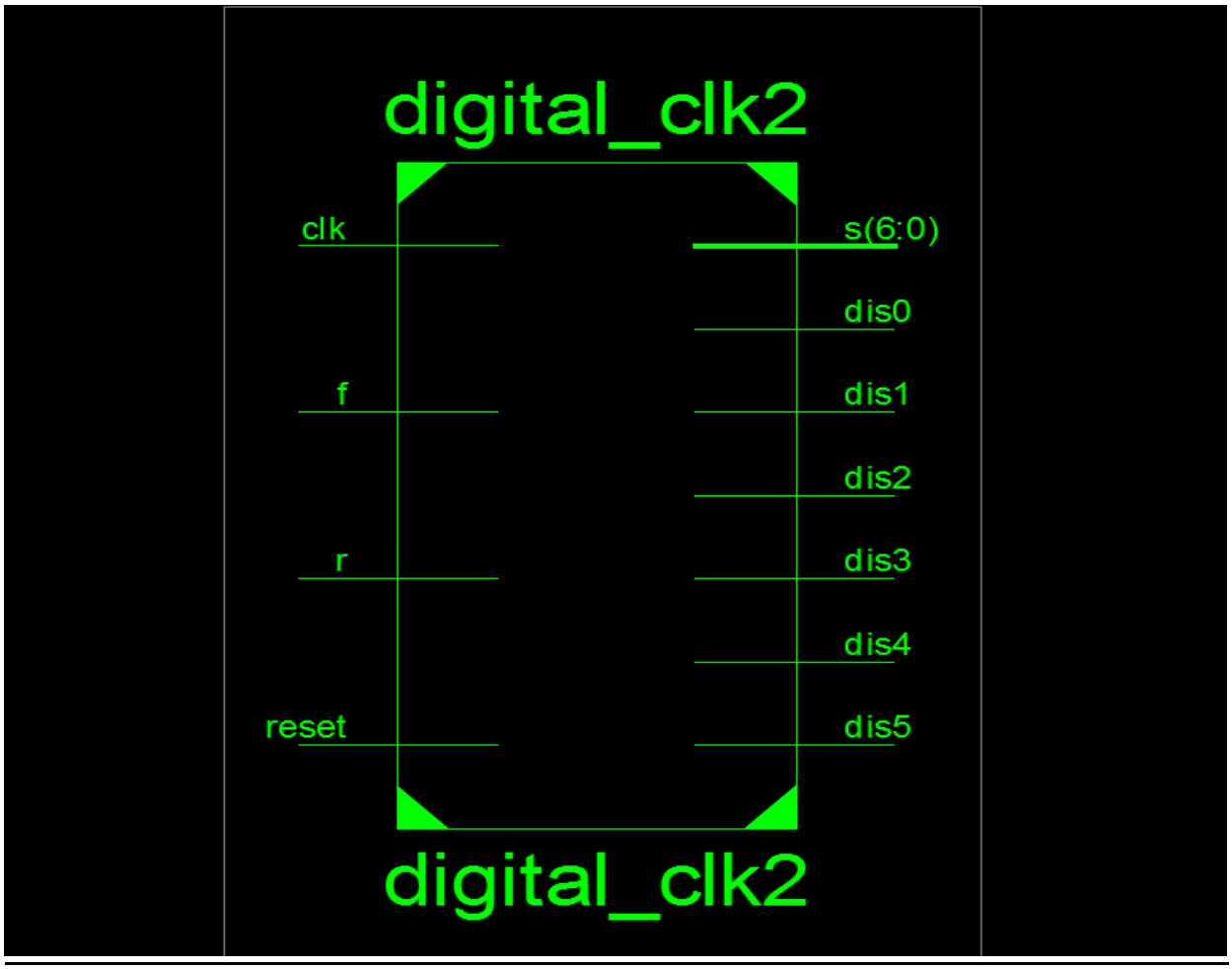
3. Synthesis and Implementation:

Perform synthesis and implementation. The synthesis process is known as logic synthesis, in which the software transforms the HDL constructs to generic gatelevel components, such as simple logic gates and FlipFlops. The implementation process consists of three smaller processes namely: translate, map, place and route. The translate process merges multiple design files to a single netlist. The map process, which is generally known as technology mapping, maps the generic gates in the netlist to FPGA's logic cells and 10Bs. The place and route process, which is generally known as placement and routing, derives the physical layout inside the FPGA chip. It places the cells in various physical locations and determines the routes to connect various signals accordingly. In the Xilinx flow, static timing analysis, which determines various timing parameters, such as maximal propagation delay and maximal clock frequency, is performed at the end of the implementation process.

4. Generation of Bit stream and configuration of the file:

Create and download the programming document. In this procedure, an arrangement record is created by the last netlist. This document is then downloaded to a FPGA gadget serially to design the switches and rationale cells. The discretionary useful reproduction can be performed after union, and the discretionary planning recreation can be performed after usage. To supplant the RTL depiction and check the accuracy of the combination handle, utilitarian reenactment utilizes an integrated netlist. Timing recreation utilizes the last netlist, alongside nitty gritty planning information, to perform reproduction. Practical and Timing recreation may require a huge sum of time as a result of the multifaceted nature of the netlist. In the event that we take after great outline and coding hones, the HDL code will be integrated and executed effectively. We have to utilize just RTL reenactment to check the accuracy of the HDL code and afterward utilize static planning examination to look at the pertinent planning data. Both useful and timing reenactments might be discarded from the improvement stream.

Pin Configuration of Block Diagram:



The block diagram gives in detail about the inputs and outputs of the Digital Clock.

INPUT PINS:

- **Clk:** It represents the global clock whose frequency is 4MHz.In the program it is used to generate one second timing signal.
- **f:** When f is '0', the clock frequency will be 1 Hz;
  When f is '1', the clock frequency will be 100Hz;
- **r:** This is used to control the MOD-6 counter.
- **reset:** Whenever reset is high all the values are set to zero.

OUTPUT PINS:

- **s(6:0):** It is used to display numbers in the positions of seconds, minutes and hours. These values are s1,s2,s3,s4,s5 and s6.
- **Disp_seg :** This is used to display numbers in the seven segment display .These values are dis0,dis1,dis2,dis3,dis4 and dis5.

How the six displays are working?

- As we know that in a six 7-segment display type FPGA, all the ports with same name like display A,B,C,D,E,F,G and Dot are all connected in parallel so if one 7-segment display changes to other value all other display also change simultaneously.
- To tackle this so that we could get different values on different displays ,we use a MOD-6 counter so that only one display will be 'ON' at a time at a frequency of 800Hz.
- So the transition between 'ON' and 'OFF' condition won't be visible as it will be at very high frequency.

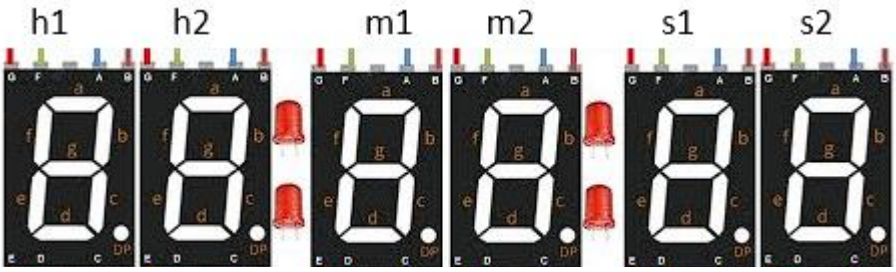
How a single display is working?

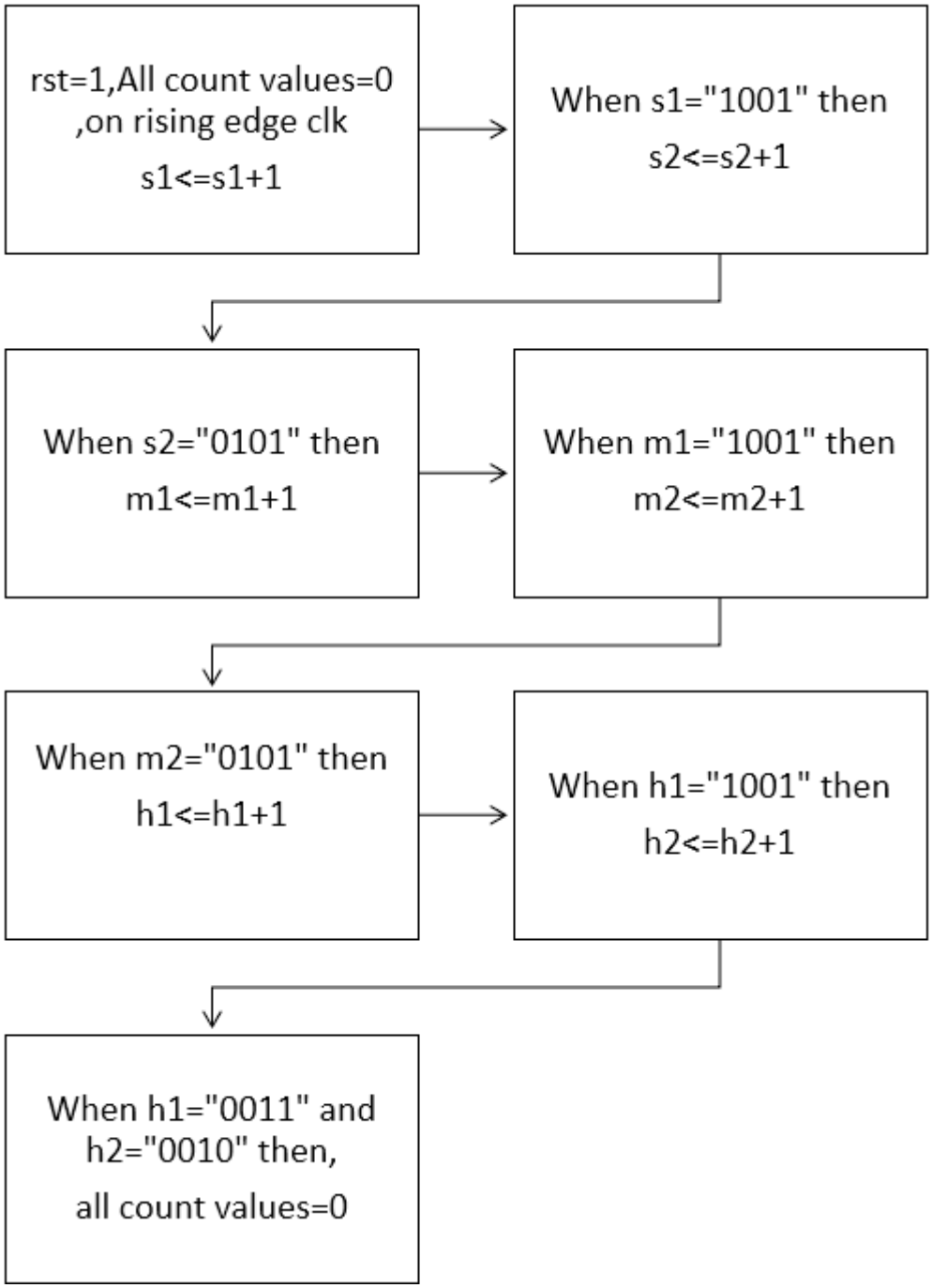
- At first we have a clock of 4MHz on the FPGA board whose port number is p181, now a 22 bit counter is used to generate a frequency of 1Hz for our

digital clock. We have also made a 100Hz counter if we want to fast our clock.

- The 1Hz clock signal is fed to the MOD-10 counter and then the output is fed to the BCD to 7-segment decoder.
- Then the output is implemented on the FPGA by indicating different ports and by generating a bit file.

FLOW DIAGRAM OF DIGITAL CLOCK





Summary Report:

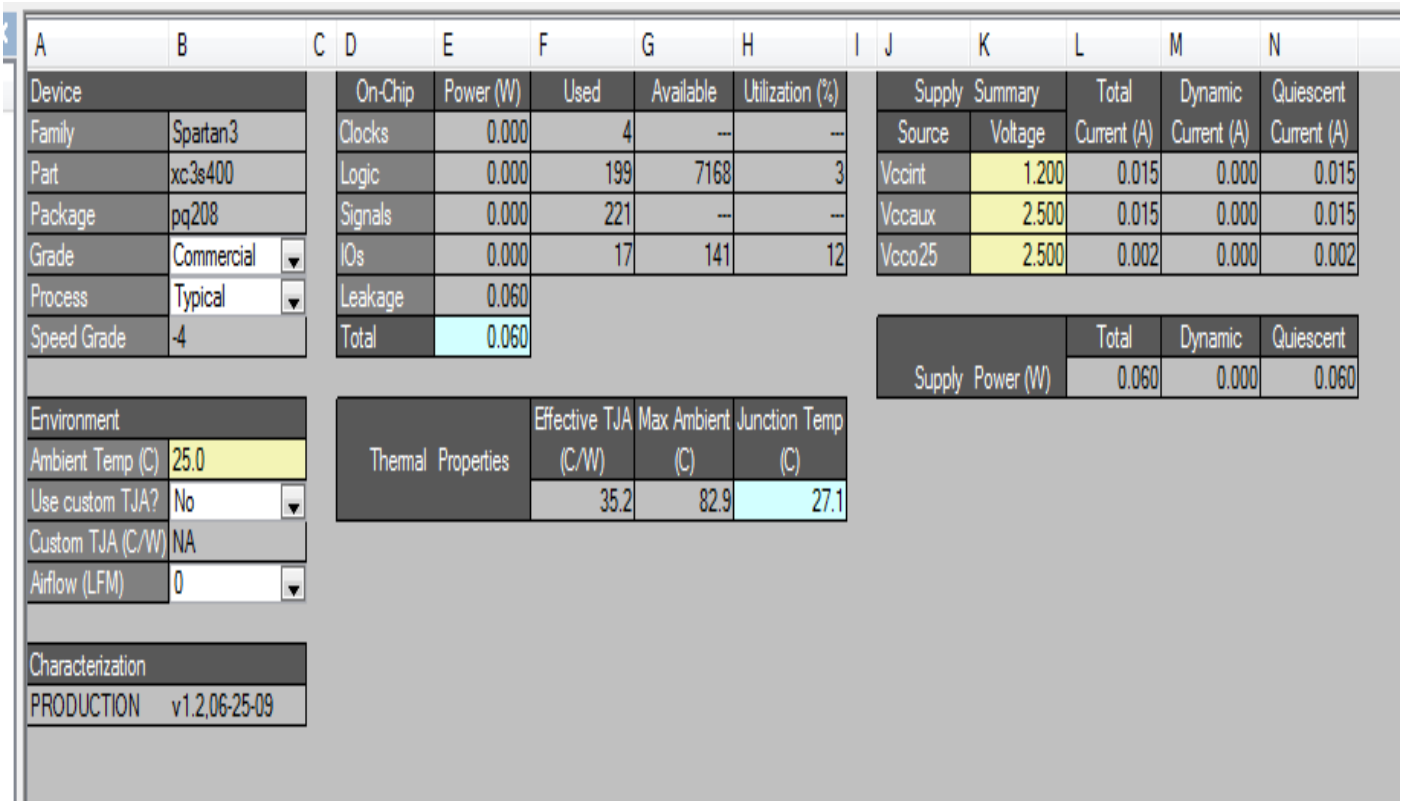
The Summary Report gives the overall synopsis of the project. It gives the information about the name of the project, project part, product family, module name, type of HDL etc., .It also gives overall view of the status of synthesis and implementation report with the number of warnings. It also states about the timing , power and utilisation .

```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : digital_clk2.ngr
Top Level Output File Name         : digital_clk2
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 17

Cell Usage :
# BELS                             : 306
#      GND                         : 1
#      INV                         : 9
#      LUT1                        : 44
#      LUT2                        : 44
#      LUT2_D                      : 1
#      LUT3                        : 19
#      LUT4                        : 85
#      LUT4_D                      : 2
#      LUT4_L                      : 1
#      MUXCY                       : 50
#      MUXF5                       : 2
#      VCC                         : 1
#      XORCY                       : 47
# FlipFlops/Latches                : 104
#      FDC                         : 53
#      FDCE                        : 20
#      FDCP                        : 1
#      LD                          : 30
# Clock Buffers                    : 3
#      BUFG                        : 2
#      BUFGP                       : 1
# IO Buffers                       : 16
#      IBUF                        : 3
#      OBUF                        : 13
=========================================================================
```

```
=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "digital_clk2.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "digital_clk2"
Output Format                      : NGC
Target Device                      : xc3s400-4-pq208

---- Source Options
Top Module Name                    : digital_clk2
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : Yes
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
Mux Extraction                     : Yes
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Multiplier Style                   : Auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 500
Add Generic Clock Buffer(BUFG)     : 8
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Yes
Use Synchronous Set                : Yes
Use Synchronous Reset              : Yes
Pack IO Registers into IOBs        : Auto
```

Power Report:

The power utilisation describes about the percentage of the power used by the code of the digital clock. From the below figure it is clear that the power used by the logic is more than the signals.



Device	
Family	Spartan3
Part	xc3s400
Package	pq208
Grade	Commercial
Process	Typical
Speed Grade	-4

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Characterization	
PRODUCTION	v1.2,06-25-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	4	---	---
Logic	0.000	199	7168	3
Signals	0.000	221	---	---
IOs	0.000	17	141	12
Leakage	0.060			
Total	0.060			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	35.2	82.9	27.1

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.015	0.000	0.015
Vccaux	2.500	0.015	0.000	0.015
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.060	0.000	0.060

Utilization Report:

The utilization Report gives the details about the utilization of number of slice registers, LUT as logic, LUT as flipflops, slices etc. The utilization is indicated in numbers or percentage.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	108	3584	3%
Number of Slice Flip Flops	98	7168	1%
Number of 4 input LUTs	205	7168	2%
Number of bonded IOBs	17	141	12%
Number of GCLKs	3	8	37%

```
Device utilization summary:
---------------------------

Selected Device : 3s400pq208-4

 Number of Slices:                      108  out of   3584     3%
 Number of Slice Flip Flops:             98  out of   7168     1%
 Number of 4 input LUTs:                205  out of   7168     2%
 Number of IOs:                          17
 Number of bonded IOBs:                  17  out of    141    12%
    IOB Flip Flops:                       6
 Number of GCLKs:                        3  out of      8    37%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

Timing Analysis:

The Timing analysis report indicates the time consumed by the digital clock design code.

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 8.708ns (Maximum Frequency: 114.837MHz)
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: 12.103ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'k1'
  Clock period: 8.708ns (frequency: 114.837MHz)
  Total number of paths / destination ports: 544 / 44
-------------------------------------------------------------------------
Delay:               8.708ns (Levels of Logic = 4)
  Source:            s1_1 (FF)
  Destination:       h2_0 (FF)
  Source Clock:      k1 rising
  Destination Clock: k1 rising

  Data Path: s1_1 to h2_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              5   0.720   1.260  s1_1 (s1_1)
     LUT4:I0->O            6   0.551   1.029  m1_cmp_eq00011 (m1_cmp_eq0001)
     LUT4:I3->O            5   0.551   0.947  s2_mux0000<0>1 (N2)
     LUT4:I3->O            6   0.551   1.029  h2_and000021 (N10)
     LUT4:I3->O            4   0.551   0.917  h2_not0001 (h2_not0001)
     FDCE:CE                   0.602          h2_0
    ----------------------------------------
    Total                      8.708ns (3.526ns logic, 5.182ns route)
                                       (40.5% logic, 59.5% route)
```

```
=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
k1(k1:O)                           | BUFG(*)(m1_0)          | 24    |
x1_or00001(x1_or00001:O)           | BUFG(*)(dis5)          | 30    |
clk                                | BUFGP                  | 47    |
h_12                               | NONE(mod_6_0)          | 3     |
-----------------------------------+------------------------+-------+
(*) These 2 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffe

Asynchronous Control Signals Information:
-----------------------------------------
-----------------------------------+------------------------+-------+
Control Signal                     | Buffer(FF name)        | Load  |
-----------------------------------+------------------------+-------+
reset                              | IBUF                   | 71    |
Mcount_mod_6_val(Mcount_mod_6_val1:O)| NONE(mod_6_0)        | 2     |
mod_6_and0000(mod_6_and00001:O)    | NONE(mod_6_1)          | 1     |
r                                  | IBUF                   | 1     |
-----------------------------------+------------------------+-------+
```

HDL Synthesis Analysis:

```
=========================================================================
HDL Synthesis Report

Macro Statistics
# ROMs                                                 : 1
 16x7-bit ROM                                         : 1
# Adders/Subtractors                                   : 5
 4-bit adder                                          : 5
# Counters                                             : 7
 12-bit up counter                                    : 1
 13-bit up counter                                    : 1
 17-bit up counter                                    : 1
 19-bit up counter                                    : 1
 22-bit up counter                                    : 1
 3-bit up counter                                     : 1
 4-bit up counter                                     : 1
# Registers                                            : 5
 4-bit register                                       : 5
# Latches                                              : 12
 1-bit latch                                          : 6
 4-bit latch                                          : 6

=========================================================================
```

```
=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# ROMs                                                 : 1
 16x7-bit ROM                                         : 1
# Adders/Subtractors                                   : 5
 4-bit adder                                          : 5
# Counters                                             : 5
 12-bit up counter                                    : 1
 13-bit up counter                                    : 1
 22-bit up counter                                    : 1
 3-bit up counter                                     : 1
 4-bit up counter                                     : 1
# Registers                                            : 20
 Flip-Flops                                           : 20
# Latches                                              : 12
 1-bit latch                                          : 6
 4-bit latch                                          : 6

=========================================================================
```

FUTURE SCOPE:

The implementation of digital clock uses all the digits of the seven-segment display and is fully functional. It has 24 hour format and we can change the 24 hour to 12 hour A.M./P.M.format.We can enhance this project to display (dd/mm/yy).We can make the alarm.