Code : 326102

MCA 1st Semester Exam., 2024

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

*(ii) There are **SEVEN** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

*(iv) Question Nos. **1** and **2** are compulsory.*

SECTION—A

1. Choose the correct answer of the following : 2×10=20

(a) In CISC architecture, most of the complex instructions are stored in

(i) CMOS

(ii) register

(iii) transistors

(iv) diodes

(b) The controller multiplexes the addresses after getting the _____ signal.

(i) INTR

(ii) ACK

(iii) RESET

(iv) Request

(c) In a 4M-bit chip organization has a total of 19 external connections, then it has _____ addresses if 8 data lines are there.

(i) 2

(ii) 5

(iii) 9

(iv) 8

(d) While using the direct mapping technique in a 16-bit system, the higher order 5 bits are used for

(i) Id

(ii) word

(iii) tag

(iv) block

(e) To increase the speed of memory access in pipelining, we make use of

(i) special memory locations

(ii) special purpose registers

(iii) cache

(iv) buffers

(f) When the processor executes multiple instructions at a time, it is said to use

(i) single issue

(ii) multiplicity

(iii) visualization

(iv) multiple issues

(g) If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have

(i) exception handling

(ii) imprecise exceptions

(iii) error correction

(iv) None of the above

(h) An interrupt that can be temporarily ignored is

(i) vectored interrupt

(ii) non-maskable interrupt

(iii) maskable interrupt

(iv) high-priority interrupt

(i) In memory-mapped I/O

(i) the I/O devices and the memory share the same address space

(ii) the I/O devices have a separate address space

(iii) the memory and I/O devices have an associated address space

(iv) a part of the memory is specifically set aside for the I/O operation

(j) The process wherein the processor constantly checks the status flags is called as

(i) polling

(ii) inspection

(iii) reviewing

(iv) echoing

SECTION—B

Answer any *four* out of *five* questions : 5×4=20

2. (a) A digital computer has a common bus system of 16 registers of 32 bits each. The bus is constructed with multiplexers.

(i) How many selection inputs are there in each multiplexer?

(ii) What size of multiplexers is needed?

(b) How do instruction set, compiler technology, CPU implementation and control, cache and memory hierarchy affect the CPU performance? Justify the effects in terms of program length, clock rate and effective CPI.

(c) Explain the *D* (Data or Delay) flip-flop. How does it differ from an *SR* flip-flop? Provide the examples of applications where *D* flip-flops are commonly used.

(d) Consider a machine with a main memory of 232 bytes having a direct-mapped cache memory of 256 Kbytes with a block size of 8 bytes.

(i) How is the 32-bit address divided into tag, line number and byte number?

(ii) In which line the data corresponding to the address EDCBA987 (H) is stored?

(e) What do you mean by asynchronous data transfer? Explain strobe controlled and handshaking mechanism for asynchronous data transfer.

SECTION—C

Answer any *three* out of *five* questions : 10×3=30

3. Mention the types of hazards that occur while executing the following instructions. Also comment on how to avoid such hazards :

(a) [1]: add r1, r2, r3
[2]: sub r3, r1, r4

(b) [1]: st r4, 20[r5]
[2]: sub r8, r9, r10
[3]: add r1, r2, 10[r3]

4. A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at the rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slowed down because of DMA transfer?

5. Explain how thread-level parallelism within a processor can be exploited. With suitable diagrams, explain simultaneous multithreading, its design challenges and potential performance enhancements.

6. What is array processor? Explain SIMD array processor with suitable example.

7. Draw the logic diagram for the 4-bit up-counter using *D* flip-flops. Show the connections between flip-flops and any additional logic gates required.

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