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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Cascade Amplifier Design

Design 1

Design a two stage RC coupled JFET amplifier to meet the following specifications $|A_V| \geq 160$, $V_{o_{rms}} = 3V$, $R_i \geq 1M\Omega$.

Solution:

1) Selection of JFET:

For above requirement, we can select JFET BFW 11 transistor from the data sheet with the following specifications:

$V_P = -2.5V$, $r_d = 50\Omega$, $I_{DSS} = 7mA$ & $g_{mo} = 5600\mu\mho$

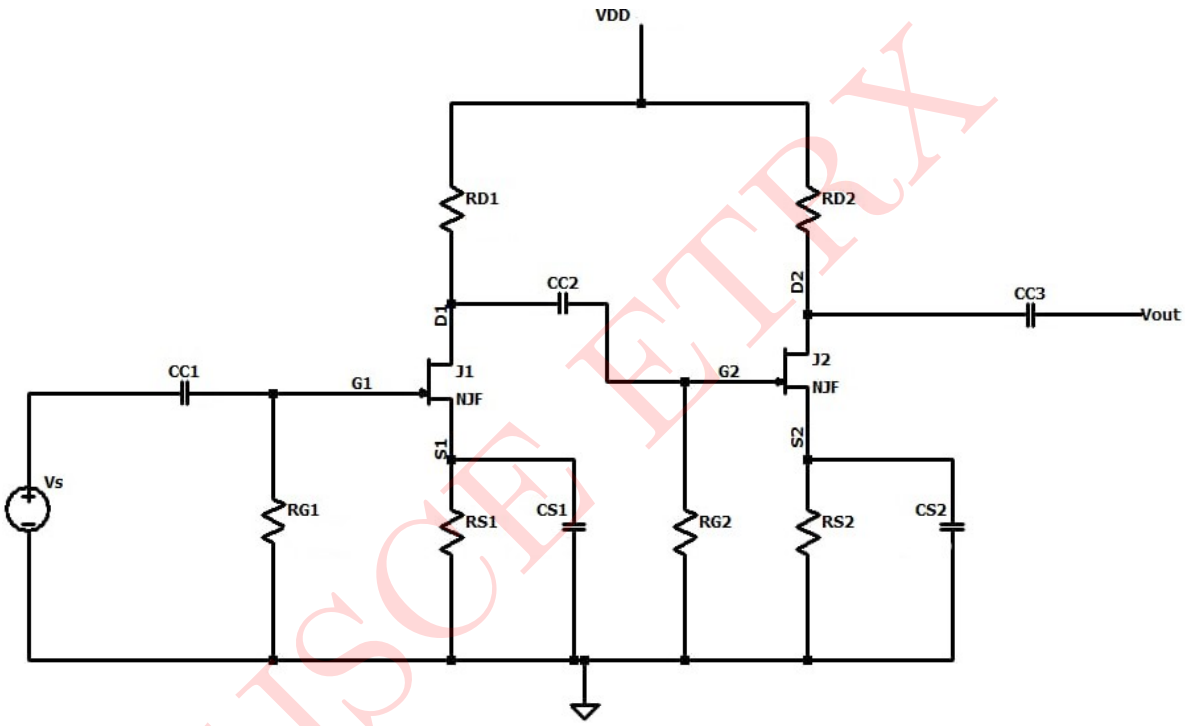

Figure 1: Circuit for Design 1

2) Selection of voltage gain:

$A_V \geq 160$ (Given)

Let $\mathbf{A_V = 180}$

Also let $A_{V_1} = 0.6A_{V_2}$

$A_V = A_{V_1} \times A_{V_2}$

$180 = 0.6A_{V_2}^2$

$A_{V_2} = \dfrac{180}{0.6}$

$\mathbf{A_{V_2} = 17.32}$

$A_{V_1} = 0.6 \times A_{V_2}$

$\mathbf{A_{V_1} = 10.39}$

Gain of 2nd Stage: $\mathbf{A_{V_2} = 18}$

Gain of 1st Stage: $\mathbf{A_{V_2} = 11}$

3) Calculation of $\mathbf{V_{GS}}$ & $\mathbf{I_D}$:

Using mid point biasing technique:

i) Calculation of I_D

For mid point biasing, $I_D = \dfrac{I_{DSS}}{2}$

i.e. $I_D = \dfrac{7mA}{2}$

$\therefore \mathbf{I_D = 3.5mA}$

ii) Calculation of V_{GS}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

i.e. $V_{GS} = V_P\left(1 - \sqrt{\dfrac{I_D}{I_{DSS}}}\right) = -2.5\left(1 - \sqrt{\dfrac{3.5}{7}}\right)$

$\mathbf{V_{GS} = -0.732V}$

iii) Calculation of g_m

$$g_m = g_{m_1} = g_{m_2} = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = 5600 \times 10^{-6}\left(1 - \frac{(-0.732)}{(-2.5)}\right)$$

$\therefore \mathbf{g_m = 3.9603m℧}$

4) Selection of $\mathbf{R_{D_2}}$:

$|A_V| = g_{m_2}(r_{d_2} \parallel R_{D_2})$ .....(1)

$r_{d_1} = r_{d_2} = r_d = 50k\Omega$

$g_m = g_{m_1} = g_{m_2} = 3.9603m℧$

From (1) we get,

$$\frac{18}{3.9603m} = \frac{R_{D_2} \times 50k}{R_{D_2} + 50k}$$

$R_{D_2} = 4.995k \approx 5k$

Select $\mathbf{R_{D_2} = 5.1k\Omega_{(std)}, 1/4W}$ .....(HSV)

5) Calculation of $\mathbf{R_{S_2}}$:

$V_{GSQ} = -I_{DQ}R_{S_2}$

$R_{S_2} = \dfrac{-V_{GSQ}}{I_{DQ}} = \dfrac{-(-0.732)}{3.5mA}$

$\therefore R_{S_2} = 209\Omega$

Select $\mathbf{R_{S_2} = 180\Omega_{(std)}, 1/4W}$.....(LSV)

6) Selection of $\mathbf{R_{G_2}}$:

To prevent loading for the 1^{st} Stage

Select $\mathbf{R_G = 1M\Omega_{(std)}, 1/4W}$

7) Selection of $\mathbf{V_{DD}}$:

$V_{DSQ} \geq V_{o_{peak}} + \mid V_P \mid$.....(Condition for undistorted output)

$V_{DSQ_2} = 1.5(V_{o_{peak}} + \mid V_P \mid)$

$V_{DSQ_2} = 1.5(V_{o_{peak}} + 2.5)$

The value is multiplied by 1.5 to take care of saturation voltages, tolerance in resistance value, variation in supply voltage and device parameter variation.

$V_{o_{rms}} = 3V$

$\therefore V_{o_{peak}} = 3\sqrt{2}$

i.e. $V_{DSQ_2} = 1.5(2.5\sqrt{2} + 2.5) = 10.05V \approx 10.1V$

Applying KVL to the JFET-2 D-S loop we get,

$V_{DD} - I_{DQ_2}R_{D_2} - V_{DSQ_2} - I_{DQ_2}R_{S_2} = 0$

$V_{DD} = V_{DSQ_2} + I_{DQ_2}(R_{D_2} + R_{S_2})$

$V_{DD} = 10.1 + 3.5 \times 10^{-3}(0.18k + 5.1k)$

$\therefore V_{DD} = 28.58V$

Select $\mathbf{V_{DD} = 30V}$

8) Selection of $\mathbf{R_{D_1}}$:

$|A_{V_2}| = g_{m_2}(r_{d_2} \parallel R_{D_2})$

$|A_{V_2}| = 3.9603 \times 10^{-3}(50k \parallel 5.1k)$

$|A_{V_2}| = 18.3281$

$|A_{V_1}| = \dfrac{A_V}{|A_{V_2}|} = \dfrac{180}{18.3281}$

$|A_{V_1}| = 9.82$

let $|A_{V_1}| = 10$

$|A_{V_1}| = g_{m_1}(r_{d_1} \parallel R_{D_1} \parallel R_{G_2})$

$10 = 3.9603 \times 10^{-3}(50k \parallel R_{D_1} \parallel 1M)$

$R_{D_1} = 2.665k\Omega$

Select $\mathbf{R_{D_1} = 3.3k\Omega_{(std)}, 1/4W}$.....(HSV)

9) Calculation of $\mathbf{R_{S_1}}$:

$V_{GSQ} = -I_{DQ}R_{S_1}$

$R_{S_1} = \dfrac{-V_{GSQ}}{I_{DQ}} = \dfrac{-(-0.732)}{3.5mA}$

$\therefore R_{S_1} = 209\Omega$

Select $\mathbf{R_{S_1} = 180\Omega_{(std)}, 1/4W}$.....(LSV)

10) Selection of $\mathbf{C_{C1}}$:

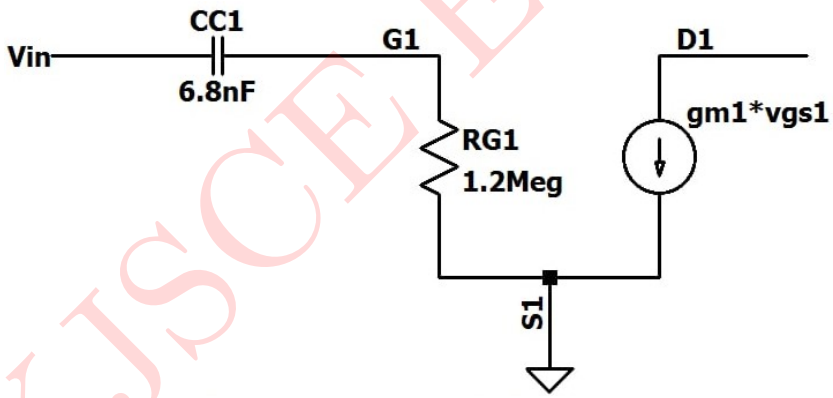

Figure 2: Small Signal Equivalent Circuit for C_{C1}

$C_{C1} = \dfrac{1}{2\pi f_{L_{CC1}} R_{eq}}$

$f_{C_{C1}} = f_L = 20Hz$

$R_{eq} = R_{G_1} = 1.2M\Omega$

$C_{C1} = \dfrac{1}{2\pi \times 20 \times 1.2M\Omega} = 6.63nF$

Select $\mathbf{C_{C1}}$ = 6.8nF/60V....(H.S.V)

11) Selection of $\mathbf{C_{C2}}$:

$C_{C2} = \dfrac{1}{2\pi f_{L_{CC2}} R_{eq}}$

$f_{L_{CC2}} = f_L = 20Hz$

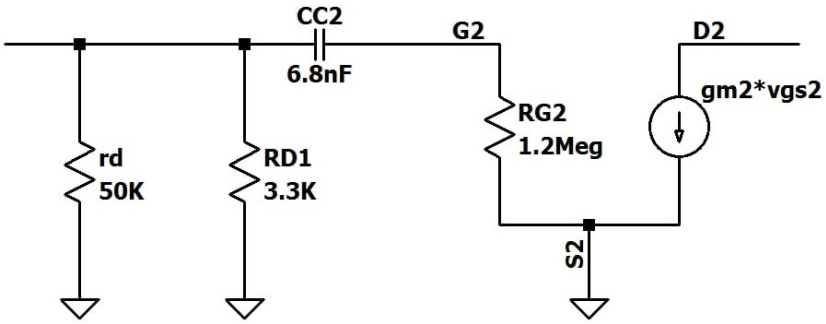

Figure 3: Small Signal Equivalent Circuit for C_{C2}

$R_{eq} = r_{d_1}||R_{D_1} + R_{G_2}$

$R_{eq} = 50k||4.7k + 1M\Omega$

$R_{eq} = 4.296k + 1M\Omega = 1.0043M\Omega$

$C_{C2} = \dfrac{1}{2\pi \times 20 \times 1.0043M\Omega}$

$C_{C2} = 7.92nF$

Select $\mathbf{C_{C2}}$ = 8.2nF/60V.....(H.S.V)

12) <u>Selection of $\mathbf{C_{C3}}$:</u>

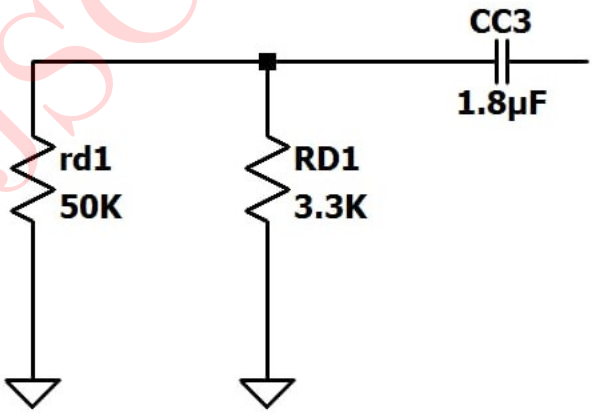

Figure 4: Small Signal Equivalent Circuit for C_{C3}

$C_{C3} = \dfrac{1}{2\pi f_{L_{CC3}} R_{eq}}$

$f_{L_{CC3}} = f_L = 20Hz$

$R_{eq} = r_{d_2}||R_{D_2}$

$R_{eq} = 50k||5.1k$

$R_{eq} = 4.6279k\Omega$

$$C_{C3} = \frac{1}{2\pi \times 20 \times 4.6279k\Omega}$$

$$C_{C3} = 1.7195\mu F$$

Select $\mathbf{C_{C3}} = \mathbf{1.87\mu F/60V}$.....(H.S.V)

12) Selection of Bypass capacitor:

$$C_{S_1} = C_{S_2} = \frac{1}{2\pi f_L R_{eq}}$$

$$f_L = 20Hz$$

$$R_{eq} = \frac{1}{g_m} \parallel R_S$$

$$R_{eq} = 252.51||180$$

$$R_{eq} = 0.105k\Omega$$

$$C_{S_1} = C_{S_2} = \frac{1}{2\pi \times 20 \times 0.1051k\Omega}$$

$$C_{S_1} = C_{S_2} = 75.7250\mu F$$

Select $\mathbf{C_{S_1}} = \mathbf{C_{S_2}} = \mathbf{100\mu F/60V}$.....(H.S.V)

13) Designed circuit:

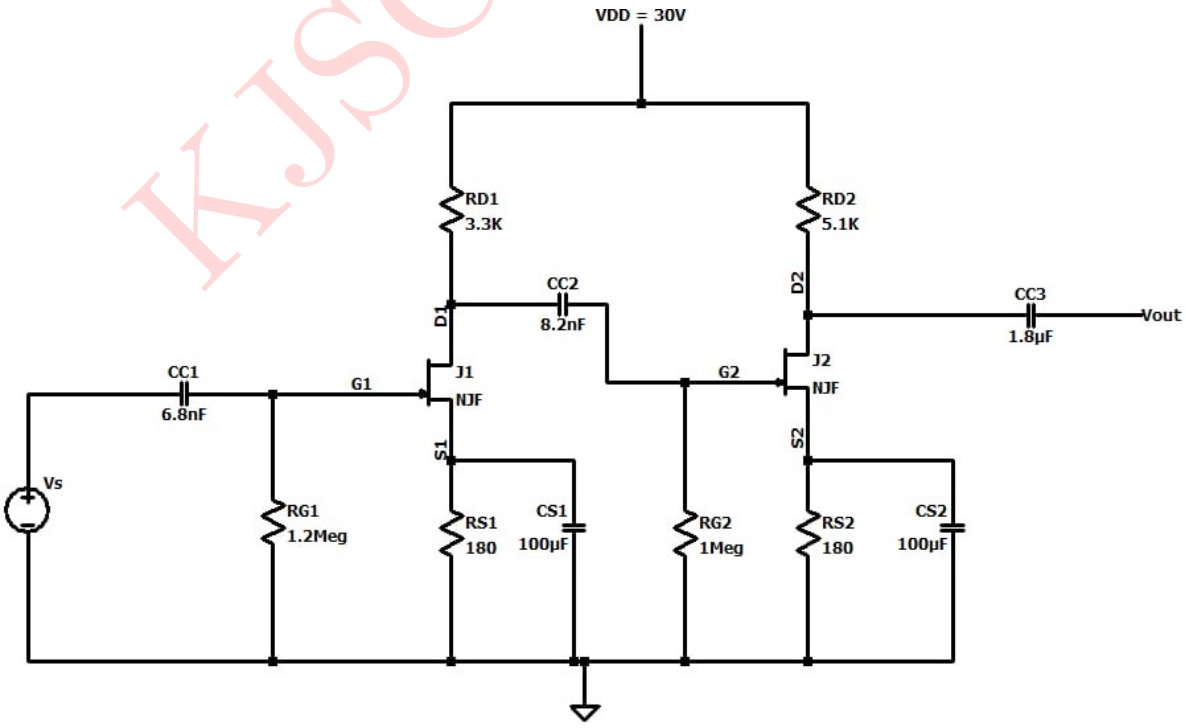

Figure 5: Designed JFET Amplifier Circuit using Mid-Point Biasing Technique

Calculation of Z_i & Z_o

From figure 2 we get,

$Z_i = R_{G_1}$

$\mathbf{Z_i = 1.2M\Omega}$

$Z_o = r_{d_2} \parallel R_{D_2} = 50k \parallel 5.1k$

$\mathbf{Z_o = 4.679k\Omega}$

Calculation of overall voltage gain:

$$g_{m_1} = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_{m_1} = \frac{2 \times 7mA}{2.5V}\left(1 - \frac{0.732}{2.5}\right)$$

$g_m = g_{m_1} = g_{m_2} = 3.96mA/V$

$A_{V_1} = -g_m(r_{d_1} \parallel R_{D_1} \parallel R_{G_2})$

$A_{V_1} = -3.96mA/V \times (50k \parallel 3.3k \parallel 1M)$

$\mathbf{A_{V_1} = -12.22}$

$A_{V_2} = -g_m(r_{d_2} \parallel R_{D_2})$

$A_{V_2} = -3.96mA/V(50k \parallel 5.1k)$

$\mathbf{A_{V_2} = -18.326}$

$A_{V_T} = A_{V_1} \times A_{V_2}$

$A_{V_T} = -12.22 \times -18.326 = 223.94$

$|A_{V_T}|(dB) = 20log_{10}(A_{V_T}) = 20log_{10}(223.94)$

$\mathbf{|A_{V_T}|(dB) = 47dB}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

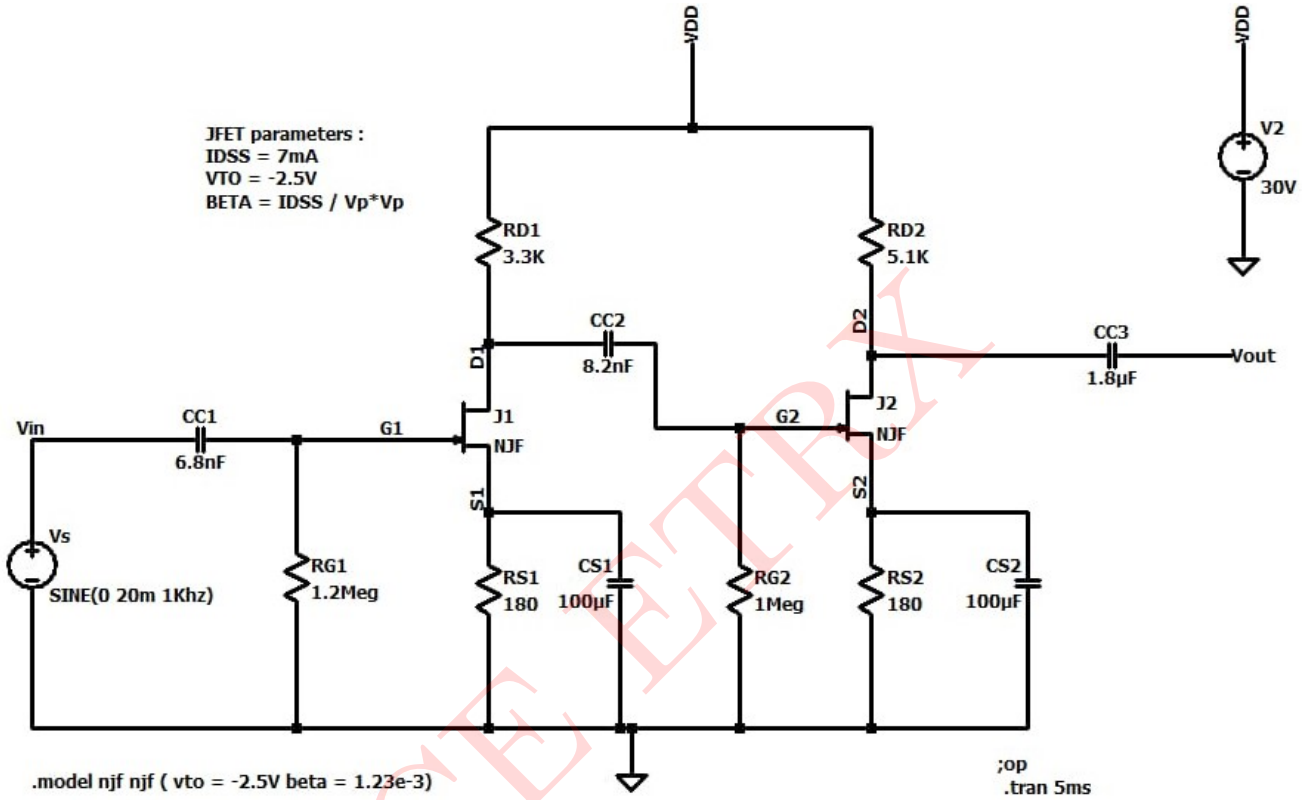

Figure 6: Circuit Schematic: Results

Output Waveforms:

The input and output waveforms are shown in figure 4 and figure 5

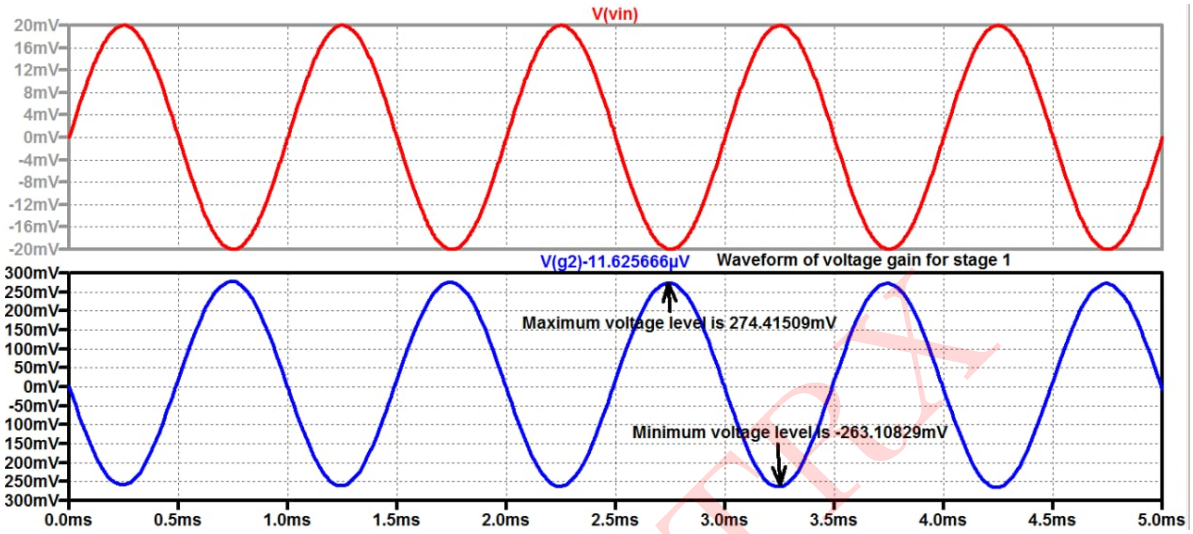

Figure 7: Input and Output Waveforms for 1^{st} Stage

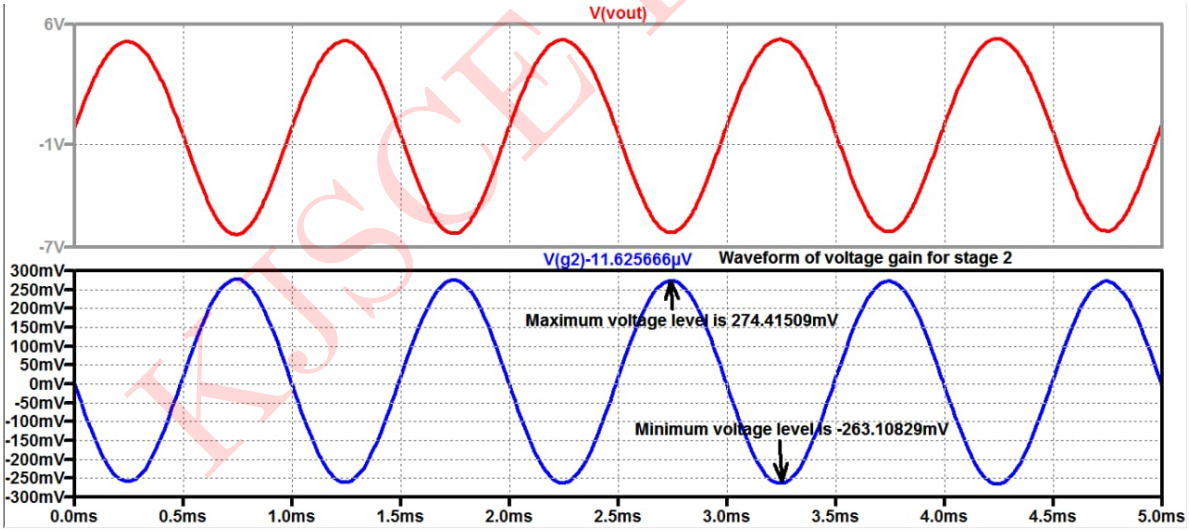

Figure 8: Input and Output Waveforms 2^{nd} Stage

Comparison between theoretical and simulated values is given below:

Parameters	**Simulated Values**	**Theoretical Values**
Stage 1: I_{D_1}	$3.6mA$	$3.5mA$
Stage 1: V_{GS_1}	$-0.7318V$	$-0.732V$
Stage 2: I_{D_2}	$3.6mA$	$3.5mA$
Stage 2: V_{GS_1}	$-0.7318V$	$-0.732V$
Voltage gain of first stage $\|A_{V_1}\|$	13.443	> 11
Voltage gain of second stage $\|A_{V_2}\|$	20.84	> 18
Overall voltage gain A_V(dB)	48.96	47
Input Impedance Z_i	–	$1.2M\Omega$
Output Impedance Z_o	–	$4.6279k\Omega$

Table 1: Design 1

Design 2

Design a two stage RC coupled amplifier to meet the following specifications $A_V \geq 650$, $V_{CC} = 18V$, $S \leq 10$, $R_i \geq 1M\Omega$.

Solution:

Above requirements can be fulfilled by CS-CE stage.

Selecting CS as 1^{st} stage since $R_i \geq 1M\Omega$

1) Circuit Diagram:

Select: BC147B

$h_{fe}(typ) = 330$, $h_{FE}(typ) = 290$, $h_{ie} = 4.5k\Omega$, $V_{CE_{sat}} = 0.25V$

Select BFW11:

$V_P = -2.5V$, $r_d = 50\Omega$, $I_{DSS} = 7mA$ & $g_{mo} = 5600\mu\mho$

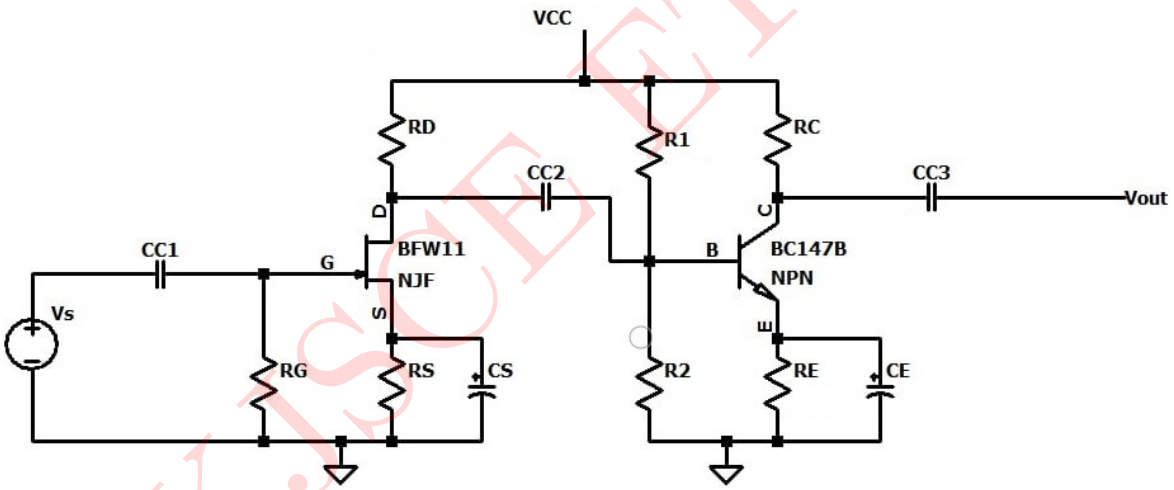

Figure 9: Circuit for Design 2

2) Selection of voltage gains:

$A_V \geq 650$ (Given)

let $\mathbf{A_{V_1} = 4}$ (Since JFET amplifier gain is less)

$$A_{V_2} = \frac{650}{4}$$

$$A_{V_2} = 162.5$$

let $\mathbf{A_{V_2} = 170}$

Design of 2nd stage

3) Selection of $\mathbf{R_C}$:

$$|A_{V_2}| = \frac{h_{fe}(typ) \times R_C}{h_{ie}}$$

$$170 = \frac{330 \times R_C}{4.5k}$$

$$R_C = 2.3k\Omega$$

Select $\mathbf{R_C = 2.4k\Omega_{(std)}, 1/4W}$.....(HSV)

4) Selection of Q-Point:

$$V_{CC} = 18V$$

$$\text{let } V_{CEQ} = \frac{V_{CC}}{2} = \frac{18}{2}$$

$$\mathbf{V_{CEQ} = 9V}$$

$$V_{R_E} = 0.1 \times V_{CC} = 0.1 \times 18$$

$$\mathbf{V_{R_E} = 1.8V}$$

Applying KVL to the C-E loop of BJT

$$V_{CC} - V_{R_C} - V_{CEQ} - V_{R_E} = 0$$

$$V_{R_C} = V_{CC} - V_{CEQ} - V_{R_E} = 18 - 9 - 1.8$$

$$\mathbf{V_{R_C} = 7.2V}$$

$$I_{CQ}R_C = V_{R_C} = 7.2$$

$$I_{CQ} = \frac{V_{R_E}}{R_C} = \frac{7.2}{2.4k}$$

$$\mathbf{I_{CQ} = 3mA}$$

5) Selection of $\mathbf{R_E}$:

$$I_{CQ}R_E = V_{R_E} = 1.8V$$

$$R_E = \frac{V_{R_E}}{I_{CQ}} = \frac{1.8}{3mA}$$

$$\mathbf{R_E = 0.6k\Omega}$$

Select $\mathbf{R_E = 560\Omega_{(std)}, 1/4W}$.....(LSV)

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{3mA}{290}$$

$$\mathbf{I_{BQ} = 10.34\mu A}$$

$I_E = I_B + I_C = 3 + 0.010$

$\mathbf{I_E = 3.01mA}$

6) Selection of biasing resistors:

$S \leq 10$

$\beta = 290$

let $S = 10$

$$S = \frac{1+\beta}{1+\beta \times \left[\frac{R_E}{R_B + R_E}\right]}$$

$$10 = \frac{1+290}{1+290\left[\frac{560}{560+R_B}\right]}$$

$\mathbf{R_B = 5.219k\Omega}$

$$R_B = R_1 \parallel R_2 = \frac{R_1 \times R_2}{R_1 + R_2} = 5.219k\Omega \quad .....(1)$$

$$V_B = V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC} \quad .....(2)$$

Applying KVL at BE loop of BJT,

$V_B - I_{BQ}R_B - V_{BE} - I_{EQ}R_E = 0$

$$V_B = \frac{I_C}{\beta} \times R_B + V_{BE} + I_{CQ}R_E$$

$$V_B = \frac{3mA}{290} \times 5.219k + 0.7 + 3mA \times 560$$

$\mathbf{V_B = 2.434V}$

From (2) we get,

$$V_B = 2.434 = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$V_B = 2.434 = \frac{R_2}{R_1 + R_2} \times 18V$$

$$\frac{R_2}{R_1 + R_2} = 0.1352 \quad .....(3)$$

$V_E = I_E R_E = 3.01mA \times 560$

$\mathbf{V_E = 1.6856V}$

Substituting (3) in (1) we get,

$R_1 \times (0.1352) = 5.219k$

$R_1 = 38.60k\Omega$

Select $\mathbf{R_1 = 39k\Omega_{(std)}, 1/4W}$.....(HSV)

From (3) $\dfrac{R_2}{R_1 + R_2} = 0.1352$

$\dfrac{R_2}{39k + R_2} = 0.1352$

$R_2 = 6k\Omega$ (Select HSV only for CS-CE)

Select $\mathbf{R_2 = 6.2k\Omega_{(std)}, 1/4W}$.....(HSV)

7) Calculation of Q-Point:

Using mid point biasing technique:

i) Calculation of I_D

For mid point biasing, $I_D = \dfrac{I_{DSS}}{2}$

i.e. $I_D = \dfrac{7mA}{2}$

$\therefore \mathbf{I_D = 3.5mA}$

ii) Calculation of V_{GS}

$I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2$

i.e. $V_{GS} = V_P\left(1 - \sqrt{\dfrac{I_D}{I_{DSS}}}\right) = -2.5\left(1 - \sqrt{\dfrac{3.5}{7}}\right)$

$\mathbf{V_{GS} = -0.732V}$

iii) Calculation of g_m

$g_m = g_{m_1} = g_{m_2} = g_{mo}\left(1 - \dfrac{V_{GS}}{V_P}\right) = 5600 \times 10^{-6}\left(1 - \dfrac{(-0.732)}{(-2.5)}\right)$

$\therefore \mathbf{g_m = 3.9603m\mho}$

4) Selection of $\mathbf{R_D}$:

$|A_{V_2}| = \dfrac{h_{fe}(typ) \times R_C}{h_{ie}}$

$|A_{V_2}| = \dfrac{330 \times 2.4k}{4.5k}$

$|A_{V_2}| = 176$

$|A_{V_1}| = \dfrac{A_V}{|A_{V_2}|} = \dfrac{650}{176} = 3.69$

$|A_{V_1}| = g_{m_1}[R_D \parallel r_d \parallel R_1 \parallel R_2 \parallel h_{ie}]$

$R_{L_1} = r_d \parallel R_1 \parallel R_2 \parallel h_{ie} = 50k \parallel 39k \parallel 6.2k \parallel 4.5k$

$R_{L_1} = 2.397k\Omega$

$|A_{V_1}| = 3.69 = g_{m_1}[R_D \parallel 2.397k]$

$\mathbf{R_D = 1.5k\Omega_{(std)}, 1/4W}$

9) Calculation of $\mathbf{R_S}$:

$V_{GSQ} = -I_{DQ}R_S$

$R_S = \dfrac{-V_{GSQ}}{I_{DQ}} = \dfrac{-(-0.732)}{3.5mA}$

$\therefore R_S = 209\Omega$

Select $\mathbf{R_S = 180\Omega_{(std)}, 1/4W}$.....(LSV)

10) Selection of $\mathbf{R_G}$:

Since $R_1 = 1M\Omega$, to prevent loading we take $R_G > 1M\Omega$

Select $\mathbf{R_G = 1.2M\Omega_{(std)}, 1/4W}$

11) Selection of $\mathbf{C_{C1}}$:

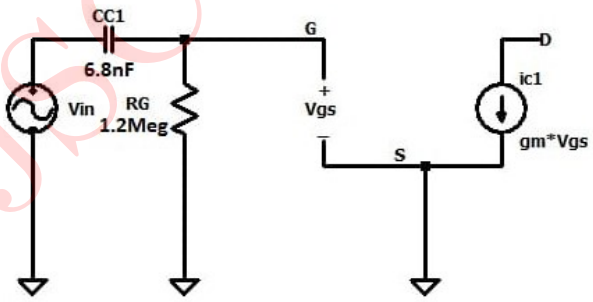

Figure 10: Low Frequency Equivalent Circuit for C_{C1}

$C_{C1} = \dfrac{1}{2\pi f_{L_{CC1}} R_{eq}}$

$f_{C_{C1}} = f_L = 20Hz$ (Assume $f_L = 20Hz$)

$R_{eq} = R_{G_1} = 1.2M\Omega$

$C_{C1} = \dfrac{1}{2\pi \times 20 \times 1.2M\Omega} = 6.63nF$

Select $\mathbf{C_{C1}}$ = 6.8nF/50V....(H.S.V)

11) Selection of C_{C2}:

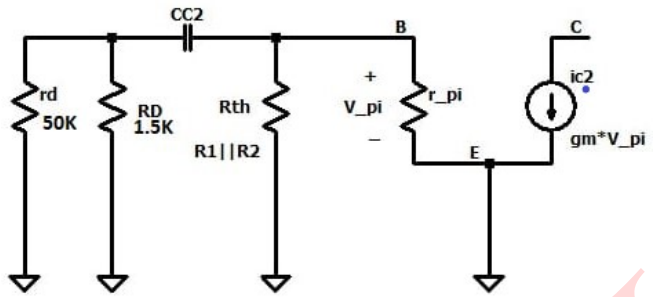

Figure 11: Low Frequency Equivalent Circuit for C_{C2}

$$C_{C2} = \frac{1}{2\pi f_{L_{CC2}} R_{eq}}$$

$$f_{L_{CC2}} = f_L = 20Hz$$

$$R_{eq} = r_{d_1} || R_{D_1} + R_1 \parallel R_2 \parallel h_{ie}$$

$$R_{eq} = 50k || 1.5k + 39k \parallel 6.2k \parallel 4.5k\Omega$$

$$R_{eq} = 1.456k + 2.446k\Omega = 3.902k\Omega$$

$$C_{C2} = \frac{1}{2\pi \times 20 \times 3.902k\Omega}$$

$$C_{C2} = 2.060\mu F$$

Select $C_{C2} = 2.2\mu F/50V$.....(H.S.V)

12) Selection of C_{C3}:

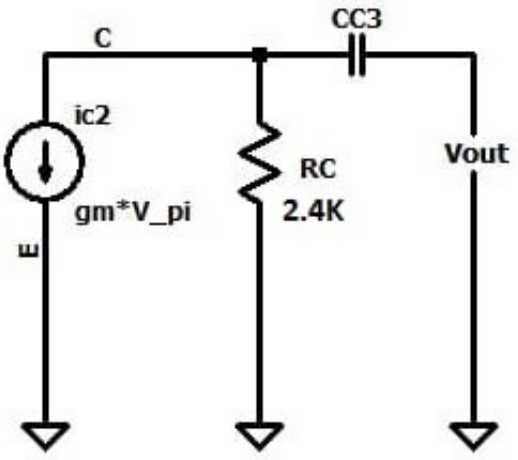

Figure 12: Low Frequency Equivalent Circuit for C_{C3}

$$C_{C3} = \frac{1}{2\pi f_{L_{CC3}} R_{eq}}$$

$f_{L_{CC3}} = f_L = 20Hz$

$R_{eq} = R_C$

$R_{eq} = 2.4k\Omega$

$$C_{C3} = \frac{1}{2\pi \times 20 \times 2.4k\Omega}$$

$C_{C3} = 3.31\mu F$

Select $\mathbf{C_{C3}} = \mathbf{3.9\mu F/50V}$.....(H.S.V)

12) Selection of Bypass capacitor:

$$C_{S_1} = C_{S_2} = \frac{1}{2\pi f_L R_{eq}}$$

$f_L = 20Hz$

$$R_{eq} = \frac{1}{g_m} \parallel R_S$$

$R_{eq} = 252.51||180$

$R_{eq} = 105.09\Omega$

$$C_{S_1} = C_{S_2} = \frac{1}{2\pi \times 20 \times 105.09\Omega}$$

$C_{S_1} = C_{S_2} = 75.7250\mu F$

Select $\mathbf{C_{S_1}} = \mathbf{C_{S_2}} = \mathbf{82\mu F/50V}$.....(H.S.V)

$X_{CE} = 0.1R_E$ (Ensures complete bypass of R_E)

$$C_E = \frac{1}{2\pi \times f_L \times 0.1R_E}$$

$$C_E = \frac{1}{2\pi \times 20 \times 0.1}$$

$C_E = 284.34\mu F$

Select $\mathbf{C_E} = \mathbf{330\mu F/50V}$.....(HSV)

12) Small Signal Analysis:

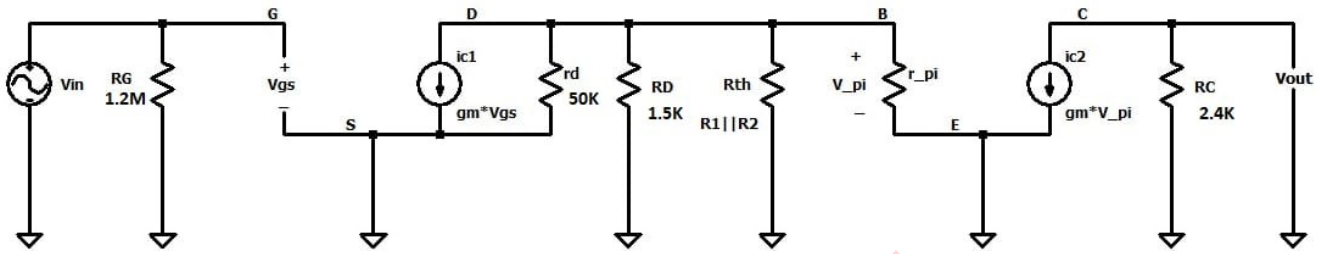

Figure 13: Small Signal Equivalent Circuit

Calculation of Z_i & Z_o

From figure 2 we get,

$Z_i = R_G$

$\mathbf{Z_i = 1.2M\Omega}$

$Z_o = R_C$

$\mathbf{Z_o = 2.4k\Omega}$

$$g_{m_2} = \frac{I_{CQ}}{V_T} = \frac{3mA}{26mV}$$

$\mathbf{g_{m_2} = 115.384mA/V}$

Calculation of A_{V_2}:

$$A_{V_2} = \frac{V_{out}}{V_1} = \frac{-g_{m_2} V_\pi R_C}{V_\pi} = -g_{m_2} R_C$$

$A_{V_2} = -115.384mA/V \times 2.4k$

$\mathbf{A_{V_2} = -276.92}$

Calculation of A_{V_1}:

$$A_{V_1} = \frac{V_1}{V_{in}} - g_{m_1} V_{gs} (r_d \parallel R_D \parallel R_{th} \parallel r_\pi)$$

$$r_\pi = \frac{\beta \times V_T}{I_C} = \frac{290 \times 26mV}{3}$$

$\mathbf{r_\pi = 2.513k\Omega}$

$A_{V_1} = -3.96 \times 10^{-3} (50k \parallel 1.5k \parallel 5.34k \parallel 2.513k)$

$\mathbf{A_{V_1} = -3.113}$

Calculation of overall voltage gain:

$A_{V_T} = A_{V_1} \times A_{V_2} = (-276.92) \times (-3.113)$

$\mathbf{A_{V_T} = 862.05}$

$A_{V_T}(dB) = 20log_{10}(A_{V_T}) = 20log_{10}(862.05)$

$\mathbf{A_{V_T}(dB) = 58.71dB}$

13) Designed circuit:

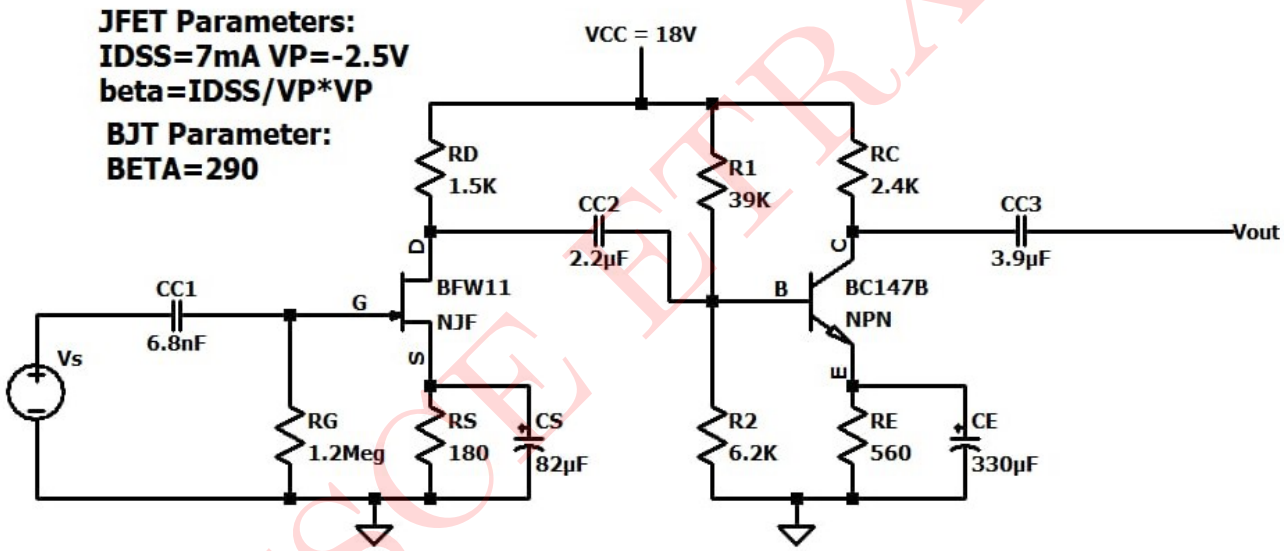

Figure 14: Designed Circuit

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

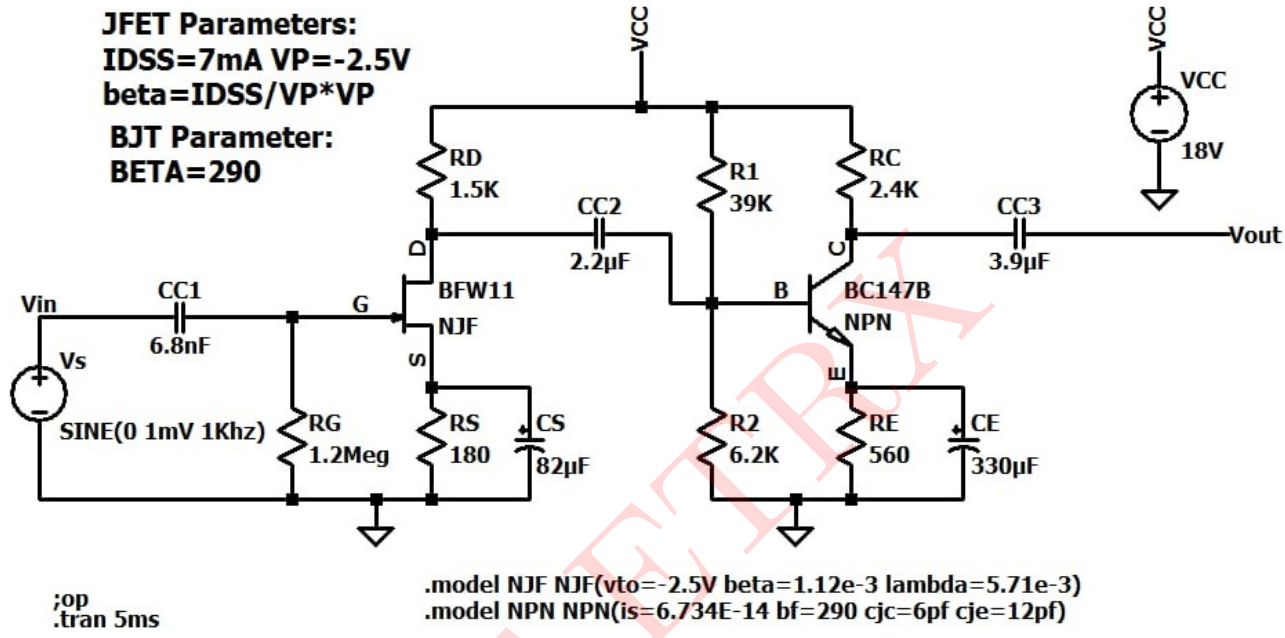

Figure 15: Circuit Schematic: Results

The input and output waveforms are shown in figure 8 and figure 9

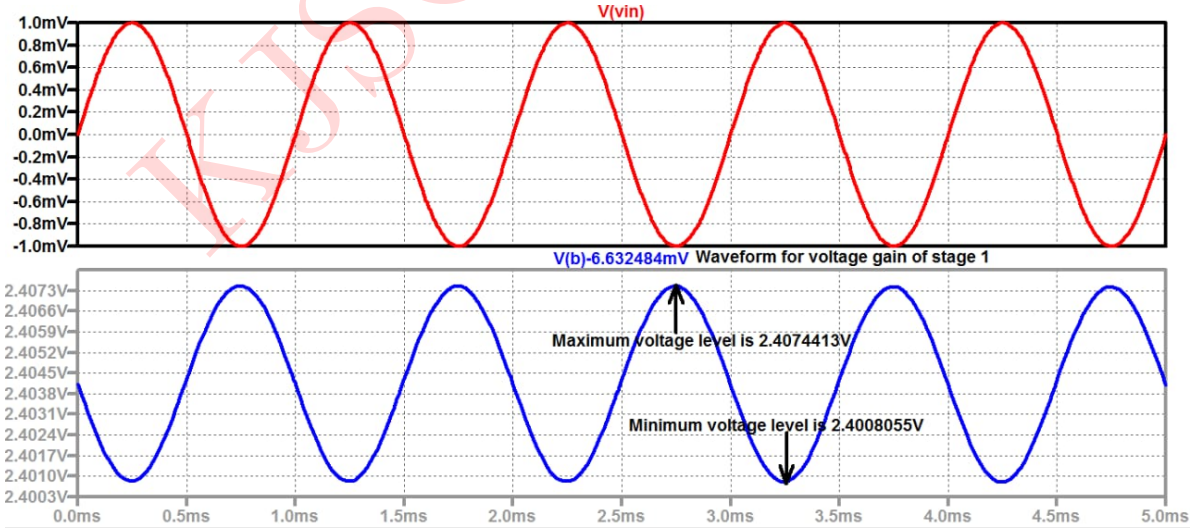

Figure 16: Input and Output Waveforms for 1^{st} Stage

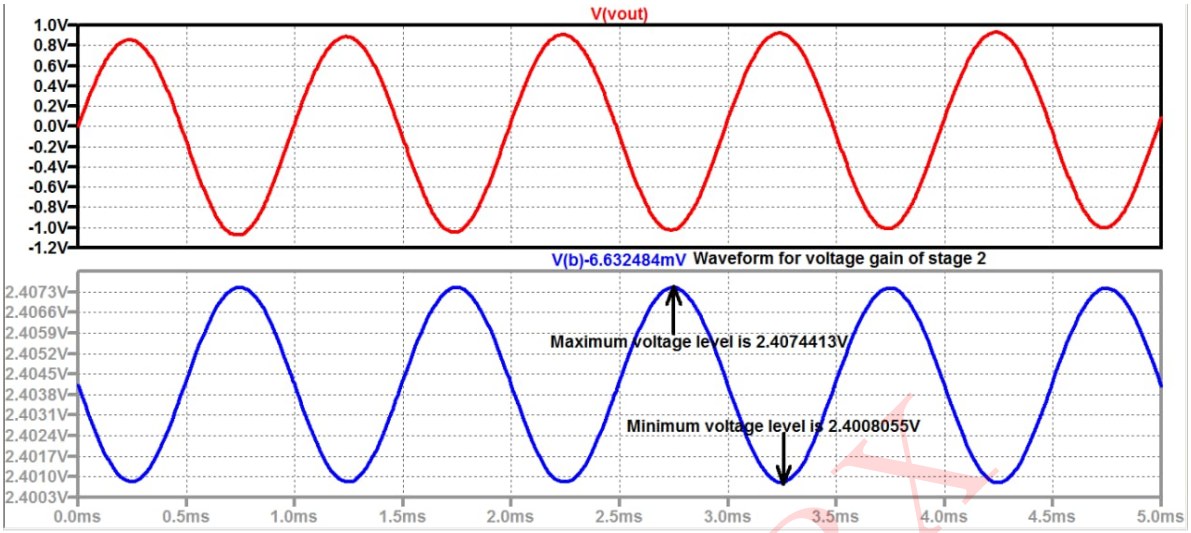

Figure 17: Input and Output Waveforms 2^{nd} Stage

Comparison between theoretical and simulated values is given below:

Parameters	**Simulated Values**	**Theoretical Values**
Stage 1: I_{DQ}	$3.87mA$	$3.5mA$
Stage 1: V_{GSQ}	$-0.691V$	$-0.732V$
Stage 2: I_B	$10.89\mu A$	$10.34\mu A$
Stage 2: I_C	$3.1mA$	$3mA$
Stage 2: I_E	$3.1mA$	$3.01mA$
Stage 2: V_E	$1.77V$	$1.68V$
Stage 2: V_B	$2.41V$	$2.434V$
Voltage gain of first stage A_{V_1}	-3.41	-3.113
Voltage gain of second stage A_{V_2}	-290.1	-276.92
Overall voltage gain A_V(dB)	$59.9dB$	$58.71dB$
Input Impedance Z_i	–	$1.2M\Omega$
Output Impedance Z_o	–	$2.4k\Omega$

Table 2: Design 2

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