K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Diode Application

Numerical 1:

For the circuit shown in figure 1, plot

a. Input $V_{IN}(t)$ & output $V_{OUT}(t)$ waveforms

b. VTC curve

Given : $V_{IN}(t) = 10V_{p-p}$ sinusoidal signal with frequency of 5000Hz. Use constant voltage model i.e $V_{D,ON} = 0.7V$, $V_B = 1V$, $R_1 = 1\text{k}\Omega$

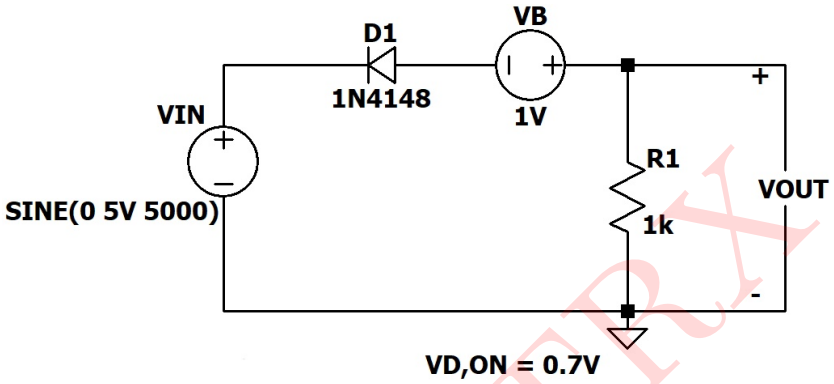


Figure 1: Circuit 1

Solution: Assuming a constant voltage model for D_1, i.e $V_{D,ON} = 0.7V$

$V_{IN} = V_m \sin \omega t = 5 \sin(2\pi \times 5000)t = 5 \sin(10000\pi t)$

In the given circuit 1, during the positive half cycle the diode D_1 is reverse biased since the voltage at the positive terminal of diode is

$-V_{D,ON} - V_B = -0.7 - 1 = -1.7V$

While for the positive half cycle the voltage at the negative terminal is always greater than 0

$\therefore V_{IN} > (-V_{D,ON} - V_B) \Rightarrow V_{IN} > -1.7V$

$\therefore$ Diode D_1 is reverse biased and turns OFF

Hence the circuit becomes,

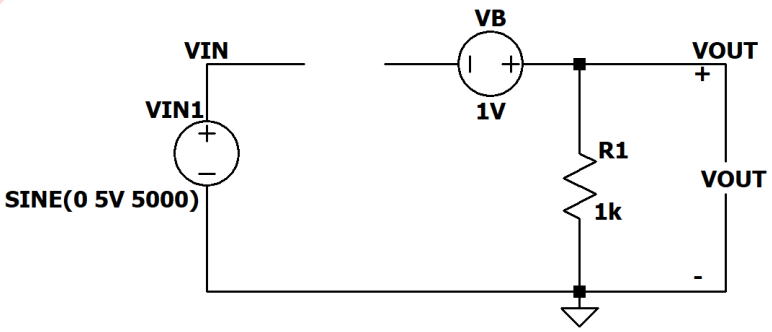


Figure 2: When diode is OFF

From the figure 2 we can observe, $V_{OUT} = 0V$

Now, for the negative half cycle diode D_1 is forward biased only when the voltage at the positive terminal of D_1 is greater than the voltage at the negative terminal.

The voltage at the positive terminal of D_1 is,

$-V_{D,ON} - V_B = -0.7 - 1 = -1.7V$

The voltage at the negative terminal is given by V_{IN}

$\therefore$ for $V_{IN} < (-V_{D,ON} - V_B)$

i.e $V_{IN} < -1.7V$

The diode D_1 is forward biased and turns ON.

Hence the circuit becomes,

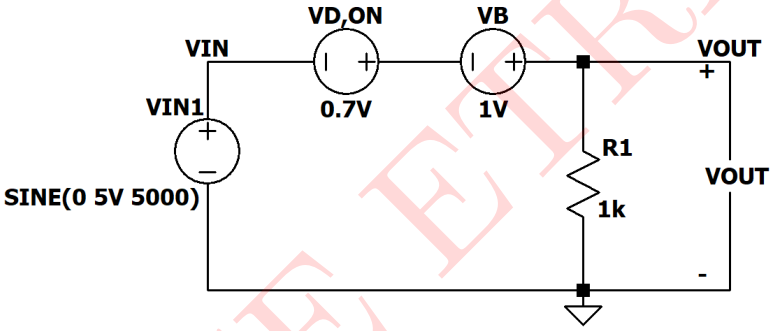


Figure 3: When diode is ON

Applying KVL,

$V_{IN} - V_{D,ON} - V_B - V_{OUT} = 0$

$V_{OUT} = V_{IN} + (V_{D,ON} + V_B)$

Maximum input voltage in negative half cycle is,

$V_{IN} = -V_m = -5V$

$V_{OUT} = -V_m + (V_{D,ON} + V_B)$

$= -5 + (0.7 + 1)$

$= \mathbf{-3.3V}$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

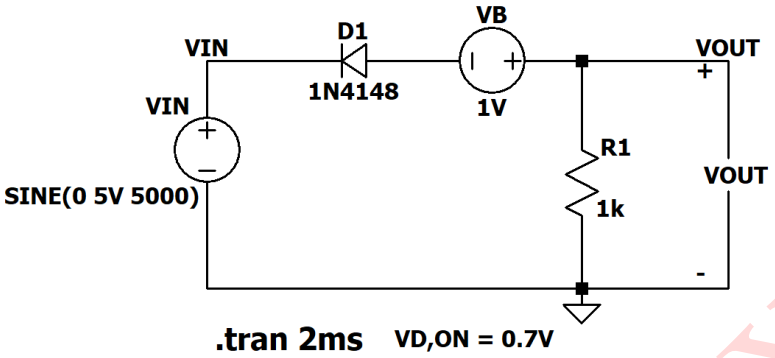


Figure 4: Circuit Schematic

The input and output waveform are shown in figure 5

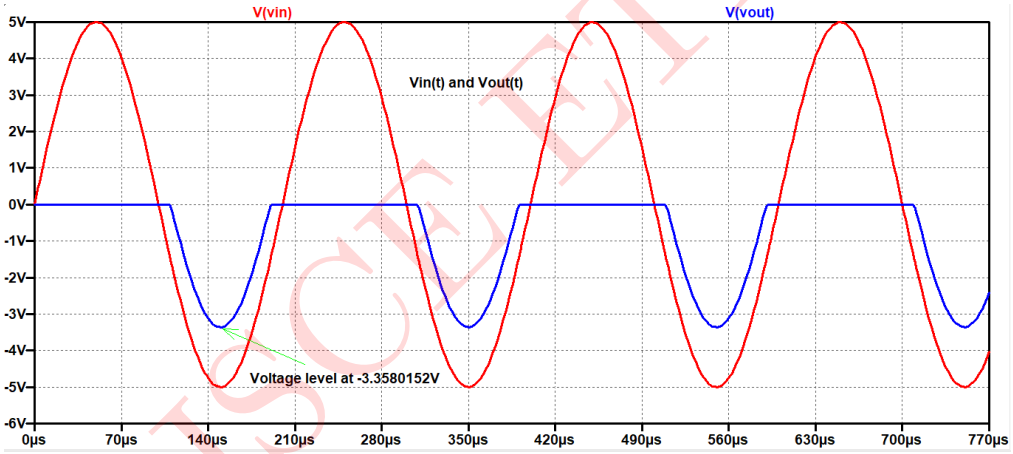


Figure 5: $V_{IN}(t)$ & $V_{OUT}(t)$

The VTC curve for the following circuit is shown in figure 6

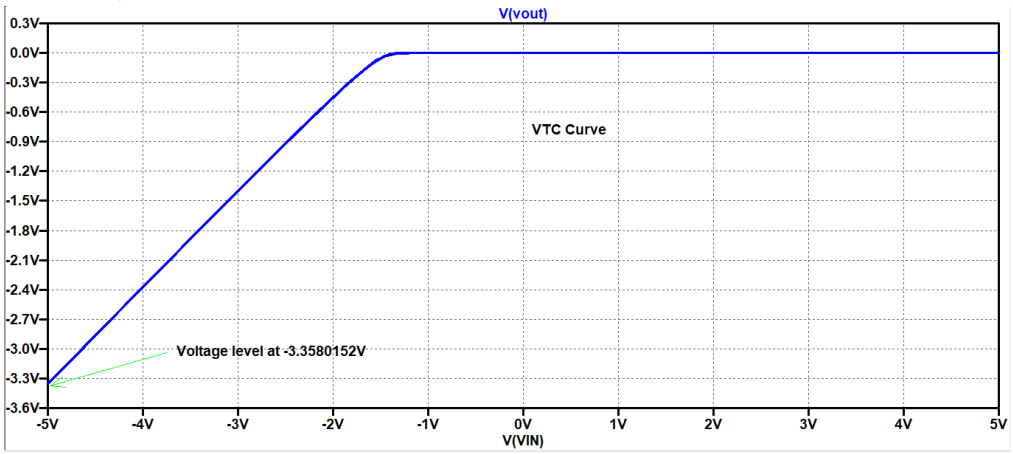


Figure 6: VTC curve

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
Maximum value output clipped voltage level	$-3.3V$	$-3.3580152V$

Table 1: Numerical 1

Numerical 2:

For the circuit shown in figure 7,

Plot: Input $V_{IN}(t)$ & output $V_{OUT}(t)$ waveforms

Given : $V_{IN}(t) = 40V_{p-p}$ sinusoidal signal with frequency of 1000Hz.

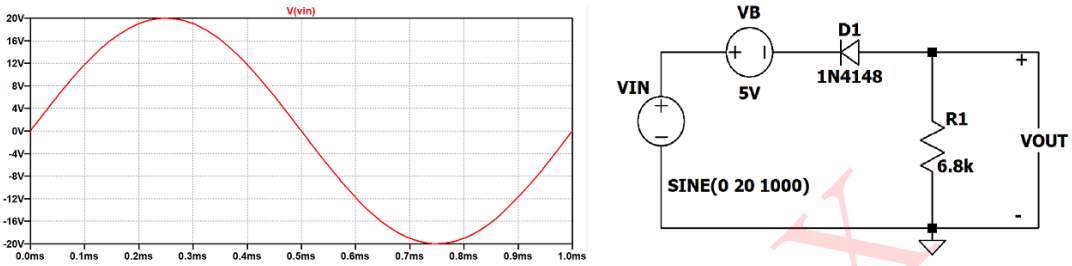


Figure 7: Circuit 2

Solution: The given circuit 2 is a constant voltage model i.e $V_{D,ON} = 0.7V$

$V_{IN} = V_m \sin \omega t = 20 \sin(2\pi \times 1000)t = 20 \sin(2000\pi t)$

In the above circuit, the diode D_1 is forward biased when the voltage at the negative terminal of D_1 is less than the voltage at the positive terminal of D_1 else it is reverse biased.

Voltage at the positive terminal of D_1 is,

$V_{IN} - V_B = V_{IN} - 5V$

Voltage at the negative terminal of D_1 is,

$-V_{D,ON} = -0.7V$

$\therefore$ For the diode to be forward biased,

$V_{IN} - V_B < -V_{D,ON}$

$V_{IN} < V_B - V_{D,ON}$

$V_{IN} < 5 - 0.7$

$V_{IN} < 4.3V$ .....(1)

When the input voltage is greater than $4.3V$

i.e $V_{IN} > 4.3V$ (This is in the positive half cycle)

The diode D_1 will be reverse biased and hence D_1 will be OFF so the circuit becomes,

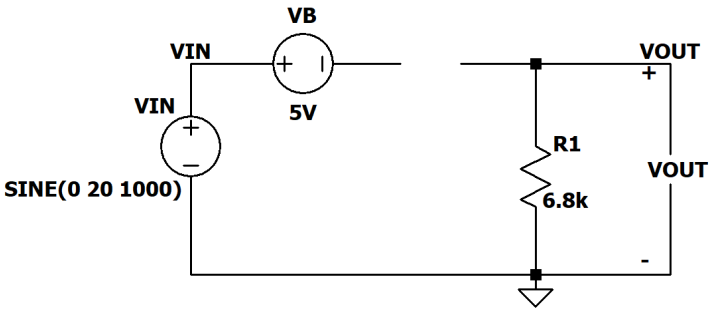


Figure 8: When diode is OFF

From the figure 8 we can observe, $V_{OUT} = 0V$

But when the input voltage is less than $4.3V$
i.e $V_{IN} < 4.3V$ .....[From (1)]

The diode D_1 is forward biased and hence it will be ON so the circuit becomes,

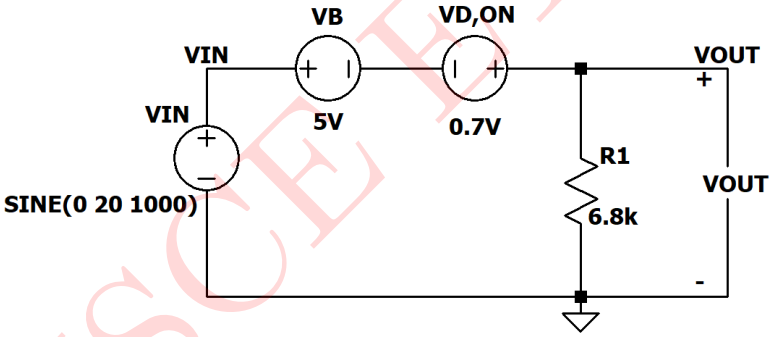


Figure 9: When diode is ON

Applying KVL,
$V_{IN} - V_B + V_{D,ON} = V_{OUT}$
$V_{OUT} = V_{IN} - 5 + 0.7$
$V_{OUT} = V_{IN}$ - 4.3
When $V_{IN} = 0$
$V_{OUT} = 0 - 4.3 = \mathbf{-4.3V}$

Maximum value of V_{IN} in the negative half cycle is,
$V_{IN} = -V_m = \mathbf{-20V}$

For peak value in negative half cycle,
$V_{OUT} = -V_m - 4.3 = \mathbf{-24.3V}$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

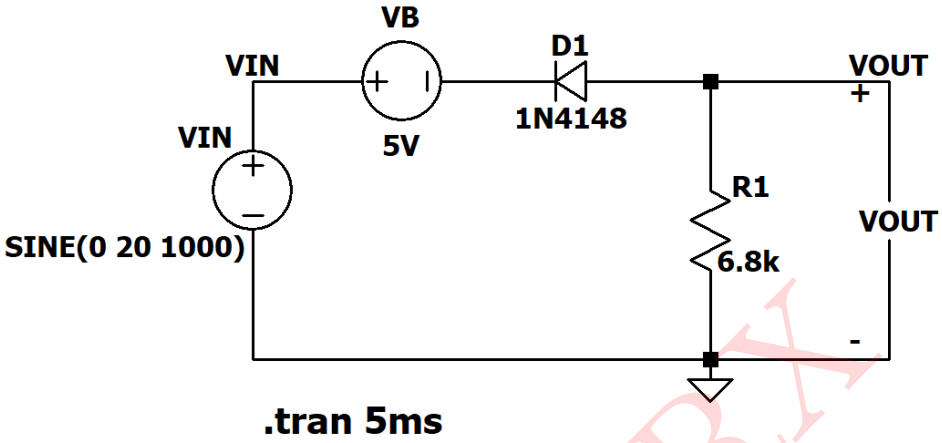


Figure 10: Circuit Schematic

The input and output waveform are shown in figure 11

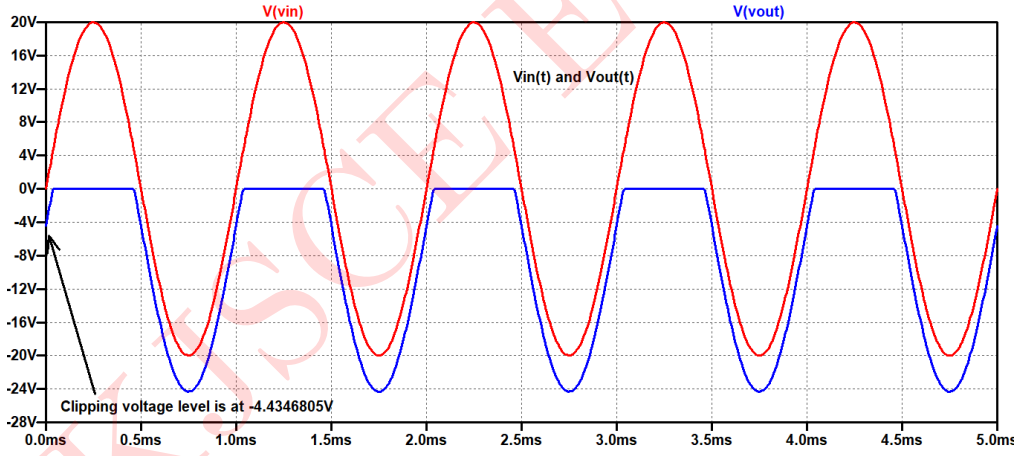


Figure 11: $V_{IN}(t)$ & $V_{OUT}(t)$

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
Clipped output voltage level	$-4.3V$	$-4.4346V$

Table 2: Numerical 2

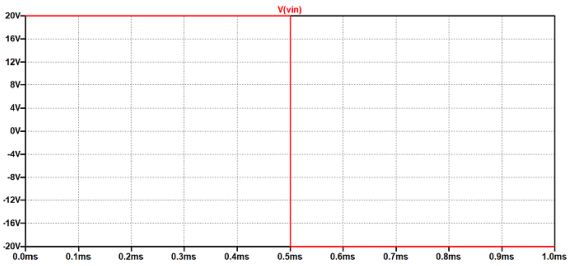
Numerical 3:

For the circuit shown in figure 12,

Plot: Input $V_{IN}(t)$ & output $V_{OUT}(t)$ waveforms

Given : $V_{IN}(t) = 40V_{p-p}$ square wave of frequency of 1000Hz, $C_1 = 10\mu$F, $R_1 = 10k\Omega$

Diode D_1 is Si diode i.e $V_{D,ON} = 0.7V$



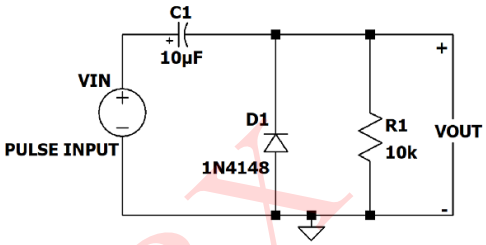


Figure 12: Circuit 3

Solution: Since the given diode is a Si, we will prefer a constant voltage model i.e $V_{D,ON} = 0.7V$

Given that $V_{IN}(t) = 40V_{p-p}$ i.e $V_m = 20V$, f = 1000Hz

Time period (t_s) of input waveform

$$t_s = \frac{1}{f} = \frac{1}{1000} = \mathbf{0.001s}$$

RC time constant $(t_{RC}) = R_1 \times C_1 = 10\mu\text{F} \times 10k\Omega = \mathbf{0.1s}$

Hence we can see that the RC time constant is much larger than the time period of input signal, i.e $t_{RC} >> t_s$

This will ensure that voltage across capacitor does not discharge significantly during the period diode is OFF

Operation:

During the negative half cycle the diode D_1 is ON when the voltage on the positive terminal of diode i.e $-V_{D,ON}$ is greater than the voltage on the negative terminal of D_1 i.e $V_{IN} = -V_m$ (For negative half cycle)

$\therefore$ For $V_{IN} < -V_{D,ON}$

Diode D_1 is ON and the circuit becomes,

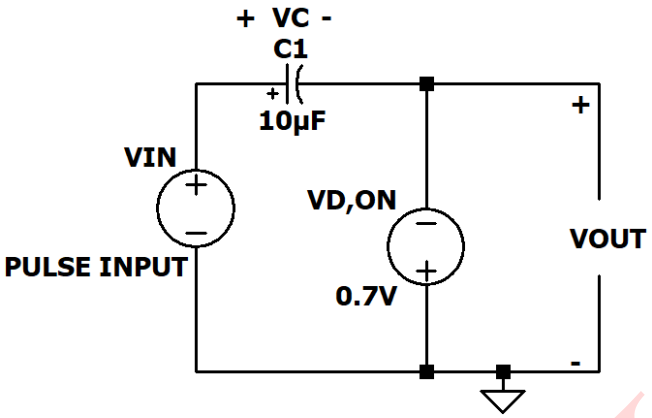


Figure 13: When diode is ON

From the figure 13 we can observe,

$V_{OUT} = -V_{D,ON} = -0.7V$ (During the negative half cycle of input)

At the same time capacitor C_1 charges and voltage across C_1 charges upto $-V_m$,

Applying KVL in figure 13,

$V_{IN} + V_C + V_{D,ON} = 0$

$V_C = -V_{IN} - V_{D,ON}$

$= -(-V_m) - V_{D,ON}$ [In negative half cycle, $V_{IN} = -V_m$]

$= -(-20) - 0.7$

$= \mathbf{19.3V}$ [Clamping level]

Now, during the positive half cycle the diode D_1 is OFF for thr entire positive half cycle as the voltage on the negative terminal is $V_{IN} = V_m$ which is greater than $0V$ whereas the voltage on the positive terminal of diode is $-V_{D,ON} = -0.7V$

$\therefore V_{IN} > -V_{D,ON}$ for the whole positive half cycle

$\therefore$ Diode D_1 is OFF i.e the circuit becomes,

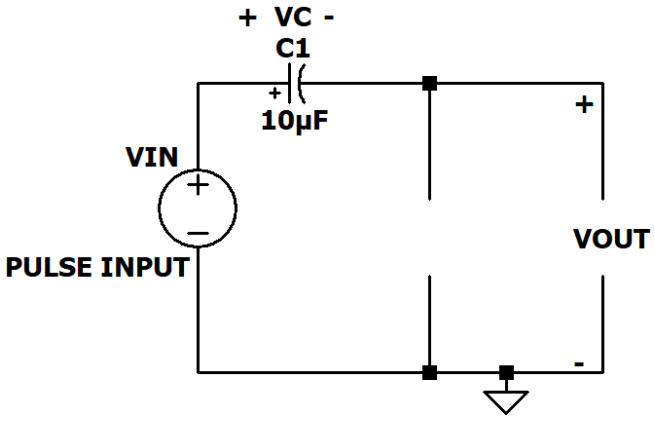


Figure 14: When diode is OFF

During the positive half cycle capacitor C_1 holds the charge $V_C = 19.3V$ as the RC time constant is much larger than time period of input signal and hence acts as a battery

Applying KVL to figure 14,

$V_{IN} + V_C - V_{OUT} = 0$

$V_{OUT} = V_{IN} + V_C$

$= V_m + V_C$ [For positive half cycle, $V_{IN} = V_m$]

$= 20 + 19.3 = \mathbf{39.3V}$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

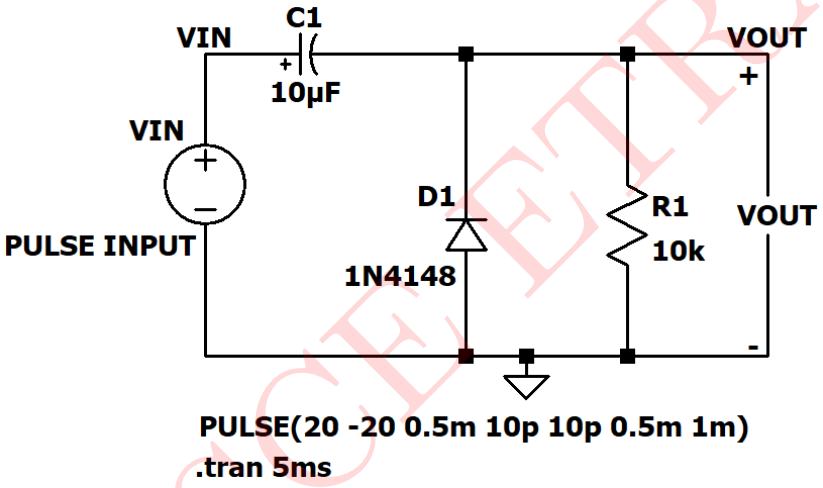


Figure 15: Circuit Schematic

The input and output waveform are shown in figure 16

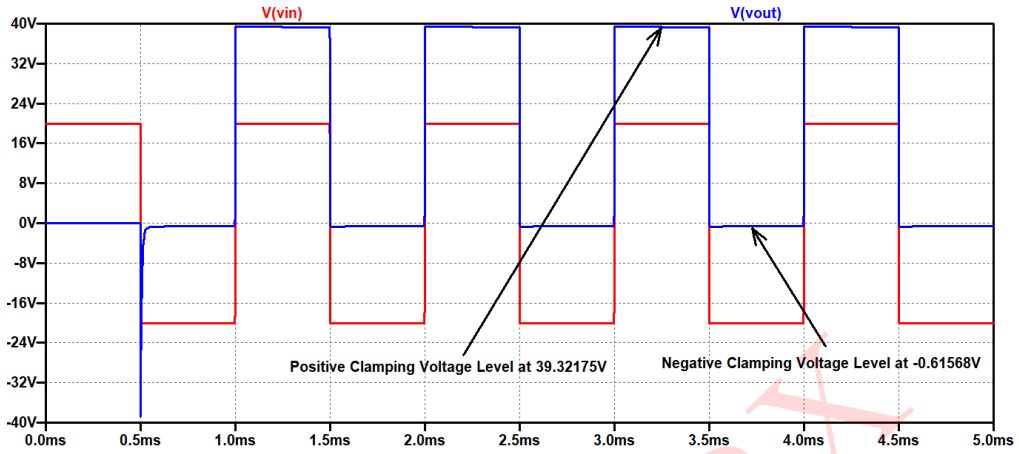


Figure 16: $V_{IN}(t)$ & $V_{OUT}(t)$

Since the output waveform is shifted above of X-axis the given circuit is a positive clamper

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
Positive Clamping level of output waveform	$39.3V$	$39.32175V$
Negative Clamping level of output waveform	$-0.7V$	$-0.61568V$

Table 3: Numerical 3

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