

K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Single Stage FET Amplifier

Numerical 1

For the JFET circuit shown in figure 1, find a) g_m b) A_V c) R_i d) R_o

Given: $V_P = -3V$, $I_{DSS} = 8mA$ & $r_d = 50k\Omega$

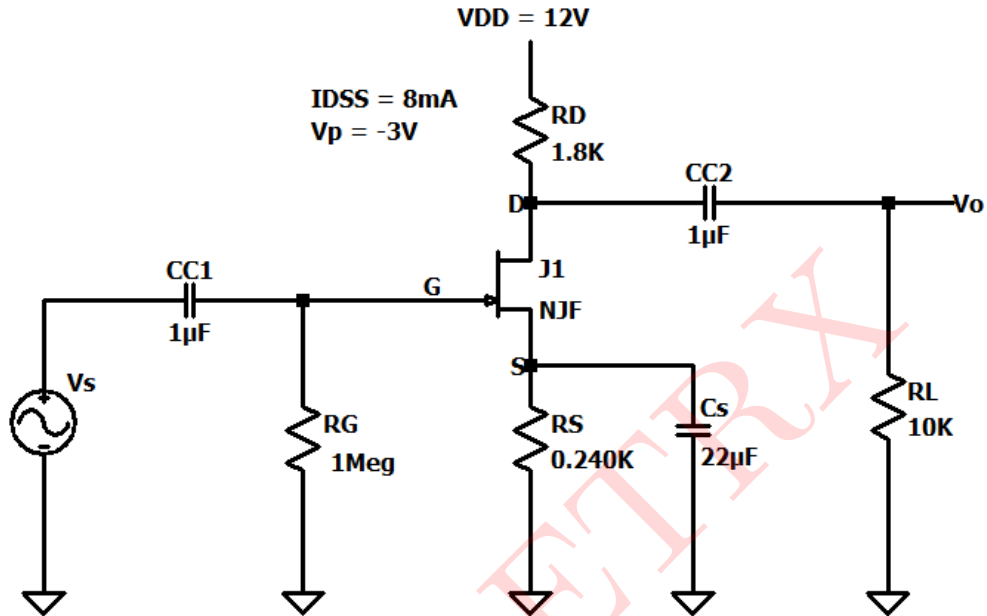


Figure 1: Circuit 1 for Numerical 1

Solution:

The given circuit is a N-Channel JFET Common-Source amplifier.

DC Analysis:

In DC analysis, the capacitors become open circuit.

From the given circuit we get,

$$V_G = 0$$

$$V_S = I_D R_S$$

$$V_{GS} = V_G - V_S = -I_D R_S$$

$$V_{GS} = -I_D (240) \quad \text{.....(1)}$$

Assuming that the JFET is working in the saturation region

$$\text{The equation for } I_D \text{ is } I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8mA \left(1 + \frac{V_{GS}}{3}\right)^2 \quad \text{.....(2)}$$

Substituting (2) in (1) we get,

$$V_{GS} = -1.92 \left(1 + \frac{V_{GS}^2}{9} + \frac{2V_{GS}}{3} \right)$$

$$0.213V_{GS}^2 + 2.28V_{GS} + 1.92 = 0$$

Solving the above quadratic equation we get,

$$V_{GS} = -0.921V \text{ or } V_{GS} = -9.782V$$

$$V_{GS} = -0.9215V \quad (\because V_{GS} > V_P)$$

$$I_D = 8 \times 10^{-3} \left(1 - \frac{(-0.921)}{(-3)} \right)^2$$

$$I_D = 3.842mA$$

AC Analysis:

The small signal parameters calculations are shown below

Given $r_d = 50k\Omega$

$$g_m = \frac{2I_{DSS}}{|V_P|} \left(1 - \frac{V_{GS}}{V_P} \right) = \frac{2 \times 8mA}{3} \left(1 - \frac{(-0.921)}{(-3)} \right)$$

$$g_m = 3.694mA/V$$

The small signal equivalent circuit is shown in figure 2

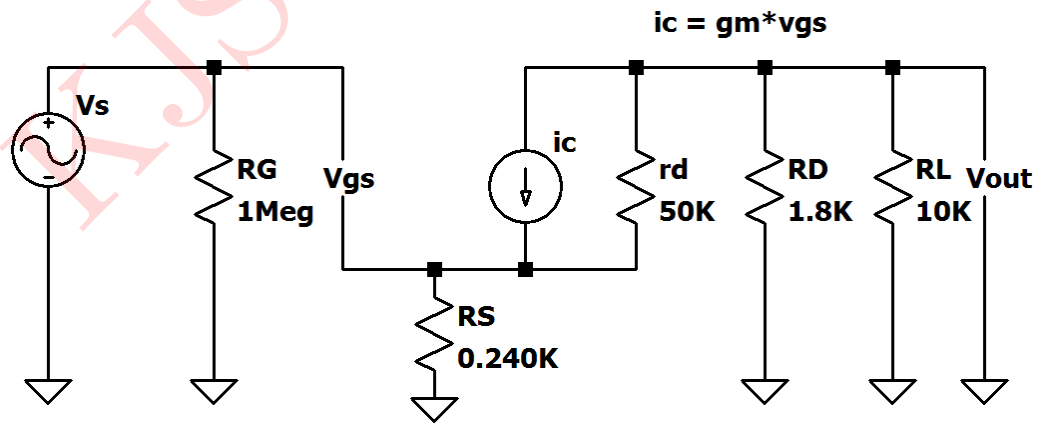


Figure 2: Small Signal Equivalent Circuit

Calculation of voltage gain (A_V)

$$A_V = -g_m(r_d \parallel R_D \parallel R_L) = -3.694 \times 10^{-3}(50k \parallel 1.8k \parallel 10k)$$

$$\mathbf{A_V = -5.46}$$

Calculation of R_i & R_o

From figure 2 we get,

$$R_i = R_G$$

$$\mathbf{R_i = 1M\Omega}$$

$$R_o = r_d \parallel R_D \parallel R_L = 50k \parallel 1.8k \parallel 10k$$

$$\mathbf{R_o = 1.48k\Omega}$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

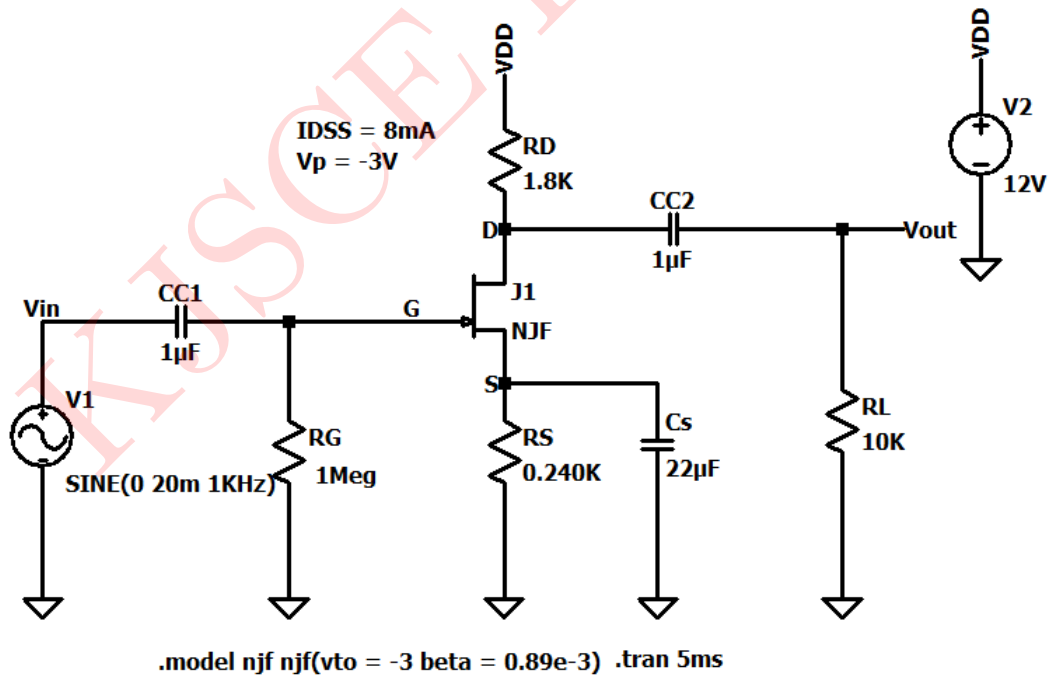


Figure 3: Circuit Schematic: Results

The input and output waveforms are shown in figure 4

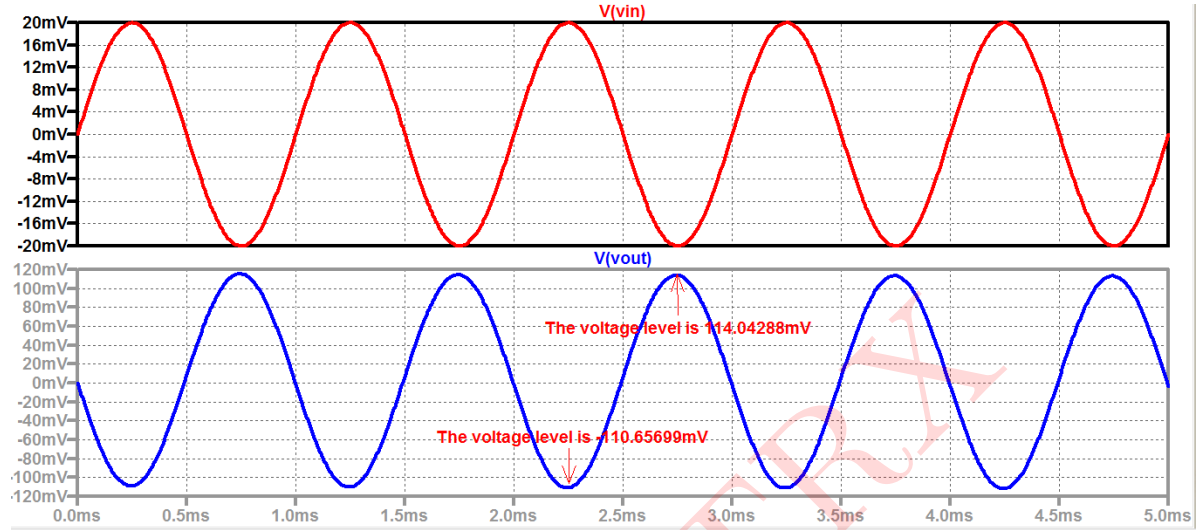


Figure 4: Input and Output Waveforms

Comparison between theoretical and simulated values is given below:

Parameters	Simulated Values	Theoretical Values
I_D	$3.842mA$	$3.84mA$
A_V	-5.57	-5.46
V_{GS}	$-0.922V$	$-0.9215V$

Table 1: Numerical 1

Numerical 2

For the MOSFET amplifier circuit shown in figure 5, find Z_i , Z_o and A_V if $V_i = 4mV$, $V_{GS_{th}} = 4V$, $I_{D_{ON}} = 4mA$, $V_{GS_{ON}} = 7V$ and $y_{os} = 20\mu s$

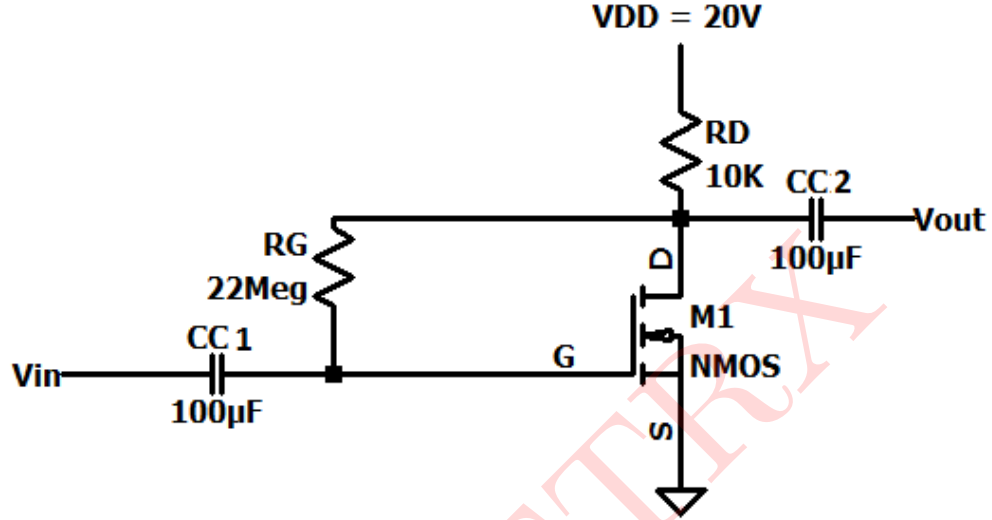


Figure 5: Circuit for Numerical 2

Solution: The given circuit is employing drain feedback biasing circuit.

DC Analysis:

In DC analysis, the capacitors become open circuit.

Since $I_G = 0$ we get,

$$V_{GS} = V_{DS}$$

$$\text{We know that } k_n = \frac{I_D}{[V_{GS} - V_{GS_{th}}]^2} = \frac{4 \times 10^{-3}}{[7 - 4]^2}$$

$$k_n = 0.44mA/V^2$$

Applying KVL to Drain-Source loop we get,

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{GS} = V_{DD} - I_D R_D \quad (\because V_{GS} = V_{DS})$$

$$V_{GS} = 20 - I_D(10k) \quad \text{.....(1)}$$

$$I_D = k_n(V_{GS} - V_{TN})^2$$

$$I_D = 0.44 \times 10^{-3}(V_{GS} - 4)^2 \quad \text{.....(2)}$$

Substituting (2) in (1) we get,

$$V_{GS} = 20 - 4.4(V_{GS} - 4)^2 = 20 - 4.4(V_{GS}^2 - 8V_{GS} + 16)$$

$$V_{GS} = 20 - 4.4V_{GS}^2 + 35.2V_{GS} - 50.4$$

$$4.4V_{GS}^2 - 34.2V_{GS} + 50.4 = 0$$

Solving the above quadratic equation we get,

$$V_{GS} = 5.7966V \text{ or } V_{GS} = 1.976V$$

$$\mathbf{V_{GS} = 5.7966V} \quad (\because V_{GS} > V_{TN})$$

$$I_D = 0.44mA(5.7966 - 4)^2$$

$$\mathbf{I_D = 1.43mA}$$

AC Analysis:

Calculation of small signal parameters is shown below

$$g_m = 2k_n[V_{GSQ} - V_{TN}] = 2 \times 0.44 \times 10^{-3}[5.7966 - 4]$$

$$\mathbf{g_m = 1.58mA/V}$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{20\mu s} = \frac{1}{I_{DQ} \times \lambda}$$

$$\frac{1}{20\mu s} = \frac{1}{I_{DQ} \times \lambda}$$

$$\lambda = \mathbf{14.08mV^{-1}}$$

The small signal equivalent circuit is shown in figure 6

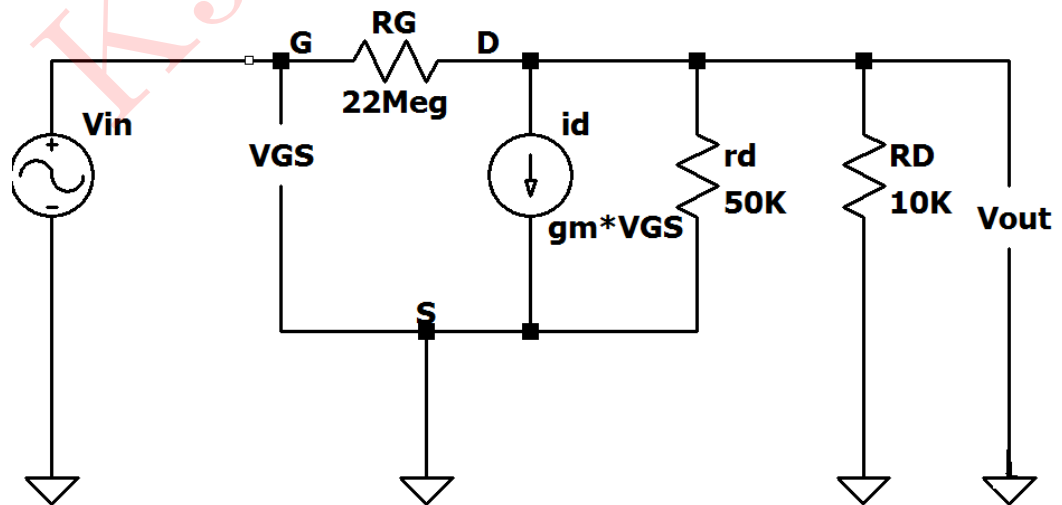


Figure 6: Small Signal Equivalent Circuit

Calculation of voltage gain (A_V):

Applying KCL at Drain(D) we get,

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \parallel R_D}$$

$$I_i = \frac{V_i - V_o}{R_G} \quad (V_i = V_{gs})$$

$$\text{i.e. } \frac{V_i - v_o}{R_G} = g_m V_i + \frac{V_o}{r_d \parallel R_D}$$

$$V_i \left[\frac{1}{R_G} - g_m \right] = V_o \left[\frac{1}{R_G} + \frac{1}{r_d \parallel R_D} \right]$$

Since $\frac{1}{R_G} \ll 1$ we get,

$$\left[\frac{1}{R_G} - g_m \right] = -g_m$$

$$A_V = \frac{V_o}{V_i} = \frac{-g_m}{\frac{1}{R_G \parallel r_d \parallel R_D}} = -g_m (R_G \parallel r_d \parallel R_D)$$

$$A_V = -1.58 \times 10^{-3} (22M \parallel 50k \parallel 10k)$$

$$\mathbf{A_V = -13.155}$$

Calculation of Z_i & Z_o :

From figure 6 we get,

$$Z_i = R_G$$

$$\mathbf{Z_i = 22M\Omega}$$

$$Z_o = R_G \parallel r_d \parallel R_D = 22M \parallel 50k \parallel 10k$$

$$\mathbf{Z_o = 8.326k\Omega}$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

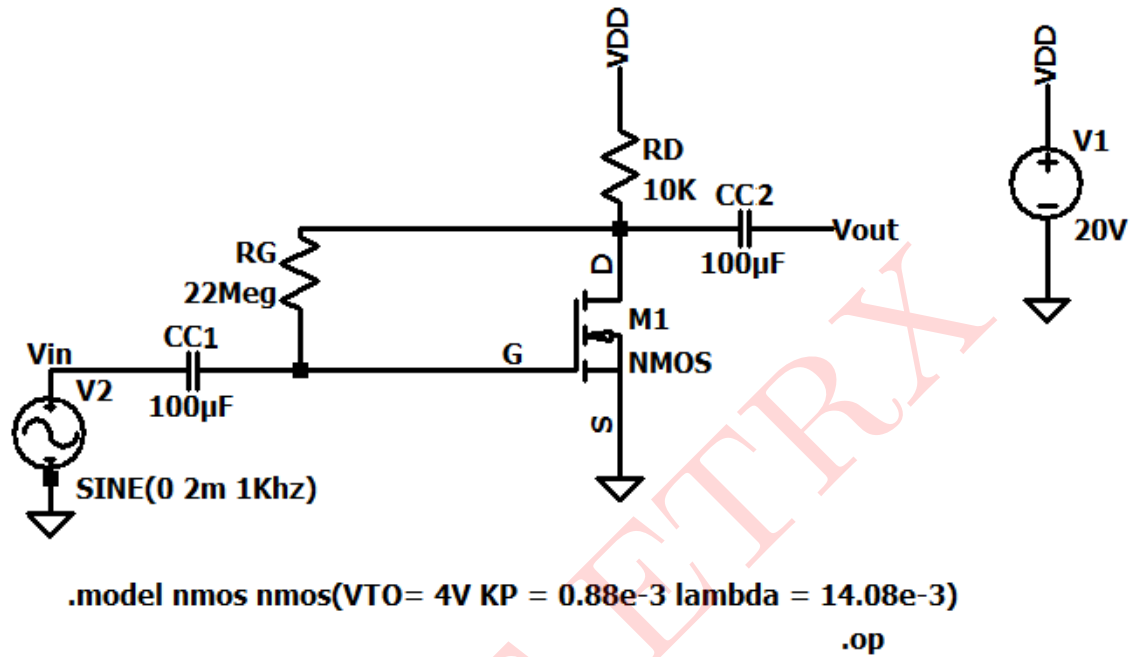


Figure 7: Circuit Schematic: Results

The input and output waveforms are shown in figure 8

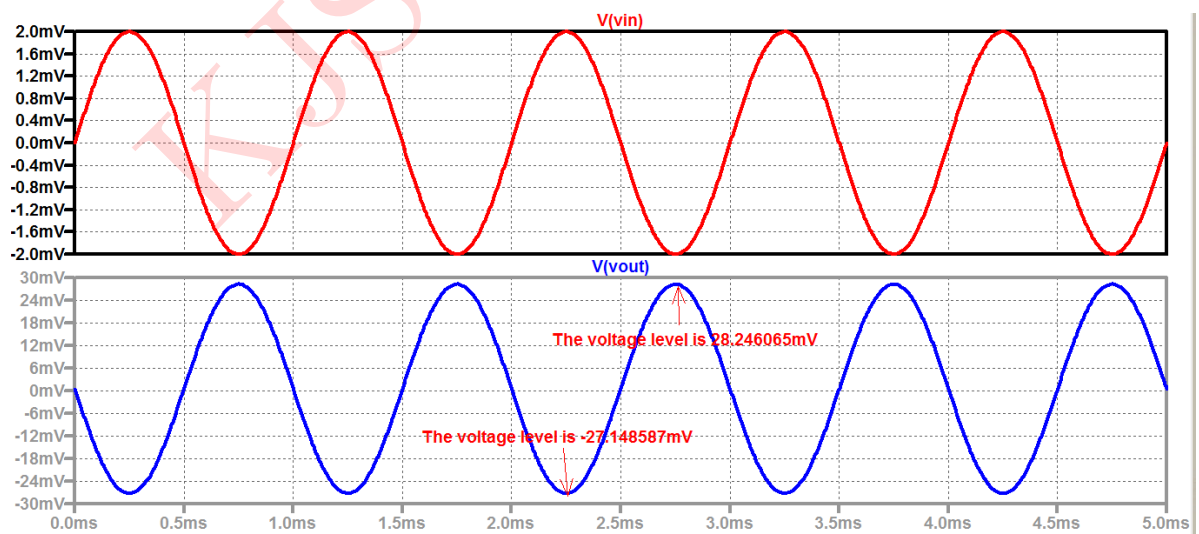


Figure 8: Input and Output Waveforms

Comparison between theoretical and simulated values is given below:

Parameters	Simulated Values	Theoretical Values
I_{DQ}	$1.42mA$	$1.43mA$
A_V	-13.2	-13.155
V_{GSQ}	$5.732V$	$5.7966V$

Table 2: Numerical 2

KJSCE ETRX