K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Multi-transistor circuits

12^{st} **July, 2020** **Numericals**

Numerical 1: Calculate voltage gain of each stage and overall AC Voltage gain for the BJT Cascade amplifier circuit shown in figure 1. Here, $V_A = 100V$ and load resistance $R_L = 12k\Omega$

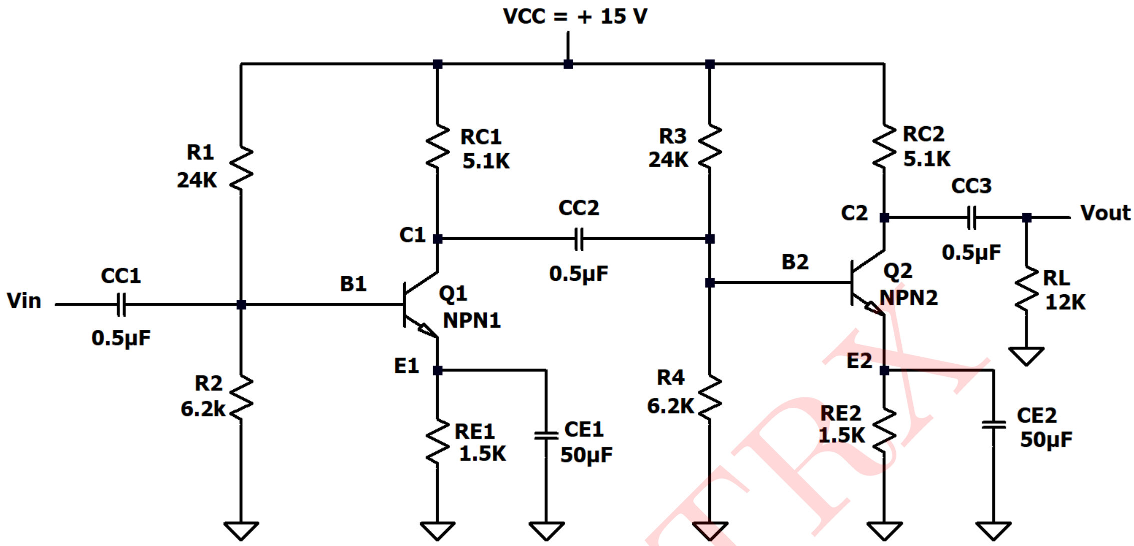

Figure 1: Circuit 1

Solution:

DC ANALYSIS:

$f = 0$, thus $X_C = \infty$, So we replace each capacitor with short circuit,
Also due to RC coupling both the stages Q points are isolated.
Since, both stages are symmetric in parameters and resistors values, DC analysis of one stage is enough.

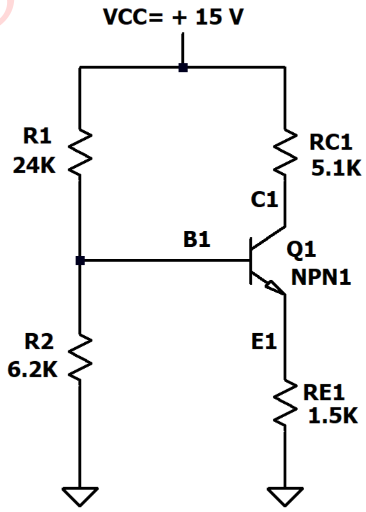

Figure 2: DC Equivalent Circuit

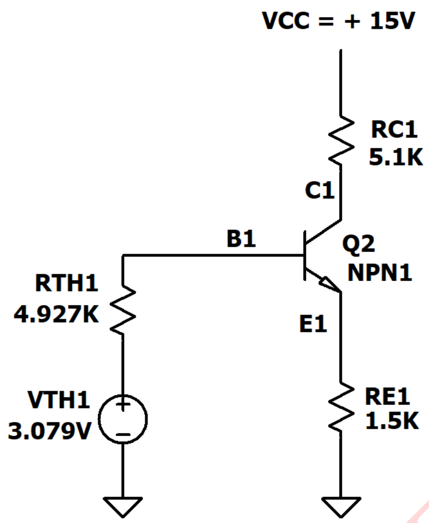

Figure 3: Thevenin equivalent circuit

Here, $R_{TH1} = R_1 \ || \ R_2 = 24k \ || \ 6.2k = \mathbf{4.927k\Omega}$

and $V_{TH1} = \dfrac{V_{CC} \times R_2}{R_1 + R_2} = \dfrac{15 \times 6.2 \times 10^3}{24k + 6.2k} = \mathbf{3.079V}$

Applying KVL to Base- Emitter loop;

$V_{TH1} - I_{B1}R_{TH1} - V_{BE1} - I_{E1}R_{E1} = 0$

But, $I_{E1} = (\beta_1 + 1)I_{B1}$

$\therefore V_{TH1} - I_{B1}R_{TH1} - V_{BE1} - I_{B1}(1 + \beta_1)R_{E1} = 0$

$\therefore V_{TH1} - V_{BE1} = I_{B1}(R_{TH1} + (1 + \beta_1)R_{E1})$

$$\therefore I_{B1} = \frac{V_{TH1} - V_{BE1}}{R_{TH1} + (1 + \beta_1)R_{E1}} = \frac{3.079 - 0.7}{4.927k + (151)1.5 \times 10^3} = \frac{2.379 \times 10^{-3}}{231.427 = 10.27 \times 10^{-6}}$$

$= \mathbf{10.27\mu A}$

But $I_{C1} = \beta I_{B1} = 150 \times 10.27 \times 10^{-6} = \mathbf{1.54mA}$

Applying KVL to Common - Emitter loop;

$V_{CC} - I_{C1}R_{C1} - V_{CE1} - I_{E1}R_{E1} = 0$

$I_{E1} = (\beta_1 + 1)I_{B1}$

$V_{CE1} = V_{CC} - I_{C1}R_{C1} - (1 + \beta_1)R_{B1}R_{E1}$

$= 15 - (1.54 \times 10^{-3})(5.1)(10^3) - 151(10.27 \times 10^{-6})(1.5 \times 10^3) = 15 - 7.854 - 2.326$

$= \mathbf{4.8198V}$

Since both the stages are identical,

$I_{CQ1} = I_{CQ2} = \mathbf{1.54mA}$

$V_{CE1Q} = V_{CE2Q} = \mathbf{4.8198V}$

Small signal parameters:

$$r_\pi = \frac{\beta_1 V_T}{I_{C1Q}} = \frac{150 \times 26 \times 10^{-3}}{1.54 \times 10^{-3}} = \mathbf{2.532k\Omega}$$

$$g_{m1} = \frac{I_{C1Q}}{V_T} = \frac{1.54 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{59.23mA/V}$$

Since, both stages are identical we have,

$r_{\pi 1} = r_{\pi 2} = \mathbf{2.532k\Omega}$

$g_{m1} = g_{m2} = \mathbf{59.23mA/V}$

$$r_{d1} = \frac{V_A}{I_{CQ1}} = \frac{100}{1.54 \times 10^{-3}} = \mathbf{64.935k\Omega}$$

$r_{d1} = r_{d2} = \mathbf{64.935k\Omega}$

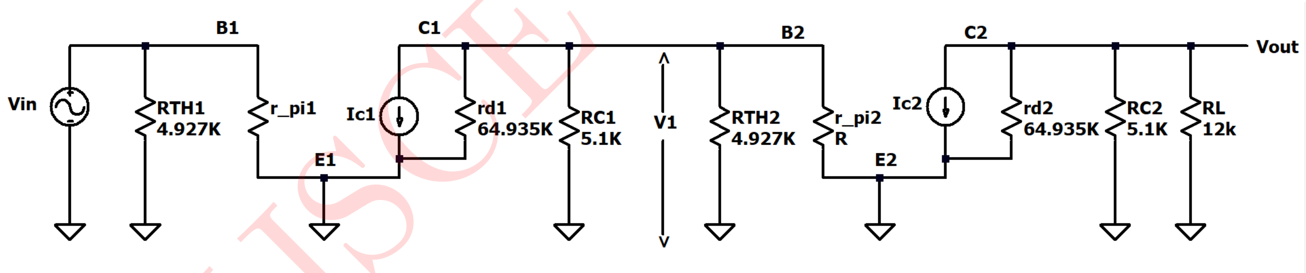

Figure 4: AC (mid band) equivalent circuit

$$A_{V1} = \frac{V_1}{V_{in}} \text{ and } A_{V2} = \frac{V_{out}}{V_1}$$

$A_{VT} = A_{V1} A_{V2}$

Input impedance of first stage:

$Z_i = R_{TH1} \;||\; r_{\pi 1} = 4.927k\Omega \;||\; 2.532k\Omega = \mathbf{1.672k\Omega}$

Output impedance of second stage:

$Z_o = R_2 \;||\; r_{d2} \;||\; R_{C2} = 64.935k \;||\; 12k \;||\; 5.1k = 3578.947 \;||\; 64.93k = \mathbf{3.392k\Omega}$

Finding A_{V1}:

$$A_{V1} = \frac{V_1}{V_{in}} = \frac{-g_m V_{\pi 1}(R_{C1} \mid\mid R_{TH1} \mid\mid r_{d1} \mid\mid r_{\pi 2})}{V_{\pi 1}} = -g_m V_{\pi 1}(R_{C1} \mid\mid R_{TH1} \mid\mid r_{d1} \mid\mid r_{\pi 2})$$

$$= -(59.23 \times 10^{-3})(95.1k \mid\mid 4.927k \mid\mid 64.935k \mid\mid 2.532k)$$
$$= -(59.23 \times 10^{-3})(2506.003 \mid\mid 2436.97)$$

$$= -(59.23 \times 10^{-3})(1235.5) = \mathbf{73.178}$$

A_{V1} in dB $= 20log_{10}(73.178) = \mathbf{37.287dB}$

Finding A_{V2}:

$$A_{V2} = \frac{V_{out}}{V_1} = \frac{-g_m V_{\pi 2}(R_{C2} \mid\mid r_{d2} \mid\mid R_L)}{V_{\pi 2}} = -g_m(R_{C2} \mid\mid r_{d2} \mid\mid R_L)$$

$$= -(59.23 \times 10^{-3})(12k \mid\mid 5.1k \mid\mid 64.935k) = -(59.23 \times 10^{-3})(3578.9 \mid\mid 64.935k)$$

$$= -(59.23 \times 10^{-3})(3391.99) = -\mathbf{200.907}$$

A_{V2} in dB $= 20log_{10}(200.907) = \mathbf{46.059dB}$

Finding A_{VT}:

$A_{VT} = A_{V1}A_{V2} = (-73.178) \times (-200.9.7) = \mathbf{14701.97}$

A_{VT} in dB $= 20log_{10}(14701.97) = \mathbf{83.346dB}$

SIMULATED RESULTS:
Above circuit is simulated in LTspice and the result is as follows:

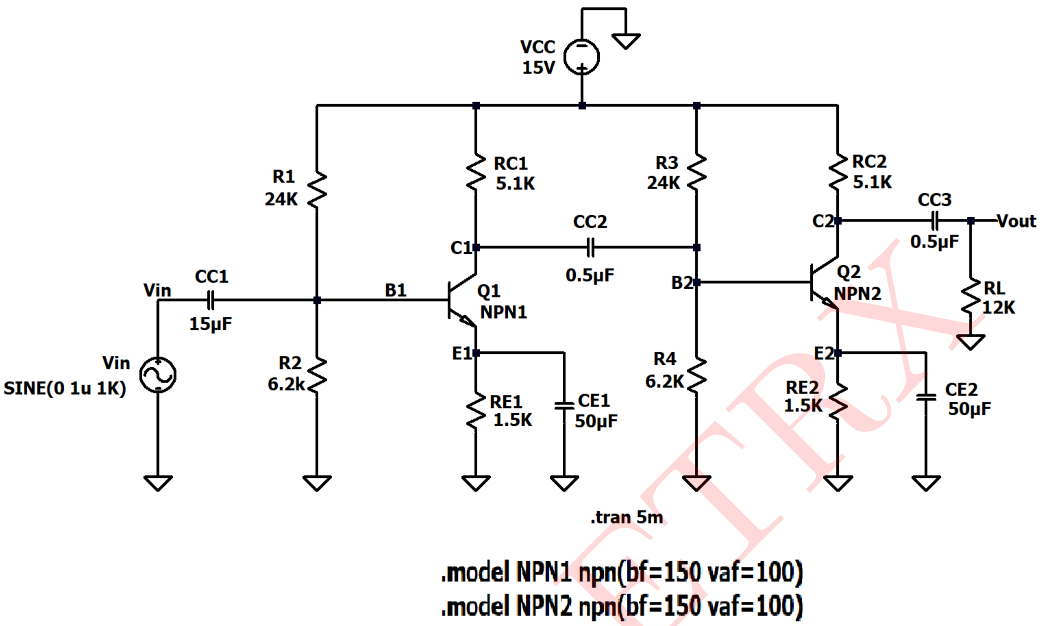

Figure 5: Circuit Schematic

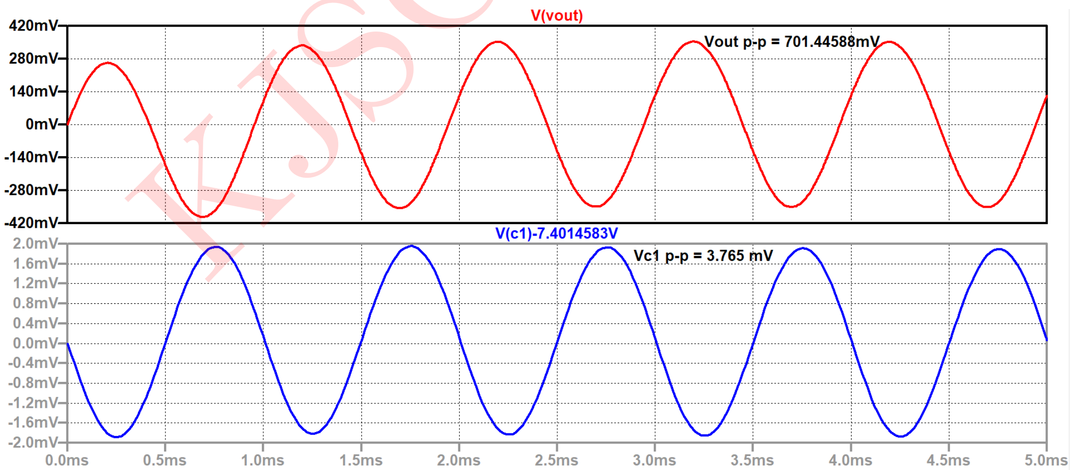

Figure 6: Input output waveform of stage 1

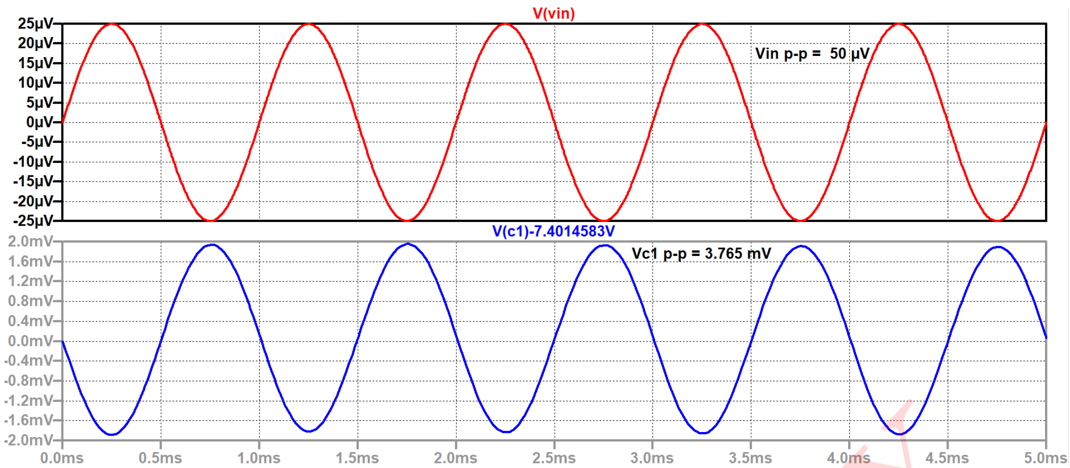

Figure 7: Input output waveform of stage 2

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
I_{C1Q}	1.54mA	1.487mA
V_{CE1Q}	4.8198V	5.167V
I_{C2Q}	1.54mA	1.487mA
V_{CE2Q}	4.8198V	5.167V
Voltage gain of 2^{nd} stage (A_{V1})	37.287dB	37.53dB
Voltage gain of 2^{nd} stage (A_{V2})	46.049dB	45.4B
Overall Voltage gain	83.346dB	82.9dB
1^{st} stage input impedance (Z_i)	$1.672k\Omega$	–
2^{nd} stage input impedance (Z_i)	$3.392k\Omega$	–

Table 1: Numerical 1

Numerical 2: For the figure 8, calculate input impedance, output impedance, voltage gain and resulting output voltage.

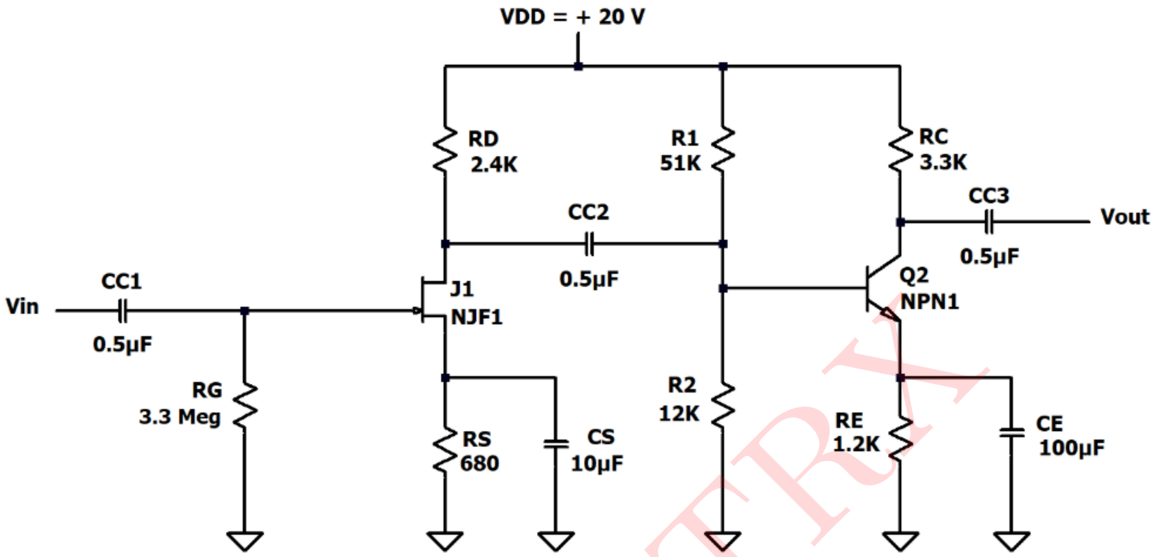

Figure 8: Circuit 2

Solution:

DC ANALYSIS:
$f = 0$, thus $X_C = \infty$, So we replace each capacitor with short circuit,
Also due to RC coupling both the stages Q points are isolated.

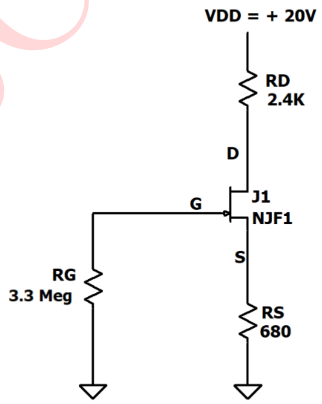

Figure 9: DC Equivalent Circuit for stage 1

DC analysis for 1^{st} stage:

Applying KVL to gate - source loop;

$\therefore -I_G R_G - V_{GS} - I_S R_S = 0$

For mosfet, $I_G = 0$ and $I_S = I_D$

$\therefore V_{GS} = -I_D R_S = -680 I_D$ 1

Also, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10 \times 10^{-3}\left(1 + \frac{V_{GS}}{4}\right)^2$ 2

From 1 and 2, we get;

$$\therefore \frac{-V_{GS}}{680} = 10 \times 10^{-3}\left(1 + \frac{V_{GS}}{4}\right)^2$$

$$\therefore -V_{GS} = 6.8\left(1 + \frac{V_{GS}}{2} + \frac{V_{GS}^2}{16}\right)$$

$$\therefore 6.8 + 3.4V_{GS} + 0.425V_{GS}^2 + V_{GS} = 0$$

$$\therefore 0.425V_{GS}^2 + 4.4V_{GS} + 6.8 = 0$$

$V_{GS} = -1.89V$ or $-8.462V$

But $V_{GS} > V_P$

$\therefore V_{GSQ} = \mathbf{-1.89V}$

Substituting value of V_{GS} in 1;

$$I_D = \frac{V_{GS}}{-680} = \frac{1.89}{680} = \mathbf{2.8mA}$$

DC analysis for 2^{nd} stage:

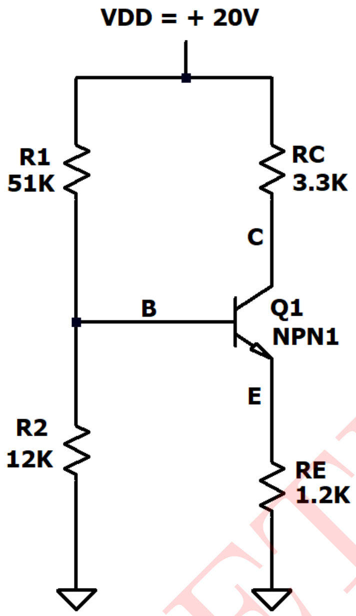

Figure 10: DC Equivalent Circuit for stage 2

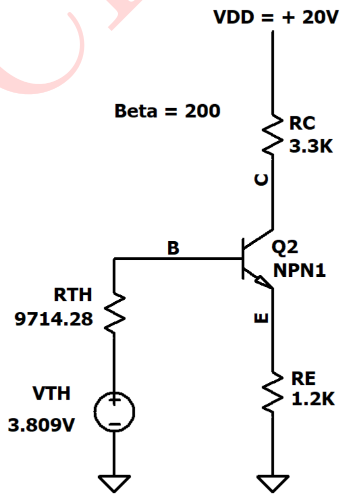

Figure 11: Thevenin equivalent circuit

Where, $V_{TH} = \dfrac{V_{DD} \times R_2}{R_1 + R_2} = \dfrac{20 \times 12k}{51k + 12k} = \mathbf{3.809V}$

Also, $R_{TH} = R_1 \;||\; R_2 = 51k \;||\; 12k = \mathbf{9714.28\Omega}$

Applying KVL to base - emitter loop;

$V_{TH} - I_B R_{TH} - I_E R_E - V_{BE} = 0$

But $I_E = (\beta + 1) I_B$

$\therefore 3.809 - 0.7 = I_B(R_{TH} + (\beta + 1)R_E)$

$I_B = \dfrac{3.809 - 0.7}{9714.28 + (201)(1.2 \times 10^3)} = \mathbf{12.39\mu A}$

$I_C = \beta I_B = 200 \times 12.39 \times 10^{-6} = \mathbf{2.478mA}$

Applying KVL to common - emitter loop;

$V_{DD} - I_C R_C - V_{CE} - I_E R_E = 0$

But, $I_E = (1 + \beta) I_B$

$\therefore V_{CE} = V_{DD} - I_C R_C - (1 + \beta) I_B R_E$

$= 20 - (2.478 \times 10^{-3})(3.3 \times 10^3) - (201)(12.39 \times 10^{-6})(1200) = 20 - 8.1774 - 2.988$

$= \mathbf{8.834V}$

Small Signal Parameters:

$g_{m1} = \dfrac{2I_{DSS}}{|V_P|}\left(1 - \dfrac{V_{GS}}{V_P}\right)$ (where g_{m1} is the trans conductance od first stage)

$g_{m1} = \dfrac{2 \times 10^{-3} \times 10}{4}\left(1 + \dfrac{(-1.89)}{4}\right) = \dfrac{10^{-3}}{2}(0.5275) \times 10 = 0.26 \times 10^{-2} = \mathbf{2.6mA/V}$

$r_{\pi 2} = \dfrac{\beta V_T}{I_{CQ}} = \dfrac{200 \times 26 \times 10^{-3}}{2.478 \times 10^{-3}} = \mathbf{2098.46\Omega}$

$g_{m2} = \dfrac{I_{CQ}}{V_T} = \dfrac{2.478 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{95.3mA/V}$

(where g_{m2} is the trans conductances of second stage)

Mid Band AC Equivalent circuit:

All the capacitors are short circuited and DC sources are open circuited.

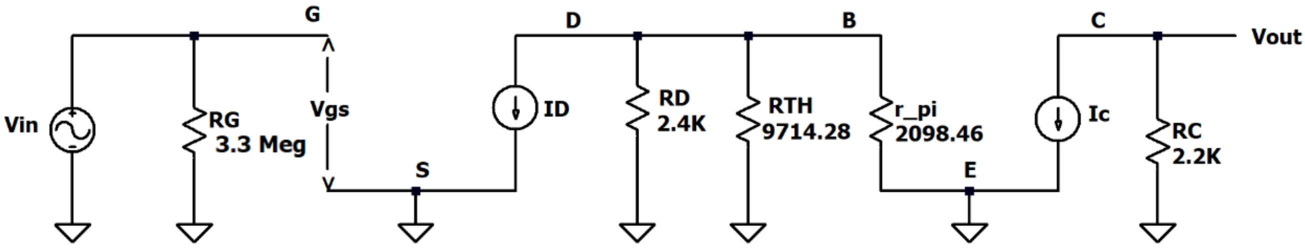

Figure 12: mid band AC equivalent circuit

Input impedance:

$Z_i = R_G = \mathbf{3.3M\Omega}$

Output Impedance:

$Z_o = R_C = \mathbf{2.2k\Omega}$

Finding out A_{V1}:

$$A_{V1} = \frac{V_1}{V_{in}} = \frac{-g_{m1}V_\pi(R_D \ || \ R_{TH} \ || \ r_{\pi2})}{V_\pi} = -g_{m1}(R_D \ || \ R_{TH} \ || \ r_{\pi2})$$

$$= -2.6 \times 10^{-3}(2.4k \ || \ 9714.28 \ || \ 2098.46) = -(2.6 \times 10^{-3})(2.4k \ || \ 1725.68) = \mathbf{-2.61}$$

A_{V1} in dB $= 20log_{10}(2.61) = \mathbf{8.332dB}$

Finding A_{V2}:

$$A_{V2} = \frac{V_{out}}{V_1} = \frac{-g_{m2}V_{\pi2}R_C}{V_{\pi2}} = -g_{m2}R_C = -95.3 \times 10^{-3}(3.3 \times 10^3) = (-314.49)$$

A_{V2} in dB $= 20log_{10}(314.49) = \mathbf{49.95dB}$

Overall AC voltage gain:

$A_{VT} = A_{V1} \times A_{V2} = (-2.61)(-314.49) = \mathbf{820.8189}$

A_{VT} in dB $= 20log_{10}(820.8189) = \mathbf{58.2849dB}$

Also, $A_{VT} = \dfrac{V_{out}}{V_{in}}$

$V_{out} = A_{VT} \times V_{in} = 10^{-3} \times 820.8189 = \mathbf{0.82mV}$

SIMULATED RESULTS:
Above circuit is simulated in LTspice and the result is as follows:

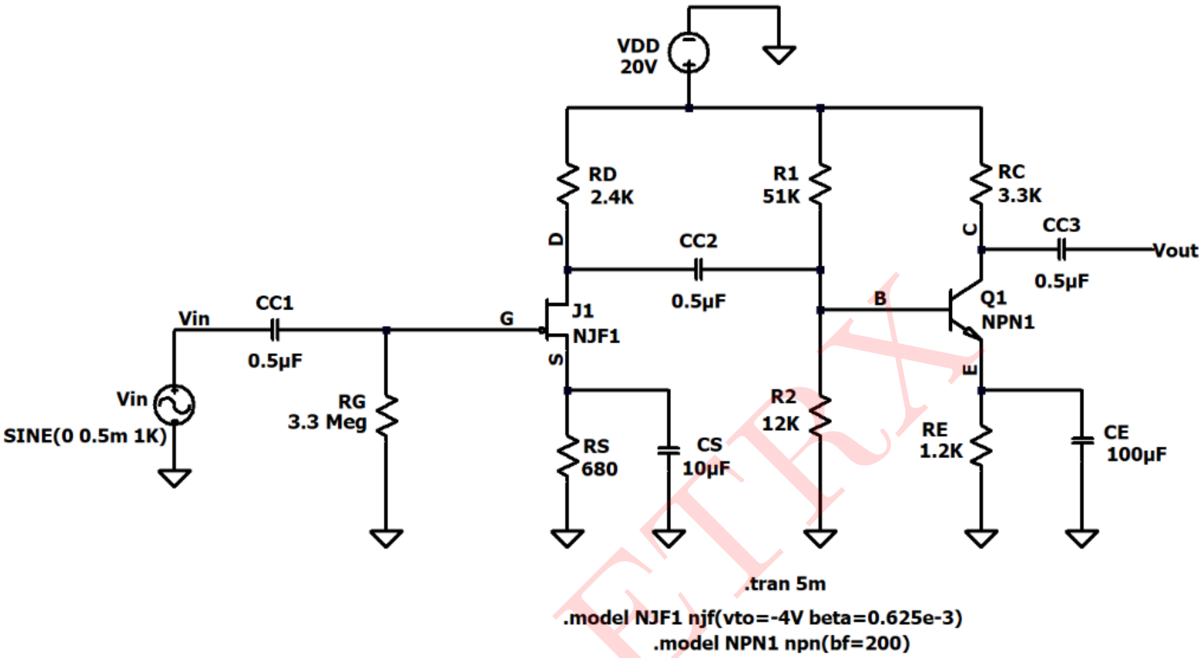

Figure 13: Circuit Schematic

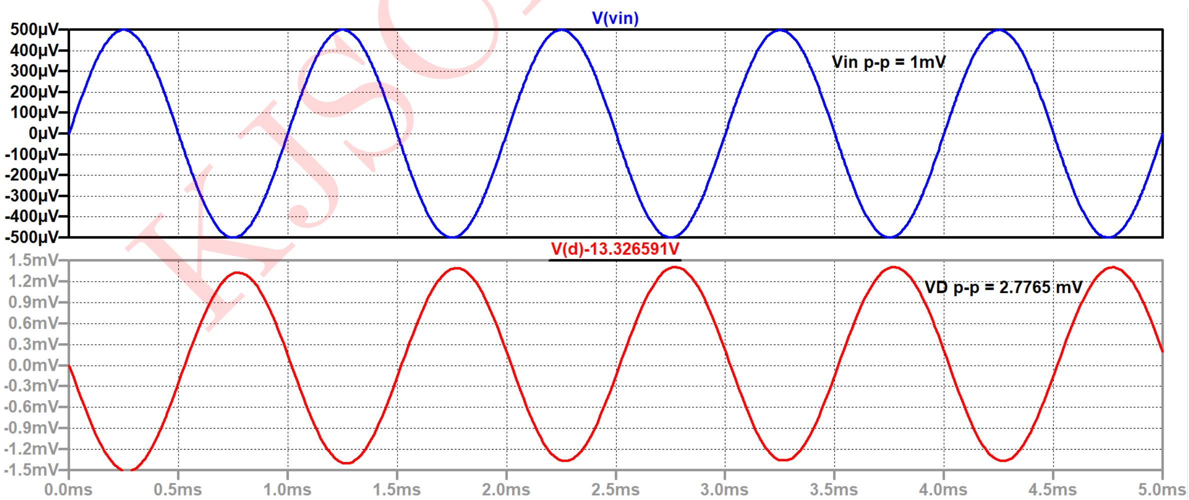

Figure 14: Input output waveform of stage 1

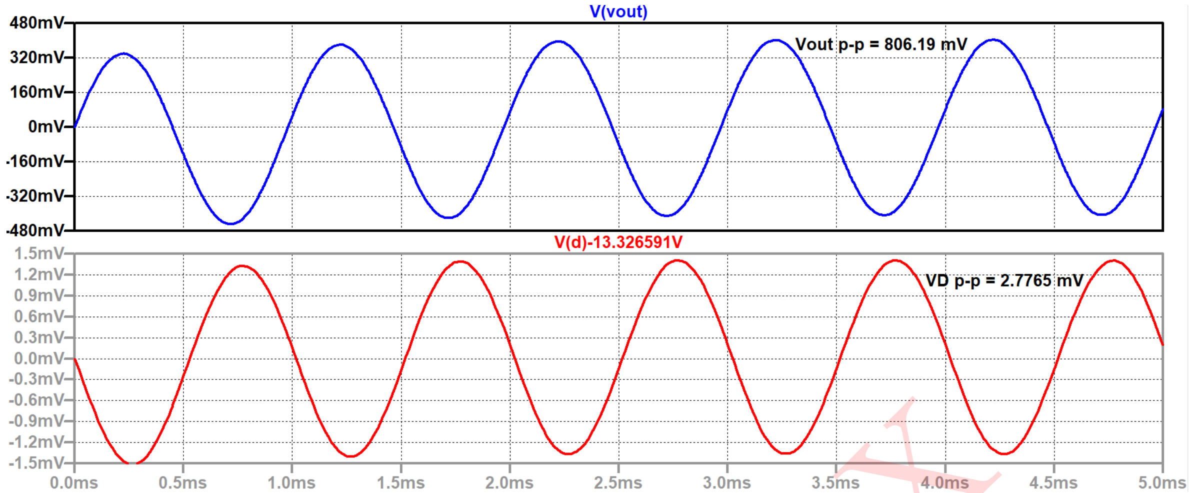

Figure 15: Input output waveform of stage 2

Comparison between Theoretical and Simulated values :-

Parameters	Simulated	Theoretical
I_{DQ}	2.8mA	2.8mA
V_{GSQ}	$-1.89V$	$-1.89V$
I_{CQ}	2.4mA	2.478mA
V_{CEQ}	9.17V	8.834V
Voltage gain of 1^{st} stage (A_{V1})	-2.27	-2.61
Voltage gain of 2^{nd} stage (A_{V2})	-291	-314.49
Overall Voltage gain	58.127dB	58.2849dB
Output Voltage	0.806V	0.82V
input impedance	–	$3.3M\Omega$
output impedance	–	$2.2k\Omega$

Table 2: Numerical 2

Numerical 3: A two stage circuit is shown in figure 16. Its BJT parameters are $\beta_1 = \beta_2 = 20$ and $V_{BE1} = V_{BE2} = 0.6$

a. Determine all node voltages and terminal currents under DC analysis.

b. Determine overall voltage gain of the circuit.

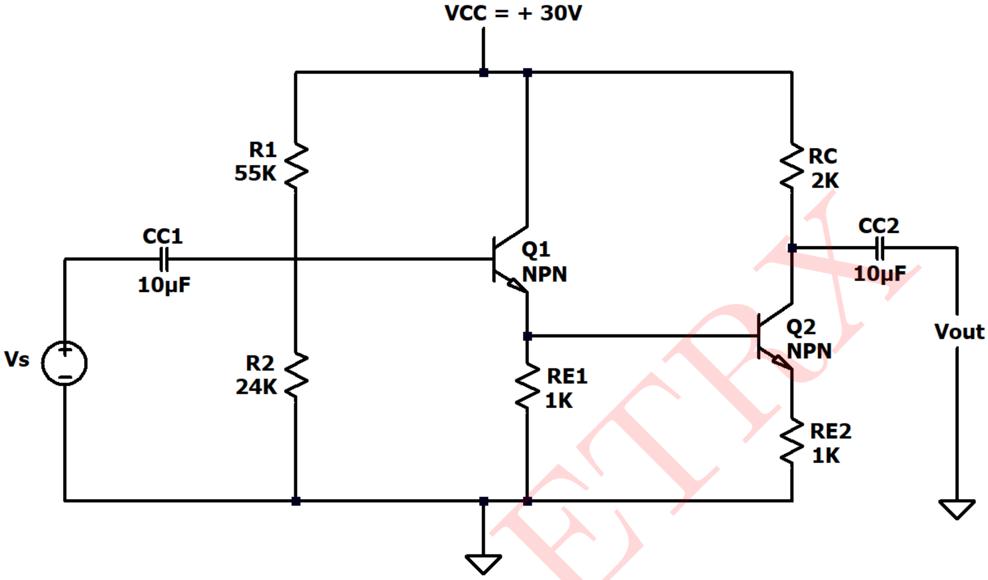

Figure 16: Circuit 1

Solution:

DC ANALYSIS:

$f = 0$, thus $X_C = \infty$, So we replace each capacitor with short circuit,

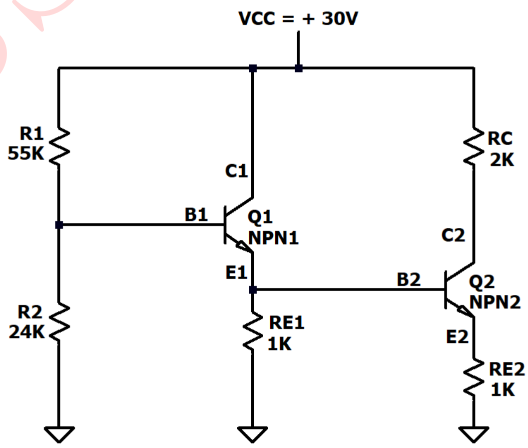

Figure 17: DC Equivalent Circuit

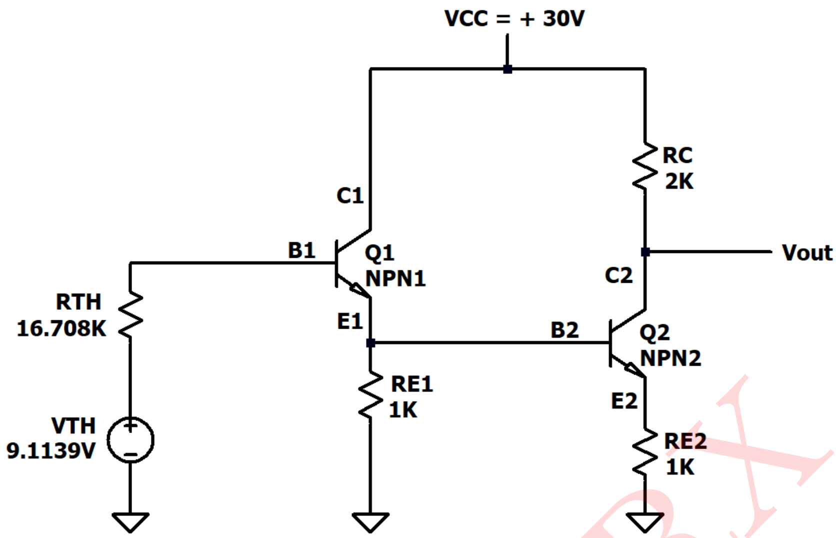

Figure 18: Thevenin Equivalent Circuit

Where, $R_{TH} = R_1 \ || \ R_2 = 55k \ || \ 24k = \mathbf{16.708k\Omega}$

And $V_{TH} = \dfrac{V_{CC} \times R_2}{R_1 + R_2} = 9.1139V$

Applying KVL to base - emitter loop;

Assuming $I_{E1} = I_{RE1}$, I_{B2} is negligible

$V_{TH} - I_{B1}R_{TH} - V_{BE1} - I_{E1}R_{E1} = 0$

But $I_{E1} = (\beta_1 + 1)I_{B1}$

$\therefore V_{TH} - V_{BE1} = I_{B1}R_{Th} + (\beta_1 + 1)I_{B1}R_{E1}$

$$I_{B1} = \frac{V_{TH} - V_{BE1}}{R_{TH} + (\beta_1 + 1)R_{E1}} = \frac{9.1139 - 0.6}{16.708k + (21)(1k)} = \mathbf{0.225mA}$$

$I_{C1} = \beta_1 I_{B1} = 20 \times 0.225 \times 10^{-3} = \mathbf{4.5mA}$

$I_{E1} = I_{C1} + I_{B1} = 4.5mA + 0.225mA = \mathbf{4.74mA}$

$V_{B1} = V_{BE1} + V_{E1}$

Where $V_{E1} = I_{RE1}R_{E1}$ 1

$V_{E1} = 4.74 \times 10^{-3}(1 \times 10^3) = \mathbf{4.74V}$ (since $I_{RE1} \approx I_{E1}$)

$V_{B1} = 4.74 + 0.6 = \mathbf{5.34V}$

From the circuit we can see that

$V_{B2} = V_{E1} = \mathbf{4.74V}$

Also, $V_{B2} = V_{E2} + V_{BE2}$

$V_{E2} = V_{B2} - V_{BE2} = 4.74 - 0.6 = \mathbf{4.14V}$

$I_{E2} = \dfrac{V_{E2}}{R_{E2}} = \dfrac{4.14}{1k} = \mathbf{4.14mA}$

$I_{B2} = \dfrac{I_{E2}}{\beta_2 + 1} = \dfrac{4.14 \times 10^{-3}}{21} = \mathbf{197\mu A}$

$I_{C2} = \beta_2 I_{B2} = 20 \times 197 \times 10^{-6} = \mathbf{3.94mA}$

Rewriting the exact expression of equation 1,

$V_{E1(new)} = I_{RE1} R_{E1}$

$I_{RE1} = I_{E1} - I_{B2} = 4.74mA - 0.197mA = \mathbf{4.543mA}$

$V_{E1(new)} = 4.53 \times 10^{-3} \times 1 \times 10^{3} = \mathbf{4.53V}$

$V_{B2(new)} = V_{E1(new)} = 4.53V$

$V_{B2(new)} = V_{BE2} + V_{E2(new)}$

$V_{E2(new)} = V_{B2(new)} - V_{BE2} = 4.53 - 0.6 = \mathbf{3.943V}$

$I_{E2(new)} = \dfrac{V_{E2(new)}}{R_{E2}} = \dfrac{3.943}{1 \times 10^{3}} = \mathbf{3.943mA}$

$I_{B2(new)} = \dfrac{I_{E2(new)}}{\beta_2 + 1} = \dfrac{3.943 \times 10^{-3}}{21} = \mathbf{187\mu A}$

$I_{C2(new)} = \beta_2 (I_{B2(new)}) = 20 \times 187 \times 10^{6} = \mathbf{3.755mA}$

$V_{C2} = V_{CC} - I_{C2} R_C = 30 - (3.755 \times 10^{-3} \times 2 \times 10^{3}) = \mathbf{22.49V}$

$V_{C1} = \mathbf{30V}$

Node Voltage:

$V_{B1} = 5.34V, \quad V_{B2} = 4.53V$

$V_{C1} = 30V, \quad V_{B2} = 22.49V$

$V_{E1} = 4.53V, \quad V_{E2} = 3.943$

Terminal currents:

$I_{B1} = 225\mu A, \quad I_{B2} = 187\mu A$

$I_{C1} = 4.5mA, \quad I_{B2} = 3.755mA$

$I_{E1} = 4.74mA, \quad I_{E2} = 3.943mA$

Small signal parameters:

$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{C1}} = \frac{20 \times 26 \times 10^{-3}}{4.5 \times 10^{-3}} = \mathbf{115.55\Omega}$$

$$r_{\pi 2} = \frac{\beta_2 V_T}{I_{C2}} = \frac{20 \times 26 \times 10^{-3}}{26 \times 10^{-3}} = 138.48\Omega$$

$$g_{m1} = \frac{I_{CQ1}}{V_T} = \frac{4.5 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{173mA/V}$$

$$g_{m2} = \frac{I_{CQ2}}{V_T} = \frac{3.755 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{144mA/V}$$

AC equivalent circuit:

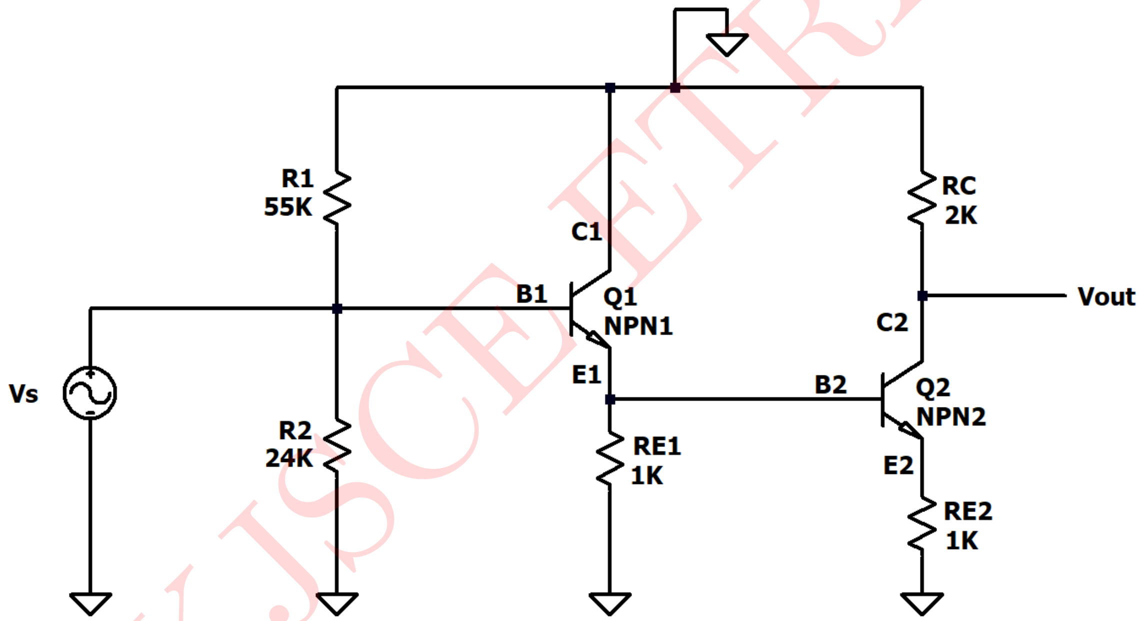

Figure 19: AC equivalent circuit

AC (mid frequency) equivalent circuit:

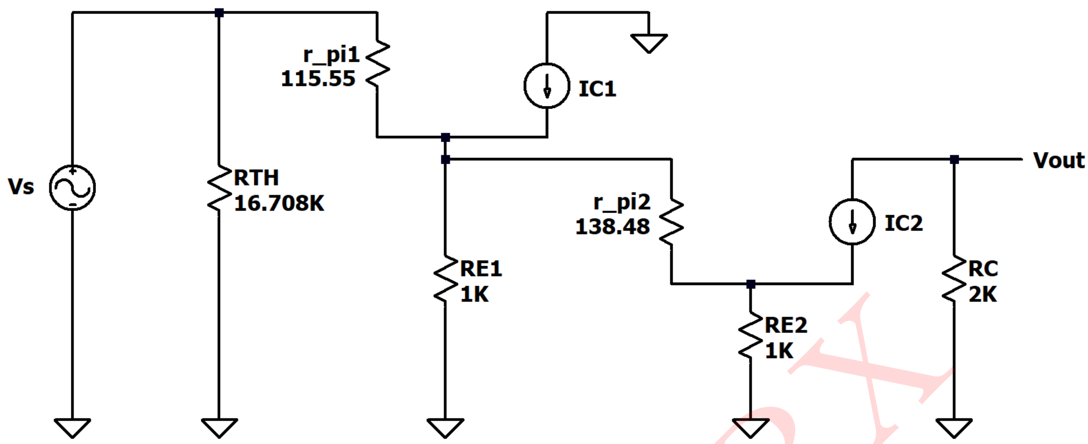

Figure 20: AC (mid band) equivalent circuit

Finding out overall voltage gain:

$$A_{VT} = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_1} \times \frac{V_1}{V_S}$$

$$i_{c2} = g_{m2} V_{\pi 2} = \beta_2 i_{b2}$$

$$\text{Now, } A_{V2} = \frac{V_{out}}{V_1} = -\frac{g_{m2} V_{\pi 2} R_S}{i_{b2}(r_{\pi 2} + (1+\beta_2) R_{E2})} = \frac{-\beta_2 (i_{b2}) R_S}{i_{b2}(r_{\pi 2} + (1+\beta_2) R_{E2})}$$

$$= \frac{-\beta_2) R_C}{(r_{\pi 2} + (1+\beta_2) R_{E2})} = \frac{-20 \times 2 \times 10^3}{138.48 + (21)(1 \times 10^3)} = \mathbf{-1.892}$$

$$i_{C1} = g_{m1 V_{\pi 1}} = \beta_1 (i_{b1})$$

$$A_{V1} = \frac{V_1}{V_S} = \frac{g_{m1} V_{\pi 1} R_{E1}}{i_{b1}(r_{\pi 1} + (1+\beta_1) R_{E1})} = \frac{\beta_1 i_{b1} R_{E1}}{i_{b1}(r_{\pi 1} + (1+\beta_1) R_{E1})} = \frac{\beta_1 R_{E1}}{(r_{\pi 1} + (1+\beta_1) R_{E1})}$$

$$= \frac{20 \times 1 \times 10^3}{115.55 + (21)(1 \times 10^3)} = \mathbf{0.947}$$

Overall voltage gain $= A_{VT} = A_{V1} \times A_{V2} = 0.947 \times (-1.892) = \mathbf{-1.792}$

Finding out output voltage:

$$A_{VT} = \frac{V_{out}}{V_S}$$

let $V_S = 2V(p-p)$

$V_{out} = V_S \times A_{VT} = 2 \times 1.79 = \mathbf{3.58V}$

SIMULATED RESULTS:
Above circuit is simulated in LTspice and the result is as follows:

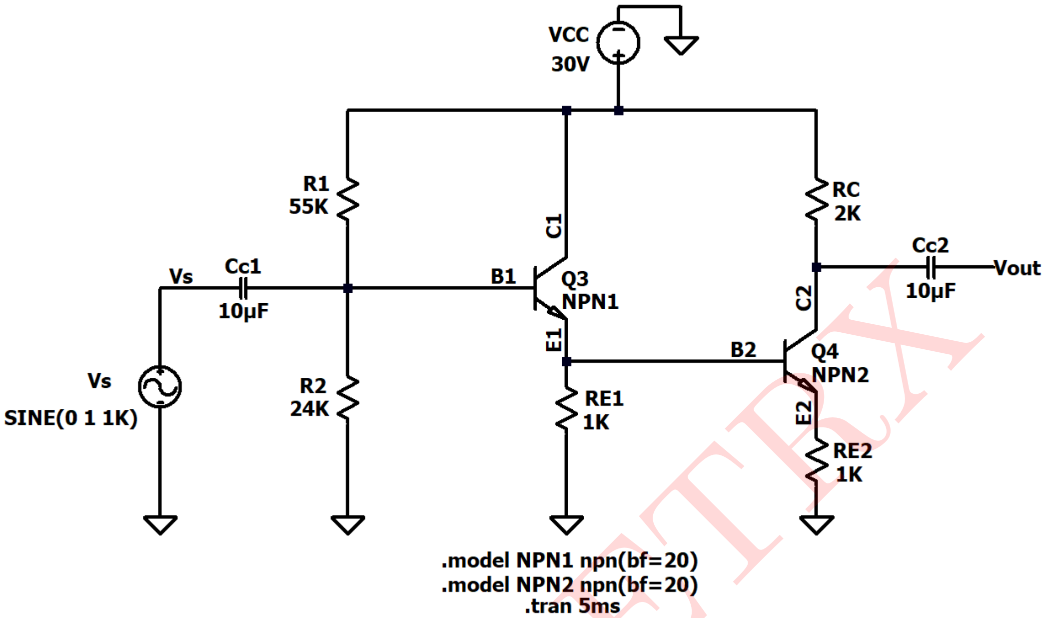

Figure 21: Circuit Schematic

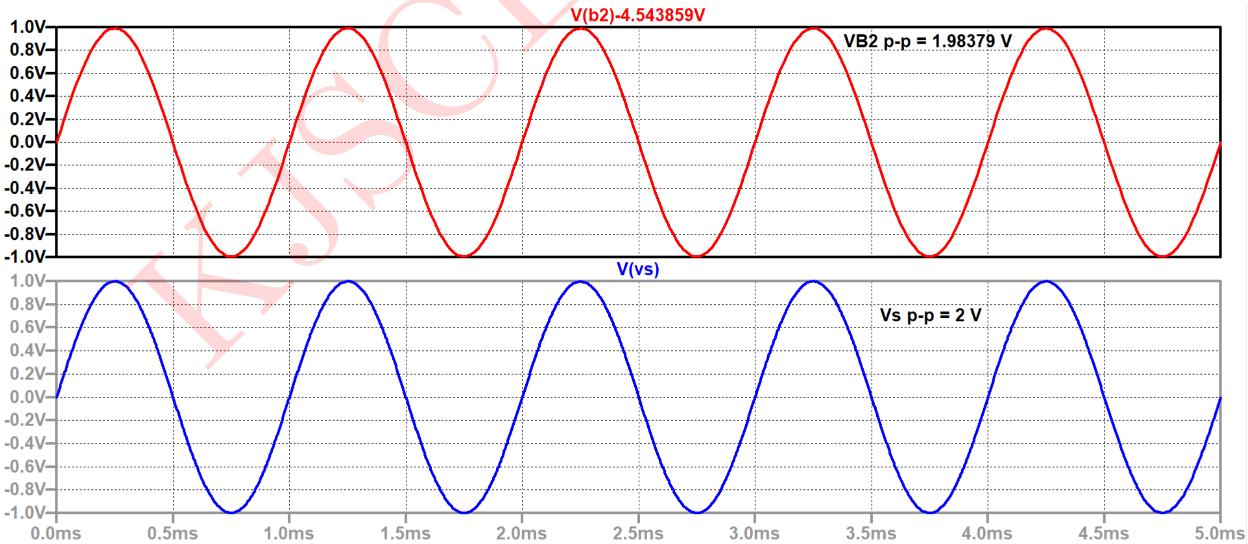

Figure 22: Input output waveform for stage 1

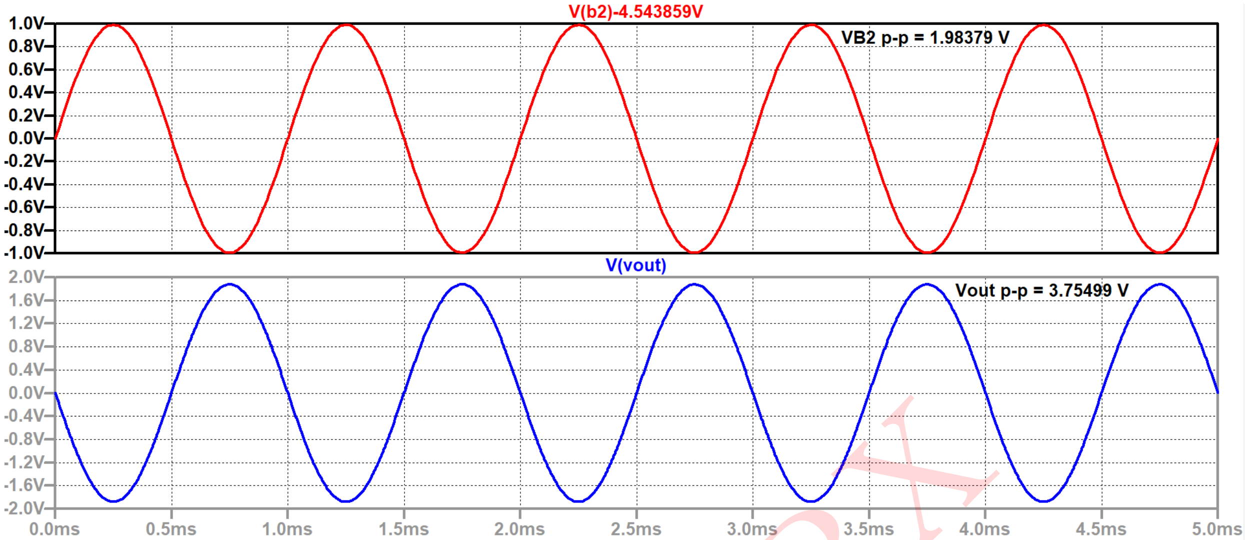

Figure 23: Input output waveform for stage 2

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
I_{B1}	0.22mA	0.225mA
I_{C1}, I_{E1}	4.4mA, 4.62mA	4.5mA , 4.74mA
I_{B2}	$117\mu A$	$1.87\mu A$
I_{C2}	3.55mA	3.755 mA
I_{E2}	3.73 mA	3.943mA
V_{C1}	30V	30V
V_{C2}	22.8V	22.49V
V_{E1}	4.54V	4.53V
V_{E2}	3.736V	3.943V
V_{B1}	5.35V	5.34V
V_{B2}	4.54V	4.53V
A_{VT}	-1.87	-1.79
V_{out}	3.7549V	3.58V

Table 3: Numerical 3

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