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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Darlington Amplifier

Numerical 1:

A two stage circuit is shown in figure 1. Calculate the Q point, input impedance, output impedance, overall voltage gain and overall current gain. Given $\beta_D = 8000$, $V_{BE} = 1.6V$

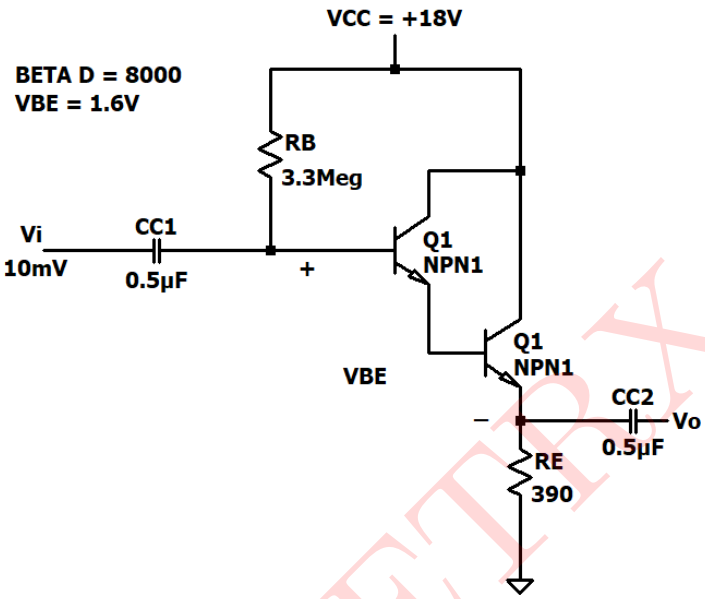

Figure 1: Circuit 1

Solution:

DC Analysis:

For DC Analysis, we open circuit all the capacitors as the frequency is $0Hz$,

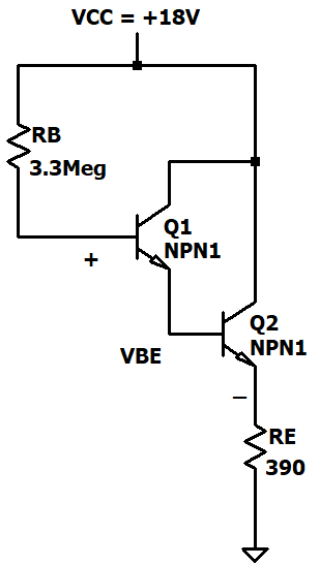

Figure 2: DC Equivalent Circuit

$B_D = \beta_1\beta_2$

Considering $\beta_1 = \beta_2$

$\therefore \beta_D = \beta^2$ [where $\beta = \beta_1 = \beta_2$]

$\beta = 89.44 = \beta_1 = \beta_2$

Applying KVL to Base Emitter loop,

$V_{CC} - I_{B_1Q}R_B - V_{BE} - I_{E_2Q}R_E = 0$

$V_{CC} - I_{B_1Q}R_B - V_{BE} - \beta_D I_{B_1Q}R_E = 0$ [For Darlington pair, $I_{E_2} = \beta_D I_{B_1}$]

$$I_{B_1Q} = \frac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}$$
$$= \frac{18V - 1.6V}{3.3M\Omega + (8000 \times 390\Omega)}$$
$$= \mathbf{2.55\mu A}$$

$$I_{C_1} = \beta_1 I_{B_1}$$
$$= (89.44) \times (2.55\mu A)$$
$$= \mathbf{0.228mA}$$

$$I_{E_1} = I_{C_1} + I_{B_1}$$
$$= 0.228mA + 2.55\mu A$$
$$= \mathbf{0.23mA}$$

$I_{E_1} = I_{B_1} = \mathbf{0.23mA}$

$$I_{C_2} = \beta_2 I_{B_2}$$
$$= (89.44) \times (0.23\mu A)$$
$$= \mathbf{20.57mA}$$

$$I_{E_2} = I_{C_2} + I_{B_2}$$
$$= 20.57mA + 0.23mA$$
$$= \mathbf{20.8mA}$$

$$V_{E_2} = I_{E_2}R_E$$
$$= (20.8mA) \times (390)$$
$$= \mathbf{8.112V}$$

$V_{C_2} = V_{C_1} = \mathbf{18V}$

$$V_{CE_2} = I_{C_2} - V_{E_2}$$
$$= 18 - 8.112$$
$$= \mathbf{9.888V}$$

Small Signal Parameters:

$$r_{\pi_1} = \frac{\beta_1 V_T}{I_{C_1}} = \frac{89.44 \times 0.026V}{0.228mA} = \mathbf{10.199k\Omega}$$

$$r_{\pi_2} = \frac{\beta_2 V_T}{I_{C_2}} = \frac{89.44 \times 0.026V}{20.578mA} = \mathbf{113.05\Omega}$$

AC (Mid Frequency) Equivalent Circuit:

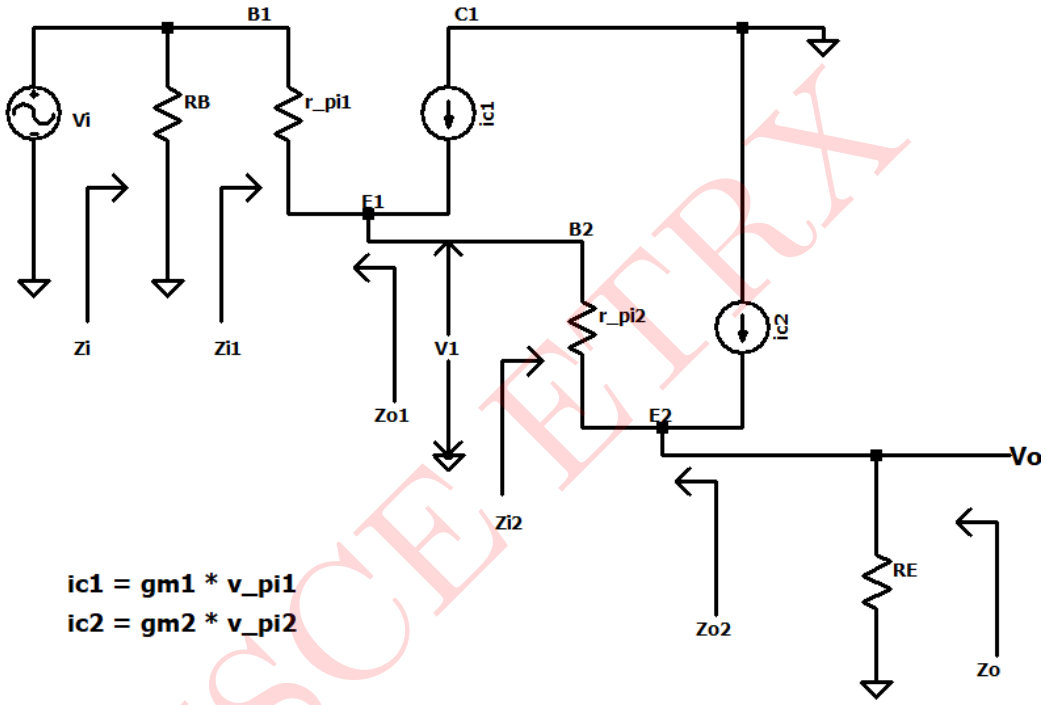

Figure 3: Small Signal Equivalent Circuit

$$\begin{aligned} Z_{i_2} &= r_{\pi_2} + (1+\beta_2)R_E \\ &= 113.05\Omega + (1+89.44)390\Omega \\ &= \mathbf{35.384k\Omega} \end{aligned}$$

$$\begin{aligned} Z_{i_1} &= Z_{i_2}(1+\beta_1) + r_{\pi_1} \\ &= (35.384k\Omega)(1+89.44) + 10.199k\Omega \\ &= \mathbf{3.21M\Omega} \end{aligned}$$

[Input Impedance of Darlington pair is very high]

Input Impedance of 1^{st} stage:$\mathbf{Z_i}$

$$\begin{aligned} Z_i &= R_B \parallel Z_{i_1} \\ &= 3.3M\Omega \parallel 3.21M\Omega \\ &= \mathbf{1.627M\Omega} \end{aligned}$$

[R_B decreases the input impedance of amplifier]

$$\begin{aligned} Z_{o_1} &= \frac{R_B + r_{\pi_1}}{1+\beta_2} \\ &= \frac{3.3M\Omega + 10.199k\Omega}{1+89.44} = \mathbf{36.6k\Omega} \end{aligned}$$

$$Z_{o_2} = \frac{Z_{o_1} + r_{\pi_2}}{1+\beta_2}$$
$$= \frac{36.6k\Omega + 113.05\Omega}{1+89.44}$$
$$= \mathbf{405.938\Omega}$$

Output Impedance of 2^{nd} stage:$\mathbf{Z_o}$

$$Z_o = Z_{o_2} \parallel R_E$$
$$= 405.938 \parallel 390$$
$$= \mathbf{198.9\Omega}$$

Current gain of 1^{st} stage:$\mathbf{Ai_1}$

$$Ai_1 = \frac{I_{E_1}}{I_{B_1}} = 1 + \beta_1 = 1 + 89.44 = \mathbf{90.44}$$

Current gain of 2^{nd} stage:$\mathbf{Ai_2}$

$$Ai_2 = \frac{I_{E_2}}{I_{B_2}} = 1 + \beta_2 = 1 + 89.44 = \mathbf{90.44}$$

Overall current gain: $\mathbf{Ai_T}$

$$Ai_T = Ai_1 \times Ai_2$$
$$= \mathbf{8179.3936}$$ [Current gain of Darlington pair is very high]

Ai_T in dB $= 20\log_{10}(Ai_T) = \mathbf{78.254}$dB

Voltage Gain of $\mathbf{1^{st}}$ stage : Av_1

$$Av_1 = \frac{V_1}{V_i} = \frac{I_{E_1}}{I_{B_1}} \times \frac{Z_{i_2}}{Z_{i_1}} = Ai_1 \times \frac{Z_{i_2}}{Z_{i_1}}$$
$$= 90.44 \times \frac{35.384k\Omega}{3.21M\Omega}$$
$$= \mathbf{0.996}$$

Voltage Gain of $\mathbf{2^{nd}}$ stage : Av_2

$$Av_2 = \frac{V_o}{V_1} = \frac{I_{E_2}}{I_{B_2}} \times \frac{R_E}{Z_{i_2}} = Ai_2 \times \frac{R_E}{Z_{i_2}}$$
$$= 90.44 \times \frac{390\Omega}{35.384k\Omega}$$
$$= \mathbf{0.996}$$

Overall Voltage Gain ($\mathbf{A_{V_T}}$):

$$A_{V_T} = Av_1 \times Av_2$$
$$= 0.996 \times 0.996$$
$$= \mathbf{0.992}$$

Output Voltage ($\mathbf{V_o}$):

$$A_{V_T} = \frac{V_o}{V_i} \implies V_o = A_{V_T} \times V_i$$

$$\therefore V_o = 0.992 \times 10mV$$

$$= \mathbf{9.92V}$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

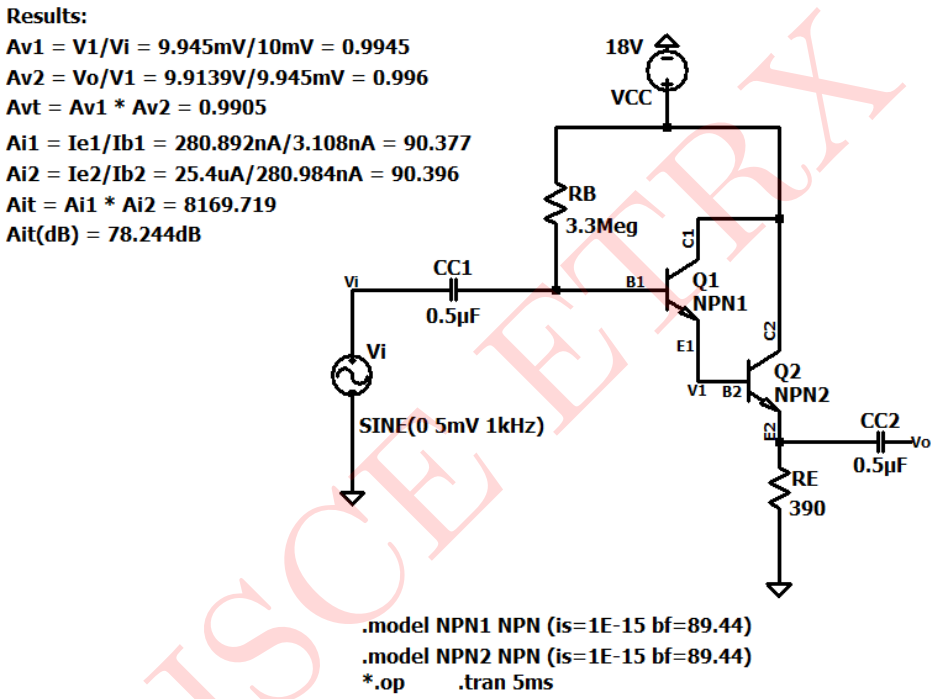

Figure 4: Circuit Schematic

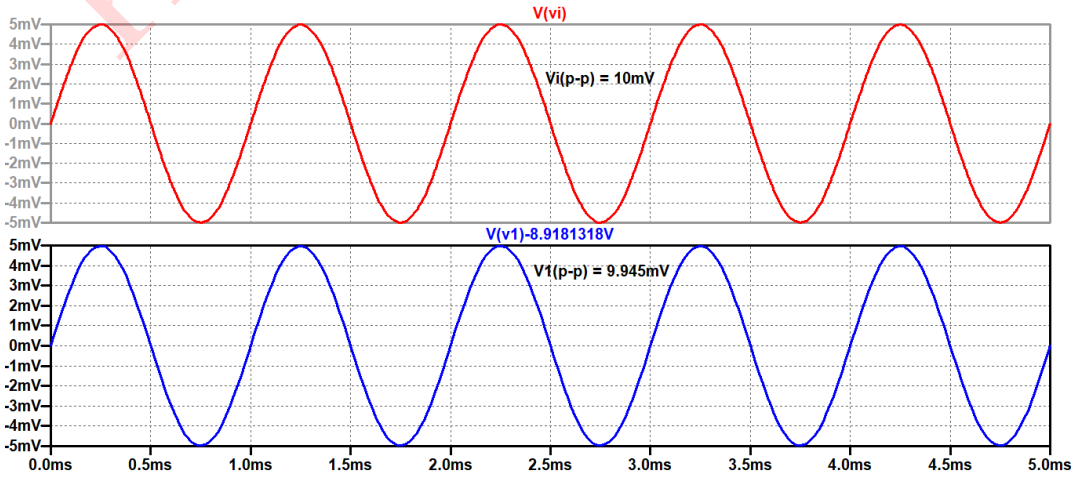

Figure 5: Voltage gain of 1^{st} stage

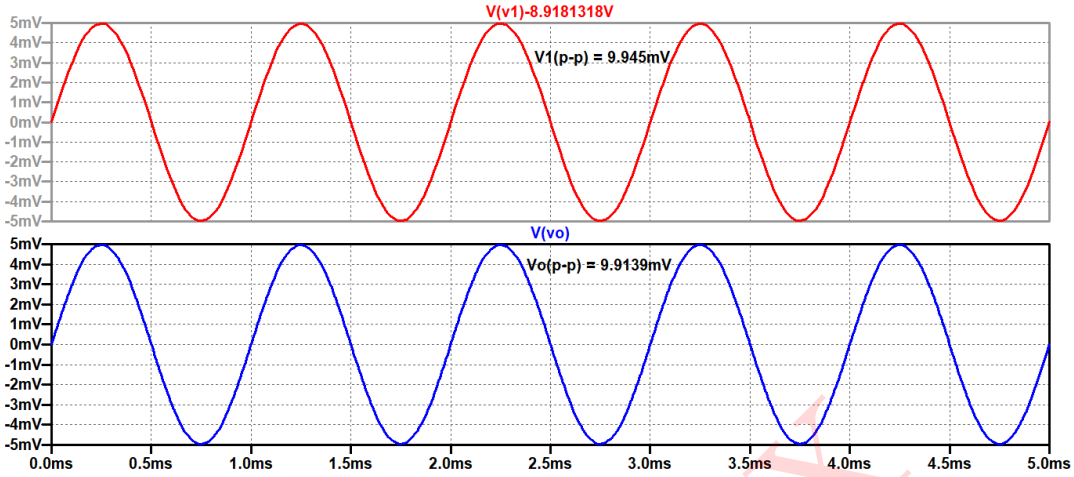

Figure 6: Voltage gain of 2^{nd} stage

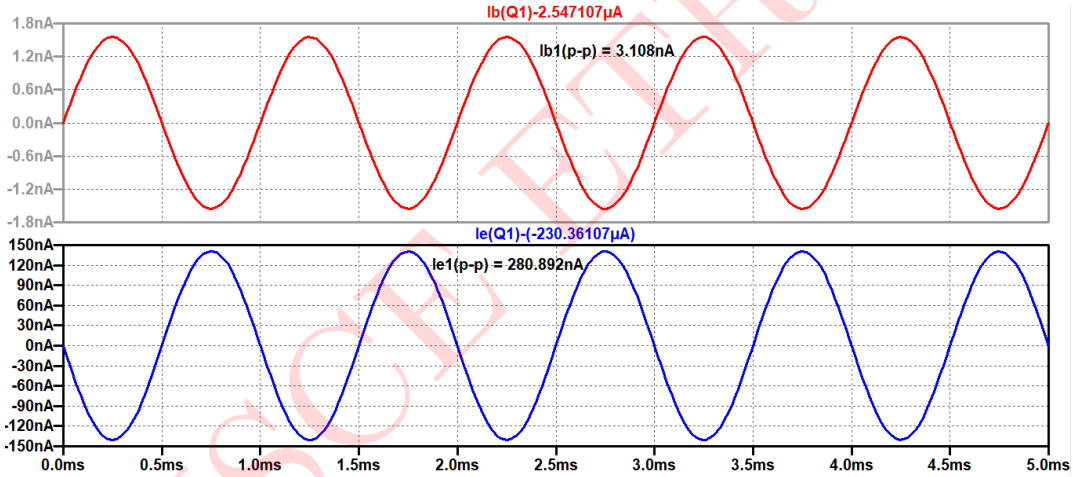

Figure 7: Current gain of 1^{st} stage

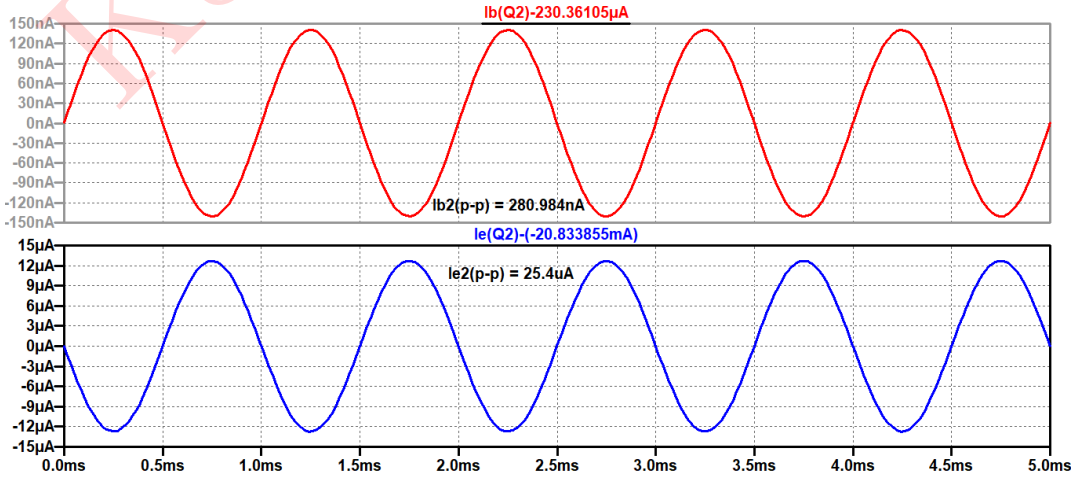

Figure 8: Current gain of 2^{nd} stage

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
I_{B_1}, I_{B_2}	$2.55\mu A$, $0.23mA$	$2.547\mu A$, $0.23mA$
I_{C_1}, I_{C_2}	$0.228mA$, $20.57mA$	$0.2278mA$, $20.6mA$
I_{E_1}, I_{E_2}	$0.23mA$, $20.8mA$	$0.23mA$, $20.83mA$
V_{E_2}	$8.112V$	$8.1252V$
V_{C_2}	$18V$	$18V$
Voltage gain of 1^{st} stage: Av_1	0.996	0.9945
Voltage gain of 2^{nd} stage: Av_2	0.996	0.996
Overall Voltage gain: A_{V_T}	0.992	0.9905
Current gain of 1^{st} stage: Ai_1	90.44	90.377
Current gain of 2^{nd} stage: Ai_2	90.44	90.396
Overall Current gain: Ai_T in dB	78.254dB	78.244dB
Input Impedance of 1^{st} stage: Z_i	$1.627M\Omega$	–
Output Impedance of 2^{nd} stage: Z_o	198.9Ω	–
Output Voltage: V_o	$9.92mV$	$9.9139mV$

Table 1: Numerical 1

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