K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Multi-transistor circuits

Numerical 1: A two-stage circuit is shown in figure 1.

Given: $\beta_1 = \beta_2 = 220$, $V_{BE1} = V_{BE2} = 0.7$ V

a) Calculate input impedance of the circuit.

b) Calculate output impedance of the circuit.

c) Calculate stage 1 voltage gain, stage 2 voltage gain, overall voltage gain in dB and Q point parameters.

d) Output voltage

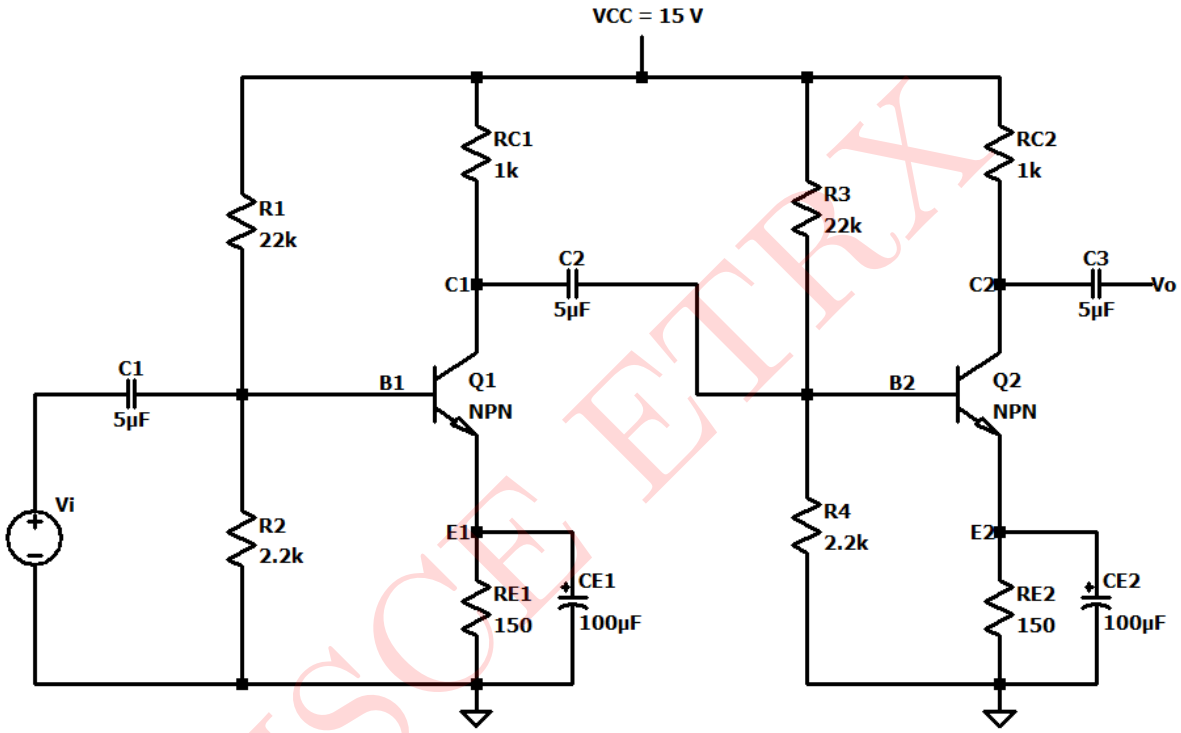

Figure 1: Circuit 1

Solution:

The given circuit 1 is a CE-CE cascade amplifier with voltage divider bias configuration employing npn BJT.

For DC biasing, the capacitors will act as an open source. As both the stages are identical, the DC biasing values will be same for both the stages.

DC Analysis:

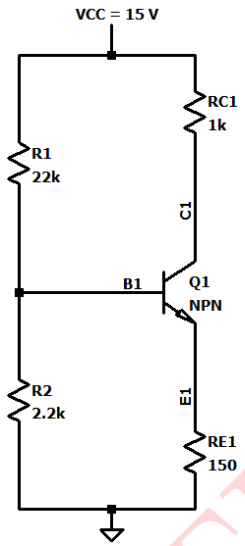

Figure 2: DC Equivalent Circuit

$$R_B = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_B = \frac{22 \times 10^3 \times 2.2 \times 10^3}{22 \times 10^3 + 2.2 \times 10^3} = \mathbf{2\ k\Omega}$$

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

$$V_B = \frac{15 \times 2.2 \times 10^3}{22 \times 10^3 + 2.2 \times 10^3} = \mathbf{1.36\ V}$$

Thevenin's Equivalent circuit:

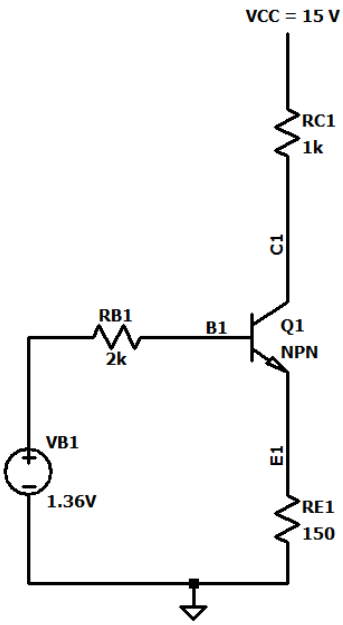

Figure 3: Thevenin's Equivalent circuit

I_{BQ} can be calculated by applying KVL to the base-collector loop,

$V_B - I_B R_B - V_{BE} - I_E R_E = 0$

$I_B R_B + (1+\beta) I_B R_E = V_B - V_{BE}$ ...($\because I_E = (1+\beta) I_B$)

$I_B (R_B + (1+\beta) R_E) = V_B - V_{BE}$

$$I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta) R_E}$$

$$I_B = \frac{1.36 - 0.7}{2 \times 10^3 + (1+220) \times 150} = \mathbf{18.77\ \mu A}$$

$I_{CQ} = \beta I_B$

$I_{CQ} = 220 \times 18.77 \times 10^{-6} = \mathbf{4.13\ mA}$

$I_E = (1+\beta) I_B$

$I_E = (1+220) \times 18.77 \times 10^{-6} = \mathbf{4.15\ mA}$

V_{CEQ} can be calculated by applying KVL to the collector-emitter loop,

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$V_{CE} = 15 - 4.13 \times 10^{-3} \times 1 \times 10^3 - 4.15 \times 10^{-3} \times 150 = \mathbf{10.2475\ V}$

As both the stages are identical,

$I_{B1Q} = I_{B2Q} = \mathbf{18.77\ \mu A}$

$I_{C1Q} = I_{C2Q} = \mathbf{4.13\ mA}$

$I_{E1} = I_{E2} = \mathbf{4.15\ mA}$

$V_{CE1Q} = V_{CE2Q} = \mathbf{10.2475\ V}$

AC Analysis:

Small Signal Parameters:

$$r_\pi = \frac{\beta V_T}{I_E}$$

$$r_\pi = \frac{220 \times 26 \times 10^{-3}}{4.15 \times 10^{-3}} = \mathbf{1.378\ k\Omega}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$g_m = \frac{4.13 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{158.85\ mA/V}$$

As both the stages are identical

$r_{\pi_1} = r_{\pi_2} = \mathbf{1.378\ k\Omega}$

$g_{m_1} = g_{m_2} = \mathbf{158.85\ mA/V}$

Small Signal Equivalent Circuit is shown in figure 4:

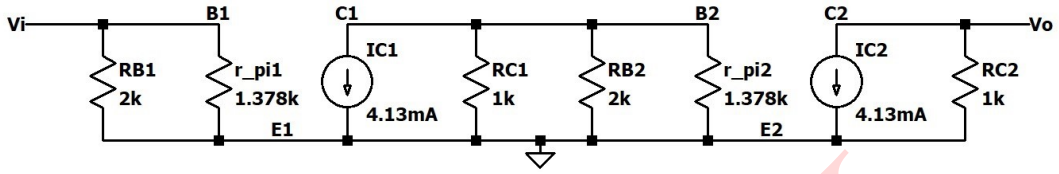

Figure 4: Small Signal Equivalent Circuit

Stage 1 voltage gain:

$$A_{V_1} = \frac{-g_m V_{\pi_1}(R_{C_1} \ || \ R_{B_2} \ || \ r_{\pi_2})}{V_{\pi_1}}$$

$$A_{V_1} = -g_m(R_{C_1} \ || \ R_{B_2} \ || \ r_{\pi_2})$$

$$A_{V_1} = -158.85 \times 10^{-3}(1 \times 10^3 \ || \ 2 \times 10^3 \ || \ 1.378 \times 10^3) = \mathbf{-71.37}$$

A_{V_1} in dB $= 20\log_{10}(|A_{V_1}|)$

A_{V_1} in dB $= 20\log_{10}(71.37) = \mathbf{37.07\ dB}$

Stage 2 Voltage gain:

$$A_{V_2} = \frac{-g_m V_{\pi_2}(R_{C_2})}{V_{\pi_2}}$$

$$A_{V_2} = -g_m R_{C_2}$$

$$A_{V_2} = -158.85 \times 10^{-3} \times 1 \times 10^3 = \mathbf{-158.85}$$

A_{V_2} in dB $= 20\log_{10}(|A_{V_2}|)$

A_{V_2} in dB $= 20\log_{10}(158.85) = \mathbf{44.02\ dB}$

Overall voltage gain:

$A_{VT} = A_{V_1} \times A_{V_2}$

$A_{VT} = (-71.37) \times (-158.85) = \mathbf{11337}$

A_{VT} in dB $= 20\log_{10}(|A_{VT}|)$

A_{VT} in dB $= 20\log_{10}(11337) = \mathbf{81.09\ dB}$

Input impedance of stage 1:

$Z_i = (R_{B_1} \ || \ r_{\pi_1})$

$Z_i = (2 \times 10^3 \ || \ 1.378 \times 10^3) = \mathbf{815.87\ \Omega}$

Output impedance of stage 2:

$Z_o = R_{C_2} = \mathbf{1\ k\Omega}$

Output Voltage:

$V_o = A_{VT} V_i$

$V_o = 11337 \times 0.1 \times 10^{-3} = \mathbf{1.1337\ V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

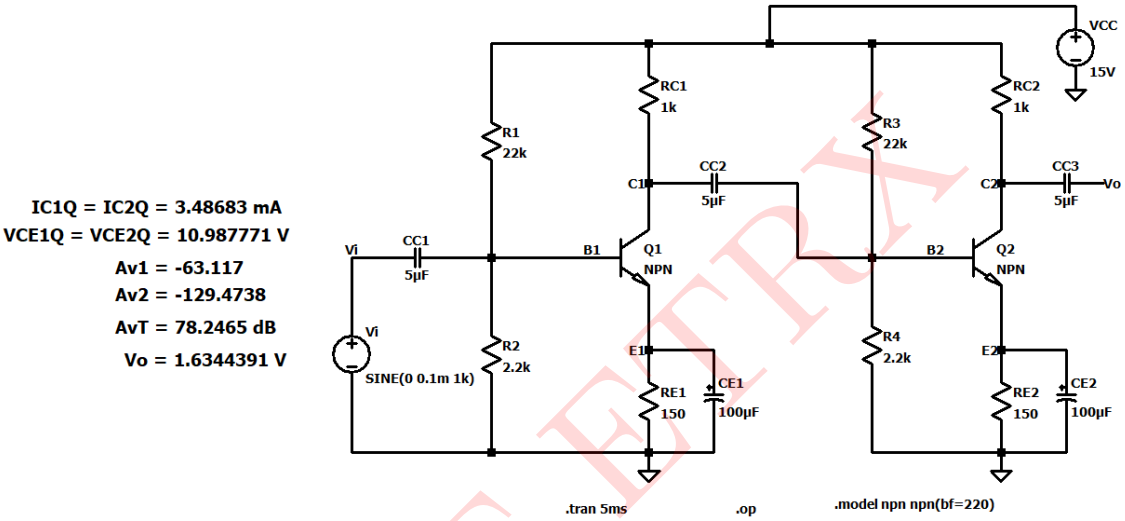

Figure 5: Circuit Schematic 1: Results

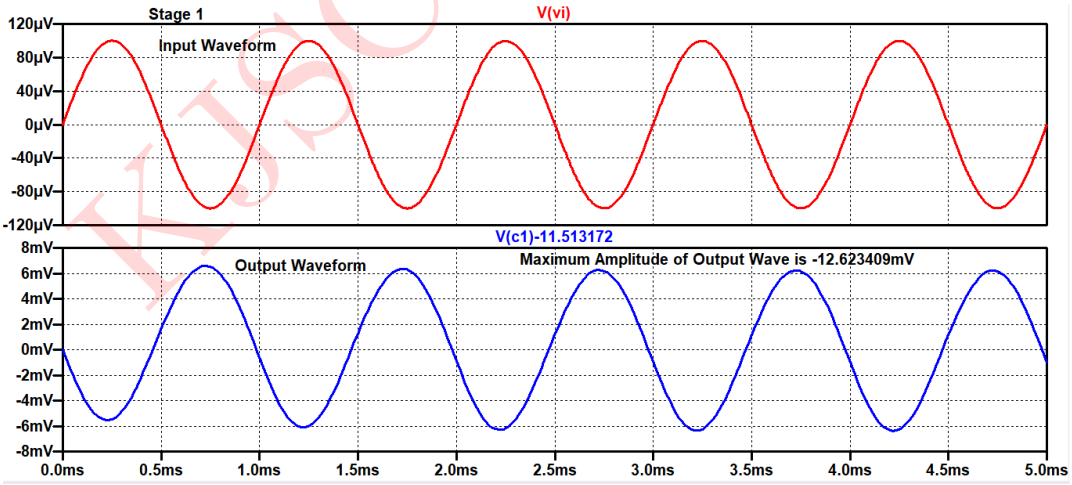

Figure 6: Input & Output waveforms for stage 1

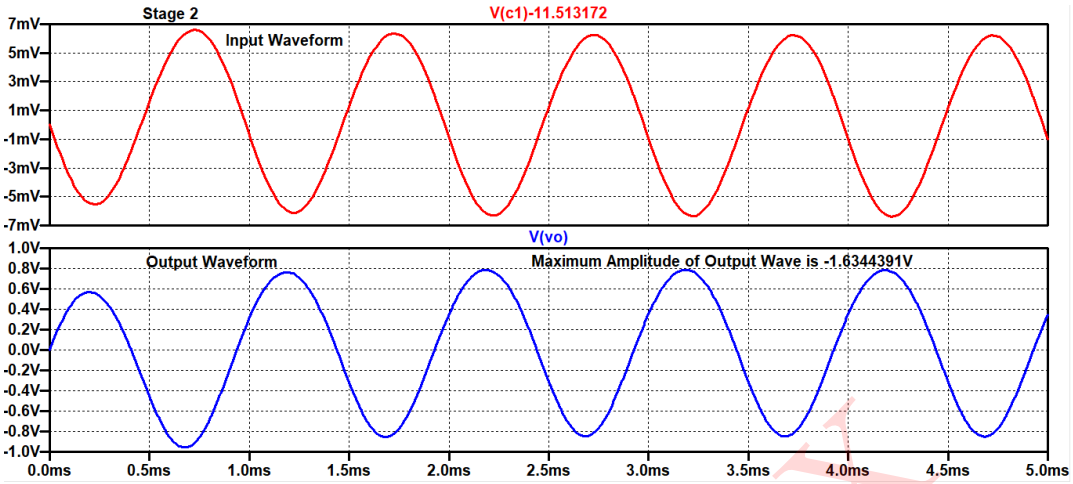

Figure 7: Input & Output waveforms for stage 2

Comparison of theoretical and simulated values:

Parameters	**Theoretical Values**	**Simulated Values**
Stage 1 Q point	4.13 mA	3.4868 mA
I_{C1Q}, V_{CE1Q}	10.2475 V	10.9877 V
Stage 2 Q point	4.13 mA	3.4868 mA
I_{C2Q}, V_{CE2Q}	10.2475 V	10.9877 V
Voltage gain of stage 1: A_{V1}	−71.37	−63.117
Voltage gain of stage 2: A_{V2}	−158.85	−129.4738
Overall voltage gain: A_{VT}	81.09 dB	78.2465 dB
Output Voltage	1.1337 V	1.6344 V
Input impedance of stage 1	815.87 Ω	–
Output impedance of stage 2	11 kΩ	–

Table 1: Numerical 1

Numerical 2: For the given circuit 2, calculate Q point values for both the stages, stage 1 and stage 2 voltage gain, overall voltage gain and output voltage. Calculate the load voltage if a 10 kΩ load is connected across the output. Also calculate input impedance and output impedance of the circuit.

Given: $I_{DSS_1} = I_{DSS_2} = 10$ mA, $V_{P_1} = V_{P_2} = -4$ V

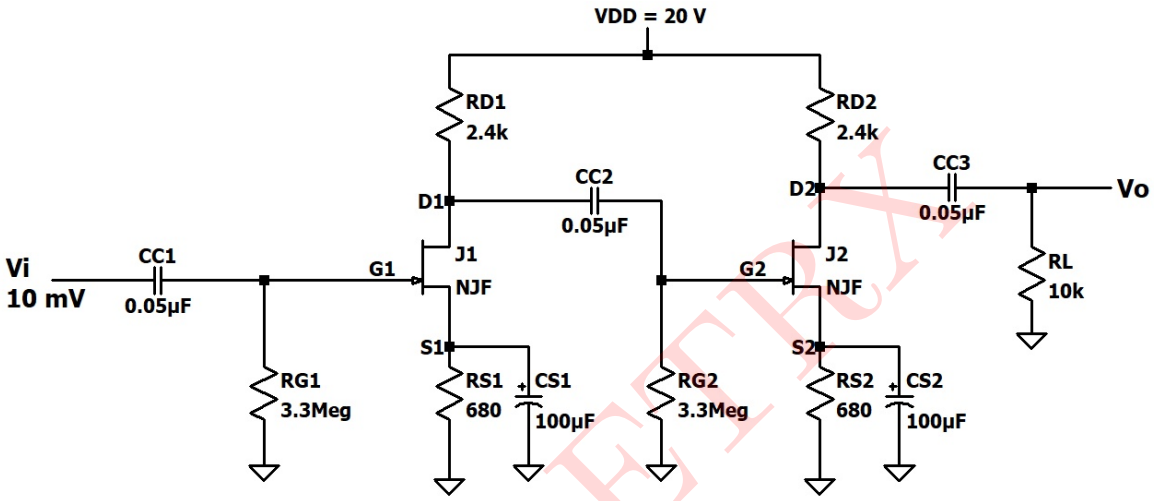

Figure 8: Circuit 2

Solution:

The given circuit 2 is a CS-CS cascade amplifier employing n-JFET.

For DC biasing, the capacitors will act as an open source. As both the stages are identical, the DC biasing values will be same for both the stages.

DC Analysis:

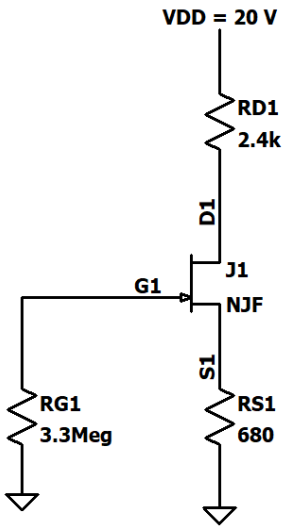

Figure 9: DC Equivalent Circuit

Applying KVL to the gate-source loop,

$-I_G R_G - V_{GS} - I_D R_S = 0$

$V_{GS} = -I_D R_S$ ...($\because I_G = 0$)

$V_{GS} = -I_D 680$

$I_D = \dfrac{-V_{GS}}{680}$ ...(1)

From current equation,

$I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2$

$I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{-4}\right)^2$

$-V_{GS} = \dfrac{680 \times 10 \times 10^{-3}}{16}(4 + V_{GS})^2$

$-V_{GS} = 0.425(16 + 8V_{GS} + V_{GS}^2)$

$-V_{GS} = 6.8 + 3.4V_{GS} + 0.425V_{GS}^2$

$0.425V_{GS}^2 + 4.4V_{GS} + 6.8 = 0$

$V_{GS} = \mathbf{-1.89}$ & $V_{GS} = \mathbf{-8.46}$

Let, $V_{GS} = -1.89$

$I_D = \dfrac{-(-1.89)}{680} = \mathbf{2.7794\ mA}$ ...(from 1)

Let, $V_{GS} = -8.46$

$I_D = \dfrac{-(-8.46)}{680} = \mathbf{12.4411\ mA}$ ...(from 1)

Since Q point should lie in the middle of the transfer characteristics,

$I_{DQ} = \mathbf{2.7794\ mA}$

$V_{GSQ} = \mathbf{-1.89\ V}$

Applying KVL to the drain-source loop,

$V_{DD} - I_D R_D - V_{DSQ} - I_D R_S = 0$

$V_{DSQ} = V_{DD} - I_D R_D - I_D R_S$

$V_{DSQ} = 20 - 2.7794 \times 10^{-3} \times 2.4 \times 10^3 - 2.7794 \times 10^{-3} \times 680 = \mathbf{11.4394\ V}$

As both the stages are identical,

$I_{D1Q} = I_{D2Q} = \mathbf{2.7794\ mA}$

$V_{GS1Q} = V_{GS2Q} = \mathbf{-1.89\ V}$

$V_{DS1Q} = V_{DS2Q} = \mathbf{11.4394\ V}$

AC Analysis:

Small signal parameters:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = \frac{2 \times 10 \times 10^{-3}}{4}\left(1 - \frac{(-1.89)}{-4}\right) = \mathbf{2.6375\ mA/V}$$

As both the stages are identical,

$g_{m_1} = g_{m_2} = \mathbf{2.6375\ mA/V}$

Small Signal Equivalent Circuit is shown in figure 10:

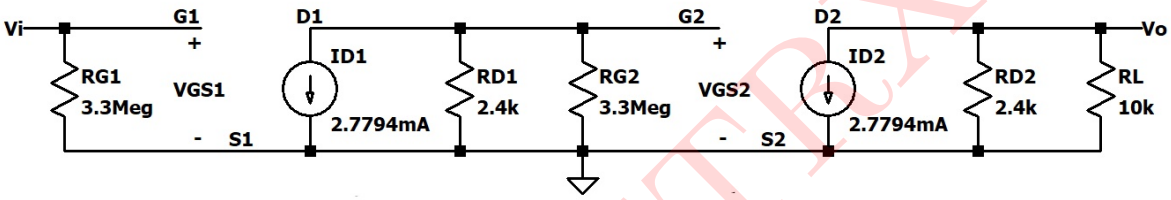

Figure 10: Small Signal Equivalent Circuit

Stage 1 voltage gain:

$$A_{V_1} = \frac{-g_{m_1} V_{gs_1}(R_{D_1} \parallel R_{G_2})}{V_{gs_1}}$$

$$A_{V_1} = -g_{m_1}(R_{D_1} \parallel R_{G_2})$$

$$A_{V_1} = -2.6375 \times 10^{-3}(2.4 \times 10^3 \parallel 3.3 \times 10^6)$$

$$A_{V_1} = -2.6375 \times 10^{-3} \times 2.3982 \times 10^3 = \mathbf{-6.3252}$$

Stage 2 Voltage gain:

$$A_{V_2} = \frac{-g_{m_2} V_{gs_2}(R_{D_2})}{V_{gs_2}}$$

$$A_{V_2} = -g_{m_2} R_{D_2}$$

$$A_{V_2} = -2.6375 \times 10^{-3} \times 2.4 \times 10^3 = \mathbf{-6.33}$$

Overall voltage gain:

$$A_{VT} = A_{V_1} \times A_{V_2}$$

$$A_{VT} = (-6.3252) \times (-6.33) = \mathbf{40.0385}$$

$$A_{VT} \text{ in dB} = 20\log_{10}(|A_{VT}|)$$

$$A_{VT} \text{ in dB} = 20\log_{10}(40.0385) = \mathbf{32.0495\ dB}$$

Input impedance of stage 1:

$$Z_i = R_{G_1} = 3.3\ \text{M}\Omega$$

output impedance of stage 2:

$$Z_o = R_{D_2} = 2.4\ \text{k}\Omega$$

Output Voltage:

$V_o = A_{VT} V_i$

$V_o = 40.0385 \times 10 \times 10^{-3} = \mathbf{400.385\ mV}$

Overall voltage gain with load:

$A_{VTL} = A_{V_1} \times A_{V_2}$

$A_{VTL} = -g_{m_1}(R_{D_1} \parallel R_{G_2}) \times -g_{m_2}(R_{D_2} \parallel R_L)$

$A_{VTL} = 2.6375 \times 10^{-3}(2.4 \times 10^3 \parallel 3.3 \times 10^6) \times 2.6375 \times 10^{-3}(2.4 \times 10^3 \parallel 10 \times 10^3)$

$A_{VTL} = 6.3252 \times 5.1048 = \mathbf{32.2888}$

A_{VTL} in dB $= 20\log_{10}(|A_{VTL}|)$

A_{VTL} in dB $= 20\log_{10}(|32.2888|) = \mathbf{30.1810\ dB}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

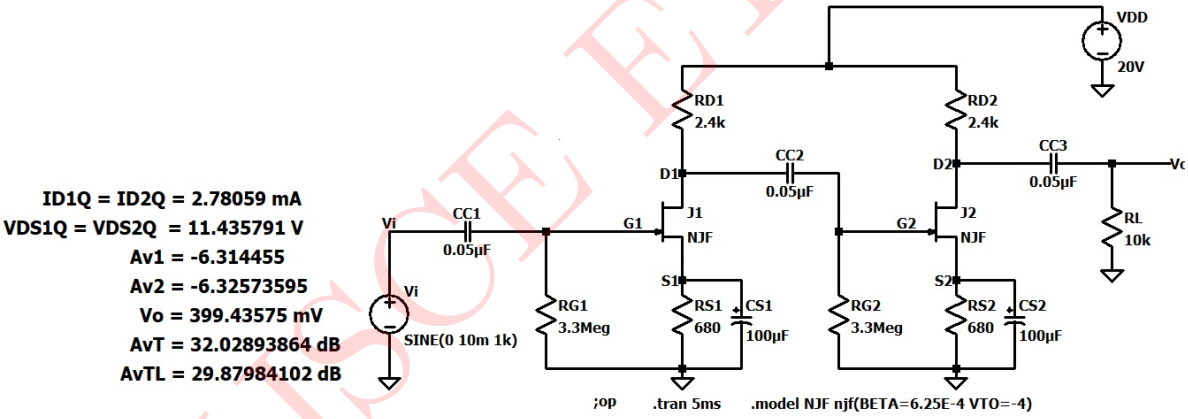

Figure 11: Circuit Schematic 2: Results

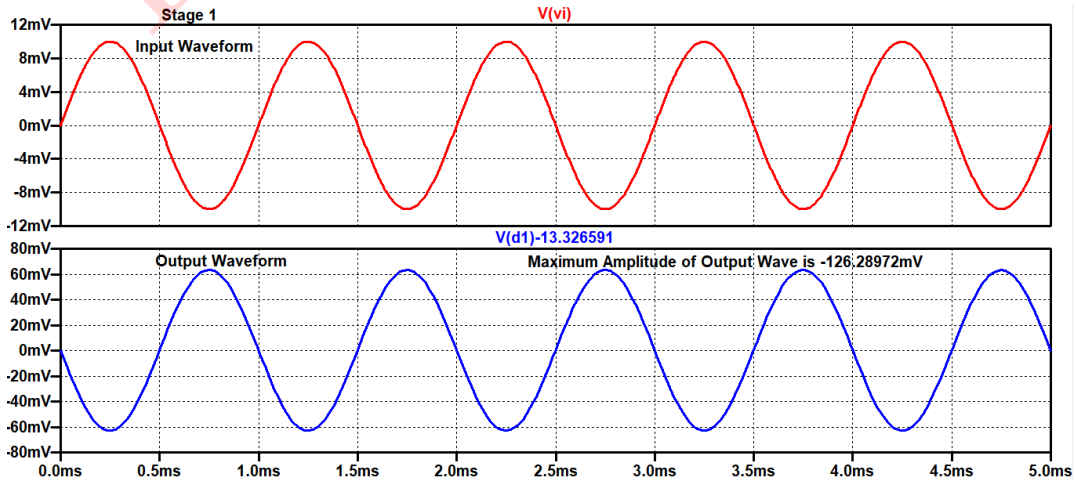

Figure 12: Input & Output waveforms for stage 1

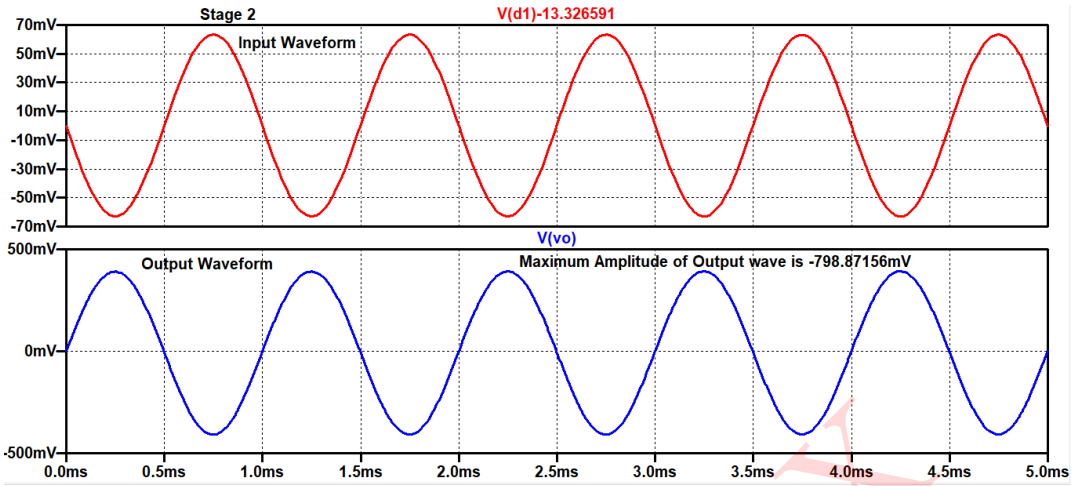

Figure 13: Input & Output waveforms for stage 2

Comparison of theoretical and simulated values:

Parameters	Theoretical Values	Simulated Values
1st stage Q point I_{D1Q}, V_{DS1Q}	2.7794 mA, 11.4394 V	2.7805 mA, 11.4357 V
2nd Stage Q point I_{D2Q}, V_{DS2Q}	2.7794 mA, 11.4394 V	2.7805 mA, 11.4397 V
Voltage gain of stage 1: A_{V1}	-6.3252	-6.3144
Voltage gain of stage 2: A_{V2}	-6.33	-6.3257
Overall voltage gain: A_{VT} in dB	32.0495 dB	32.0289 dB
Overall voltage gain: A_{VT} in dB	30.1810 dB	29.8798 dB
Input impedance of stage 1	3.3 MΩ	–
Output impedance of stage 2	2.4 kΩ	–
Output Voltage	400.385 mV	399.4357 mV

Table 2: Numerical 2

Numerical 3: Consider the circuit shown in figure 14. The current gain for the npn transistor is $\beta_1 = 120$ and for the pnp transistor is $\beta_2 = 80$

Determine: I_{B_1}, I_{C_1}, I_{E_1}, I_{B_2}, I_{C_2}, I_{E_2}, V_{C_1}, V_{C_2}, V_{E_1}, V_{E_2}, V_{B_1}, V_{B_2}, V_{CE_1}, V_{EC_2}

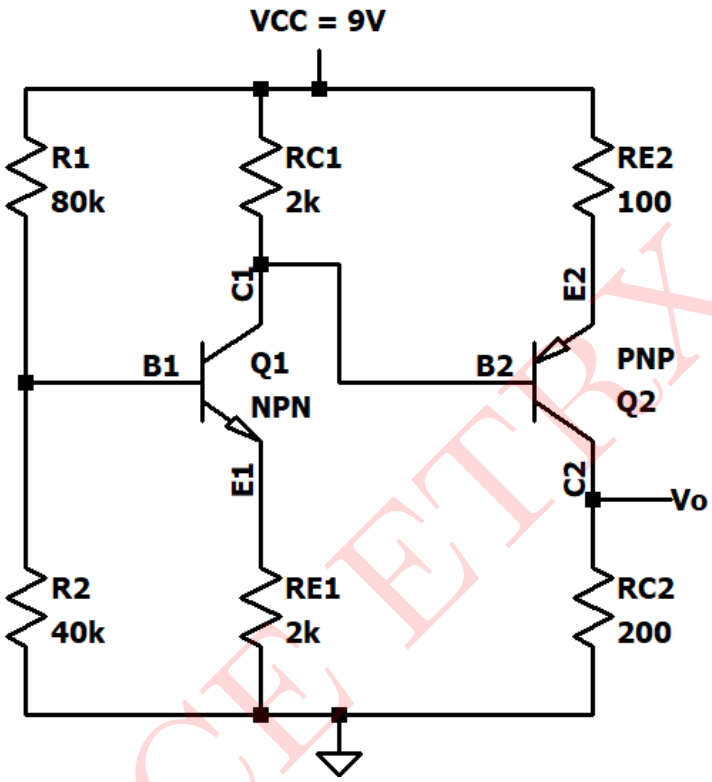

Figure 14: Circuit 3

Solution:

The given circuit 3 is a direct-coupled cascade amplifier employing npn and pnp BJT.

Calculating thevenin's equivalent of base circuit of transistor Q_1:

$$V_{B_1} = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

$$V_{B_1} = \frac{9 \times 40 \times 10^3}{80 \times 10^3 + 40 \times 10^3} = \mathbf{3\ V}$$

$$R_{B_1} = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_{B_1} = \frac{80 \times 10^3 \times 40 \times 10^3}{80 \times 10^3 + 40 \times 10^3} = \mathbf{26.67\ k\Omega}$$

Thevenin's Equivalent circuit:

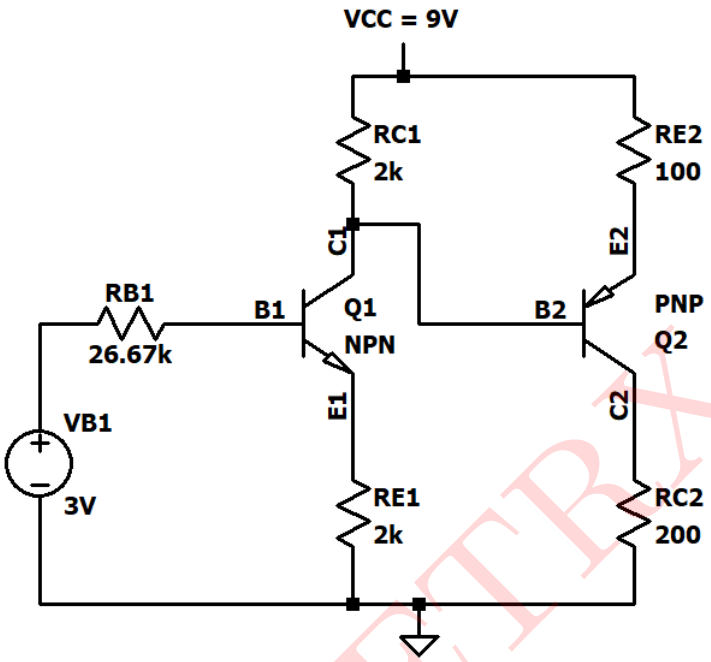

Figure 15: Thevenin's Equivalent circuit

I_{B_1} can be calculated by applying KVL to the base-emitter loop of transistor Q_1,

$$V_{B_1} - I_{B_1}R_{B_1} - V_{BE_1} - I_{E_1}R_{E_1} = 0$$

$$I_{B_1}R_{B_1} + (1+\beta_1)I_{B_1}R_{E_1} = V_{B_1} - V_{BE_1}$$

$$I_{B_1}(R_{B_1} + (1+\beta_1)R_{E_1}) = V_{B_1} - V_{BE_1}$$

$$I_{B_1} = \frac{V_{B_1} - V_{BE_1}}{R_{B_1} + (1+\beta_1)R_{E_1}}$$

$$I_{B_1} = \frac{3 - 0.7}{26.67 \times 10^3 + (1+120) \times 2 \times 10^3} = \mathbf{8.56\ \mu A}$$

$$I_{C_1} = \beta_1 I_{B_1}$$

$$I_{C_1} = 120 \times 8.56 \times 10^{-6} = \mathbf{1.027\ mA}$$

$$I_{E_1} = (1+\beta_1)I_{B_1}$$

$$I_{E_1} = (1+120) \times 8.56 \times 10^{-6} = \mathbf{1.035\ mA}$$

Voltage at terminal C_1 is given as,

$$V_{C_1} = V_{CC} - I_{C_1}R_{C_1}$$

$$V_{C_1} = 9 - 1.027 \times 10^{-3} \times 2 \times 10^3 = \mathbf{6.946\ V}$$

Voltage at terminal E_1 is given as,

$$V_{E_1} = I_{E_1}R_{E_1}$$

$$V_{E_1} = 1.035 \times 10^{-3} \times 2 \times 10^3 = \mathbf{2.07\ V}$$

Voltage across terminal C_1 is same as voltage across terminal B_2,

$V_{C_1} = V_{B_2} = \mathbf{6.946\ V}$

Voltage across terminal E_2 is given as,

$V_{E_2} = V_{B_2} + V_{EB_2}$

$V_{E_2} = 6.946 + 0.7 = \mathbf{7.646\ V}$

$$I_{E_2} = \frac{V_{CC} - V_{E_2}}{R_{E_2}}$$

$$I_{E_2} = \frac{9 - 7.646}{100} = \mathbf{13.54\ mA}$$

$$I_{B_2} = \frac{I_{E_2}}{1 + \beta_2}$$

$$I_{B_2} = \frac{13.54 \times 10^{-3}}{81} = \mathbf{167.16\ \mu A}$$

$I_{C_2} = \beta_2 I_{B_2}$

$I_{C_2} = 80 \times 167.16 \times 10^{-6} = \mathbf{13.37\ mA}$

Now, rewriting exact exprssion for equation 1,

$V_{C_1} = V_{CC} - I_{RC_1} R_{C_1}$

$I_{RC_1} = I_{C_1} - I_{B_2}$

$I_{RC_1} = 1.027 \times 10^{-3} - 167.16 \times 10^{-6} = \mathbf{0.859\ mA}$

$V_{C_1\,new} = 9 - 0.859 \times 10^{-3} \times 2 \times 10^{3} = \mathbf{7.282\ V}$

$V_{E_2\,new} = V_{C_1\,new} + V_{EB_2}$

$V_{E_2\,new} = 7.282 + 0.7 = \mathbf{7.982\ V}$

$$I_{E_2\,new} = \frac{V_{CC} - V_{E_2\,new}}{R_{E_2}}$$

$$I_{E_2\,new} = \frac{9 - 7.982}{100} = \mathbf{10.18\ mA}$$

$$I_{B_2\,new} = \frac{I_{E_2\,new}}{1 + \beta_2}$$

$$I_{B_2\,new} = \frac{10.18 \times 10^{-3}}{1 + 80} = \mathbf{125.67\ \mu A}$$

$I_{C_2\,new} = \beta_2 I_{B_2}$

$I_{C_2\,new} = 80 \times 125.67 \times 10^{-6} = \mathbf{10.05\ mA}$

Voltage across terminal C_2 is given as,

$V_{C_2} = I_{C_2} R_{C_2}$

$V_{C_2} = 10.05 \times 10^{-3} \times 200 = \mathbf{2.01\ V}$

Voltage across terminal B_2 is same as voltage across terminal C_1,

$V_{B_2} = V_{C_1\,new} =$ **7.282 V**

Voltage between terminal C_1 and terminal E_1 is given as,

$V_{CE_1} = V_{C_1} - V_{E_1}$

$V_{CE_1} = 7.282 - 2.07 =$ **5.212 V**

Voltage between terminal E_2 and terminal C_2 is given as,

$V_{EC_2} = V_{E_2} - V_{C_2}$

$V_{EC_2} = 7.982 - 2.01 =$ **5.972 V**

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

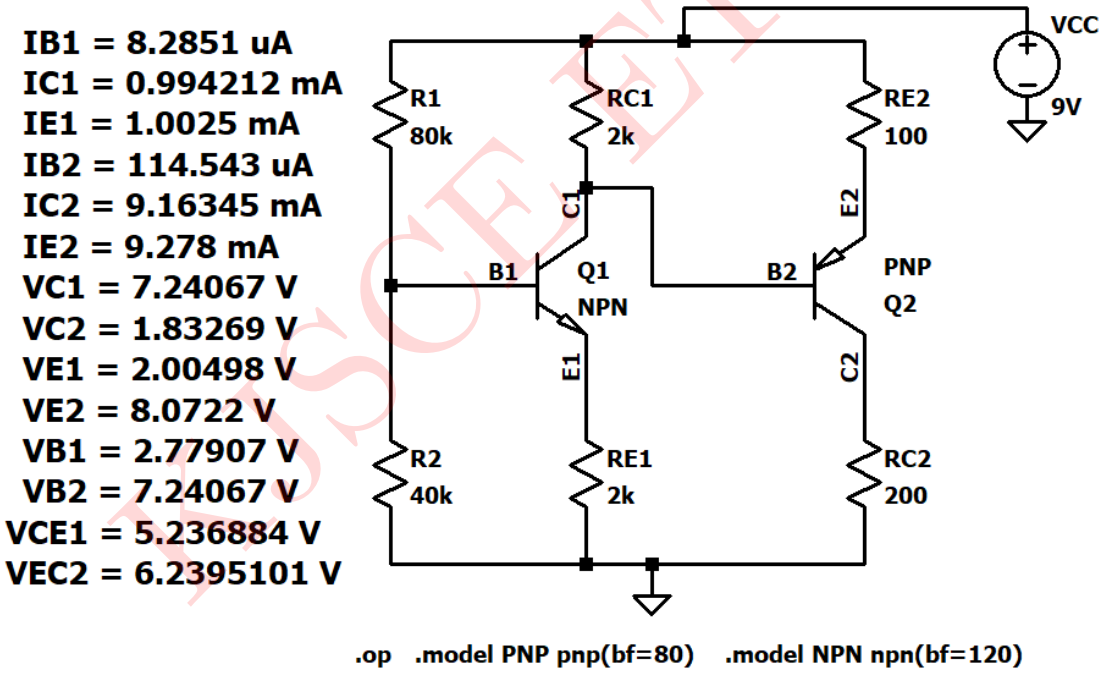

Figure 16: Circuit Schematic 3: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical Values	Simulated Values
I_{B_1}	8.56 μA	8.2851 μA
I_{C_1}	1.027 mA	0.9942 μA
I_{E_1}	1.035 mA	1.0025 μA
I_{B_2}	125.67 μA	114.543 μA
I_{C_2}	10.05 mA	9.1634 μA
I_{E_2}	10.18 mA	9.278 μA
V_{C_1}	7.282 V	7.2406 V
V_{C_2}	2.01 V	1.8326 V
V_{E_1}	2.07 V	2.0049 V
V_{E_2}	7.982 V	8.0722 V
V_{B_1}	3 V	2.7790 V
V_{B_2}	7.282 V	7.2406 V
V_{CE_1}	5.212 V	5.2368 V
V_{EC_2}	5.972 V	6.2395 V

Table 3: Numerical 3

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