K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Oscillator Circuits

Design 1

Design a RC phase shift oscillator to oscillate at 800Hz. Supply voltage is 10V

Solution:

1) Selection of transistor and circuit diagram:

Select transistor BC147A:

$h_{fe}(typ) = 220$, $h_{FE}(typ) = \beta = 180$, $h_{ie} = r_\pi = 2.7k\Omega$, $V_{CE_{sat}} = 0.25V$

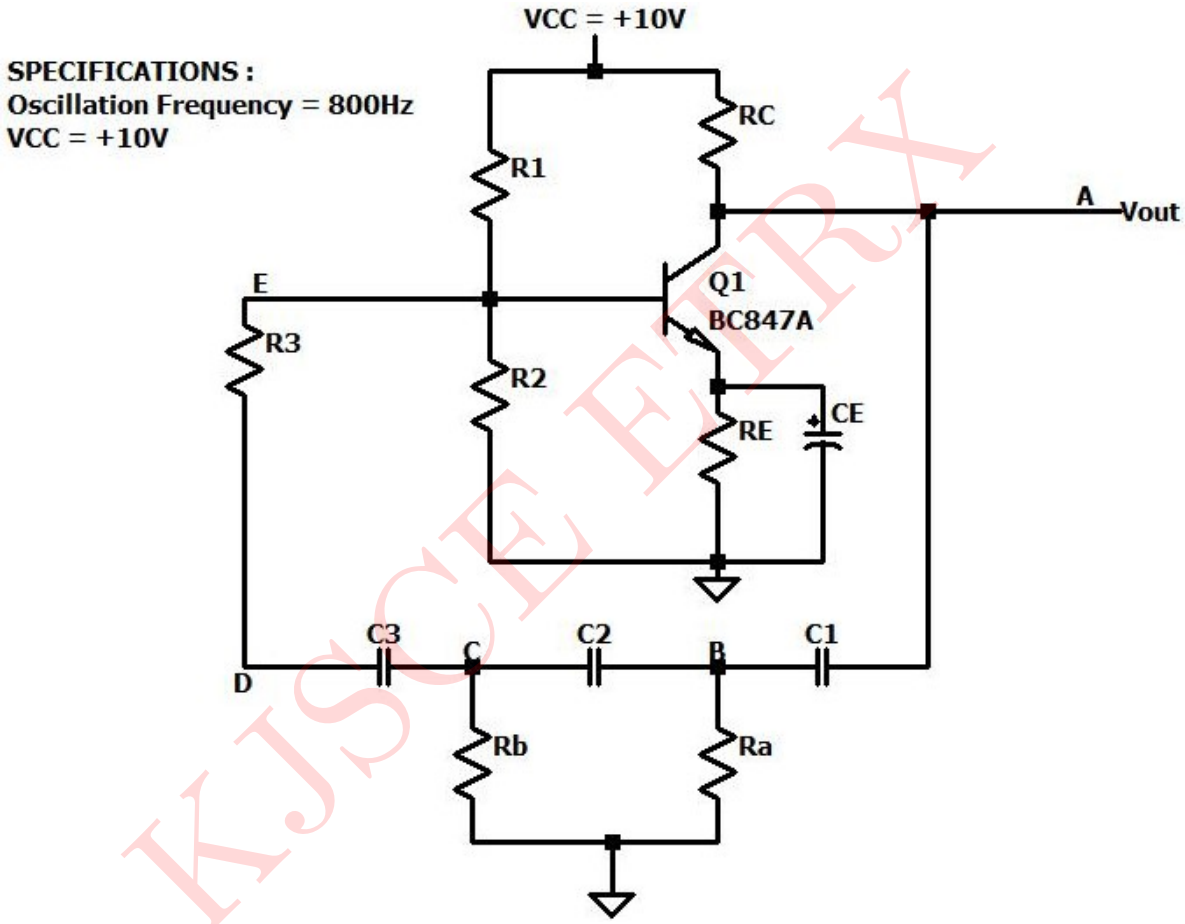

Figure 1: Circuit for Design 1

2) Selection of R and C:

For RC phase shift oscillator,

$$f = \frac{1}{2\pi RC} \times \frac{1}{\sqrt{6+4k}}$$

where $k = \dfrac{R_C}{R}$

Minimum value of k is 2.7

$$800 = \frac{1}{2\pi RC\sqrt{6+4\times 2.7}}$$

$$RC = \frac{1}{2\pi \times 800 \times 4.0987}$$

$$RC = 4.85 \times 10^{-5}$$

Let $C = 0.01\mu F$

$$R = \frac{4.85 \times 10^{-5}}{0.01 \times 10^{-6}}$$

$$R = 4.85k\Omega$$

Select $\mathbf{R_a = R_b = R = 5.1k\Omega_{(std)}, 1/4W}$.....(HSV)

3) Selection of $\mathbf{R_C}$:

$$k = \frac{R_C}{R}$$

$$R_C = k \times R = 2.7 \times 5.1k$$

$$R_C = 13.77k\Omega$$

Select $\mathbf{R_C = 15k\Omega_{(std)}, 1/4W}$.....(HSV)

4) Selection of $\mathbf{R_E}$:

$$V_{R_E} = 0.1 \times V_{CC} = 0.1 \times 10$$

$\mathbf{V_{R_E} = 1V}$ (For good stability)

For maximum symmetrical output voltage swing, select Q-Point at the center of DC load line

$$V_{CC} = 18V$$

$$V_{CEQ} = \frac{V_{CC}}{2} = \frac{10}{2}$$

$\mathbf{V_{CEQ} = 5V}$

Applying KVL to the C-E loop of BJT

$$I_{CQ} = \frac{V_{CC} - V_{CEQ} - V_{R_E}}{R_C}$$

$$I_{CQ} = \frac{10V - 5V - 1V}{15k}$$

$\mathbf{I_{CQ} = 0.266mA}$

$$I_{CQ} = \alpha \times I_{EQ} = \frac{I_{CQ}}{\alpha} \qquad \left(\alpha = \frac{\beta}{\beta+1} = \frac{180}{181} = 0.994\right)$$

$$I_{EQ} = \frac{0.266mA}{0.994}$$

$\mathbf{I_{EQ} = 0.267mA}$

$$R_E = \frac{V_{R_E}}{I_{EQ}} = \frac{1}{0.267mA}$$

$\mathbf{R_E = 3.745k\Omega}$

Select $\mathbf{R_E = 3.3\Omega_{(std)}, 1/4W}$.....(LSV)

5) Selection of R_1 and R_2:

$\beta = 180$

Assume $s = 8$

$$s = \frac{1+\beta}{1+\beta \times \left[\frac{R_E}{R_B + R_E}\right]}$$

$$s = \frac{1+180}{1+180\left[\frac{3.3k}{3.3k + R_B}\right]}$$

$\mathbf{R_B = 24.17k\Omega}$

$$R_B = R_1 \parallel R_2 = \frac{R_1 \times R_2}{R_1 + R_2} = 3.3k\Omega \quad \text{.....(1)}$$

$$V_B = V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC} \quad \text{.....(2)}$$

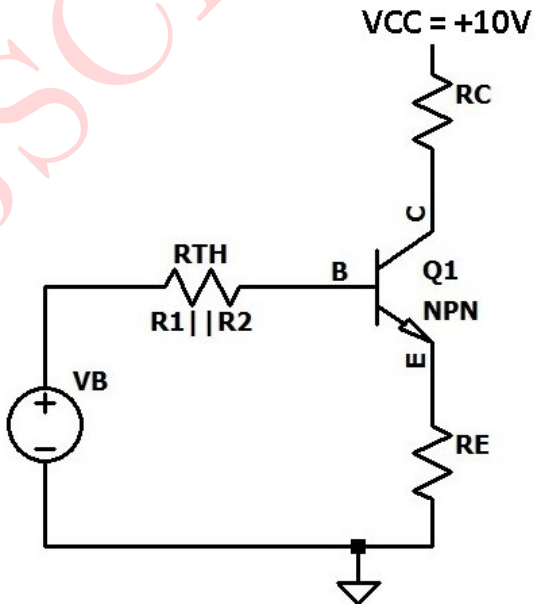

Figure 2: Thevenin's Equivalent Circuit

Applying KVL at BE loop of BJT shown in figure 2 we get,

$V_B - I_{BQ}R_B - V_{BE} - I_{EQ}R_E = 0$

$$V_B = \frac{I_C}{\beta} \times R_B + V_{BE} + I_{EQ}R_E$$

$$V_B = \frac{0.266mA}{180} \times 24.17k + 0.7 + 0.267mA \times 3.3k$$

$$\mathbf{V_B = 1.62V}$$

From (2) we get,

$$V_B = 1.62V = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$V_B = 1.62V = \frac{R_2}{R_1 + R_2} \times 10V$$

$$\frac{R_2}{R_1 + R_2} = 0.162 \qquad \text{.....(3)}$$

Substituting (3) in (1) we get,

$$R_1 \times (0.162) = 24.17k$$

$$R_1 = 149.19k\Omega$$

$$\mathbf{Select\ R_1 = 150k\Omega_{(std)}, 1/4W.....(HSV)}$$

From (3) $\frac{R_2}{R_1 + R_2} = 0.162$

$$\frac{R_2}{150k + R_2} = 0.1352$$

$$\mathbf{Select\ R_2 = 27k\Omega_{(std)}, 1/4W.....(HSV)}$$

12) <u>Selection of Bypass capacitor:</u>

$X_{CE} = 0.1R_E$ (Ensures complete bypass of R_E)

Since f_L is not given, we assume that $f_L = 20Hz$

$$C_E = \frac{1}{2\pi \times f_L \times 0.1R_E}$$

$$C_E = \frac{1}{2\pi \times 20 \times 0.1.3k}$$

$$C_E = 0.4825\mu F$$

$$\mathbf{Select\ C_E = 1\mu F/25V.....(HSV)}$$

Selection of 3^{rd} 'R' in RC section

To avoid loading effect by input impedance of BJT towards 3^{rd} 'R' in RC section; $R' = R_3 + R_i$

$R_i = R_1 \parallel R_2 \parallel r_\pi$

$R_i = 150k \parallel 27k \parallel 2.7k$

$R_i = 2.42k\Omega$

$R' = R_3 + R_i$

$R' = 5.1k + 2.42k$

$\mathbf{R' = 7.5k}$

13) Designed circuit:

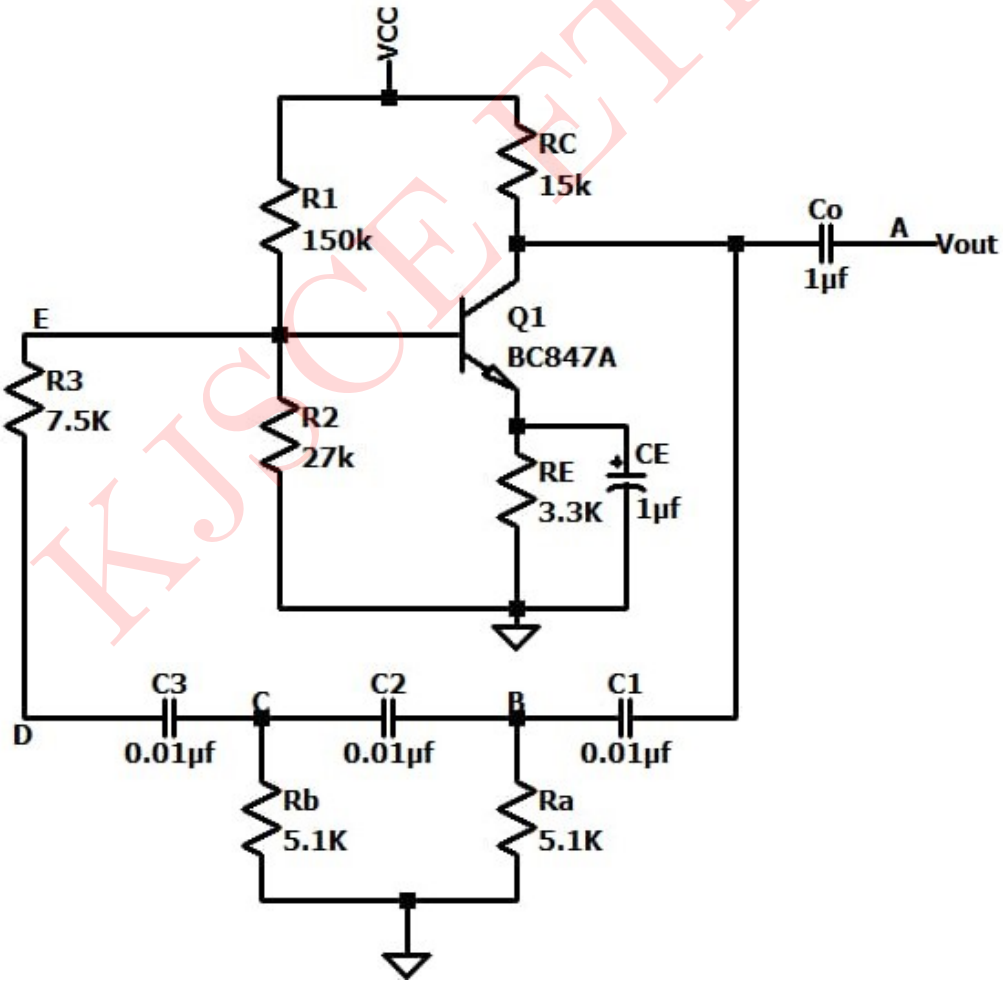

Figure 3: Designed Circuit

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

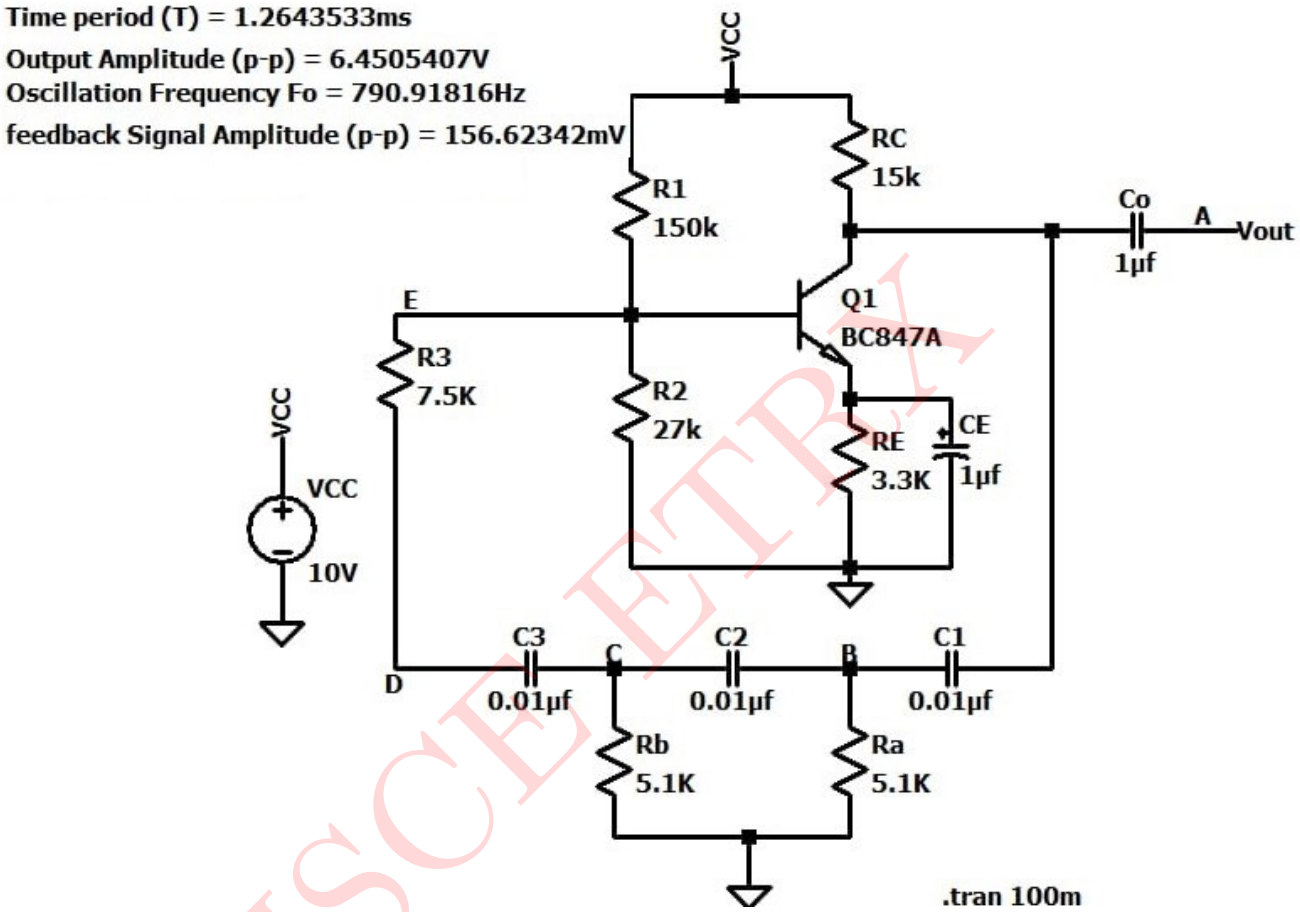

Figure 4: Circuit Schematic: Results

Output Waveforms:

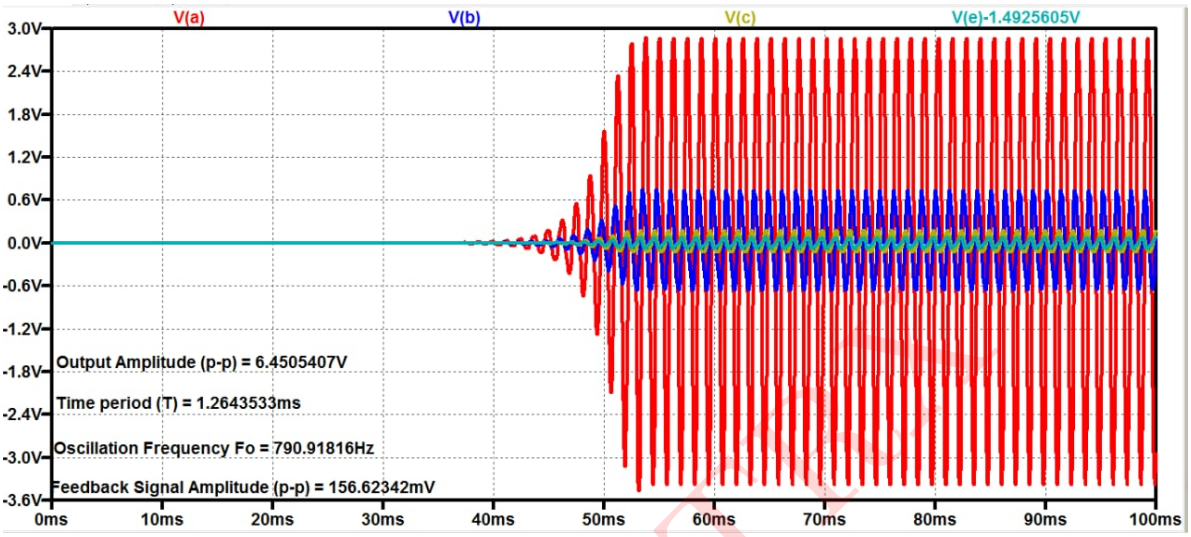

Figure 5: Output of RC phase shift oscillator

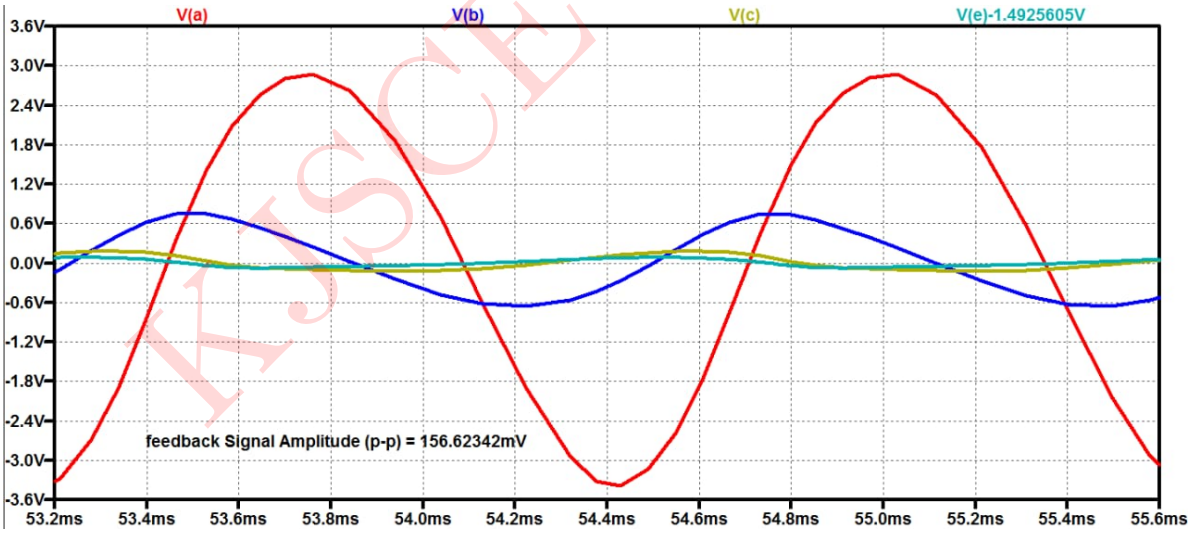

Figure 6: Output of all stages of RC phase shift oscillator

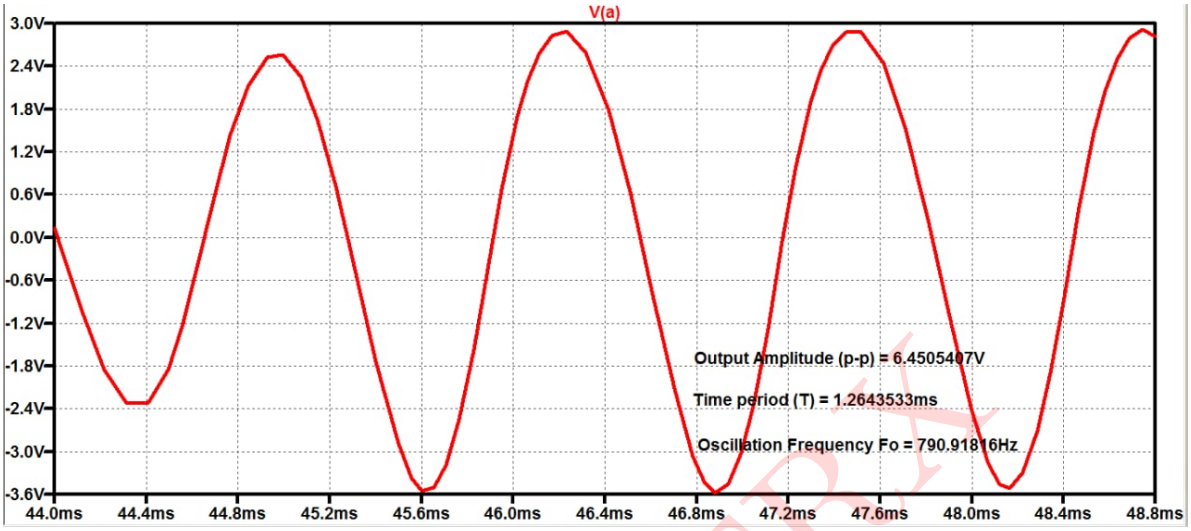

Figure 7: Output of final stage of oscillator

Comparison between theoretical and simulated values is given below:

Parameters	**Simulated Values**	**Theoretical Values**
Frequency of oscillation f_o	$790.91Hz$	$800Hz$
Time Period	$1.2643533ms$	$1.25ms$
Amplitude of output peak-peak voltage	$6.4505407V$	–
Feedback fraction	0.034	0.024
Phase shift offered by feedback network	180^o	180^o
feedback signal amplitude	$156.62mV$	–

Table 1: Design 1

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