**K. J. SOMAIYA COLLEGE OF ENGINEERING**
**DEPARTMENT OF ELECTRONICS ENGINEERING**
**ELECTRONIC CIRCUITS**
**Cascade Amplifier Design**

**Design 1:**
Design a two stage RC coupled cascade amplifier to meet the following specifications, $A_V \geq 130$, $V_{ORMS} = 3V$, $R_i \geq 1M\Omega$. Select a suitable transistor from data-sheet.

**Solution:**
Step 1: For above requirements, we can use CS-CS self bias JFET amplifier

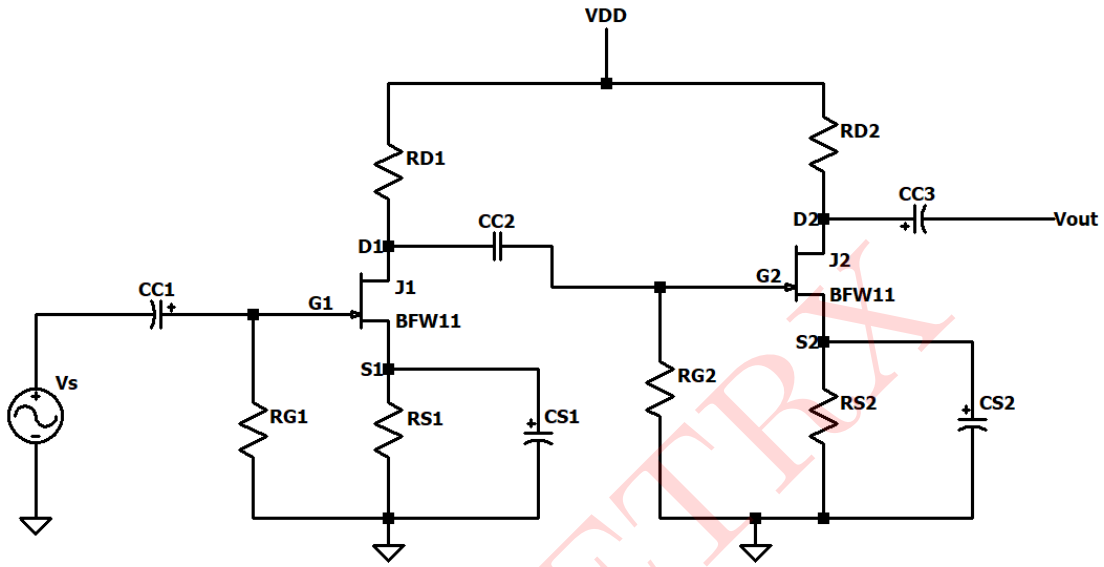


Figure 1: Circuit 1

JFET BFW-11 parameters
$I_{DSS} = 7mA$, $V_P = -2.5V$
$r_d = 50k\Omega$, $g_{m_o} = 5600\mu\mho$

Step 2: Selection of voltage gain:
$A_V \geq 130$
Let $A_V = 140$
Also, let $A_{V_1} = 0.6A_{V_2}$
$\because A_V = A_{V_1}A_{V_2}$
$\therefore 140 = 0.6{A_{V_2}}^2$
$A_{V_2} = \mathbf{15.275}$
$\because A_{V_1} = 0.6A_V$
$= 0.6 \times 15.275 = \mathbf{9.165}$
$\therefore$ Voltage gain of 2nd stage($A_{V_2}$)$\approx \mathbf{16}$
$\therefore$ Voltage gain of 1st stage($A_{V_2}$)$\approx \mathbf{9}$

Design of 2nd stage:

Step 3: Calculation of Q-point($V_{GSQ_2}$, $I_{DQ_2}$)

a) Zero-temperature drift

$|V_P| - |V_{GS}| = 0.63$

$2.5 - |V_{GS}| = 0.63$ $\quad [V_P = -2.5V$ from datasheet(BFW-11)]

$|V_{GS}| = 2.5 - 0.63$

$|V_{GS}| = 1.87V$

$V_{GS} = -1.87V$

$\therefore V_{GSQ_2} = \mathbf{-1.87V}$

In JFET,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 7mA\left[1 - \frac{(-1.87)}{(-2.5)}\right]^2 \quad [I_{DSS} = 7mA \text{ from datasheet(BFW-11)}]$$

$$I_D = 7mA\left[1 - \frac{1.87}{2.5}\right]^2$$

$$I_D = 7mA(0.252)^2$$

$$I_D = 7mA \times 0.063 = 0.4445mA$$

$\therefore I_{DQ_2} = \mathbf{0.4445mA}$

Calculation for $R_{D_2}$:

$|A_{V_2}| = g_{m_2}(r_{d_2} \parallel R_{D_2})$

$$g_m = g_{m_1} = g_{m_2} = g_{m_o}\left(1 - \frac{V_{GSQ}}{V_P}\right)$$

$$= 5600 \times 10^{-6}\left[1 - \frac{(-1.87)}{(-2.5)}\right]$$

$$= 5600 \times 10^{-6}\left[1 - \frac{1.87}{2.5}\right]$$

$$= 5600 \times 10^{-6} \times 0.252 = \mathbf{1.4112mA/V}$$

$r_d = r_{d_1} = r_{d_2} = \mathbf{50k\Omega}$

$\because |A_{V_2}| = g_{m_2}(r_{d_2} \parallel R_{D_2})$

$16 = 1.4112 \times 10^{-3}A/V(50k\Omega \parallel R_{D_2})$

$$\frac{16}{1.4112 \times 10^{-3}A/V} = \frac{R_{D_2} \times 50k\Omega}{R_{D_2} + 50k\Omega}$$

$$11337.868\Omega = \frac{R_{D_2} \times 50k\Omega}{R_{D_2} + 50k\Omega}$$

$11337.868(R_{D_2} + 50k\Omega) = R_{D_2}(50k\Omega)$

$11337.868R_{D_2} + 566893.424k\Omega = R_{D_2}(50k\Omega)$

$566893.424k\Omega = R_{D_2}(50 \times 10^3 - 11337.868)$

$566893.424k\Omega = R_{D_2}(38662.132)$

$$R_{D_2} = \frac{566893.424k\Omega}{38662.132\Omega} = \mathbf{14.662k\Omega}$$

$\because$We have to select higher standard value(H.S.V) for $R_{D_2}$,

Select $R_{D_2} = \mathbf{15k\Omega_{(std)}}$, $\mathbf{1/4W}$

Step 5: Calculation of $R_{S_2}$:

$\because V_{GSQ_2} = -I_{DQ_2}R_{S_2}$

$\therefore -1.87V = -0.4445 \times 10^{-3} \times R_{S_2}$

$$\therefore R_{S_2} = \frac{-1.87V}{-0.4445 \times 10^{-3}A} = \mathbf{4.2k\Omega}$$

$\because$ We have to select lower standard value(L.S.V) for $R_{S_2}$,

Select $R_{S_2} = \mathbf{3.9k\Omega_{(std)}}$, $\mathbf{1/4W}$

Step 6: Calculation of $R_{G_2}$:

Let, $R_{G_2} = 1.2M\Omega$, 1/4W

We select $R_{G_2} = \mathbf{11.2M\Omega}$, $\mathbf{1/4W}$ to prevent loading for first stage

Step 7: Calculation of $V_{DD}$:

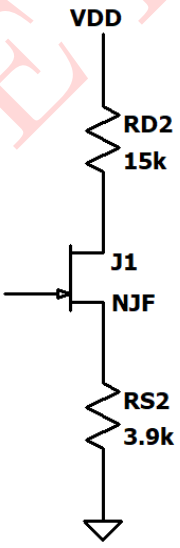


Figure 2: D-S loop for JFET

Applying KVL to drain-source loop for JFET 2,

$V_{DD} - I_{DQ_2}R_{D_2} - V_{DSQ_2} - I_{DQ_2}R_{S_2} = 0$

$\therefore V_{DD} = I_{DQ_2}(R_{D_2} + R_{S_2}) + V_{DSQ_2}$

We know,

$V_{DSQ_2} \geq 1.5\ [\ |V_P| + V_{o_{peak}}]$

The value is multiplied by 1.5 to take care of saturation voltages,
variation in resistance, variation in supply voltage and device parameter variation

$V_{DSQ_2} \geq 1.5\ [\ |V_P| + V_{o_{peak}}]$

$V_{DSQ_2} \geq 1.5\ [\ 2.5V + \sqrt{2}V_{ORMS}]$

$V_{DSQ_2} \geq 1.5\ [\ 2.5V + \sqrt{2} \times 3V]$

$V_{DSQ_2} \geq 1.5\ [\ 2.5V + 4.24V]$

$V_{DSQ_2} \geq 1.5\ [\ 6.74V]$

$V_{DSQ_2} \geq \mathbf{10.11V}$

Let $V_{DSQ_2} \approx 10.2V$

$\because V_{DD} = I_{DQ_2}(R_{D_2} + R_{S_2}) + V_{DSQ_2}$

$= 0.4445 \times 10^{-3}(15k\Omega + 3.9k\Omega) + 10.2V$

$= 0.4445 \times 10^{-3}(18.9k\Omega) + 10.2V$

$= 0.4445 \times 10^{-3}(18.9 \times 10^{-3}\Omega) + 10.2V = \mathbf{18.6V}$

Select $V_{DD} = \mathbf{20V}$

Design of 1st stage:

Step 8: Selection of $R_{D_1}$:

$|A_{V_1}| = g_{m_1}(r_{d_2} \parallel R_{D_1} \parallel R_{G_2})$

i.e $|A_{V_1}| = g_{m_1}(r_{d_2} \parallel R_{G_2} \parallel R_{D_1})$

$\therefore 9 = 1.4112mA/V(50k\Omega \parallel 1.2M\Omega \parallel R_{D_1})$

$9 = 1.4112mA/V\left(\dfrac{50k\Omega \times 1.2M\Omega}{50k\Omega + 1.2M\Omega} \parallel R_{D_1}\right)$

$9 = 1.4112mA/V\ (48k\Omega \parallel R_{D_1})$

$\dfrac{9}{1.4112mA/V} = 48k\Omega \parallel R_{D_1}$

$6.378k\Omega(48k\Omega + R_{D_1}) = (48k\Omega)(R_{D_1})$

$306.144k\Omega + (6.378k\Omega)(R_{D_1}) = (48k\Omega)(R_{D_1})$

$306.144k\Omega = R_{D_1}(48k\Omega - 6.378k\Omega)$

$306.144k\Omega = R_{D_1}(41.622k\Omega)$

$R_{D_1} = \dfrac{306.144k\Omega}{41.622k\Omega} = 7.355k\Omega$

$\because$We have to select higher standard value(H.S.V) for $R_{D_1}$,

Select $R_{D_1} = \mathbf{7.5k\Omega_{(std)}}$, $\mathbf{1/4W}$

Step 9: Selection of $R_{G_1}$:

To avoid loading effect and fulfill the requirement of $R_i \geq 1M\Omega$

Select $R_{G_1} = \mathbf{1.5M\Omega_{(std)}}$, $\mathbf{1/4W}$

Step 10: Selection of $R_{S_1}$:

$\because V_{GSQ_1} = V_{GSQ_2}$

$\therefore V_{GSQ_1} = \mathbf{-1.87V}$

$\because V_{GSQ_1} = -I_{DQ}R_{S_1}$

$\therefore -1.87V = -0.4445 \times 10^{-3}A \times R_{S_1}$

$$R_{S_1} = \frac{-1.87V}{-0.4445 \times 10^{-3}A} = \mathbf{4.206k\Omega}$$

$\because$We have to select lower standard value(L.S.V) for $R_{S_1}$,

Select $R_{S_1} = \mathbf{3.9k\Omega}$, $\mathbf{1/4W}$

Step 11: Selection of coupling capacitors($C_{C_1}$, $C_{C_2}$, $C_{C_3}$):

a) $C_{C_1}$:

$$C_{C_1} = \frac{1}{2\pi R_{eq} f_L}$$

$R_{eq} = R_{G_1} = 1.5M\Omega$

$f_L = 20Hz$ (Since $f_L$ is not given, weassume audio frequency, $f_L$=20Hz)

$$C_{C_1} = \frac{1}{2\pi \times 1.5M\Omega \times 20Hz} = \mathbf{5.30 \times 10^{-9}F}$$

We have to select higher standard value(H.S.V) for $C_{C_1}$,

Select $C_{C_1} = \mathbf{5.6nF/50V}$

b) $C_{C_2}$:

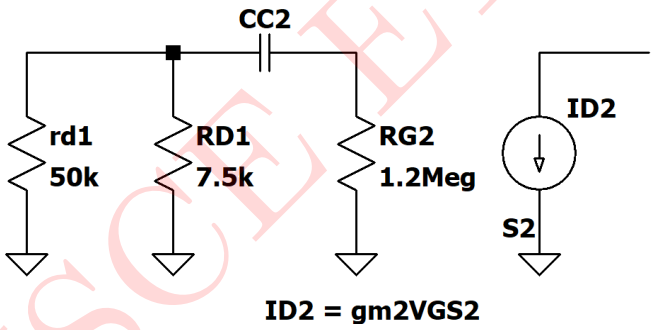


Figure 3: Low frequency equivalent circuit for $C_{C_2}$

$$C_{C_2} = \frac{1}{2\pi R_{eq} f_L}$$

$$\begin{aligned} R_{eq} &= (r_{d_1} \parallel R_{D_1}) + R_{G_2} \\ &= (50k\Omega \parallel 7.5k\Omega) + R_{G_2} \\ &= \left(\frac{50k\Omega \times 7.5k\Omega}{50k\Omega + 7.5k\Omega}\right) + 1.2M\Omega \\ &= 6.52k\Omega + 1.2M\Omega = \mathbf{1.206M\Omega} \end{aligned}$$

$$C_{C_2} = \frac{1}{2\pi \times 1.206M\Omega \times 20Hz} = \mathbf{6.601 \times 10^{-9}F}$$

We have to select higher standard value(H.S.V) for $C_{C_2}$,

Select $C_{C_2} = \mathbf{6.8nF/50V}$

c) $C_{C_3}$:

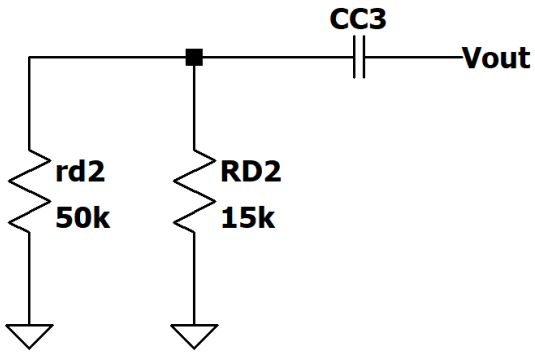


Figure 4: Low frequency equivalent circuit for $C_{C_3}$

$$C_{C_3} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = r_{d_2} \parallel R_{D_2}$$

$$= 50k\Omega \parallel 15k\Omega$$

$$= \frac{50k\Omega \times 15k\Omega}{50k\Omega + 15k\Omega} = \mathbf{11.538k\Omega}$$

$$C_{C_3} = \frac{1}{2\pi \times 11.538k\Omega \times 20Hz} = \mathbf{0.690\mu F}$$

$\because$We have to select higher standard value(H.S.V) for $C_{C_3}$,

Select, $C_{C_3} = \mathbf{1\mu F/50V}$

Step 12: Selection of bypass capacitors($C_{S_1}$, $C_{S_2}$):

Since $g_{m_1} = g_{m_2} = g_m = 1.4112mA/V$ and $R_{S_1} = R_{S_2} = 3.9k\Omega$

$$\therefore C_{S_1} = C_{S_2} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = \frac{1}{g_m} \parallel R_S$$

$$= \frac{1}{1.4112mA/V} \parallel 3.9k\Omega$$

$$= 708.8\Omega \parallel 3.9k\Omega$$

$$= \frac{708.8\Omega \times 3.9k\Omega}{708.8\Omega + 3.9k\Omega} = \mathbf{599.72\Omega}$$

$$\therefore C_{S_1} = C_{S_2} = \frac{1}{2\pi \times 599.72\Omega \times 20Hz} = \mathbf{13.27\mu F}$$

$\because$We have to select higher standard value(H.S.V) for $C_{S_1}$ and $C_{S_2}$,

Select, $C_{S_1} = C_{S_2} = \mathbf{15\mu F/50V}$

Step 13: Complete Designed Circuit:

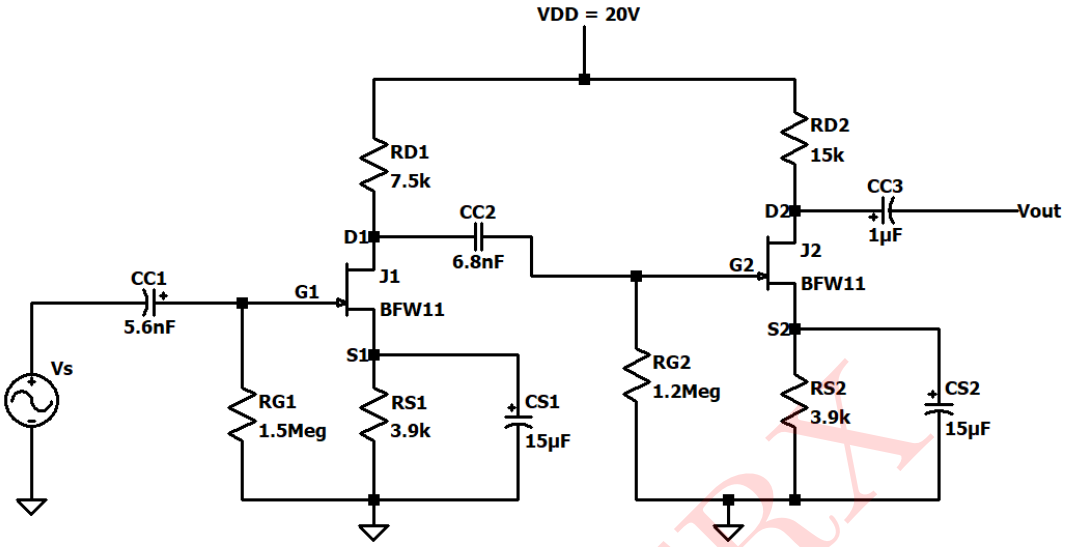


Figure 5: Complete Designed Circuit

Mid-frequency AC equivalent circuit:

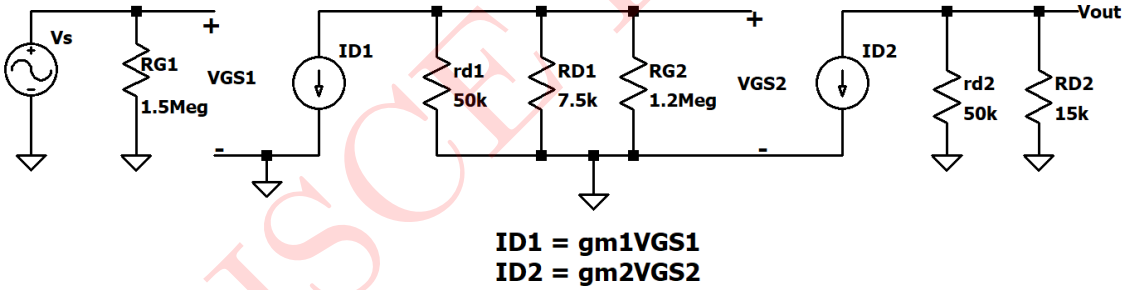


Figure 6: Mid-frequency AC equivalent circuit

Input impedance,

$Z_i = R_{G_1} = \mathbf{1.5M\Omega}$

Output impedance,

$Z_o = r_{d_2} \parallel R_{D_2}$

$= 50k\Omega \parallel 15k\Omega$

$= \dfrac{50k\Omega \times 15k\Omega}{50k\Omega + 15k\Omega} = \mathbf{11.53k\Omega}$

$$
\begin{aligned}
|A_{V_1}| &= g_m(r_d \parallel R_D \parallel R_{G_2}) \\
&= 1.4112mA/V(50k\Omega \parallel 7.5k\Omega \parallel 1.2M\Omega) \\
&= 1.4112mA/V\left(\frac{50k\Omega \times 7.5k\Omega}{50k\Omega + 7.5k\Omega} \parallel 1.2M\Omega\right) \\
&= 1.4112mA/V(6.52k\Omega \parallel 1.2M\Omega) \\
&= 1.4112mA/V\left(\frac{6.52k\Omega \times 1.2M\Omega}{6.52k\Omega + 1.2M\Omega}\right) \\
&= 1.4112mA/V \times 6.484k\Omega = \mathbf{9.15}
\end{aligned}
$$

$$
\begin{aligned}
|A_{V_2}| &= g_m(r_d \parallel R_{D_2}) \\
&= 1.4112mA/V(50k\Omega \parallel 15k\Omega) \\
&= 1.4112mA/V\left(\frac{50k\Omega \times 15k\Omega}{50k\Omega + 15k\Omega}\right) \\
&= 1.4112mA/V \times 11.53k\Omega = \mathbf{16.28}
\end{aligned}
$$

$$
\begin{aligned}
A_V &= A_{V_1} A_{V_2} \\
&= 9.15 \times 16.28 = \mathbf{148.99}
\end{aligned}
$$

$\therefore$ Achieved gain $A_V$ is 148.99 and designed gain is greater than 130

**SIMULATED RESULTS:**

Above circuit is simulated in LTspice and results are as follows:

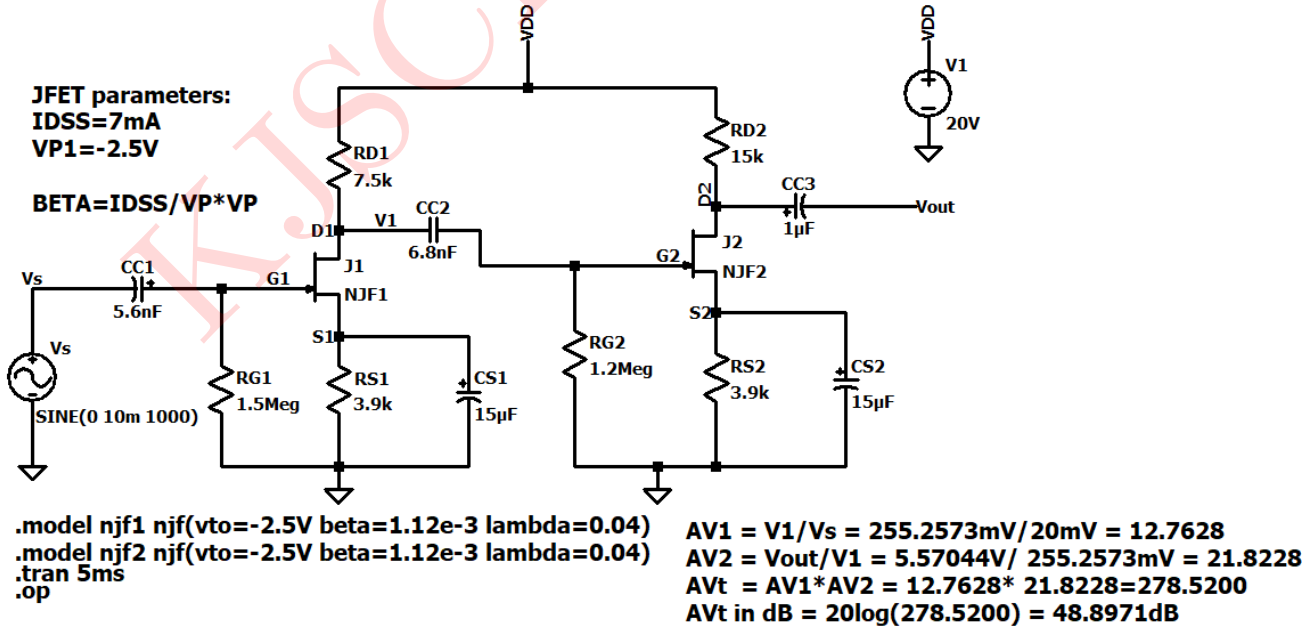


Figure 7: Circuit Schematic

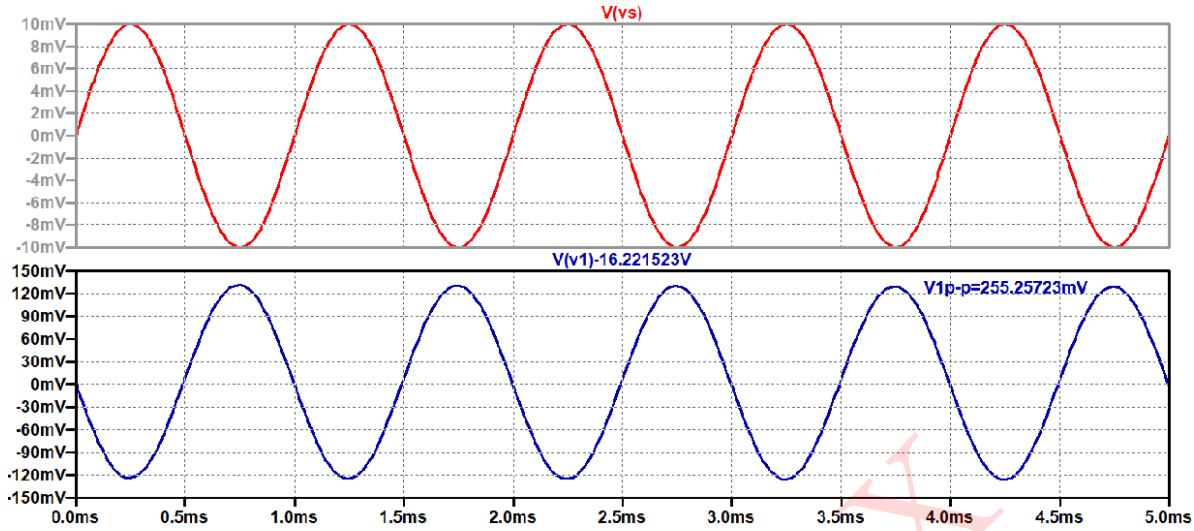


Figure 8: Input and ouput waveforms for Stage 1 current gain

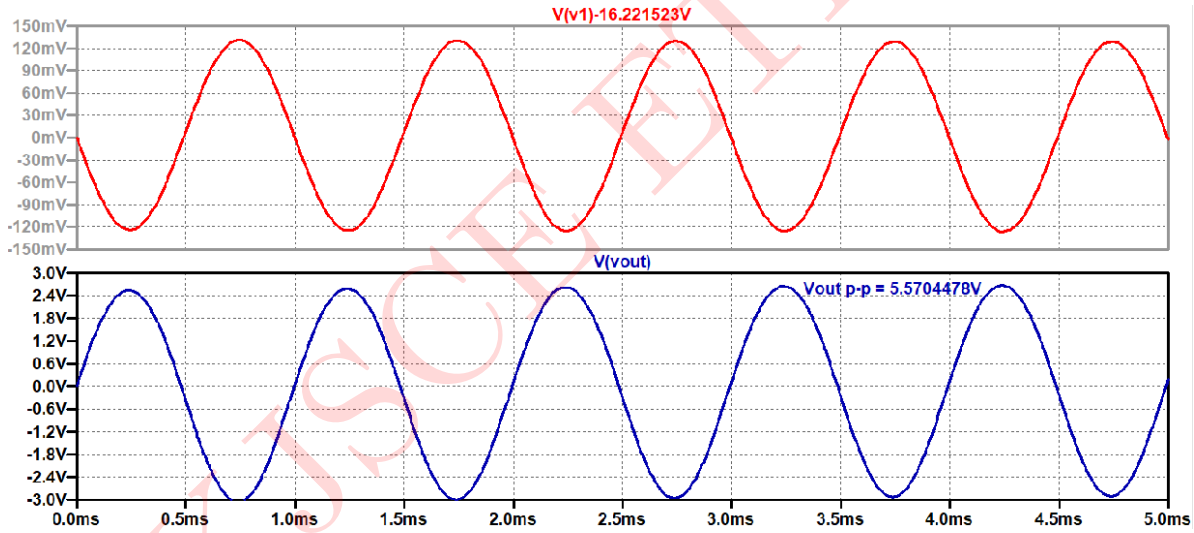


Figure 9: Input and ouput waveforms for Stage 2 current gain

**Comparison between theoretical and simulated values:**

| Parameters | Theoretical values | Simulated values |
|---|---|---|
| 1st stage DC parameters: $I_{DQ_1}$, $V_{GSQ_1}$ | 0.4445mA, −1.87V | 0.5037mA, −1.9412V |
| 2nd stage DC parameters: $I_{DQ_2}$, $V_{GSQ_2}$ | 0.4445mA, −1.87V | 0.5037mA, −1.9412V |
| Voltage gain of 1st stage $A_{V_1}$ | >9 | 12.7682 |
| Voltage gain of 2nd stage $A_{V_2}$ | >16 | 21.8228 |
| Overall voltage gain $A_{V_T}$ in dB | >42.27dB | 48.8971dB |
| Input impedance of 1st stage | 1.5MΩ | – |
| Output impedance of 2nd stage | 11.53kΩ | – |

Table 1: Design 1

**Design 2:**
Design a two stage RC coupled cascade amplifier for following specifications,
$A_V \geq 600$, $V_{CC} = 20V$, $S \leq 10$, $R_i \geq 1M\Omega$. Select a suitable transistor from data-sheet.

**Solution:**
Above requirements can be fulfilled by CS-CE stage.
We select CS as 1st stage since $R_i \geq 1M\Omega$
Step 1: Circuit diagram and selection of transistor

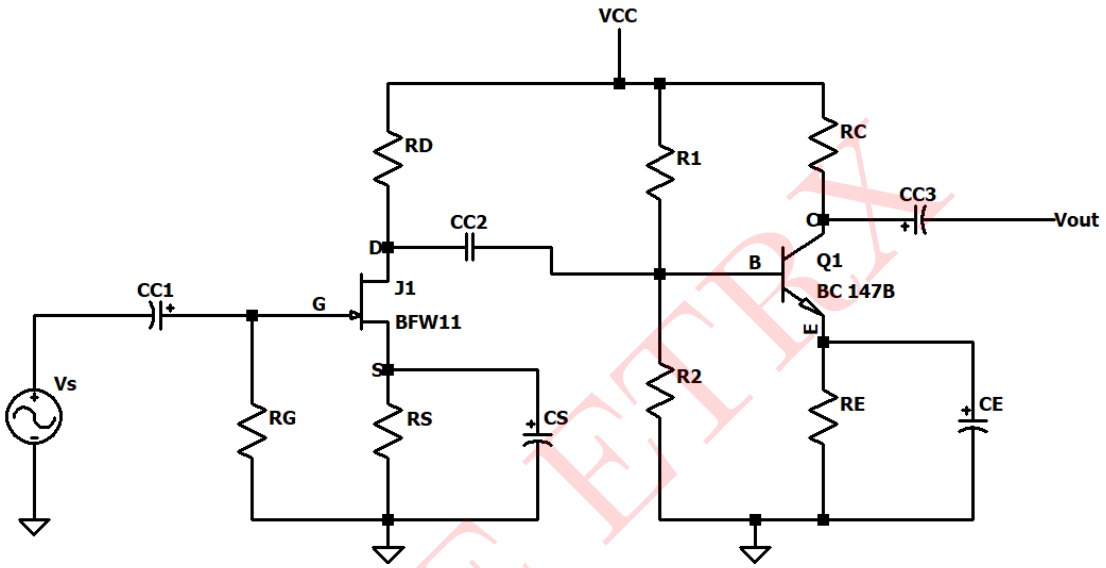


Figure 10: Circuit 2

Select BC 147B: hfc(typ) = 330; $h_{FE}$(typ) = 290 = $\beta$; hie = 4.5kΩ; $V_{CE}$(sat) = 0.25V
We select BC 147B because its hfc(typ) and hie is higher
Select BFW11: $I_{DSS} = 7mA$; $g_{m_o} = 5600\mu\mho$; $V_P = -2.5V$; $r_d = 50k\Omega$

Step 2: Selection of gains:
$A_V \geq 600$
Let $A_{V_1} = 4$ (Since gain of JFET amplifier is less)
$\because A_V = A_{V_1} A_{V_2}$
$\therefore 600 = 4A_{V_2}$
$A_{V_2} =$ **150**
$\therefore$ Voltage gain of 2nd stage($A_{V_2}$)= **150**
$\therefore$ Voltage gain of 1st stage($A_{V_1}$)= **4**

Design of 2nd stage:

Step 3: Selection of $R_C$:

$$|A_{V_2} = \frac{hfe(typ)R_C}{hie}$$

$$150 = \frac{330 \times R_C}{4.5k\Omega}$$

$$R_C = \frac{650k\Omega}{330} = \mathbf{2.04k\Omega}$$

$\therefore$We have to select higher standard value(H.S.V) for $R_C$,

Select $R_C = \mathbf{2.2k\Omega}$, $\mathbf{1/4W}$

Step 4: Selection of Q-point($V_{CEQ}, I_{CQ}$):

$V_{CC} = 20V$

Let $V_{CEQ} = \frac{V_{CC}}{2} = 10V$

$V_{RE} = 0.1V_{CC}$

$= 0.1 \times 20 = \mathbf{2V}$

Applying KVL to collector-emitter loop of BJT,

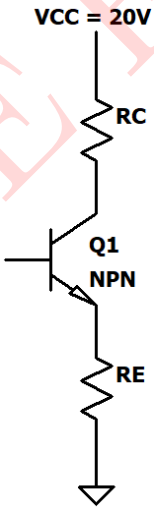


Figure 11: C-E output loop fot BJT

$$V_{CC} - V_{RC} - V_{CEQ} - V_{RE} = 0$$

$$\therefore V_{RC} = V_{CC} - V_{CEQ} - V_{RE}$$

$$\therefore V_{RC} = 20 - 10 - 2 = \mathbf{8V}$$

$$\because V_{RC} = I_{CQ}R_C$$

$$8V = I_{CQ}(2.2k\Omega)$$

$$I_B = \frac{I_{CQ}}{\beta}$$

$$I_B = \frac{3.6363mA}{290} = \mathbf{12.5389\mu A}$$

$$I_E = (\beta + 1)I_B$$
$$= (290 + 1)(12.53\mu A)$$
$$= (291)(12.53\mu A) = \mathbf{3.6462mA}$$

Step 5: Calculation of $R_E$:

$\because V_{RE} = 2V$

$\therefore V_{RE} = I_{EQ}R_E$

$2V = 3.6462mA \times R_E$

$$\therefore R_E = \frac{2V}{3.6462mA} = \mathbf{548.51\Omega}$$

$\because$ We have to select lower standard value(L.S.V) for $R_E$,

Select $R_E = \mathbf{510\Omega}$, $\mathbf{1/4W}$

Step 6: Selection of biasing resistors($R_1, R_2$):

$S \leq 10$

Let S = 9

$$S = \frac{1 + 290}{1 + 290\left[\frac{R_E}{R_E + R_B}\right]}$$

$$9 = \frac{1 + 290}{1 + 290\left[\frac{510\Omega}{510\Omega + R_B}\right]}$$

$$9 = \frac{291}{\frac{510 + R_B + 147900}{510 + R_B}}$$

$$\frac{9}{510 + R_B} = \frac{291}{R_B + 148410}$$

$9(R_B + 148410) = 291(510 + R_B)$

$9R_B + 1335690 = 148410 + 291R_B$

$1187280 = R_B(282)$

$$R_B = \frac{118728}{282} = \mathbf{4.210k\Omega}$$

$R_B = R_1 \parallel R_2$

$R_1 \parallel R_2 = 4.210k\Omega$

$$\frac{R_1 \times R_2}{R_1 + R_2} = 4.210k\Omega \qquad ....(1)$$

$$V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC} \qquad ....(2)$$

Applying KVL to base-emitter loop of BJT,

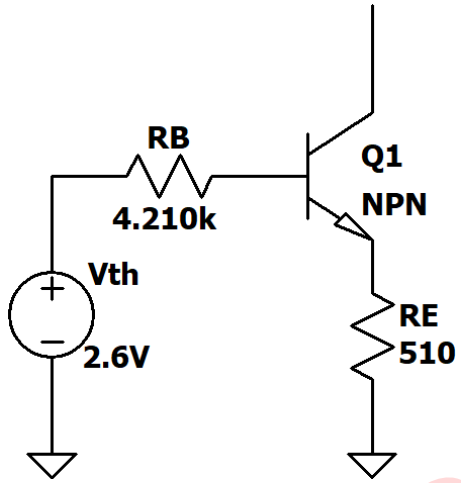


Figure 12: Thevenin's equivalent circuit for BJT

$V_{th} - I_{BQ}R_B - V_{BE} - I_{EQ}R_E = 0$

$\therefore V_{th} = \frac{I_{CQ}}{\beta}R_B + V_{BE} + I_{EQ}R_E \qquad (\because I_{CQ} = \beta I_{BQ}, I_{CQ} \approx I_{EQ})$

$\therefore V_{th} = \frac{3.6363mA}{290} \times 4.210k\Omega + 0.7 + 3.6363mA \times 510\Omega$

$\therefore V_{th} = 0.05V + 0.7 + 1.85V = \mathbf{2.6V}$

$\because V_B = V_{th} = \mathbf{2.6V}$

$\because V_{BE} = 0.7$

$\therefore V_B - V_E = 0.7V$

$\therefore 2.6V - V_E = 0.7V$

$\therefore V_E = 2.6 - 0.7 = \mathbf{1.9V}$

From (2),

$V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC}$

$2.6V = \frac{R_2}{R_1 + R_2} \times 20V$

$\frac{R_2}{R_1 + R_2} = \frac{2.6V}{20V}$

$\frac{R_2}{R_1 + R_2} = 0.13 \qquad ....(3)$

Put (3) in (1), we get

$R_1 \times 0.13 = 4.210k\Omega$

$R_1 = \frac{4.210k\Omega}{0.13} = \mathbf{32.38k\Omega}$

$\because$We have to select higher standard value(H.S.V) for $R_1$,

Select $R_1 = \mathbf{33k\Omega}$, $\mathbf{1/4W}$

From (3),

$$\frac{R_2}{R_1+R_2}=0.13$$

$$\therefore \frac{R_2}{33k\Omega+R_2}=0.13$$

$$R_2=0.13(33k\Omega+R_2)$$

$$R_2=4.29k\Omega+0.13R_2$$

$$0.87R_2=4.29k\Omega$$

$$R_2=\frac{4.29k\Omega}{0.87}=\mathbf{4.931k\Omega}$$

$\because$We have to select higher standard value(H.S.V) for $R_2$,

Select $R_2=\mathbf{5.1k\Omega}$, $\mathbf{1/4W}$

Design of 1st stage:

Step 7: Selection of Q-point $(I_{DQ}, V_{GSQ})$:

Using mid-point biasing,

$$I_{DQ}=\frac{I_{DSS}}{2}=\frac{7mA}{2}\approx\mathbf{3.5mA}$$

$$I_{DQ}=I_{DSS}\left(1-\frac{V_{GSQ}}{V_P}\right)^2$$

$$V_{GSQ}=V_P\left(1-\sqrt{\frac{I_{DQ}}{I_{DSS}}}\right)$$

$$=-2.5\left(1-\sqrt{\frac{3.5}{7}}\right)=\mathbf{-0.732V}$$

$$\because g_{m_1}=g_{m_o}\left(1-\frac{V_{GSQ}}{V_P}\right)$$

$$=5600\times10^{-6}\left[1-\frac{(-0.732)}{(-2.5)}\right]$$

$$=5600\times10^{-6}\left[1-\frac{0.732}{2.5}\right]$$

$$=5600\times10^{-6}(0.7072)=\mathbf{3.96mA/V}$$

Step 8: Selection of $R_D$:

$$|A_{V_2}|=\frac{hfc(typ)\times R_C}{hie}$$

$$=\frac{330\times2.2k\Omega}{4.5k\Omega}=\mathbf{161.33}$$

$$|A_{V_1}|=\frac{A_V}{|A_{V_2}|}$$

$$=\frac{600}{161.33}=\mathbf{3.71}$$

Let $|A_{V_1}|=3.5$

$$|A_{V_1}|=g_{m_1}[R_D \parallel r_d \parallel R_1 \parallel R_2 \parallel hie]$$

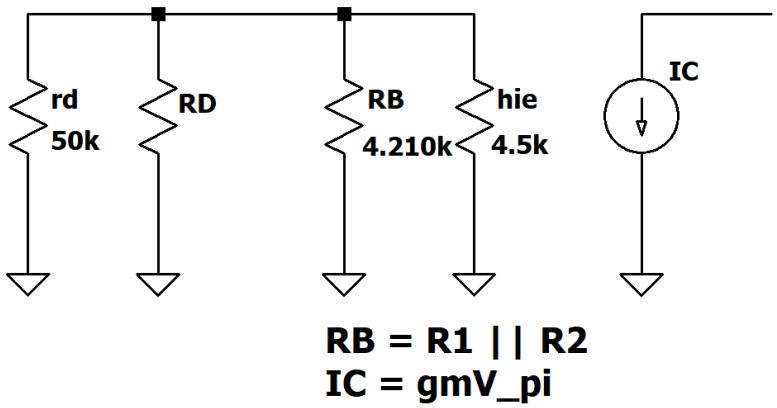


Figure 13: Small signal equivalent circuit for selection of $R_D$

$$
\begin{aligned}
R_{L_1} &= r_d \parallel R_1 \parallel R_2 \parallel hie \\
&= 50k\Omega \parallel 33k\Omega \parallel 5.1k\Omega \parallel 4.5k\Omega \\
&= \left(\frac{50k\Omega \times 33k\Omega}{50k\Omega + 33k\Omega}\right) \parallel \left(\frac{5.1k\Omega \times 4.5k\Omega}{5.1k\Omega + 4.5k\Omega}\right) \\
&= 19.87k\Omega 2.39k\Omega \\
&= \frac{19.87k \times 2.39k\Omega}{19.87k\Omega + 2.39k\Omega} = \mathbf{2.13k\Omega}
\end{aligned}
$$

$$|A_{V_1}| = g_{m_1}[R_D \parallel 2.13k\Omega]$$

$$3.5 = 3.96 \times 10^{-3} A/V \left(\frac{R_D \times 2.13k\Omega}{R_D + 2.13k\Omega}\right)$$

$$883.838 = \frac{R_D \times 2.13k\Omega}{R_D + 2.13k\Omega}$$

$$883.838(R_D + 2.13k\Omega) = R_D(2.13k\Omega)$$

$$883.838R_D + 1885.57k\Omega = R_D(2.13k\Omega)$$

$$1885.57k\Omega = R_D(2.13k\Omega - 883.838)$$

$$R_D = \frac{1885.57k\Omega}{1246.16k\Omega} = \mathbf{1.513k\Omega}$$

$\therefore$We have to select higher standard value(H.S.V) for $R_D$,

Select $R_D = \mathbf{1.8k\Omega}$, $\mathbf{1/4W}$

Step 9: Selection of $R_S$:

$\because V_{GSQ} = I_{DQ} \times R_S$

$-0.732 = -3.5mA \times R_S$

$\therefore R_S = \dfrac{-0.732V}{3.5mA} = \mathbf{209.14\Omega}$

$\therefore$We have to select lower standard value(L.S.V) for $R_S$,

Select $R_S = \mathbf{180\Omega}$, $\mathbf{1/4W}$

Step 10: Selection of $R_G$:

Let $R_G = \mathbf{1.2M\Omega}$, $\mathbf{1/4W}$

Since $R_i \geq 1M\Omega$ is required and to prevent loading we take $R_G = 1.2M\Omega$

Step 11: Selection of coupling capacitors($C_{C_1}$, $C_{C_2}$, $C_{C_3}$):

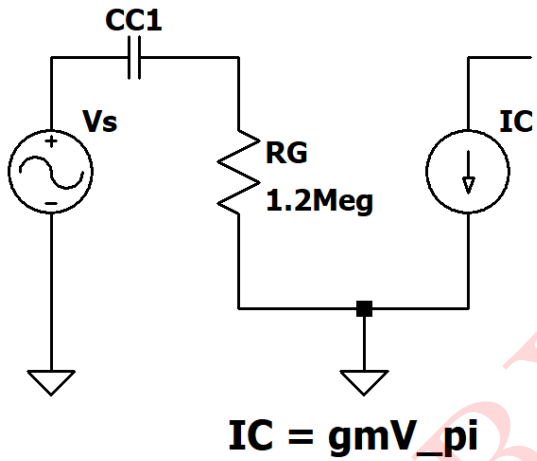


Figure 14: Low frequency equivalent circuit for $C_{C_1}$

Since $f_L$ is not given, we consider audio frequency, $f_L = 20Hz$

a) $C_{C_1}$:

$$C_{C_1} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = R_G = 1.2M\Omega$$

$$C_{C_1} = \frac{1}{2\pi \times 1.2M\Omega \times 20Hz} = \mathbf{6.63nF}$$

$\because$ We have to select higher standard value(H.S.V) for $C_{C_1}$,

Select $C_{C_1} = \mathbf{6.8nF/50V}$

b) $C_{C_2}$:

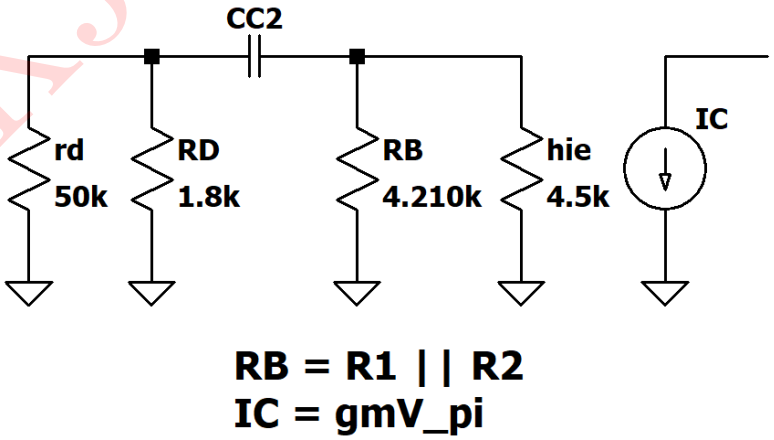


Figure 15: Low frequency equivalent circuit for $C_{C_2}$

$$C_{C_2} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = (r_d \parallel R_D) + R_1 \parallel R_2 \parallel hie$$

$$= (50k\Omega \parallel 1.8k\Omega) + 33k\Omega \parallel 5.1k\Omega \parallel 4.5k\Omega$$

$$= \left(\frac{50k\Omega \times 1.8k\Omega}{50k\Omega + 1.8k\Omega}\right) + 33k\Omega \parallel \left(\frac{5.1k\Omega \times 4.5k\Omega}{5.1k\Omega + 4.5k\Omega}\right)$$

$$= 1.73k\Omega + 33k\Omega \parallel 2.39k\Omega$$

$$= 1.73k\Omega + \frac{33k\Omega \times 2.39k\Omega}{33k\Omega + 2.39k\Omega}$$

$$= 1.73k\Omega + 2.22k\Omega = \mathbf{3.95k\Omega}$$

$$C_{C_2} = \frac{1}{2\pi \times 3.95k\Omega \times 20Hz} = \mathbf{2.015\mu F}$$

$\because$ We have to select higher standard value(H.S.V) for $C_{C_2}$,

Select $C_{C_2} = \mathbf{2.2\mu F/50V}$

c) $C_{C_3}$:

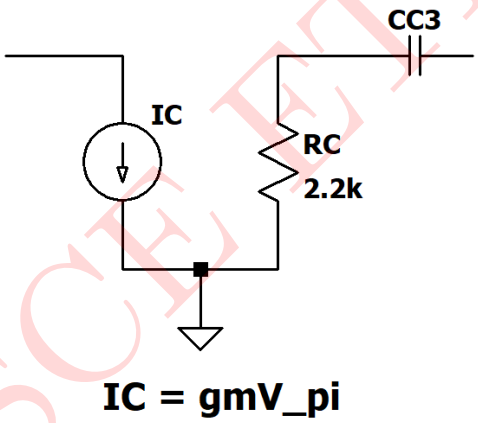


Figure 16: Low frequency equivalent circuit for $C_{C_3}$

$$C_{C_3} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = R_C = 2.2k\Omega$$

$$C_{C_3} = \frac{1}{2\pi \times 2.2k\Omega \times 20Hz} = \mathbf{3.61\mu F}$$

$\therefore$We have to select higher standard value(H.S.V) for $C_{C_3}$,

Select, $C_{C_3} = \mathbf{3.9\mu F/50V}$

Step 12: Selection of bypass capacitors:

a) $C_S$:

$$C_S = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = \frac{1}{g_m} \parallel R_S$$

$$= \frac{1}{3.96 \times 10^{-3}} \parallel 180\Omega$$

$$= 252.52\Omega \parallel 180\Omega$$

$$= \frac{252.52 \times 180}{252.52 + 180} = \mathbf{105.09\Omega}$$

$$\therefore C_S = \frac{1}{2\pi \times 105.09\Omega \times 20Hz} = \mathbf{75.72\mu F}$$

$\because$We have to select higher standard value(H.S.V) for $C_S$,

Select, $C_S = \mathbf{32\mu F/50V}$

a) $C_E$:

$X_{CE} = 0.1R_E$ (ensures complete bypass of $R_E$)

$$\frac{1}{2\pi f_L C_E} = 0.1R_E$$

$$C_E = \frac{1}{2\pi f_L \times 0.1R_E}$$

$$= \frac{1}{2\pi \times 20 \times 0.1 \times 510\Omega} = \mathbf{156.11\mu F}$$

$\because$We have to select higher standard value(H.S.V) for $C_E$,

Select, $C_E = \mathbf{180\mu F/50V}$

Step 13: Complete Designed Circuit:

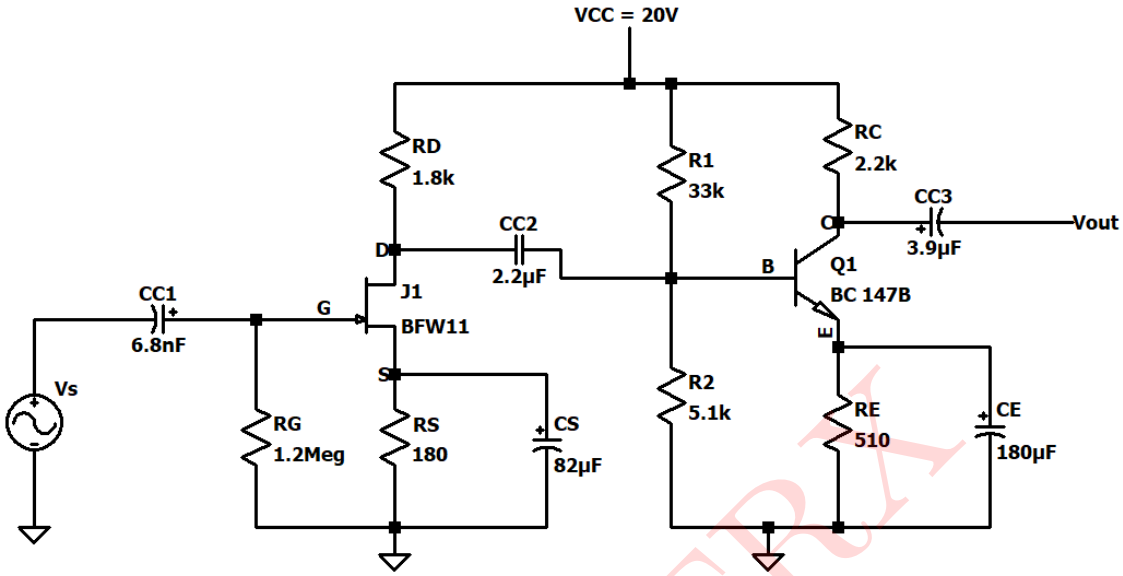


Figure 17: Complete Designed Circuit

Mid-frequency AC equivalent circuit:

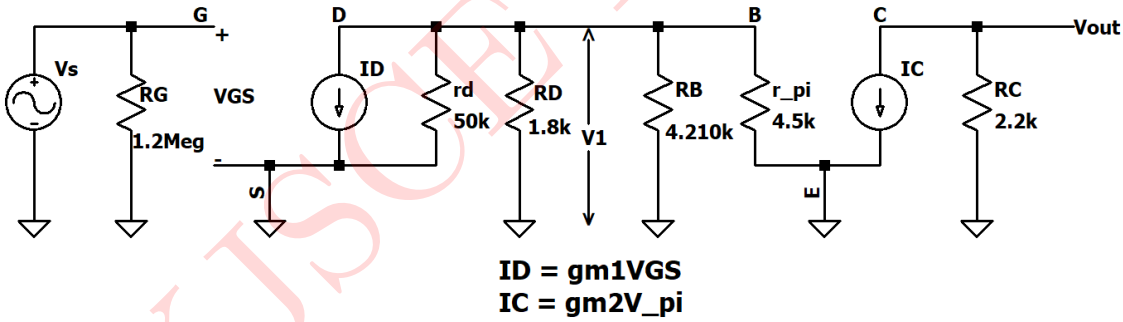


Figure 18: Mid-frequency AC equivalent circuit

Input impedance of 1st stage,

$Z_i = R_G = \mathbf{1.2M\Omega}$

Output impedance of 2nd stage,

$Z_o = R_C = \mathbf{2.2k\Omega}$

$$
\begin{aligned}
|A_{V_1}| &= g_{m_1}(r_d \parallel R_D \parallel R_B \parallel r_\pi) \\
&= 3.96mA/V(50k\Omega \parallel 1.8k\Omega \parallel 4.210k\Omega \parallel 4.5k\Omega) \\
&= 3.96mA/V \left(\frac{50k\Omega \times 7.5k\Omega}{50k\Omega + 7.5k\Omega} \parallel \frac{4.210k\Omega \times 4.5k\Omega}{4.210k\Omega + 4.5k\Omega}\right) \\
&= 3.96mA/V(1.73k\Omega \parallel 2.17k\Omega) \\
&= 3.96mA/V \left(\frac{1.73k\Omega \times 2.17k\Omega}{1.73k\Omega + 2.17k\Omega}\right) \\
&= 1.4112mA/V \times 0.96k\Omega = \mathbf{3.811}
\end{aligned}
$$

$|A_{V_2}| = g_{m_2}(R_C)$

$= 1.39.85mA/V(2.2k\Omega) = \mathbf{307.686}$

$A_{V_t} = A_{V_1} A_{V_2}$

$= 3.811 \times 307.686 = \mathbf{1172.594}$

$\therefore$ Achieved gain $A_{V_t}$ is 148.99 and designed gain is greater than 600

**SIMULATED RESULTS:**

Above circuit is simulated in LTspice and results are as follows:

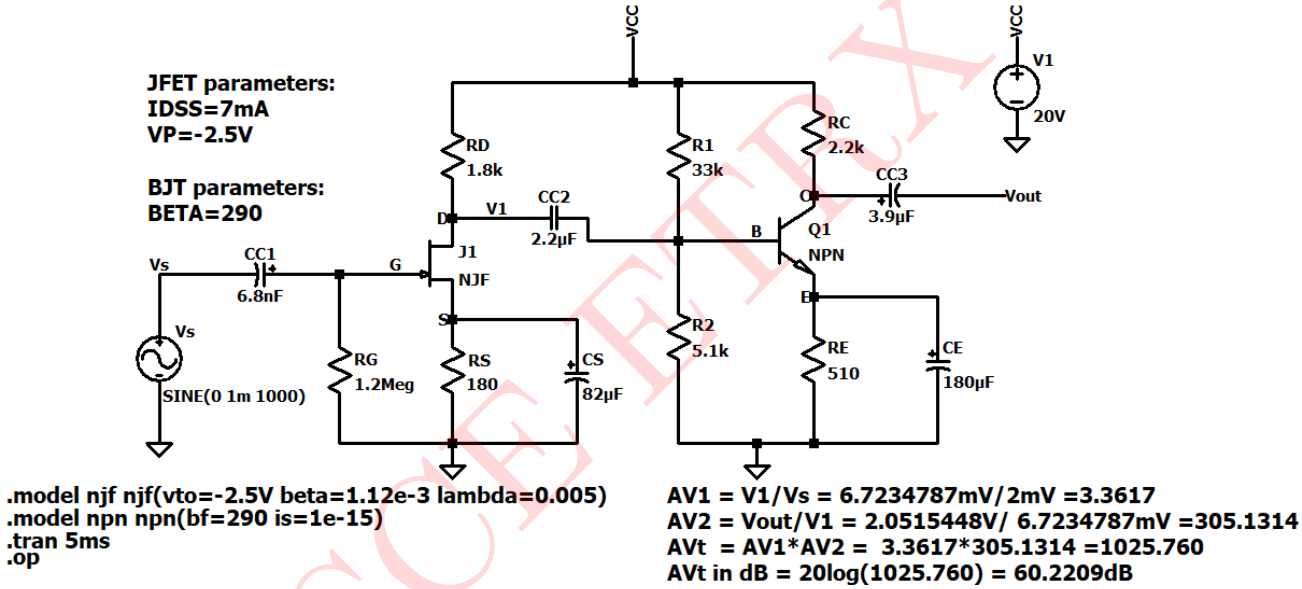


Figure 19: Circuit Schematic

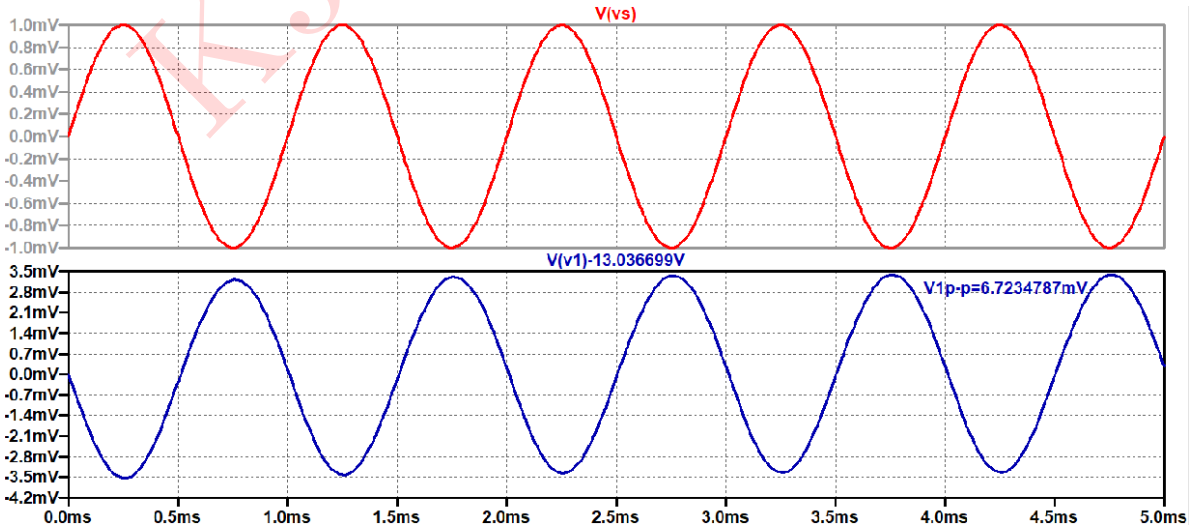


Figure 20: Input and ouput waveforms for Stage 1 voltage gain

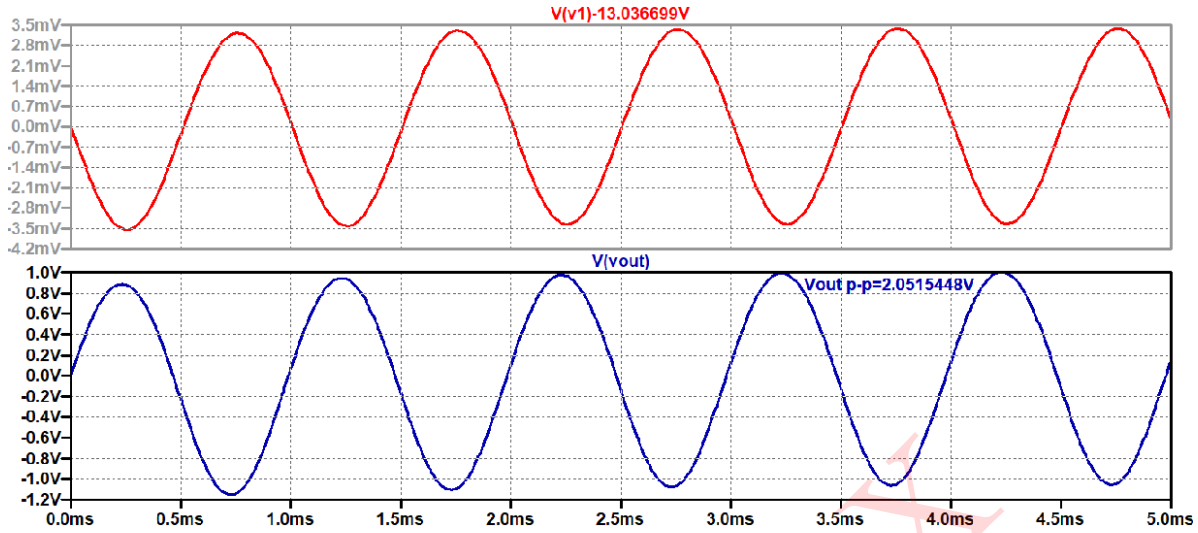


Figure 21: Input and ouput waveforms for Stage 2 voltage gain

**Comparison between theoretical and simulated values:**

| Parameters | Theoretical values | Simulated values |
|---|---|---|
| 1st stage DC parameters: $I_{DQ}$, $V_{GSQ}$ | 3.5mA, $-0.732$V | 3.8685mA, $-0.69633$V |
| 2nd stage DC parameters: $I_B$, $I_C$, $I_E$, $V_E$, $V_B$ | 12.5389$\mu$A, 3.6363mA, 3.6462mA, 1.9V, 2.6V | 12.6216$\mu$A, 3.6602mA, 3.6728mA, 1.8731V, 2.6214V |
| Voltage gain of 1st stage $\lvert A_{V_1}\rvert$ | 3.5 | 3.3617 |
| Voltage gain of 2nd stage $\lvert A_{V_2}\rvert$ | 161.33 | 305.1314 |
| Overall voltage gain $A_{V_T}$ in dB | 55.56dB | 60.220dB |
| Input impedance of 1st stage | 1.2M$\Omega$ | – |
| Output impedance of 2nd stage | 2.2k$\Omega$ | – |

Table 2: Design 2

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