K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Cascade Amplifier Design

16^{th} **July, 2020**

Design 1: Design a two stage RC coupled cascade amplifier for following specifications $A_V \geq 1750$, $V_{ORMS} = 2V$, $S \leq 10$, $f_L \geq 30Hz$. Use transistor BC 147A from the data sheet.

Solution:

1) Circuit diagram selection and selection of transistor:

Given: $A_V \geq 1750$, $V_{ORMS} = 2V$, $S \leq 10$, $f_L \geq 30Hz$
Transistor BC 147A specification:
$h_{fe(typ)} = 220$, $h_{ie} = 2.7k\Omega$
$h_{FE(typ)} = 180$, $V_{CE(sat)} = 0.25V$
We use voltage divider biasing because it provides stability of Q point against variations in β or stability of Q point against variations in temperature

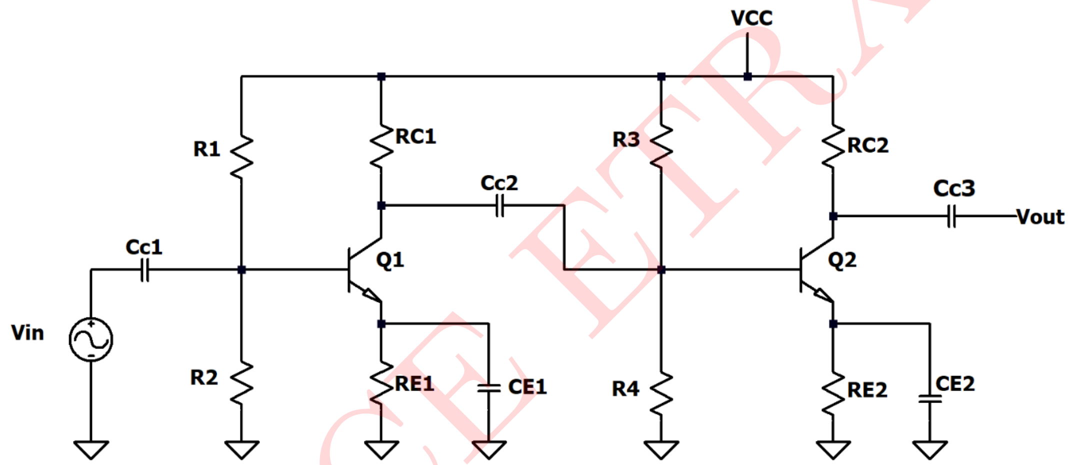

Figure 1: Circuit 1

2. Selection of voltage gains:

$$A_{VT} = A_{V1} \times A_{V2} = 1750$$

$$A_{V1} \approx 0.5A_{V2}$$

$$\therefore A_{VT} = 0.5A_{V2}^2$$

$$1750 = 0.5A_{V2}^2$$

$$A_{V2} = \sqrt{\frac{1750}{0.5}} = \mathbf{59.16}$$

$$A_{V1} = 0.5 \times 59.16 = \mathbf{29.58}$$

Let $A_{V1} = 30$ and $A_{V2} = 59$

Design of second stage:

3. Calculations of R_{C2}:

$$|A_{V2}| = \frac{h_{fe(typ)} R_{C2}}{h_{ie}} = \frac{220 \times R_{C2}}{2.7 \times 10^3} = \mathbf{59}$$

$$\therefore R_{C2} \frac{2.7 \times 10^3 \times 59}{220} = \mathbf{724\Omega}$$

Selecting HSV, $R_{C2} = \mathbf{750\Omega, 1/4W}$

4. Selection of Q point (V_{CEQ2}, I_{CQ2})

Since V_{CC} is not given to us, we take;

$V_{CEQ2} \geq 1.5(V_{opeak} + V_{CE(sat)})$

(The value is multiplies by 1.5 to take care of saturation voltages, variations in resistors, variation in supply voltage and decide parameter variations.)

$V_{opeak} = V_{orms} \times \sqrt{2} = 2\sqrt{2} = \mathbf{2.828V}$

$V_{CEQ2} \geq 1.5(2.828 + 0.25)$

$V_{CEQ2} \geq \mathbf{4.6176}$

$V_{CEQ2} = \mathbf{4.7V}$

$$I_{opeak} = \frac{V_{opeak}}{R_{C2}} = \frac{2.828}{750} = \mathbf{3.77mA}$$

$I_{CQ2} \geq I_{opeak}$ (for undistorted output signal)

$I_{CQ2} \geq 3.77mA$

$I_{CQ2} = 3.8mA$

5. Selection of DC power supply (V_{CC})**:**

In order to achieve maximum symmetrical output swing, we always select Q point at center of DC load line

$V_{CC} \geq 2V_{CEQ2} \geq 2 \times 4.7 \geq 9.4V$ (select HSV)

Select $V_{CC} = 10V$

6. Calculations of R_{E2}:

For proper operation,

$V_{RE2} = 10\% \text{of } V_{CC} = 0.1 \times 10 = \mathbf{1V}$

$V_{RE2} = I_{EQ2} R_{E2}$

$$R_{E2} = \frac{V_{RE2}}{I_{EQ2}}$$

$I_{EQ2} = I_{CQ2}$

$R_{E2} = \frac{V_{RE2}}{I_{EQ2}} = \frac{1}{3.8 \times 10^{-3}} = 263.16V$

$R_{E2} = \mathbf{240\Omega, 1/4W}$ (selecting LSV)

7. Calculation of biasing resistors (R_3 and R_4):

$$S\frac{1+\beta}{1+\beta\left(\frac{R_{E2}}{R_{E2}+R_{B2}}\right)}$$

$\beta = h_{FE(typ)} = 180$

$$10 = \frac{1+180}{1+180\left(\frac{240}{240+R_{B2}}\right)} = \mathbf{2286.315\Omega}$$

$$R_{B2} = \frac{R_3R_4}{R_3+R_4} \quad .....1$$

$$V_{TH2} = V_{B2} = \frac{R_4}{R_3R_4} \times V_{CC} \quad .....2$$

Applying KVL at loop of Q_2

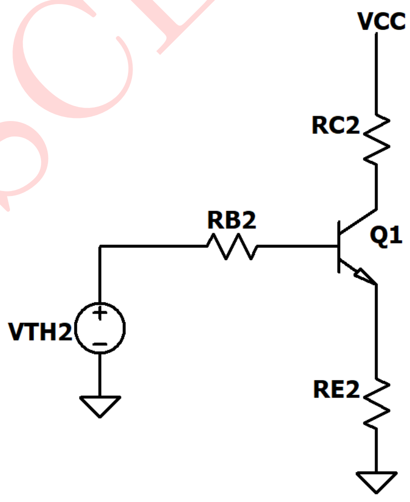

Figure 2: Thevenin Equivalent Circuit of Q_1

Applying KVL at loop of Q_2

$V_{B2} - I_{BQ2}R_{B2} - V_{BE2} - I_{EQ2}R_{E2} = 0$

$V_{B2} = V_{BE2} + I_{BQ2}R_{B2} + I_{EQ2}R_{E2}$

But $I_{EQ2} = I_{CQ2}$ and $I_{BQ2} = \frac{I_{CQ2}}{\beta_2}$

$$V_{B2} = 0.7 + \frac{I_{CQ2}}{\beta_2} R_{B2} + I_{CQ2} R_{E2} = 0.7 + \frac{3.8 \times 10^{-3}}{180}(2286.315) + (3.8 \times 10^{-3})(240)$$

$$= 0.7 + 0.04826 + 0.912 = \mathbf{1.66V}$$

From 2, $V_{B2} = 1.66 = \frac{R_4}{R_3 + R_4} \times V_{CC}$

$$\frac{R_4}{R_3 + R_3} = \frac{1.66}{10} = \mathbf{0.166} \qquad .....3$$

Putting 3 in 1, $0.166 \times R_3 = \mathbf{2286.315}$

$R_3 = 13.772k\Omega$

Selecting HSV $R_3 = \mathbf{15k\Omega, 1/4W}$

From 3, $\frac{R_4}{R_3 + R_4} = 0.166$

$$\frac{R_4}{15k + R_4} = 0.166$$

$R_4 = 0.166 \times 15 \times 10^3 + 0.166R_4$

$0.824R_4 = 2490$

$R_4 = 2985.61$

Selecting LSV, $R_4 = \mathbf{2.7k\Omega, 1/4W}$

Design of first stage:

8. Selection of R_{C1}:

$$|A_{V2}| = \frac{h_{fe(typ)} R_{C2}}{h_{ie}} = \frac{220 \times 750}{2.7 \times 10^3} = \mathbf{61.11}$$

$$A_{V1} = \frac{A_{VT}}{A_{V2}} = \frac{1750}{61.11} = \mathbf{28.636}$$

Let $A_{V1} = 29$

$$|A_{V1}| = \frac{h_{fe(typ)} R_{L1}}{h_{ie}}$$

Where, $R_{L1} = R_{C1} \mid\mid R_3 \ R_4 \mid\mid h_{ie} = R_{C1} \mid\mid 15k \mid\mid 2.7k \mid\mid 2.7k = R_{C1} \mid\mid 15k \mid\mid 1.35k$

$$= R_{C1} \mid\mid 1.2385k$$

$$\therefore 29 = \frac{220 \times (R_{C1} \mid\mid 1.2385k)}{2.7k} = \frac{220 \times R_{C1} \times 1.2385k}{2.7k(R_{C1} + 1.2385k)}$$

$$\frac{R_{C1}}{R_{C1} + 1.2385k} = 0.28737$$

$R_{C1}(1 - 0.28737) = 0.38737 \times 1.2385 \times 10^3 = 499.43\Omega$

Selecting HSV , $R_{C1} = 510\Omega, 1/4W$

9. Calculation of R_{E1}:

$V_{CEQ1} = V_{CEQ2} = 4.7V$

$V_{RE1} = V_{RE2} = 1V$

$V_{RC1} = V_{RC2}$

So, $I_{CQ1}R_{C1} = I_{CQ2}R_{C2}$

$$\frac{I_{CQ2}R_{C2}}{R_{C1}} = \frac{3.8 \times 10^{-3} \times 750}{510} = \mathbf{5.588mA}$$

$V_{RE1} = I_{EQ1}R_{E1} = 1V$

$$R_{E1} = \frac{V_{RE1}}{I_{CQ1}} = \frac{1}{5.588 \times 10^{-3}} = \mathbf{178.95\Omega}$$

Selecting LSV, $R_{E1} = 150\Omega, 1/4W$

10. Calculation of biasing resistors (R_1 and R_2):

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_{E1}}{R_{B1}+R_{E1}}\right)}$$

$R_{B1} = R_1 \ || \ R_2$

$h_{fe(typ)} = \beta = 180$

$$10 = \frac{1+180}{1+180\left(\frac{150}{R_{B1}+150}\right)} = \mathbf{1428.94}$$

$$R_{B1} = \frac{R_1R_2}{R_1+R_2} = \mathbf{1428.94} \qquad .....4$$

Applying KVL at Base - Emitter Loop of Q_1;

$V_{B1} - V_{BE1} - I_{BQ1}R_{B1} - I_{EQ1}R_{E1} = 0$

$$I_{BQ1} = \frac{I_{CQ1}}{\beta_1} \text{ and } I_{EQ1} = I_{CQ1}$$

$$V_{B1} = V_{BE1} + \frac{I_{CQ1}}{\beta_1}R_{B1} + I_{CQ1}R_{E1} = 0.7 + \frac{5.588 \times 10^{-3}}{180}(1428.94) + (5.588 \times 10^{-3} \times 150)$$

$V_{B1} = 0.7 + 0.044 + 0.8382 = 1.5822V$

$$\text{Now, } V_{B1} = V_{TH1} = \frac{R_2V_{CC}}{R_1+R_2}$$

$$1.5822 = \frac{R_2}{R_1+R_2} \times 10$$

$$\frac{R_2}{R_1+R_2} = 0.15822 \qquad .....5$$

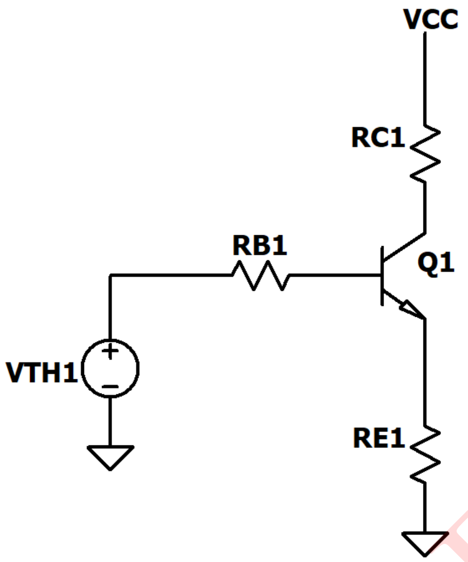

Figure 3: Thevenin Equivalent Circuit of Q_1

From 4 and 5, we get;

$R_1(0.15822) = 1428.94 = \mathbf{9.0313k\Omega}$

Select HSV, $R_1 = 9.1K\Omega, 1/4W$

$$\frac{R_2}{9.1k + R_2} = 0.15822$$

$R_2(1 - 0.15822) = 0.15822 \times 9.1 \times 10^3 = 17104\Omega$

Select LSV, $R_2 = 1.5k\Omega, 1/4W$

11. Calculations of Coupling capacitors (C_{C1}, C_{C2} , C_{C3})

a. $C_{C1} = \dfrac{1}{2\pi R_{eq} f_L}$

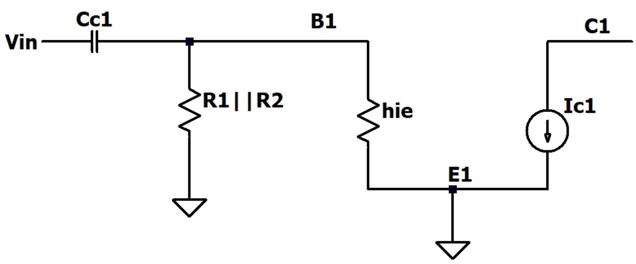

Figure 4: Small signal equivalent circuit of C_{C1}

Where, $R_{eq} = R_1 \ || \ R_2 \ || \ h_{ie} = 9.1k \ || \ 1.5k \ || \ 2.7k = 871.89\Omega$

$$C_{C1} = \frac{1}{2\pi \times 30 \times 871.89} = 6.0846\mu F$$

Select HSV, $C_{C1} = \mathbf{6.2\mu F/25V}$

b. $C_{C2} = \dfrac{1}{2\pi R_{eq2} f_L}$

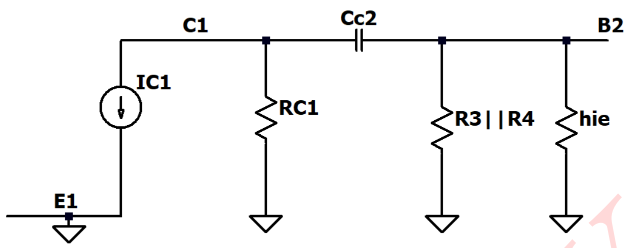

Figure 5: Small signal equivalent circuit of C_{C2}

Where,

$R_{eq2} = R_{C1} + (R_3 \parallel R_4 \parallel h_{ie}) = 510 + (15k \parallel 2.7k \parallel 2.7k) = 510 + 1.2385k = 1748.53\Omega$

$$C_{C2} = \frac{1}{2\pi \times 30 \times 1748.53} = 3.034\mu F$$

Select HSV, $C_{C2} = \mathbf{3.3\mu F/25V}$

c. $C_{C3} = \dfrac{1}{2\pi R_{eq3} f_L}$

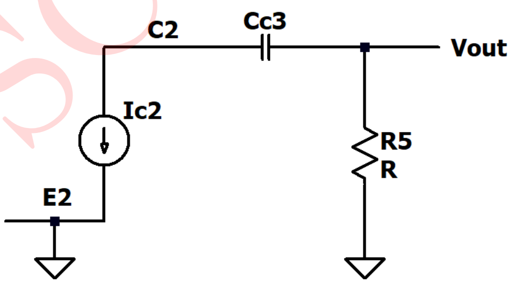

Figure 6: Small signal equivalent circuit of C_{C3}

$R_{eq3} = R_{C2} = 750\Omega$

$$\therefore C_{C3} = \frac{1}{2\pi \times 30 \times 750} = 7.07\mu F$$

Select HSV, $C_{C3} = \mathbf{7.5\mu F/25V}$

12. Calculations of bypass capacitors (C_{E1}, C_{E2})

a. For C_{E1}:

$$X_{CE1} = \frac{R_{E1}}{10}$$

$$\frac{1}{2\pi f_L C_{E1}} = \frac{R_{E1}}{10}$$

$$C_{E1} = \frac{10}{2\pi f_L R_{E1}} = \frac{10}{2\pi \times 30 \times 150} = 353.67\mu F$$

Select HSV, $C_{E1} = \mathbf{390\mu F/25V}$

b. For C_{E2}:

$$X_{CE2} = \frac{R_{E2}}{10} = \frac{240}{10} = 24$$

$$\frac{1}{2\pi C_{E2} f_L} = 24$$

$$C_{E2} = \frac{1}{2\pi \times 24 \times 30} = 221.04\mu F$$

Select HSV, $C_{E2} = \mathbf{240\mu F/25V}$

13. Complete designed circuit:

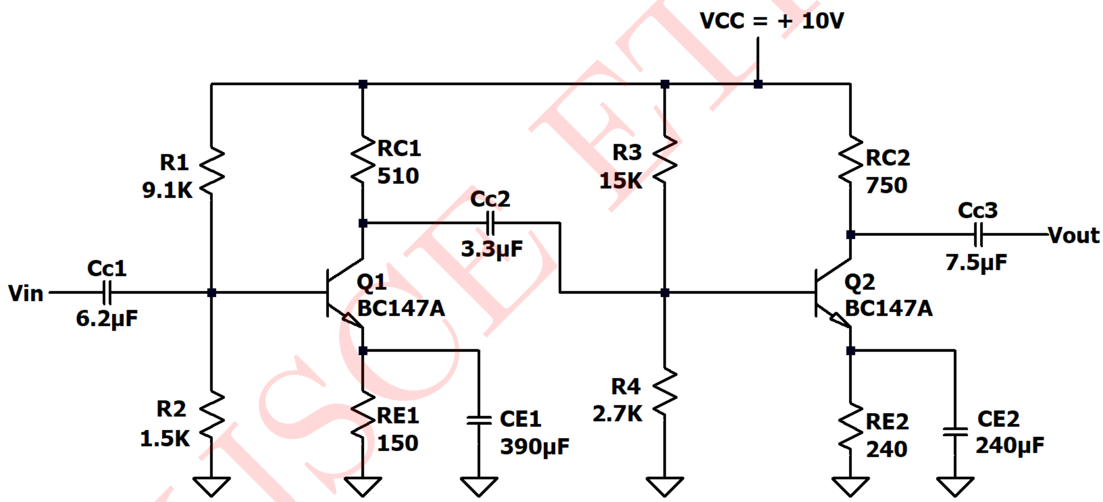

Figure 7: Designed circuit

Verification of Overall gain A_{VT}:

$$A_{V2} = \frac{h_{fe(typ)} R_{C2}}{h_{ie}} = \frac{220 \times 750}{2.7 \times 10^3} = 61.111$$

$$A_{V1} = \frac{h_{fe(typ)}(R_{C2} \ || \ R_3 \ || \ R_4 \ || \ h_{ie})}{h_{ie}} = \frac{220 \times (510 \ || \ 15k \ || \ 2.7k \ || \ 2.7k)}{2.7 \times 10^3}$$

$$= \frac{220 \times (493.23 \ || \ 1350)}{2.7 \times 10^3} = \mathbf{29.43}$$

Now, $A_{VT} = A_{V1} \times A_{V2} = 61.111 \times 29.43 = 1798.79$

So, $A_{VT} \geq 1750$

DC Analysis: For first stage:

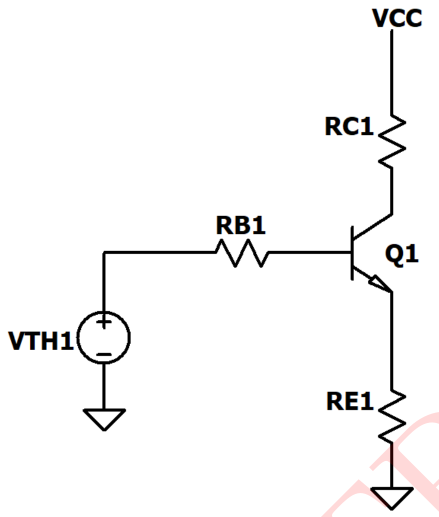

Figure 8: Thevenin equivalent circuit for first stage

$R_{TH1} = R_1 \ || \ R_2 = 9.1k \ || \ 1.5k = 1.2877k\Omega$

$V_{TH1} = \dfrac{R_2}{R_1 + R_2} \times V_{CC} = \dfrac{1.5k}{9.1k + 1.5k} \times 10 = 1.415V$

Applying KVL to Base - Emitter loop;

$V_{TH1} - I_{B1}R_{TH1} - V_{BE1} - I_{E1}R_{E1} = 0$

But$I_{E1} = (1 + \beta_1)I_{B1}$

$\therefore V_{TH1} - V_{BE1} = I_{B1}R_{TH1} + (1 + \beta_1)I_{B1}R_{E1}$

$I_{B1} = \dfrac{V_{TH} - V_{BE1}}{R_{TH1} + (1 + \beta_1)R_{E1}} = \dfrac{1.415 - 0.7}{1.2877k + (181)(150)} = \dfrac{0.71509}{28437.7} = \mathbf{25.14\mu A}$

Now, $I_{C1} = \beta_1 I_{B1} = 4.5mA$

$I_{E1} = (\beta_1 + 1)I_B = 181 \times 25.14 \times 10^{-6} = \mathbf{4.5mA}$

$V_{E1} = I_{E1}R_{E1} = 4.5 \times 10^{-3} \times 150 = \mathbf{0.675V}$

$V_{BE1} = 0.7 = V_{B1} - V_{E1}$

$V_{B1} = 0.7 + V_{E1} = 0.7 + 0.675 = 1.375V$

Here, $R_{TH2} = 15||2.7k = 2.288k\Omega$

$V_{TH} = \dfrac{R_2}{R_1 R_2} \times V_{CC} = \dfrac{2.7k}{15k + 2.7k} \times 10 = \mathbf{1.5254V}$

Applying KVL to Base - Emitter loop;

$V_{TH2} - I_{B2}R_{TH2} - V_{BE2} - I_{E2}R_{E2} = 0$

But, $I_{E2} = (1 + \beta_2)I_{B2}$

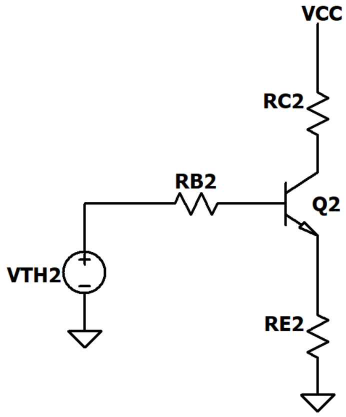

Figure 9: Thevenin equivalent circuit for second stage

$$I_{B2} = \frac{V_{TH} - V_{BE2}}{R_{TH2} + (1+\beta_2)R_{E2}} = \frac{1.5254 - 0.7}{2.288k + (181)(240)} = \frac{0.8254}{45728} = \mathbf{18\mu A}$$

$$I_{C2} = \beta_2 I_{B2} = 180 \times 18 \times 10^{-6} = \mathbf{3.24mA}$$

$$I_{E2} = (\beta_2 + 1)I_{B2} = 181 \times 3.24mA = \mathbf{3.26mA}$$

$$V_{E2} = I_{E2}R_{E2} = 03.26 \times 10^{-3} \times 240 = \mathbf{0.78V}$$

$$V_{B2} = V_{BE2} + V_{E2} = 0.7 + 0.78 = \mathbf{1.48V}$$

Small signal parameters:

$$g_{m1} = \frac{I_{C1}}{V_T} = \frac{4.5 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{173.076mA/V}$$

$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{C1}} = \frac{180 \times 26 \times 10^{-3}}{4.5 \times 10^{-3}} = \mathbf{1040\Omega}$$

$$g_{m2} = \frac{I_{C2}}{V_T} = \frac{3.24 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{124.6mA/V}$$

$$r_{\pi 2} = \frac{\beta_2 V_T}{I_{C2}} = \frac{18 \times 26 \times 10^{-3}}{3.24 \times 10^{-3}} = \mathbf{1444.44\Omega}$$

Mid band frequency equivalent circuit

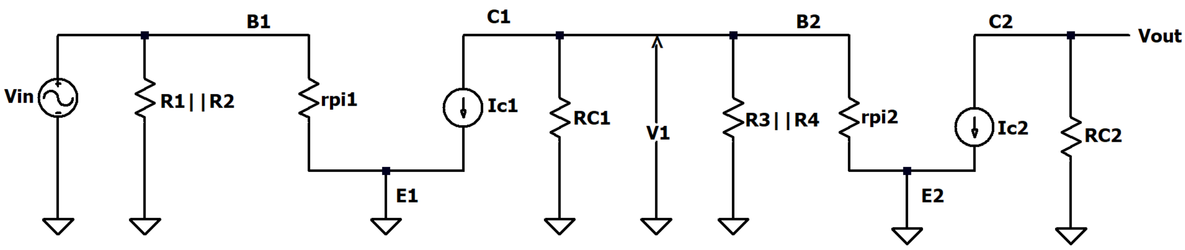

Figure 10: mid band frequency equivalent circuit

Voltage gain of first stage:

$$A_{V1} = \frac{V_1}{V_{in}} = \frac{-g_m V_{\pi 1}(R_{C1} \mid\mid R_3 \mid\mid R_4 \mid\mid r_{\pi 2})}{V_\pi} = -g_m(R_{C1} \mid\mid R_3 \mid\mid R_4 \mid\mid r_{\pi 2})$$

$$= -173.076 \times 10^{-3}(15k \mid\mid 2.7k \mid\mid 510 \mid\mid 1444.44)$$

$$= -173.076 \times 10^{-3}(2288.135 \mid\mid 376.918) = \mathbf{-56}$$

Voltage gain of second stage:

$$A_{V2} = \frac{V_{out}}{V_1} = \frac{-g_{m2}V_{\pi 2}R_{C2}}{V_{\pi 2}} = -g_{m2}R_{C2} = -124.6 \times 10^{-3} \times 750 = \mathbf{-93.45}$$

Overall voltage gain:

$$A_{VT} = A_{V1} \times A_{V2} = -56 \times -93.45 = \mathbf{5233.2}$$

$$A_{VT} \text{ in dB} = 20log_{10}(5233.2) = \mathbf{74.375dB}$$

Input impedance of first stage

$$Z_i = R_1 \mid\mid R_2 \mid\mid r_{\pi 1} = 9.1k \mid\mid 1.5k \mid\mid 1040 = \mathbf{575.34\Omega}$$

Output impedance of second stage:

$$Z_o = R_C = \mathbf{750\Omega}$$

SIMULATED RESULTS:
Above circuit is simulated in LTspice and the result is as follows:

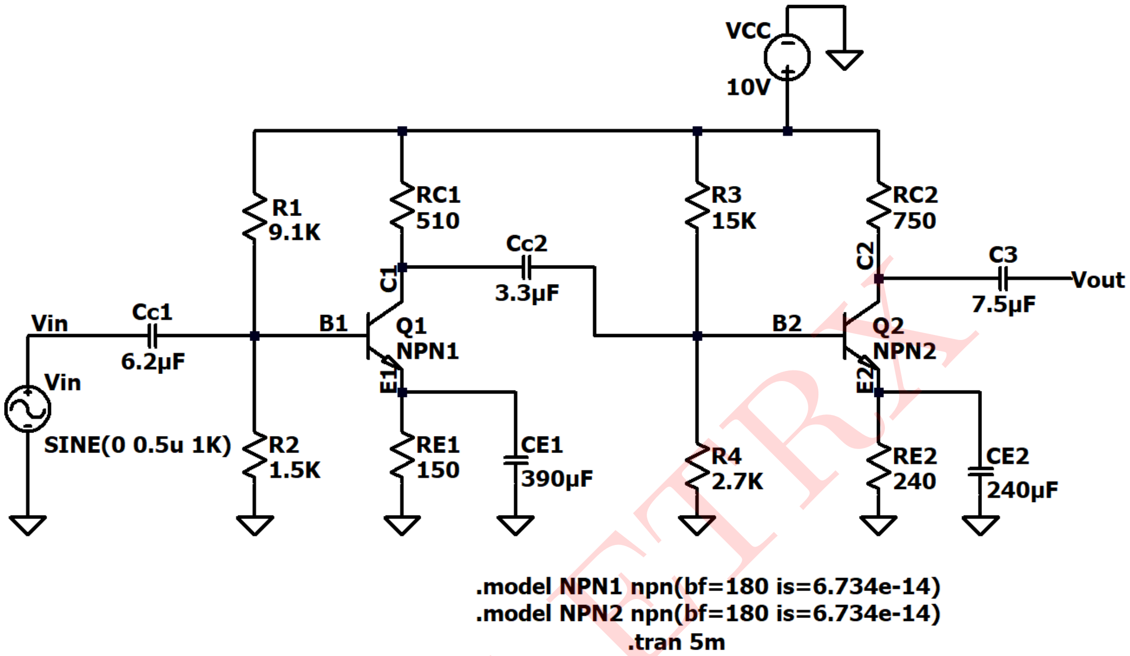

Figure 11: Circuit Schematic

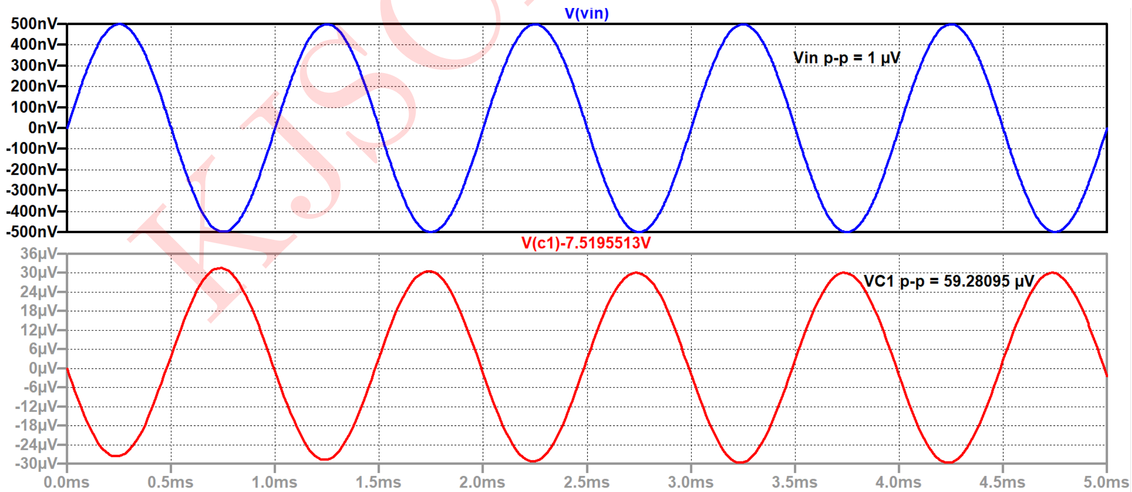

Figure 12: Input output waveform stage 1

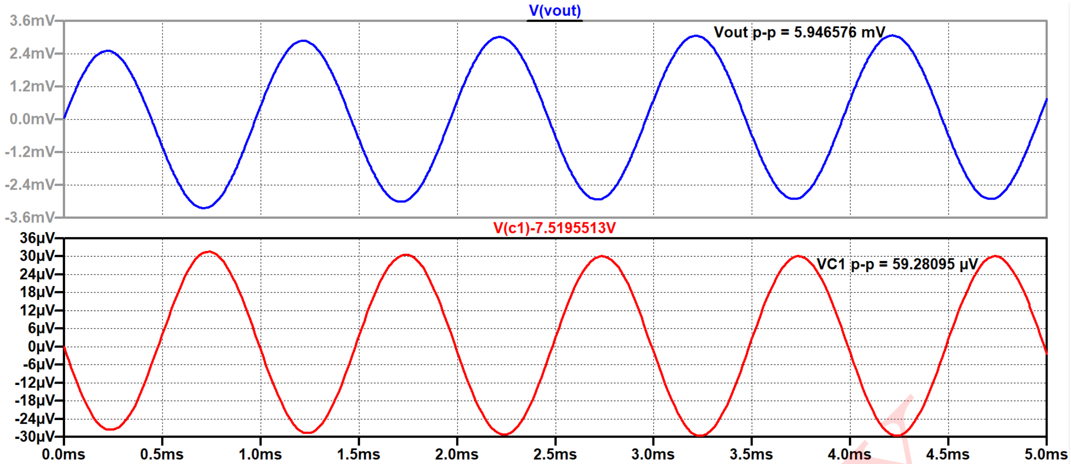

Figure 13: Input output waveform stage 2

Comparison between Theoretical and Simulated values :-

Parameters	Theoretical	Simulated
I_{B1}	$25\mu A$	$27\mu A$
I_{C1}	4.5mA	4.8mA
I_{E1}	4.5mA	4.8mA
I_{B2}	$18\mu A$	$19\mu A$
I_{C2}	3.2mA	3.49mA
I_{E2}	3.2mA	3.5mA
V_{B1}	1.375V	1.38V
V_{E1}	0.67V	0.73V
V_{B2}	1.48V	1.48V
V_{E2}	0.88V	0.84V
Voltage gain of first stage	-30	-59.28
Voltage gain of second stage	-59	-100.3
Overall voltage gain	64.86dB	75.48dB
input impedance	575.34Ω	–
output impedance	750Ω	–

Table 1: Numerical 1

Design 2: Design a two stage RC coupled cascade amplifier for following specifications $A_V \geq 400$, $V_{CC} = 20V$, $S \leq 10$, $R_i \geq 1M\Omega$. Use transistor BC 147A from the data sheet.

Solution:

Above requirements can be fulfilled by CS - CS stage. (We select CS as the first stage since $R_i \geq 1M\Omega$)

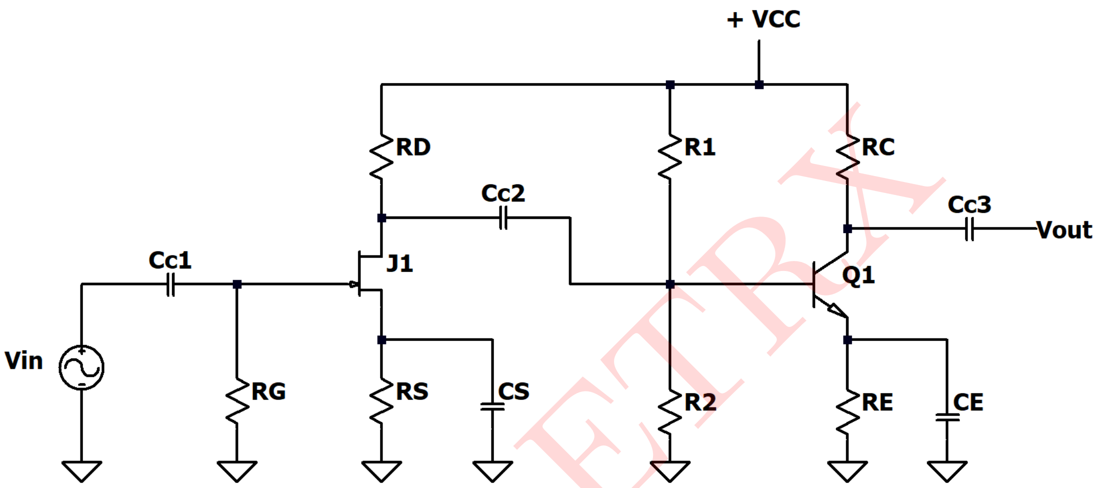

Figure 14: Circuit 2

1)Selection of transistor:

Selecting BC147B:
$h_{fe(typ)} = 330$, $h_{FE(typ)} = 290 = \beta$
$h_{ie} = 4.5k\Omega$, $V_{CE(sat)} = 0.25V$

Selecting BFW11:
$I_{DSS} = 7mA$, $g_{mo} = 5600\mu\mho$
$V_P = -2.5V$, $r_d = 50k\Omega$

2. Selection of voltage gains:

$A_V \geq 400$

Ley $A_{V1} = 4$ (Since JFET amplifier gain is less)

$$A_{V2} = \frac{400}{4} = \mathbf{100}$$

Let $A_{V2} = 100$

Design of second stage:

3. Calculations of R_C:

$$|A_{V2}| = \frac{h_{fe(typ)} R_C}{h_{ie}}$$
$$100 = \frac{330 \times R_C}{4.5 \times 10^3}$$

$R_C = 1.3636k\Omega$

Selecting HSV, $R_{C2} = \mathbf{1.5k\Omega, 1/4W}$

4. Selection of Q point (V_{CEQ2}, I_{CQ2})

$V_{CC} = 20V;$

Let $V_{CEQ2} = \frac{V_{CC}}{2} = \mathbf{10V}$

$V_{RE} = 0.1V_{CC} = 0.1 \times 20 = \mathbf{2V}$

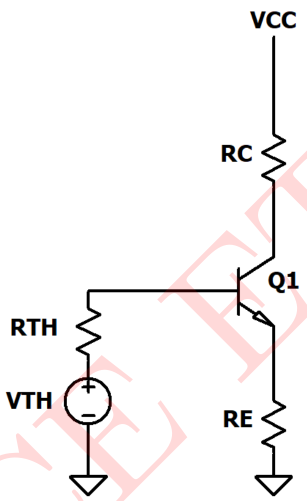

Figure 15: Thevenin Equivalent Circuit of BJT

Applying KVL to Common - emitter loop;

$V_{CC} - V_{RC} - V_{CEQ} - V_{RE} = 0$

$V_{RC} = V_{CC} - V_{CEQ} - V_{RE} = 20 - 10 - 2 = \mathbf{8V}$

$V_{RC} = I_{CQ}R_C = 8$

$I_{CQ} = \frac{8}{1.5 \times 10^3} = \mathbf{5.33mA}$

5. Selection of R_E**:**

$V_{RE} = 2V$

$\therefore I_{EQ}R_E = 2$

$\therefore R_E = \frac{2}{5.33 \times 10^{-3}} = \mathbf{375.23\Omega}$ (since $I_{EQ} = I_{CQ}$)

Selecting LSV, $R_E = \mathbf{390\Omega, 1/4W}$

$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{5.33 \times 10^{-3}}{290} = \mathbf{18.37\mu A}$

$I_{EQ} = I_{CQ} + I_{BQ} = 5.34mA$

6. Selection of biasing resistors R_1 and R_2:

$S \leq 10$ and $\beta = 290$

Let $S = 10$

$$S = \frac{1+\beta}{1+\beta\left(\dfrac{R_E}{R_B+R_E}\right)}$$

$$10 = \frac{1+290}{1+290\left(\dfrac{390}{390+R_B}\right)}$$

$R_B = 3.6349k\Omega$

$$R_B = R_1 \mid\mid R_2 = \frac{R_1R_2}{R_1+R_2} = 3.6349k\Omega \qquad .....1$$

$$V_B = V_{TH2} = \frac{R_2}{R_1+R_2} \times V_{CC} \qquad .....2$$

Applying KVL at base -emitter loop of BJT;

$V_B - I_{BQ}R_B - V_{BE} - I_{EQ}R_E = 0$

$V_B = I_{BQ}R_B + V_{BE} + I_{EQ}R_E$

$I_{EQ} = I_{CQ}$ and $I_{BQ} = \dfrac{I_{CQ}}{\beta}$

$$\therefore V_B = \frac{I_{CQ}}{\beta}R_B + V_{BE} + I_{CQ}R_E = \frac{5.33}{290} \times 10^{-3} \times 3.6349 \times 10^3 + 0.7 + 5.33 \times 10^{-3} \times 390 = \mathbf{2.8455V}$$

From 2, $2.8455 = \dfrac{R_2}{R_1+R_2} \times 20$

$$\frac{R_1}{R_1+R_2} = 0.142275 \qquad .....3$$

Putting 3 in 1;

$R_1 \times 0.142275 = 3.6349 \times 10^3$

$R_1 = \mathbf{25548.40\Omega}$

Selecting HSV, $R_1 = \mathbf{27k\Omega, 1/4W}$

From 3; $\dfrac{R_2}{R_2+27k} = 0.142275$

$R_2 = 0.142275R_2 + 3841.425 = \mathbf{4.4786k\Omega}$

Selecting HSV, $R_2 = \mathbf{4.7k\Omega, 1/4W}$

$V_E - I_{EQ}R_E = 5.34 \times 10^{-3} \times 390 = \mathbf{2.0826V}$

Design of first stage:

7. Selection of Q point I_{DQ}, V_{GSQ}:

using Mid- point biasing

$$I_{DQ} = \frac{I_{DSS}}{2} = \frac{7mA}{2} = \mathbf{3.5mA}$$

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_{DQ}}{I_DS}}\right) = -2.5\left(1 - \sqrt{\frac{3.5}{7}}\right) = \mathbf{-0.732V}$$

$$g_{m1} = g_{mo}\left(1 - \frac{V_{GSQ}}{V_P}\right) = 5600 \times 10^{-6}\left(1 - \frac{(-0.732)}{-2.5}\right) = \mathbf{3.96mA/V}$$

8. Calculation of R_D:

$$|A_{V2}| = \frac{h_{fe(typ)} \times R_C}{h_{ie}} = \frac{330 \times 1.5 \times 10^3}{4.5 \times 10^3} = \mathbf{110}$$

$$A_{V1} = g_{m1}(R_D \parallel r_d \parallel R_1 \parallel R_2 \parallel h_{ie})$$

$$R_{L1} = r_d \parallel R_1 \parallel R_2 \parallel h_{ie} = 50k \parallel 27k \parallel 4.7k \parallel 4.5k = \mathbf{2032.426\Omega}$$

$$|A_{V1}| = g_m(R_D \parallel 2032.416)$$

Now, $|A_{V1}| = \frac{A_{VT}}{A_{V2}} = \frac{400}{110} = \mathbf{3.636}$

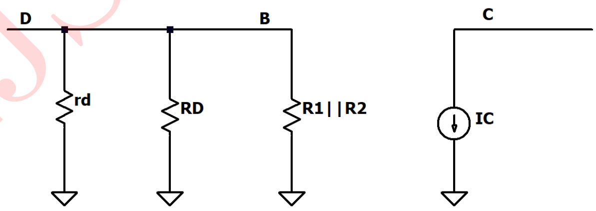

Figure 16: Small signal equivalent circuit for selection of R_D

$$\therefore 3.636 = 3.96 \times 10^{-3}(R_D \parallel 2032.416)$$

$$\therefore 3.636 = 3.96 \times 10^{-3}\left(\frac{R_D \times 2032.416}{R_D + 2032.416}\right)$$

$$\therefore 918.27(R_D) = 1866314.05 = 2032.416(R_D)$$

$$R_D = 1.675k\Omega$$

Selecting HSV, $R_D = 1.8k\Omega, 1/4W$

9. Selection of R_S:

$$V_{GSQ} = -I_{DQ}R_S$$

$-0.732 = -3.5 \times 10^{-3} R_S$

$R_S = 209.14\Omega$

Selecting LSV, $R_S = 180\Omega, 1/4W$

10. Calculations of R_G

Let $R_G =$ **$1.2M\Omega, 1/4W$** (since $R_i \geq 1M\Omega$, to prevent loading $R_G \geq R_i$)

11. Calculations of Coupling capacitors (C_{C1}, C_{C2} , C_{C3})

a. $C_{C1} = \dfrac{1}{2\pi R_G f_L}$ (since f_L is not given we consider audio frequency $f_L = 20Hz$)

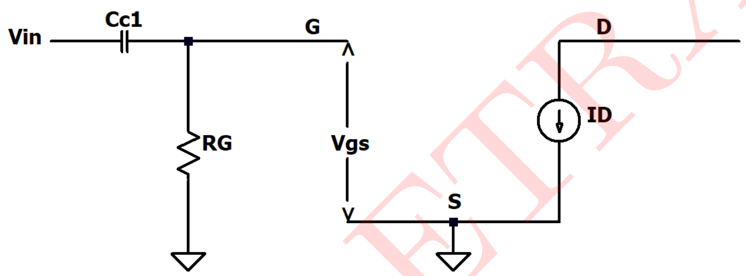

Figure 17: Low frequency equivalent circuit of C_{C1}

$C_{C1} = \dfrac{1}{2\pi \times 1.2 \times 10^6 \times 20} = 6.63nFF$

Select HSV, $C_{C1} =$ **6.63nF/50V**

b. $C_{C2} = \dfrac{1}{2\pi R_{eq} f_L}$

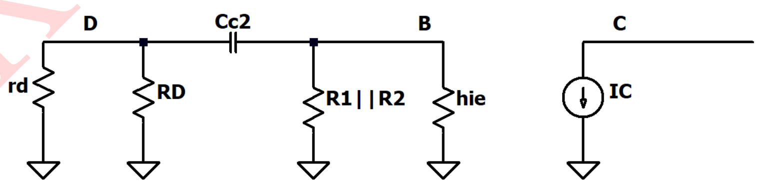

Figure 18: Low frequency equivalent circuit of C_{C2}

$R_{eq} = r_d \; || \; R_D + (R_1 \; || \; R_2 \; || \; h_{ie}) = (50k \; || \; 1.8k) + (27k \; || \; 4.7k \; || \; 4.5k)$

$= 1737.45 + 2118.53 = \mathbf{3855.98\Omega}$

$C_{C2} = \dfrac{1}{2\pi \times 3855.98 \times 20} = 32.06374\mu F$

Select HSV, $C_{C2} = \mathbf{2.2\mu F/50V}$

c. $C_{C3} = \dfrac{1}{2\pi R_{eq2} f_L}$

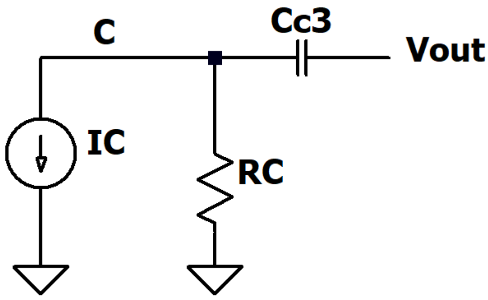

Figure 19: Low frequency equivalent circuit of C_{C3}

$R_{eq3} = R_C = 1.5k\Omega$

$\therefore C_{C3} = \dfrac{1}{2\pi \times 1.5 \times 10^3 \times 20} = 5.305\mu F$

Select HSV, $C_{C3} = \mathbf{5.6\mu F/50V}$

12. Calculations of bypass capacitors:

a. For C_S:

$R_{eq} = \left(\dfrac{1}{g_m} ||R_S\right) = \left(\dfrac{1}{3.96 \times 10^{-3}} || 180\right) = \mathbf{105.09\Omega}$

$C_S = \dfrac{1}{2\pi \times 105.09 \times 20} = \mathbf{75.72\mu F}$

Selecting HSV, $C_S = 82\mu F/50V$

b. For C_E:

$X_{CE} = 0.1R_E$

$\dfrac{1}{2\pi C_E f_L} = 0.1R_E$

$C_E = \dfrac{1}{2\pi \times 20 \times 0.1 \times 390} = 204\mu F$

Select HSV, $C_E = \mathbf{220\mu F/50V}$

13. Complete designed circuit:

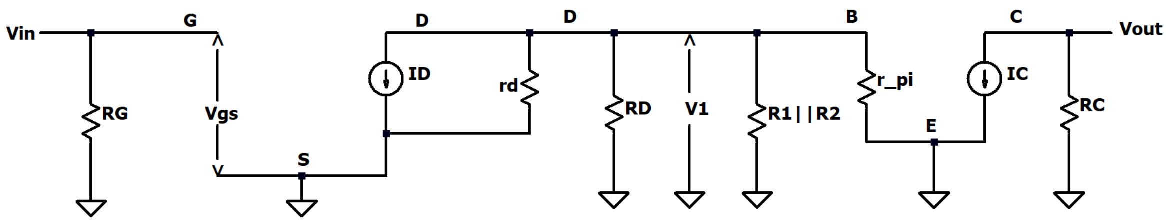

Figure 20: Designed circuit

Mid band frequency equivalent circuit

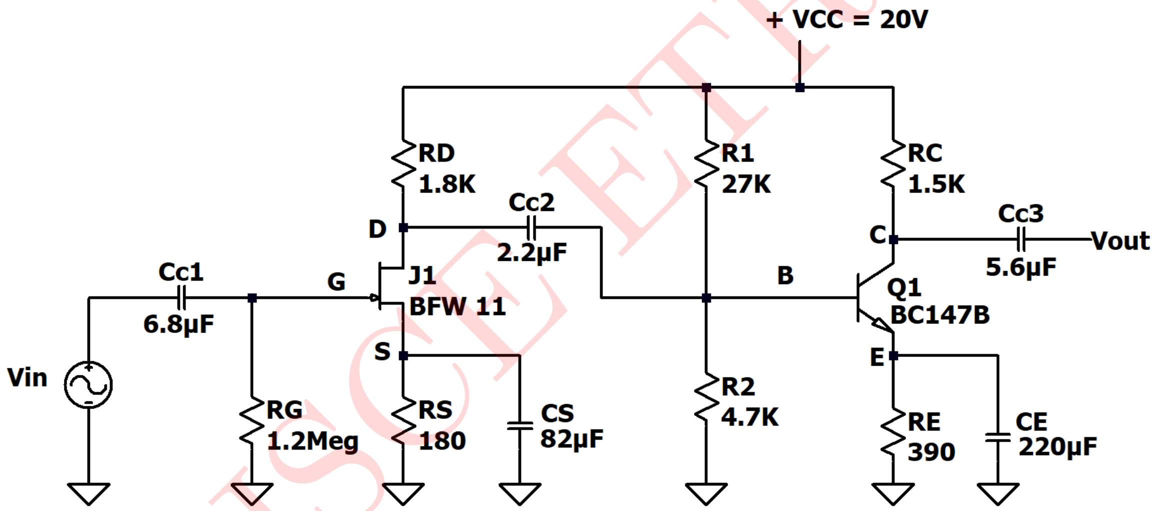

Figure 21: Mid band frequency equivalent circuit

Input impedance:

$Z_i = R_G = \mathbf{1.2M\Omega}$

Output impedance :

$Z_o = R_C = \mathbf{1.5k\Omega}$

$g_{m1} = \mathbf{3.96mA/V}$

$$g_{m2} = \frac{I_CQ}{V_T} = \frac{5.33 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{205mA/V}$$

$A_{VT} = A_{V1} \times A_{V2}$

Here, $A_{V2} = \dfrac{V_{out}}{V_1}$ and $A_{V1} = \dfrac{V_1}{V_{in}}$

$$A_{V2} = \frac{-g_{m2} V_\pi R_C}{V_\pi} = -g_{m2} R_C = -205 \times 10^{-3} \times 1.5 \times 10^3 = \mathbf{-307.5}$$

$$A_{V1} = \frac{V_1}{V_{in}} = \frac{-g_{m1} V_{gs} (r_d \parallel R_D \parallel R_L \parallel R_2 \parallel r_\pi)}{V_{gs}} = -g_{m1}(r_d \parallel R_D \parallel R_1 \parallel R_2 \parallel r_\pi)$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{290 \times 26 \times 10^{-3}}{5.33 \times 10^{-3}} = 1.4146k\Omega$$

$$A_{V1} = -3.96 \times 10^{-3}(50k \parallel 1.8k \parallel 27k \parallel 4.7k \parallel 1.4146k) = \mathbf{-2.584}$$

$$A_{VT} = -307.5 \times -2.584 = \mathbf{794.58}$$

$$A_{VT} \text{ in dB} = 20log_{10}(794.58) = \mathbf{58dB}$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and the result is as follows:

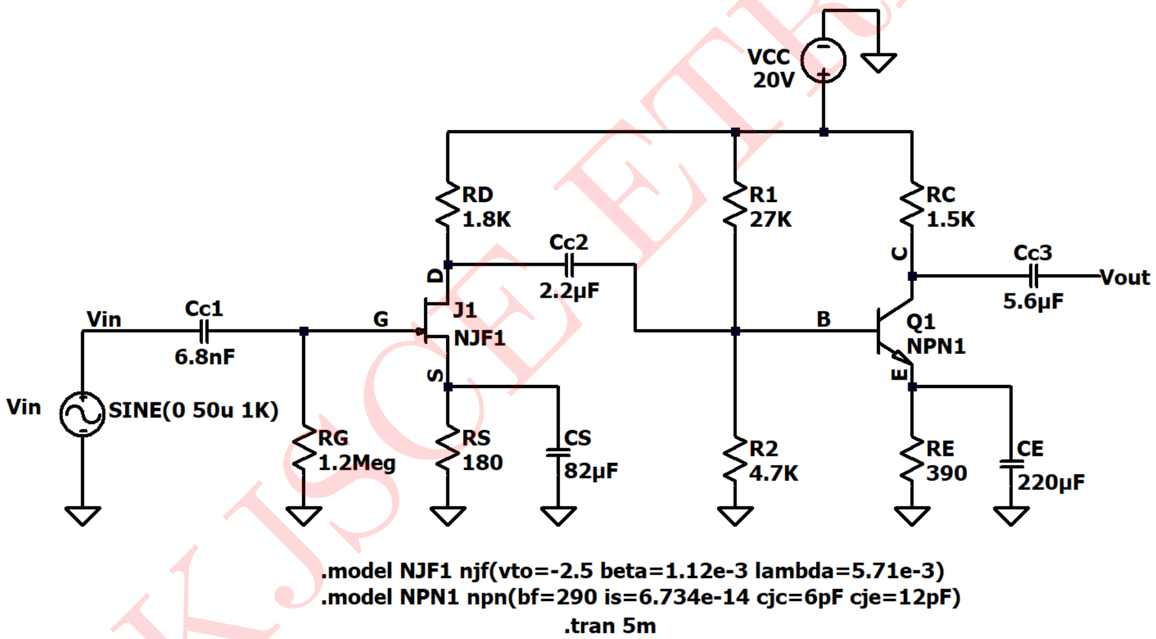

Figure 22: Circuit Schematic

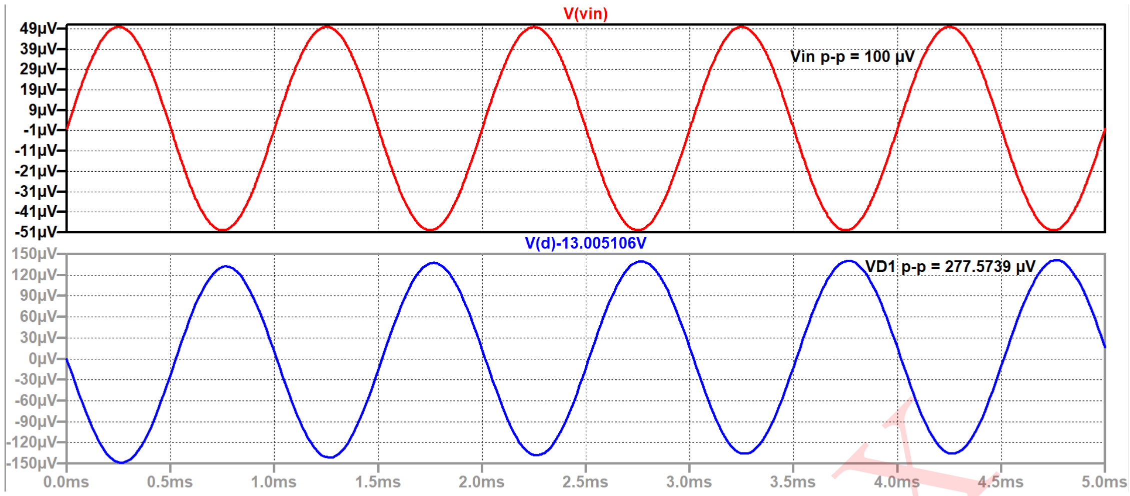

Figure 23: Input output waveform of stage 1

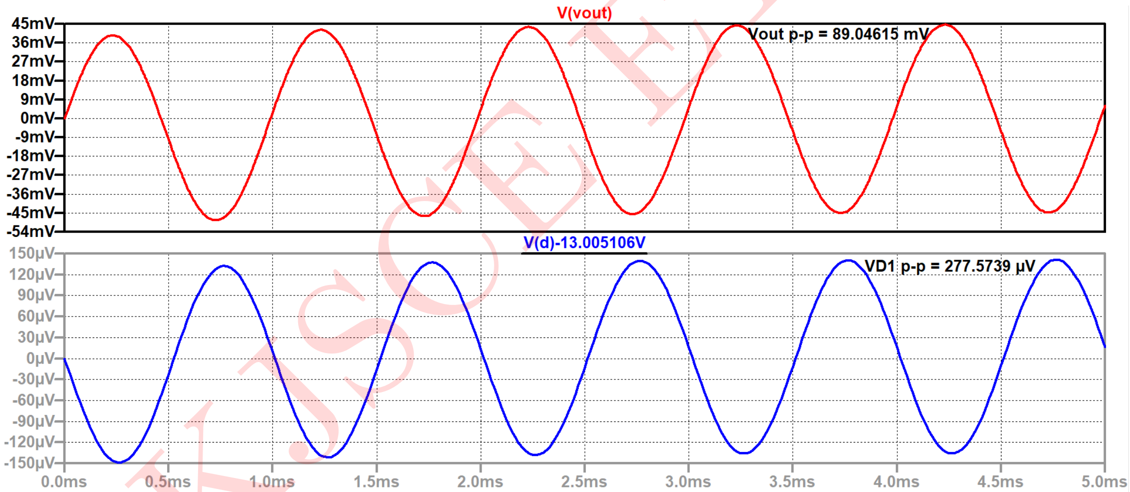

Figure 24: Input output waveform of stage 2

Comparison between Theoretical and Simulated values :-

Parameters	Theoretical	Simulated
I_{DQ}	3.5mA	3.8mA
V_{GSQ}	$-0.732V$	-0.6885
I_B	$18.37\mu A$	$19.67\mu A$
I_C	5.33mA	5.7mA
I_E	5.34mA	5.7mA
V_E	2.0826V	2.23V
V_B	2.8455V	2.88V
Voltage gain of first stage	-2.584	-2.77
Voltage gain of second stage	-307.5	-320.08
Overall voltage gain	52.04dB	58.97dB
input impedance	$1.2M\Omega$	$-$
output impedance	$1.5k\Omega$	$-$

Table 2: Numerical 2

****