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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Oscillator circuits

13^{th} **July, 2020**

Design 1:
Design a RC phase shift oscillator to oscillate at 600Hz. Supply voltage is given as 10V.

Solution:
Step 1: Circuit diagram and selection of transistor.

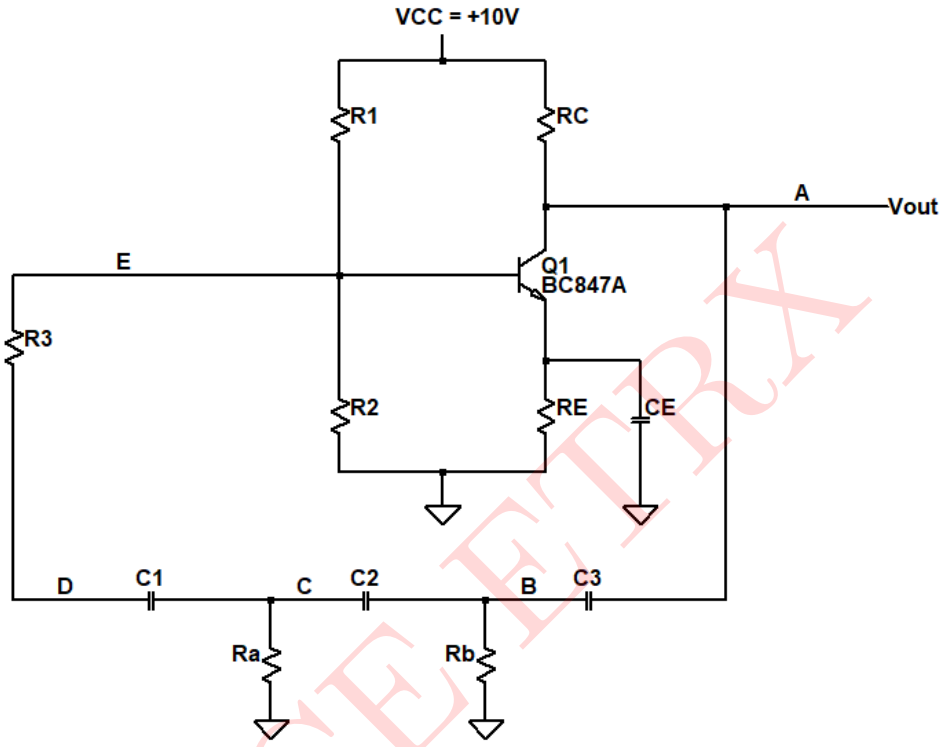

Figure 1: Circuit diagram

Here, $R_a = R_b$ and $R_3 > R_a$, R_b

$C_1 = C_2 = C_3 = C$ and $\beta = 180$

Select transistor BC147A
$h_{fe} = 220$, $h_{ie} = 2.7k\Omega$, $h_{FE} = 180$, $V_{CE(sat)} = 0.25$

Step 2: Selection of R and C:

For RC phase shift oscillators, $f = \dfrac{1}{2\pi RC\sqrt{6+4k}}$

where k $= \dfrac{R_C}{R}$

Minimum value of k is 2.7

$$\therefore 600 = \frac{1}{2\pi RC\sqrt{6+4(2.7)}}$$

$$\therefore RC = \frac{1}{2\pi \times 600 \times \sqrt{6+4(2.7)}}$$

Assuming C = 0.01μF,

$$\therefore R = \frac{1}{2\pi(600)(0.01\mu F)(\sqrt{6+4(2.7)})}$$

$$\therefore R = 6.4716k\Omega$$

Choosing higher standard value, $R = 6.8k\Omega$, 1/4W

Step 3: Selection of R_C:

We know, $k = \frac{R_C}{R}$

$$\therefore R_C = kR$$

$$\therefore R_C = 2.7(6.8k\Omega)$$

$$\therefore R_C = 18.36k\Omega$$

Choosing higher standard value, $R_C = 22k\Omega$, 1/4W

Step 4: Selection of R_E:

$V_E = 10\%$ of V_{CC} for good stability

$$\therefore V_E = 0.1(10)$$

$$\therefore V_E = 1$$

For maximum symmetrical output voltage swing, select Q-point at the centre of DC load line.

$$V_{CEQ} = 0.5V_{CC} = 0.5(10)$$

$$\therefore V_{CEQ} = 5V$$

Applying KVL to C-E loop:

$$I_{CQ} = \frac{V_{CC} - V_{CEQ} - V_E}{R_C}$$

$$\therefore I_{CQ} = \frac{10 - 5 - 1}{22k\Omega}$$

$$\therefore I_{CQ} = 0.1818mA$$

$$\therefore I_{BQ} = \frac{I_{CQ}}{\beta} \quad ...(\because I_{CQ} = \beta I_{BQ})$$

$$\therefore I_{BQ} = \frac{0.1818mA}{180} = 1.0101\mu\text{A}$$

Also, $I_{EQ} = (\beta + 1)I_{BQ}$

$\therefore I_{EQ} = 181(1.0101\mu A) = 0.1828mA$

$V_E = I_{EQ}R_E$

$\therefore R_E = \dfrac{V_E}{I_{EQ}} = \dfrac{1V}{0.1828mA}$

$\therefore R_E = 5.4696k\Omega$

Choosing higher standard value,

$R_E = 4.7k\Omega$, 1/4W

Step 5: Selection of R_1 & R_2:

Let S = 8,

$$\therefore S = \frac{\beta + 1}{1 + \beta \times \left[\dfrac{R_E}{R_B + R_E}\right]}$$

here, $R_B = R_1 \parallel R_2$

$$\therefore 8 = \frac{180 + 1}{1 + \left[\dfrac{180 \times 4.7k\Omega}{4.7k\Omega + R_B}\right]}$$

On solving, $R_B = 34.4214k\Omega$ ...(1)

Also, $V_B = \dfrac{R_2 \times V_{CC}}{R_1 + R_2}$

Applying KVL to B-E loop:

$$V_B = \left(\frac{I_{CQ}}{\beta}\right) R_B + V_{BE(ON)} + I_{EQ}R_E$$

$$\therefore V_B = \left(\frac{0.1818mA}{180}\right)(34.4214k\Omega) + 0.7 + (0.1828mA)(4.7k\Omega)$$

$\therefore V_B = 1.5939V$

From (1), (2) and (3):

$$R_1 = \frac{34.4214 \times 10}{1.5939} = 215.9571\text{k}\Omega$$

Choosing higher standard value, $\therefore R_1 = 220k\Omega$, 1/4W

From (2), we get:

$$\frac{10 \times R_2}{220k\Omega + R_2} = 1.5939$$

$$\therefore R_2 = 40.8059k\Omega$$

Choosing lower standard value, $R_2 = 39k\Omega$, 1/4W

Step 6: Selection of C_E:

To ensure complete bypass, $X_{CE} \leq \frac{R_E}{10} \leq 0.1R_E$

$$X_{CE} = \frac{1}{2\pi f_L C_E} = 0.1R_E$$

$$\therefore C_E = \frac{1}{2\pi f_L (0.1) R_E} = \frac{1}{2\pi(600)(0.1)4.7k\Omega}$$

$$\therefore C_E = 5.6438 \times 10^{-7} F$$

Choosing higher standard value, $C_E = 1\mu F/25\text{V}$

Step 7: Selection of R_3 in R_C selection:

To avoid loading effect by input impedance of BJT towards R_3,

$$\therefore R_3 = R + R_i$$

here, $R_i = R_1 \parallel R_2 \parallel h_{ie}$

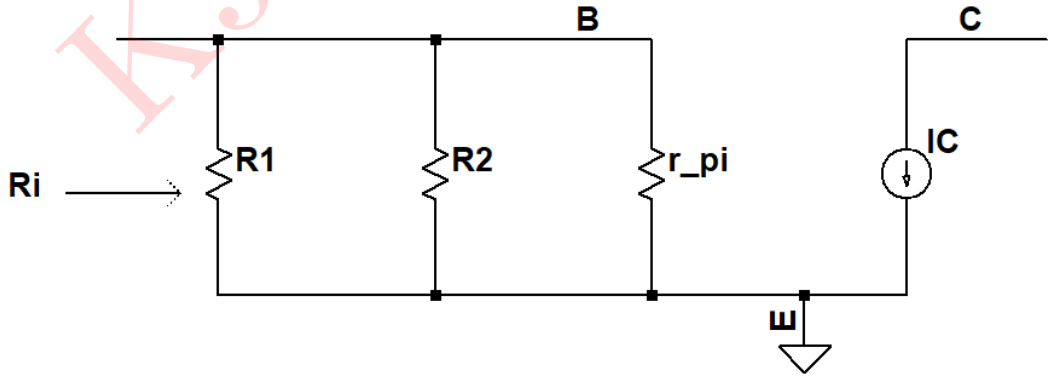

Figure 2: For calculation of R_i

$$\therefore R_i = 220k\Omega \parallel 39k\Omega \parallel 2.7k\Omega \qquad ...h_{ie} = r_\pi$$

$$\therefore R_i = 2.4965k\Omega$$

$R_3 = 6.8k\Omega + 2.4965k\Omega$

$\therefore R_3 = 9.2965k\Omega$

Choosing higher standard value, $R_3 = 10k\Omega$, 1/4W

Step 8: Designed completed circuit:

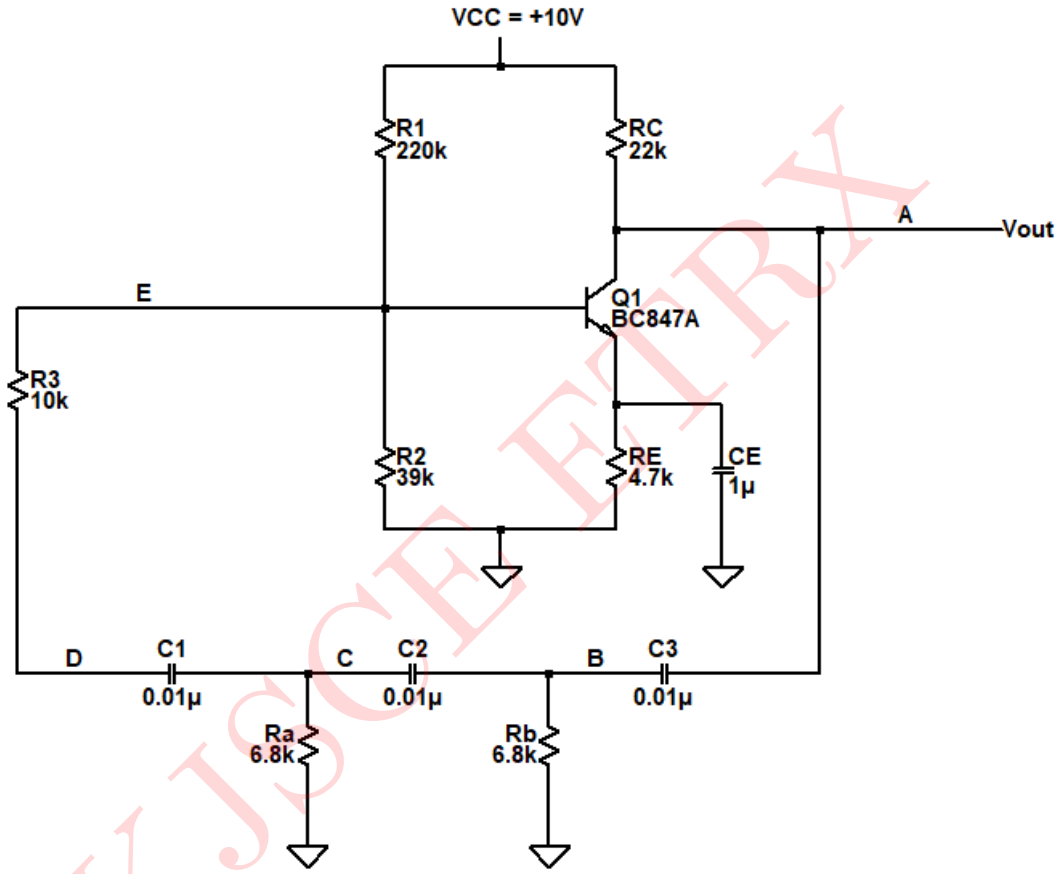

Figure 3: Designed circuit

Frequency of oscillations are given as,

$$f_L = \frac{1}{2\pi RC\sqrt{6+4k}}$$

$$f_L = \frac{1}{2\pi(6.8k\Omega)(0.01\mu F)(\sqrt{6+4(2.7)})}$$

$\therefore f_L = 571.0269Hz$

Time period of oscillations, $T = 1/f_L$

$\therefore T = 1.7512$ ms

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

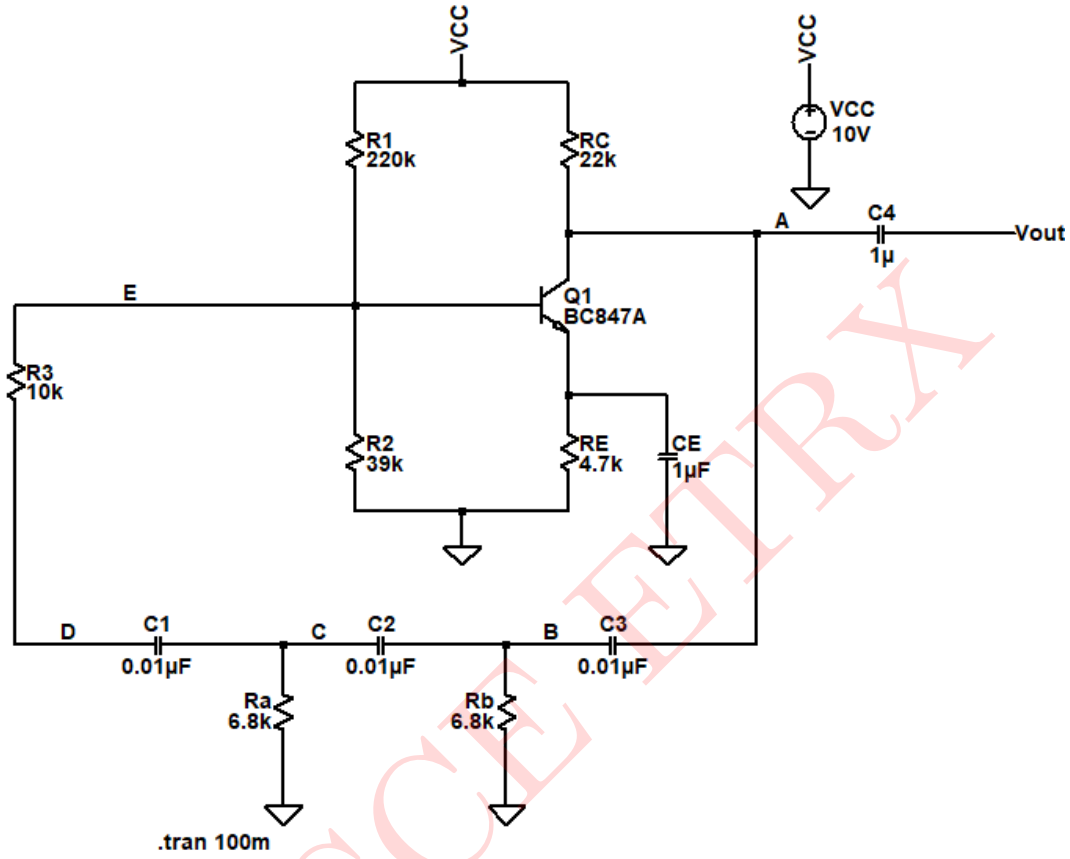

Figure 4: Circuit Schematic: Results

Waveforms observed are shown below:

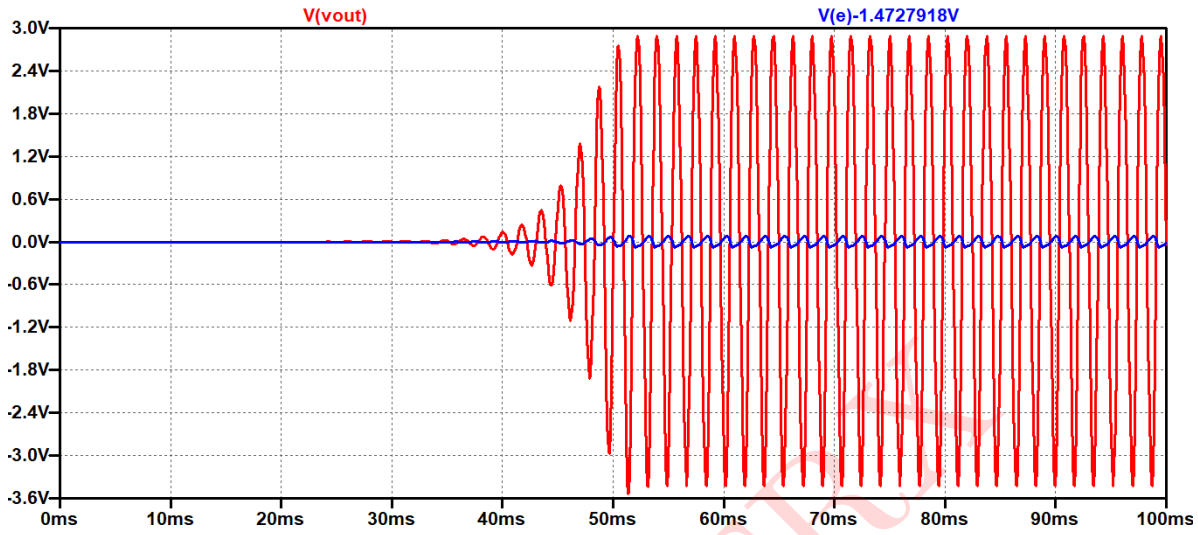

Figure 5: Output oscillations and feedback signal

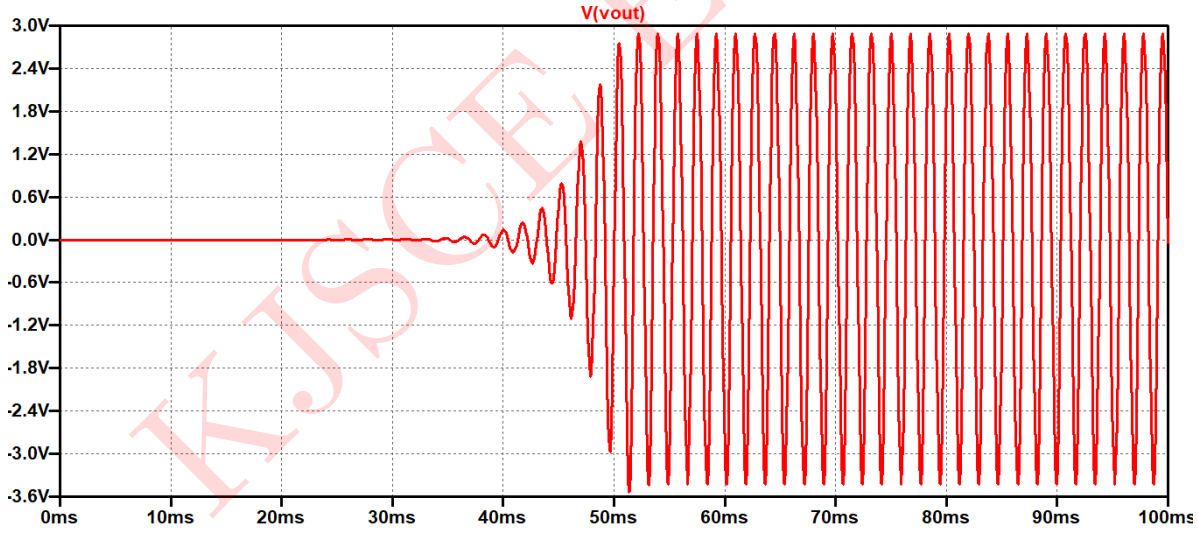

Figure 6: Output oscillations

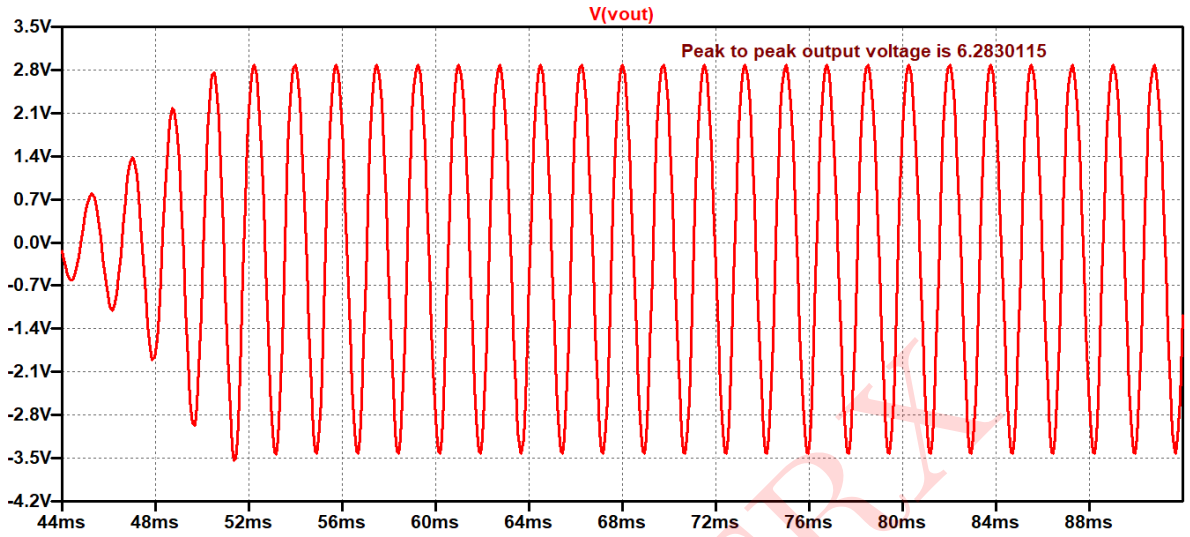

Figure 7: Output oscillations: Zoomed in

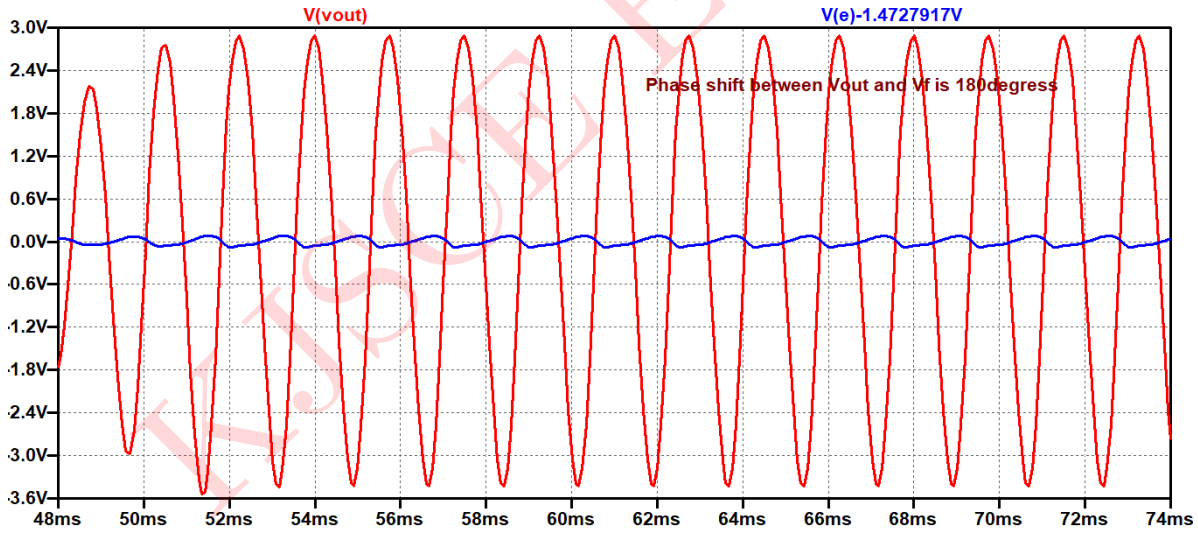

Figure 8: Phase shift between output and feedback signal

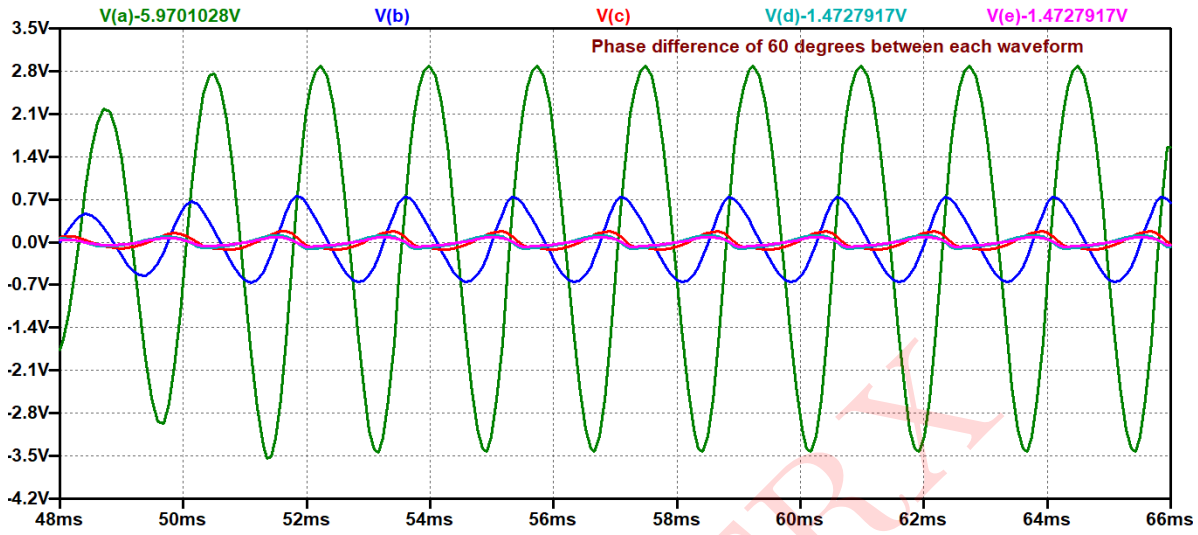

Figure 9: Phase shift between signals from each stage

Comparison between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
Frequency of oscillations (f_L):	571.0269Hz	570.9702Hz
Time period of oscillations:	1.7512 ms	1.7514 ms
Amplitude of oscillations (V_{p-p}):	–	6.2830V
Feedback signal V_f amplitude and new phase w.r.t V_{out}	–	159.2456 mV_{p-p} 180°
Feedback fraction: V_f/V_{out}	0.0253	0.0344
Phase shift offered by feedback network	180 °	180°

Table 1: Numerical 1