# K. J. SOMAIYA COLLEGE OF ENGINEERING DEPARTMENT OF ELECTRONICS ENGINEERING ELECTRONIC CIRCUITS

# Differential Amplifier Circuits

 $15^{th}$  July, 2020

### Numerical 1:

For the differential amplifier shown in figure 1,  $\beta = 100$ , find:

- a. Name of the circuit
- b. Differential voltage gain
- c. Common mode gain
- d. CMRR

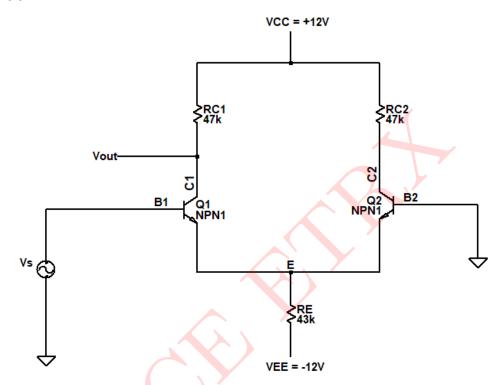


Figure 1: Circuit diagram

**Solution:** Circuit shown in figure 1 is a single input unbalanced output (SIUO) differential amplifier.

DC Analysis: Considering all the internal and external parameters same,

$$V_{CE1} = V_{CE2} = V_{CEQ}$$

Also, 
$$I_{CQ1} = I_{CQ2} = I_{CQ}$$
  
and  $I_{EQ} = I_{EQ1} + I_{EQ2} = 2I_{EQ1}$ 

Applying KVL to B-E loop of Q1:

$$V_{EE} - 2I_E R_E - V_{BE} = 0$$
 ...(:  $I_{EQ} = (\beta + 1)I_{BQ}$ )

$$\therefore V_{EE} - 2(\beta + 1)I_{BQ}R_E - V_{BE} = 0$$

$$\therefore I_{BQ} = \frac{V_{EE} - V_{BE}}{2(\beta + 1)R_E} = \frac{12 - 0.7}{12 \times 101 \times 43k\Omega}$$

$$I_{BQ} = 1.301 \mu A$$

$$I_{CQ} = \beta I_{BQ} = 100(1.301 \mu A)$$

$$I_{CQ} = 0.1301mA$$

$$I_{CQ1} = I_{CQ2} = I_{CQ} = 0.1301 mA$$

Applying KVL to C-E loop of Q1:

$$V_{CC} - I_{CQ}(R_{C1}) - V_{CE1} - 2I_{EQ1}R_E - V_{EE} = 0$$

$$V_{CC} - I_{CQ}(R_{C1}) - V_{CE1} - 2I_{CQ}R_E - V_{EE} = 0$$
 ...(:  $I_{CQ} \approx I_{EQ}$ )

$$V_{CE1} = (V_{CC} - V_{EE}) + I_{CQ}(R_{C1} + 2R_E)$$

$$V_{CE1} = (12 + 12) + (0.1301mA)(47k\Omega + 2 \times 4.3k\Omega)$$

$$V_{CE1} = 6.6967V$$

$$V_{CE1} = V_{CE2} = V_{CE} = 6.6967V$$

Small signal parameters:

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{100 \times 26 mV}{0.1301 mA}$$

$$\therefore r_{\pi} = 19.984k\Omega$$

$$\therefore$$
 Q-point  $\equiv (V_{CE1}, I_{CQ1}) \equiv (6.6967 \text{V}, 0.1301 \text{mA})$ 

Now, 
$$V_{E1} = V_{E2} = R_E(2I_{EQ}) + V_{EE}$$

$$V_{E1} = V_{E2} = (43k\Omega)(2 \times 0.1301mA) - 12 = -0.8114V$$

$$\therefore V_{C1} = V_{CE1} + V_{E1} = 6.6967 + (-0.8114)$$

$$V_{C1} = 5.8853V$$

$$\therefore$$
 Q-point  $\equiv (V_{CEQ1}, I_{CQ1}) \equiv (V_{CEQ2}, I_{CQ2})$ 

: Q-point 
$$\equiv (V_{CEQ}, I_{CQ}) \equiv (6.6967 \text{V}, 0.1301 \text{mA})$$

Differential mode gain:

$$\mid A_d \mid = \frac{1}{2} \times \frac{\beta R_C}{r_\pi + R_B}$$

here,  $R_B = 0\Omega$ 

$$\therefore \mid A_d \mid = \frac{1}{2} \times \frac{100 \times 47k\Omega}{19.984k\Omega + 0}$$

$$\therefore \mid A_d \mid = 117.5941$$

Common mode gain:

$$A_{CM} = \left| \frac{R_C}{2R_E} \right| = \left| \frac{47k\Omega}{2(43k\Omega)} \right|$$

$$\therefore A_{CM} = 0.5465$$

CMRR (Common Mode Rejection Ratio):

$$CMRR = \left| \frac{A_d}{A_{CM}} \right| = \frac{117.5941}{0.5465}$$

CMRR=215.1768

$$CMRR \text{ (in dB)} = 20 \log_{10} \left( \frac{A_d}{A_{CM}} \right) = 20 \log_{10} (215.78)$$

 $\therefore CMRR = 46.5591dB$ 

## SIMULATED RESULTS:

Above circuit was simulated in LTspice and results obtained are as follows:

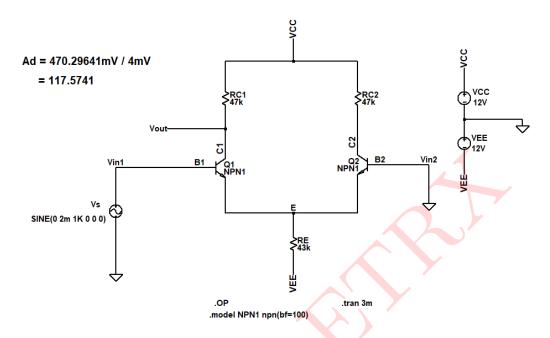


Figure 2: Circuit Schematic: Results for differential mode

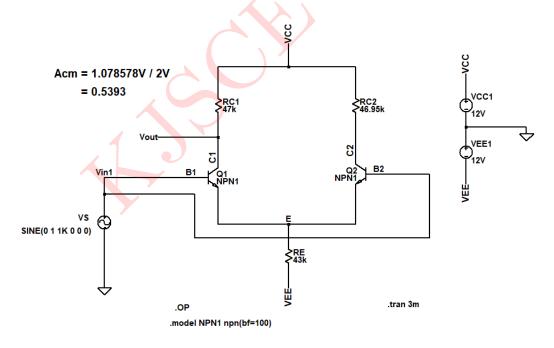


Figure 3: Circuit Schematic: Results for common mode

Input and output waveforms for differential and common mode are shown below:

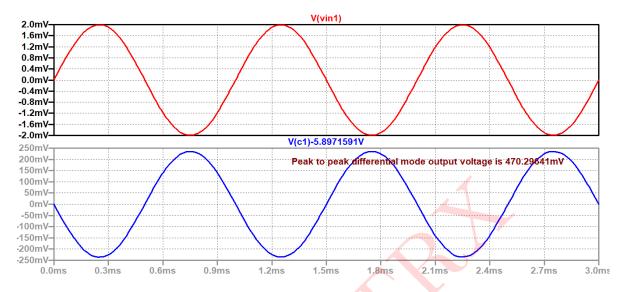


Figure 4: For differential mode

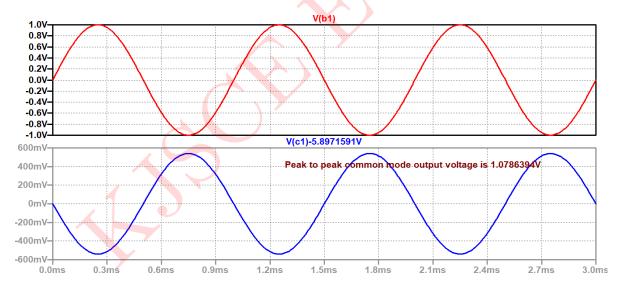


Figure 5: For common mode

# Comparison between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
$I_{C1}, I_{C2}$	$0.1301 \mathrm{mA}$	$0.1298 \mathrm{mA}$
$V_{C1}, V_{C2}$	5.8853V	5.8972
$V_{CE1}, V_{CE2}$	6.6967V	6.6186V
Differential voltage gain $ A_d $	117.5941	117.5814
Common mode voltage gain $ A_{CM} $	0.5465	0.5390
CMRR (in dB)	46.6559	46.7750

Table 1: Numerical 1

### Numerical 2:

For circuit shown in figure 6, determine the following:

- a. Name the circuit
- b. Current flowing through resistor  $R_{D1},\,R_{D2},\,R_{S1}$  and  $R_{S2}$
- c.  $V_{D1}$ ,  $V_{D2}$ ,  $V_{GS1}$ ,  $V_{GS2}$
- d. Differential voltage gain
- e. Common mode gain
- f. CMRR in dB

Assume:  $V_{TN1} = V_{TN2} = 1V$ ,  $k_{N1} = k_{N2} = 50 \mu A/V^2$ 

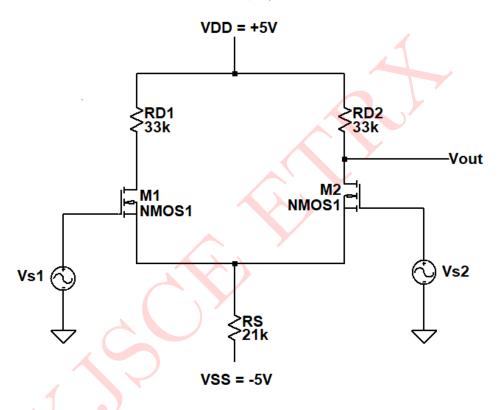


Figure 6: Circuit diagram

**Solution:** Circuit shown in figure 6 is a Dual Input Balanced Output differential amplifier circuit.

## DC Analysis:

Applying KVL to G-S loop of M1:

$$-V_{GSQ1} - 2I_{DQ1}R_S + V_{SS} = 0$$

$$\therefore V_{GSQ1} = V_{SS} - 2I_{DQ1}R_S \qquad \dots (1)$$

Also, for MOSFET in saturation,

$$I_{DQ1} = k_N [V_{GSQ1} - V_{TN}]^2$$

From (1):

$$I_{DQ1} = \frac{5 - V_{GSQ1}}{2R_S}$$

$$\therefore \frac{5 - V_{GSQ1}}{2R_S} = k_N [V_{GSQ1} - V_{TN}]^2$$

Substituting values:

$$\frac{5 - V_{GSQ1}}{2(21k\Omega)} = (50 \times 10^{-6})[V_{GSQ1} - 1]^2$$

$$\therefore 5 - V_{GSQ1} = 2.1[V_{GSQ1}^2 + 1 - 2V_{GSQ1}]$$

$$\therefore 2.1V_{GSQ1}^2 - 3.2V_{GSQ1} - 2.9 = 0$$

$$V_{GSQ1} = 2.1624V, -0.63861V$$

$$V_{SQ1} > V_{TN1}$$

$$V_{GSQ1} = 2.1624V$$

$$\therefore I_{DQ1} = \frac{5 - 2.1624}{42k\Omega} = 67.5619\mu A$$

Applying KVL to D-S loop of M1:

$$V_{DD} - I_{DQ}(R_{D1}) - V_{DSQ1} - 2I_{DQ}R_S + V_{SS} = 0$$

$$V_{DSQ1} = (V_{DD} + V_{SS}) + I_{DQ}[R_{D1} + 2R_S]$$

$$\therefore V_{DSQ} = (5+5) + (67.5619\mu A)[33k\Omega + 42k\Omega]$$

$$V_{DSO1} = 4.9329V$$

Now, 
$$V_{D1} = V_{D2} = V_D = V_{DD} - I_{DQ}R_D$$

$$V_D = 5 - (67.5619\mu A)(33k\Omega)$$

$$V_D = 2.7705V$$

Also, 
$$I_S = \frac{V_S - V_{SS}}{21k\Omega}$$
 ...(2)

We know,  $V_D = 2.7705$ 

$$\therefore V_{DS} = V_D - V_S$$

$$V_S = V_D - V_{DS} = 2.7705 - 4.9329$$

$$V_S = -2.1624$$

From (2),

$$I_S = \frac{-2.1624 + 5}{21k\Omega} = 0.1351mA$$

Due to symmetry of the circuitry,

$$I_{DQ1} = I_{DQ2} = I_{DQ}, V_{GSQ1} = V_{GSQ2} = V_{GSQ}$$

and 
$$V_{DSQ1} = V_{DSQ2} = V_{DSQ}$$

Small signal parameters:

$$g_m = 2k_N[V_{GSQ} - V_{TN}]$$

$$\therefore g_m = 2(50 \times 10^{-6})[V_{GSQ} - 1]$$

$$\therefore g_m = 100 \times 10^{-6} (1.1624)$$

$$\therefore g_m = 0.11624 mA/V$$

Differential gain:

$$A_d = 0.5 \times g_m \times R_D = 0.5(0.11624 \times 10^{-3})(33k\Omega)$$

$$A_d = 1.9180$$

Common mode gain:

$$A_{CM} = \left| \frac{g_m R_D}{1 + 2g_m R_S} \right| = \left| \frac{(0.11624 \times 10^{-3})(33k\Omega)}{1 + 2(0.11624 \times 10^{-3})(21k\Omega)} \right|$$

$$\therefore A_{CM} = \frac{3.83592}{5.8821} = 0.6521$$

$$CMRR = \begin{vmatrix} A_d \\ A_{CM} \end{vmatrix} = \frac{1.9180}{0.6521} = 3.0363$$

$$\therefore CMRR \text{ (in dB)} = 20 \log_{10} \left( \frac{A_d}{A_{CM}} \right) = 20 \log_{10}(3.0363)$$

$$\therefore CMRR = 9.6470 dB$$

### SIMULATED RESULTS:

Above circuit was simulated in LTspice and results obtained are as follows:

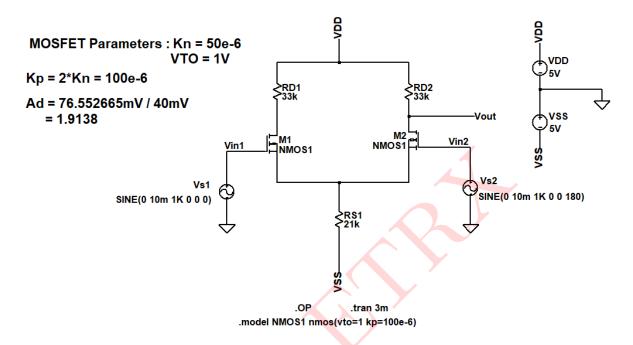


Figure 7: Circuit Schematic: Results

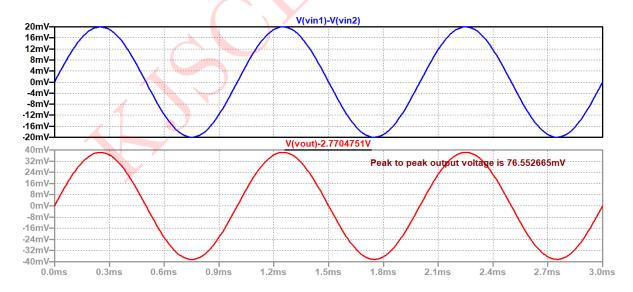


Figure 8: Input and output voltage waveform

# Comparison between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
$I_S,I_{D1},I_{D2}$	$0.1351 \text{mA}, 67.5619 \mu \text{A},$	$0.1351 \text{mA}, 67.5614 \mu\text{A},$
	$67.5619 \mu A$	$67.5614 \mu A$
$V_{D1}, V_{D2}, V_{GS1}, V_{GS2}$	2.7705V, 2.7705V,	2.7705V, 2.7705V
	2,1624V, 2.1624V	2.1624V, 2.1624V
Differential gain: $ A_d $	1.9180	1.9134
Common mode gain: $ A_{CM} $	0.65821	_
CMRR (in dB)	$9.6470\mathrm{dB}$	_

Table 2: Numerical 2

### Numerical 3:

For differential amplifier circuit shown in figure 9,  $k_{N1}=k_{N2}=30\mu A/V^2$ ,  $V_{TN1}=V_{TN2}=0.7V$ . Find: a.  $I_{D1},\,I_{D2},\,V_{D1}$  and  $V_{D2}$  b.  $A_d$ 

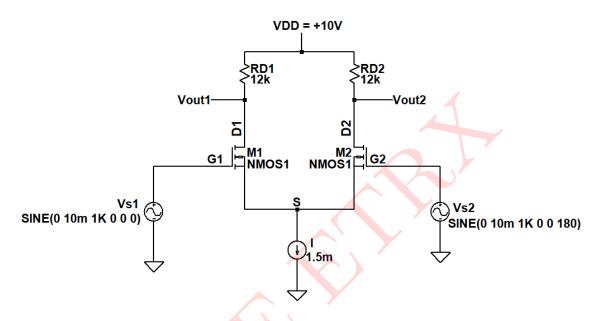


Figure 9: Circuit diagram

**Solution:** Circuit shown in figure 9 is Dual Input Balanced Output (DIBO) differential amplifier.

$$I_{D1} = I_{D2} = \frac{1.5mA}{2} = 0.75mA$$

Also, 
$$V_{D1} = V_{DD} - I_{D1}R_{D}$$

$$V_{D1} = 10 - (0.75mA)(12k\Omega)$$

$$\therefore V_{D1} = 1V$$

Due to symmetry of circuit,

$$V_{D1} = V_{D2} = 1V$$

For MOSFET in saturation,

$$g_m = 2k_N[V_{GS} - V_{TN}]$$
 ...(2)

From (1) and (2):

$$g_m = 2\sqrt{I_D k_N}$$

$$\therefore g_m = 2\sqrt{(0.75mA)(30\mu A/V^2)}$$

$$\therefore g_m = 0.3mA/V^2$$

From (2):

$$g_m = 2k_N[V_{GS} - V_{TN}]$$

$$\therefore 0.3 \times 10^{-3} = 2 \times 30 \times 10^{-6} [v_{GS} - 0.7]$$

$$\therefore V_{GS} = \frac{0.3 \times 10^{-3}}{2 \times 30 \times 10^{-6}} + 0.7$$

$$\therefore V_{GS} = 5.7V$$

$$\therefore V_{GSQ1} = V_{GSQ2} = 5.7V$$

Differential gain:

$$A_d = -g_m R_D = -(0.3 \times 10^{-3})(12k\Omega)$$

$$A_d = -3.6$$

### SIMULATED RESULTS:

Above circuit was simulated in LTspice and results obtained are as follows:

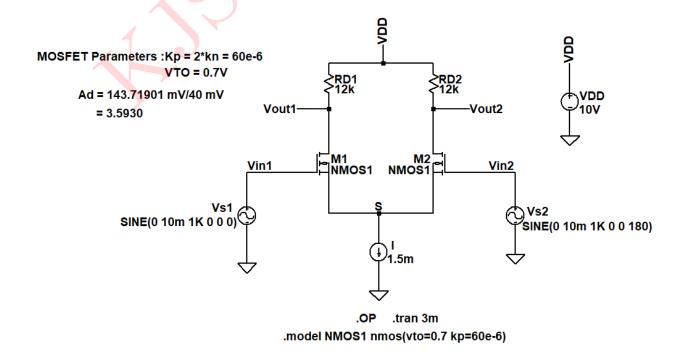


Figure 10: Circuit Schematic: Results

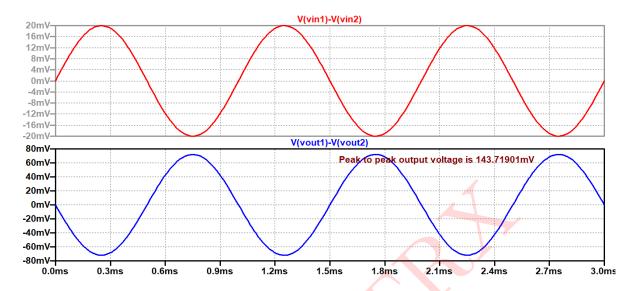


Figure 11: Input and output voltage waveform

# Comparison between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
$I_{D1}, I_{D2}$	$0.75 \mathrm{mA}$	$0.75 \mathrm{mA}$
$V_{D1}, V_{D2}$	1V	1V
Differential gain: $ A_d $	3.6	3.5930

Table 3: Numerical 3