K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
DC Biasing Circuits

1. For the given circuit shown in figure 1. Find V_G, I_D, V_{GS} and V_{DS}. Also, determine the region of operation of the given device.

   Given data: $V_{GS_{(th)}} = 5V$, $V_{GS_{(ON)}} = 10V$, $I_{D_{(ON)}} = 3mA$

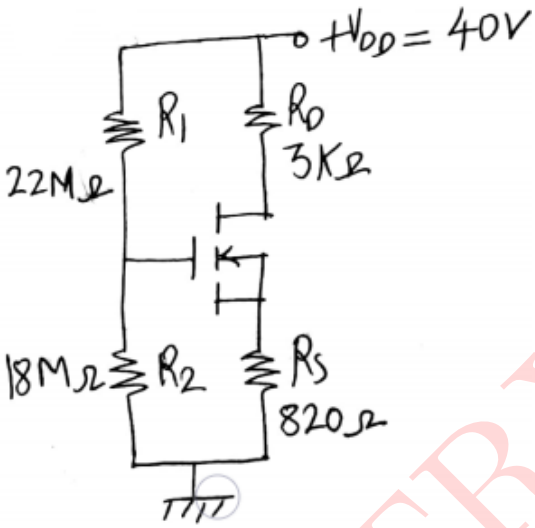

Figure 1: Mosfet Circuit

Solution:

Using zero-temperature drift biasing technique

1.) Data:

$| A_v | = 10$, $V_o = 2V$, $f_L = 20Hz$

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{18M\Omega}{18M\Omega + 22M\Omega} \times 40 = 18V$$

For E-NMOS transistor,

$$k_n = \frac{I_{D_{(ON)}}}{\left[V_{GS_{(ON)}} - V_{GS_{(th)}}\right]^2} = \frac{3mA}{[10-5]^2}$$

$$k_n = 0.12\ mA/V^2$$

V_{GS} is given by,

$$V_{GS} = V_G - V_S = V_G - I_D R_S$$

$$V_{GS} = 18 - I_D(820) \qquad .....(1)$$

Assuming that the given E-NMOS transistor is working in the saturation region,

$$I_D = k_n \left(V_{GS} - V_{GS_{(th)}}\right)^2$$

$$I_D = 0.12 \times 10^{-3}(V_{GS} - 5)^2 \qquad .....(2)$$

Substituting Eq.(2) in Eq.(1), we get

$V_{GS} = 18 - 820 \times 0.12 \times 10^{-3}(V_{GS} - 5)^2$

$V_{GS} = 18 - 0.0984(V_{GS}^2 - 10V_{GS} + 25)$

$V_{GS} = 18 - 0.0984V_{GS}^2 + 0.984V_{GS} - 2.46$

i.e. $0.0984V_{GS}^2 + 0.016V_{GS} - 15.54 = 0$

Solving the above quadratic equation we get,

$V_{GS} = 12.48V$ or $V_{GS} = -12.64V$

Since $V_{GS} < V_{GS_{(th)}}$ for $V_{GS} = -12.64V$, it is rejected.

$\therefore \mathbf{V_{GS} = 12.48V}$

i.e. $I_D = k_n(V_{GS} - 5)^2 = 0.12 \times 10^{-3}(12.48 - 5)^2$

$\therefore \mathbf{I_D = 6.72mA}$

Now, $V_{DS} = V_{DD} - I_D(R_D + R_S) = 40 - 6.72mA(3k + 820)$

$\therefore \mathbf{V_{DS} = 14.32V}$

$\because V_{GS} > V_{GS_{(th)}}$ & $V_{DS} > V_{GS} - V_T$ i.e $V_{DS} > (12.48 - 5)$

$\therefore$ **the given E-NMOS device is working in the saturation region**

2. Design a E-NMOS DC biasing circuit to give $I_D = 0.25mA$, $V_{DS_Q} = 4V$, $V_{R_S} = 1V$. The mosfet parameters are $k'_n = 80\mu A/V^2$, $W/L = 4$, $V_{TN} = 1.2V$. The current in the bias resistors (R_1 & R_2) should be approximately $20\mu A$. $V_{DD=} + 5V$ and $V_{SS} = -5V$

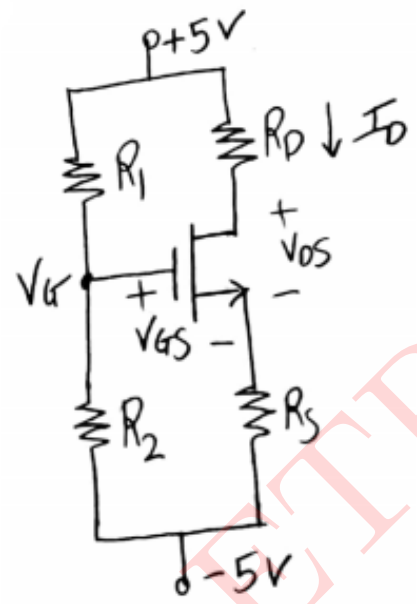

Figure 2: DC Biasing Circuit

Solution:

From figure 2, we have

$V_{R_S} = R_S I_{D_Q}$

$$R_S = \frac{V_{R_S}}{I_{D_Q}} = \frac{1V}{0.25mA} = 4k\Omega$$

Select $\mathbf{R_S = 3.9k\Omega_{(std)}}$, 1/4 W.....(L.S.V)

Applying KVL to D-S loop we get,

$V_{DD} - I_{D_Q} R_D - V_{DS} - I_{D_Q} R_S + V_{SS} = 0$

$\therefore 5 - I_{D_Q}(R_D + R_S) - 4 + 5 = 0$

$I_{D_Q} = 0.25mA$.....(given)

$R_S = 3.9k\Omega$ & $R_D = 20.1k\Omega$

Select $\mathbf{R_D = 22k\Omega_{(std)}}$, 1/4 W.....(H.S.V)

$I_D = k_n(V_{GS} - V_T)^2$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

$$0.25mA = \frac{80\mu}{2} \times 4^2 \times (V_{GS} - 1.2)^2$$

$1.5625 = (V_{GS} - 1.2)^2$

$\therefore \mathbf{V_{GS} = 2.45V}$

$\because$ Current through bias resistor is $20\mu A$

$$R_1 + R_2 = \frac{V_{DD} + V_{SS}}{I_{R_1+R_2}} = \frac{5+5}{20\mu A} = 500k\Omega$$

$$V_G = \left[\frac{R_2}{R_1 + R_2}(5+5)\right] - 5$$

$$V_G = \frac{R_2 \times 10}{500k} - 5$$

$V_S = I_D R_S - 5$

Since, we know that $V_{GS} = V_G - V_S$

$$2.45 = \left[\frac{R_2 \times 10}{500k} - 5\right] - [3.9k \times 0.25mA - 5]$$

$$2.45 = \frac{R_2}{50k} - 5 - 0.975 + 5$$

$$3.425 = \frac{R_2}{50k}$$

$\therefore R_2 = 171.25k\Omega$

Select $\mathbf{R_2 = 150k\Omega_{(std)}}$, 1/4W.....(L.S.V)

$R_1 = 328.75$ kΩ .....$(\because R_1 + R_2 = 500k)$

Select $\mathbf{R_1 = 330k\Omega_{(std)}}$, 1/4W.....(H.S.V)

The designed MOSFET Biasing Circuit is shown in the figure below

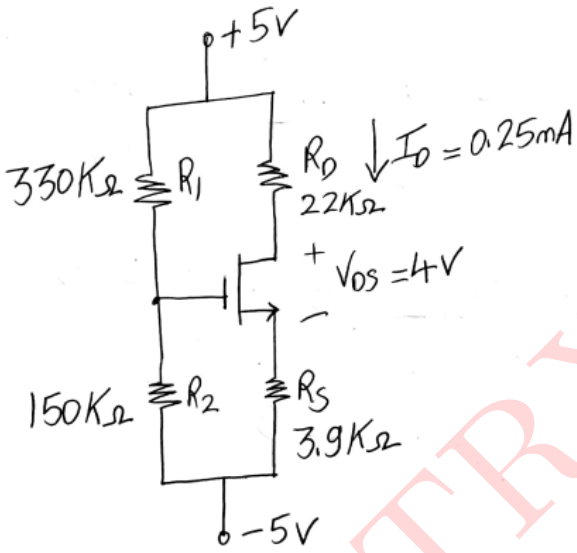

Figure 3: Designed MOSFET Biasing Circuit

3. Design a single stage CS JFET amplifier to give output voltage of $2V$ and voltage gain of -10. The circuit should be suitable for operation upto frequency of $20Hz$
Note: If frequency is not given, then assume it to be $50Hz$

Solution: Using zero-temperature drift biasing technique for designing the circuit.

1) Data:

$| A_v | = 10$, $V_o = 2V$, $f_L = 20Hz$

2) Selection of JFET:

We select n-JFET BFW11 for the datasheet with the following specifications:
$g_{m_o} = 5600\mu\mho$, $V_p = -2.5V$, $r_d = 50k\Omega$ and $I_{DSS} = 7mA$

3) Selection of Biasing Network:

We select self-bias circuit shown in figure 4 for our design.

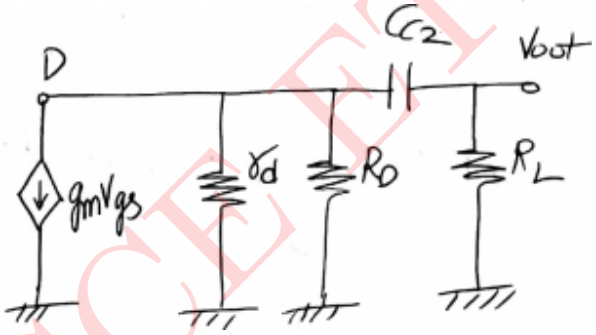

Figure 4: JFET Self-Biasing Circuit

4) Selection of Q-point:

i) For zero-temp drift, $| V_p | - | V_{GS} | = 0.63$

$$2.5 - | V_{GS} | = 0.63$$

$\therefore | V_{GS} | = 1.87$

i.e. $\mathbf{V_{GS} = -1.87V}$

ii) $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_p}\right)^2 = 7mA\left(1 - \dfrac{(-1.87)}{(-2.5)}\right)^2$

$\therefore \mathbf{I_D = 0.44mA}$

iii) $g_m = g_{m_o}\left(1 - \dfrac{V_{GS}}{V_p}\right) = 5600 \times 10^{-6}\left(1 - \dfrac{(-1.87)}{(-2.5)}\right)$

$\therefore \mathbf{g_m = 1.4112mA/V}$

5) Selection of $\mathbf{R_S}$:

$V_{GS} = -R_S I_D$.....(Self-Bias)

i.e. $R_S = \dfrac{-V_{GS}}{I_D} = \dfrac{-(-1.87)}{0.44mA} = 4.25k\Omega$

Select L.S.V to maintain Q-point in middle of transfer curve.

$\therefore$ **Select $\mathbf{R_S = 3.9k\Omega_{(std)}, 1/4W}$**

6) Selection of $\mathbf{R_D}$

$A_v = -g_m(r_d \,||\, R_D)$

Note: If R_L is given, then $A_v = -g_m(r_d \,||\, R_D \,||\, R_L)$

$A_v = -g_m \left(\dfrac{r_d R_D}{r_d + R_D}\right)$

$\therefore -10 = -1.4112 \times 10^{-3} \left(\dfrac{50k\Omega \times R_D}{50k\Omega + R_D}\right)$

Solving the above equation we get,

$R_D = 8.256k\Omega$

Select H.S.V to increase the gain,

$\therefore$ **Select $\mathbf{R_D = 9.1k\Omega_{(std)}, 1/4W}$**

7) Selection of $\mathbf{R_G}$:

To prevent loading of preceding stage,

Select $\mathbf{R_G = 1M\Omega_{(std)}, 1/4W}$

8) Selection of $\mathbf{V_{DD}}$:

$V_{DS} \geqslant V_{o_{peak}} + |\, V_p \,|$.....(Condition for undistorted output)

$V_{DS} = 1.5(V_{o_{peak}} + |\, V_p \,|)$

$\mathbf{V_{DS} = 1.5(V_{o_{peak}} + 2.5)}$

The value is multiplied by 1.5 to take care of saturation voltages, tolerance in resistance value, variation in supply voltage and device parameter variation.

$V_{o_{rms}} = 2V$

$\therefore V_{o_{peak}} = 2\sqrt{2}$

i.e. $V_{DS} = 1.5(2\sqrt{2} + 2.5) = 7.99V$

$\therefore \mathbf{V_{DS} = 8V}$

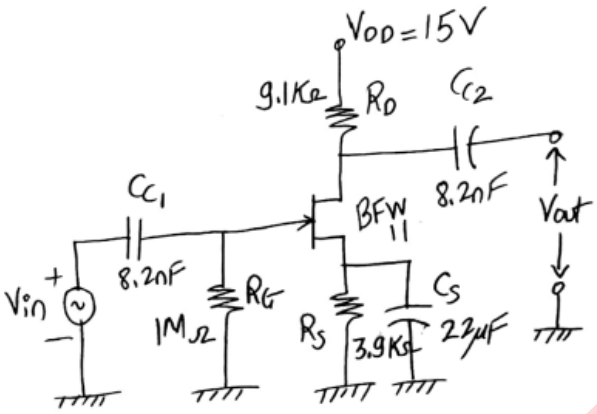

Figure 5: JFET Circuit

Applying KVL to the D-S loop shown in figure 5 we get,

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$V_{DD} = V_{DS} + I_D(R_D + R_S)$

$V_{DD} = 8 + 0.44 \times 10^{-3}(3.9k + 9.1k)$

$\therefore V_{DD} = 13.72V$

Select $\mathbf{V_{DD}} = \mathbf{15V}$

9) Selection of $\mathbf{C_S}$:

$f_L = 20Hz$

$X_{C_S} \leq 0.1R_S$

i.e. $\dfrac{1}{2\pi f_L C_S} \leq 0.1R_S$

i.e. $C_S \geq \dfrac{1}{2\pi f_L \times 0.1R_S} \geq \dfrac{1}{2\pi \times 20 \times 0.1 \times 3.9k}$

$\therefore C_S = 20.4\mu F$

Select $\mathbf{C_S} = \mathbf{22\mu F/25V}$.....(H.S.V)

10) Selection of C_{C1}:

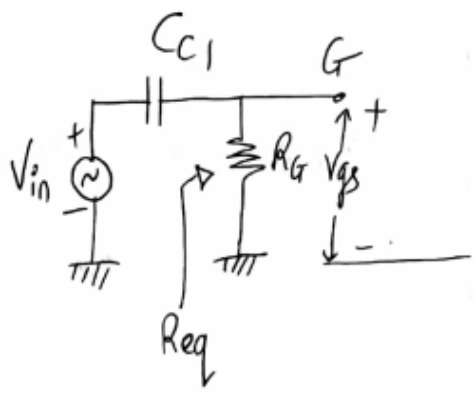

Figure 6: JFET Small Signal Equivalent Input Circuit

$$C_{C1} = \frac{1}{2\pi f_{L_{C_{C1}}} R_{eq}}$$

$$f_{C_{C1}} = f_L = 20Hz$$

$$R_{eq} = R_G = 1M\Omega$$

$$C_{C1} = \frac{1}{2\pi \times 20 \times 1M\Omega} = 7.957nF$$

Select C_{C1} = 8.2nF/25V....(H.S.V)

11) Selection of C_{C2}:

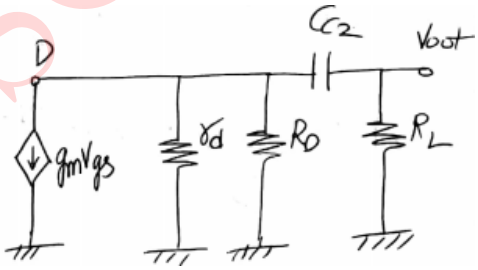

Figure 7: JFET Small Signal Equivalent Output Circuit

$$C_{C2} = \frac{1}{2\pi f_{L_{C_{C2}}} R_{eq}}$$

$$R_{eq} = r_d \,||\, R_D + R_L$$

If R_L is not given, Select $R_L = R_i(nextstage)$

$$R_L = R_G = 1M\Omega$$

$$R_{eq} = 9.1k \,||\, 50k + 1M\Omega$$

$$R_{eq} = 7.698k + 1M\Omega = 1.0077m\Omega$$

$$f_{L_{C_{C2}}} = f_L = 20Hz$$

$$C_{C2} = \frac{1}{2\pi \times 20 \times 1.077M\Omega}$$

$$C_{C2} = 7.89nF$$

Select $\mathbf{C_{C2}}$ = 8.2nF/25V.....(H.S.V)

12) The designed JFET circuit is:

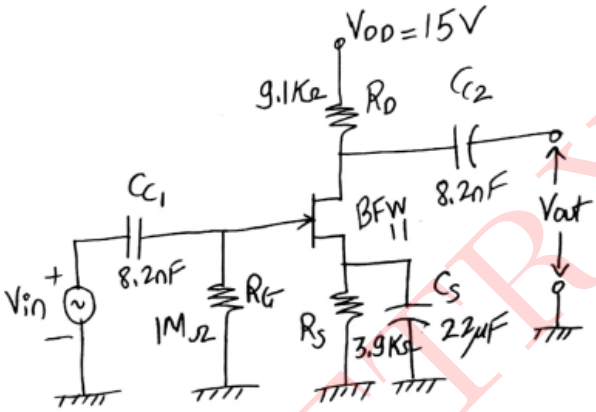

Figure 8: Designed JFET Amplifier Circuit using Zero-temperature Drift Technique

4. For the network shown in figure 9, determine
   a) I_{D_Q} & V_{GS}
   b) V_D & V_S
   c) V_{DS_Q}

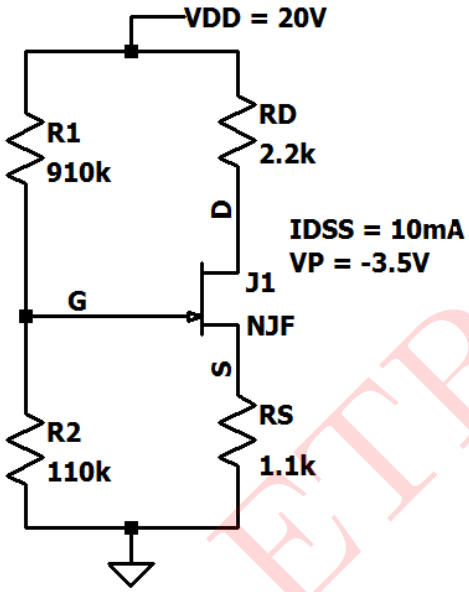

Figure 9: Circuit 1 for Numerical 4

Solution: The circuit given above is a voltage divider biased circuit.

By applying KVL at the G-S loop we get,

$V_G - R_2 I_G - V_{GS} - I_S R_S = 0$

But for JFET, $I_G = 0$

$\therefore I_D = I_S$

From equations (1), (2) and (3) we get,

$V_G - V_{GS} - I_D R_S = 0$

$\therefore V_{GS} = V_G - I_D R_S$ .....(1)

By voltage division rule,

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{110k}{110k + 910k} \times 20$$

$\mathbf{V_G = 2.15V}$

Substituting the value of V_G and R_S in equation (1) we get,

$V_{GS} = 2.15 - I_D(1.1k)$ .....(2)

We know that $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

$\therefore I_D = 10 \times 10^{-3}\left(1 + \frac{V_{GS}}{3.5}\right)^2$ .....(3)

Substituting equation (3) in equation (2) we get,

$$V_{GS} = 2.15 - 11\left(1 + \frac{V_{GS}^2}{12.25} + \frac{2V_{GS}}{3.5}\right)$$

$$\therefore V_{GS} = 2.15 - \left(11 + \frac{11V_{GS}^2}{12.25} + \frac{22V_{GS}}{3.5}\right)$$

$\therefore V_{GS} = -1.487V$ or $V_{GS} = -6.66V$

Accepting the value of $V_{GS} = -1.48V$ because $V_{GS} > V_p$

$\therefore \mathbf{V_{GS} = -1.487V}$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = 10mA\left(1 - \frac{(-1.48)}{(-3.5)}\right)^2$$

$\therefore \mathbf{I_D = 3.307mA}$

We know that $V_{GS} = V_G - V_S$

$\therefore V_S = V_G - V_{GS} = 2.15 + 1.487$

$\therefore \mathbf{V_S = 3.637V}$

Applying KVL to D-S loop we get,

$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$

$\therefore V_{DS} = 20 - 3.307 \times 2.2 - 3.3.07 \times 1.1$

$\therefore \mathbf{V_{DS} = 9.086V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

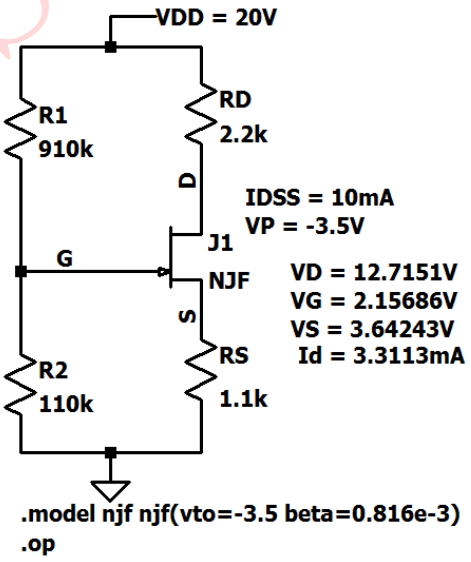

Figure 10: Circuit Schematic: Results

Comparison between observed and theoretical values:

Parameters	**Simulated**	**Theoretical**
V_G	2.15V	2.15V
V_S	3.367V	3.64V
I_D	3.31mA	3.307mA

Table 1: Question 4

5. For the network shown in figure 11, determine
   a) I_{D_Q} & V_{GS_Q}
   b) V_{DS} & V_D

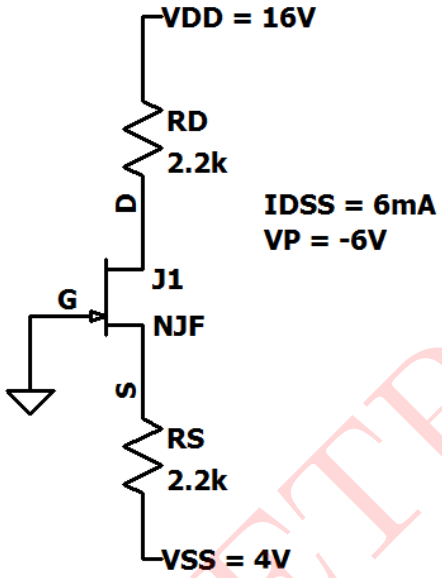

Figure 11: Circuit 1 for Numerical 5

Solution: The circuit given above is common gate configuration.

By applying KVL to the G-S loop we get,

$$0 - V_{GS} - I_S R_S + V_{SS} = 0 \quad \text{.....(1)}$$

But for JFET, $I_G = 0$

$$\therefore I_D = I_S \quad \text{.....(2)}$$

From equations (1) and (2) we get,

$$V_{GS} = V_{SS} - I_D R_S$$

$$\therefore V_{GS} = 4 - I_D(2.2k) \quad \text{.....(3)}$$

We know that $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

Substituting the given values in the formula we get,

$$I_D = 6mA\left(1 + \frac{V_{GS}}{6}\right)^2 \quad \text{.....(4)}$$

Substituting equation (4) in equation (3) we get,

$$V_{GS} = 4 - 13.2\left(1 + \frac{2V_{GS}}{6} + \frac{V_{GS}^2}{36}\right)$$

$$\therefore V_{GS} = 4 - 13.2 - 4.4V_{GS} - 0.3667V_{GS}^2$$

i.e. $0.3667V_{GS}^2 + 5.4V_{GS} + 9.2$

Solving the above quadratic equation we get,

$V_{GS} = -1.966V$ or $V_{GS} = 12.75V$

We will select $-1.966V$ because $V_{GS} > V_p$

$\therefore \mathbf{V_{GS} = -1.966V}$

Assuming the transistor to be in the saturation region,

$$I_D = I_{DSS}\left(1 - \frac{-1.966}{-6}\right)^2$$

$\therefore \mathbf{I_D = 2.71mA}$

Applying KVL to D-S we get,

$V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$

$\therefore V_{DD} + V_{SS} - V_{DS} - I_D(R_D + R_S) = 0$

$\therefore V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S) = 16 + 4 - 2.71mA(2.2k + 2.2k)$

$\therefore \mathbf{V_{DS} = 8.076V}$

We know that, $V_D = V_{DD} - I_D R_D = 16 - 2.71mA \times 2.2k\Omega$

$\therefore \mathbf{V_D = 10.038V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

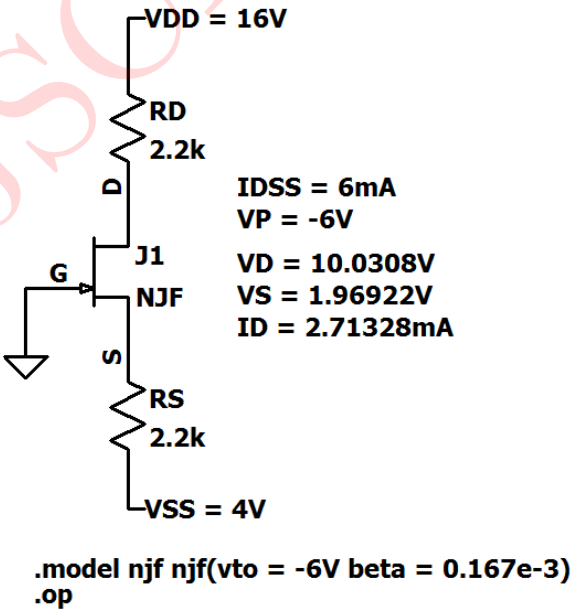

Figure 12: Circuit Schematic: Results

Comparison between observed and theoretical values:

Parameters	**Simulated**	**Theoretical**
V_D	10.038V	10.038V
V_{DS}	8.07V	8.076V
I_D	0.00271A	2.71mA

Table 2: Question 5

6. For the network shown in figure 13, determine
   a) V_{GS_Q} & I_{D_Q}
   b) V_{DS}
   c) V_D & V_S

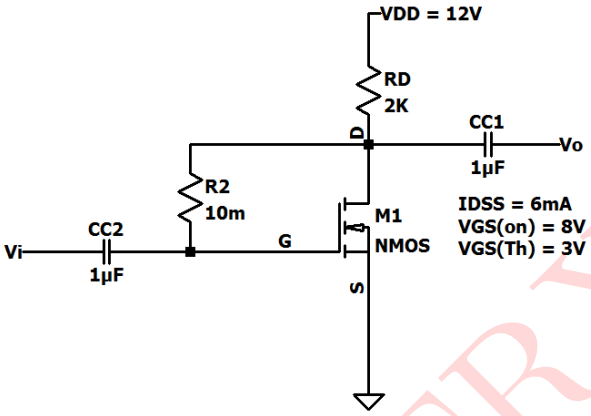

Figure 13: Circuit 1 for Numerical 6

Solution: The circuit 1 is a common gate configuration.

We know that, $V_{GS} = V_G - V_S$

Applying KVL to G-S loop we get,

$V_{GS} = -I_D R_S + V_{SS}$

$\therefore V_{GS} = 10 - I_D(1.5k)$ .....(1)

Also, $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_p}\right)^2$

$I_D = 9mA\left(1 + \dfrac{V_{GS}}{3}\right)^2$ .....(2)

Substituting (2) in (1) we get

$V_{GS} = 10 - 13.5\left(1 + \dfrac{V_{GS}^2}{9} + \dfrac{2V_{GS}}{3}\right)$

$\therefore V_{GS} = \left(-13.5 - \dfrac{13.5V_{GS}^2}{9} - \dfrac{2 \times 13.5V_{GS}}{3}\right)$

$\therefore 1.5V_{GS}^2 + 10V_{GS} + 3.5 = 0$

Solving the above quadratic equation we get,

$V_{GS} = -0.3706V$ or $V_{GS} = -6.296V$

We select $\mathbf{V_{GS} = -0.3706V}$ because $V_{GS} > V_p$

$\therefore I_D = 9mA\left(1 - \dfrac{0.3706}{3}\right)^2$

$\therefore \mathbf{I_D = 6.913mA}$

Applying KVL to D-S loop we get,

$-V_{SS} + I_S R_S + V_{DS} + I_D R_D - V_{DD} = 0$

$V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S) \qquad (\because I_S = I_D),$

$\therefore V_{DS} = 20 + 10 - (6.9mA)(1.8k + 1.5k) = 30 - 22.77$

$\therefore \mathbf{V_{DS} = 7.23V}$

We know that, $V_D = V_{DD} - I_D R_D = 20 - (6.9mA)(1.8k) = 20 - 12.42$

$\therefore \mathbf{V_D = 7.58V}$

$V_{DS} = V_D - V_S$

$\therefore V_S = V_D - V_{DS} = 7.58 - 7.23$

$\therefore \mathbf{V_S = 0.35V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

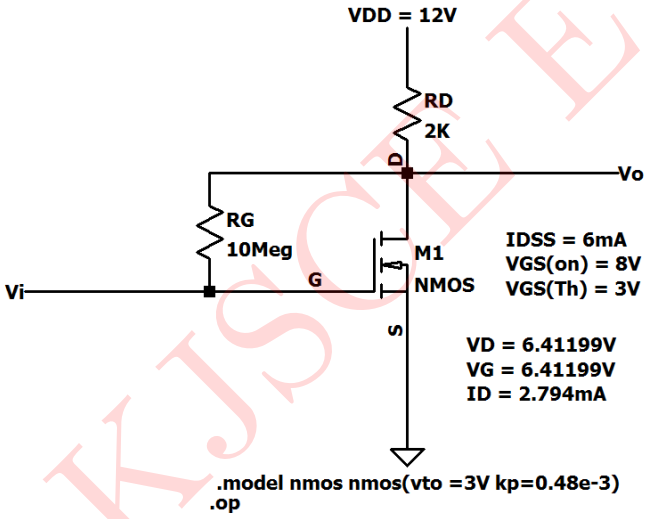

Figure 14: Circuit Schematic: Results

Comparison between theoretical and simulated values is given below:

Parameters	Simulated	Theoretical
V_D	7.55V	7.58V
V_S	0.37V	0.35V
I_D	6.913mA	6.913mA

Table 3: Question 6

7. Find V_{DS_Q} and I_{D_Q} for the enhancement type MOSFET shown in figure 15.

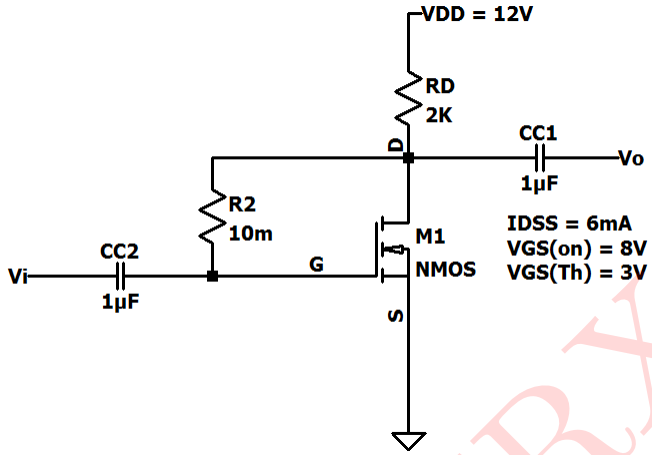

Figure 15: Circuit 1 for Numerical 7

Solution:

Given data: $I_{DSS} = 6mA$

$V_{GS_{(ON)}} = 8V$

$V_{GS_{(Th)}} = 3V$

Solving for k_n we get,

$$k_n = \frac{I_{D_{(ON)}}}{\left[V_{GS_{(ON)}} - V_{GS_{(Th)}}\right]^2} = \frac{6mA}{(8V - 3V)^2}$$

$\therefore k_n = 0.24mA/V^2$

Applying KVL to D-S loop we get,

$V_{GS} = V_{DD} - I_D R_D = 12 - I_D(2000)$ .....(1)

Assuming that the given NMOS-E is in saturation region

$I_D = k_n(V_{GS} - V_{GS_{(ON)}})^2 = 0.24 \times 10^{-3}(V_{GS} - 3)^2$

Substituting (2) in (1) we get,

$V_{GS} = 12 - 0.48(V_{GS} - 3)^2 = 12 - 0.48(V_{GS}^2 - 6V_{GS} + 9)$

$\therefore V_{GS} = 12 - 0.48V_{GS}^2 + 2.88V_{GS} - 4.32$

$\therefore 0.48V_{GS}^2 - 1.88V_{GS} - 7.68 = 0$

Solving the above quadratic equation we get,

$V_{GS} = 6.41V$ or $V_{GS} = -2.49V$

We select $\mathbf{V_{GS} = 6.41V}$

$\mathbf{V_{DS} = V_{GS} = 6.41V}$

$I_D = k_n(V_{GS} - 3)^2 = 0.24 \times 10^{-3}(6.41 - 3)^2$

$\mathbf{I_D = 2.79mA}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

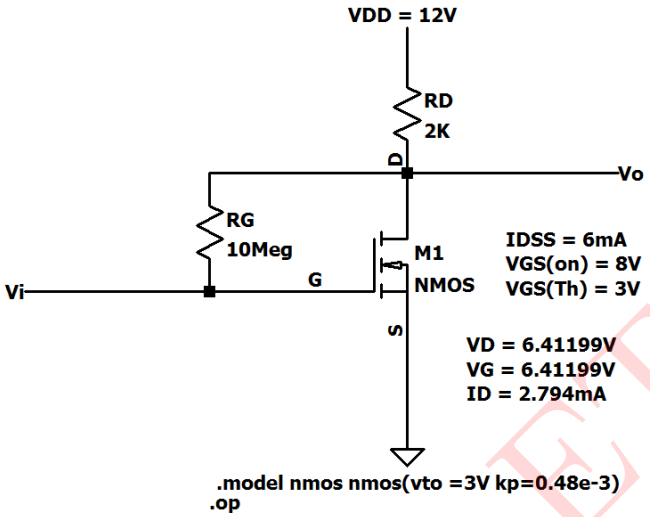

Figure 16: Circuit Schematic: Results

Comparison between observed and theoretical values:

Parameters	Simulated	Theoretical
V_{GS}	6.411V	6.41V
V_{DS}	6.411V	6.41V
I_D	2.794A	2.794mA

Table 4: Question 7

8. The pnp transistor shown in figure 17 has $\beta = 100$ and $V_{EB} = 0.7V$. Find I_B and V_{EC}

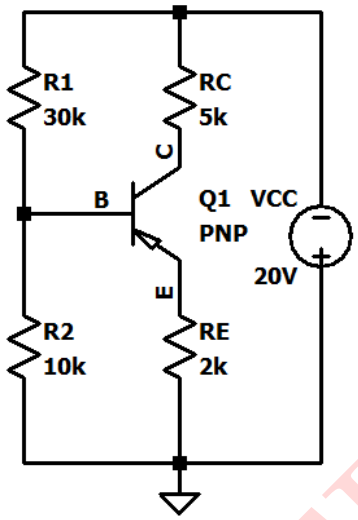

Figure 17: Circuit 1 for Numerical 8

Solution:

Given: $\beta = 100$ and $V_{EB} = 0.7V$

From figure 1 we get,

$R_{th} = R_1 \parallel R_2$

$R_1 = 30k\Omega$ and $R_2 = 10k\Omega$

$R_{th} = 10k \parallel 30k$

$\therefore R_{th} = 7.5k\Omega$

We know that, $V_{th} = \dfrac{R_2}{R_1 + R_2} \times V_{CC} = \dfrac{10k}{10k + 30k} \times (-20)$

$\therefore V_{th} = -5V$

In DC analysis, the capacitors become open circuit,

Applying KVL to E-B loop we get,

$-V_{th} - I_B R_{th} - I_E R_E - V_{EB} = 0$

$-V_{th} - V_{EB} = I_B R_{th} + (1 + \beta) I_B R_E$

$I_B = \dfrac{-V_{th} - V_{BE}}{R_{th} + (1 + \beta) R_E} = \dfrac{-(-5)V - 0.7V}{7.5 + (101)2}$

$\therefore \mathbf{I_B = 20.52\mu A}$

$I_C = \beta I_B = 100 \times 20.52\mu A$

$\therefore \mathbf{I_C = 2.052mA}$

Applying KVL to the E-C loop we get,

$V_{CC} - I_C R_C - V_{EC} - I_E R_E = 0$

$V_{EC} = V_{CC} - I_C R_C - I_E R_E = 20 - (2.052mA)(5k) - (2.072mA)(2k)$

$\mathbf{V_{EC} = 5.596V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

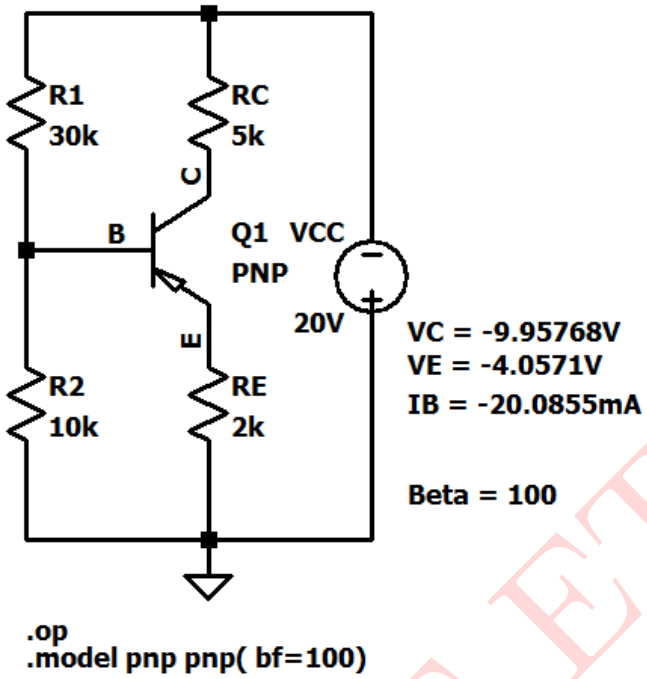

Figure 18: Circuit Schematic: Results

Comparison between theoretical and simulated values is given below:

Parameters	Simulated	Theoretical
I_B	20.0855μA	20.52μA
V_{EC}	5.9V	5.596V

Table 5: Question 8

9. The parameters of the amplifier circuit shown in figure 19 are $V_{CC} = 5V$, $R_c = 500\Omega$, $R_1 = 6.5k\Omega$, $R_E = 450\Omega$, $R_S = 500\Omega$, $R_L = 5k\Omega$ and C_1 & $C_2 = 1\mu F$, $\beta = 100$

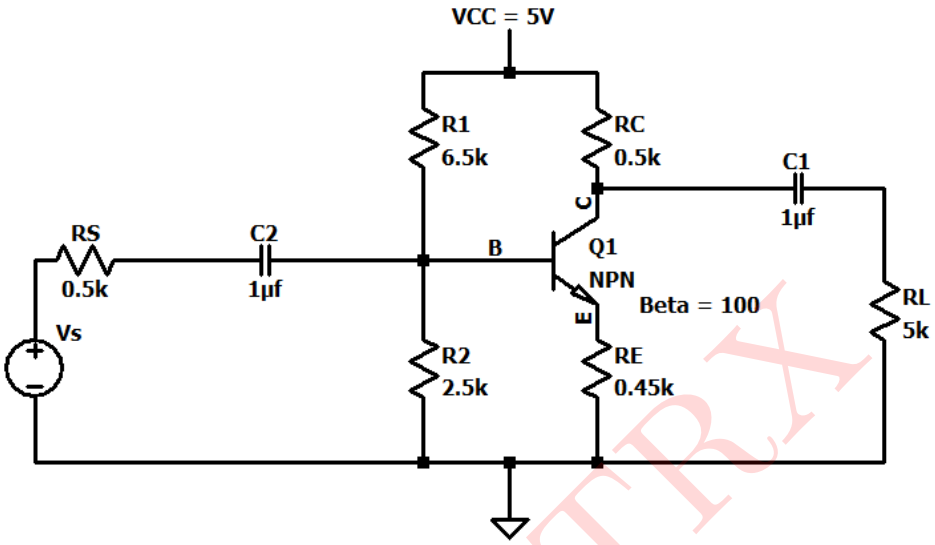

Figure 19: Circuit 1 for Numerical 9

Solution:

From figure 1 we get,

$R_{th} = R_1 \,||\, R_2$

$R_{th} = 6.5k \,||\, 2.5k$

$\therefore R_{th} = 1.80k\Omega$

We know that, $V_{th} = \dfrac{R_2}{R_1 + R_2} \times V_{CC} = \dfrac{2.5}{6.5 + 2.5} \times 5$

$\therefore V_{th} = 1.389V$

In DC analysis, the capacitors become open circuit,

Applying KVL to B-E loop we get,

$V_{th} - I_B R_{th} - I_E R_E - V_{BE} = 0$

$V_{th} - V_{BE} = I_B R_{th} + (1 + \beta) I_B R_E$

$I_B = \dfrac{V_{th} - V_{BE}}{R_{th} + (1 + \beta) R_E} = \dfrac{1.389V - 0.7V}{1.8 + (101)0.45} = \dfrac{0.689}{47.25}$

$\therefore \mathbf{I_B = 14.58\mu A}$

$I_C = \beta I_B = 100 \times 14.58\mu A$

$\therefore \mathbf{I_C = 1.458mA}$

Applying KVL to the C-E loop we get,

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 5 - (1.458mA)(0.5k) - (1.473mA)(0.45k) \quad (\because I_E = I_B + I_C)$

$\mathbf{V_{CE} = 3.61V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

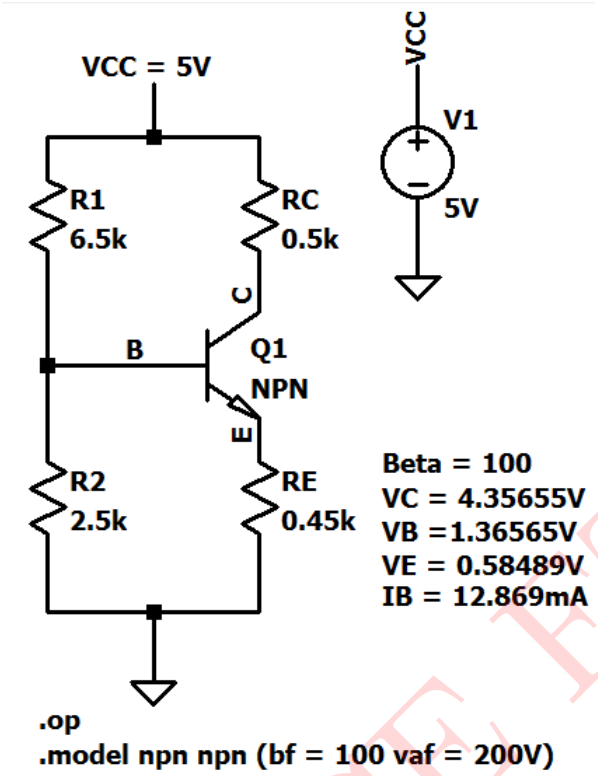

Figure 20: Circuit Schematic: Results

Comparison between theoretical and simulated values is given below:

Parameters	Simulated	Theoretical
I_B	12.869μA	14.58 μA
V_{CE}	3.77V	3.61V

Table 6: Question 9

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