K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Cascade Amplifier

Design 1:
Design a two stage RC coupled cascade amplifier to meet the following specifications:-
$V_{O_{RMS}} = 2.5V$, $R_i \geq 1M\Omega$ and $|A_V| \geq 180$
Select suitable transistor from data-sheet

Solution:

Step 1:- For above experiment, we can use CS-CS self bias JFET Amplifier

$g_{m_o} = 5600\mu A/V$, $V_P = -2.5V$, $r_d = 50k\Omega$ and $I_{DSS} = 7mA$

Step 2:- Selection of voltage gain

$A_V \geq 180$

Lets select $\rightarrow A_V = 190$

Also, let $A_{V_1} = 0.6A_{V_2}$

$\therefore A_V = A_{V_1} \times A_{V_2}$

$190 = 0.6 \times {A_{V_2}}^2$

$A_{V_2} \approx 17.79$

$\therefore A_{V_2} = 18$ and $A_{V_1} = 11$

Design of second stage:-

Step 3:- Calculation of Q-Point($V_{GS_{Q2}}$, I_{DQ_2})

Using mid-point biasing

$$I_D = \frac{I_{DSS}}{2} = 3.5mA$$

In Saturation, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

On rearranging, $V_{GS} = V_p\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) = -2.5 \times \left(1 - \sqrt{\frac{3.5}{7}}\right) = -0.732V$

$\boldsymbol{V_{GS_{Q2}} = -0.732V}$

Step 4:- Selection of R_{D_2}

$|A_{V_2}| = g_m(r_{d_2} \parallel R_{D_2})$ .....(1)

$$g_m = g_{m_2} = g_{m_1} = g_{m_o}\left(1 - \frac{V_{GS}}{V_P}\right) = 5600\mu A/V\left(1 - \frac{0.732}{2.5}\right) = 3.96mA/V$$

$\boldsymbol{g_{m_1} = g_{m_2} = 3.96mA/V}$

$\boldsymbol{r_{d_1} = r_{d_2} = 50k\Omega}$

From equation (1)

$18 = 3.96mA/V(50k \;||\; R_{D_2})$

$$\frac{18}{3.96 \times 10^{-3}} = \frac{50k \times R_{D_2}}{50k + R_{D_2}}$$

$R_{D_2} = 4.99k\Omega \approx 5k\Omega$

Select $\boldsymbol{R_{D_2} = 5.1k\Omega}$, $\boldsymbol{1/4W}$

Step 5:- Selection of $\boldsymbol{R_{S_2}}$

$V_{GS_Q} = -I_{D_Q} R_{S_2}$

$$R_{S_2} = \frac{-V_{GS_Q}}{I_{D_Q}} = \frac{0.732}{3.5mA} = 209\Omega$$

Select $\boldsymbol{R_{S_2} = 180\Omega}$, $\boldsymbol{1/4W}$

Step 6:- Selection of $\boldsymbol{R_{G_2}}$

For present loading for first stage

Select $\boldsymbol{R_{G_2} = 1M\Omega}$, $\boldsymbol{1/4W}$

Step 7:- Calculation of $\boldsymbol{V_{DD}}$

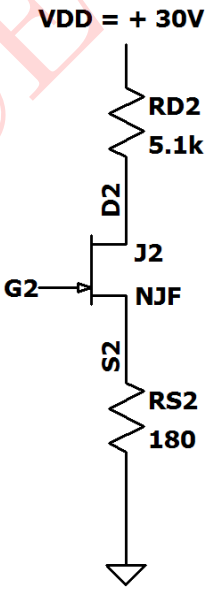

Figure 1: D to S Loop for JFET-2

Applying KVl to the D-S loop for JFET-2, we get,

$V_{DD} - I_{D_Q} R_{D_2} - V_{DS_2} - I_{D_2} R_{S_2} = 0$

$V_{DD} = I_{D_2}(R_{D_2} + R_{S_2}) + V_{DS_2}$

$V_{DS_2} \geq 1.5[|V_p| + V_{o_{peak}}]$

$V_{DS_2} \geq 1.5[2.5 + 2.5(\sqrt{2})]$

$V_{DS_2} \geq 9.053$

$\therefore V_{DS_2} = 9.1V$

$\therefore V_{DD} = 3.5m(0.18k + 5.1k) + 9.1$

$V_{DD} = 27.58V$

Select $\boldsymbol{V_{DD} = 30V}$

Design for first stage:-

Step 8:- Selection of $\boldsymbol{R_{D_1}}$

$|A_{V_1}| = g_m(r_d \parallel R_{D_2})$

$|A_{V_1}| = 3.96(50k \parallel 5.1k) = |8.328|$

$|A_{V_1}| = \dfrac{A_V}{|A_{V_2}|} = \dfrac{190}{|8.318|} = 10.36$

Let, $A_{V_1} = 11$

$|A_{V_1}| = g_{m_1}(r_{d_1} \parallel R_{D_1} \parallel R_{G_2})$

$11 = 3.96(50k \parallel R_{D_1} \parallel 1M)$

$11 = 3.96(47.62k \parallel R_{D_1})$

$11 = \dfrac{47.62k \times R_{D_1}}{47.62k + R_{D_1}}$

$R_{D_1} = 2.9496k\Omega$

Select $\boldsymbol{R_{D_1} = 3.3k\Omega}$, $\boldsymbol{1/4W}$

Step 9:- Selection of $\boldsymbol{R_{S_1}}$

$V_{GS_Q} = -I_{D_1 Q_1} R_{S_1}$

$R_{S_1} = \dfrac{-V_{GS_Q}}{I_{D_Q}}$

$R_{S_1} = \dfrac{0.732}{35mA} = 209.1\Omega$

Select **$\boldsymbol{R_{S_1} = 180\Omega}$, $\boldsymbol{1/4W}$**

Step 10:- Selection of $\boldsymbol{R_{G_1}}$

To avoid loading effect and fulfill the requirement of $R_i \geq 1M\Omega$

Select $\boldsymbol{R_{G_1} = 1M\Omega}$, $\boldsymbol{1/4W}$

Step 11:- Selection of coupling capacitors C_{C_2}, C_{C_1}, C_{C_3}

a) C_{C_1}

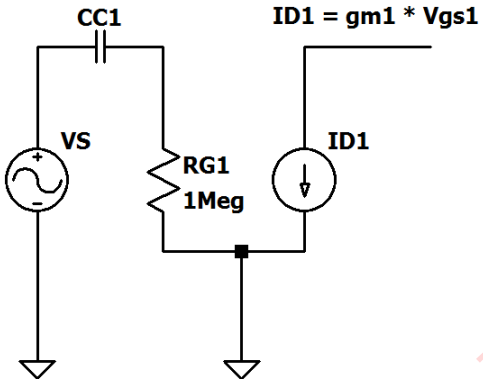

Figure 2: Small Signal low frequency equivalent circuit for C_{C_1}

$$C_{C_1} = \frac{1}{2\pi f_L R_{G_1}}$$

$$C_{C_1} = \frac{1}{2\pi \times 1.2M \times 20} = 6.63nF$$

Select, $\boldsymbol{C_{C_1} = 6.8nF/60V}$

b) C_{C_2}

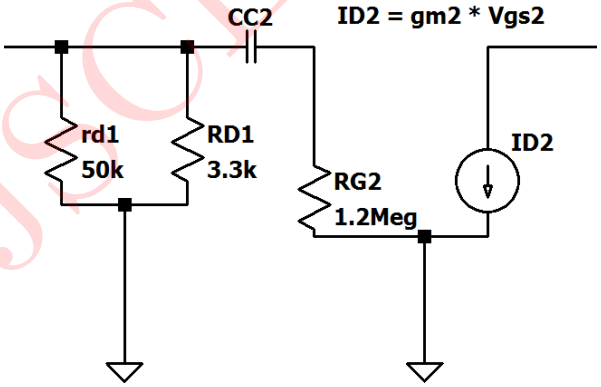

Figure 3: Small Signal low frequency equivalent circuit for C_{C_2}

$$C_{C_2} = \frac{1}{2\pi f_L R_{eq}}$$

$$R_{eq} = (r_{d_1} || R_{D_1}) + R_{G_1}$$

$$R_{eq} = (50k\Omega \;||\; 3.3k\Omega) + 1M\Omega = 3.1k + 1M\Omega = 1.0031M\Omega$$

$$C_{C_2} = \frac{1}{2\pi \times 1.0031 \times 10^6 \times 20} = 7.93nF$$

Select, $\boldsymbol{C_{C_2} = 7.93nF/60V}$

c) C_{C_3}

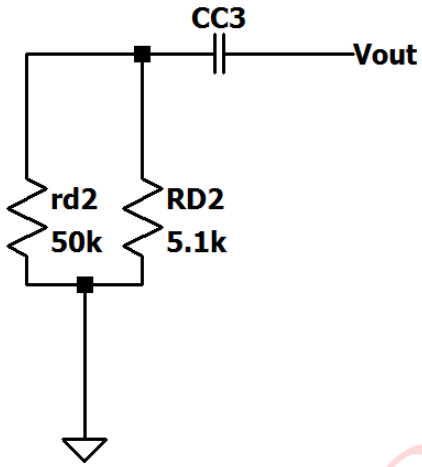

Figure 4: Small Signal low frequency equivalent circuit for C_{C_3}

$$C_{C_3} = \frac{1}{2\pi f_L R_{eq}}$$

$$R_{eq} = (r_{d_2} || R_{D_2})$$

$$R_{eq} = (50k\Omega \ || \ 5.1k\Omega) = 4.6279k\Omega$$

$$C_{C_3} = \frac{1}{2\pi \times 4.62 \times 10^3 \times 20} = 1.7195\mu F$$

Select, $\boldsymbol{C_{C_3} = 1.8\mu F/60V}$

Step 12:- Selection by pass capacitors

Since, $g_{m_1} = g_{m_2} = 3.96mA/V$

$$R_{S_1} = R_{S_2} = 180\Omega$$

$$C_{S_1} = C_{S_2} = \frac{1}{2\pi \times R_{eq} f_L}$$

$$R_{eq} = (1/g_m || R_S$$

$$R_{eq} = (252.51\Omega \ || \ 180\Omega) = 0.1051k\Omega$$

$$C_{S_1} = C_{S_2} = \frac{1}{2\pi \times 105.1 \times 20} = 75.92\mu F$$

Select, $\boldsymbol{C_{S_1} = C_{S_2} = 100\mu F \ /60V}$

Step 13:- Complete designed circuit

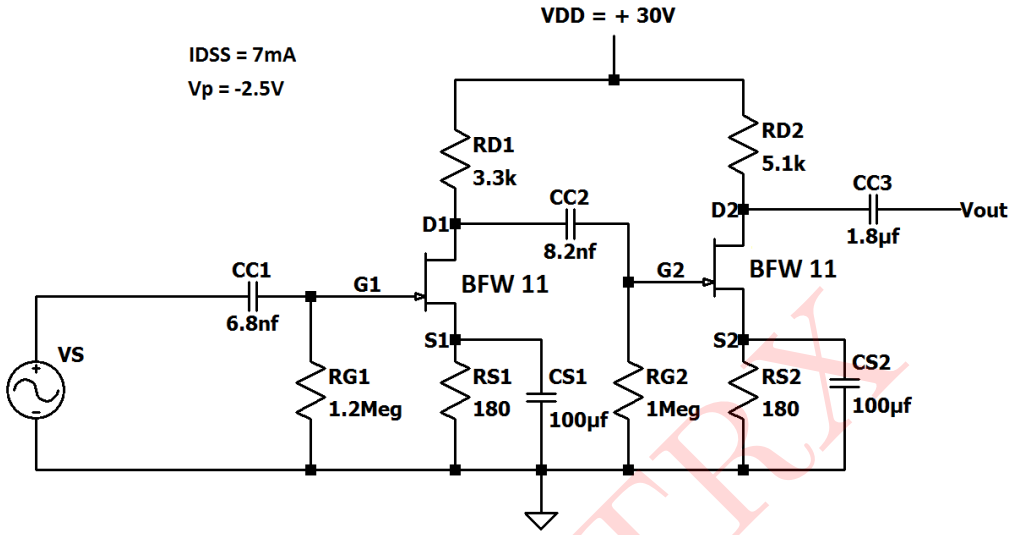

Figure 5: Designed Circuit

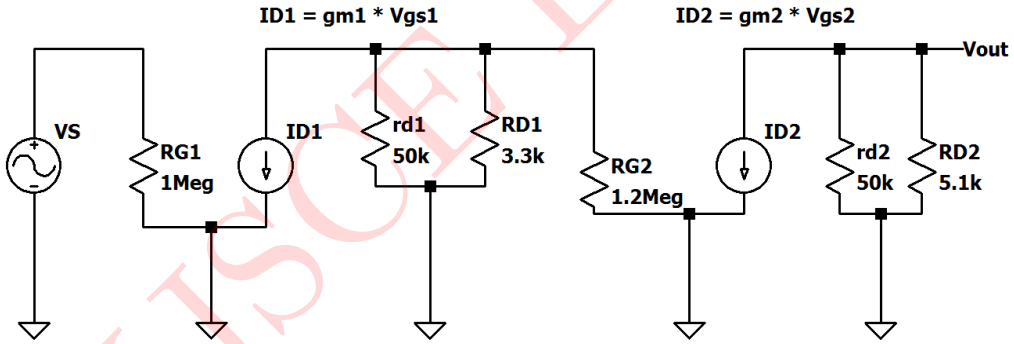

Figure 6: Small Signal Equivalent Circuit

Voltage Gain:-

$A_{V_1} = -g_{m_1}(r_{d_1} \parallel R_{D_1} \parallel R_{G_2})$

$A_{V_1} = -3.96m(50k \parallel 1M \parallel 3.3k)$

$A_{V_1} = -3.96m(3.086k) = -12.22$

$\boldsymbol{A_{V_1} = -12.22}$

$A_{V_2} = -g_{m_2}(r_d \parallel 5.1k)$

$A_{V_2} = -3.96m(50k \parallel 5.1k)$

$A_{V_2} = -3.96m(4.63k) = 18.35$

$\boldsymbol{A_{V_2} = -18.35}$

$A_{V_T} = A_{V_1} \times A_{V_2}$

$A_{V_T} = -12.22 \times -18.35 = 224.237$

$\boldsymbol{A_{V_T} = 224.237}$

$\boldsymbol{A_{V_T}}$ **in dB** $= \boldsymbol{47.02dB}$

Input Impedance:-

$Z_i = R_{G_1} = 1.2M\Omega$

$\boldsymbol{Z_i = 1.2M\Omega}$

Output Impedance:-

$Z_o = R_{D_2}||r_{d_2} = 50k\Omega \;||\; 5.1k\Omega = 4.6279k\Omega$

$\boldsymbol{Z_o = 4.6279k\Omega}$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

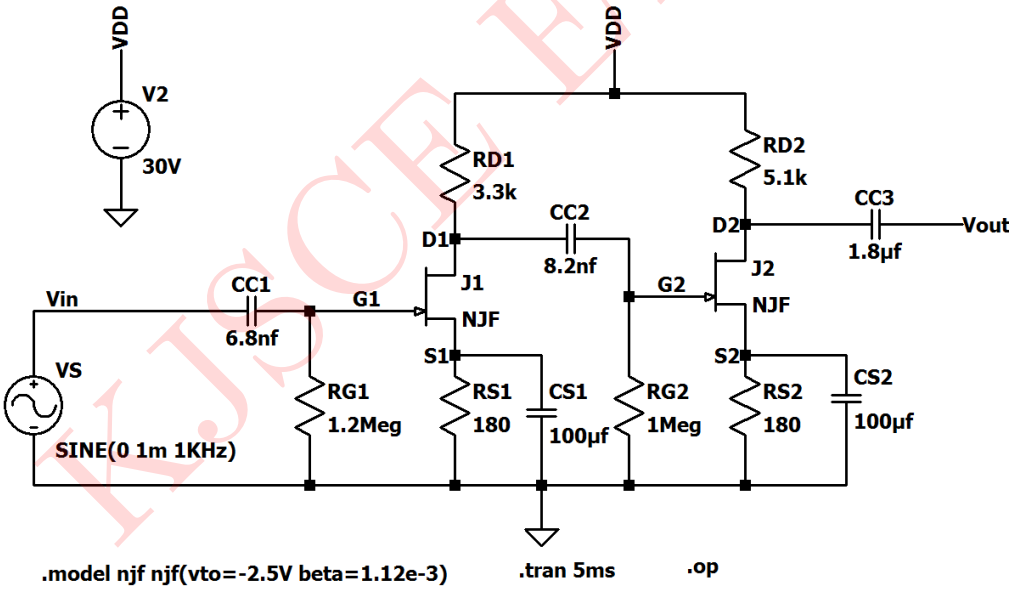

Figure 7: Circuit Schematic 1

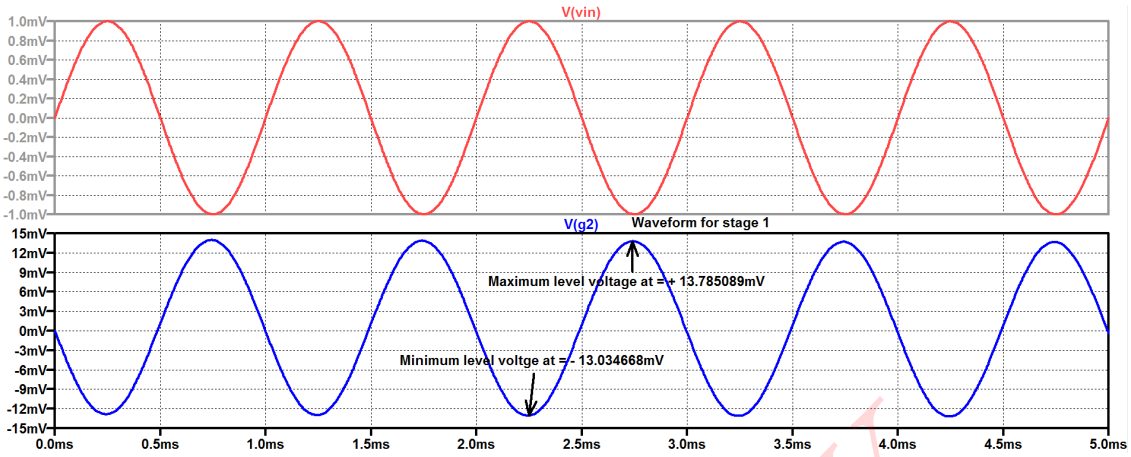

Figure 8: Input & Output waveform for 1^{st} Stage

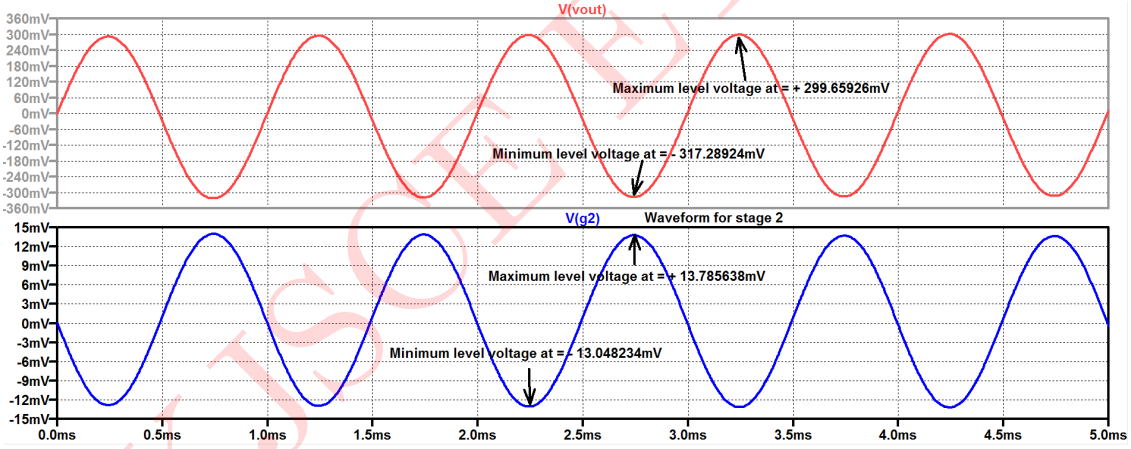

Figure 9: Input & Output waveform for 2^{nd} Stage

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_{D_1}, V_{GS_1}	$3.5mA$, $-0.732V$	$3.73mA$, $-0.673V$
I_{D_2}, V_{GS_2}	$3.5mA$, $-0.732V$	$3.73mA$, $-0.673V$
A_{V_1}	-12.22	-12.5
A_{V_2}	-18.35	-22.78
$A_{V_T}(dB)$	47.02	48.84
V_{out}	$0.51V$	$0.62V$
Z_i, Z_o	$1.2M\Omega, 4.63k\Omega$	$-$

Table 1: Design 1

Design 2:

Design a two stage RC coupled cascade amplifier to meet the following specifications:-
$V_{CC} = 22V$, $R_i \geq 1M\Omega$, $S \leq 10$ and $|A_V| \geq 500$
Select suitable transistor from data-sheet

Solution:

Above requirements can be fulfilled by CS-CE stage(we select CS as 1^{st} stage since $R_i \geq 1M\Omega$)

Step 1:- Selection of transistor

Select BC147B $\rightarrow h_{fe} = 330$, $h_{fE} = \beta = 290$, $h_{ie} = 4.5k\Omega$ and $V_{CE} = 0.25V$

Select BFW11 $\rightarrow I_{DSS} = 7mA$, $g_{m_o} = 5600\mu A/V$, $V_P = -2.5V$ and $r_d = 50k\Omega$

Step 2:- Selection of voltage gain

$A_V \geq 500$

Also, let $A_{V_1} = 4$

$$A_{V_2} = \frac{500}{4} = 12.5$$

Let $A_{V_2} = 12.5$

Design of second stage:-

Step 3:- Selection of R_C

$$|A_{V_2}| = \frac{h_{fe}R_C}{h_{ie}}$$

$$12.5 = \frac{330 \times R_C}{4.5k}$$

$R_C = 1.7045k\Omega$

Select $R_C = 1.8k\Omega, 1/4W$

Step 4:- Calculation of Q-Point(V_{CE_Q}, I_{C_Q})

$V_{CC} = 22V$

$$Let, V_{CE} = \frac{V_{CC}}{2} = 11V$$

$V_{R_E} = 0.1V_{CC} = 0.1 \times 22 = 2.2V$

Applying KVL to the C-E loop of BJT:-

$V_{CC} - V_{R_C} - V_{CE} - V_{R_E} = 0$

$V_{R_C} = V_{CC} - V_{CE} - V_{R_E}$

$V_{R_C} = 22 - 11 - 2.2$

$V_{R_C} = 8.8V$

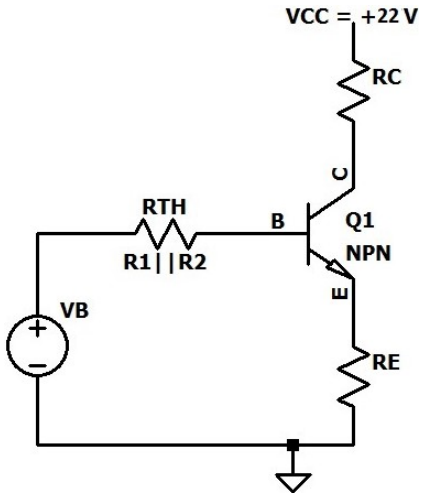

Figure 10: DC Equivalent circuit for BJT

$V_{R_C} = I_C R_C = 8.8V$

$I_C = \dfrac{8.8}{1.8k\Omega} = 4.89mA$

Step 5:- Selection of R_E

$V_{R_E} = 2.2V$

$I_E R_E = 2.2V$

$R_E = \dfrac{2.2}{I_{C_Q}} = \dfrac{2.2}{4.89mA} = 449.89\Omega$

Select $R_E = 420\Omega, 1/4W$

$I_{B_Q} = \dfrac{I_{C_Q}}{\beta} = \dfrac{4.89mA}{290} = 16.86\mu A$

$I_E = I_B + I_C = 4.91mA$

Step 6:- Selection of biasing resistors R_1 & R_2

$S \leq 10,\ \beta = 290$

Let, $S = 10$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B+R_E}\right)}$$

$$10 = \frac{291}{1+291\left(\frac{420}{420+R_B}\right)}$$

$R_B = 3.9145k\Omega = R_1 \,||\, R_2$

$$\frac{R_1 R_2}{R_1+R_2} = 3.9145k\Omega \qquad .....(1)$$

$$V_B = V_{th} = \frac{R_2}{R_1+R_2} \times V_{CC} \qquad .....(2)$$

Applying KVL to the B-E loop of BJT:-

$V_B = I_B R_B + V_{BE} + I_C R_E$

$V_B = (16.86 \times 10^{-6} \times 3.9145k) + 0.7 + 4.89 \times 10^{-3} \times 420$

$V_B = 0.7659 + 2.0538$

$V_B = 2.82V$

From (2),

$$V_B = 2.82 = \frac{R_2}{R_1 + R_2} \times 22 \rightarrow \frac{R_2}{R_1 + R_2} = 0.128 \quad \text{.....(3)}$$

$V_E = I_E R_E = 4.91 \times 420 = 2.062V$

Put (3) in (1),

$R_1(0.128) = 3.9145k$

$R_1 = 30.58k\Omega$

Select $\boldsymbol{R_1 = 33k\Omega, 1/4W}$

From (3), $\frac{R_2}{R_1 + R_2} = 0.128 \rightarrow \frac{R_2}{3.3k + R_2} = 0.128$

$R_2 = 4.84k\Omega$

Select $\boldsymbol{R_2 = 5.1k\Omega, 1/4W}$

Design for first stage:-

Step 7:- Selection of Q-Point $\boldsymbol{V_{GS_Q}}$, $\boldsymbol{I_{D_Q}}$

Using mid-point biasing

$$I_D = \frac{I_{DSS}}{2} = 3.5mA$$

In Saturation, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

On rearranging, $V_{GS} = V_p\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) = -2.5 \times \left(1 - \sqrt{\frac{3.5}{7}}\right) = -0.732V$

$\boldsymbol{V_{GS_{Q2}} = -0.732V}$

$$g_{m_1} = g_{m_o}\left(1 - \frac{V_{GS}}{V_P}\right) = 5600\mu A/V\left(1 - \frac{0.732}{2.5}\right) = 3.96mA/V$$

$\boldsymbol{g_{m_1} = g_{m_o} = 3.96mA/V}$

Step 8:- Selection of R_D

$$|A_{V_2}| = \frac{h_{fe} \times R_C}{h_{ie}} = \frac{300 \times 1.8k}{4.5k} = 132$$

$$|A_{V_1}| = \frac{A_V}{|A_{V_2}|} = \frac{500}{132} = 3.7878$$

$$|A_{V_1}| = g_{m_1}(r_d \parallel R_D \parallel R_1 \parallel R_2 \parallel h_{ie})$$

$$R_{L_1} = r_d \parallel R_1 \parallel R_2 \parallel h_{ie}$$

$$R_{L_1} = 80k \parallel 13k \parallel 5.9k \parallel 4.5k$$

$$R_{L_1} = 2.13k\Omega$$

$$|A_{V_1}| = g_m[R_D \parallel 2.13k]$$

$$3.7878 = \frac{3.96}{1000} \times \frac{R_D \times 2.13k}{R_D + 2.13k}$$

$$956.515(R_D + 2.13k) = 2.13k \times R_D$$

$$R_D = 1.736k\Omega$$

Select $R_D = 1.8k\Omega, 1/4W$

Step 9:- Selection of R_S

$$V_{GS_Q} = -I_{DQ_1} R_S$$

$$R_S = \frac{-V_{GS_Q}}{I_{D_Q}}$$

$$R_{S_1} = \frac{0.732}{3.5mA} = 201.1\Omega$$

Select **$R_S = 180\Omega$, $1/4W$**

Step 10:- Selection of R_G

To avoid loading effect and fulfill the requirement of $R_i \geq 1M\Omega$

Select $R_G = 1.2M\Omega$, $1/4W$

Step 11:- Selection of coupling capacitors C_{C_2}, C_{C_1}, C_{C_3}

Since, f_L is not given we consider $f_L = 20Hz$

a) C_{C_1}

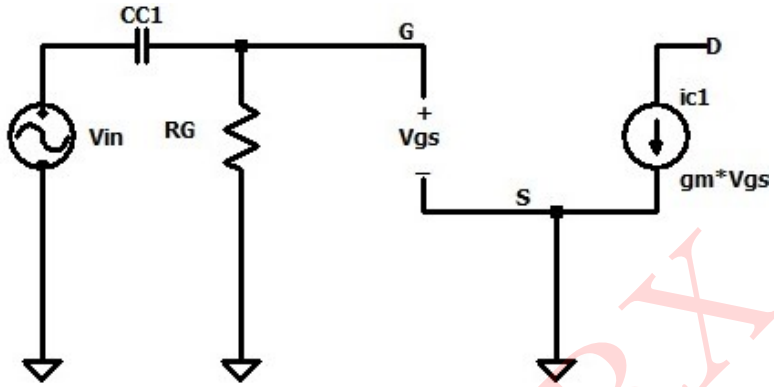

Figure 11: Small Signal low frequency equivalent circuit for C_{C_1}

$$C_{C_1} = \frac{1}{2\pi f_L R_G}$$

$$C_{C_1} = \frac{1}{2\pi \times 1.2M \times 20} = 6.63nF$$

Select, $\boldsymbol{C_{C_1} = 6.8nF/50V}$

b) C_{C_2}

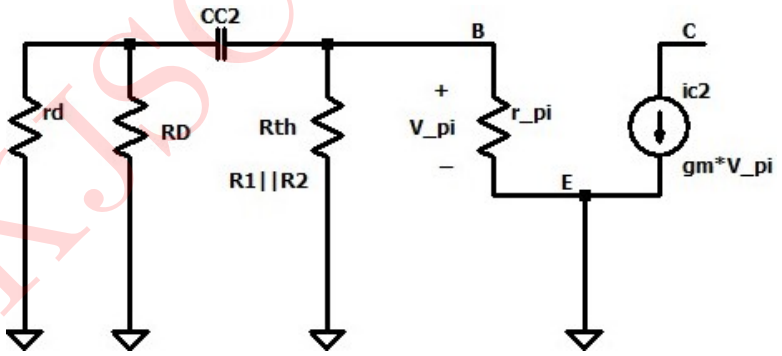

Figure 12: Small Signal low frequency equivalent circuit for C_{C_2}

$$C_{C_2} = \frac{1}{2\pi f_L R_{eq}}$$

$$R_{eq} = (r_d \parallel R_D) + (R_1 \parallel R_2 \parallel h_{ie})$$

$$R_{eq} = (50k \parallel 1.8k) + (3.3k \parallel 5.1k \parallel 4.5k)$$

$$R_{eq} = (1.737k) + (2.23k)$$

$$R_{eq} = 3.97k\Omega$$

$$C_{C_2} = \frac{1}{2\pi \times 3.97k \times 20} = 2.004\mu F$$

Select, $\boldsymbol{C_{C_2} = 2.2\mu F/50V}$

c) C_{C_3}

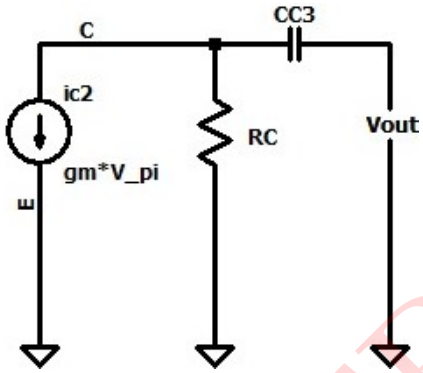

Figure 13: Small Signal low frequency equivalent circuit for C_{C_3}

$$C_{C_3} = \frac{1}{2\pi f_L R_{eq}}$$

$$R_{eq} = R_C = 1.8k$$

$$C_{C_3} = \frac{1}{2\pi \times 1 \times 10^3 \times 20} = 4.42\mu F$$

Select, $\boldsymbol{C_{C_3} = 4.47\mu F/50V}$

Step 12:- Selection bypass capacitors

a) C_S

$$C_S = \frac{1}{2\pi \times R_{eq} \times f_L}$$

$$R_{eq} = \left(\frac{1}{g_m} || R_S\right) = \frac{1}{3.96m} || 180 = 105.09\Omega$$

$$C_S = \frac{1}{2\pi \times 105.09 \times 20} = 75.72\mu A$$

Select $\boldsymbol{C_S = 82\mu F/50V}$

a) C_E

$$X_{CE} = 0.1R_E$$

i.e $$\frac{1}{2\pi \times f_L \times 0.1R_E} = 0.1R_E$$

$$C_E = \frac{1}{2\pi \times 0.1RE \times f_L}$$

$$C_E = \frac{1}{2\pi \times 20 \times 0.1 \times 420} = 189.47\mu A$$

Select $\boldsymbol{C_E = 220\mu F/50V}$

Step 13:- Small Signal Analysis

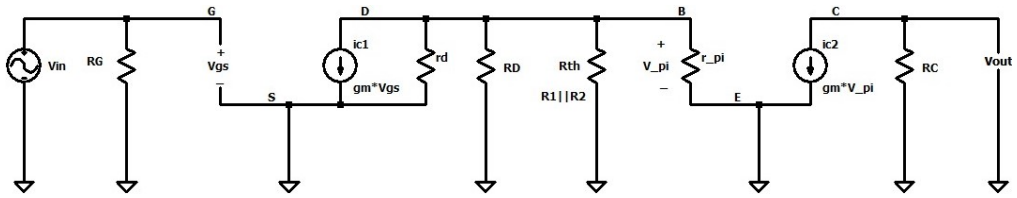

Figure 14: Small Signal Equivalent Circuit

$$g_{m_2} = \frac{I_{C_Q}}{V_T} = \frac{4.89mA}{26mV} = 188.07mA/V$$

$$\boldsymbol{g_{m_2} = 188.07mA/V}$$

Input Impedance:-

$$Z_i = R_G = 1.2M\Omega$$

$$\boldsymbol{Z_i = 1.2M\Omega}$$

Output Impedance:-

$$Z_o = R_C = 50k\Omega = 1.8k\Omega$$

$$\boldsymbol{Z_o = 1.8k\Omega}$$

Voltage Gain:-

$$A_{V_1} = \frac{V_1}{V_S} = \frac{-g_{m_1}V_{gs}(r_d||R_D||R_{th}||r_\pi)}{V_{gs}}$$

$$A_{V_1} = \frac{V_1}{V_S} = -g_{m_1}(r_d \;||\; R_D \;||\; R_{th} \;||\; r_\pi)$$

$$r_\pi = \frac{\beta V_T}{I_C} = \frac{290 \times 26mV}{4.89mA} = 1.54k\Omega$$

$$A_{V_1} = -3.96m(50k \;||\; 1.8k \;||\; 4.42k \;||\; 1.54k) = -2.732$$

$$\boldsymbol{A_{V_1} = -2.732}$$

$$A_{V_2} = \frac{V_{out}}{V_1} = \frac{-g_{m_2}V_\pi R_C}{V_\pi}$$

$$A_{V_2} = -g_{m_2}R_C$$

$$A_{V_2} = -188.07(1.8) = -338.53$$

$$\boldsymbol{A_{V_2} = -338.53}$$

$A_{V_T} = A_{V_1} \times A_{V_2}$

$A_{V_T} = -338.53 \times -2.732 = 924.85$

$\boldsymbol{A_{V_T} = 924.85}$

$\boldsymbol{A_{V_T}}$ **in dB** $= \mathbf{59.32}\boldsymbol{dB}$

$V_{out} = A_{V_T} \times V_S = 924.85 \times 2mV = 1.85V$

$\boldsymbol{V_{out} = 1.85V}$

Step 14:- Compete designed circuit

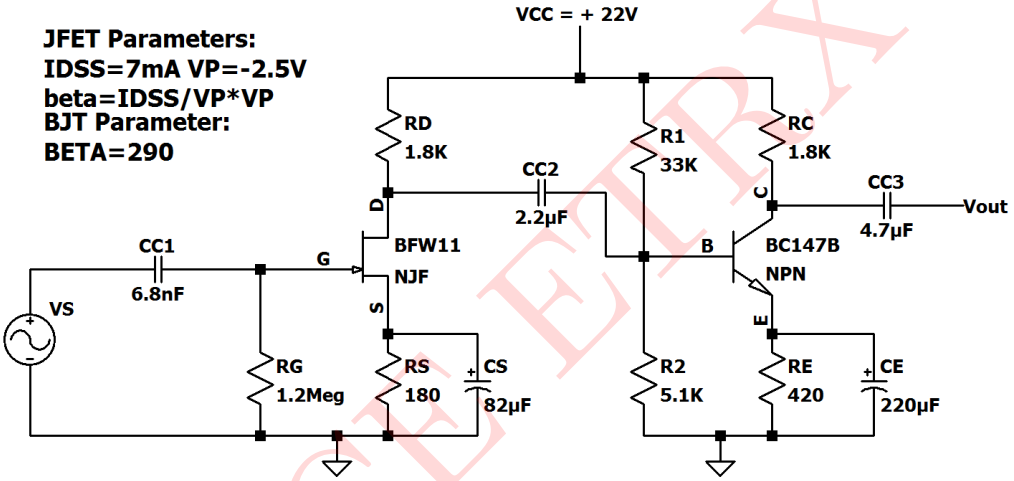

Figure 15: Designed Circuit 2

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

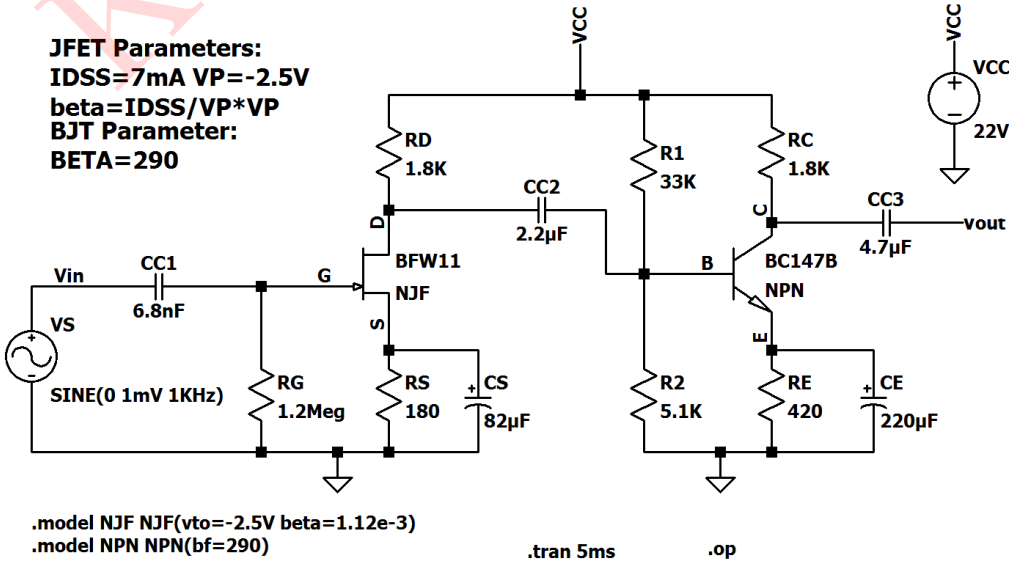

Figure 16: Circuit Schematic 2

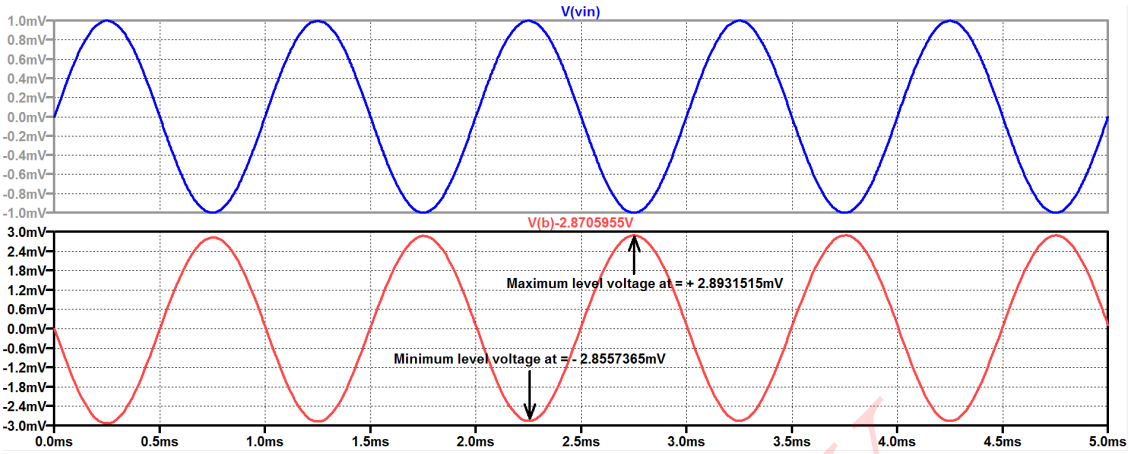

Figure 17: Input & Output waveform for 1^{st} Stage

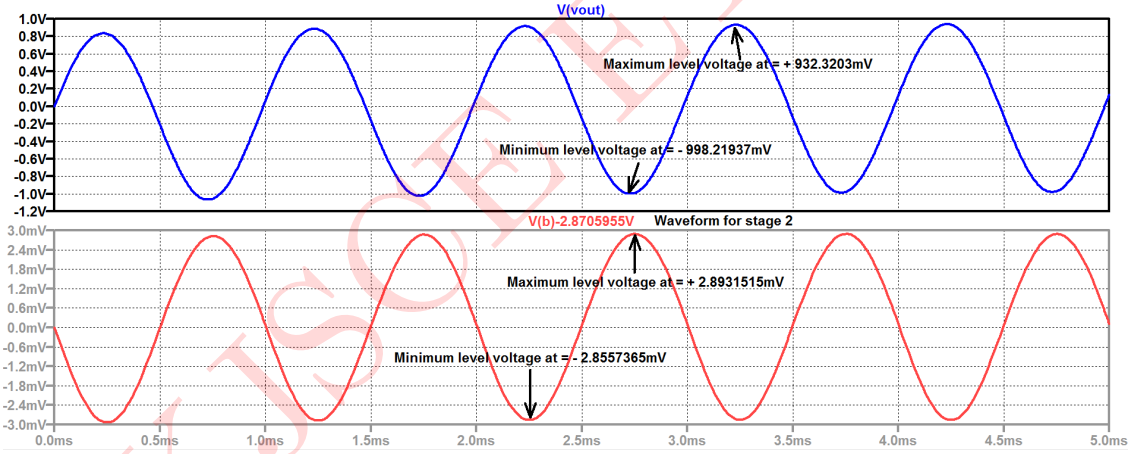

Figure 18: Input & Output waveform for 2^{nd} Stage

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_{D_1}, V_{GS_1}	$3.5mA$, $-0.732V$	$3.73mA$, $-0.673V$
I_B, I_C, I_E	$16.86\mu A$, $4.89mA$, $4.91mA$	$16.82\mu A$, $4.88mA$, $4.90mA$
V_B, V_E	$2.82V$, $2.062V$	$2.87V$, $2.055V$
A_{V_1}	-2.732	-2.874
A_{V_2}	-338.53	-335.82
$A_{V_{in}}(dB)$	59.32	59.69
Z_i, Z_o	$1.2M\Omega, 1.8k\Omega$	–

Table 2: Design 2

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