

K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Cascode Amplifier

Q1. Calculate DC voltages at each mode and DC currents in the given circuit.

Given: $R_1 = 65k\Omega$, $R_2 = 33k\Omega$, $R_C = 2.7k\Omega$, $R_L = 6.2k\Omega$, $R_E = 0.5k\Omega$, $R_3 = 12k\Omega$, $V_{CC} = 12V$, $\beta_1 = \beta_2 = 100$.

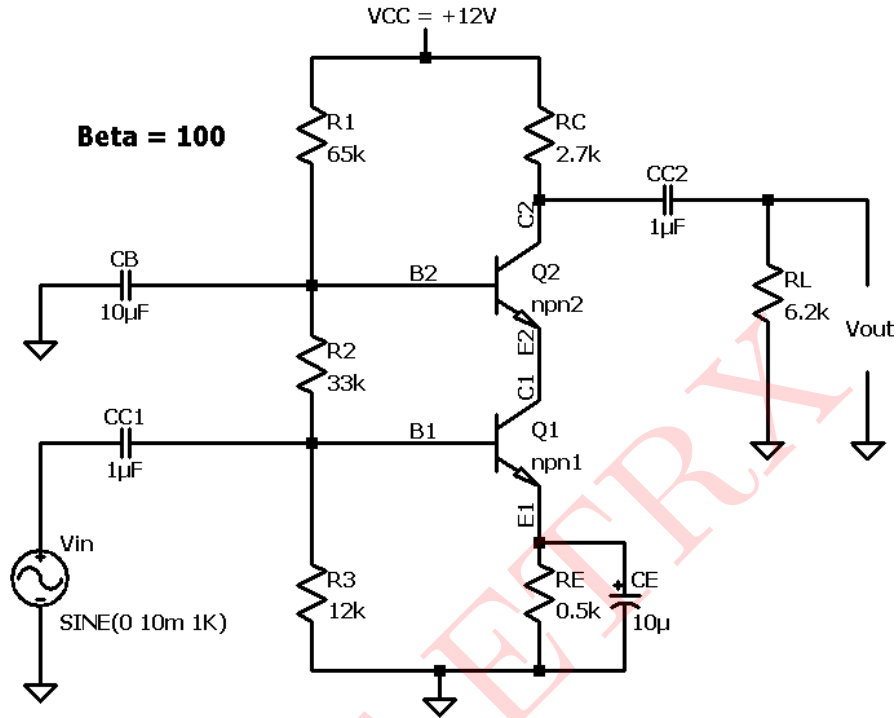


Figure 1: Circuit 1

Solution:

The above circuit is a CE-CB bjt cascode amplifier

$$V_{B1} = \left(\frac{R_3}{R_1 + R_2 + R_3} \right) \times V_{CC} = \left(\frac{12k}{65k + 33k + 12k} \right) 12 = \mathbf{1.3090V}$$

$$V_{B1} = \left(\frac{R_3 + R_2}{R_1 + R_2 + R_3} \right) \times V_{CC} = \left(\frac{12k + 33k}{65k + 33k + 12k} \right) 12 = \mathbf{4.090V}$$

Applying KVL to the B-E loop of Q1

$$V_{E1} = V_{B1} - V_{BE1} = 1.309 - 0.7 = \mathbf{0.609V}$$

$$V_{E1} = I_{E1} R_E$$

$$I_{E1} = V_{E1} / R_E = 0.609 / 500 = \mathbf{1.218mA}$$

$$I_{C1} = I_{E1} = I_{E2} = I_{C2} = \mathbf{1.218mA}$$

$$V_{C2} = V_{CC} - I_{C2} R_C = 12 - (1.218mA)(2.7k) = \mathbf{8.7114V}$$

$$V_{E2} = V_{B2} - V_{BE2} = 4.909 - 0.7 = \mathbf{4.209V}$$

$$V_{E2} = V_{C1} = 4.209V$$

$$V_{CE1} = V_{C1} - V_{E1} = 4.209 - 0.609 = \mathbf{3.6V}$$

$$V_{CE2} = V_{C2} - V_{E2} = 8.7114 - 4.209 = \mathbf{4.5024V}$$

$$I_C = \beta I_B$$

$$I_B = I_C / \beta = 1.218 \text{mA} / 100 = \mathbf{12.18 \mu A}$$

Small signal parameters:

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{100 \times 26 \times 10^{-3}}{1.218 \times 10^{-3}} = \mathbf{2.134 \text{k}\Omega}$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.218 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{46.846 \text{ mA/V}}$$

Mid frequency equivalent circuit:

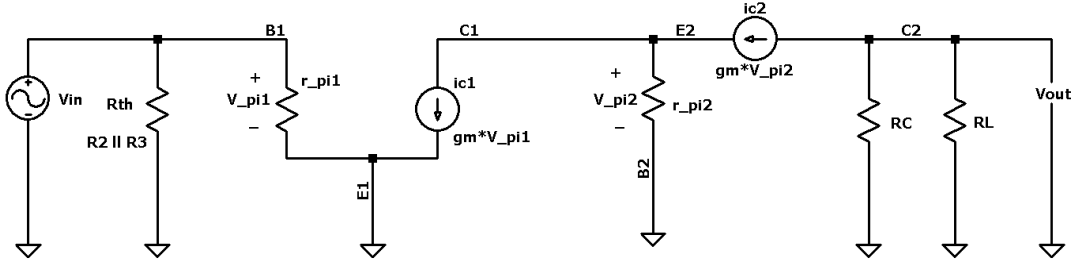


Figure 2: Mid frequency equivalent circuit

$$Z_i = R_2 \parallel R_3 \parallel r_\pi = 33 \text{k} \parallel 12 \text{k} \parallel 2.134 \text{k} = \mathbf{1.717 \text{k}\Omega}$$

$$Z_o = R_C \parallel R_L = 2.7 \text{k} \parallel 6.2 \text{k} = \mathbf{1.88 \text{k}\Omega}$$

$$\text{Gain of CB stage} = A_{V_2} = g_m (R_C \parallel R_L) = \frac{46.864 \text{mA/V}}{1.88 \text{k}} = \mathbf{88.0714}$$

$$\text{Gain of CB stage} = A_{V_1} = -g_m \left(\frac{r_\pi}{1 + \beta} \right) = -46.842 \left(\frac{2.134 \text{k}}{101} \right) = \mathbf{-0.9897}$$

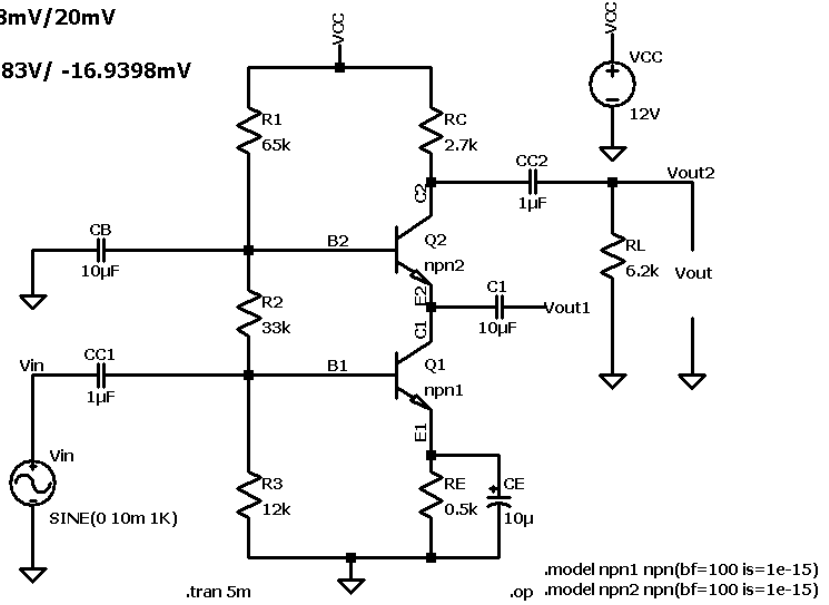
$$A_{V_T} = A_{V_1} \times A_{V_2} = 88.0704 \times -0.9897 = \mathbf{-87.1632}$$

$$A_{V_T} \text{ in dB} = 20 \log(87.16321) = \mathbf{38.806 \text{dB}}$$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

$AV1 = V_{out1}/V_{in} = -16.9398\text{mV}/20\text{mV}$
 $Av1 = -0.8469$
 $Av2 = V_{out2}/V_{out1} = -1.0583\text{V}/-16.9398\text{mV}$
 $AV2 = 62.4741$
 $AVT = AV1*AV2 = 52.90931$
 $AVT \text{ in dB} = 34.4706$
 $\text{Beta} = 100$



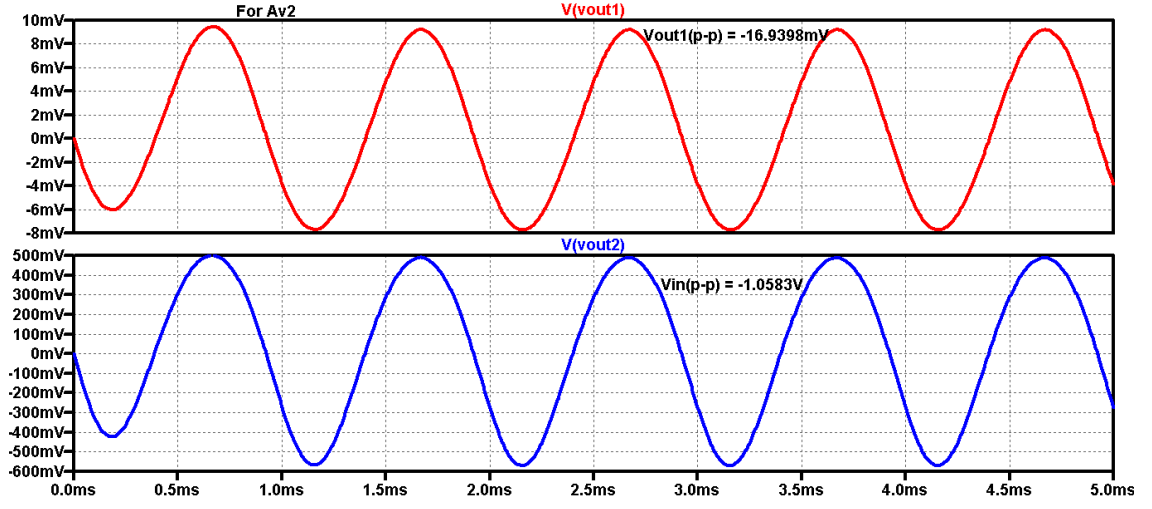


Figure 5: Input output waveform for A_{V_2}

Comparison of Theoretical and Simulated Values:

Parameters	Simulated	Theoretical
Stage 1: I_{E1}	0.876mA	1.218mA
I_{B1}, I_{C1}	8.764 μ A, 0.8764mA	12.18 μ A, 1.218mA
V_{B1}, V_{C1}	1.153V, 3.905V	1.309V, 4.209V
V_{E1}, V_{CE1}	0.442V, 3.463V	0.609V, 3.6V
Stage 2: I_{E2}	0.876mA	1.218mA
I_{B2}, I_{C2}	8.677 μ A, 0.876mA	12.18 μ A, 1.218mA
V_{B2}, V_{C2}	4.616V, 9.657V	4.909V, 8.7114V
V_{E2}, V_{CE2}	3.905V, 5.752V	4.209V, 4.5024V
A_{V_1}	-0.8469	-0.9897
A_{V_2}	62.4741	88.0704
A_{V_T} in dB	34.4706dB	38.8066dB
Z_i	—	1.717k Ω
Z_o	—	1.88k Ω

Table 1: Numerical 1

Q2. Calculate DC voltages at each node and DC currents in the give circuit.

Given:

$R_1 = 110k\Omega$, $R_2 = 33k\Omega$, $R_S = 1k\Omega$, $R_D = 3.3k\Omega$, $R_3 = 12k\Omega$, $V_{DD} = 20V$, $k_{n1} = k_{n2} = 0.8 \text{ mA/V}^2$.

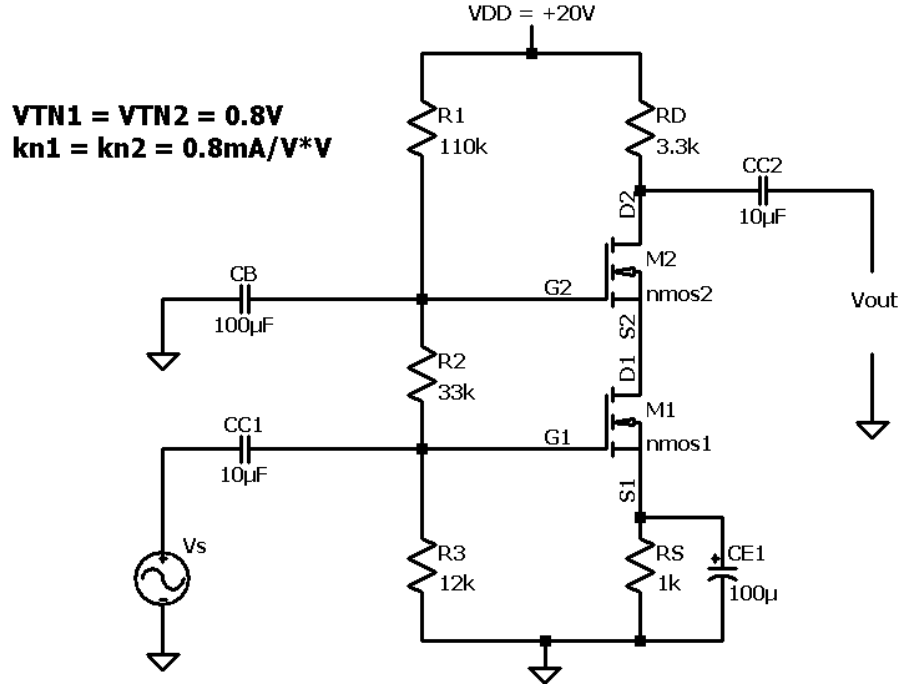


Figure 6: Circuit 1

Solution:

The above circuit is a CS-CG directly coupled MOSFET amplifier

$$R_T = R_1 + R_2 + R_3 = 110k + 33k + 12k = 155K\Omega$$

$$V_{G1} = \left(\frac{R_3}{R_1 + R_2 + R_3} \right) \times V_{DD} = \left(\frac{12k}{155k} \right) 20 = \mathbf{1.548V}$$

$$V_{G2} = \left(\frac{R_3 + R_2}{R_1 + R_2 + R_3} \right) \times V_{DD} = \left(\frac{12k + 33k}{155k} \right) 20 = \mathbf{5.806V}$$

Applying KVL to the B-E loop of Q1

$$V_{GS1} = V_{G1} - V_{S1}$$

$$V_{GS1} = V_{G1} - I_{D1}R_S$$

$$V_{GS1} = V_{G1} - I_{D1} \times 1k \longrightarrow (1)$$

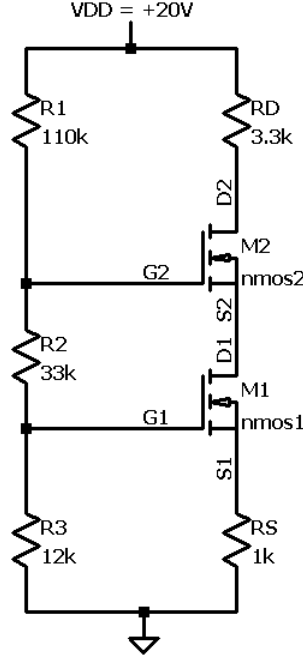


Figure 7: DC equivalent circuit

Assuming NMOS in Saturation Region

$$I_{D1} = k_{n1}(V_{GS1} - V_{TN1})^2$$

$$I_{D1} = 0.8 \times 10^{-3}(V_{GS1} - 0.8)^2 \text{ ——— (2)}$$

Solving equations (1) and (2)

$$V_{GS1} = 1.548 - 0.8(V_{GS1} - 0.8)^2$$

$$V_{GS1} = 1.548 - 0.8(V_{GS}^2 + 0.64 - 1.6V_{GS1})$$

$$0.8V_{GS1}^2 - 0.28V_{GS1} - 1.036 = 0$$

$$V_{GS1} = 1.3263V \text{ or } -0.9763V$$

We choose $V_{GS1} = 1.3263$ ($\because V_{GS1} > V_{TN1}$)

$$I_{D1} = 0.8 \times 10^{-3}(V_{GS1} - 0.8)^2$$

$$I_{D1} = 0.8 \times 10^{-3}(1.3263 - 0.8)^2$$

$$I_{D1} = I_{D2} = \mathbf{0.2215mA}$$

$$V_{GS2} = V_{G2} - V_{S2}$$

$$V_{S2} = V_{GS2} - V_{G2} = 5.806 - 1.3263 = \mathbf{4.4797V}$$

$$V_{DS2} = V_{D2} - V_{S2} = 19.269 - 4.4797 = \mathbf{14.7893V}$$

$$V_{DS1} = V_{D1} - V_{S1} = 4.4797 - 0.2215 = \mathbf{4.2582V}$$

Small signal parameters:

$$g_{m1} = g_{m2} = 2k_n(V_{GS} - V_{TN}) = 2 \times 0.8 \times 10^{-3}(1.3263 - 0.8) = \mathbf{40.84208 \text{ mA/V}}$$

Mid frequency equivalent circuit:

$$Z_i = R_2 \parallel R_3 = 33k \parallel 12k = \mathbf{8.8k\Omega}$$

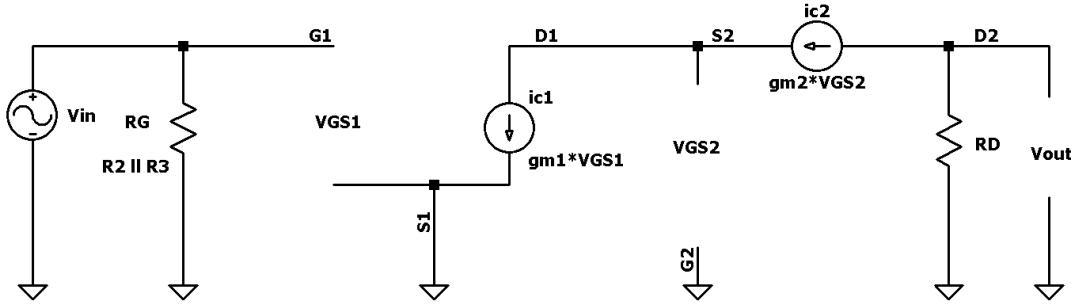


Figure 8: Mid frequency equivalent circuit

$$Z_o = R_D = \mathbf{2.7788k\Omega}$$

$$A_{V_2} = -g_m(R_D) = 0.84208 \times 3.3 = \mathbf{2.7788}$$

$$A_{V_1} = \frac{-V_{gs2}}{V_{gs1}} = \mathbf{-1}$$

$$A_{V_T} = A_{V_1} \times A_{V_2} = 2.7788 \times -1 = \mathbf{-2.7788}$$

$$A_{V_T \text{ in dB}} = 20 \log_{10}(-2.7788) = \mathbf{8.8771dB}$$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

$AV1 = V_{out1}/V_{in} = -19.9591\text{mV}/20\text{mV}$
 $Av1 = -0.9979$
 $Av2 = V_{out2}/V_{out1} = -55.4242\text{mV}/-19.9591\text{mV}$
 $AV2 = 2.7768$
 $AVT = AV1*AV2 = -2.770968$
 $AVT \text{ in dB} = 8.85263 \text{ dB}$
 $VTN1 = VTN2 = 0.8\text{V}$
 $kn1 = kn2 = 0.8\text{mA/V}^2$
 $KP = 2*kn1 = 1.6\text{E-3}$

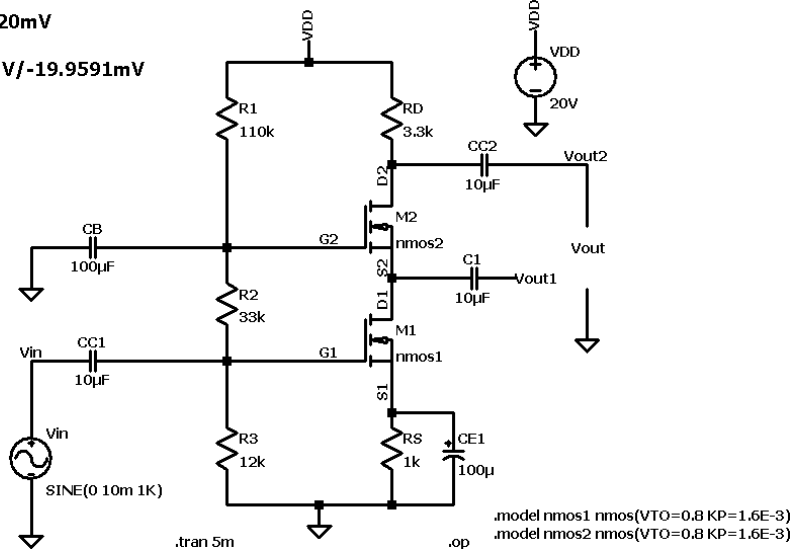


Figure 9: Circuit Schematic

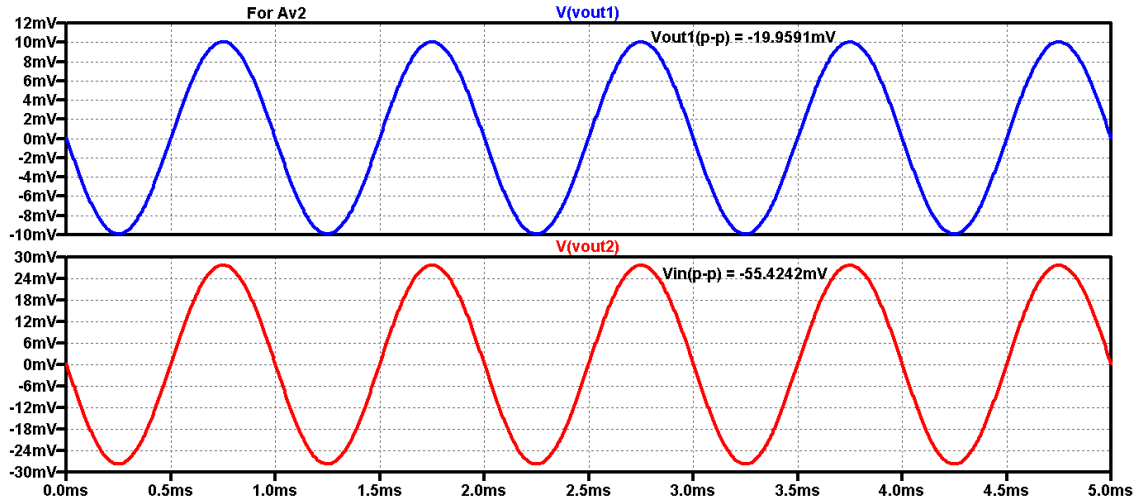


Figure 10: Input output waveform for AV_2

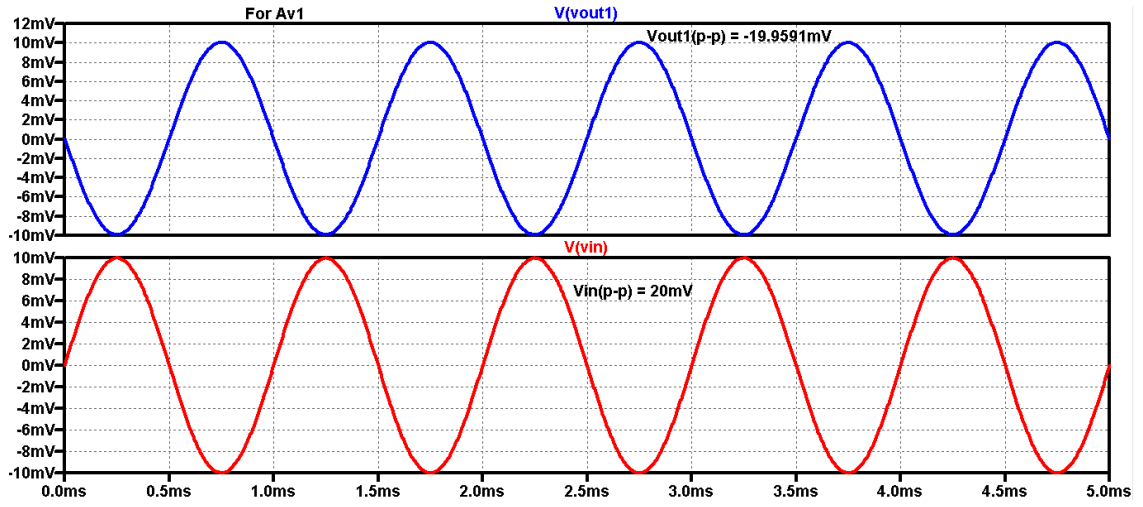


Figure 11: Input output waveform for A_{V_1}

Comparison of Theoretical and Simulated Values:

Parameters	Simulated	Theoretical
Stage 1:		
V_{G1}, I_{D1}	1.548V, 0.2218mA	1.548V, 0.2215mA
V_{S1}, V_{D1}	0.2218V, 4.4798V	0.2215V, 4.4797V
V_{GS1}, V_{DS1}	1.3265V, 4.258VV	1.3263V, 4.2582V
Stage 2:		
I_{G2}, I_{D2}	5.806V, 0.2218mA	5.806V, 0.2215mA
V_{S2}, V_{D2}	4.4698V, 19.268V	4.4797V, 19.269V
V_{GS2}, V_{DS2}	1.3262V, 14.7882V	1.3263V, 14.789V
A_{V_1}	-0.9979	-1
A_{V_2}	2.7768	2.7788
A_{V_T} in dB	8.88526	8.8771
Z_i	—	8.8k Ω
Z_o	—	3.3k Ω

Table 2: Numerical 2
