K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Multi-transistor circuits

Numerical 1:

The parameters of each transistor in the circuit given below in figure 1 are
$\beta_1 = \beta_2 = 100$, $V_A = \infty$ and $V_{BE_1} = V_{BE_2} = 0.7V$

a) Determine the small-signal parameters g_m, r_π and r_o for both transistors

b) Determine the small-signal voltage gain $A_{V_1} = V_{o_1}/V_S$, assuming V_{o_1} is connected to an open circuit and determine the gain $A_{V_2} = V_{out}/V_{o_1}$

c) Determine the overall small-signal voltage gain $A_{V_T} = V_{out}/V_S$

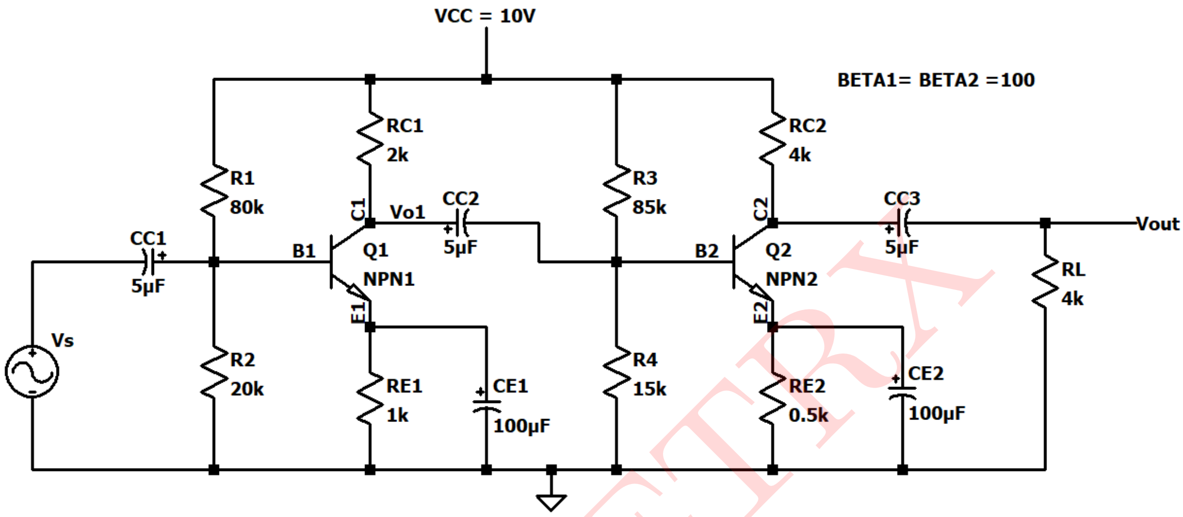

Figure 1: Circuit 1

Solution:

The circuit given above is a 2-stage RC-coupled CE-CE amplifier.

DC analysis:

Due to R-C coupling, both the stage's Q-point are isolated.

Since R-C coupling is employed, DC analysis of both stages can be performed individually.

DC analysis of stage 1 CE amplifier:

$$V_{TH_1} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{20k\Omega}{80k\Omega + 20k\Omega} \times 10V = \mathbf{2V}$$

$$R_{B_1} = \frac{R_1 R_2}{R_1 + R_2} = \frac{80k\Omega \times 20k\Omega}{80k\Omega + 20k\Omega} = \mathbf{16k\Omega}$$

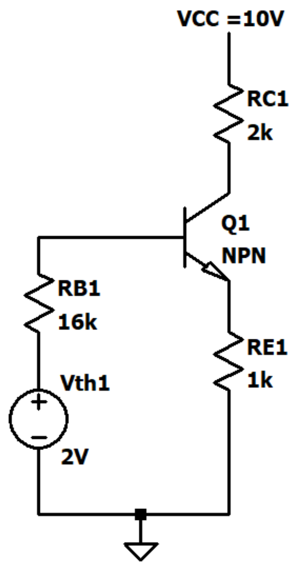

Figure 2: Thevenin's equivalent circuit of stage 1

Applying KVL to base-emitter loop,

$V_{th_1} - I_{B_1} R_{B_1} - V_{BE_1} - I_{E_1} R_{E_1} = 0$

i.e $V_{th_1} - I_{B_1} R_{B_1} - V_{BE_1} - (\beta_1 + 1) I_{B_1} R_{E_1} = 0 \qquad (\because I_E = (\beta + 1) I_B)$

$\therefore 2V - I_{B_1}(16k\Omega) - 0.7V - (101) I_{B_1}(1k\Omega) = 0$

$\therefore 1.3V - I_{B_1}(16k\Omega + 101(1k\Omega)) = 0$

$$I_{B_1} = \frac{1.3V}{16k\Omega + 101k\Omega} = \mathbf{11.111\mu A}$$

$$\therefore I_{C_1} = \beta_1 I_{B_1} = (100)(11.111\mu A) = \mathbf{1.111mA}$$

$$\therefore I_{E_1} = (\beta_1 + 1) I_{B_1} = (100 + 1)(11.111\mu A) = \mathbf{1.122mA}$$

Applying KVL to collector emitter loop,

$V_{CC} - I_{C_1} R_{C_1} - V_{CE_1} - I_{E_1} R_{E_1} = 0$

$10V - (1.111mA)(2k\Omega) - V_{CE_1} - (1.122mA)(1k\Omega) = 0$

$10V - 2.22V - V_{CE_1} - 1.122V = 0$

$\therefore V_{CE_1} = 10 - 3.342 = \mathbf{6.658V}$

DC analysis of stage 2 CE amplifier:

$$V_{TH_2} = \frac{R_4}{R_3 + R_4} \times V_{CC} = \frac{15k\Omega}{85k\Omega + 15k\Omega} \times 10V = \mathbf{1.5V}$$

$$R_{B_2} = \frac{R_3 R_4}{R_3 + R_4} = \frac{15k\Omega \times 85k\Omega}{15k\Omega + 85k\Omega} = \mathbf{12.75k\Omega}$$

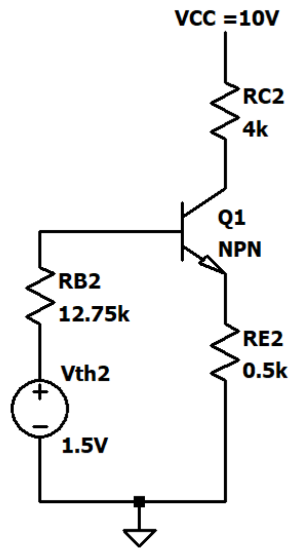

Figure 3: Thevenin's equivalent circuit of stage 2

Applying KVL to base-emitter loop,

$V_{th_2} - I_{B_2}R_{B_2} - V_{BE_2} - I_{E_2}R_{E_2} = 0$

i.e $V_{th_2} - I_{B_2}R_{B_2} - V_{BE_2} - (\beta_2+1)I_{B_2}R_{E_2} = 0 \qquad (\because I_E = (\beta+1)I_B)$

$\therefore 1.5V - I_{B_2}(12.75k\Omega) - 0.7V - (101)I_{B_2}(0.5k\Omega) = 0$

$\therefore 0.8V - I_{B_2}(12.75k\Omega + 101(.05k\Omega)) = 0$

$$I_{B_2} = \frac{0.8V}{12.75k\Omega + 50.5k\Omega} = \mathbf{12.648\mu A}$$

$\therefore I_{C_2} = \beta_2 I_{B_2} = (100)(12.64\mu A) = \mathbf{1.264mA}$

$\therefore I_{E_2} = (\beta_2+1)I_{B_2} = (100+1)(12.648\mu A) = \mathbf{1.277mA}$

Applying KVL to collector emitter loop,

$V_{CC} - I_{C_2}R_{C_2} - V_{CE_2} - I_{E_2}R_{E_2} = 0$

$10V - (1.264mA)(4k\Omega) - V_{CE_2} - (1.277mA)(0.5k\Omega) = 0$

$10V - 5.056V - V_{CE_2} - 0.6385 = 0$

$\therefore V_{CE_2} = 10 - 5.6885 = \mathbf{4.3115V}$

Small signal parameters of stage 1:

i) $r_{\pi_1} = \beta_1 \dfrac{V_T}{I_{C_1}} = 100 \times \dfrac{26mV}{1.111mA} = \mathbf{2.340k\Omega}$

ii) $g_{m_1} = \dfrac{I_{C_1}}{V_T} = \dfrac{1.111mA}{26mV} = 42.730mA/V$

iii) $r_{o_1} = \infty$

Small signal parameters of stage 2:

i) $r_{\pi_2} = \beta_2 \dfrac{V_T}{I_{C_2}} = 100 \times \dfrac{26mV}{1.264mA} = \mathbf{2.056k\Omega}$

ii) $g_{m_2} = \dfrac{I_{C_2}}{V_T} = \dfrac{1.264mA}{26mV} = \mathbf{48.61mA/V}$

iii) $r_{o_2} = \infty$

Mid-band AC equivalent circuit:

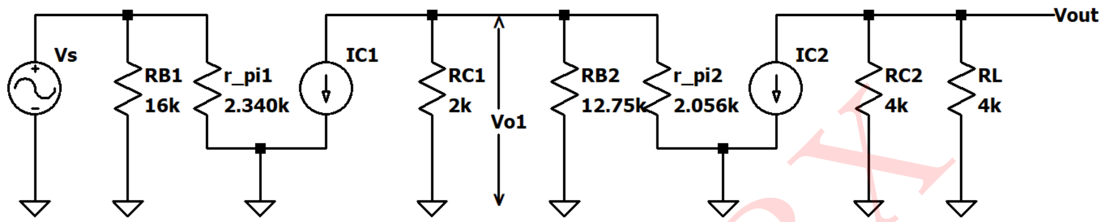

Figure 4: Mid-band AC equivalent circuit

Input impedance of stage 1

$$Z_i = R_{B_1} \parallel r_{\pi_1}$$
$$= 16k\Omega \parallel 2.340k\Omega$$
$$= \frac{16k\Omega \times 2.340k\Omega}{16k\Omega + 2.340k\Omega} = \mathbf{2.041k\Omega}$$

Output impedance of stage 2

$$Z_o = R_{C_2} \parallel R_L$$
$$= 4k\Omega \parallel 4k\Omega$$
$$= \frac{4k\Omega \times 4k\Omega}{4k\Omega + 4k\Omega} = \mathbf{2k\Omega}$$

$$A_{V_1} = \frac{V_{o_1}}{V_S}$$
$$= \frac{(-g_{m_1} V_{\pi_1})(R_{C_1} \parallel R_{B_2} \parallel r_{\pi_2})}{V_{\pi_1}}$$
$$= -g_{m_1}(R_{C_1} \parallel R_{B_2} \parallel r_{\pi_2} d)$$
$$= -42.730mA/V(2k\Omega \parallel 12.75k\Omega \parallel 2.065k\Omega)$$
$$= -42.7305mA/V\left[2k\Omega \parallel \left(\frac{12.75k\Omega \times 2.056k\Omega}{12.75k\Omega + 2.056k\Omega}\right)\right]$$
$$= -42.730mA/V[2k\Omega \parallel 1.77k\Omega]$$
$$= -42.730mA/V\left(\frac{2k\Omega \times 1.77k\Omega}{2k\Omega + 1.77k\Omega}\right)$$
$$= -42.730mA/V \times 0.938k\Omega = \mathbf{-40.123}$$

$$
\begin{aligned}
A_{V_2} &= \frac{V_{out}}{V_{o_1}} \\
&= \frac{(-g_{m_2} V_{\pi_2})(R_{C_2} \parallel R_L)}{V_{\pi_1}} \\
&= -g_{m_2}(R_{C_2} \parallel R_L) \\
&= -48.61mA/V(4k\Omega \parallel 4k\Omega) \\
&= -48.61mA/V \left(\frac{4k\Omega \times 4k\Omega}{4k\Omega + 4k\Omega} \right) \\
&= -48.61mA/V \times 2k\Omega = -\mathbf{97.22}
\end{aligned}
$$

Overall small signal voltage gain,

$$
\begin{aligned}
A_{V_T} &= \frac{V_{out}}{V_S} \\
&= \frac{V_{out}}{V_{o_1}} \times \frac{V_{o_1}}{V_S} \\
&= A_{V_2} \times A_{V_1} \\
&= -97.22 \times -40.123 = \mathbf{3900.7580}
\end{aligned}
$$

Overall voltage gain in dB,

$$|A_{V_T}|_{dB} = 20 \log_{10}(3900.7580) = \mathbf{71.82dB}$$

Output voltage,

$$
\begin{aligned}
V_{out} &= A_{V_T} \times V_S \\
&= 3900.7580 \times 0.4mV = \mathbf{1.560V}
\end{aligned}
$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

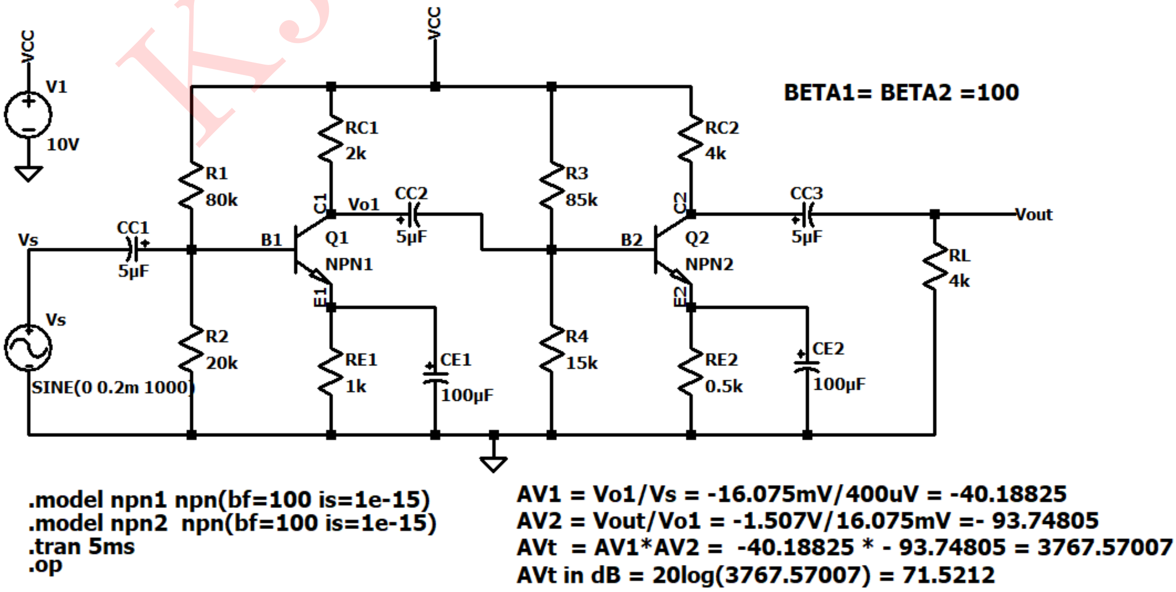

Figure 5: Circuit Schematic

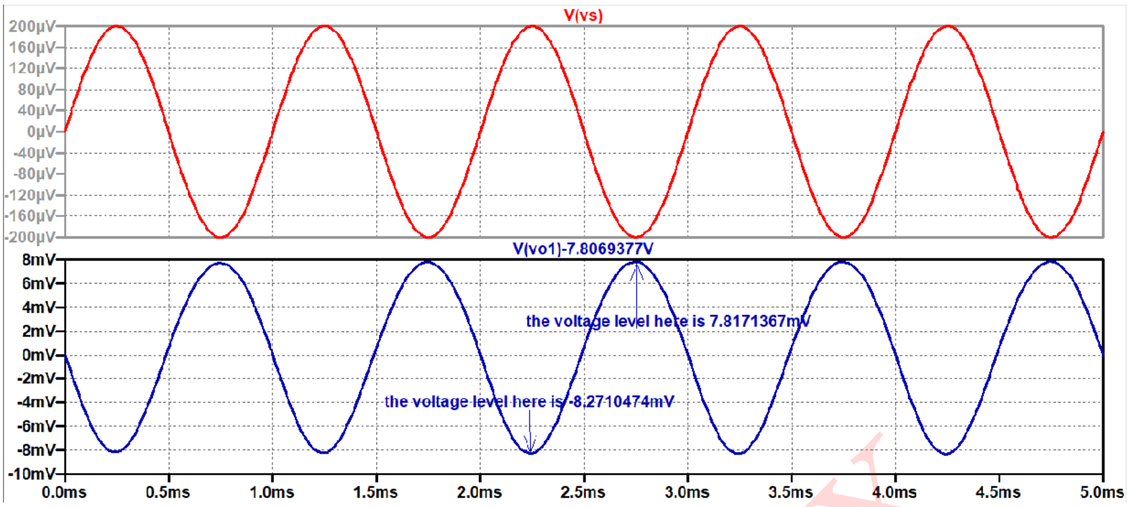

Figure 6: Input and ouput waveforms for Stage 1 voltage gain

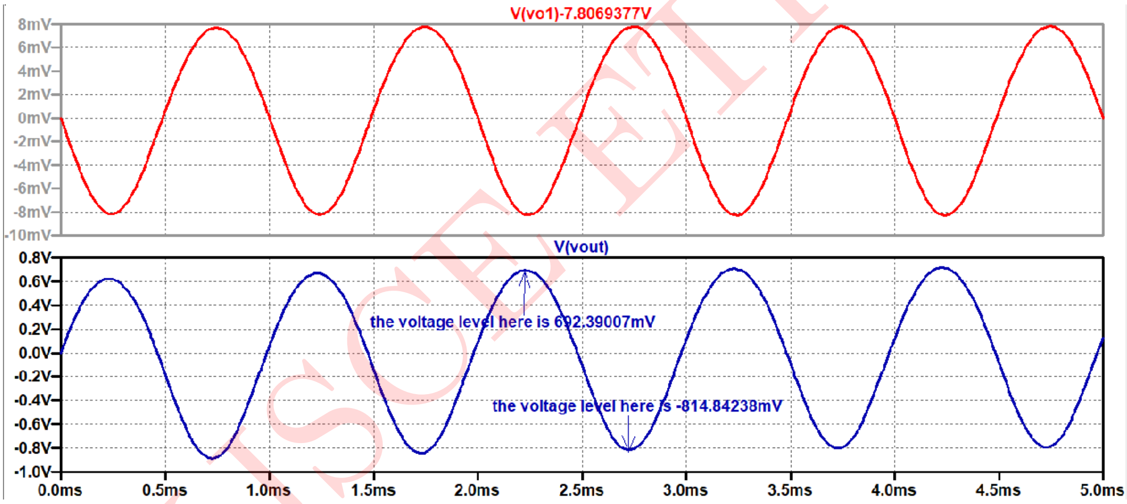

Figure 7: Input and ouput waveforms for Stage 2 voltage gain

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
1^{st} stage Q-point I_{C_1Q}, V_{CE_1Q}	1.111mA, 6.658V	1.0965mA, 6.6994V
2^{nd} stage Q-point I_{C_2Q}, V_{CE_2Q}	1.264mA, 4.3115V	1.23305mA, 4.4450V
Voltage gain of 1st stage: A_{V1}	-40.123	-40.18825
Voltage gain of 2nd stage: A_{V2}	-97.22	-98.7480
Overall voltage gain: A_{V_T} in dB	71.82dB	71.52dB
Input impedance of 1st stage (Z_i)	2.041kΩ	–
Output impedance of 2nd stage (Z_o)	2kΩ	–
Output voltage (V_o)	1.560V	1.5078V

Table 1: Numerical 1

Numerical 2:
A two stage circuit is shown in figure 8 below, BJT paramters are $V_{BE} = 0.7V$, $\beta = 200$, JFET parameters are $I_{DSS} = 10mA$, $V_P = -4V$

a) Determine the Q point for both stages
b) Draw mid-frequency equivalent circuit
c) Calculate A_{V_1} and A_{V_2}
d) Calculate A_{V_T} in dB
e) Calculate V_{out} if $V_S = 2mV_{p-p}$
f) Calculate Z_i and Z_o

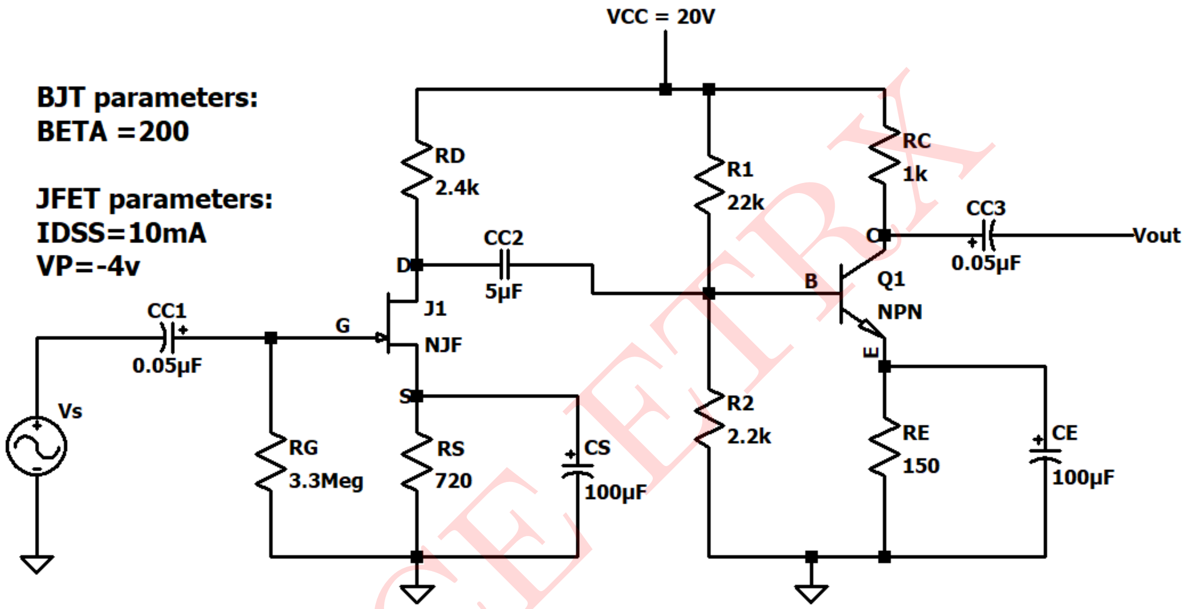

Figure 8: Circuit 2

Solution:
Since RC coupling is employed, DC analysis of both stages can be performed individually.

DC analysis of JFET:
Applying KVL to gate-source loop,

$-I_g R_G - V_{GS} - I_D R_S = 0$

i.e $0 - V_{GS} - I_D R_S = 0 \qquad (\because I_g = 0, I_g R_G = 0)$

$\therefore V_{GS} = -I_D R_S$

$\therefore V_{GS} = -I_D(720\Omega)$

$V_{GS} = -720 I_D \qquad ....(1)$

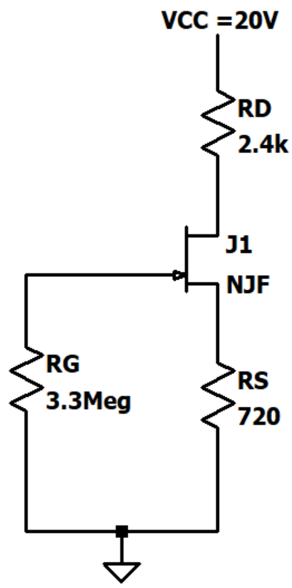

Figure 9: DC equivalent circuit of stage 1

In JFET,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$\therefore I_D = 10mA\left(1-\frac{V_{GS}}{(-4V)}\right)^2$$

$$\therefore I_D = 10mA\left(1+\frac{V_{GS}}{4V}\right)^2 \qquad ....(2)$$

Put (2) in (1), we get

$$V_{GS} = -720 \times \left[10mA\left(1+\frac{V_{GS}}{4}\right)^2\right]$$

$$V_{GS} = -720 \times 10mA\left(1+\frac{2V_{GS}}{4}+\frac{{V_{GS}}^2}{16}\right)$$

$$V_{GS} = -7.2\left(1+\frac{V_{GS}}{2}+\frac{{V_{GS}}^2}{16}\right)$$

$$V_{GS} = -7.2 - 3.6V_{GS} - 0.45{V_{GS}}^2$$

$$0 = -7.2 - 4.6V_{GS} - 0.45{V_{GS}}^2$$

$\therefore V_{GS} = -1.929V$ or $V_{GS} = -8.292V$

We reject the value $V_{GS} = -8.292V$ because $V_{GSQ} > V_P$

$\therefore V_{GS} = \mathbf{-1.929V}$

$$\therefore I_{DQ} = I_{DSS}\left(1-\frac{V_{GSQ}}{V_P}\right)^2$$

$$\therefore I_{DQ} = 10mA\left(1-\frac{(-1.929V)}{(-4V)}\right)^2$$

$$\therefore I_{DQ} = 10mA\left(1-\frac{1.929V}{4V}\right)^2$$

$\therefore I_{DQ} = 10mA\,(1 - 0.48225)^2$

$\therefore I_{DQ} = 10mA\,(0.51775)^2 = \mathbf{2.678mA}$

Small signal parameters of JFET:

i) $g_{m_1} = \dfrac{2I_{DSS}}{|V_P|}\left(1 - \dfrac{V_{GSQ}}{V_P}\right)$

$$= \frac{2 \times 10mA}{4V}\left(1 - \frac{(-1.929)}{(-4)}\right)$$

$$= 5mA/V\,(1 - 0.48225)$$

$$= 5mA/V\,(0.51775) = \mathbf{2.588mA/V}$$

$r_d = \infty$

DC analysis of BJT:

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{2.2k\Omega}{22k\Omega + 2.2k\Omega} \times 20V = \mathbf{1.8V}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{22k\Omega \times 2.2k\Omega}{22k\Omega + 2.2k\Omega} = \mathbf{2k\Omega}$$

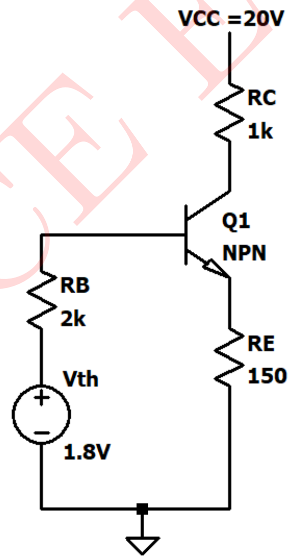

Figure 10: Thevenin's equivalent circuit of stage 2

Applying KVL to base-emitter loop,

$V_{th} - I_B R_B - V_{BE} - I_E R_E = 0$

i.e $V_{th} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$

$\therefore 1.8V - I_B(2k\Omega) - 0.7V - (201) I_B(150\Omega) = 0$

$\therefore 1.1V - I_B(2k\Omega + 201(150\Omega)) = 0$

$I_B = \dfrac{1.1V}{2k\Omega + 30.15k\Omega} = \mathbf{34.214\mu A}$

$\therefore I_C = \beta I_B = (200)(34.214\mu A) = \mathbf{6.842mA}$

$\therefore I_E = (\beta + 1) I_B = (200 + 1)(34.214\mu A) = \mathbf{6.877mA}$

Applying KVL to collector emitter loop,

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$20V - (6.842mA)(1k\Omega) - V_{CE} - (6.877mA)(150\Omega) = 0$

$20V - 6.842V - V_{CE} - 1.031V = 0$

$\therefore V_{CEQ} = 20 - 7.873 = \mathbf{12.126V}$

Small signal parameters of BJT:

i) $r_\pi = \dfrac{\beta V_T}{I_{CQ}} = \dfrac{200 \times 26mV}{6.842mA} = \mathbf{0.76k\Omega}$

ii) $g_{m_2} = \dfrac{I_{CQ}}{V_T} = \dfrac{6.842mA}{26mV} = \mathbf{263.15mA/V}$

iii) $r_o = \infty$

Mid-band AC equivalent circuit:

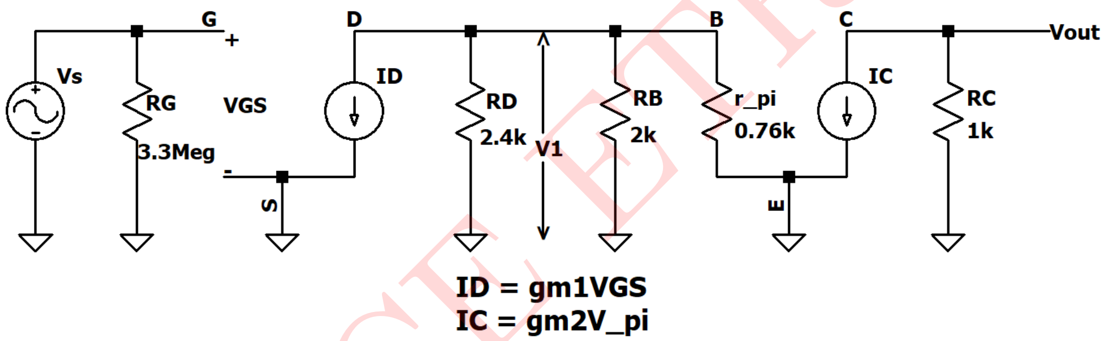

Figure 11: Mid-band AC equivalent circuit

Input impedance of 1^{st} stage

$Z_i = R_G = \mathbf{3.3M\Omega}$

Output impedance of 2^{nd} stage

$Z_o = R_C = \mathbf{1k\Omega}$

$$A_{V_1} = \frac{V_1}{V_S}$$

$$= \frac{(-g_{m_1} V_{gs})(R_D \parallel R_B \parallel r_\pi)}{V_{gs}}$$

$$= -g_{m_1}(R_D \parallel R_B \parallel r_\pi)$$

$$= -2.588mA/V(2.4k\Omega \parallel 2k\Omega \parallel 0.76k\Omega)$$

$$= -2.588mA/V\left[2.4k\Omega \parallel \left(\frac{2k\Omega \times 0.76k\Omega}{2k\Omega + 0.76k\Omega}\right)\right]$$

$$= -2.588mA/V[2.4k\Omega \parallel 0.55k\Omega]$$

$$= -2.588mA/V \times 0.44k\Omega = \mathbf{-1.158}$$

$$
\begin{aligned}
A_{V_2} &= \frac{V_{out}}{V_1} \\
&= \frac{-g_{m_2} V_\pi R_C}{V_\pi} \\
&= -g_{m_2} R_C \\
&= -263.15 mA/V \times 1k\Omega = -\mathbf{263.15}
\end{aligned}
$$

Overall small signal voltage gain,

$$
\begin{aligned}
A_{V_T} &= \frac{V_{out}}{V_S} \\
&= \frac{V_{out}}{V_1} \times \frac{V_1}{V_S} \\
&= A_{V_2} \times A_{V_1} \\
&= -263.15 \times -1.158 = \mathbf{304.733}
\end{aligned}
$$

Overall voltage gain in dB,

$|A_{V_T}|_{dB} = 20 \log_{10}(304.733) = \mathbf{49.678dB}$

$\because A_{V_T} = \frac{V_{out}}{V_S}$

$\therefore V_{out} = A_{V_T} \times V_S = 304.733 \times 2mV = \mathbf{0.60V}$

i.e $V_{out} = 0.60V$ for $V_S = 2mV_{P-P}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

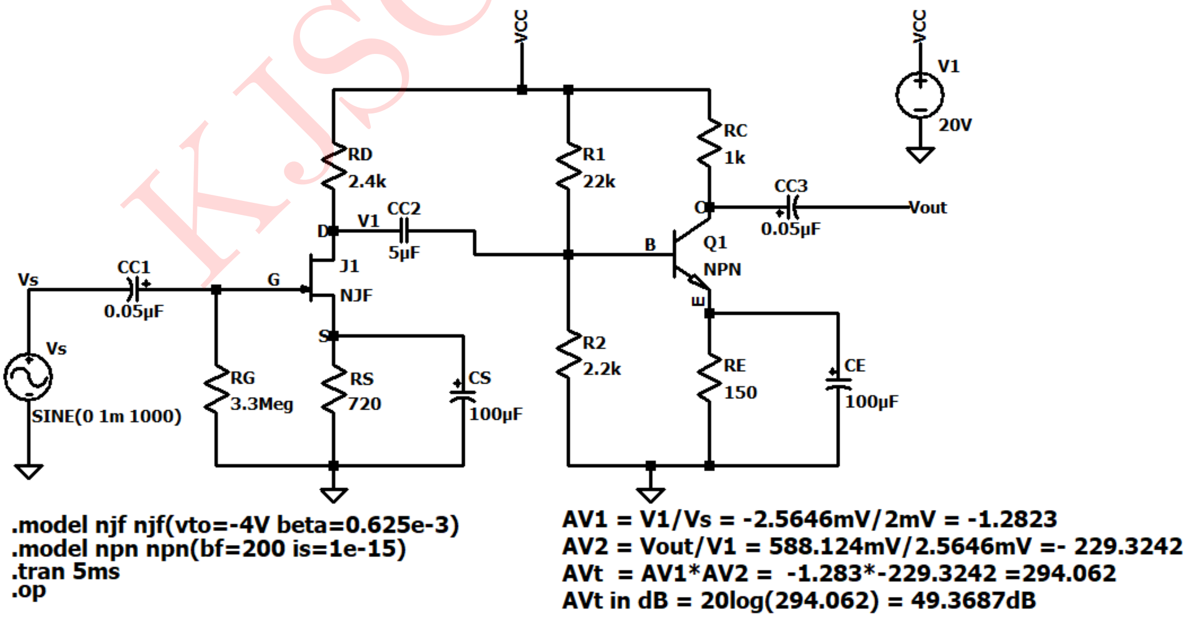

Figure 12: Circuit Schematic

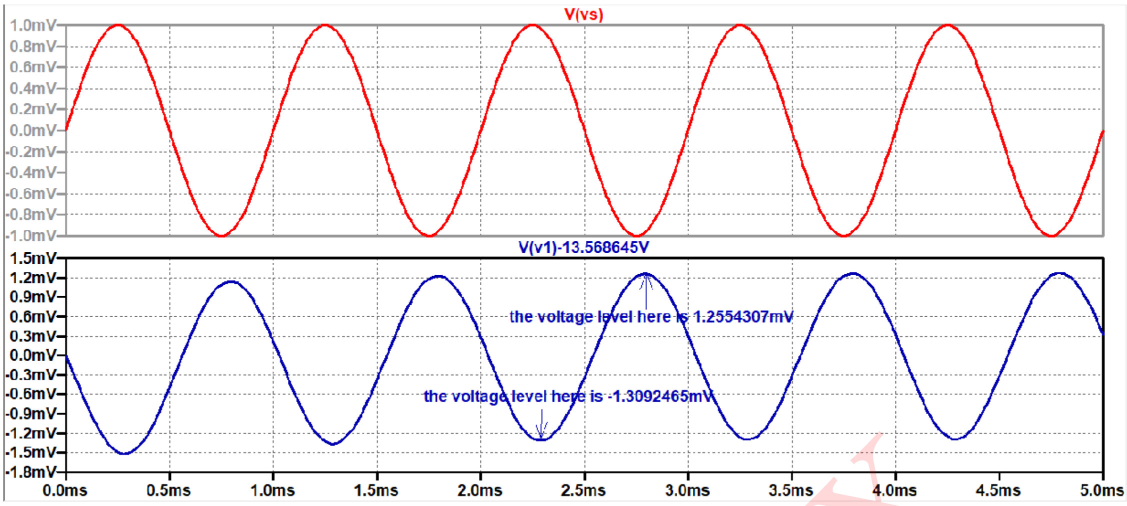

Figure 13: Input and ouput waveforms for Stage 1 voltage gain

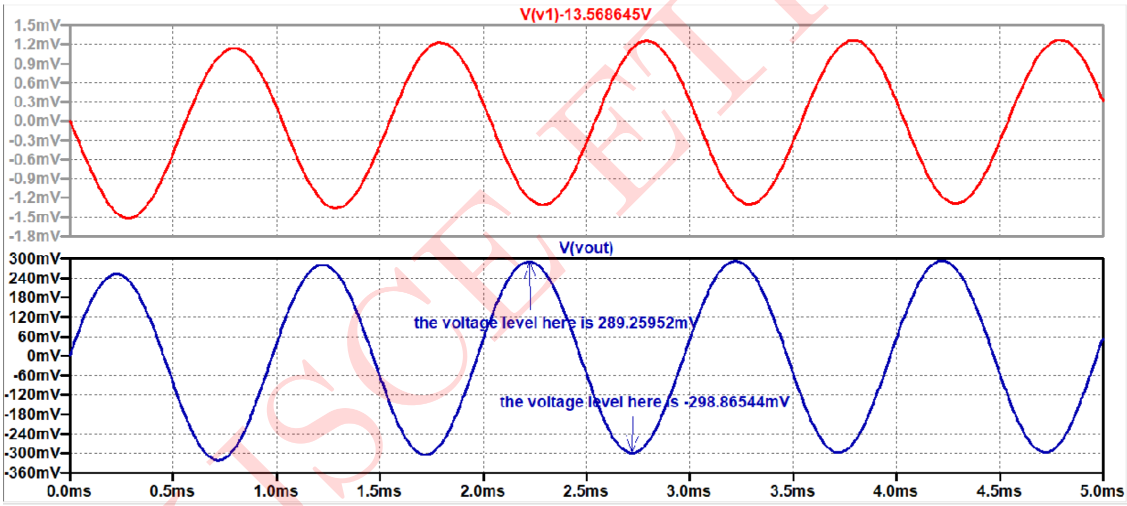

Figure 14: Input and ouput waveforms for Stage 2 voltage gain

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
1st stage Q-point I_{DQ}, V_{GSQ}	2.678mA, −1.929V	2.6797mA, −1.9294V
2nd stage Q-point I_{CQ}, V_{CEQ}	6.842mA, 12.126V	6.5620mA, 12.4487V
Voltage gain of 1st stage: A_{V1}	−1.158	−1.2823
Voltage gain of 2nd stage: A_{V2}	−263.15	−229.3242
Overall voltage gain: A_{V_T} in dB	49.678dB	49.3687dB
Input impedance of 1st stage (Z_i)	3.3MΩ	–
Output impedance of 2nd stage (Z_o)	1kΩ	–
Output voltage (V_o)	0.60V	0.5882V

Table 2: Numerical 2

Numerical 3:
A two stage circuit is shown in figure 15 below, BJT paramters are $V_{BE_1} = V_{BE_2} = 0.6V$, $\beta_1 = \beta_2 = 100$
a) Determine all node voltages and terminal currents under DC analysis
b) Determine overall voltage gain of the circuit

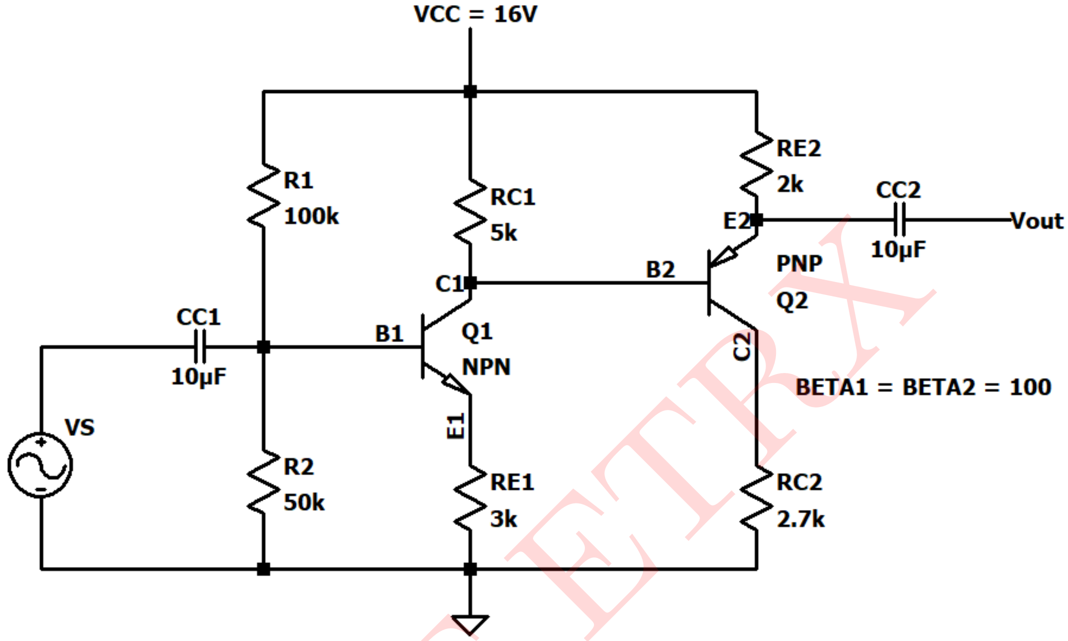

Figure 15: Circuit 3

Solution:
DC analysis:
Considering the thevenin's equivalent of base circuit of transistor Q_1,

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{50k\Omega}{100k\Omega + 50k\Omega} \times 16V = \mathbf{5.33V}$$

$$R_{B_1} = \frac{R_1 R_2}{R_1 + R_2} = \frac{50k\Omega \times 100k\Omega}{50k\Omega + 100k\Omega} = \mathbf{33.33k\Omega}$$

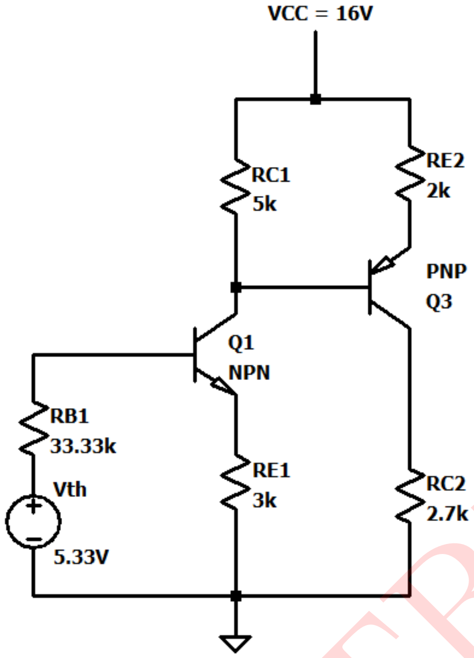

Figure 16: DC equivalent circuit

Applying KVL to base-emitter loop of transistor Q_1,

$V_{th_1} - I_{B_1}R_{B_1} - V_{BE_1} - I_{E_1}R_{E_1} = 0$

i.e $V_{th_1} - I_{B_1}R_{B_1} - V_{BE_1} - (\beta_1 + 1)I_{B_1}R_{E_1} = 0$

$\therefore 5.33V - I_{B_1}(33.33k\Omega) - 0.6V - (101)I_{B_1}(3k\Omega) = 0$

$\therefore 4.73V - I_{B_1}(33.33k\Omega + 101(3k\Omega)) = 0$

$$I_{B_1} = \frac{4.73V}{33.33k\Omega + 303k\Omega} = \mathbf{14.063\mu A}$$

$\therefore I_{C_1} = \beta I_{B_1} = (100)(14.063\mu A) = \mathbf{1.4063mA}$

$\therefore I_{E_1} = (\beta + 1)I_{B_1} = (100 + 1)(14.063\mu A) = \mathbf{1.420mA}$

$V_{C_1} = V_{CC} - I_{C_1}R_{C_1}$ (Ignoring I_{B_2} and $I_{RC} \approx I_{C_1}$) ....(1)

$\therefore V_{C_1} = 16 - 1.4063mA(5k\Omega)$

$\therefore V_{C_1} = 16 - 7.0315 = \mathbf{8.968V}$

$V_{E_2} = V_{B_2} + V_{EB_2(ON)}$

$\therefore V_{E_2} = V_{C_1} + V_{EB_2(ON)}$ $(\because I_{B_2}$ and $I_{RC} \approx I_{C_1})$

$\therefore V_{E_2} = 8.968V + 0.6V = \mathbf{9.568V}$

According to KCL at emitter of transistor Q_2,

$$I_{E_2} = \frac{V_{CC} - V_{E_2}}{R_{E_2}}$$

$$\therefore I_{E_2} = \frac{16V - 9.568V}{2k\Omega}$$

$$\therefore I_{E_2} = \frac{6.432V}{2k\Omega} = \mathbf{3.216mA}$$

$$\because I_{C_2} = \frac{\beta_2}{1+\beta_2} \times I_{E_2}$$
$$= \frac{100}{101} \times 3.216mA = \mathbf{3.184mA}$$

$$\because I_{B_2} = \frac{I_{E_2}}{1+\beta_2}$$
$$= \frac{3.216mA}{101} = \mathbf{31.814\mu A}$$

Now, rewriting exact expression for equation (1)

$V_{C_1} = V_{CC} - I_{RC_1} R_{C_1}$

$\therefore I_{RC_1} = I_{C_1} - I_{B_2}$

$\therefore I_{RC_1} = 1.4063mA - 31.841\mu A = \mathbf{1.374mA}$

$\therefore V_{C_1new} = 16 - (1.374mA)(5k\Omega) = \mathbf{9.13V}$

$\therefore V_{E_2new} = V_{C_1new} + V_{EB_2(ON)}$

$\therefore V_{E_2new} = 9.13V + 0.6V = \mathbf{9.73V}$

$$\therefore I_{E_2new} = \frac{V_{CC} - V_{E_2new}}{R_{E_2}}$$
$$= \frac{16V - 9.73V}{2k\Omega} = \mathbf{3.135mA}$$

$$\therefore I_{C_2new} = \frac{\beta_2}{1+\beta_2} \times I_{E_2new}$$
$$= \frac{100}{101} \times 3.135mA = \mathbf{3.103mA}$$

$$\therefore I_{B_2new} = \frac{I_{E_2new}}{1+\beta_2}$$
$$= \frac{3.135mA}{101} = \mathbf{31.039\mu A}$$

$$\because V_{E_1} = I_{E_1} R_{E_1}$$
$$= (1.420mA)(3k\Omega) = \mathbf{4.26V}$$

$$\because V_{C_2} = I_{C_2} R_{C_2}$$
$$= (3.184mA)(2.7k\Omega) = \mathbf{8.596V}$$

$$\because V_{B_1} = V_{BE_1(ON)} + V_{E_1}$$
$$= 0.6V + 4.26V = \mathbf{4.86V}$$

Node voltages:

$V_{B_1} = 4.86V$

$V_{C_1} = 9.13V$

$V_{E_1} = 4.26V$

$V_{C_2} = 8.596V$

$V_{E_2} = 9.73V$

$V_{B_2} = 9.13V$

Terminal currents:

$I_{B_1} = 14.063\mu A$
$I_{C_1} = 1.4063mA$
$I_{E_1} = 1.420mA$
$I_{B_2} = 31.039\mu A$
$I_{C_2} = 3.103mA$
$I_{E_2} = 3.135mA$

Small signal parameters:

$$r_{\pi_1} = \frac{\beta_1 V_T}{I_{CQ_1}} = \frac{100 \times 26mV}{1.4063mA} = \mathbf{1.848k\Omega}$$

$$r_{\pi_2} = \frac{\beta_2 V_T}{I_{CQ_2}} = \frac{100 \times 26mV}{3.103mA} = \mathbf{837.89\Omega}$$

Mid-frequency AC equivalent circuit:

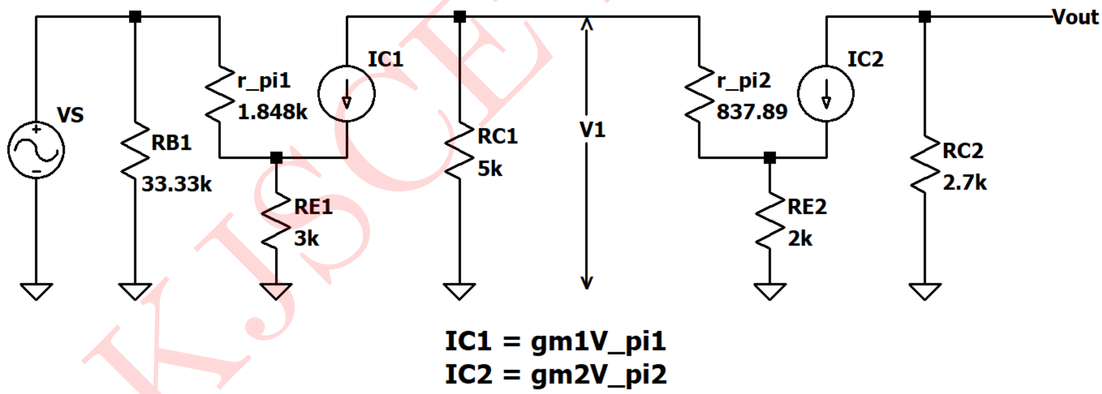

Figure 17: Mid-frequency AC equivalent circuit

$$\begin{aligned} A_{V_1} &= \frac{V_1}{V_S} \\ &= \frac{(-g_{m_1} V_{\pi_1}) R_{C_1}}{I_{B_1}[r_{\pi_1} + (1+\beta_1) R_{E_1}]} \\ &= \frac{-(\beta_1 I_{B_1}) R_{C_1}}{I_{B_1}[r_{\pi_1} + (1+\beta_1) R_{E_1}]} \\ &= \frac{-\beta_1 R_{C_1}}{r_{\pi_1} + (1+\beta_1) R_{E_1}} \\ &= \frac{-100 \times 5k\Omega}{1.848k\Omega + (1+100)3k\Omega} = \mathbf{-1.640} \end{aligned}$$

$$
\begin{aligned}
A_{V_2} &= \frac{V_o}{V_1} \\
&= \frac{(g_{m_2} V_{\pi_2}) R_{E_2}}{I_{B_2}[r_{\pi_2} + (1+\beta_2)R_{E_2}]} \\
&= \frac{(\beta_2 I_{B_2}) R_{E_2}}{I_{B_2}[r_{\pi_2} + (1+\beta_2)R_{E_2}]} \\
&= \frac{\beta_2 R_{E_2}}{r_{\pi_2} + (1+\beta_2)R_{E_2}} \\
&= \frac{100 \times 2k\Omega}{837.89\Omega + (1+100)2k\Omega} = \mathbf{0.986}
\end{aligned}
$$

Overall voltage gain,

$$
\begin{aligned}
\therefore V_{out} &= A_{V_T} \times A_{V_2} \\
&= -1.640 \times 0.986 = -\mathbf{1.617}
\end{aligned}
$$

$$
\because A_{V_T} = \frac{V_{out}}{V_S}
$$

$$
\begin{aligned}
\therefore V_{out} &= A_{V_T} \times V_S \\
&= -1.617 \times 40mV = -\mathbf{64.68V}
\end{aligned}
$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

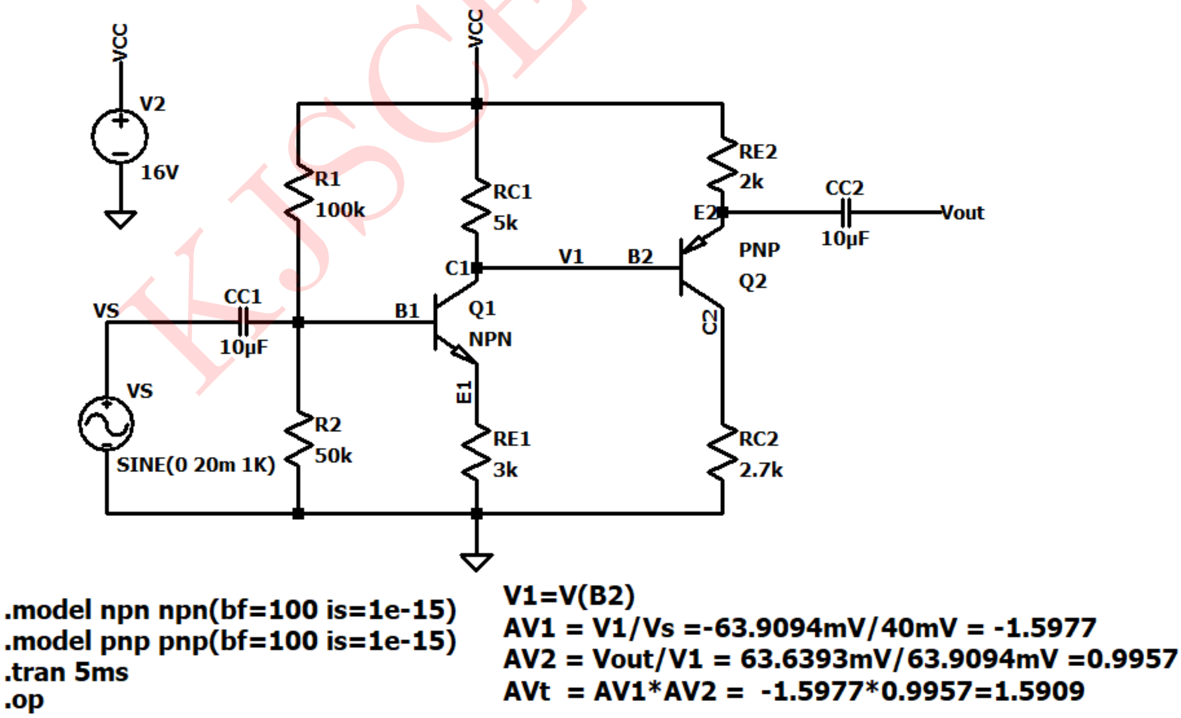

Figure 18: Circuit Schematic

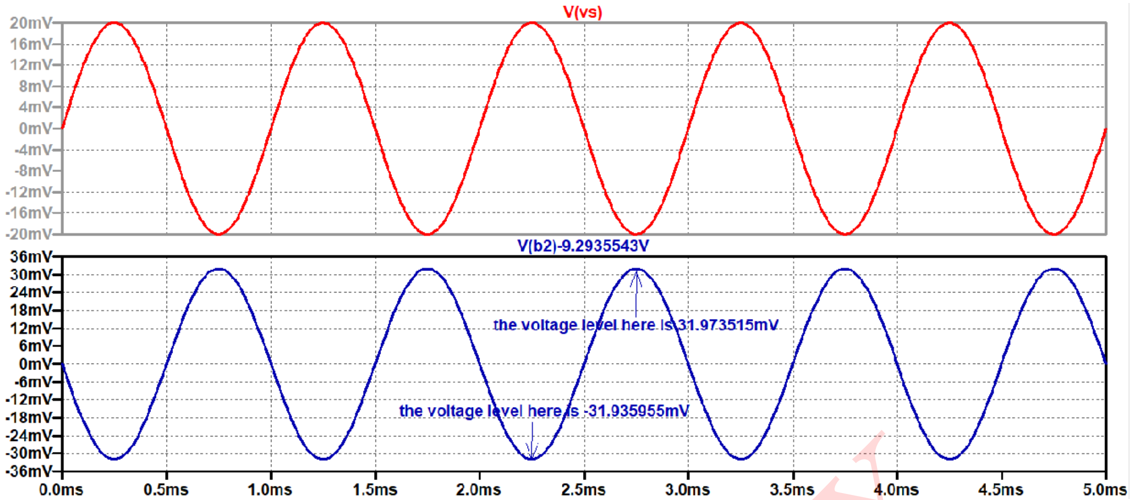

Figure 19: Input and ouput waveforms for Stage 1 voltage gain

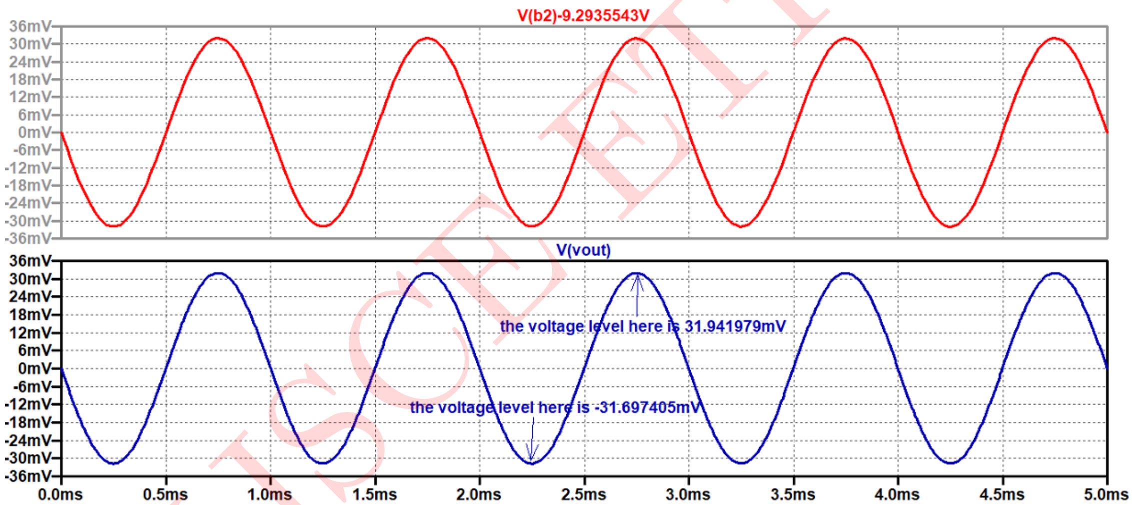

Figure 20: Input and ouput waveforms for Stage 2 voltage gain

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
I_{B_1}	14.063μA	13.7081μA
I_{C_1}, I_{E_1}	1.4063mA, 1.420mA	1.3708mA, 1.3845mA
I_{B_2}	31.039μA	29.5236μA
I_{C_2}, I_{E_2}	3.103mA, 3.135mA	2.9523mA, 2.98188mA
V_{C_1}	9.13V	9.2935V
V_{C_2}	8.596V	7.9718V
V_{E_1}	4.26V	4.1535V
V_{E_2}	9.73V	10.0362V
V_{B_1}	4.86V	4.8764V
V_{B_2}	9.13V	9.2935V
A_{V_T}	-1.617	-1.5909
V_{out}	-64.68mV	-63.6393mV

Table 3: Numerical 3

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