K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
DC Biasing Circuits

Numerical 1:
Determine I_{D_Q}, V_{GS_Q}, V_{DS} for the network given in figure 1.

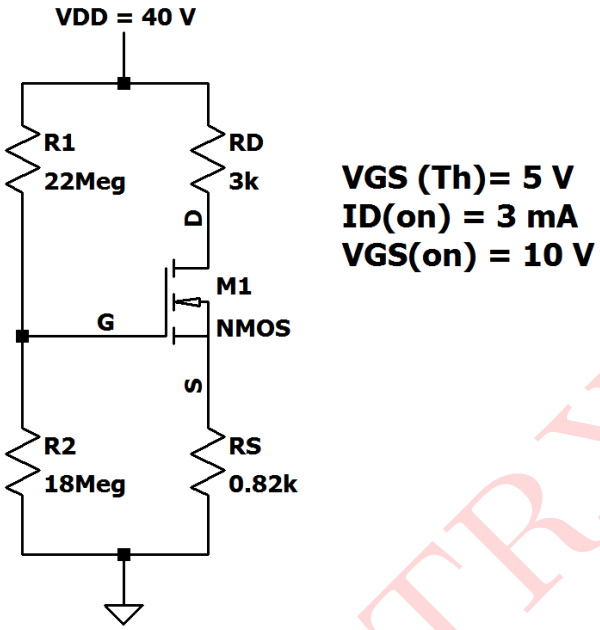

Figure 1: Circuit 1

Solution:

Figure 1 is a voltage divider E-MOSFET network

By using voltage divider rule:

$$V_G = \frac{R_2}{R_1 + R_2} \times 40 = \frac{18M\Omega}{18M\Omega + 22M\Omega} \times 40 = 18\text{V}$$

$$\boldsymbol{V_G = 18V}$$

For E-NMOS transistor,

$$k_n = \frac{I_{D_{on}}}{[V_{GS_{on}} - V_{GS_{th}}]^2}$$

$$k_n = \frac{3mA}{[10-5]^2} = 0.12\frac{mA}{V^2}$$

$$\boldsymbol{k_n = 0.12\frac{mA}{V^2}}$$

$$V_{GS} = V_G - V_S = V_G - I_D R_S = 18 - I_D(820)$$

$$V_{GS} = 18 - I_D \times (820) \quad \text{.....(1)}$$

Assuming that given NMOS-E transistor is working in saturation region,

$$I_D = k_n \times (V_{GS} - V_{GS_{th}})^2$$

$$I_D = 0.12 \times 10^{-3} \times (V_{GS} - 5)^2 \quad \text{.....(2)}$$

Put (2) in (1), we get

$V_{GS} = 18 - 820 \times 0.12 \times 10^{-3} \times (V_{GS} - 5)^2$

$= 18 - 0.0984 \times (V_{GS} - 5)^2$

$V_{GS} = 18 - 0.0984{V_{GS}}^2 + 0.984V_{GS} - 2.46$

$0.0984{V_{GS}}^2 + 0.016V_{GS} - 15.54 = 0$

Solving above equation we get,

$V_{GS} = 12.48V$

or

$V_{GS} = -12.64V$, We reject this value, as $(V_{GS} > V_{GS_{th}})$

$\therefore \boldsymbol{V_{GS} = 12.48V}$

$I_D = k_n \times (V_{GS} - 5)^2$

$= 0.12 \times 10^{-3} \times (12.48 - 5)^2$

$\boldsymbol{I_D = 6.72mA}$

Now, Applying KVL in Drain-Source loop,

$V_{DS} = V_{DD} - I_D \times (R_D + R_S)$

$= 40 - 6.72 \times (3k + 820)$

$\boldsymbol{V_{DS} = 14.32V}$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

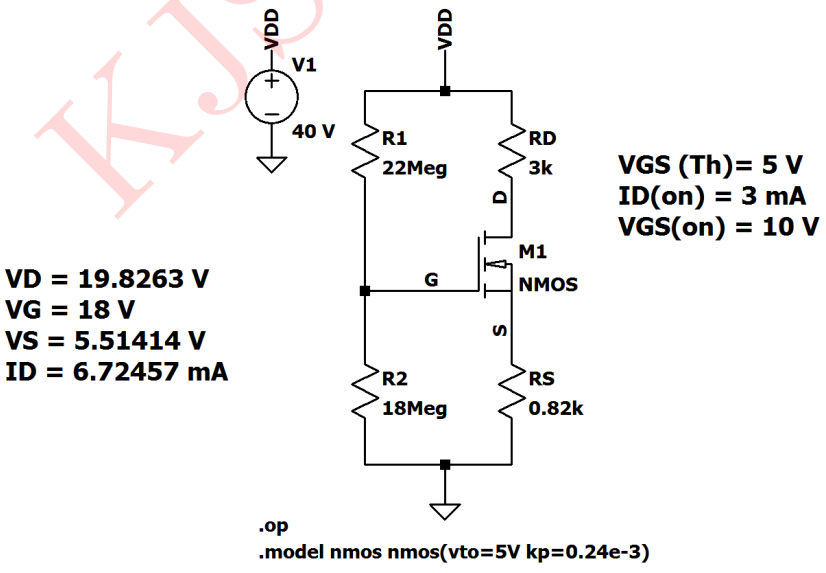

Figure 2: Circuit Schematic 1: Results

Comparison between theoretical and simulated result:

Parameters	Theoretical	Simulated
V_{GS}	12.48V	12.48V
I_D	6.72mA	6.724mA
V_{DS}	14.32V	14.31V

Table 1: Question 1

Numerical 2:
Determine I_D, V_{GS}, V_{DS} for the network given in figure 3.

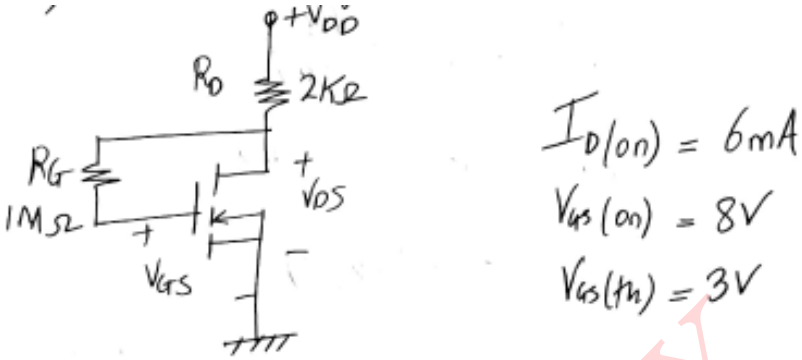

Figure 3: Circuit 2

Solution:

$$k_n = \frac{I_{D_{on}}}{[V_{GS_{on}} - V_{GS_{th}}]^2}$$

$$k_n = \frac{6mA}{[8-3]^2} = 0.24\frac{mA}{V^2}$$

$$\boldsymbol{k_n = 0.24\frac{mA}{V^2}}$$

$$V_{GS} = V_{DD} - I_D R_D = 12 - I_D(2000)$$

$$V_{GS} = 12 - I_D \times (2000) \quad \text{.....(1)}$$

Assuming that given NMOS-E transistor is working in saturation region,

$$I_D = k_n \times (V_{GS} - V_{GS_{th}})^2$$

$$I_D = 0.24 \times 10^{-3} \times (V_{GS} - 3)^2 \quad \text{.....(2)}$$

Put (2) in (1), we get

$$V_{GS} = 12 - 0.48 \times (V_{GS} - 3)^2$$

$$= 12 - 0.48 \times ({V_{GS}}^2 - 6V_{GS} + 9)$$

$$V_{GS} = 12 - 0.48{V_{GS}}^2 + 2.88V_{GS} - 4.32$$

$$0.48{V_{GS}}^2 - 1.88V_{GS} - 7.68 = 0$$

Solving above equation we get,

$$V_{GS} = 6.41$$

or

$V_{GS} = -2.49V$, We reject this value, as $(V_{GS} > V_{GS_{th}})$

$$\therefore \boldsymbol{V_{GS} = 6.41V}$$

$$\therefore \boldsymbol{V_{DS} = V_{GS} = 6.41V}$$

$$I_D = k_n \times (V_{GS} - 3)^2$$

$$= 0.24 \times 10^{-3} \times (6.41 - 3)^2$$

$$\boldsymbol{I_D = 2.79mA}$$

Numerical 3:
Determine I_D, V_{GS}, V_{DS} for the network given in figure 4.

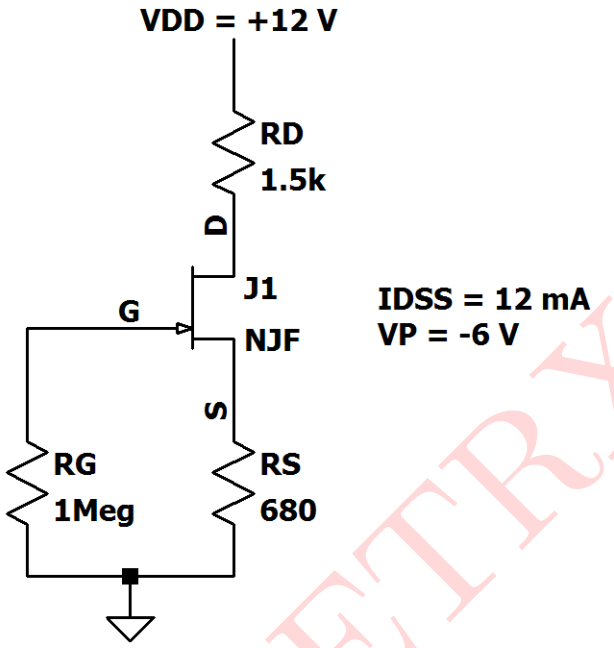

Figure 4: Circuit 3

Solution:

Above circuit 3 is self-biased N-Channel JFET

Applying KVL in gate-source loop:

$-V_{GS} - I_D R_S = 0$

$V_G = -I_D R_S = -680 \times I_D$

For JFET, we assume it in saturation region

$$I_D = I_{DSS} \times \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 12 \times 10^{-3} \times \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$-\frac{V_{GS}}{680} = \frac{12}{1000} \times \left(1 + \frac{V_{GS}}{6}\right)^2$$

$-0.122V_{GS} = 1 + 0.027{V_{GS}}^2 + 0.33V_{GS}$

$0.027{V_{GS}}^2 + 0.455V_{GS} + 1 = 0$

Solving above equation we get,

$V_{GS} = -2.598V$

or

$V_{GS} = -14.25V$, We reject this value, as $(V_{GS} > V_P)$

$\therefore \boldsymbol{V_{GS} = -2.598V}$

$$I_D = 12 \times 10^{-3} \times \left(1 - \frac{2.598}{6}\right)^2$$

$$= 12 \times 10^{-3} \times (0.568)^2 = 3.87mA$$

$\boldsymbol{I_D = 3.87mA}$

Applying KVL in Drain-Source loop:

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$V_{DS} = 12 - 3.84 \times 10^{-3}(1.5 + 0.68) \times 10^3$

$\boldsymbol{V_{DS} = 3.63V}$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

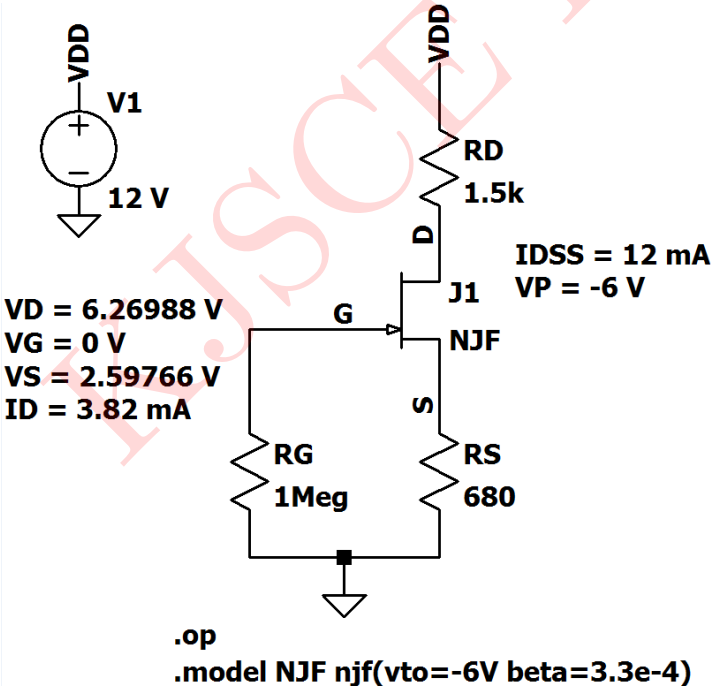

Figure 5: Circuit Schematic 3: Results

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
V_{GS}	3.63V	3.67V
V_{DS}	2.59V	2.597V
I_D	3.87mA	3.82mA

Table 2: Question 3

Numerical 4:
Determine I_D, V_{GS}, V_{DS} and g_m for the network given in figure 6.

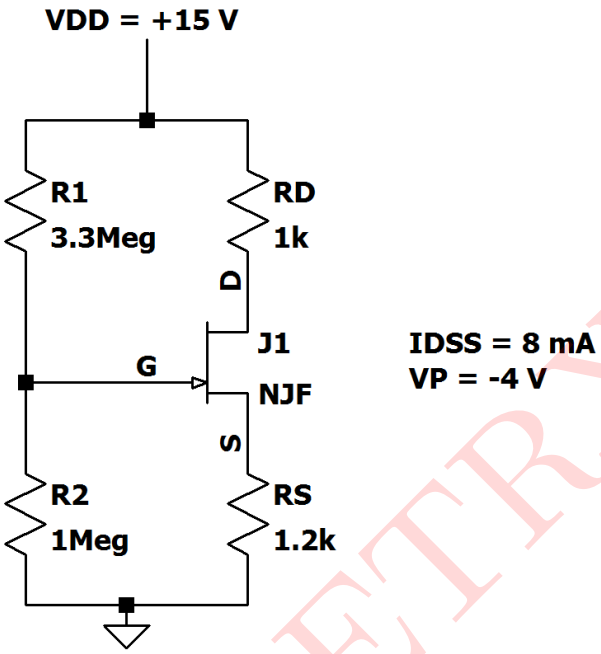

Figure 6: Circuit 4

Solution:

Above circuit 4 is voltage divider biased N-Channel JFET

$$V_G = \left(\frac{1M\Omega}{1M\Omega + 3.3M\Omega}\right) \times 15 = 3.48V$$

$$\boldsymbol{V_G = 3.48V}$$

Now,

$$V_{GS} = V_G - V_S = V_G - I_D R_S = 3.488 - 1200I_D$$

For JFET, we assume it in saturation region

$$I_D = I_{DSS} \times \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$-\frac{3.488 - V_{GS}}{1200} = \frac{8}{1000} \times \left(1 + \frac{V_{GS}}{4}\right)^2$$

$$3.488 - V_{GS} = 9.6 + \frac{9.6}{16}{V_{GS}}^2 + \frac{9.6}{2}V_{GS}$$

Solving above equation we get,

$V_{GS} = -1.2V$

or

$V_{GS} = -8.46V$, We reject this value, as $(V_{GS} > V_P)$

$\therefore \boldsymbol{V_{GS} = -1.2V}$

$$I_D = 8 \times 10^{-3} \times \left(1 - \frac{1.2}{4}\right)^2$$

$$= 8 \times 10^{-3} \times (0.7)^2 = 3.92mA$$

$\boldsymbol{I_D = 3.92mA}$

Applying KVL in Drain-Source loop:

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$V_{DS} = V_{DD} - I_D \times (R_D + R_S)$

$V_{DS} = 15 - 3.91 \times 10^{-3} \times (1 + 1.2) \times 10^3$

$\boldsymbol{V_{DS} = 6.398V}$

$$g_m = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) = -\frac{2 \times 8 \times 10^{-3}}{4}\left(1 + \frac{1.2}{4}\right)$$

$\boldsymbol{g_m = 2.8\frac{mA}{V}}$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

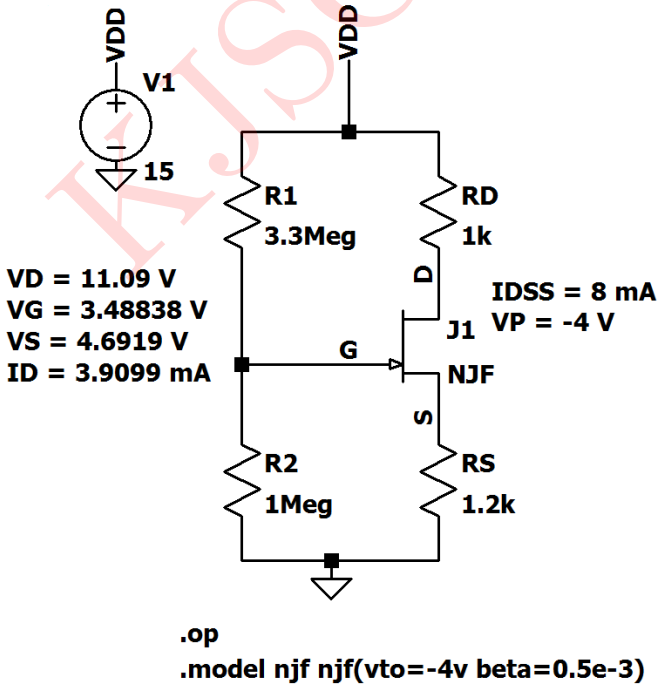

Figure 7: Circuit Schematic 4: Results

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
V_{GS}	1.2V	1.2V
V_{DS}	6.398V	6.398V
I_D	3.91mA	3.909mA

Table 3: Question 4

Numerical 5:
Determine I_{D_Q}, V_{GS_Q}, V_{DS_Q}, V_D, V_S for the network given in figure 8.

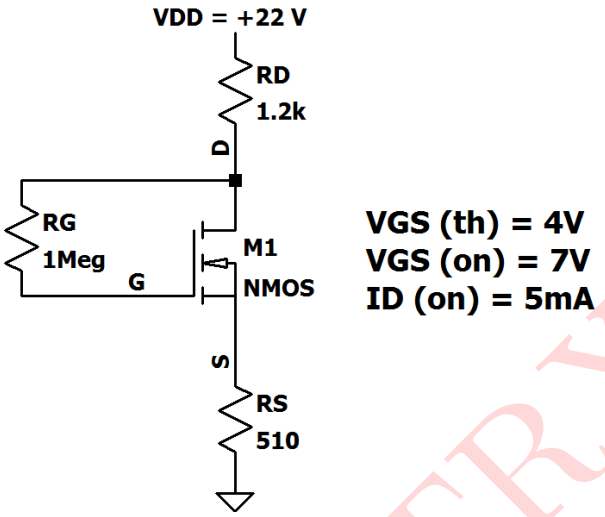

Figure 8: Circuit 5

Solution:

Above circuit 5 is a drain-feedback biased E-NMOS

Applying KVL in gate-source loop:

$V_{DD} - (I_D + I_G)R_D - I_G R_G - V_{GS} - I_D R_S = 0$

For MOSFET, $I_G \approx 0$

$V_{GS} = V_{DD} - I_D(R_D + R_S)$

$V_{GS} = 22 - I_D(1710)$ .....(1)

For E-NMOS transistor,

$$k_n = \frac{I_{D_{on}}}{[V_{GS_{on}} - V_{GS_{th}}]^2} = \frac{5 \times 10^{-3}}{9} = 0.55 \frac{mA}{V^2}$$

$\boldsymbol{k_n = 0.55 \frac{mA}{V^2}}$

Assuming that given NMOS-E transistor is working in saturation region,

$I_D = k_n \times (V_{GS} - V_{GS_{th}})^2$

$I_D = 0.55 \times 10^{-3} \times (V_{GS} - 4)^2$ .....(2)

Put (2) in (1), we get

$V_{GS} = 22 - 0.55 \times 1.71 \times (V_{GS} - 4)^2$

$= 22 - 0.94 \times (V_{GS} - 4)^2$

$V_{GS} = 22 - 0.94({V_{GS}}^2 - 8V_{GS} + 16)$

$0.94{V_{GS}}^2 - 6.52V_{GS} - 6.96 = 0$

Solving the above quadratic equation we get,

$V_{GS} = 7.87V$

or

$V_{GS} = -0.94V$, We reject this value, as $(V_{GS} > V_{GS_{th}})$

$\therefore \boldsymbol{V_{GS} = 7.87V}$

$I_D = k_n \times (V_{GS} - 4)^2$

$= 0.55 \times 10^{-3} \times (7.87 - 4)^2$

$\boldsymbol{I_D = 8.23mA}$

Applying KVL to the drain-source loop,

$V_{DS} = V_{DD} - I_D \times (R_D + R_S)$

$= 22 - 8.23 \times 10^{-3}(1200 + 510)$

$\boldsymbol{V_{DS} = 7.87V}$

$V_S = I_D R_S = 510 \times 8.23 \times 10^{-3} = 4.197V$

$\boldsymbol{V_S = 6.197V}$

$V_D = V_{DD} + V_S = 7.87 + 4.197 = 12.067V$

$\boldsymbol{V_D = 12.067V}$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

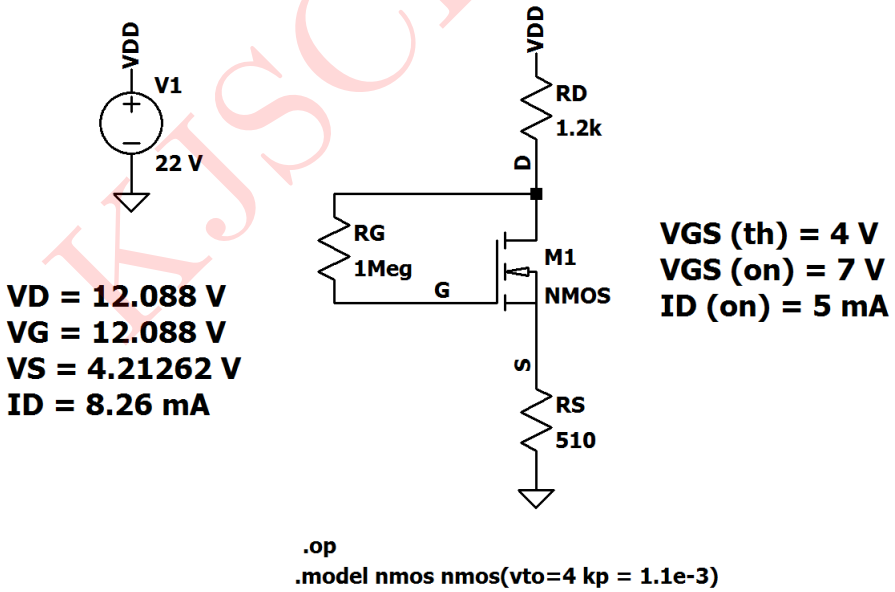

Figure 9: Circuit Schematic 5: Results

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_D	8.23mA	8.26mA
V_D	12.067V	12.088V
V_S	4.197V	4.216V
V_{DS}	7.87V	7.87V
V_{GS}	7.87V	7.87V

Table 4: Question 5

Numerical 6:
Determine I_{D_Q}, V_{GS_Q}, V_D, V_S for the network given in figure 10.

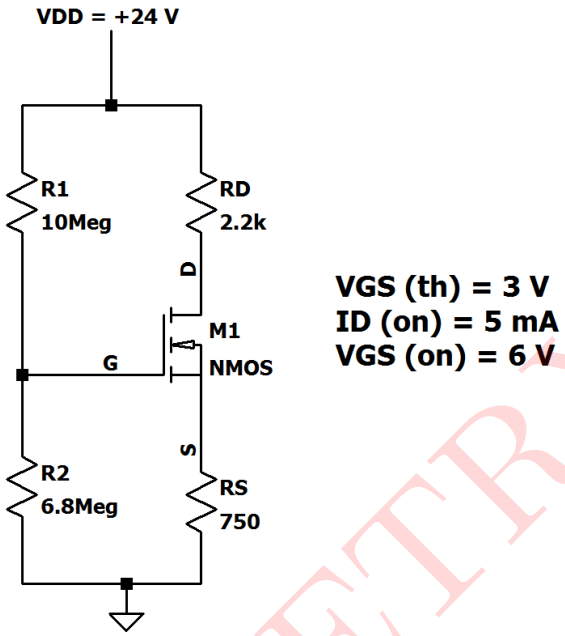

Figure 10: Circuit 6

Solution:

Above circuit 6 is a voltage divider biased E-NMOS

Applying thevenin's equivalent circuit at the gate terminal:

$$R_G = R_1||R_2 = \frac{10M\Omega \times 68M\Omega}{16.8M\Omega} = \mathbf{4.04M\Omega}$$

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{10M\Omega}{16.8M\Omega} \times 24V = \mathbf{9.714V}$$

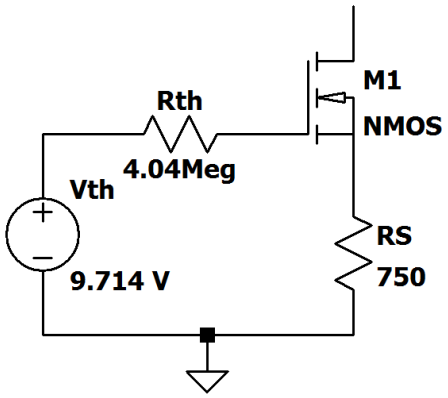

Figure 11: Thevenin's Equivalent Circuit

Applying KVL to the gate-source loop:

$V_G - I_G R_G - V_{GS} - I_D R_S = 0$

For MOSFET, $I_G \approx 0$

$V_{GS} = V_G - I_D R_S$

$V_{GS} = 9.714 - I_D(750)$ .....(1)

For E-NMOS transistor,

$$k_n = \frac{I_{D_{on}}}{[V_{GS_{on}} - V_{GS_{th}}]^2} = \frac{5 \times 10^{-3}}{9} = 0.55 \frac{mA}{V^2}$$

$\boldsymbol{k_n = 0.55 \frac{mA}{V^2}}$

Assuming that given NMOS-E transistor is working in saturation region,

$I_D = k_n \times (V_{GS} - V_{GS_{th}})^2$

$I_D = 0.55 \times 10^{-3} \times (V_{GS} - 3)^2$ .....(2)

Put (2) in (1), we get

$V_{GS} = 9.714 - 0.55 \times 0.74 \times (V_{GS} - 3)^2$

$= 9.714 - 0.4125 \times (V_{GS} - 3)^2$

$V_{GS} = 9.714 - 0.4125({V_{GS}}^2 - 6V_{GS} + 9)$

$0.4125{V_{GS}}^2 - 1.475V_{GS} - 6 = 0$

Solving the above quadratic equation we get,

$V_{GS} = 6V$

or

$V_{GS} = -2.4V$, We reject this value, as $(V_{GS} > V_{GS_{th}})$

$\therefore \boldsymbol{V_{GS} = 6V}$

$I_D = k_n \times (V_{GS} - 3)^2$

$= 0.55 \times 10^{-3} \times (6 - 3)^2$

$\boldsymbol{I_D = 4.95mA}$

Applying KVL to the drain-source loop,

$V_{DS} = V_{DD} - I_D \times (R_D + R_S)$

$= 24 - 4.95 \times 10^{-3}(2.2k + 0.75k)$

$\boldsymbol{V_{DS} = 9.3975V}$

$V_S = I_D R_S = 4.95 \times 10^{-3} \times 750 = 3.7125V$

$\boldsymbol{V_S = 3.7125V}$

$V_D = V_{DS} + V_S = 9.3975 + 3.7125 = 13.11V$

$\boldsymbol{V_D = 13.11V}$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

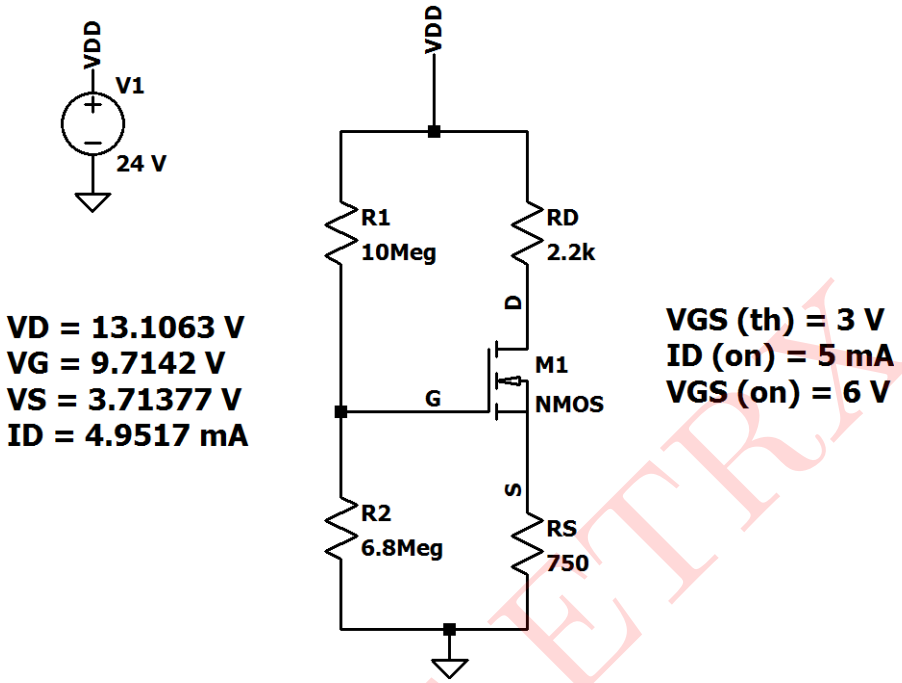

Figure 12: Circuit Schematic 6: Results

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_D	4.95mA	4.95mA
V_{GS}	6V	6V
V_D	13.110V	13.106V
V_S	3.7125V	3.7137V

Table 5: Question 6

Numerical 7:
Determine I_{B_Q}, V_{CE_Q}, I_{C_Q} for $\beta = 80$, also find % change in V_{CE_Q} and I_{C_Q} if β is changed to $\beta = 120$ for the network given in figure 13.

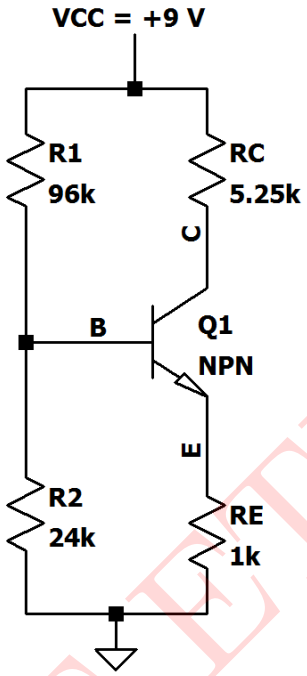

Figure 13: Circuit 7

Solution:

Above circuit 7 is a voltage divider biased employing npn-BJT

Applying thevenin's equivalent circuit at the base terminal:

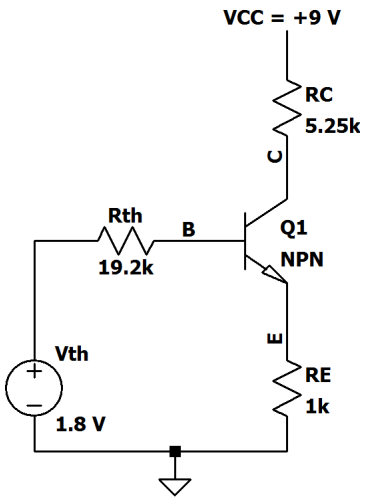

Figure 14: Thevenin's Equivalent Circuit

$$R_{TH} = R_1||R_2 = \frac{24k\Omega \times 96k\Omega}{120k\Omega} = \mathbf{19.2k\Omega}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{24k\Omega}{120k\Omega} \times 9V = \mathbf{1.8V}$$

Applying KVL to the base-emitter loop:

$$V_{TH} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = I_B + I_C = I_B + \beta I_B = (\beta + 1) I_B$$

$$V_{TH} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (\beta + 1) R_E} \quad \text{.....(1)}$$

$$I_B = \frac{1.8 - 0.7}{19.2k\Omega + 81 \times 1k\Omega} = 10.978\mu A$$

$$\boldsymbol{I_B = 10.978\mu A}$$

$$I_C = \beta I_B = 80 \times 10.978\mu A = 0.878mA$$

$$\boldsymbol{I_C = 0.878mA}$$

Applying KVL to the collector-emitter loop:

$$V_{CE} = V_{CC} - R_E \times (I_B + I_C) - I_C R_C \quad \text{.....(2)}$$
$$= 9 - 1k\Omega \times (10.97\mu A + 0.878mA) - (5.25k\Omega \times 0.878mA)$$

$$\boldsymbol{V_{CE} = 3.501V}$$

For $\beta = 120$

Using equation (1),

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (\beta + 1) R_E} = \frac{1.8 - 0.7}{19.2k\Omega + (121 \times 1k\Omega)} = 7.845\mu A$$

$$\boldsymbol{I_B = 7.845\mu A}$$

$$I_C = \beta I_B = 120 \times 7.845\mu A = 0.949mA$$

$$\boldsymbol{I_C = 0.949mA}$$

Using equation (2),

$$V_{CE} = V_{CC} - R_E \times (I_B + I_C) - I_C R_C$$
$$= 9 - 1k\Omega \times (7.84\mu A + 0.949mA) - (5.25k\Omega \times 0.949mA)$$

$$\boldsymbol{V_{CE} = 3.0612V}$$

$$\%\text{ Change in } I_C = \frac{0.949 - 0.878}{0.878} \times 100\% = \mathbf{8.08\%}$$

$$\%\text{ Change in } V_{CE} = \frac{3.501 - 3.061}{3.501} \times 100\% = \mathbf{12.56\%}$$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

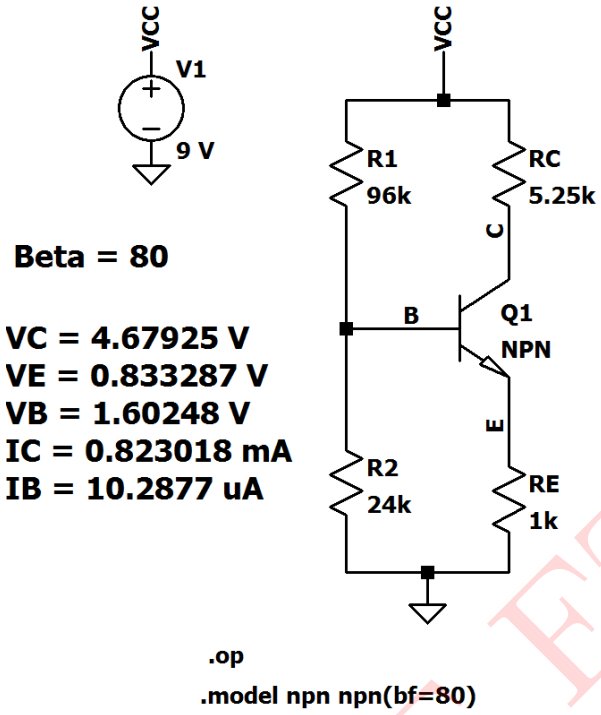

Figure 15: Circuit Schematic 7: Results

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_B	$10.97\mu A$	$10.28\mu A$
I_C	$0.878mA$	$0.823mA$
V_{CE}	$3.501V$	$3.845V$

Table 6: Question 7

Numerical 8:
Determine R_{TH}, V_{TH}, V_{CE_Q} and I_{C_Q} for the network given in figure 16.
Given: $\beta = 100$

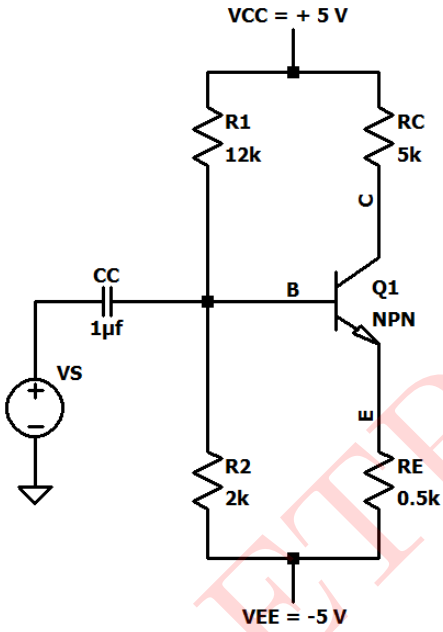

Figure 16: Circuit 8

Solution:

Above circuit 8 is a voltage divider biased employing npn-BJT

For DC analysis, $f = 0$,

$$X_C = \frac{1}{2\pi f C} = \infty$$

$\therefore$ Capacitors act as open circuits

Applying thevenin's equivalent circuit at the base terminal:

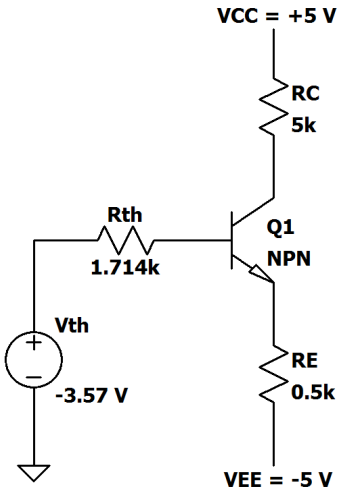

Figure 17: Thevenin's Equivalent Circuit

$$R_{TH} = R_1||R_2 = \frac{24k\Omega}{14k\Omega} = \mathbf{1.714k\Omega}$$

$$V_{TH} = \frac{R_2(V_{CC} - V_{EE})}{R_1 + R_2} + V_{EE} = \frac{2k\Omega(5+5)}{14k\Omega} - 5V = -3.5714V$$

Applying KVL to the base-emitter loop:

$$V_{TH} - I_B R_B - V_{BE} - I_E R_E = V_{EE}$$

$$I_E = I_B + I_C = I_B + \beta I_B = (\beta + 1) I_B$$

$$V_{TH} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E - V_{EE} = 0$$

$$I_B = \frac{V_{TH} - V_{BE} - V_{EE}}{R_B + (\beta + 1) R_E} \quad \text{.....(1)}$$

$$I_B = \frac{-3.571 - 0.7 + 5}{1.7142k\Omega + (101 \times 500\Omega)} = 13.96\mu A$$

$$\boldsymbol{I_B = 13.96\mu A}$$

$$I_C = \beta I_B = 100 \times 13.96\mu A = 1.396mA$$

$$\boldsymbol{I_C = 1.396mA}$$

Applying KVL to the collector-emitter loop:

$$V_{CE} = V_{CC} - I_C \times (R_C + R_E) - I_B R_E - V_{EE} \quad \text{.....(2)}$$

$$= 5 + 5 - 1.396mA \times (5k\Omega + 0.5k\Omega) - (0.5k\Omega \times 13.96mA)$$

$$\boldsymbol{V_{CE} = 2.313V}$$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

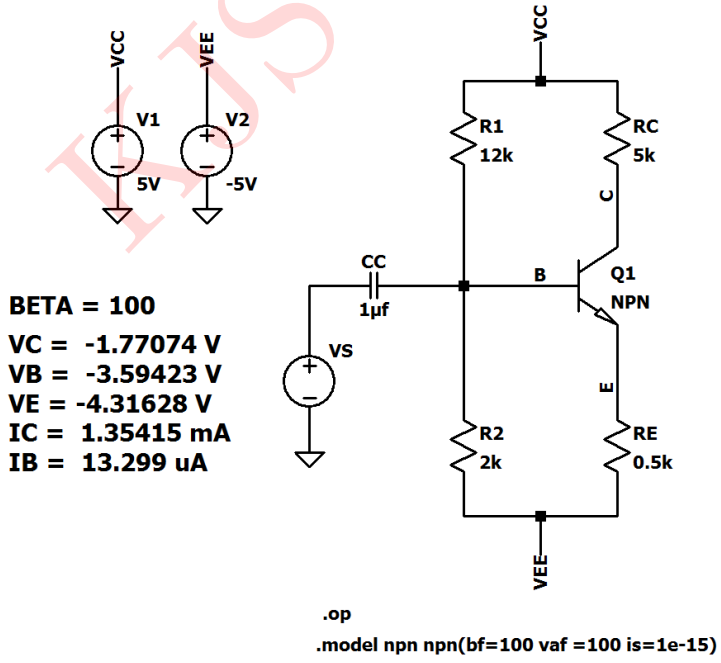

Figure 18: Circuit Schematic 8: Results

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_B	$13.96\mu A$	$13.23\mu A$
I_C	$1.396mA$	$1.354mA$
V_{CE}	$2.31V$	$2.54V$

Table 7: Question 8

Numerical 9:
Determine a) I_B, I_C, I_E, V_{CE}, for $\beta = 50$, b) repeat part a) if $R_E = 0$ for the network given in figure 19.

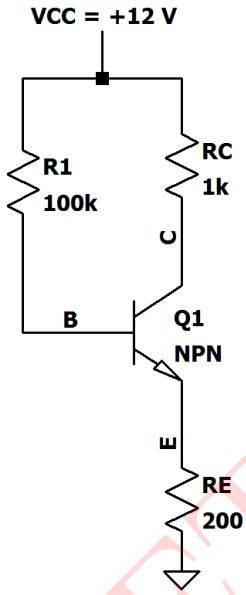

Figure 19: Circuit 9

Solution:

Above circuit 9 is a fixed emitter biased employing npn-BJT

Applying KVL to the base-emitter loop:

$V_{CC} - I_B R_1 - V_{BE} - I_E R_E = 0$

$I_E = I_B + I_C = I_B + \beta I_B = (\beta + 1) I_B$

$V_{CC} - I_B R_1 - V_{BE} - (\beta + 1) I_B R_E = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_1 + (\beta + 1) R_E} \quad \text{.....(1)}$$

$$I_B = \frac{12 - 0.7}{100k\Omega + (51 \times 200\Omega)} = 102.5\mu A$$

$\boldsymbol{I_B = 102.5\mu A}$

$I_C = \beta I_B = 50 \times 102.5\mu A = 5.125mA$

$\boldsymbol{I_C = 5.125mA}$

Applying KVL to the collector-emitter loop:

$V_{CE} = V_{CC} - R_E I_B \times (\beta + 1) - I_C R_C$ .....(2)

$= 12 - (200\Omega \times 102.5\mu A \times 51) - (1k\Omega \times 5.125mA)$

$\boldsymbol{V_{CE} = 5.8295V}$

For $R_E = 0$

Using equation (1),

$$I_B = \frac{V_{CC} - V_{BE}}{R_1 + (\beta + 1)R_E} = \frac{12 - 0.7}{100k\Omega} = 113\mu A$$

$\boldsymbol{I_B = 113\mu A}$

$I_C = \beta I_B = 50 \times 113\mu A = 5.65mA$

$\boldsymbol{I_C = 5.65mA}$

Using equation (2),

$V_{CE} = V_{CC} - R_E I_B \times (\beta + 1) - I_C R_C$

$= 12 - (5.65mA \times 1k\Omega)$

$\boldsymbol{V_{CE} = 6.35V}$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

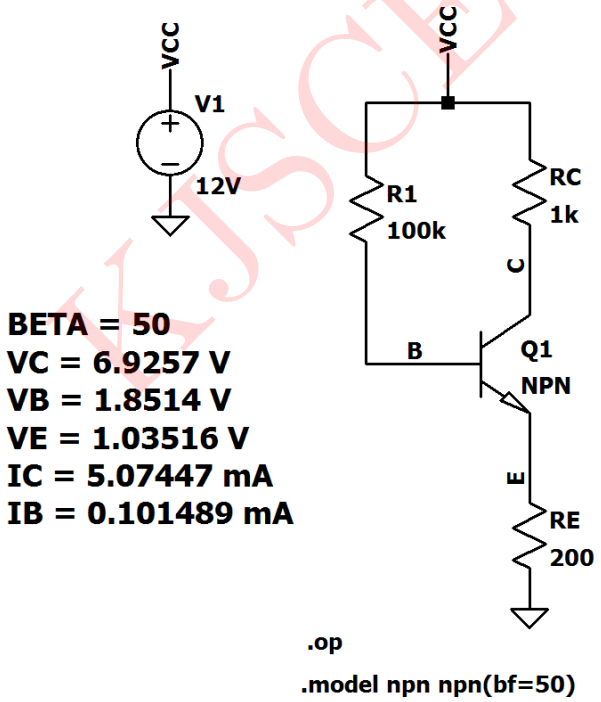

Figure 20: Circuit Schematic 9: Results

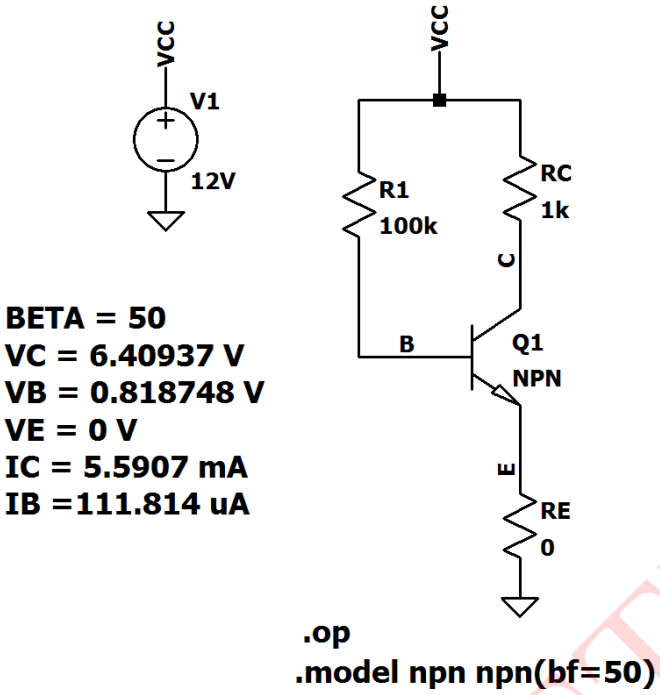

Figure 21: Circuit Schematic 9: Results when $R_E = 0$

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_B	$102\mu A$	$101\mu A$
I_C	$5.125mA$	$5.324mA$
V_{CE}	$5.8295V$	$5.602V$

Table 8: Question 9

When $R_E = 0$

Parameters	Theoretical	Simulated
I_B	$113\mu A$	$111.814\mu A$
I_C	$5.65mA$	$5.59mA$
V_{CE}	$6.35V$	$6.409V$

Table 9: Question 9

Numerical 10:
Determine a) I_B, I_C, I_E, V_{CE}, for $\beta = 50$ and $\beta = 250$, b) repeat part a) if $R_E = 0$ for the network given in figure 22.

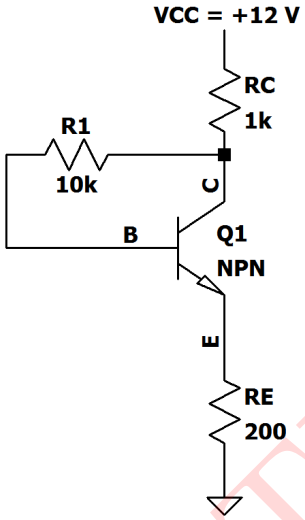

Figure 22: Circuit 10

Solution:

Above circuit 10 is a collector to base biased employing npn-BJT

Applying KVL to the base-emitter loop:

$V_{CC} - (I_B + I_C)R_C - I_B R_1 - V_{BE} - I_E R_E = 0$

$V_{CC} - I_B R_1 - V_{BE} - (I_B + I_B\beta)R_C - (\beta + 1)I_B R_E = 0$

$V_{CC} - V_{BE} = I_B[R_1 + (\beta + 1)R_C + (\beta + 1)R_E]$

$$I_B = \frac{V_{CC} - V_{BE}}{R_1 + (\beta + 1)(R_C + R_E)} \quad \text{.....(1)}$$

$$I_B = \frac{12 - 0.7}{10k\Omega + (51 \times 1.2k\Omega)} = 158\mu A$$

$\boldsymbol{I_B = 158\mu A}$

$I_C = \beta I_B = 50 \times 158\mu A = 7.9mA$

$\boldsymbol{I_C = 7.9mA}$

$I_E = I_B + I_C = 158\mu A + 7.9mA = 8.058mA$

$\boldsymbol{I_E = 8.058mA}$

Applying KVL to the collector-emitter loop:

$V_{CE} = V_{CC} - R_E I_B \times (\beta + 1) - (I_B + I_C)R_C$ .....(2)

$= 12 - 51(200\Omega \times 158\mu A) - (8.058mA \times 1k\Omega)$

$\boldsymbol{V_{CE} = 2.3304V}$

For $\beta = 250$

Using equation (1),

$$I_B = \frac{V_{CC} - V_{BE}}{R_1 + (\beta + 1)(R_C + R_E)}$$

$$I_B = \frac{12 - 0.7}{10k\Omega + (251 \times 1.2k\Omega)} = 36.31\mu A$$

$\boldsymbol{I_B = 36.31\mu A}$

$I_C = \beta I_B = 250 \times 36.31\mu A = 9.077mA$

$\boldsymbol{I_C = 9.077mA}$

$I_E = I_B + I_C = 36.31\mu A + 9.077mA = 9.113mA$

$\boldsymbol{I_E = 9.113mA}$

Using equation (2),

$V_{CE} = V_{CC} - R_E I_B \times (\beta + 1) - (I_B + I_C)R_C$

$= 12 - 251(200\Omega \times 36.31\mu A) - (9.113mA \times 1k\Omega)$

$\boldsymbol{V_{CE} = 1.065V}$

For $R_E = 0$ & $\beta = 50$

Using equation (1),

$$I_B = \frac{V_{CC} - V_{BE}}{R_1 + (\beta + 1)(R_C + R_E)}$$

$$I_B = \frac{12 - 0.7}{10k\Omega + (51 \times 1k\Omega)} = 185\mu A$$

$\boldsymbol{I_B = 185\mu A}$

$I_C = \beta I_B = 50 \times 185\mu A = 9.25mA$

$\boldsymbol{I_C = 9.25mA}$

Using equation (2),

$V_{CE} = V_{CC} - R_E I_B \times (\beta + 1) - (I_B + I_C)R_C$

$= 12 - (9.435mA \times 1k\Omega)$

$\boldsymbol{V_{CE} = 2.565V}$

For $R_E = 0$ & $\beta = 250$

Using equation (1),

$$I_B = \frac{V_{CC} - V_{BE}}{R_1 + (\beta + 1)(R_C + R_E)}$$

$$I_B = \frac{12 - 0.7}{10k\Omega + (251 \times 1k\Omega)} = 43.29\mu A$$

$$\boldsymbol{I_B = 43.29\mu A}$$

$$I_C = \beta I_B = 250 \times 43.29\mu A = 10.822mA$$

$$\boldsymbol{I_C = 10.822mA}$$

Using equation (2),

$$V_{CE} = V_{CC} - R_E I_B \times (\beta + 1) - (I_B + I_C)R_C$$
$$= 12 - ((10.822mA + 43.29\mu A) \times 1k\Omega))$$

$$\boldsymbol{V_{CE} = 1.134V}$$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

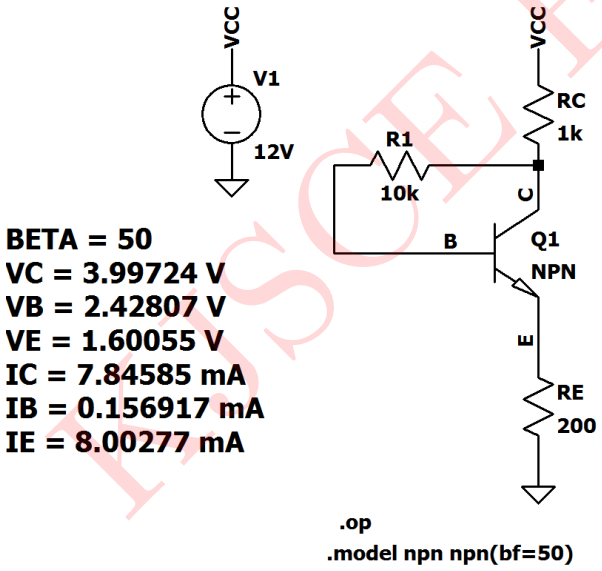

Figure 23: Circuit Schematic 10: Results when $\beta = 50$

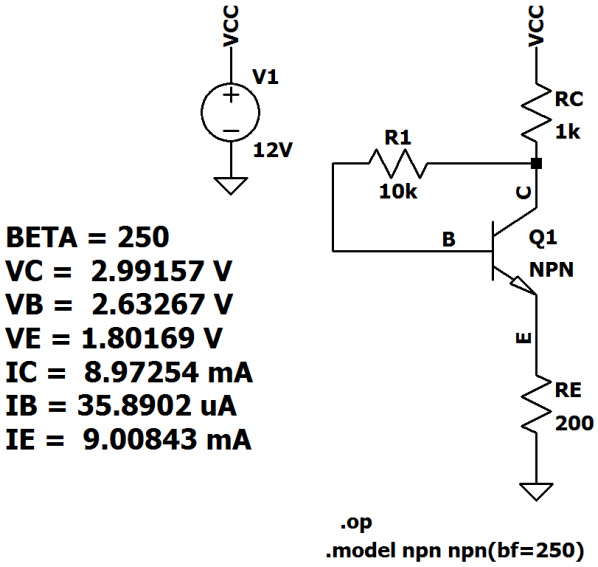

Figure 24: Circuit Schematic 10: Results when $\beta = 250$

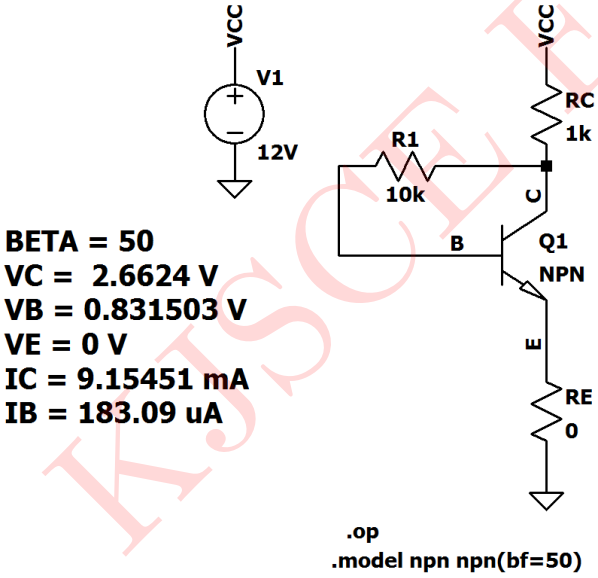

Figure 25: Circuit Schematic 10: Results when $\beta = 50$ & $R_E = 0$

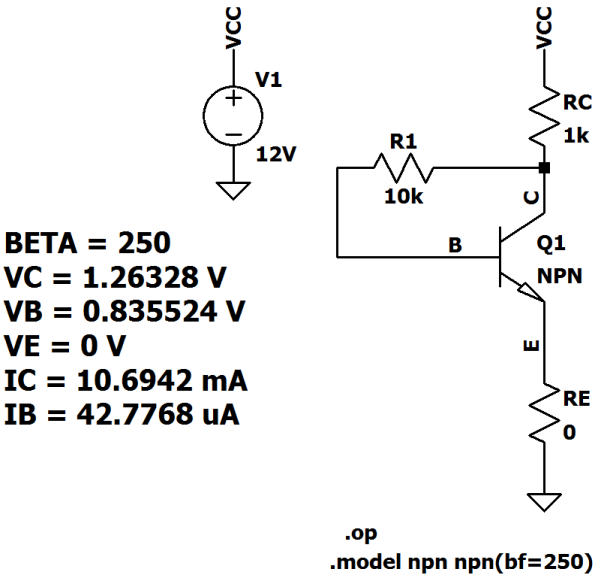

Figure 26: Circuit Schematic 10: Results when $\beta = 250$ & $R_E = 0$

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_B	$158\mu A$	$156\mu A$
I_C	$7.9mA$	$7.84mA$
V_{CE}	$2.3304V$	$2.396V$

Table 10: Question 10

When $\beta = 250$

Parameters	Theoretical	Simulated
I_B	$36.31\mu A$	$35.89\mu A$
I_C	$9.077mA$	$8.97mA$
V_{CE}	$1.065V$	$1.18V$

Table 11: Question 10

When $\beta = 50$ & $R_E = 0$

Parameters	Theoretical	Simulated
I_B	$185\mu A$	$183.09\mu A$
I_C	$9.25mA$	$9.15mA$
V_{CE}	$2.565V$	$2.66V$

Table 12: Question 10

When $\beta = 250$ & $R_E = 0$

Parameters	Theoretical	Simulated
I_B	$43.29\mu A$	$42.77\mu A$
I_C	$10.822mA$	$10.69mA$
V_{CE}	$1.134V$	$1.263V$

Table 13: Question 10

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