K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Single Stage FET Amplifier

Numerical 1:
For the circuit shown in figure 1, Determine I_{D_Q}, V_{GS_Q}, V_{DS} and A_V, if R_S is unbypassed. Given: $I_{DSS} = 12mA$, $V_P = -3V$

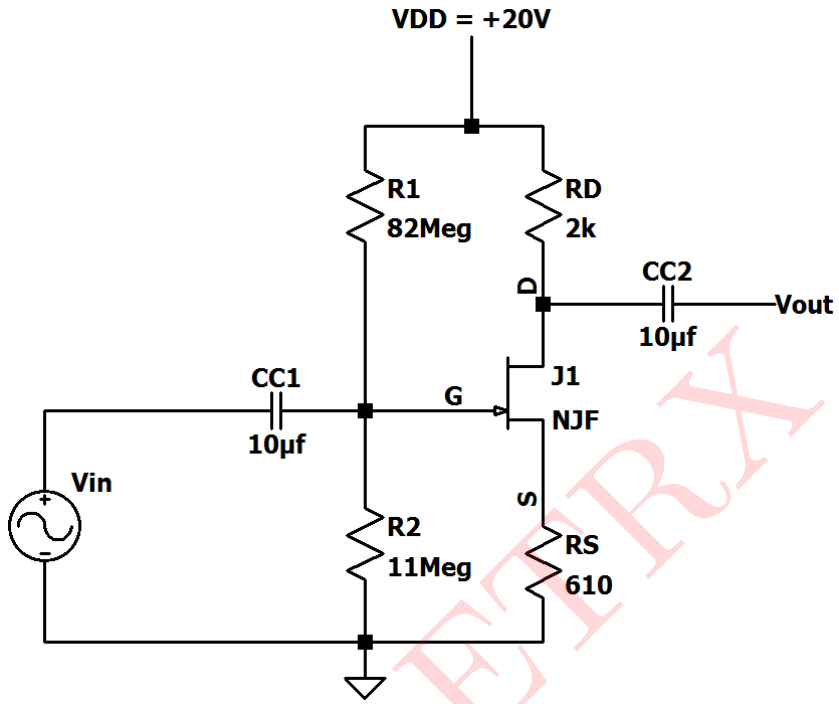

Figure 1: Circuit 1

Solution:

DC Analysis:-

$$V_G = V_{th} = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{11M\Omega}{11M\Omega + 82M\Omega} \times 20 = 2.36V$$

$$\boldsymbol{V_{th} = 2.36V}$$

$$R_{th} = R1||R2 = \frac{11M\Omega \times 82M\Omega}{93M\Omega} = 9.698M\Omega$$

$$\boldsymbol{R_{th} = 9.698M\Omega}$$

Applying KVL to the Gate-Source loop:-

$$V_{th} - V_{GS} - I_D R_S = 0$$

$$V_{GS} = 2.36 - I_D(610\Omega) \quad \text{.....(1)}$$

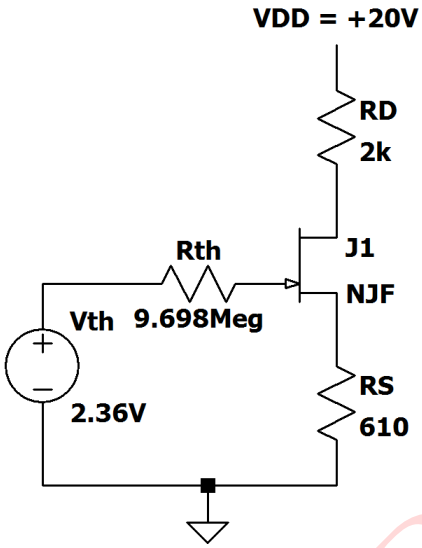

Figure 2: DC Equivalent circuit

For JFET, we assume it in saturation region

$$I_D = I_{DSS} \times \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 12 \times 10^{-3} \times \left(1 + \frac{V_{GS}}{3}\right)^2 \qquad \text{.....(2)}$$

Put (2) in (1), we get

$$V_{GS} = 2.36 - \left(12mA\left(1 + \frac{V_{GS}}{3}\right)^2 \times 610\right)$$

$$V_{GS} = 2.36 - 7.32 \times \left(1 + \frac{{V_{GS}}^2}{9} + \frac{2V_{GS}}{3}\right)$$

$$V_{GS} = 2.36 - 7.32 - 0.813{V_{GS}}^2 - 4.88V_{GS}$$

$$0.813{V_{GS}}^2 + 5.88V_{GS} + 4.96 = 0$$

Solving the above quadratic equation we get,

$V_{GS} = -0.975V$

or

$V_{GS} = -6.257V$, We reject this value, as $(V_{GS} > V_P)$

$\therefore \boldsymbol{V_{GS} = -0.975V}$

$$I_D = \frac{2.36 - V_{GS}}{610\Omega} = 5.47mA \qquad \text{[Using equation 1]}$$

$\boldsymbol{I_D = 5.47mA}$

Applying KVL to the drain-source loop,

$V_{DS} = V_{DD} - I_D \times (R_D + R_S)$

$= 20 - 5.47 \times 10^{-3}(2000 + 610) = 5.723$

$\boldsymbol{V_{DS} = 5.723}$

Small-Signal parameters:-

$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) = \frac{2 \times 12mA}{3}\left(1 - \frac{0.975}{3}\right) = 5.4\frac{mA}{V}$

$\boldsymbol{g_m = 5.4\frac{mA}{V}}$

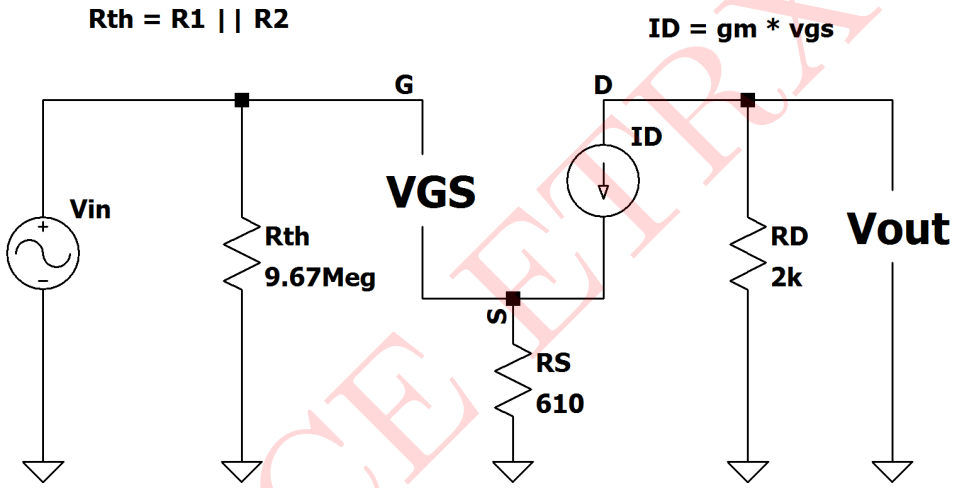

Figure 3: Small Signal Equivalent Circuit

Applying KCL at the collector terminal:-

$g_m V_{GS} + \frac{V_{out}}{R_D} = 0$

$V_{GS} = -\frac{V_{out}}{g_m R_D}$ .....(3)

Applying KVL to the Gate-Source loop:-

$V_{in} = V_{GS} + \left(\frac{V_{out}}{R_D}\right) R_S = 0$

$V_{in} = -\frac{V_{out}}{g_m R_D} - \frac{V_{out}}{R_D} R_S$

$V_{in} = -\frac{V_{out}}{R_D}\left(\frac{1}{g_m} + R_S\right)$

$A_V = \frac{V_{out}}{V_{in}} = -\frac{-R_D}{\frac{1}{g_m} + R_S} = \frac{-2k\Omega}{\frac{10^3}{5.4} + 610} = -2.515$

$\boldsymbol{A_V = -2.515}$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

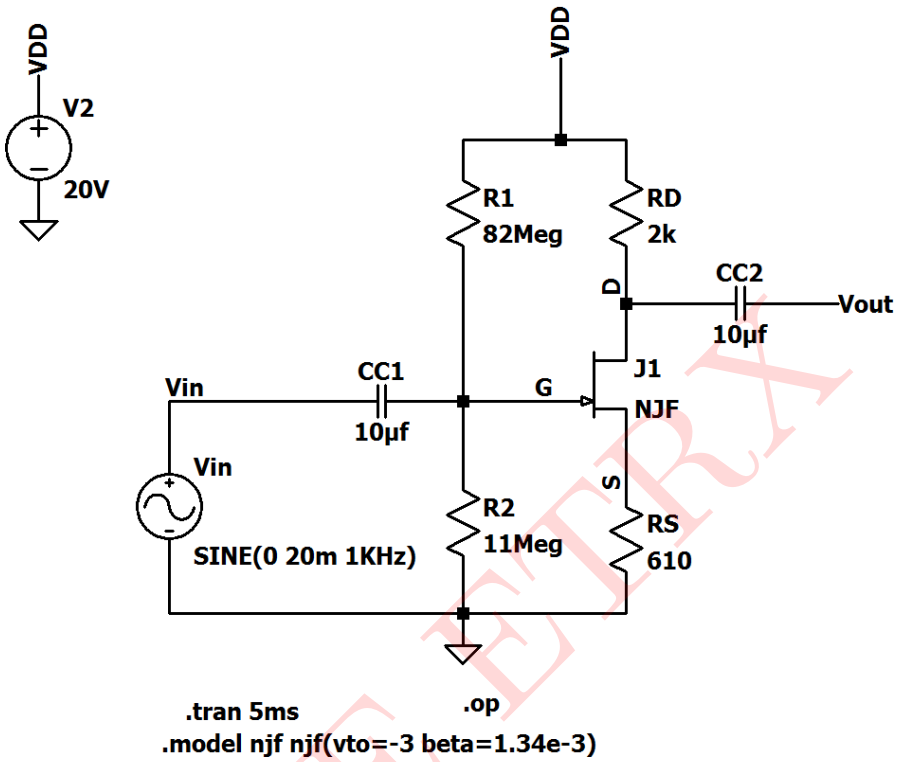

Figure 4: Circuit Schematic 1

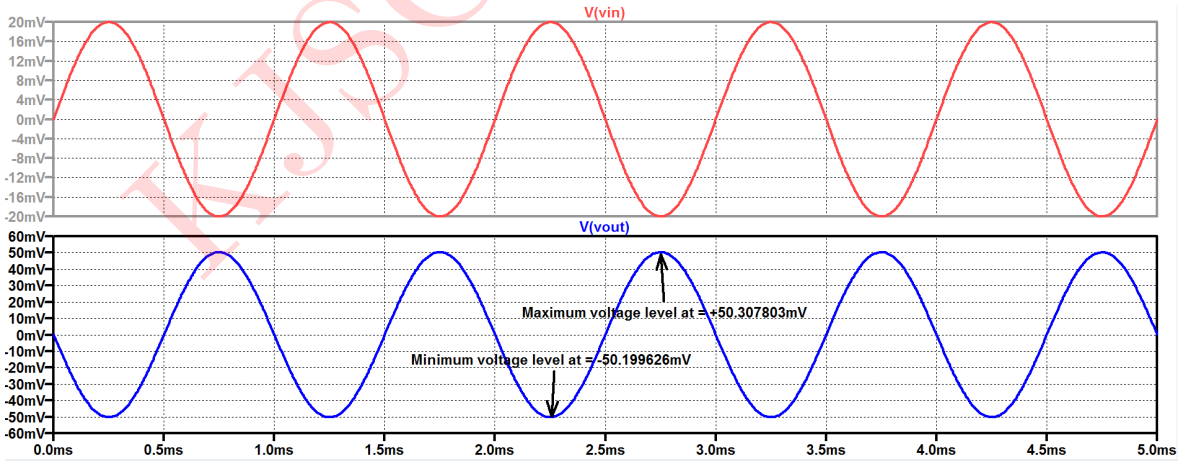

Figure 5: Input & Output waveform

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_D	$5.47mA$	$5.48mA$
V_{GS}	$-0.975V$	$-0.977V$
V_{DS}	$5.72V$	$5.69V$
A_V	-2.515	-2.512

Table 1: Numerical 1

Numerical 2:
For the circuit shown in figure 6, $R_L = 10k\Omega$, $V_m = -150V$, $V_t = 2.4V$, $k_n = 2.042\frac{mA}{V^2}$. Calculate a) Input Resistance R_{in} b) No load voltage gain A_{V_o} c) Output resistance R_o d) Overall voltage gain A_V

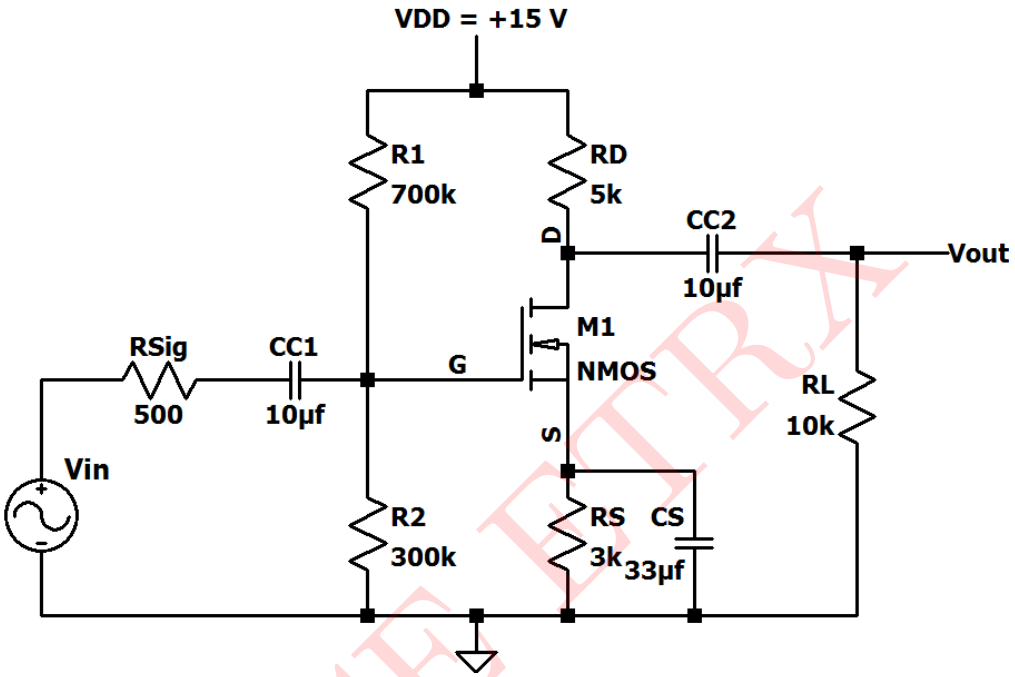

Figure 6: Circuit 2

Solution:

Above circuit 2 is a voltage divider bias employing NMOS:-

DC Analysis:-

$$V_G = V_{th} = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{300k\Omega}{700k\Omega + 300k\Omega} \times 15 = 4.5V$$

$\boldsymbol{V_{th} = 4.5V}$

$$R_{th} = R1||R2 = \frac{700k\Omega \times 300k\Omega}{1000k\Omega} = 210k\Omega$$

$\boldsymbol{R_{th} = 210k\Omega}$

Applying KVL to the Gate-Source loop:-

$V_{th} - V_{GS} - I_G R_G - I_D R_S = 0$

For MOSFET, $I_G = 0$

$V_{GS} = V_G - I_D R_S$

$V_{GS} = 4.5 - I_D(3k\Omega)$ .....(1)

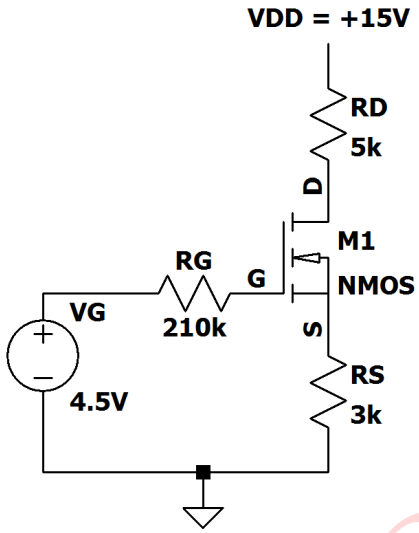

Figure 7: DC Equivalent circuit

For NMOS, we assume it in saturation region

$I_D = k_n(V_{GS} - V_t)^2 \times (1 + \lambda V_{DS})$

$\lambda = \frac{1}{|V_m|} = \frac{1}{150} = 6.67 \times 10^{-3}$

$I_D = 2.042\frac{mA}{V^2}(V_{GS} - 2.4)^2 \times \left(1 + \frac{1}{150} \times V_{DS}\right)$ .....(2)

Applying KVL to the drain-source loop,

$V_{DS} = V_{DD} - I_D \times (R_D + R_S)$

$V_{DS} = 15 - I_D \times (8000\Omega)$ .....(3)

$I_D = \frac{4.5 - V_{GS}}{3000}$ [from equation 1] .....(4)

Put (4) in (3), we get

$V_{DS} = 15 - \frac{4.5 - V_{GS}}{3000} \times 8000$

$V_{DS} = 15 - (12 - 2.67V_{GS})$

$V_{DS} = 3 + 2.67V_{GS}$ .....(5)

Put (5) and (4) in (2)

$\frac{4.5 - V_{GS}}{3000} = 2.042\frac{mA}{V^2}(V_{GS} - 2.4)^2 \times \left(1 + \frac{1}{150}(3 + 2.67V_{GS})\right)$

$\frac{4.5 - V_{GS}}{3000} = 2.042\frac{mA}{V^2}({V_{GS}}^2 + 5.67 - 4.8V_{GS}) \times (1 + 0.02 + 0.0178V_{GS})$

$4.5 - V_{GS} = 6.126({V_{GS}}^2 + 5.76 - 4.8V_{GS})(1.02 + 0.0178V_{GS})$

$V_{GS} = 6.25{V_{GS}}^2 + 36 - 30V_{GS} + 0.11{V_{GS}}^3 + 0.634V_{GS} - 0.53{V_{GS}}^2$

$0.11V_{GS}^3 + 5.72{V_{GS}}^2 - 28.37V_{GS} + 31.5 = 0$

Solving the above cubic equation we get,

$V_{GS} = -56.64V$, We reject this value, as $(V_{GS} > V_t)$

or

$V_{GS} = 2.818V$

$\therefore \boldsymbol{V_{GS} = 2.818V}$

Using equation 4

$$I_D = \frac{4.5 - 2.898}{3000\Omega} = 0.534mA$$

$\boldsymbol{I_D = 0.534mA}$

$V_{DS} = 3 + 2.67V_{GS} = 10.737V$

$\boldsymbol{V_{DS} = 10.737V}$

Small-Signal parameters:-

$$g_m = \frac{dI_D}{dV_{DS}} = \frac{d}{dV_{GS}}(k_n(V_{GS} - V_t)^2(1 + \lambda V_{DS}))$$

$$g_m = 2k_n(V_{GS} - V_t)(1 + \lambda V_{DS}) = 2 \times 2.042\frac{mA}{V^2}\left(2.898 - 2.4\left(1 + \frac{10.732}{150}\right)\right) = 2.17\frac{mA}{V}$$

$\boldsymbol{g_m = 2.17\frac{mA}{V}}$

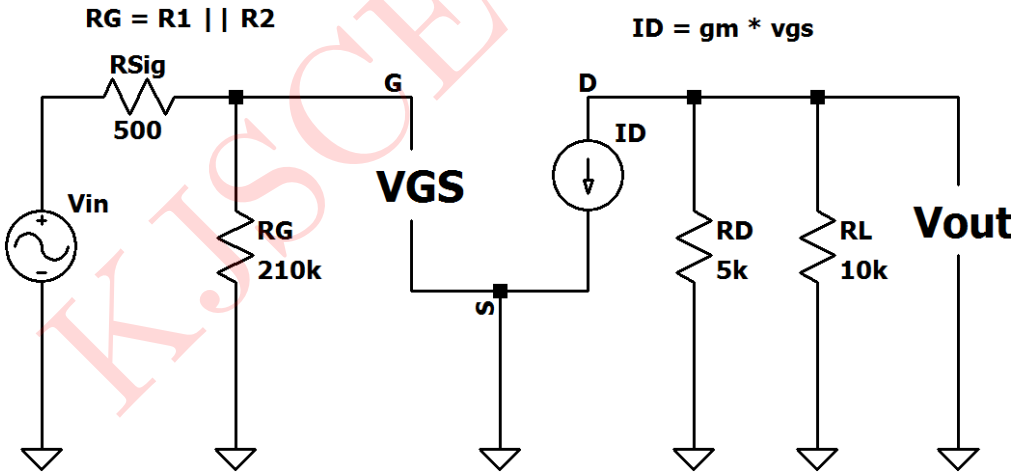

Figure 8: Small Signal Equivalent Circuit

Applying KCL at the drain terminal:-

$$g_m V_{GS} + \frac{V_{out}}{R_D} + \frac{V_{out}}{R_L} = 0$$

$$g_m V_{in} = -V_{out}\left(\frac{1}{R_D} + \frac{1}{R_L}\right)$$

$$\frac{V_{out}}{V_{in}} = -g_m(R_D||R_L)$$

$$A_V = -g_m(R_D||R_L)$$

$$A_V = -2.17\frac{mA}{V}\left(\frac{5k\Omega \times 10k\Omega}{15k\Omega}\right) = -7.23$$

$$\boldsymbol{A_V = -7.23}$$

$$A_{V_S} = \frac{V_{out}}{V_S} = \frac{V_{out}}{V_{in}} \times \frac{V_{in}}{V_S} = A_V \times \frac{V_{in}}{V_S}$$

$$\frac{V_{in}}{V_S} = \frac{R_1||R_2}{(R_1||R_2) + R_{sig}} = \frac{210k\Omega}{210k\Omega + 500\Omega} = 0.9976$$

$$A_{V_S} = 0.9976 \times -7.23 = -7.21$$

$$\boldsymbol{A_{V_S} = -7.21}$$

Without Load Resistance(R_L):-

$$A_V = -g_m R_D = -2.17 \times 5k\Omega = 10.85$$

$$A_{V_S} = 0.9976 \times -10.85 = -10.82$$

$$\boldsymbol{A_{V_S} = -10.82}$$

Input Impedance:-

$$R_i = R_{sig} + (R_1||R_2) = 500 + 210k\Omega = 210.5k\Omega$$

$$\boldsymbol{R_i = 210.5k\Omega}$$

Output Impedance:-

$$R_o = R_D||R_L = 5k\Omega||10k\Omega = 3.34k\Omega$$

$$\boldsymbol{R_o = 3.34k\Omega}$$

Without Load Resistance(R_L):-

$$R_o = R_D = 5k\Omega$$

$$\boldsymbol{R_o = 5k\Omega}$$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

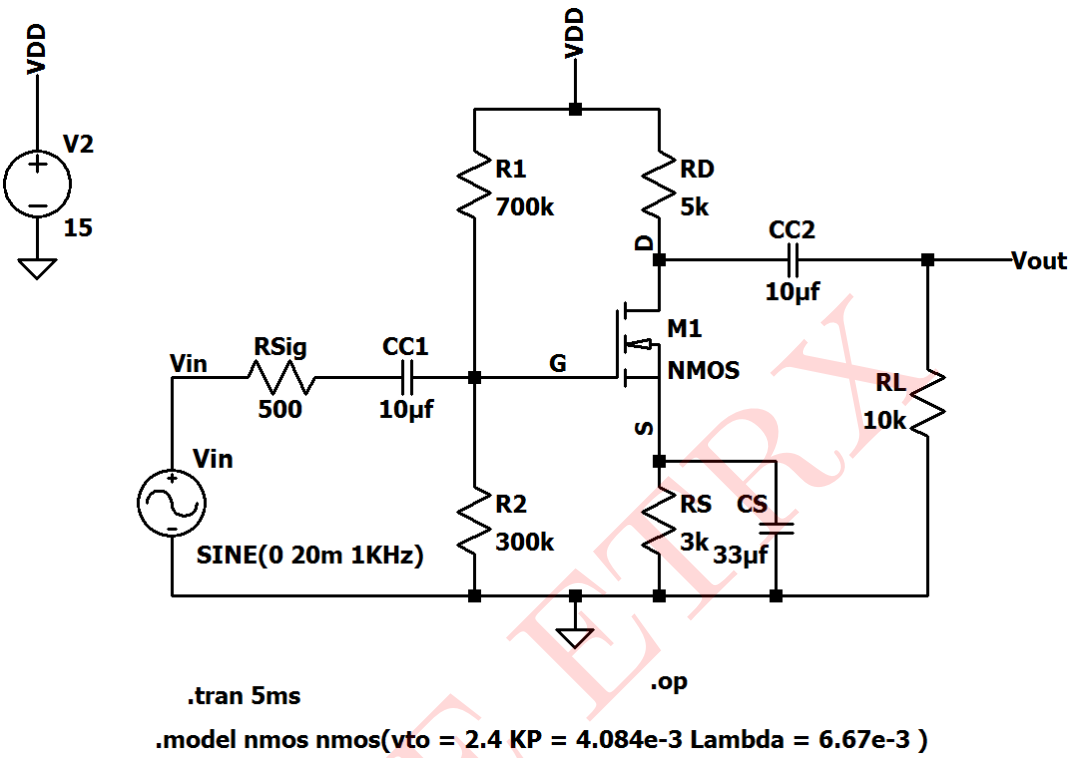

Figure 9: Circuit Schematic 2

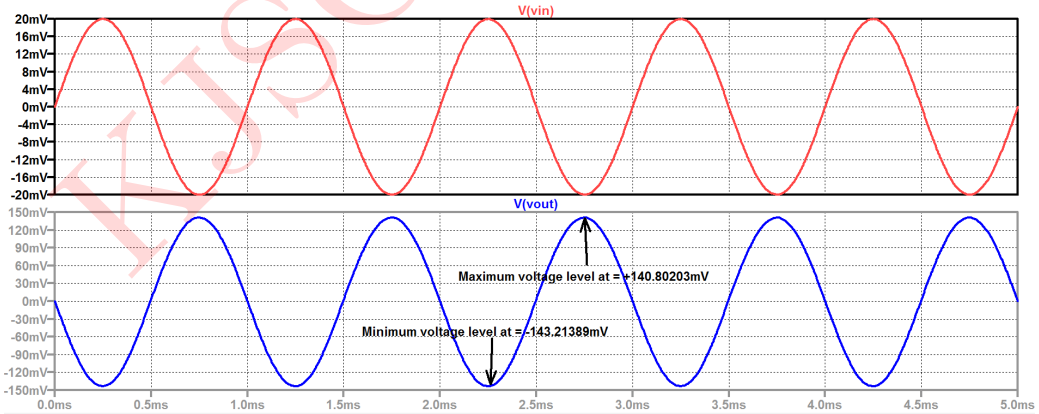

Figure 10: Input & Output waveform

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_D	$0.534mA$	$0.535mA$
V_{GS}	$2.898V$	$2.894V$
A_V	-7.21	-7.10

Table 2: Numerical 2

****