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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Cascade Amplifier Design

9^{th} **July, 2020**

Design 1:
Design two stage RC coupled cascade amplifier to meet the following specifications: $A_V \geq 170$, $V_{o(rms)} = 2.5V$, $R_i \geq 1M\Omega$. Select suitable transistor from datasheet.

Solution:
Step 1: For the above given requirement, we can use CS-CS self-bias JFET amplifier.

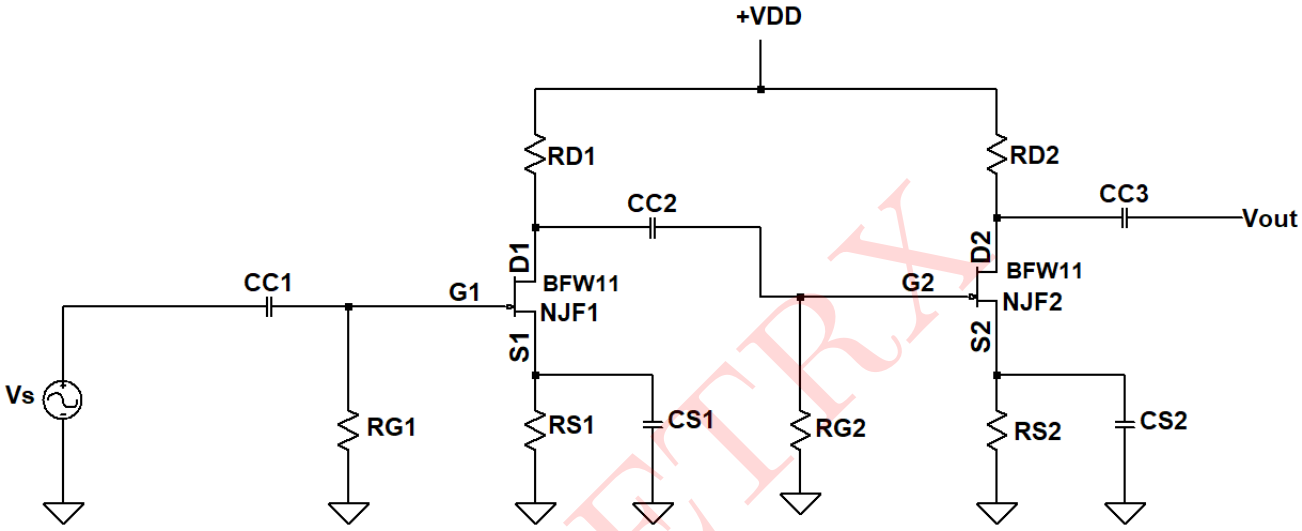

Figure 1: Circuit diagram

JFET BFW11 parameters: (from datasheet)
$I_{DSS} = 7mA$ $V_P = -2.5V$
$r_d = 50k\Omega$ $g_{mo} = 5600\mu\mho$

Step 2: Selection of voltage gain: $A_V \geq 170$ ...(given)
Let $A_V = 190$
Also, let $A_{V1} = 0.6A_{V2}$

$\therefore A_V = A_{V1} \times A_{V2}$

$\therefore 190 = 0.6A_{V2}^2 \implies A_{V2} = 17.7951$

$\therefore A_{V2} \approx 18$

$\therefore A_{V1} = 10.6771 \implies A_{V1} \approx 11$

Step 3: Design of second stage:
Calculation of Q-point: (V_{GSQ2}, I_{DQ2})

Since I_{DQ} is not given, using mid-point biasing we can find I_{DQ} and V_{GSQ}

$$\therefore I_{DQ} = \frac{I_{DSS}}{2} = \frac{7mA}{2} = 3.5mA$$

In saturation, $I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$\therefore V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$

$V_{GS} = (-2.5)\left[1 - \sqrt{\frac{3.5mA}{7mA}}\right]$

$\therefore V_{GS} = -0.7302V$

Step 4: Calculation of R_{D2} :

$| A_{V2} | = g_m(r_{d2} \parallel R_{D2})$ ...(1)

$g_{m1} = g_{m2} = g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right]$

$\therefore g_m = 5600 \times 10^{-6}\left[1 - \frac{0.732}{2.5}\right]$

$\therefore g_m = 3.9603mA/V$

Also, $r_{d1} = r_{d2} = r_d = 50k\Omega$

From (1), $18 = 3.9603 \times 10^{-3}[50k\Omega \parallel R_{D2}]$

$\frac{18}{3.9603 \times 10^{-3}} = \frac{R_{D2} \times 50k\Omega}{50k\Omega + R_{D2}}$

$\therefore R_{D2} = 4.9995k\Omega$

Choosing higher standard values, $R_{D2} = 2.1k\Omega, 1/4W$

Step 5: Calculation of R_{S2}:

$V_{GSQ} = -I_{DQ}R_{S2}$

$\therefore R_{S2} = \frac{-V_{GSQ}}{I_{DQ}} = \frac{0.732}{3.5mA}$

$\therefore R_{S2} = 0.2091k\Omega$

Choosing higher standard value, $R_{S2} = 180\Omega, 1/4W$

Step 6: Selection of R_{G2}:
To prevent loading for first stage, let $R_{G2} = 1M\Omega, 1/4W$

Step 7: Calculation for V_{DD}:

Applying KVL to JFET 2, D-S loop:
$V_{DD} - I_{DQ2}R_{D2} - V_{DSQ2} - I_{DQ2}R_{S2} = 0$

$\therefore V_{DD} = I_{DQ2}(R_{D2} + R_{S2}) + V_{DSQ2}$

$V_{DSQ2} \geq 1.5\,[\,|\,V_P\,| + V_{opeak}]$

The value is multiplied by 1.5 to take care of the saturation voltages, variations in resistance, variation in supply voltage and device parameter variation.
$V_{DSQ2} \geq 1.5\,[\,|\,V_P\,| + V_{opeak}]$

$V_{DSQ2} \geq 1.5\,\left[2.5 + \sqrt{2}(2.5)\right]$

$\therefore V_{DSQ2} \geq 9.0533$

$\therefore V_{DSQ} = 9.1V$

$\therefore V_{DD} = (3.5 \times 10^{-3})(0.18k\Omega + 5.1k\Omega) + 9.1$

$\therefore V_{DD} = 27.58V$
selecting $V_{DD} = 30V$

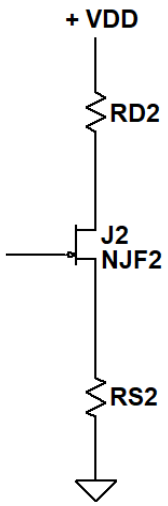

Figure 2: D-S loop of JFET 2

Design of first stage:

Step 8: Selection of R_{D1} :

$| A_{V2} | = g_m(r_d \parallel R_{D2}) = 3.6603(50k\Omega \parallel 5.1k\Omega)$

$\therefore | A_{V2} | = 18.3281$

$i.e. | A_{V1} | = \dfrac{A_V}{| A_{V2} |} = \dfrac{190}{18.3281} = 10.3666$

Let $A_{V1} = 11$

$\therefore | A_{V1} | = g_{m1}(r_{d1} \parallel R_{D1} \parallel R_{G2})$

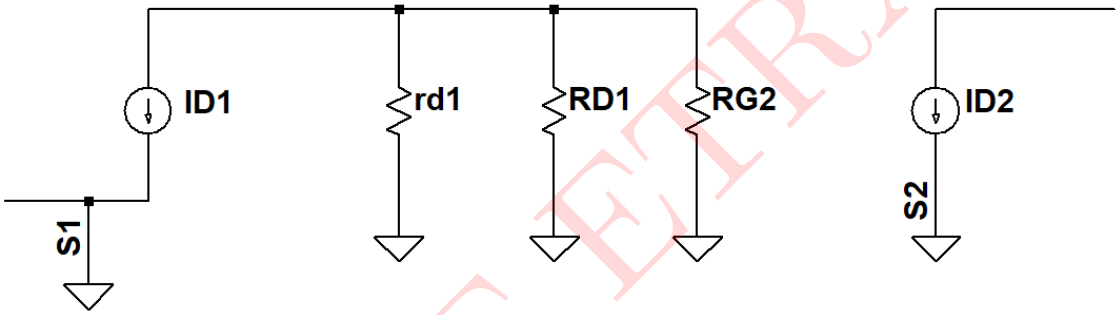

Figure 3: Small signal equivalent circuit for stage 1

$\therefore 11 = 3.9603(50k\Omega \parallel R_{D1} \parallel 1M\Omega)$

$\therefore 11 = 3.9603(47.62k\Omega \parallel R_{D1})$

$\therefore \dfrac{11}{3.9603} = \dfrac{R_{D1}(47.62k\Omega)}{R_{D1} + 47.62k\Omega}$

$\therefore R_{D1} = 2.9496k\Omega$

Choosing higher standard value, $\therefore R_{D1} = 3.3k\Omega, 1/4W$

Step 9: Selection of R_{S1} : $V_{GSQ1} = -I_{DQ1}R_{S1}$

$\therefore R_{S1} = \dfrac{-V_{GSQ1}}{I_{DQ1}} = \dfrac{0.7320}{3.5mA}$

$\therefore R_{S1} = 0.2091k\Omega = 209.1\Omega$

Choosing lower standard value, $R_{S1} = 180\Omega, 1/4W$

Step 10: Selection of R_{G1}:
To avoid loading effect and fulfill the requirement of $R_i \geq 1M\Omega$
Select $R_{G1} = 1.2M\Omega, 1/4W$

Step 11: Selection of coupling capacitors:
C_{C1}, C_{C2}, C_{C3}: Since f_L is not given, we choose audio frequency $f_L = 20Hz$

For C_{C1}:

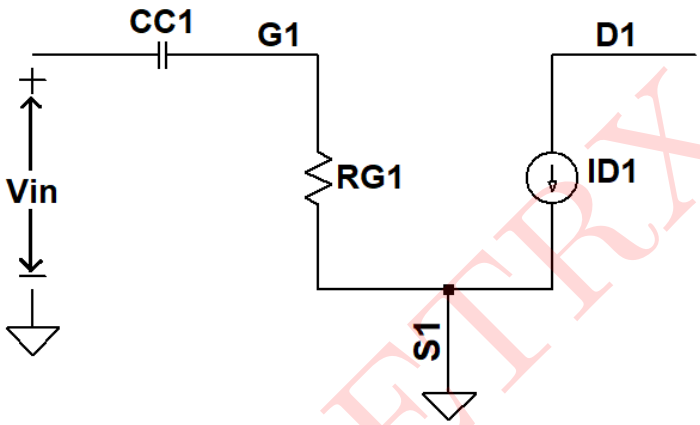

Figure 4: For calculating C_{C1}

$$\therefore C_{C1} = \frac{1}{2\pi R_{eq} f_L} \quad \text{...(here } R_{eq} = R_{G1})$$

$$\therefore C_{C1} = \frac{1}{2\pi R_{G1} f_L} = \frac{1}{2\pi(1.2M)(20)}$$

$$\therefore C_{C1} = 6.63nF$$

Choosing higher standard value, $\therefore C_{C1} = 6.8nF/60V$

Here, voltage rating should be greater than twice of V_{DD}

For C_{C2} :

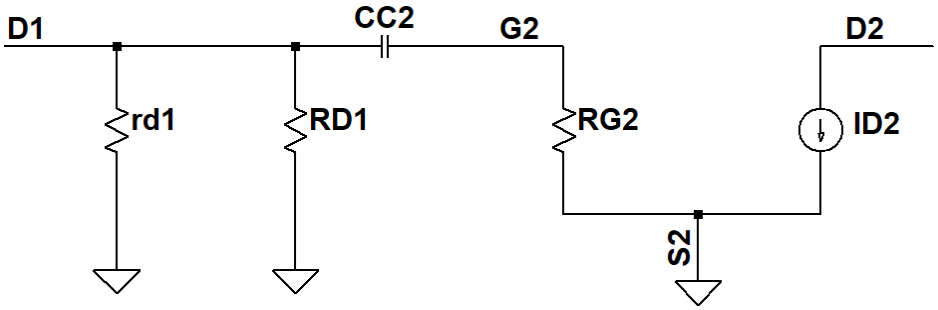

Figure 5: For calculating C_{C2}

$$\therefore C_{C2} = \frac{1}{2\pi R_{eq} f_L}$$

here, $R_{eq} = r_{d1} \parallel R_{D1} + R_{G2}$

$\therefore R_{eq} = 50k\Omega \parallel 3.3k\Omega + 1M\Omega$

$\therefore R_{eq} = 1.0031M\Omega$

$$\therefore C_{C2} = \frac{1}{2\pi(1.00031M\Omega)(20)}$$

$\therefore C_{C2} = 7.933nF$

Choosing higher standard value, $C_{C2} = 8.2nF/60V$

For C_{C3} :

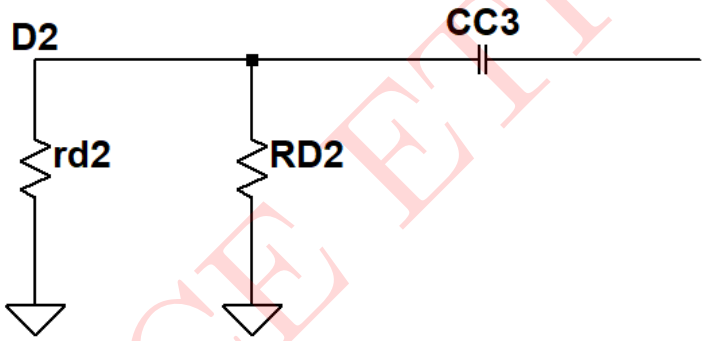

Figure 6: For calculating C_{C3}

$R_{eq} = r_{d2} \parallel R_{D2}$

$$\therefore C_{C3} = \frac{1}{2\pi R_{eq} f_L}$$

$R_{eq} = 50k\Omega \parallel 5.1k\Omega$

$\therefore R_{eq} = 4.6279k\Omega$

$$\therefore C_{C3} = \frac{1}{2\pi(4.6279k\Omega)(20)} = 1.7195\mu F$$

Choosing higher standard value, $C_{C3} = 1.8\mu F, 60V$

Step 12: Selection of bypass capacitor:

Since $g_{m1} = g_{m2} = g_m = 3.6603mA/V$ and $R_{S1} = R_{S2} = 180\Omega$

$$\therefore C_{S1} = C_{S2} = \frac{1}{2\pi R_{eq} f_L}$$

here, $R_{eq} = 1/g_m \parallel R_S$

$\therefore R_{eq} = 252.51 \parallel 180 = 0.1051k\Omega$

$$\therefore C_{S1} = C_{S2} = \frac{1}{2\pi(0.1051k\Omega)(20)}$$

$$\therefore C_{S1} = C_{S2} = 75.7250\mu F$$

Choosing higher standard value, $C_{S1} = C_{S2} = 100\mu F$

Step 13: Completed Designed circuit:

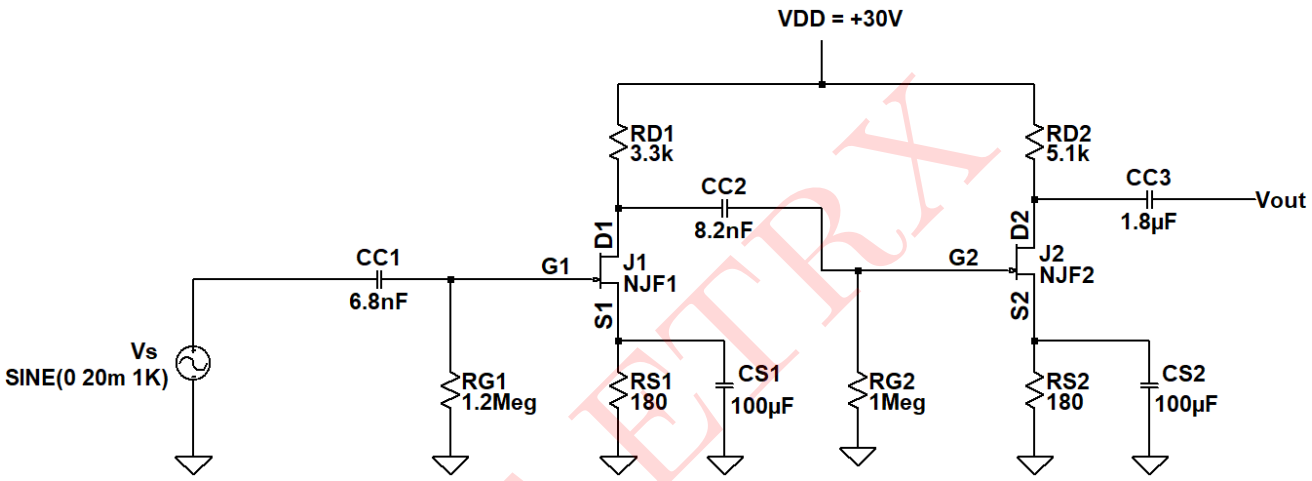

Figure 7: Completed Designed circuit

Small signal equivalent circuit is shown in figure 8:

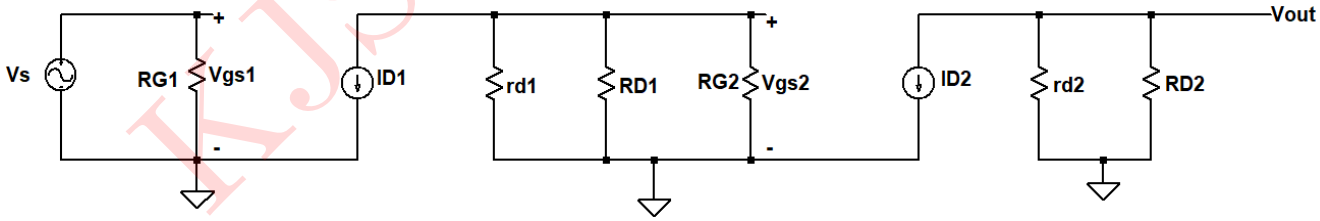

Figure 8: Small signal equivalent circuit

Input impedance: $Z_i = R_{G1} = 1.2M\Omega$

Output impedance: $Z_o = r_{d2} \parallel R_{D2}$

$\therefore Z_o = 50k\Omega \parallel 5.1k\Omega = 4.6279k\Omega$

For Stage 1, $A_{V1} = V_1/V_s$ here, $V_s = V_{gs}$

$\therefore V_1 = -g_m V_{gs}(r_{d1} \parallel R_{D1} \parallel R_G)$

$\therefore A_{V1} = -g_m(r_{d1} \parallel R_{D1} \parallel R_G)$

$\therefore A_{V1} = (-3.9603 \times 10^{-3})(50k\Omega \parallel 3.3k\Omega \parallel 1.2M\Omega)$

$\therefore A_{V1} = (-3.9603 \times 10^{-3})(3.0877k\Omega) = -12.22$

$\therefore \mid A_{V1} \mid = 12.2200$

For stage 2, $A_{V2} = V_{out}/V_1$

$\therefore V_{out} = -g_m V_{gs}(r_{d2} \parallel R_{D2})$

here, $V_1 = V_{gs}$

$\therefore A_{V2} = -g_m(r_{d2} \parallel R_{D2})$

$\therefore A_{V2} = -(3.9603 \times 10^{-3})(4.6279k\Omega)$

$\therefore A_{V2} = -18.3281$

$\therefore \mid A_{V2} \mid = 18.3281$

Overall gain: $A_{Vt} = A_{V1} \times A_{V2} = 223.9694$

$\therefore A_{Vt} = 47dB$

SIMULATED RESULTS:

Above circuit was simulated in LTspice and results obtained are as follows:

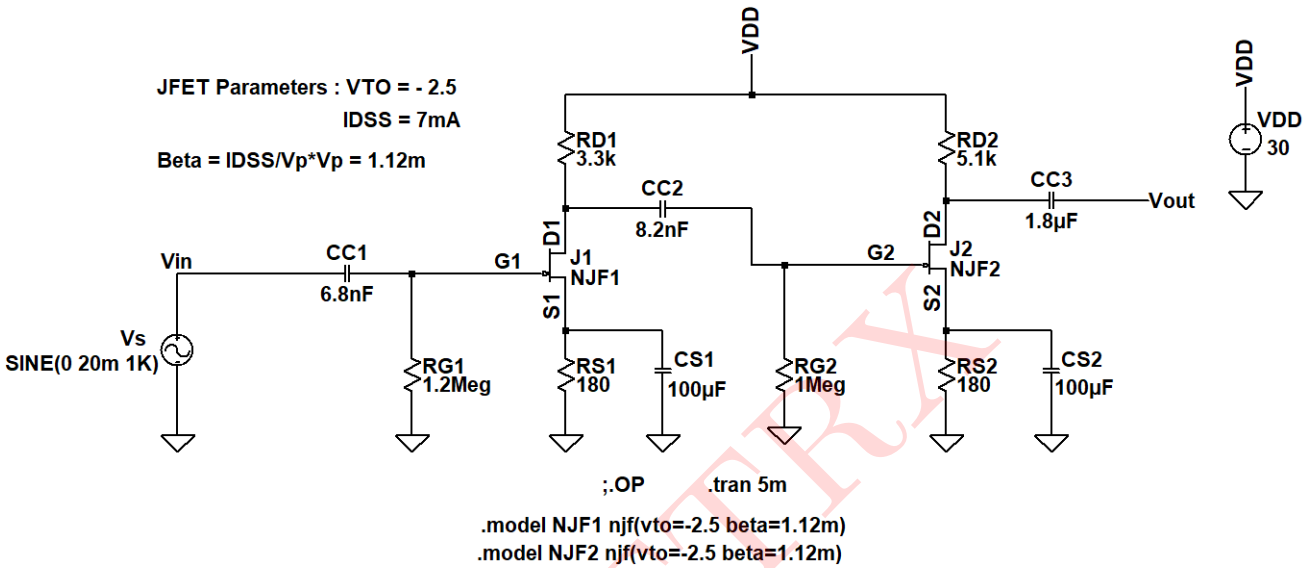

Figure 9: Circuit Schematic: Results

Input and output waveforms for each stage are shown below:

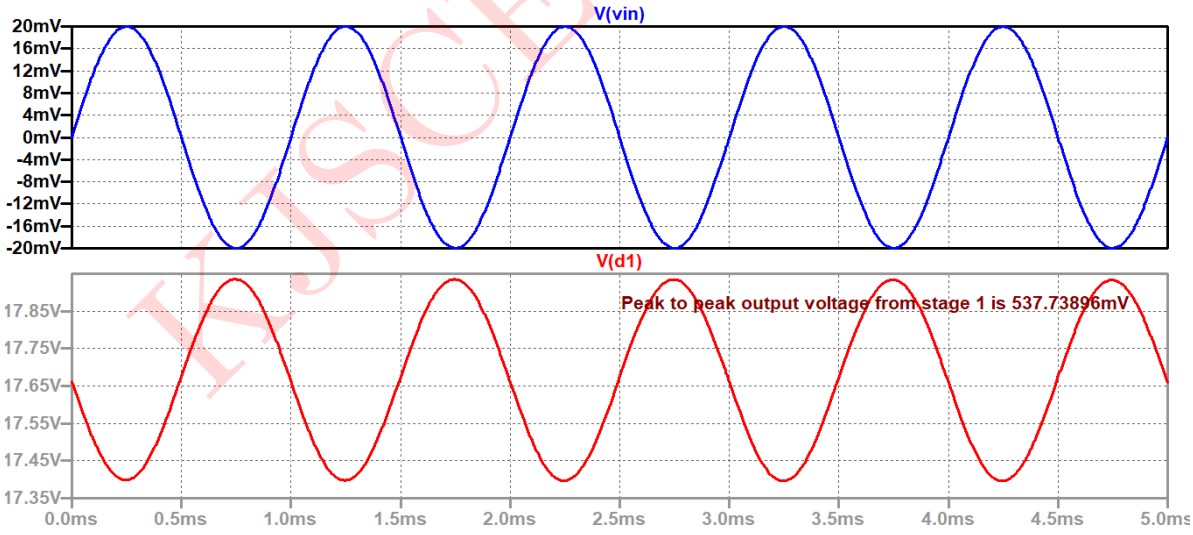

Figure 10: Input and output waveform for Stage 1

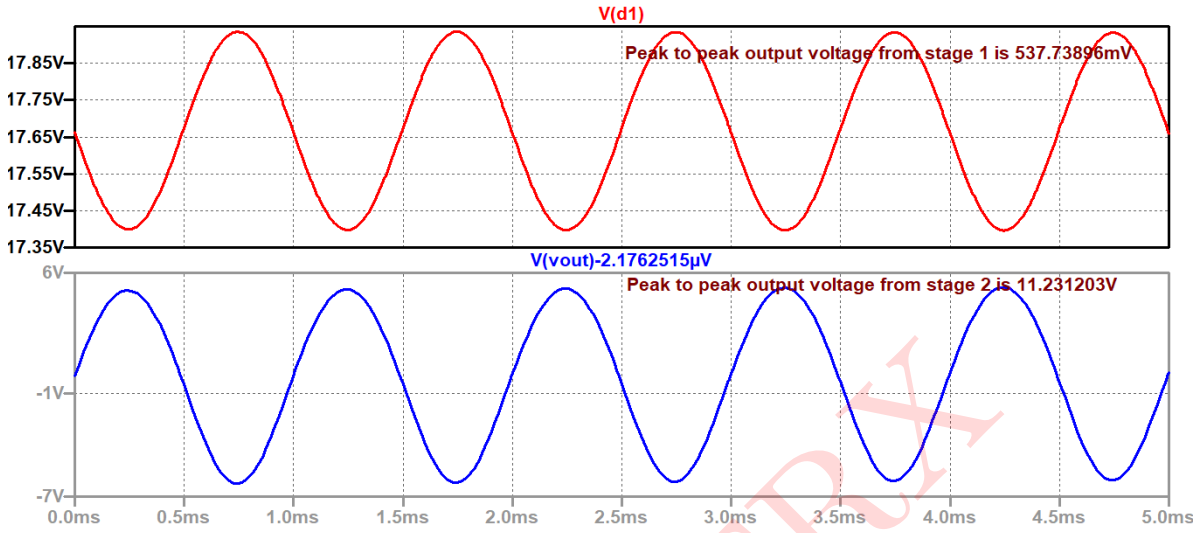

Figure 11: Input and output waveform for Stage 2

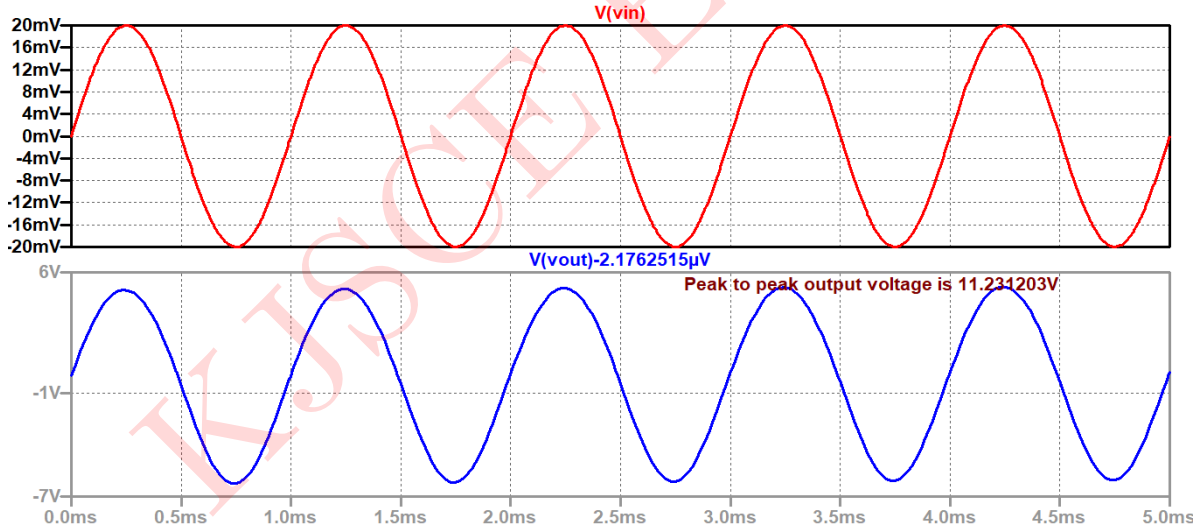

Figure 12: Input and output waveform for designed circuit

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
DC parameters of Stage 1: I_{DQ1}, V_{GSQ1}	3.5mA, $-0.732V$	3.5016mA, $-0.7318V$
DC parameters of Stage 1: I_{DQ2}, V_{GSQ2}	3.5mA, $-0.732V$	3.5016mA, $-0.7318V$
Voltage gain of Stage 1 : $\mid A_{V1} \mid$	> 11	13.4435
Voltage gain of Stage 2 : $\mid A_{V2} \mid$	>18	20.8860
Overall voltage gain: A_V (in dB)	47dB	48.9673
Input impedance: Z_i	1.2MΩ	–
Output impedance: Z_o	4.6279kΩ	–

Table 1: Design 1

Design 2:
Design two stage RC coupled cascade amplifier for following specifications:
$A_V \geq 450$, $V_{CC} = 20V$, $S \leq 10$, $R_i \geq 1M\Omega$
Select a suitable transistor from datasheet.

Solution: Above requirements can be fulfilled by CS-CE stage.
Stage 1 is of JFET since $R_i \geq 1M\Omega$

Step 1: Circuit diagram and selection of transistor:

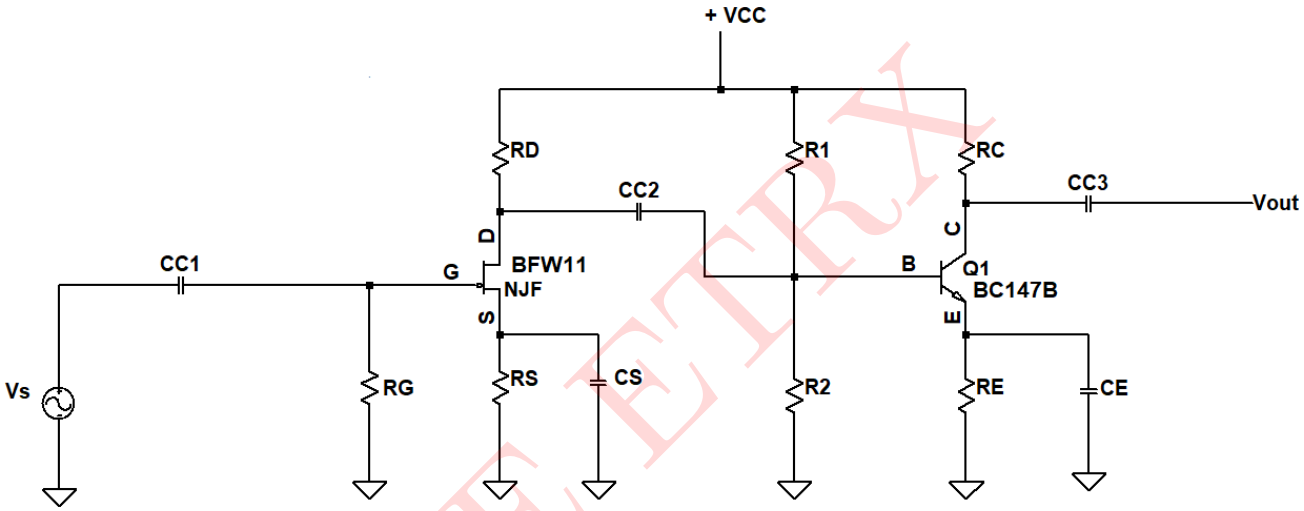

Figure 13: Circuit diagram

Select BC147B, since h_{fe} and h_{ie} are high.

BC147B Parameters: $h_{fe} = 330$ $h_{FE} = 290 = \beta$

$h_{ie} = 4.5k\Omega$ $V_{CC(sat)} = 0.25V$

BFW11 Parameters: $I_{DSS} = 7mA$, $g_{mo} = 5600\mho$, $V_P = -2.5V$, $r_d = 50k\Omega$

Step 2: Selection of gain:

$A_V \geq 450$ ...(given)

Let $A_{V1} = 4$, since JFET Amplifier gain is small.

then $A_{V2} = \dfrac{A_V}{A_{V1}}$

$\therefore A_{V2} = \dfrac{450}{4} = 120$

Design of second stage:
Step 3: Selection of R_C:

$$| A_{V2} | = \frac{h_{fe} R_C}{h_{ie}}$$

$$\therefore 120 = \frac{330 \times R_C}{4.5 \times 10^3}$$

$$\therefore R_C = 1.636k\Omega$$

Choosing higher standard value, $R_C = 1.8k\Omega, 1/4W$

Step 4: Selection of Q-point (V_{CEQ}, I_{CQ})

$V_{CC} = 20V$ ...(given)

$$V_{CE} = \frac{V_{CC}}{2} = 10V$$

$$V_E = 0.1V_{CC} = 0.1(20)$$

$$\therefore V_E = 2V$$

Applying KVL to C-E loop:

$$V_{CC} - V_{RC} - V_{CEQ} - V_E = 0$$

$$\therefore V_{RC} = V_{CC} - V_{CEQ} - V_E = 20 - 10 - 2$$

$$\therefore V_{RC} = 8V$$

Now, $V_{RC} = I_{CQ}(R_C)$

$$\therefore I_{CQ} = \frac{V_{RC}}{R_C} = \frac{8V}{1.8k\Omega}$$

$$\therefore I_{CQ} = 4.444mA$$

$$\therefore I_B = \frac{I_{CQ}}{\beta} = \frac{4.444mA}{290}$$

$$\therefore I_B = 15.3255\mu A$$

$$I_E = (1 + \beta) I_B$$

$$\therefore I_E = (290 + 1)(15.3255\mu A)$$

$$\therefore I_E = 4.4597mA$$

Step 5: Selection of R_E:

$V_E = 2V$

$\therefore V_E = I_E R_E$

$\therefore R_E = \dfrac{V_E}{I_E} = \dfrac{2}{4.4597mA}$

$R_E = 448.46\Omega$

Choosing lower standard value, this is only in case of CS-CE amplifier.

$\therefore R_E = 420\Omega, 1/4W$

Step 6: Selection of biasing resistors: (R_1 & R_2)

$S \leq 10$ ...(given)

Let $S = 9$

$$S = \frac{1+\beta}{1+\beta\left[\dfrac{R_E}{R_B+R_E}\right]}$$

here, $R_B = R_1 \parallel R_2$

$$\therefore 9 = \frac{1+290}{1+\left[290 \times \dfrac{420}{420+R_B}\right]}$$

$\therefore R_B = 3.4672k\Omega$

i.e. $\dfrac{R_1 R_2}{R_1+R_2} = 3.4672k\Omega$ ...(1)

Also, $V_{TH} = V_B = \dfrac{R_2 V_{CC}}{R_1+R_2}$

$\therefore V_B = \dfrac{R_2(20)}{R_1+R_2}$ ...(2)

Applying KVL to B-E loop:

$V_B - I_{BQ}R_B - V_{BE} - I_{EQ}R_E = 0$

$\therefore V_B = \dfrac{I_{CQ}}{\beta}R_B + V_{BE} + I_{CQ}R_E$ ...($\because I_{CQ} = \beta I_{BQ}$ & $I_{CQ} \approx I_{EQ}$)

$\therefore V_B = \dfrac{4.444mA}{290}(3.4672k\Omega) + 0.7 + (4.444mA)(0.42)$

$\therefore V_B = 2.6179V$

From (2), $2.6179 = \dfrac{R_2(20)}{R_1 + R_2}$

$\therefore \dfrac{R_2}{R_1 + R_2} = 0.13$

From (1), $(0.13)R_1 = 3.4672$

$\therefore R_1 = 26.6708k\Omega$

Choosing higher standard value, $R_1 = 27k\Omega, 1/4W$

Also, $\dfrac{R_1 R_2}{R_1 + R_2} = 3.4672$

$\therefore \dfrac{(27k\Omega)R_2}{27k\Omega + R_2} = 3.4672$

$\therefore R_2 = 3.9780k\Omega$

Choosing higher standard value, $R_2 = 4.2k\Omega, 1/4W$

Design of first stage:

Step 7: Selection of Q-point (I_{DQ}, V_{GSQ})

Using mid-point biasing technique, $I_{DQ} = \dfrac{I_{DSS}}{2} = \dfrac{7mA}{2}$ ...(from datasheet)

$\therefore I_{DQ} = 3.5mA$

For JFET in saturation, $I_D = I_{DSS}\left[1 - \dfrac{V_{GS}}{V_P}\right]^2$

On rearranging, $V_{GSQ} = V_P\left[1 - \sqrt{\dfrac{I_{DQ}}{I_{DSS}}}\right]$ = -2.5$\left[1 - \sqrt{\dfrac{3.5mA}{7mA}}\right]$

$\therefore V_{GSQ} = -0.732V$

Now, $g_{m1} = g_{mo}\left[1 - \dfrac{V_{GS}}{V_P}\right]$

$\therefore g_{m1} = (5600 \times 10^{-6})\left[1 - \dfrac{0.732}{2.5}\right]$

$\therefore g_{m1} = 3.9603mA/V$

Step 8: Selection of R_D:

$| A_{V2} | = \dfrac{h_{fe} \times R_C}{hie} = \dfrac{330 \times 1.8k\Omega}{4.5} = 132$

$\therefore | A_{V1} | = \dfrac{A_V}{| A_{V2} |} = \dfrac{450}{132} = 3.41$

Let $| A_{V1} | = 3.5$

$| A_{V1} | = g_m(r_d \parallel R_1 \parallel R_2 \parallel hie \parallel R_D)$

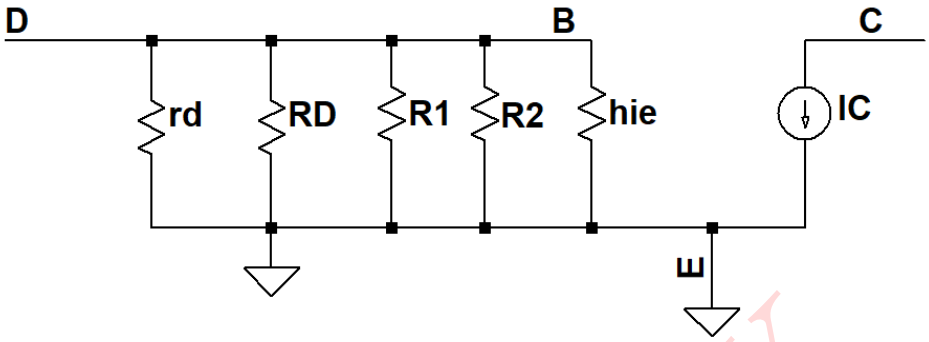

Figure 14: For selection of R_D

$\therefore 3.5 = (3.9603 \times 10^{-3})(50k\Omega \parallel 27k\Omega \parallel 4.2k\Omega \parallel 4.5k\Omega \parallel R_D)$

$\therefore 3.5 = (3.9603 \times 10^{-3})(1.9329k\Omega \parallel R_D)$

$$\therefore 0.8838 = \frac{R_D(1.9329k\Omega)}{R_D + 1.9329k\Omega}$$

$\therefore R_D = 1.6283k\Omega$

Choosing higher standard value, $R_D = 1.8k\Omega, 1/4W$

Step 9: Selection of R_S

$V_{GSQ} = -I_{DQ}(R_S)$

$$\therefore R_S = \frac{-V_{GSQ}}{I_{DQ}}$$

$$\therefore R_S = \frac{-(-0.732)}{3.5mA}$$

$\therefore R_S = 209.14\Omega$

Choosing lower standard value, $R_S = 180\Omega, 1/4W$

Step 10: Selection of R_G :

Let $R_G = 1.2M\Omega$ since $R_i \geq 1M\Omega$

$\therefore R_G = 1.2M\Omega, 1/4W$

Step 11: Selection of coupling capacitors:

For C_{C1}:

Since f_L is not given, we choose $f_L = 20Hz$ which is audio frequency.

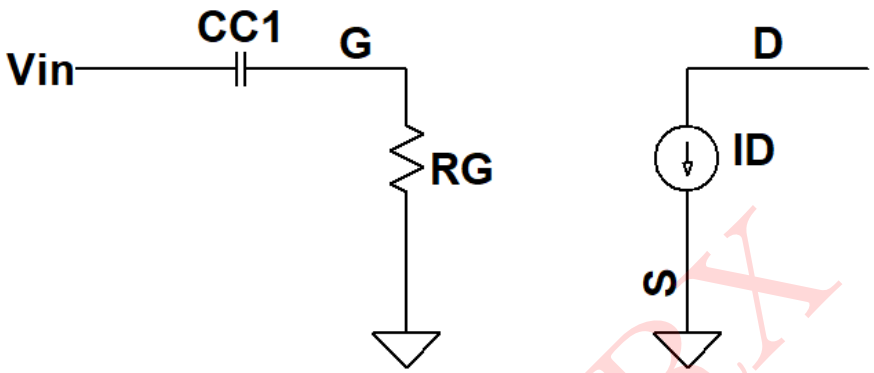

Figure 15: Low frequency equivalent circuit for C_{C1}

$$\therefore C_{C1} = \frac{1}{2\pi R_{eq} f_L}$$

here $R_{eq} = R_G$

$$\therefore R_{eq} = 1.2M\Omega$$

$$\therefore C_{C1} = \frac{1}{2\pi(1.2M\Omega)(20)} = 6.63nF$$

Choosing higher standard value, $\therefore C_{C1} = 6.8nF/50V$

For C_{C2}:

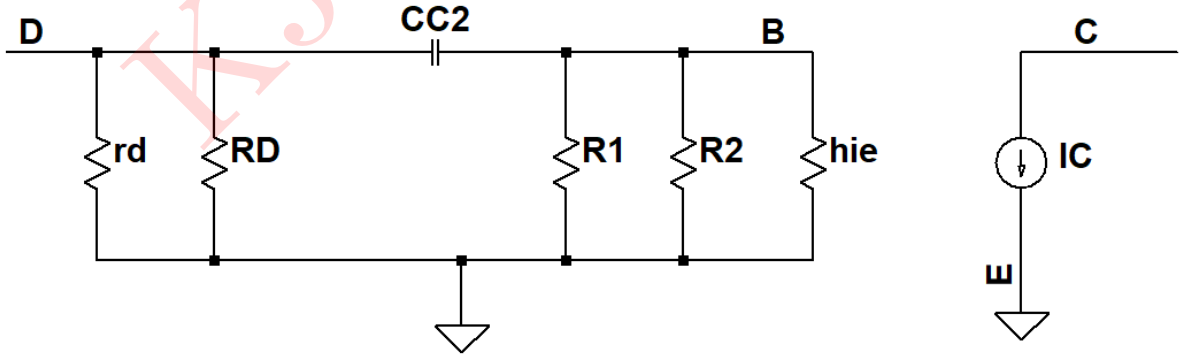

Figure 16: Low frequency equivalent circuit for C_{C2}

here, $R_{eq} = r_d \parallel R_D + R_1 \parallel R_2 \parallel h_{ie}$

$\therefore R_{eq} = 50k\Omega \parallel 1.8k\Omega + 27k\Omega \parallel 4.2k\Omega \parallel 4.5k\Omega$

$\therefore R_{eq} = 1.7375k\Omega + 2.0106k\Omega$

$\therefore R_{eq} = 3.7481k\Omega$

$\therefore C_{C2} = \dfrac{1}{2\pi R_{eq} f_L} = \dfrac{1}{2\pi(3.7481k\Omega)(20)}$

$\therefore C_{C2} = 2.1231\mu F$

Choosing higher standard value, $C_{C2} = 2.1231\mu F$

For C_{C3} :

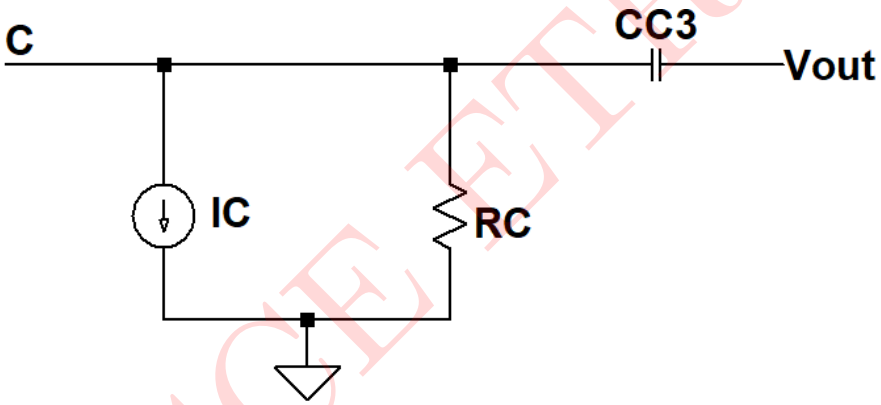

Figure 17: Low frequency equivalent circuit for C_{C3}

here, $R_{eq} = R_C = 1.8k\Omega$

$\therefore C_{C3} = \dfrac{1}{2\pi R_{eq} f_L}$

$\therefore C_{C3} = \dfrac{1}{2\pi(1.8k\Omega)(20)} = 4.42\mu F$

Choosing higher standard value, $C_{C3} = 4.7\mu F/50\text{V}$

Step 12: Selection of bypass capacitors:

a. C_S :

$C_S = \dfrac{1}{2\pi R_{eq} f_L}$

$\therefore R_{eq} = R_S \parallel 1/g_m = 180 \parallel 252.52$

$R_{eq} = 105.09\Omega$

$\therefore C_S = \dfrac{1}{2\pi(105.09)(20)} = 75.72\mu F$

Choosing higher standard value, $C_S = 82\mu F/50V$

b. C_E :

$X_{C_E} = 0.1R_E$

$$\frac{1}{2\pi f_L C_E} = 0.1R_E$$

$$\therefore C_E = \frac{1}{0.1(R_E)f_L(20)}$$

$$\therefore C_E = \frac{1}{0.1(0.42k\Omega)(20)(2\pi)}$$

$\therefore C_E = 189.47\mu F$

Choosing higher standard value, $C_E = 220\mu F/50V$

Step 13: Completed Designed circuit:

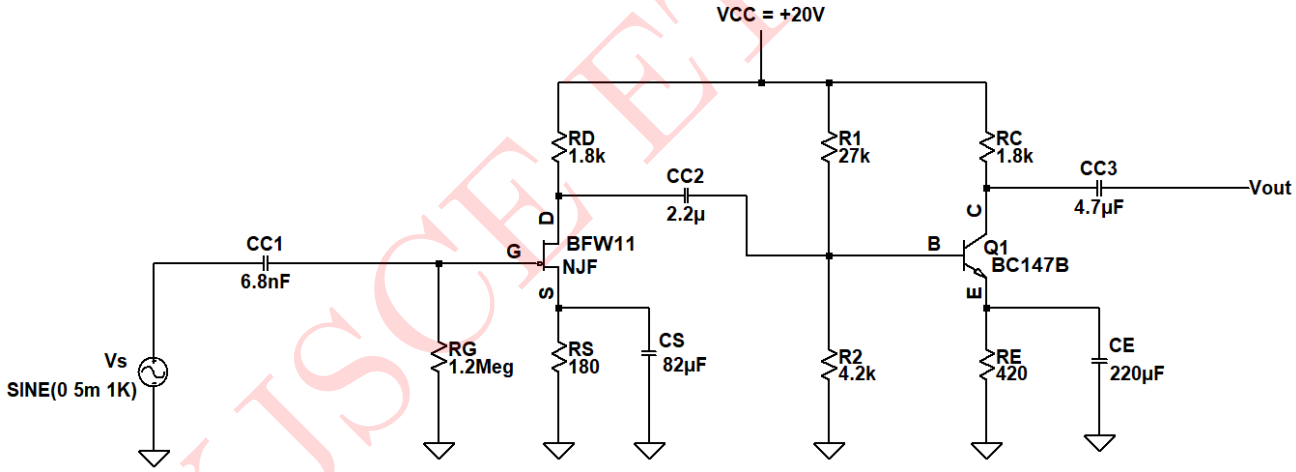

Figure 18: Completed Designed circuit

Small signal equivalent circuit is shown in figure 19:

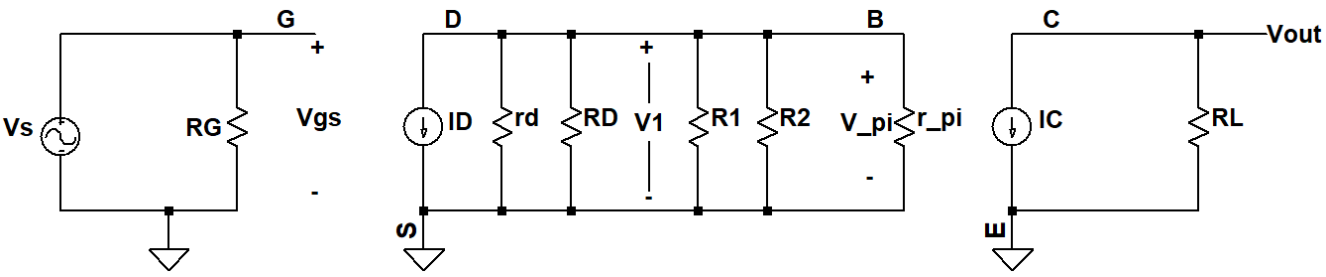

Figure 19: Small signal equivalent circuit

$$A_{V1} = \frac{V_1}{V_s} \qquad \text{...(here } V_s = V_{gs})$$

$$\therefore V_1 = -g_{m1} V_{gs} (r_d \parallel R_D \parallel R_1 \parallel R_2 \parallel r_\pi)$$

$$\therefore A_{V1} = -g_{m1} (r_d \parallel R_D \parallel R_1 \parallel R_2 \parallel r_\pi)$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{290(26mV)}{4.44mA}$$

$$\therefore r_\pi = 1.6967k\Omega$$

$$g_{m2} = \frac{I_{CQ}}{V_T} = \frac{4.44mA}{26mV}$$

$$\therefore g_{m2} = 170.7692mA/V$$

$$\therefore A_{V1} = -(3.9603 \times 10^{-3})(50k\Omega \parallel 1.8k\Omega \parallel 27k\Omega \parallel 4.2k\Omega \parallel 1.6967k\Omega)$$

$$\therefore A_{V1} = -2.7501$$

For A_{V2}:

$$A_{V2} = \frac{V_{out}}{V_1}$$

$$\therefore V_1 = V_\pi$$

Also, $V_{out} = -g_{m2} V_\pi R_C$

$$\therefore A_{V2} = -g_{m2} R_C$$

$$\therefore A_{V2} = -(170.7692 \times 10^{-3})(1.8k\Omega)$$

$$\therefore A_{V2} = -307.38V$$

Overall gain: $A_{Vt} = A_{V1} \times A_{V2}$

$$\therefore A_{Vt} = (-2.7501)(-307.38)$$

$$\therefore A_{Vt} = 845.3257$$

Input impedance:

$$Z_i = R_G = 1.2M\Omega$$

Output impedance:

$$Z_o = r_d \parallel R_D = 50k\Omega \parallel 1.8k\Omega$$

$$\therefore Z_o = 1.7375k\Omega$$

SIMULATED RESULTS:

Above circuit was simulated in LTspice and results obtained are as follows:

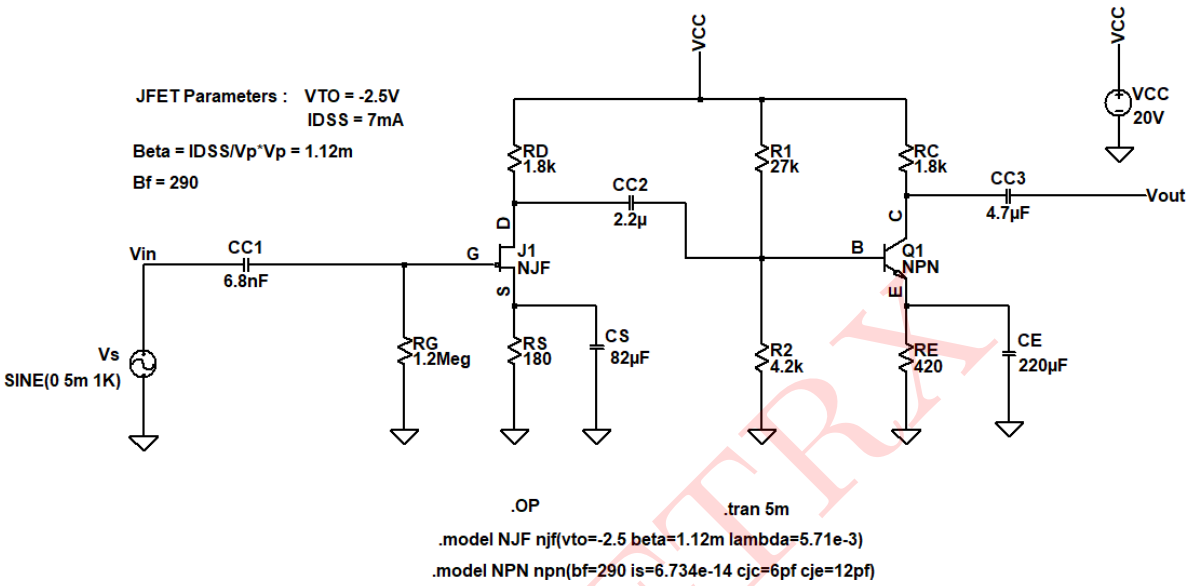

Figure 20: Circuit Schematic: Results

Input and output waveforms for each stage are shown below:

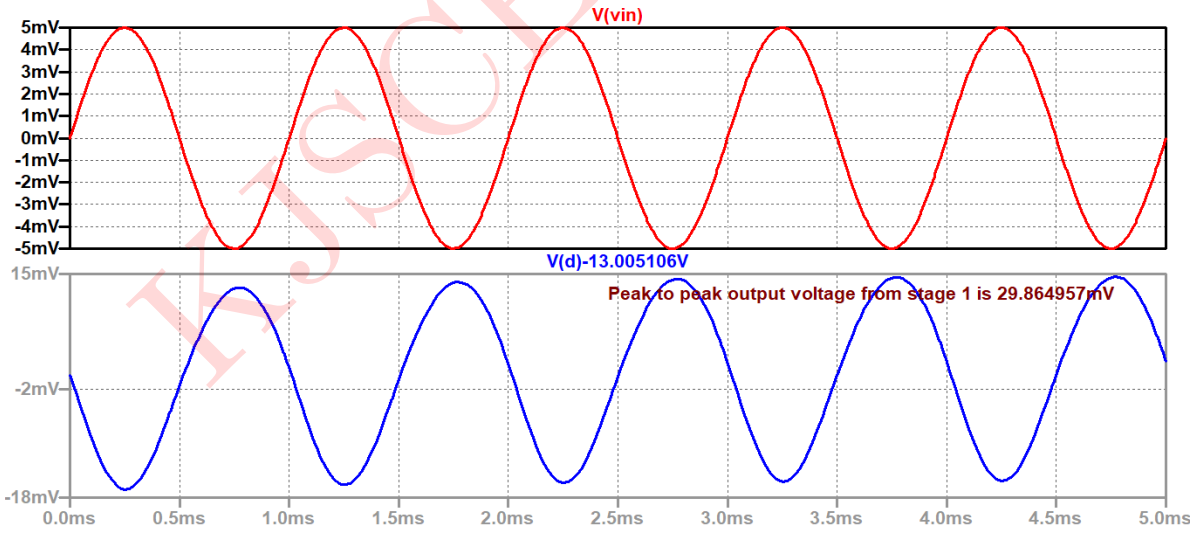

Figure 21: Input and output waveform for Stage 1

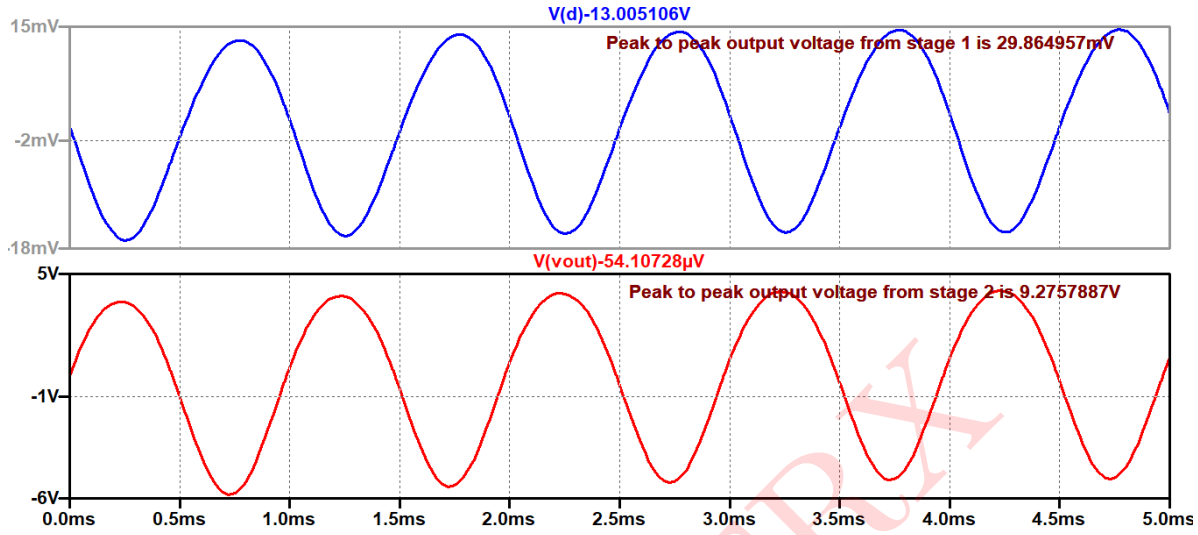

Figure 22: Input and output waveform for Stage 2

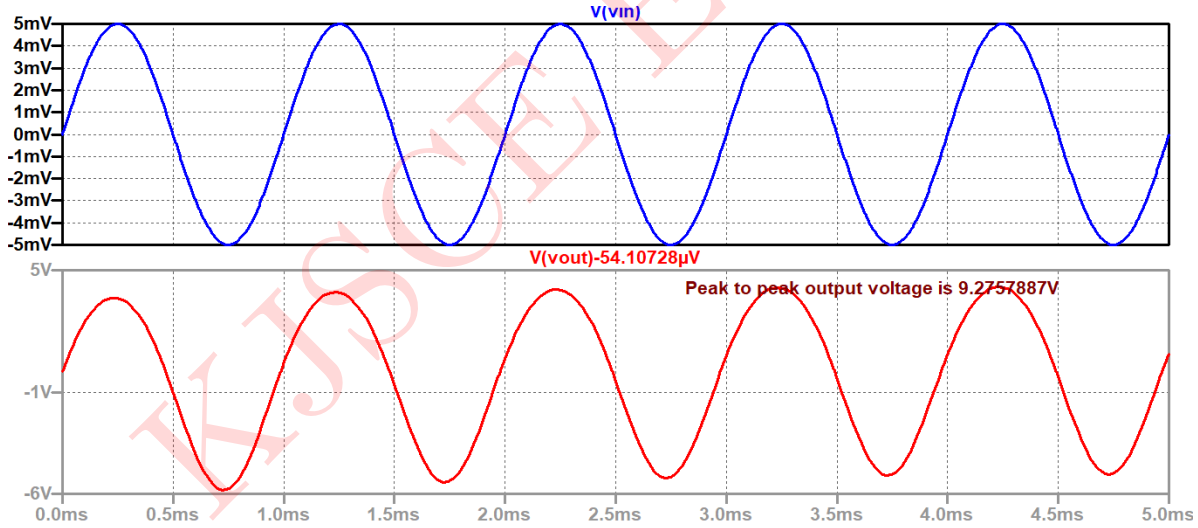

Figure 23: Input and output waveform for designed circuit

Comparsion between theoretical and simulated values:

Parameters	Theoretical value	Simulated value
Stage 1 DC parameters: I_{DQ1}, V_{GSQ1}	8.5mA, $-0.732V$	3.8861mA, $-0.7V$
Stage 2 DC parameters: I_B, I_C I_E, V_E, V_B	15.3255μA, 4.44mA 4.4597mA, 2V, 2.1697V	16.2601μA, 4.715mA 4.7317mA, 1.9837V, 2.6333V
Voltage gain of Stage 1: $\mid A_{V1} \mid$	2.7501	2.9618
Voltage gain of Stage 2: $\mid A_{V2} \mid$	307.38	313.25
Overall voltage gain: A_{Vt}	845.3257	927.8
Input impedance: Z_i	1.2MΩ	–
Output impedance: Z_o	1.7375kΩ	–

Table 2: Design 2