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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Design of Single Stage Amplifier

Design 1:
Design a single stage RC coupled JFET amplifier for the following specifications:- $V_{out} = 2V$, $f_L \leq 20Hz$ and $|A_V| \geq 10$ using mid-point biasing technique. Also calculate A_V, Z_i and Z_o of the amplifier you have designed.

Solution:

Step 1:- Data

$|A_V| = 10$, $V_{out} = 2V$, $f_L = 20Hz$

Step 2:- Selection of JFET

We select n-channel JFET BFW11 from the datasheet with the following specifications:- $g_{m_o} = 5600\frac{\mu A}{V}$, $V_P = -2.5V$, $r_d = 50k\Omega$ and $I_{DSS} = 7mA$

Step 3:- Selection of biasing circuit

Self-bias circuit is used to give mid-point biasing

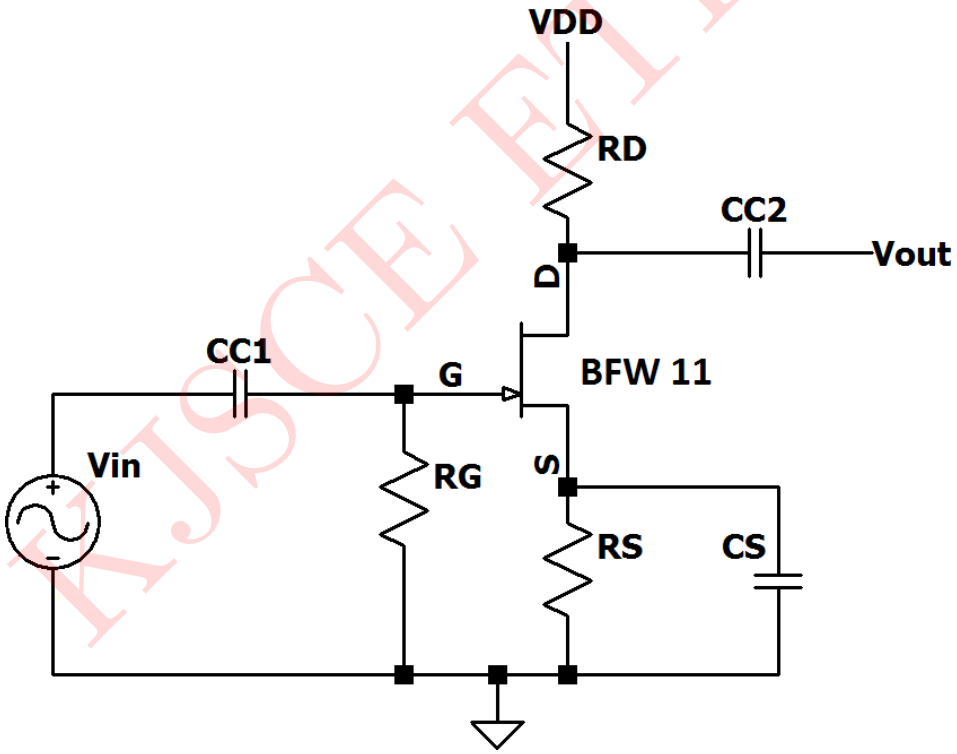

Figure 1: Circuit 1

Step 4:- Selection of Q-point

(i) For midpoint biasing, $I_D = \frac{I_{DSS}}{2}$

i.e. $I_D = \frac{7mA}{2} = 3.5mA$

(ii) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$\frac{3.5}{7} = \left(1 - \frac{V_{GS}}{V_P}\right)^2$

$0.5 = \left(1 + \frac{V_{GS}}{2.5}\right)^2$

$\sqrt{0.5} = 1 + \frac{V_{GS}}{2.5}$

$V_{GS} = (\sqrt{0.5} - 1) \times 2.5$

$\boldsymbol{V_{GS} = -0.732}$

(iii) $g_m = g_{m_o}\left(1 - \frac{V_{GS}}{V_P}\right)$

$g_m = 5600 \times 10^{-6}\left(1 - \frac{0.732}{2.5}\right) = 3.96mA/V$

$\boldsymbol{g_m = 3.96mA/V}$

Step 5:- Selection of R_S

$V_{GS} = I_D R_S$ [Self Bias]

$R_S = \frac{-V_{GS}}{I_D} = \frac{0.732}{3.5mA} = 209\Omega$

Select $\boldsymbol{R_S = 220\Omega, 1/4W}$

Step 6:- Selection of R_D

$A_V = -g_m(r_d||R_D)$

$-10 = -3.9\frac{mA}{V}\left(\frac{50k\Omega \times R_D}{R_D + 50k\Omega}\right)$

$\frac{10k}{3.96} = \frac{50k\Omega \times R_D}{50k\Omega + R_D}$

$50k + R_D = 19.8R_D$

$R_D = 2.67k\Omega$

Select $\boldsymbol{R_D = 2.7k\Omega, 1/4W}$

Step 7:- Selection of R_G

Select $\boldsymbol{R_G = 1M\Omega, 1/4W}$

Step 8:- Selection V_{DD}

$V_{DS} \geq V_{o_{peak}} + |V_P|$ $\quad [V_{o_{RMS}} = 2V \text{ and } V_{o_{peak}} = 2\sqrt{2}]$

$V_{DS} = 1.5(V_{o_{peak}} + 2.5)$

$V_{DS} = 1.5(2\sqrt{2} + 2.5)$

$V_{DS} \approx 8V$

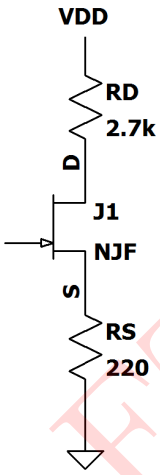

Figure 2: D to S Loop

Applying KVL to the Drain-Source loop:-

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$V_{DD} = V_{DS} + I_D(R_D + R_S)$

$V_{DD} = 8 + 3.5mA(2.7k\Omega + 220\Omega) = 18.22V$

Select $\boldsymbol{V_{DD} = 20V}$

Step 9:- Selection of C_S

$X_{C_S} \leq 0.1R_S$

$\dfrac{1}{2\pi f_{L_{CS}} \leq 0.1R_S}$ $\quad [f_{L_{CS}} = f_L = 20Hz]$

$C_S \geq \dfrac{1}{2\pi f_L \times 0.1R_S} \geq \dfrac{1}{2\pi 20 \times 0.1 \times 220}$

$C_S \geq 361.715\mu F$

Select $\boldsymbol{C_S = 390\mu F/25V}$

Step 10:- Selection of C_{C_1}

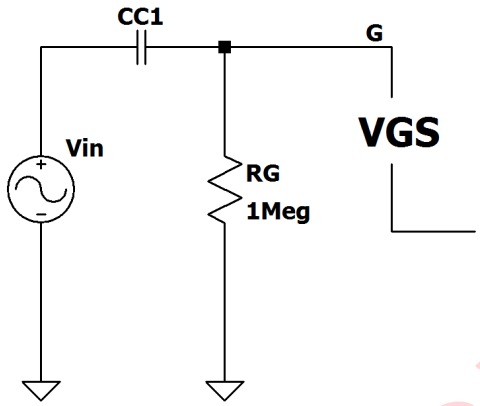

Figure 3: Small Signal low frequency equivalent circuit for C_{C_1}

$$C_{C_1} = \frac{1}{2\pi f_{L_{CC1}} R_{eq}}$$

$R_{eq} = 1M\Omega = R_G$

i.e. $C_{C_1} = \dfrac{1}{2\pi 20 \times 1M\Omega} = 7.95nF$

Select, $\boldsymbol{C_{C_1} = 8.2nF/25V}$

Step 11:- Selection of C_{C_2}

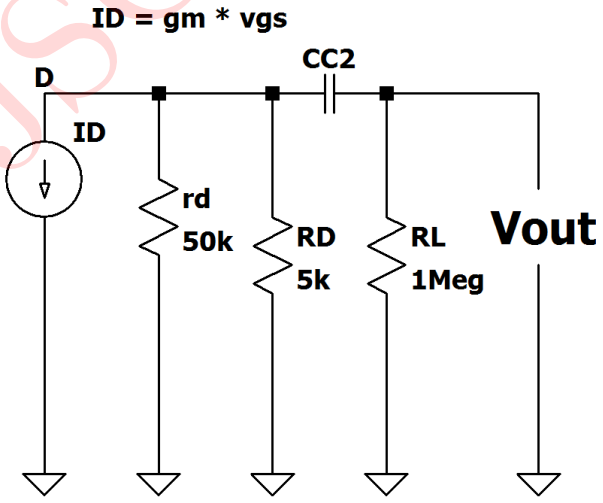

Figure 4: Small Signal low frequency equivalent circuit for C_{C_2}

$$C_{C_2} = \frac{1}{2\pi f_{L_{CC2}} R_{eq}}$$

$R_{eq} = (r_d || R_D) + R_L$

$R_L = R_G = 1M\Omega \qquad [\because R_L \text{ is not given, } R_L = R_{i_{nextstage}}]$

$R_{eq} = (2.7k\Omega || 50k\Omega) + 1M\Omega \approx 1M\Omega$

$$C_{C_2} = \frac{1}{2\pi \times 1 \times 10^6 \times 20} = 7.95\mu F$$

Select, $\boldsymbol{C_{C_2} = 8.2nF/25V}$

Step 12:- Designed Circuit

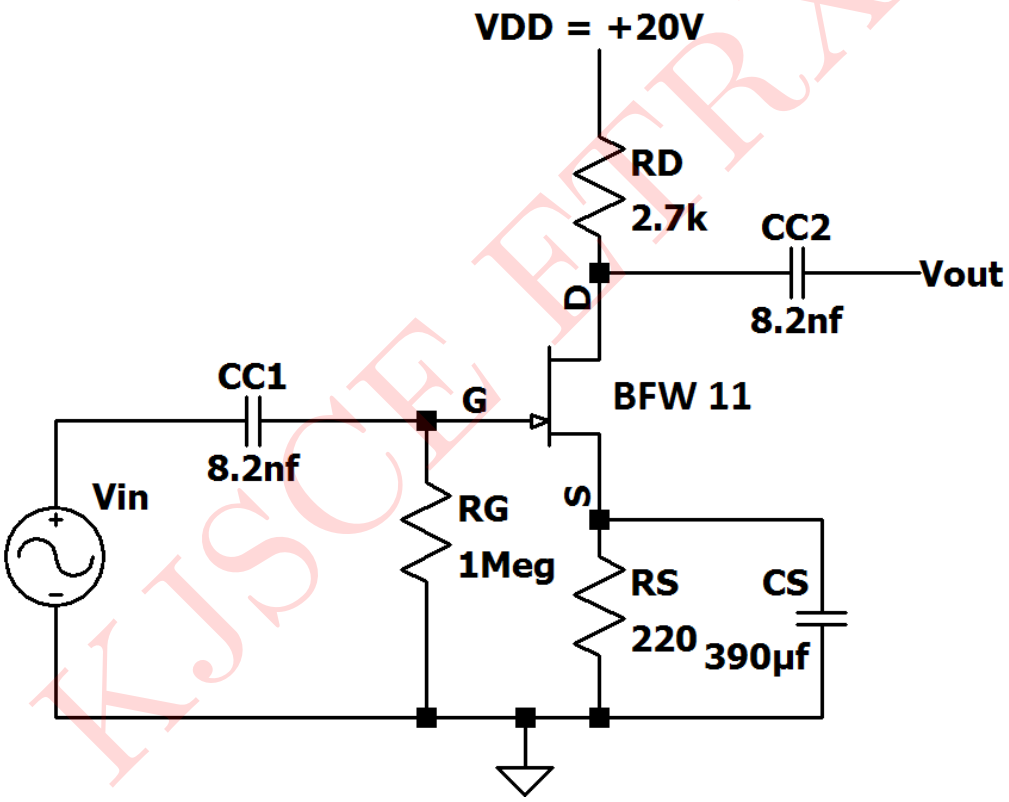

Figure 5: Designed Circuit

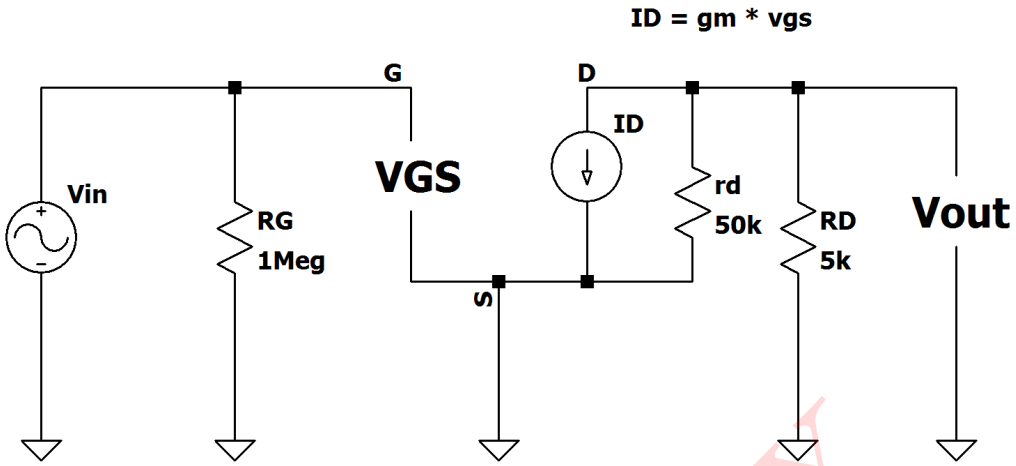

Figure 6: Small Signal Equivalent Circuit

$$A_V = -g_m(R_D||r_d)$$

$$A_V = -3.96\frac{mA}{V}\left(\frac{2.7k\Omega \times 50k\Omega}{52.7k\Omega}\right) = -10.15$$

$$\boldsymbol{A_V = -10.15}$$

Input Impedance:-

$$Z_i = R_G = 1M\Omega$$

$$\boldsymbol{Z_i = 1M\Omega}$$

Output Impedance:-

$$Z_o = R_D||r_d = \left(\frac{2.7k\Omega \times 50k\Omega}{52.7k\Omega}\right) = 2.56k\Omega$$

$$\boldsymbol{Z_o = 2.56k\Omega}$$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

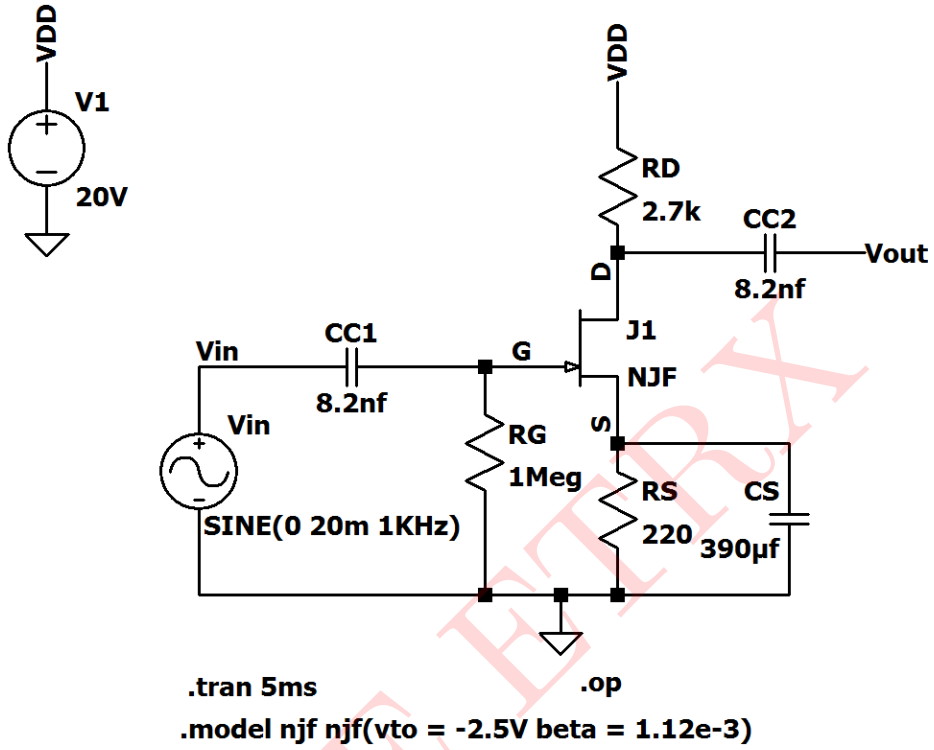

Figure 7: Circuit Schematic 1

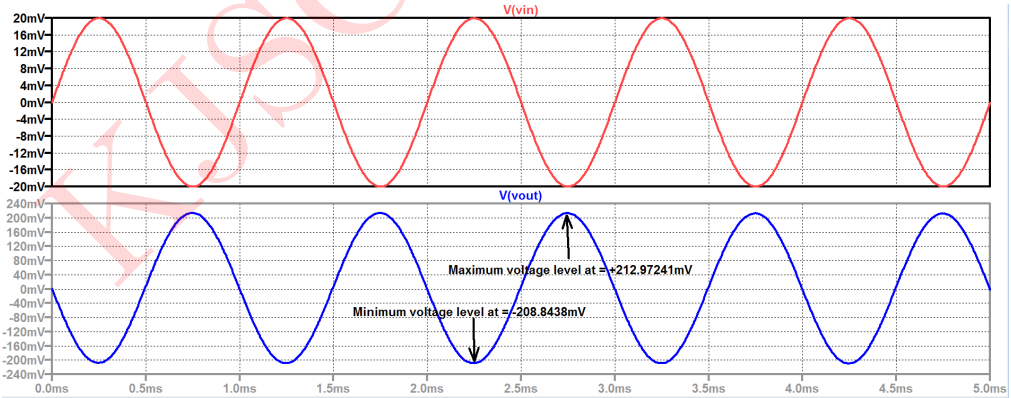

Figure 8: Input & Output waveform

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_D	$3.5mA$	$3.42mA$
A_V	-10.15	-10.51

Table 1: Design 1

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