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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Design of single-stage Amplifier

Design 1:
Design a single stage RC coupled JFET amplifier for following specifications: $V_o = 2.5V$, $f_L \leq 20Hz$, $|A_V| \geq 10$. Select transistor BFW 11 from the datasheet. Use zero-temperature Drift technique. Calculate A_V, Z_i and Z_o of the amplifier you have designed.

Solution:

We use zero-temperature drift biasing:

1) Data:
$|A_V| \leq 10$, $V_o = 2.5V$, $f_L \leq 20Hz$

2) Selection of JFET:
We select N-channel JFET BFW 11 from the datasheet with following specifications:
$g_{m_o} = 5600\mu\mho$, $V_P = -2.5V$, $r_d = 50k\Omega$, $I_{DSS} = 7mA$

3) Selection of biasing network:
We select self-bias circuit for our design

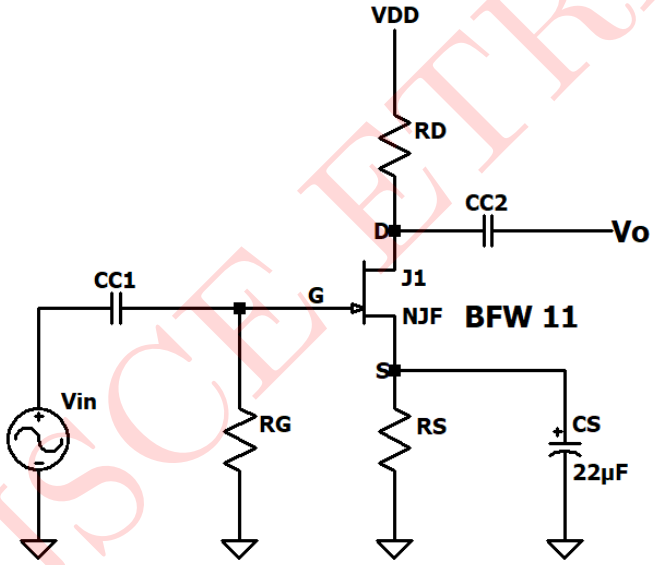

Figure 1: Circuit 1

4) Selection of Q-point:

i) For zero temperature drift,
$|V_P| - |V_{GS}| = 0.63$
$2.5 - |V_{GS}| = 0.63$
$\therefore |V_{GS}| = 1.87$
i.e $V_{GS} = \mathbf{-1.87V}$

ii) $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2$

$I_D = 7mA\left(1 - \dfrac{(-1.87)}{(-2.5)}\right)^2$

$I_D = 7mA(1 - 0.748)^2 = 7mA(0.252)^2 = \mathbf{0.44mA}$

iii) $g_m = g_{m_o}\left(1 - \frac{V_{GS}}{V_P}\right)$

$g_m = 5600 \times 10^{-6}\left(1 - \frac{(-1.87)}{(-2.5)}\right)$

$g_m = 5600 \times 10^{-6}\,(1 - 0.748) = \mathbf{1.4112mA/V}$

5) Selection of R_S:

$V_{GS} = -R_S I_D$ ....(for self-bias network)

i.e $R_S = \frac{-V_{GS}}{I_D} = \frac{1.87}{0.44mA} = 4.25k\Omega$

Select lower standard value(L.S.V) to maintain Q-point in middle of transfer curve.

Select $R_S = \mathbf{3.9k\Omega, 1/4W}$

6) Selection of R_D:

$A_V = -g_m(r_d \parallel R_D)$

$-10 = -g_m\left(\frac{r_d R_D}{r_d + R_D}\right)$

$-10 = -1.4112 \times 20^{-3}\left(\frac{50k\Omega \times R_D}{50k\Omega + R_D}\right)$

$10R_D + 500k\Omega = 70.56 \times R_D$

$500k\Omega = 70.56R_D - 10R_D$

$500k\Omega = 60.56R_D$

$R_D = \frac{500k\Omega}{60.56} = 8.256k\Omega$

Select higher standard value(H.S.V) to increase the gain.

Select $R_D = \mathbf{9.1k\Omega, 1/4W}$

7) Selection of R_G:

To prevent loading of preceding stage,

Select $R_G = \mathbf{1M\Omega, 1/4W}$

8) Selection of V_{DD}:

$V_{DS} \geq V_{o_{peak}} + |V_P|$ ....(condition for undistorted output)

$V_{DS} = 1.5(V_{o_{peak}} + |V_P|)$

$V_{DS} = 1.5(V_{o_{peak}} + 2.5)$

The value is multiplied by 1.5 to take care of saturation voltages, tolerance in resistance value, variation in supply voltage and device parameter variation.

$V_{o_{rms}} = 2.5V$

$\therefore V_{o_{peak}} = 2.5\sqrt{2}$ $(\because V_{o_{peak}} = \sqrt{2}V_{o_{rms}})$

i.e $V_{DS} = 1.5(2.5\sqrt{2} + 2.5) = 1.5(6.03) = \mathbf{9.05V}$

Applying KVL to drain source loop,

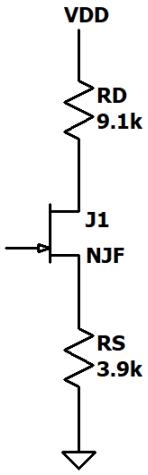

Figure 2: JFET DC circuit: D-S loop

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$\therefore V_{DD} = V_{DS} + I_D(R_D + R_S)$

$V_{DD} = 9.05 + 0.44 \times 10^{-3}(9.1k\Omega + 3.9k\Omega)$

$V_{DD} = 9.05 + 0.44 \times 10^{-3}(13k\Omega)$

$V_{DD} = 9.05 + 5.72 = 14.77$

Select $V_{DD} = \mathbf{15V}$

9) Selection of C_S:

$f_L = 20Hz$

$Y_{CS} \leq 0.1R_S$

i.e $\dfrac{1}{2\pi f_L C_S} \leq 0.1R_S$

i.e $C_S \geq \dfrac{1}{2\pi f_L \times 0.1R_S}$

i.e $C_S \geq \dfrac{1}{2\pi \times 20 \times 0.1 \times 3.9k\Omega}$

i.e $C_S \geq 20.4\mu F$

Select $C_S = \mathbf{22\mu F/25V}$ ....(H.S.V)

10) Selection of C_{C1}:

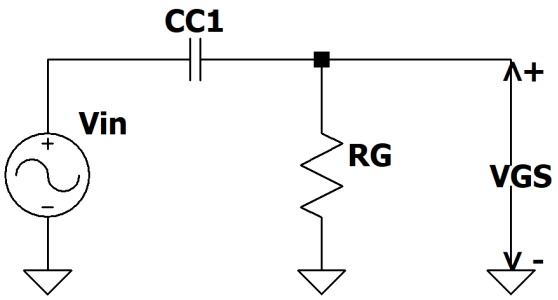

Figure 3: Small Signal low frequency equivalent circuit for C_{C1}

$$C_{C1} = \frac{1}{2\pi f_{L_{C_{C1}}} R_{eq}}$$

$f_{L_{C_{C1}}} = f_L = 20Hz$

$R_{eq} = R_G = 1M\Omega$

$$\therefore C_{C1} = \frac{1}{2\pi \times 20 \times 1M\Omega} = 7.957nF$$

Select $C_{C1} = \mathbf{8.2nF/25V}$ ....(H.S.V)

11) Selection of C_{C2}:

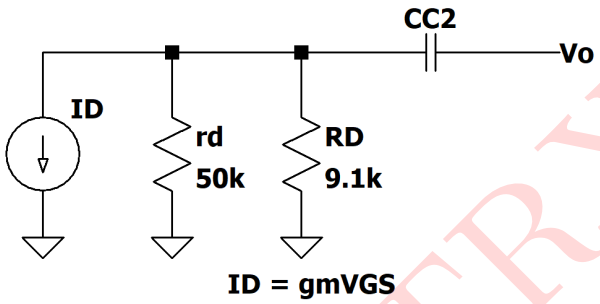

Figure 4: Small Signal Low frequency equivalent circuit for C_{C2}

$$C_{C2} = \frac{1}{2\pi f_{L_{C_{C2}}} R_{eq}}$$

$R_{eq} = r_d \parallel R_D$

$R_{eq} = 50k\Omega \parallel 9.1k\Omega$

$$R_{eq} = \frac{50k\Omega \times 9.1k\Omega}{50k\Omega + 9.1k\Omega} = 7.698k\Omega$$

$f_{L_{C_{C2}}} = f_L = 20Hz$

$$\therefore C_{C2} = \frac{1}{2\pi \times 20 \times 7.698k\Omega} = 1.03\mu F$$

Select $C_{C2} = \mathbf{1.2\mu F}$ ....(H.S.V)

12) Designed circuit is,

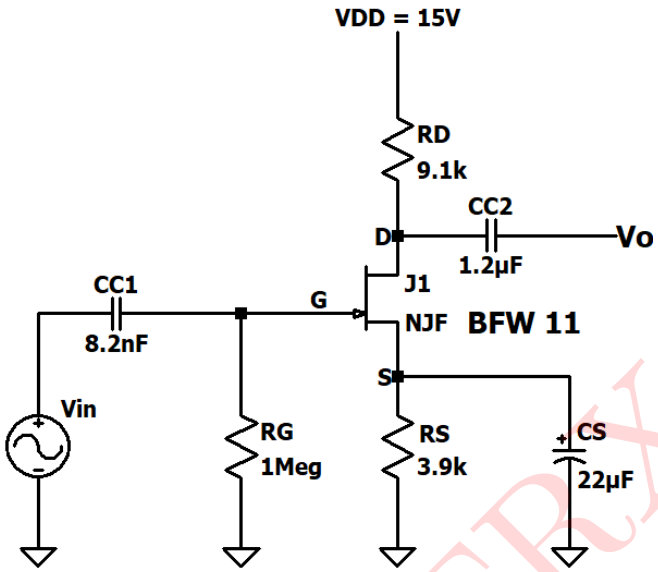

Figure 5: Designed Circuit

Small signal equivalent circuit:

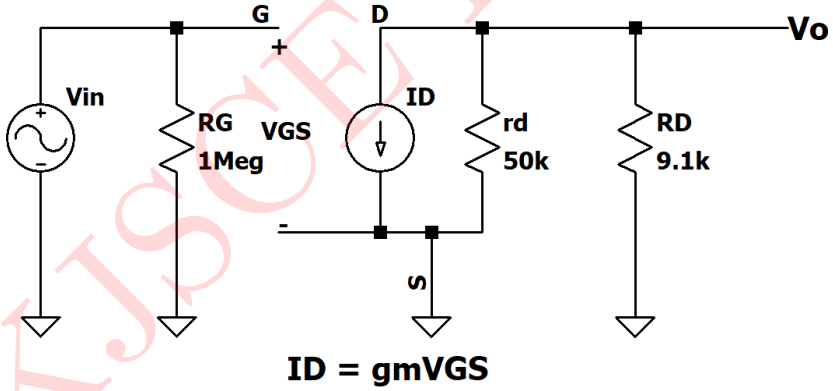

Figure 6: Small signal equivalent circuit

$$A_V = -g_m(r_d \parallel R_D)$$

$$\therefore A_V = -1.4112mA/V(50k\Omega \parallel 9.1k\Omega)$$

$$= -1.4112mA/V\left(\frac{50k\Omega \times 9.1k\Omega}{50k\Omega + 9.1k\Omega}\right)$$

$$= -1.4112mA/V\,(7.698k\Omega) = \mathbf{-10.86}$$

Input impedance,
$Z_i = R_G = \mathbf{1M\Omega}$

Output impedance,
$Z_o = r_d \parallel R_D$
$= 50k\Omega \parallel 9.1k\Omega$
$= \dfrac{50k\Omega \times 9.1k\Omega}{50k\Omega + 9.1k\Omega} = \mathbf{7.698k\Omega}$

SIMULATED RESULTS:
Above circuit is simulated in LTspice and results are as follows:

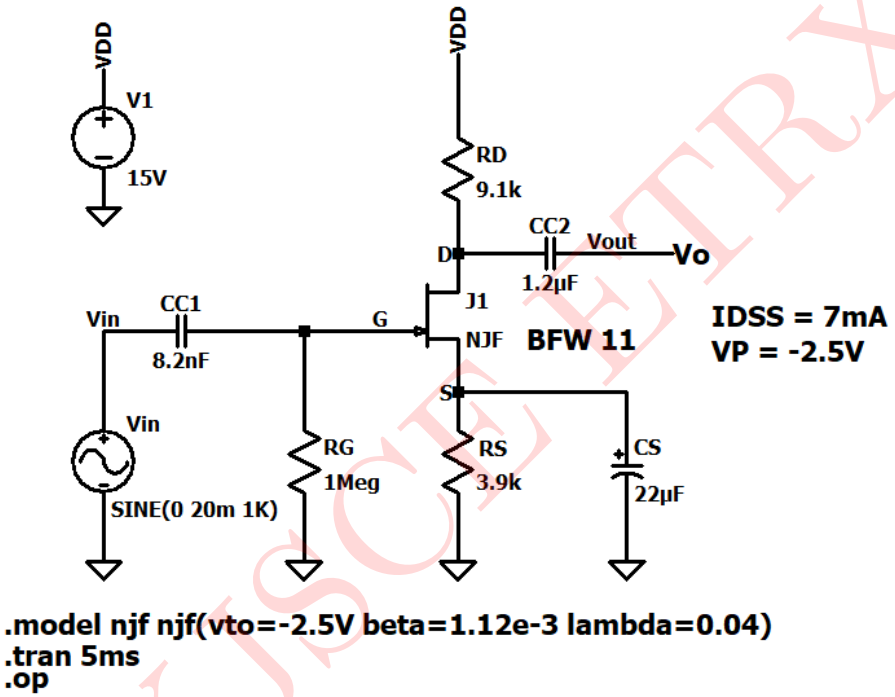

Figure 7: Circuit Schematic

The input and output waveforms are shown in figure 8.

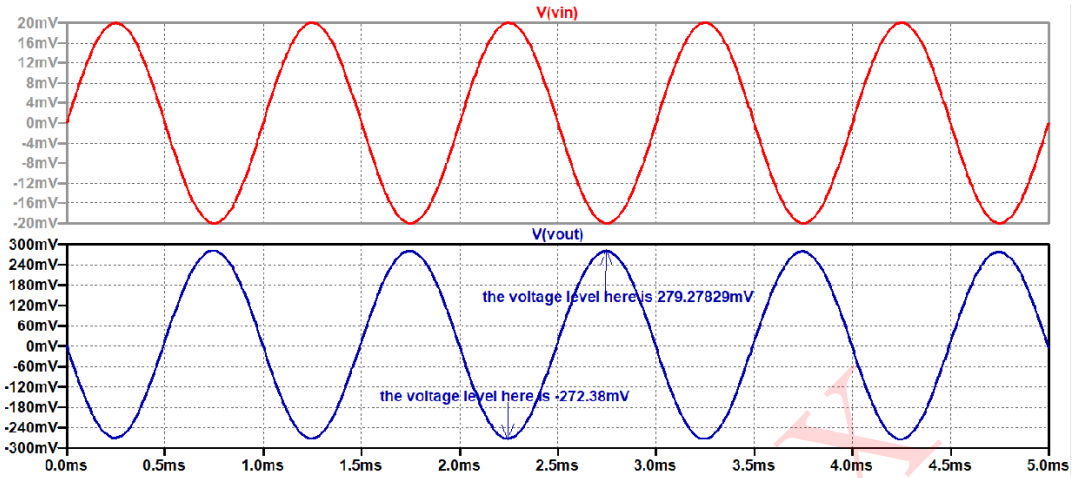

Figure 8: Input-Output waveforms

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
I_D	0.44mA	0.4741mA
$\|A_V\|$	$\geq$10	13.79

Table 1: Design 1

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