**K. J. SOMAIYA COLLEGE OF ENGINEERING**
**DEPARTMENT OF ELECTRONICS ENGINEERING**
**ELECTRONIC CIRCUITS**
**Multi-transistor circuits**

## Numerical 1

The parameters for each circuit shown in figure 1 are $\beta_1 = \beta_2 = 110$ & $V_A = \infty$

a) Determine small signal parameters

b) Determine small signal voltage gain assuming $V_{o_1}$ is connected to o.c, then determine small signal voltage gain for stage 2.

c) Determine the overall small signal voltage gain

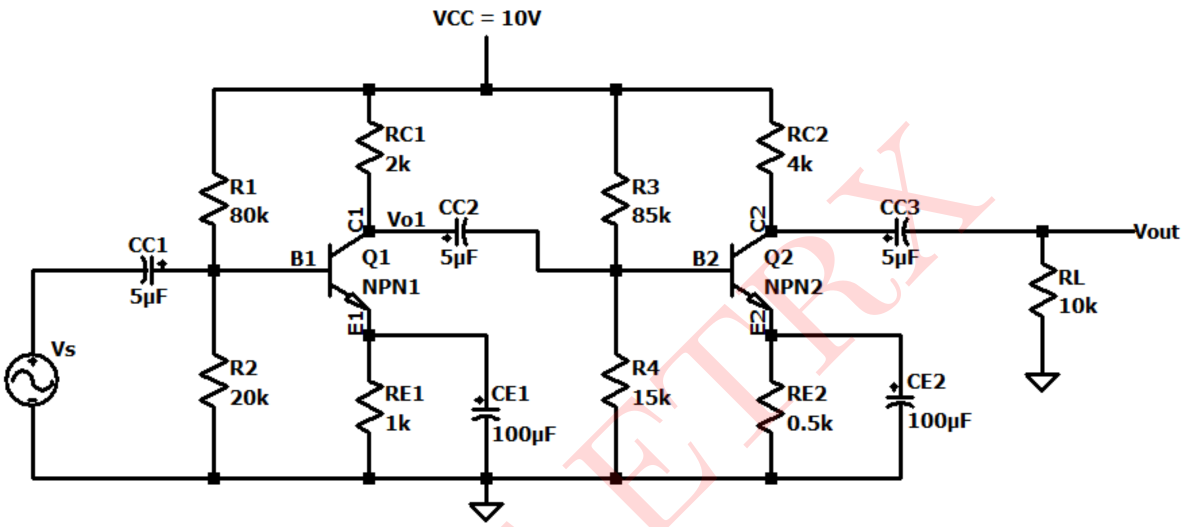


Figure 1: Circuit for Numerical 1



**Solution:** The above circuit is a 2-stage RC coupled CE-CE amplifier

**<u>DC Anaylsis:</u>** During DC analysis, capacitors become open circuit.

Since both the stages are different, DC analysis for both the stages will be different.

**STAGE-1:**

From figure 1 we get,

$R_{th_1} = R_1 \parallel R_2 = 80k \parallel 20k$

$\therefore \mathbf{R_{th_1} = 16k\Omega}$

$$V_{th_1} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{20k}{20k + 80k} \times 10$$

$\therefore \mathbf{V_{th_1} = 2V}$

The thevenin's equivalent circuit for stage-1 is shown in figure 2

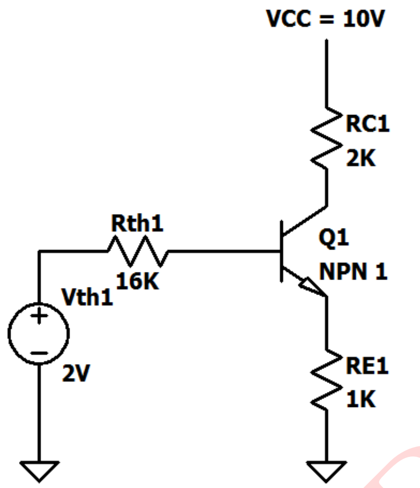


Figure 2: Thevenin's Equivalent Circuit for Stage-1

Applying KVL to the B-E loop for figure 2 we get,

$V_{th_1} - I_{BQ_1}R_{th_1} - V_{BE_1} - I_{E_1}R_{E_1} = 0$

$V_{th_1} - I_{BQ_1}R_{th_1} - V_{BE_1} - (1+\beta_1)I_{BQ_1}R_{E_1} = 0 \qquad (\because I_E = (1+\beta)I_B)$

$$I_{BQ_1} = \frac{V_{th_1} - V_{BE_1}}{R_{th_1} + (1+\beta_1)R_{E_1}} = \frac{2V - 0.7V}{16k + (1+110)\times 1K}$$

$\therefore \mathbf{I_{BQ_1} = 10.23\mu A}$

$I_{CQ_1} = \beta_1 \times I_{BQ_1} = 110 \times 10.23\mu A$

$\therefore \mathbf{I_{CQ_1} = 1.126mA}$

Applying KVL to C-E loop of figure 2 we get,

$V_{CC} - I_{CQ_1}R_{C_1} - V_{CEQ_1} - I_{CQ_1}R_{E_1} = 0$

$V_{CEQ_1} = V_{CC} - I_{CQ_1}(R_{C_1} + R_{E_1}) = 10 - 1.126mA(2k + 1k)$

$\therefore \mathbf{V_{CEQ_1} = 6.622V}$

**Calculation of small signal parameters:**

$$g_{m_1} = \frac{I_{CQ_1}}{V_T} = \frac{1.126mA}{0.026}$$

$\therefore \mathbf{g_{m_1} = 43.30mA/V}$

$$r_{\pi_1} = \frac{\beta_1 V_T}{I_{CQ_1}} = \frac{110 \times 26mV}{1.126mA}$$

$\therefore \mathbf{r_{\pi_1} = 2.5k\Omega}$

$\mathbf{r_{o_1}} = \infty \qquad (\because V_A = \infty)$

**STAGE-2:**

From figure 1 we get,

$R_{th_2} = R_3 \parallel R_4 = 85k \parallel 15k$

$\therefore \mathbf{R_{th_2} = 12.75k\Omega}$

$$V_{th_2} = \frac{R_4}{R_3 + R_4} \times V_{CC} = \frac{15k}{15k + 85k} \times 10$$

$\therefore \mathbf{V_{th_2} = 1.5V}$

The thevenin's equivalent circuit for stage-2 is shown in figure 3

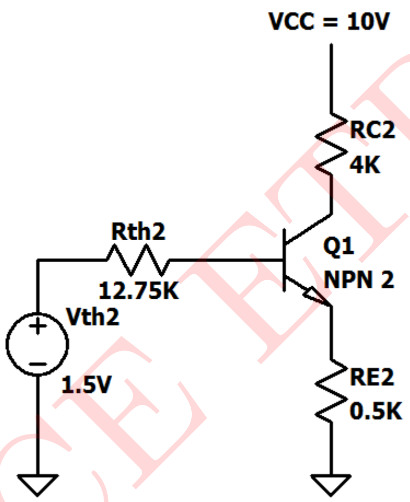


Figure 3: Thevenin's Equivalent Circuit for Stage-2

Applying KVL to the B-E loop for figure 2 we get,

$V_{th_2} - I_{BQ_2}R_{th_2} - V_{BE_2} - I_{E_2}R_{E_2} = 0$

$V_{th_2} - I_{BQ_2}R_{th_2} - V_{BE_2} - (1 + \beta_2)I_{BQ_2}R_{E_2} = 0$ $\quad (\because I_E = (1 + \beta_2)I_B)$

$$I_{BQ_2} = \frac{V_{th_2} - V_{BE_2}}{R_{th_2} + (1 + \beta_2)R_{E_2}} = \frac{1.5V - 0.7V}{12.75k + (1 + 110) \times 0.5k}$$

$\therefore \mathbf{I_{BQ_1} = 11.722\mu A}$

$I_{CQ_2} = \beta_2 \times I_{BQ_2} = 110 \times 11.722\mu A$

$\therefore \mathbf{I_{CQ_2} = 1.289mA}$

Applying KVL to C-E loop of figure 3 we get,

$V_{CC} - I_{CQ_2}R_{C_2} - V_{CEQ_2} - I_{CQ_2}R_{E_2} = 0$

$V_{CEQ_2} = V_{CC} - I_{CQ_2}(R_{C_2} + R_{E_2}) = 10 - 1.289mA(4k + 0.5k)$

$\therefore \mathbf{V_{CEQ_2} = 4.199V}$

**Calculation of small signal parameters:**

$$g_{m_2} = \frac{I_{CQ_2}}{V_T} = \frac{1.289mA}{0.026}$$

$$\therefore \mathbf{g_{m_2} = 49.576mA/V}$$

$$r_{\pi_2} = \frac{\beta_2 V_T}{I_{CQ_2}} = \frac{110 \times 26mV}{1.289mA}$$

$$\therefore \mathbf{r_{\pi_2} = 2.2k\Omega}$$

$$\mathbf{r_{o_2}} = \infty \qquad\qquad (\because V_A = \infty)$$

## AC Analysis:

Mid band small signal equivalent circuit is shown in figure 4

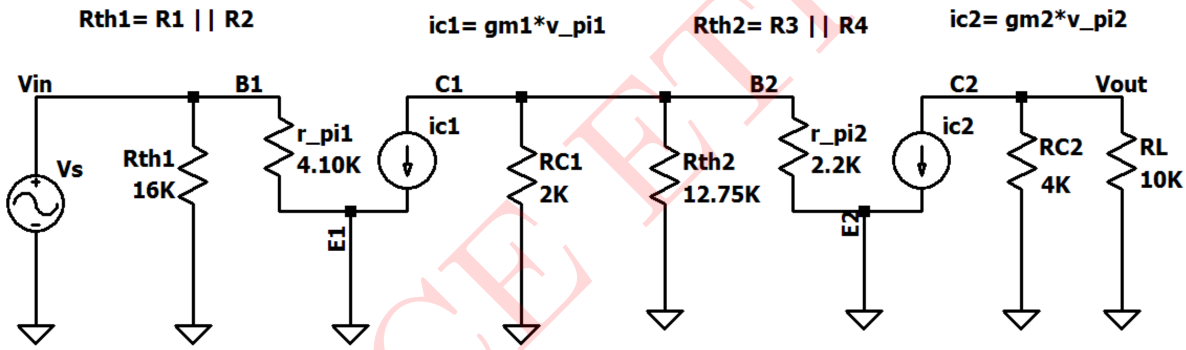


Figure 4: Small Signal Equivalent Circuit

**Calculation of voltage gain:**

$$A_{V(mid)} = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_{o_1}} \times \frac{V_{o_1}}{V_{in}}$$

For Stage-1:

$$A_{V_1} = \frac{V_{o_1}}{V_{in}} = -g_{m_1}(R_{C_1} \parallel R_{th_2} \parallel r_{\pi_2}) = -43.30mA/V(2k \parallel 12.75k \parallel 2.2k)$$

$$\mathbf{A_{V_1} = -41.91}$$

For Stage-2:

$$A_{V_2} = \frac{V_{out}}{V_{o_1}} = -g_{m_2}(R_{C_2} \parallel R_L) = -49.576mA/V(4k \parallel 10k)$$

$$\mathbf{A_{V_2} = -141.645}$$

**The overall voltage gain $\mathbf{A_{V(mid)}}$**

$$A_{V(mid)} = -141.645 \times -41.91 = 5936.34$$

$$A_{V(mid)(dB)} = 20log(5936.34)$$

$A_{V(mid)(dB)} = 75.47dB$

**SIMULATED RESULTS:**

Above circuit is simulated in LTspice and results are as follows:

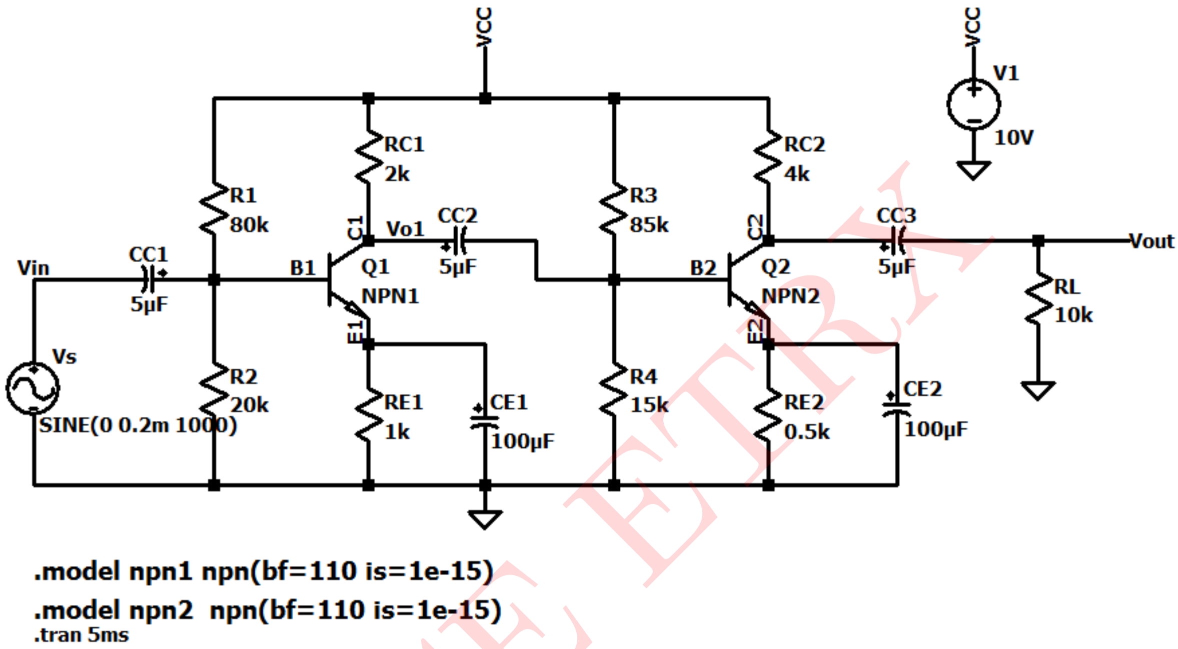


Figure 5: Circuit Schematics: Results



**Output Waveforms:**

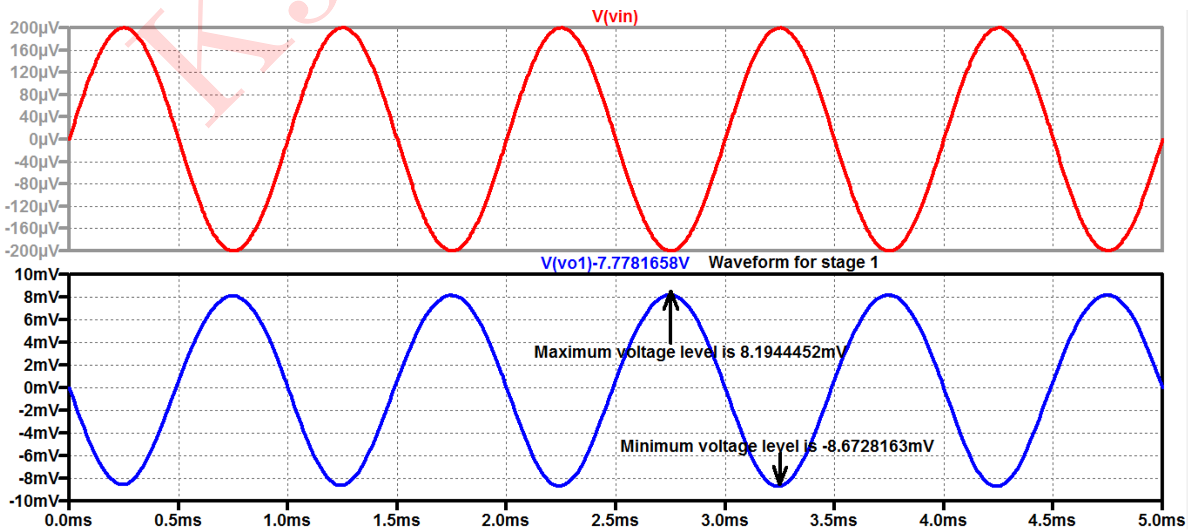


Figure 6: Input and Output Waveforms for $1^{st}$ Stage

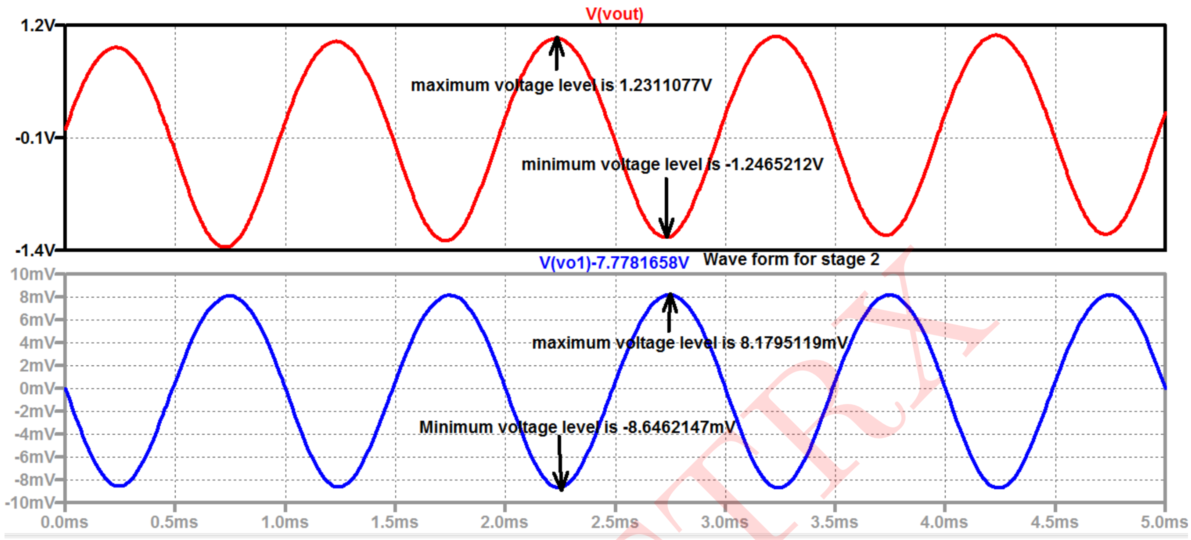


Figure 7: Input and Output Waveforms for $2^{nd}$ Stage



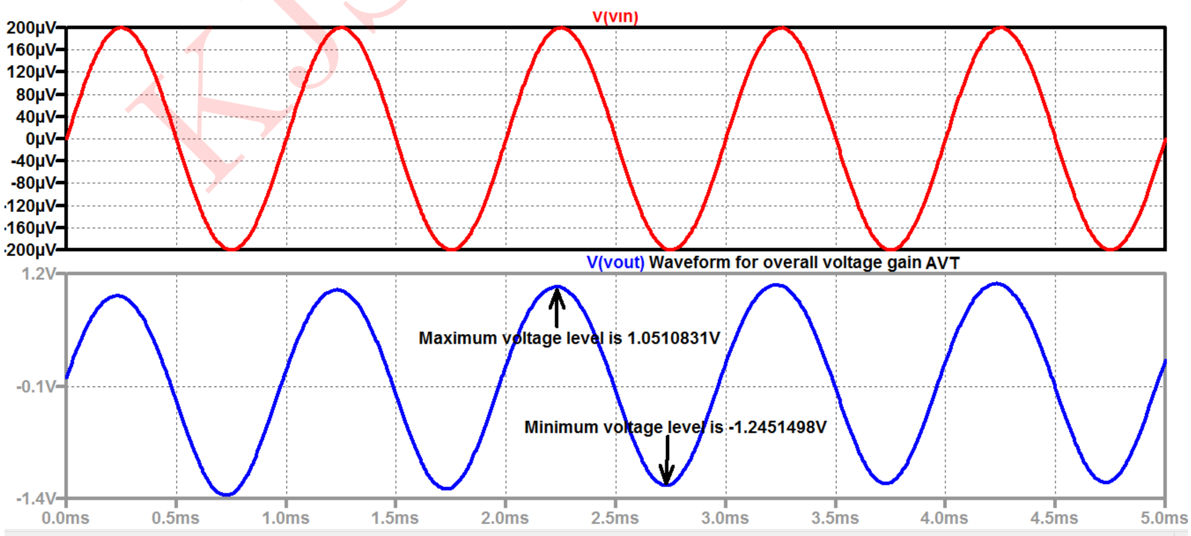


Figure 8: Input and Output Waveforms for the circuit

Comparison between theoretical and simulated values is given below:

| **Parameters** | **Simulated Values** | **Theoretical Values** |
|---|---|---|
| Stage-1: $I_{CQ_1}$ | $1.11mA$ | $1.126mA$ |
| Stage-1: $V_{CEQ_1}$ | $6.65V$ | $6.622V$ |
| Stage-2: $I_{CQ_2}$ | $1.25mA$ | $1.289mA$ |
| Stage-2: $V_{CEQ_2}$ | $4.34V$ | $4.199V$ |
| Stage-1: Voltage gain | $-42.1$ | $-41.91$ |
| Stage-2: Voltage gain | $-138.52$ | $-141.645$ |
| Overall voltage gain $A_V$ in dB | $75.155dB$ | $75.47dB$ |

Table 1: Numerical 1

**Numerical 2**

Calculate the DC bias, output impedance, voltage gain and resulting voltage for cascade amplifier shown in figure 9. Calculate the load voltage if $10k\Omega$ is connected across the output.

Given: $R_L = 10k\Omega$, $I_{DSS} = 10mA$, $V_P = -4V$

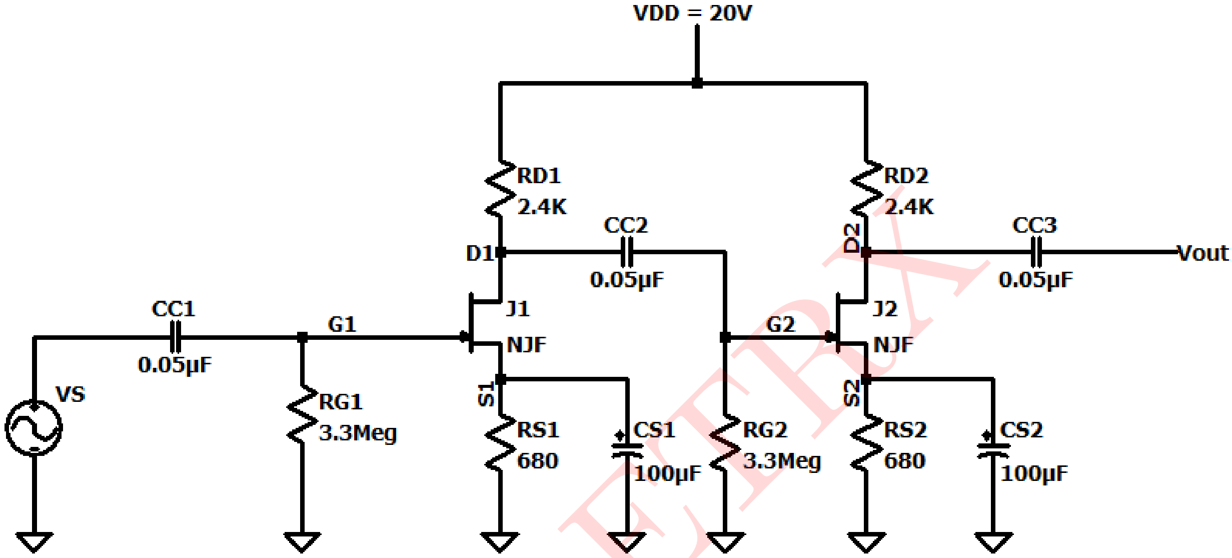


Figure 9: Circuit for Numerical 2

**Solution:** The above circuit is a 2-stage RC coupled cascaded amplifier

<u>**DC Anaylsis:**</u> During DC analysis, capacitors become open circuit.

Due to RC coupling, both the stage's Q-points are isolated. Since both the stage's parameters and resistor values are identical, DC analysis of one stage will be sufficient.

The DC equivalent circuit for stage-1 is shown in figure 10

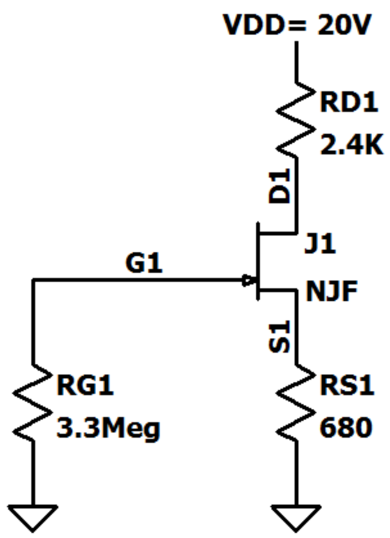


Figure 10: DC Equivalent Circuit for Stage-1

Applying KVL to G-S loop of figure 10 we get,

$V_{GS_1} = -I_{D_1} R_{S_1}$

$V_{GS_1} = -I_{D_1}(680)$ .....(1)

$$I_{D_1} = I_{DSS}\left(1 - \frac{V_{GS_1}}{V_P}\right)^2$$

$$I_{D_1} = 10mA \times \left(1 + \frac{V_{GS_1}}{4}\right)^2 \qquad .....(2)$$

Substituting (2) in (1) we get,

$$V_{GS_1} = -6.8\left(1 + \frac{V_{GS_1}}{2} + \frac{V_{GS_1}^2}{16}\right)$$

$V_{GS_1} = -6.8 - 3.4V_{GS_1} - 0.425V_{GS_1}^2$

$0.425V_{GS_1}^2 + 4.4V_{GS_1} + 6.8 = 0$

Solving the above quadratic equation we get,

$V_{GS_1} = -1.89V$ or $V_{GS_1} = -8.46V$

$\mathbf{V_{GS_1} = -1.89V}$ $\qquad (\because V_{GS} > V_P)$

$$I_{D_1} = 10mA \times \left(1 - \frac{(-1.89V)}{(-4)}\right)^2$$

$\mathbf{I_{D_1} = 2.779mA}$

Both the stages are identical so, $V_{GS_1} = V_{GS_2} = -1.89V$ & $I_{D_1} = I_{D_2} = 2.779mA$

**Calculation of small signal parameters:**

$$g_{m_1} = \frac{2I_{DSS}}{\mid V_P \mid}\left(1 - \frac{V_{GS_1}}{V_P}\right) = \frac{2 \times 10mA}{\mid -4 \mid}\left(1 - \frac{(-1.89V)}{(-4V)}\right)$$

$\mathbf{g_{m_1} = 2.6mA/V}$

i.e. $g_{m_1} = gm_2 = 2.6mA/V$

## AC Analysis:

Mid band small signal equivalent circuit is shown in figure 11

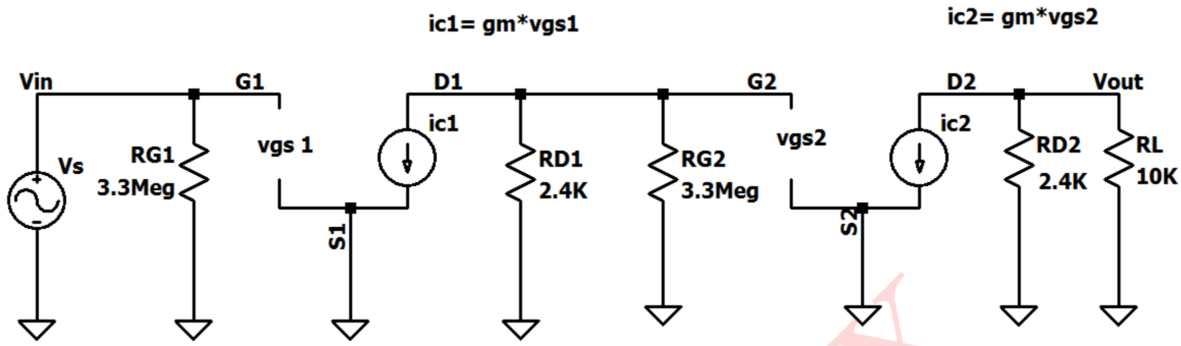


Figure 11: Small Signal Equivalent Circuit

**Calculation of voltage gain:**

$$A_{V(mid)} = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_{o_1}} \times \frac{V_{o_1}}{V_{in}}$$

For Stage-1:

$$A_{V_1} = \frac{V_{o_1}}{V_{in}} = -g_{m_1}(R_{D_1} \parallel R_{G_2}) = -2.6mA/V(2.4k \parallel 3.3M) \approx -2.6mA/V \times 2.4k$$

$$\mathbf{A_{V_1} = -6.24}$$

For Stage-2:

$$A_{V_2} = \frac{V_{out}}{V_{o_1}} = -g_{m_2}(R_{D_2}) = -2.6mA/V \times 2.4k$$

$$\mathbf{A_{V_2} = -6.24}$$

**The overall voltage gain $\mathbf{A_{V_T}}$:**

$$A_{V_T} = A_{V_1} \times A_{V_2} = -6.24 \times -6.24$$

$$\mathbf{A_{V_T} = 38.93}$$

$$A_{V_T}(dB) = 20log_{10}(38.93)$$

$$\mathbf{A_{V_T}(dB) = 31.80dB}$$

**Calculation of output voltage $\mathbf{V_o}$:**

$$V_o = A_{V_T} \times V_i = 38.93 \times 10mV$$

$$\mathbf{V_o = 389.3mV}$$

**Calculation of input and output impedances:**

$$Z_i = R_G$$
$$\mathbf{Z_i = 3.3M\Omega}$$

$Z_o = R_D$

$\mathbf{Z_o = 2.4k\Omega}$

**The output voltage across 10kΩ load:**

$$V_L = \frac{R_L}{Z_o + R_L} \times V_o = \frac{10k}{2.4k + 10k} \times 389.3mV$$

$\mathbf{V_L = 313.7mV}$

**SIMULATED RESULTS:**

Above circuit is simulated in LTspice and results are as follows:

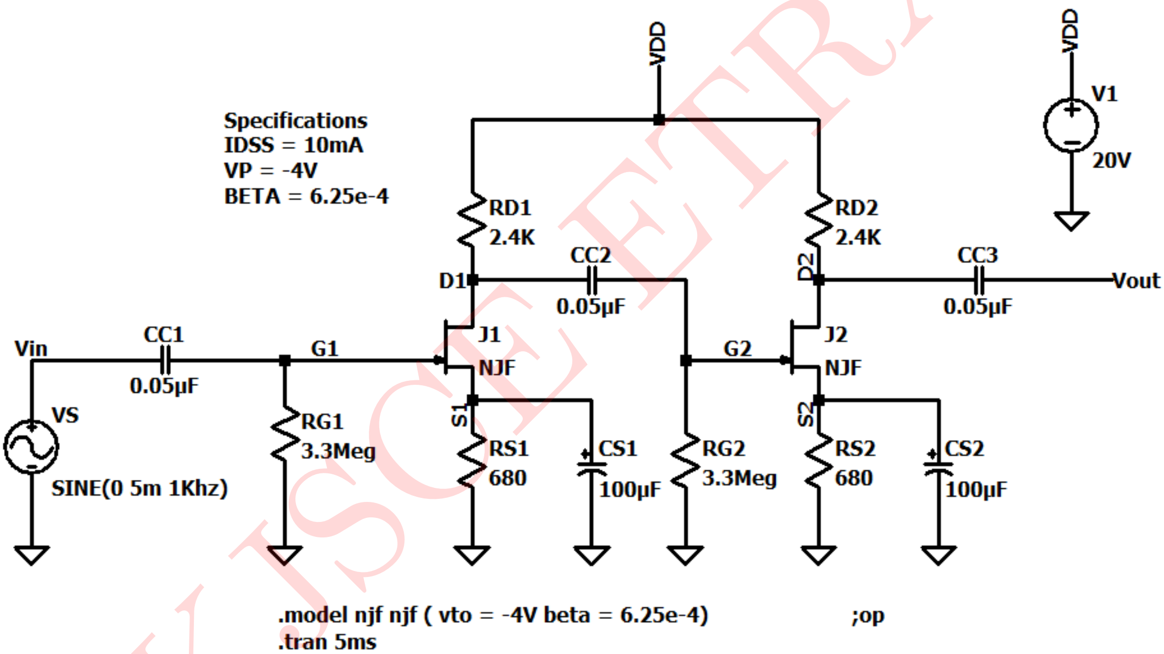


Figure 12: Circuit Schematics: Results

**Output Waveforms:**

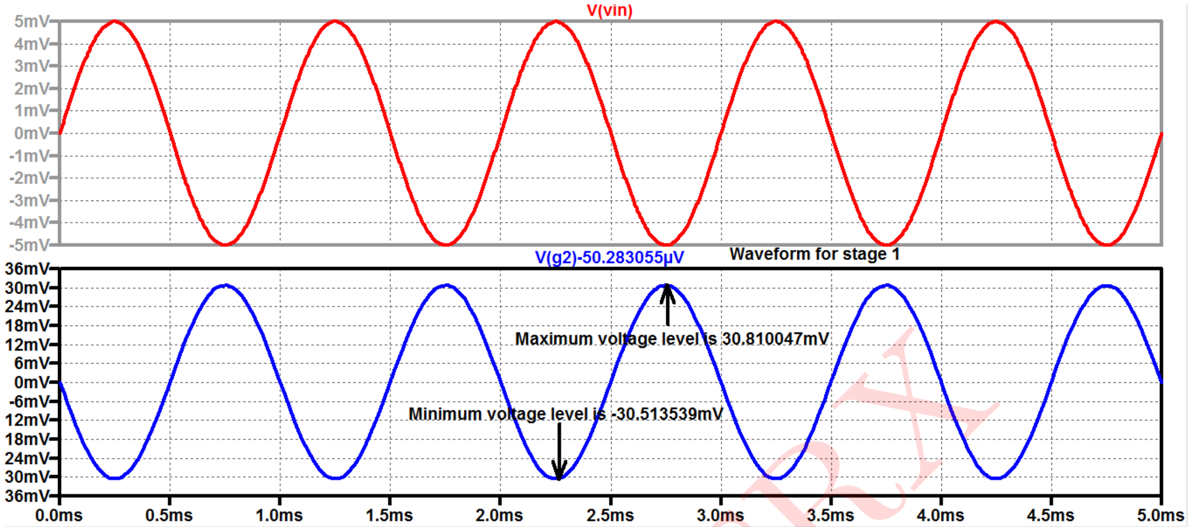


Figure 13: Input and Output Waveforms for $1^{st}$ Stage

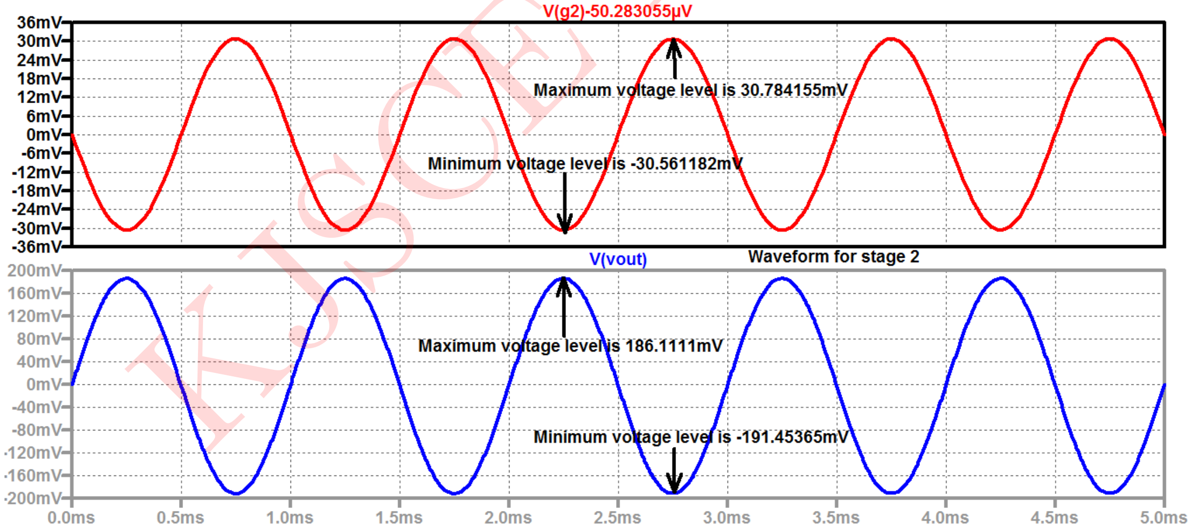


Figure 14: Input and Output Waveforms for $2^{nd}$ Stage

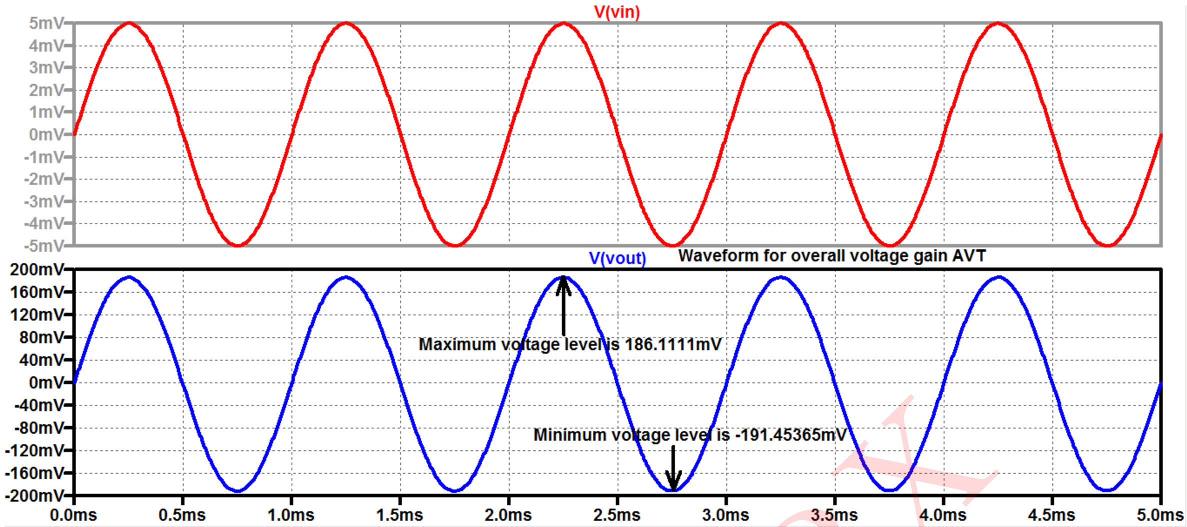


Figure 15: Input and Output Waveforms for the circuit

Comparison between theoretical and simulated values is given below:

| Parameters | Simulated Values | Theoretical Values |
|---|---|---|
| Stage-1: $I_{DQ_1}$ | $2.78mA$ | $2.779mA$ |
| Stage-1: $V_{GSQ_1}$ | $-1.89V$ | $-1.89V$ |
| Stage-2: $I_{DQ_2}$ | $2.78mA$ | $2.779mA$ |
| Stage-2: $V_{GSQ_2}$ | $-1.89V$ | $-1.89V$ |
| Stage-1: Voltage gain $A_{V_1}$ | $-6.12$ | $-6.24$ |
| Stage-2: Voltage gain $A_{V_2}$ | $-6.14$ | $-6.24$ |
| Overall Voltage gain $A_{V_T}$ | $31.52dB$ | $31.80dB$ |
| Output Voltage | $0.377V$ | $0.38V$ |
| Input impedance $Z_i$ | – | $3.3M\Omega$ |
| Output impedance $Z_o$ | – | $2.4k\Omega$ |

Table 2: Numerical 2

**Numerical 3**

A two stage circuit is shown in figure 16, its BJT parameters are $\beta_1 = \beta_2 = 20$ & $V_{BE_1} = V_{BE_2} = 0.6V$

a) Determine all node voltages and terminal currents under DC analysis

b) Determine the overall small signal voltage gain

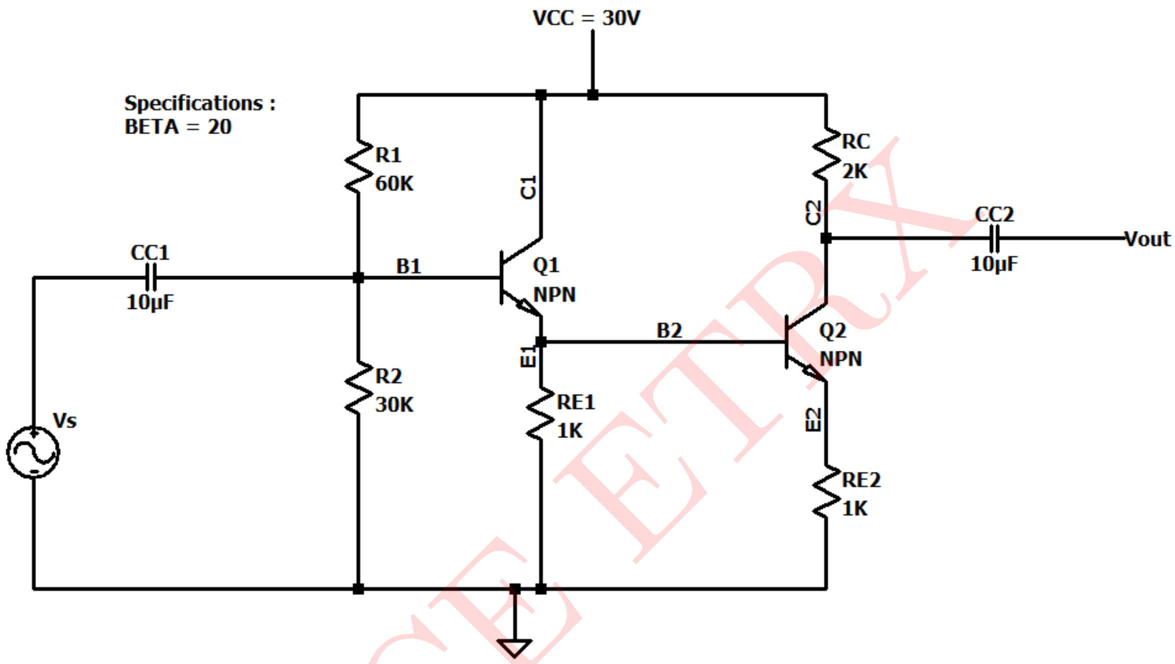


Figure 16: Circuit for Numerical 3

**Solution:**

<u>**DC Anaylsis:**</u> During DC analysis, capacitors become open circuit.

Since both the stages are different, DC analysis for both the stages will be different.

**STAGE-1:**

From figure 1 we get,

$R_{th_1} = R_1 \parallel R_2 = 60k \parallel 30k$

$\mathbf{R_{th_1} = 20k\Omega}$

$$V_{th_1} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{30k}{30k + 60k} \times 30V$$

$\mathbf{V_{th_1} = 10V}$

The thevenin's equivalent of base circuit of $Q_1$ is shown in figure 17

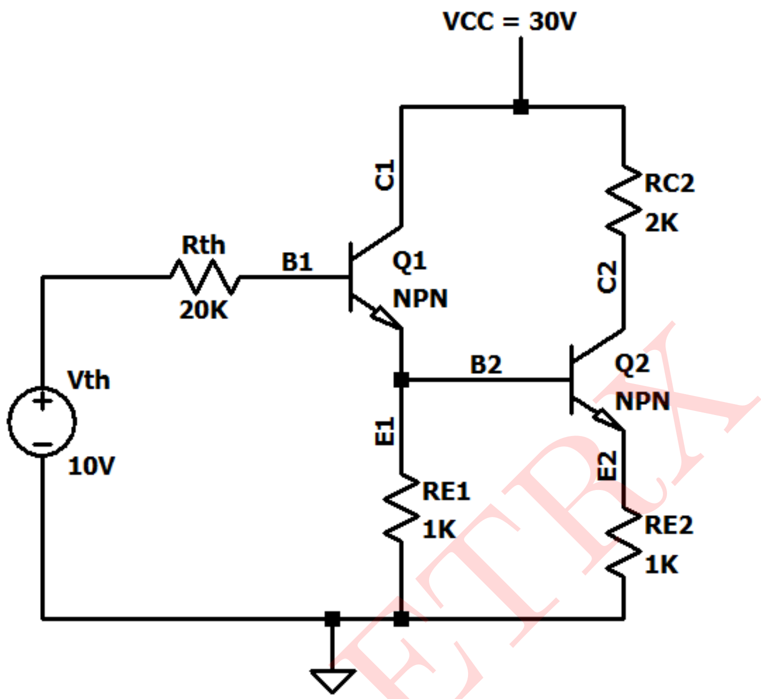


Figure 17: Thevenin's Equivalent Circuit

**Calculation of terminal currents for stage-1:**

Applying KVL to the B-E loop for figure 17 we get,

$V_{th} - I_{B_1}R_{th} - V_{BE_1} - I_{E_1}R_{E_1} = 0$

$V_{th} - I_{B_1}R_{th} - V_{BE_1} - (1+\beta_1)I_{B_1}R_{E_1} = 0$ $\qquad (\because I_E = (1+\beta)I_B)$

$$I_{B_1} = \frac{V_{th} - V_{BE_1}}{R_{th} + (1+\beta_1)R_{E_1}} = \frac{10V - 0.7V}{20k + (1+20)\times 1k}$$

$\mathbf{I_{B_1} = 229.27\mu A}$

$I_{C_1} = \beta_1 \times I_{B_1} = 20 \times 229.27\mu A$

$\mathbf{I_{C_1} = 4.585mA}$

Now, $I_{E_1} = I_{C_1} + I_{B_1} = 4.585mA + 229.27\mu A$

$\mathbf{I_{E_1} = 4.814mA}$

**Calculation of node voltages of stage-1:**

$V_{E_1} = I_{E_1}R_{E_1} = 4.814mA \times 1k\Omega$

$\mathbf{V_{E_1} = 4.814V}$

$V_{B_1} = V_{BE_1} + V_{E_1} = 0.6V + 4.814V$

$\mathbf{V_{B_1} = 5.414V}$

**STAGE-2:**

**Calculation of node voltages of stage-2:**

From figure 2 we get,

$V_{E_1} = V_{B_2}$

$\mathbf{V_{B_2} = 4.814V}$

$V_{E_2} = V_{B_2} - V_{BE_2} = 4.814V - 0.6V$

$\mathbf{V_{E_2} = 4.214V}$

$V_{C_2} = V_{CC} - I_{C_2}R_{C_2}$

$V_{C_2} = 30V - I_{C_2} \times 2k$ .....(1)

**Calculation of terminal currents of stage-2:**

$I_{E_2} = \frac{V_{E_2}}{R_{E_2}} = \frac{4.214V}{1k}$

$\mathbf{I_{E_2} = 4.214mA}$

$I_{C_2} = \alpha_2 \times I_{E_2} = \frac{\beta_2}{1+\beta_2} \times I_{E_2} = \frac{20}{21} \times 4.214mA$

$\mathbf{I_{C_2} = 4.013mA}$ .....(2)

$I_{B_2} = \frac{I_{E_2}}{1+\beta_2} = \frac{4.214mA}{21}$

$\mathbf{I_{B_2} = 200.67\mu A}$

From (1) and (2) we get,

$V_{C_2} = 30 - 3.822mA \times 2k$

$\mathbf{V_{C_2} = 22.356V}$

**Calculation of small signal parameters:**

$g_{m_1} = \frac{I_{CQ_1}}{V_T} = \frac{4.585mA}{0.026V}$

$\mathbf{g_{m_1} = 176.35mA/V}$

$r_{\pi_1} = \frac{\beta_1 V_T}{I_{CQ_1}} = \frac{20 \times 26mV}{4.585mA}$

$\mathbf{r_{\pi_1} = 113.41\Omega}$

$$g_{m_2} = \frac{I_{CQ_2}}{V_T} = \frac{3.822mA}{0.026}$$

$$\mathbf{g_{m_2} = 147mA/V}$$

$$r_{\pi_2} = \frac{\beta_2 V_T}{I_{CQ_2}} = \frac{20 \times 26mV}{3.822mA}$$

$$\mathbf{r_{\pi_2} = 136.054\Omega}$$

## AC Analysis:

Mid band small signal equivalent circuit is shown in figure 18

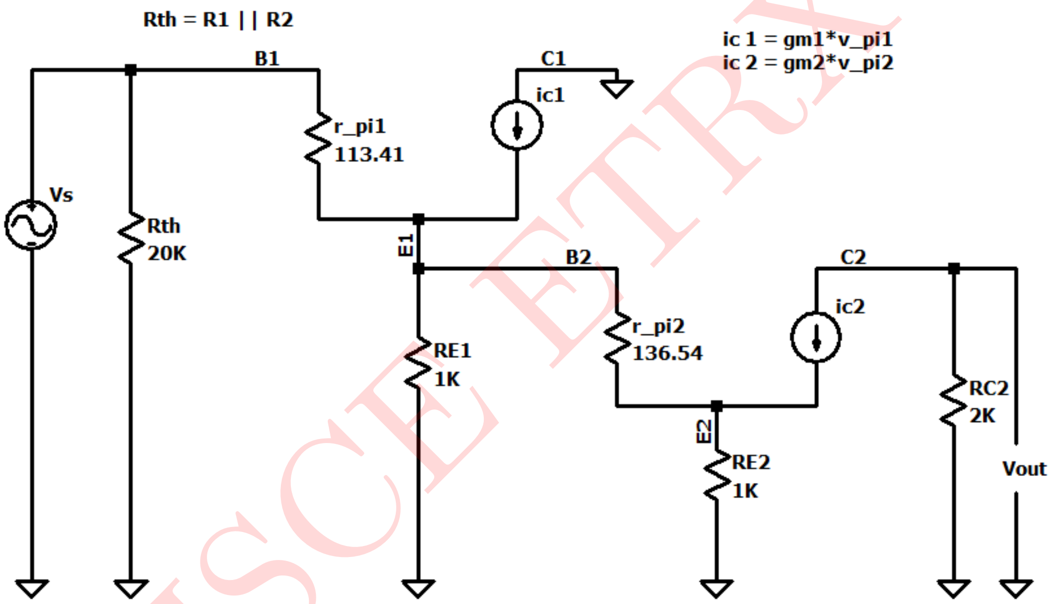


Figure 18: Small Signal Equivalent Circuit



**Calculation of voltage gain:**

$$A_{V_T} = \frac{V_{out}}{V_s} = \frac{V_{out}}{V_{o1}} \times \frac{V_{o1}}{V_s}$$

For Stage-1:

$$A_{V_1} = \frac{V_{o1}}{V_s} = \frac{(g_{m_1} V_{\pi_1}) R_{E_1}}{i_{b_1}[r_{\pi_1} + (1+\beta) R_{E_1}]}$$

$$A_{V_1} = \frac{\beta i_{b_1} R_{E_1}}{i_{b_1}[r_{\pi_1} + (1+\beta) R_{E_1}]} \qquad (\because ic_1 = g_{m_1} V_{\pi_1} = \beta i_{b_1})$$

$$A_{V_1} = \frac{\beta R_{E_1}}{r_{\pi_1} + (1+\beta) R_{E_1}}$$

$$A_{V_1} = \frac{20 \times 1k}{113.41 + 21 \times 1k}$$

$$\mathbf{A_{V_1} = -0.9473}$$

For Stage-2:

$$A_{V_2} = \frac{V_{out}}{V_{o_1}} = \frac{-(g_{m_2} V_{\pi_2}) R_{C_2}}{i_{b_2}[r_{\pi_2} + (1+\beta) R_{E_2}]}$$

$$A_{V_2} = \frac{-\beta i_{b_2} R_{C_2}}{i_{b_2}[r_{\pi_2} + (1+\beta) R_{E_2}]} \qquad (\because ic_2 = g_{m_2} V_{\pi_2} = \beta i_{b_2})$$

$$A_{V_2} = \frac{-\beta R_{C_2}}{r_{\pi_2} + (1+\beta) R_{E_2}}$$

$$A_{V_2} = \frac{-20 \times 2k}{136.054 + 21 \times 1k}$$

$$\mathbf{A_{V_2} = -1.8925}$$

**The overall voltage gain $\mathbf{A_{V_T}}$:**

$$A_{V_T} = A_{V_1} \times A_{V_2} = 0.9472 \times -1.8925$$

$$\mathbf{A_{V_T} = -1.7927}$$

**Calculation of output voltage:**

$$V_o = A_{V_T} \times V_{in} = 1.79 \times 40mV$$

$$\mathbf{V_o = 71.6mV}$$

**SIMULATED RESULTS:**

Above circuit is simulated in LTspice and results are as follows:

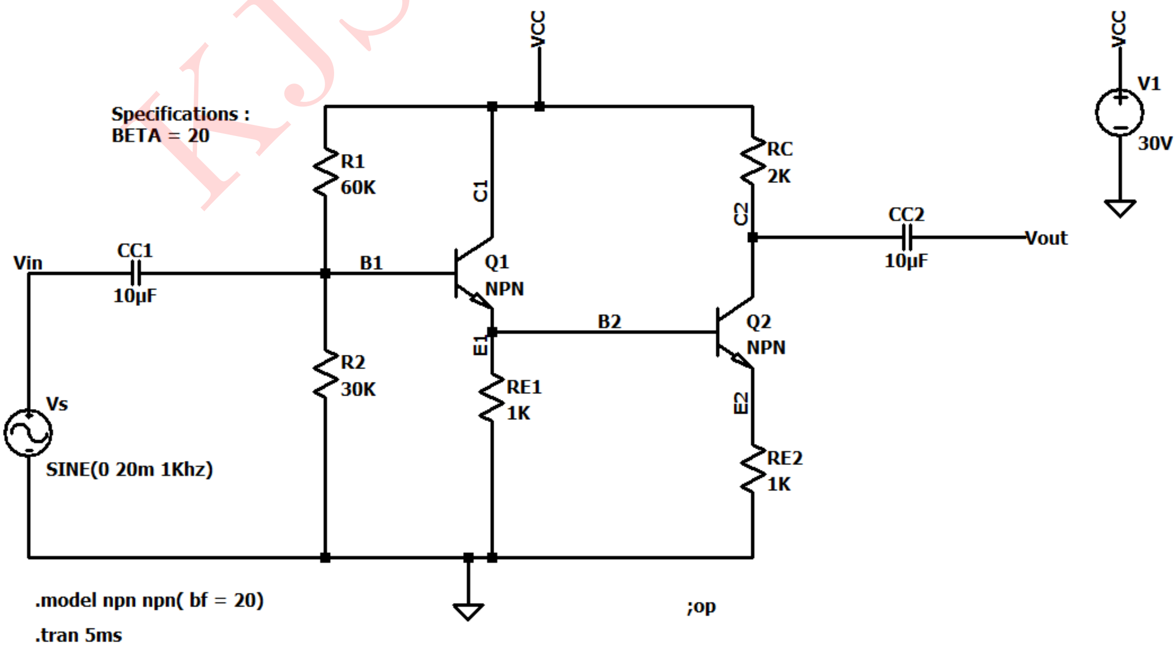


Figure 19: Circuit Schematics: Results

**Output Waveforms:**

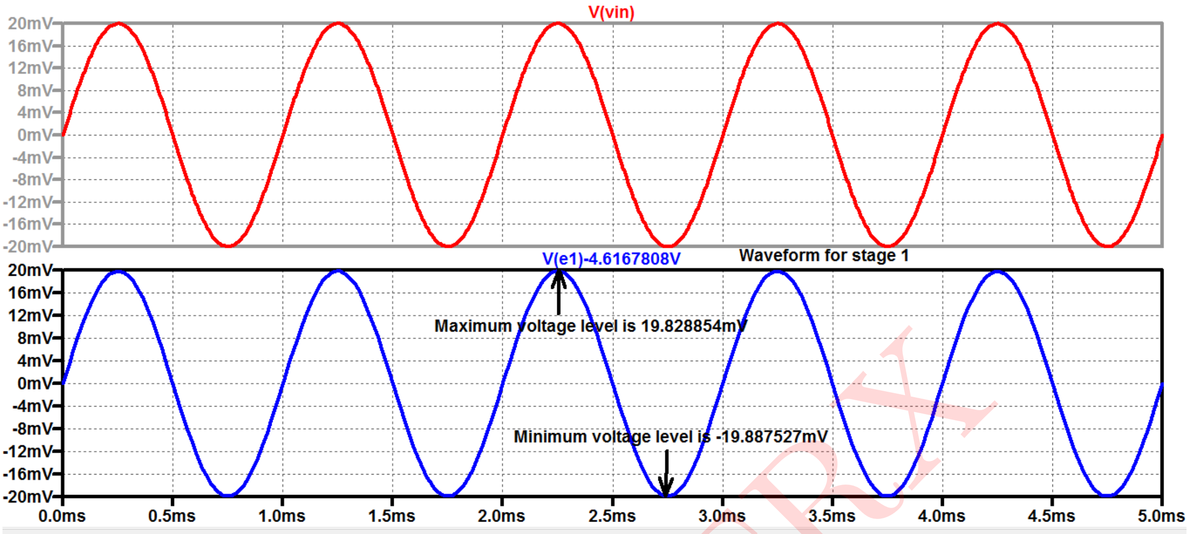


Figure 20: Input and Output Waveforms for $1^{st}$ Stage

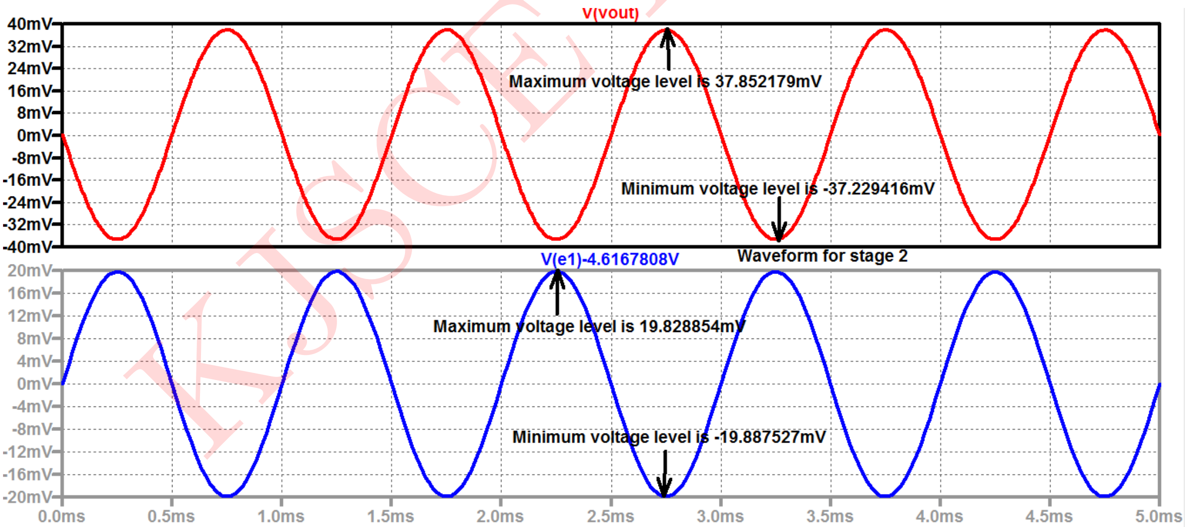


Figure 21: Input and Output Waveforms for $2^{nd}$ Stage

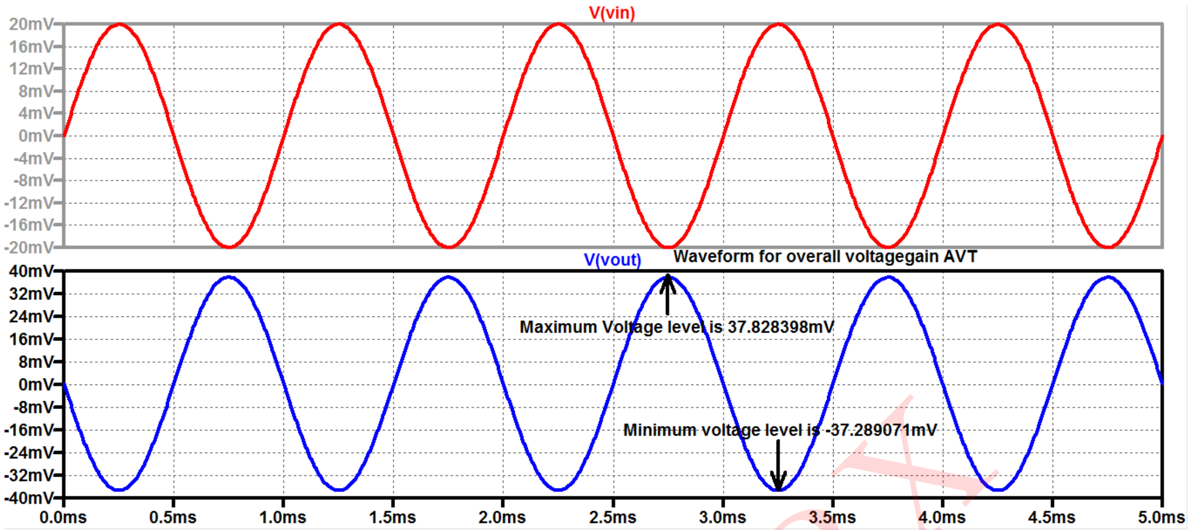


Figure 22: Input and Output Waveforms for the circuit

Comparison between theoretical and simulated values is given below:

| Parameters | Simulated Values | Theoretical Values |
|---|---|---|
| Stage-1: $I_{B_1}$ | $228.48\mu A$ | $229.27\mu A$ |
| Stage-1: $I_{C_1}$ | $4.569mA$ | $4.585mA$ |
| Stage-1: $I_{E_1}$ | $4.798mA$ | $4.814mA$ |
| Stage-1: $V_{B_1}$ | $5.43V$ | $5.414V$ |
| Stage-1: $V_{C_1}$ | $30V$ | $30V$ |
| Stage-1: $V_{E_1}$ | $4.616V$ | $4.814V$ |
| Stage-2: $I_{B_2}$ | $181.39\mu A$ | $200.67\mu A$ |
| Stage-2: $I_{C_2}$ | $3.8mA$ | $4.013mA$ |
| Stage-2: $I_{E_2}$ | $3.81mA$ | $4.214mA$ |
| Stage-2: $V_{B_2}$ | $4.616V$ | $4.814V$ |
| Stage-2: $V_{C_2}$ | $22.74V$ | $22.356V$ |
| Stage-2: $V_{E_2}$ | $3.809V$ | $4.214V$ |
| Overall voltage gain $A_{V_T}$ | $-1.877$ | $-1.79$ |
| Output voltage | $74.11mV$ | $71.6mV$ |

Table 3: Numerical 3

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