K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Diode Application

Numerical 1: For the circuit shown in figure 1, plot:

a) Input V_{in}(t) and output V_{out}(t) waveforms

b) VTC curve

Given: V_{in}(t) = $10V_{p-p}$ sinusoidal signal with frequency of 5000 Hz.

Use constant voltage model i.e. V_{D_1ON} = 0.7 V, V_B = 1 V, R_1 = 1 kΩ

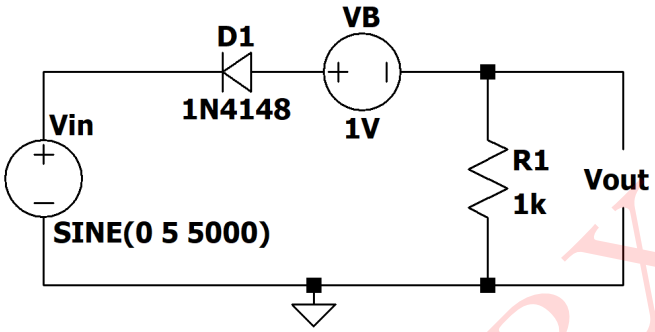

Figure 1: Circuit 1

Solution:

The given circuit 1 is a positive bias positive clipper circuit.
Assuming constant voltage model for diode D.

$\therefore V_{D_1ON}$ = **0.7 V**

The diode will be on when anode voltage will be greater than cathode voltage.

Case 1: During positive half cycle, the diode is off. But diode is on for a particular time due to bias voltage.

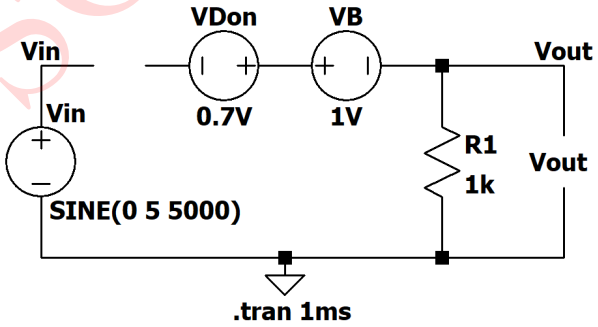

Figure 2: Diode is OFF

Applying KVL to the input loop,

$V_{in} + V_{D_1ON} - V_B - V_{out} = 0$

$V_{out} = V_{in} + V_{D_1ON} - V_B$

As the diode is off for positive half cycle, $V_{in} = 0$

$\therefore V_{out} = 0 + 0.7 - 1 =$ **−0.3 V**

This is the clipping level.

Case 2: During negative half cycle, the diode is on.

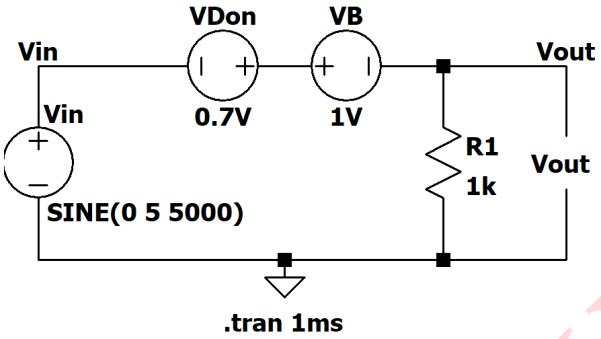

Figure 3: Diode is ON

Applying KVL to the input loop,

$V_{in} + V_{D_1ON} - V_B - V_{out} = 0$

$V_{out} = V_{in} + V_{D_1ON} - V_B$

$V_{out} = -5 + 0.7 - 1 = \mathbf{-5.3\ V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

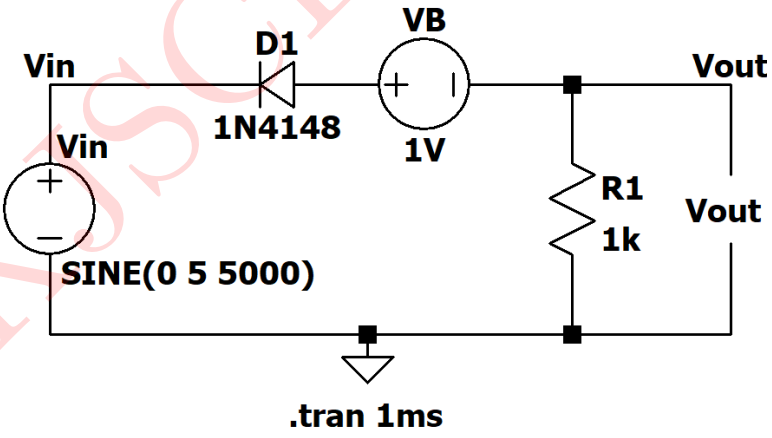

Figure 4: Circuit Schematic

The input and output waveforms are shown in figure 5.

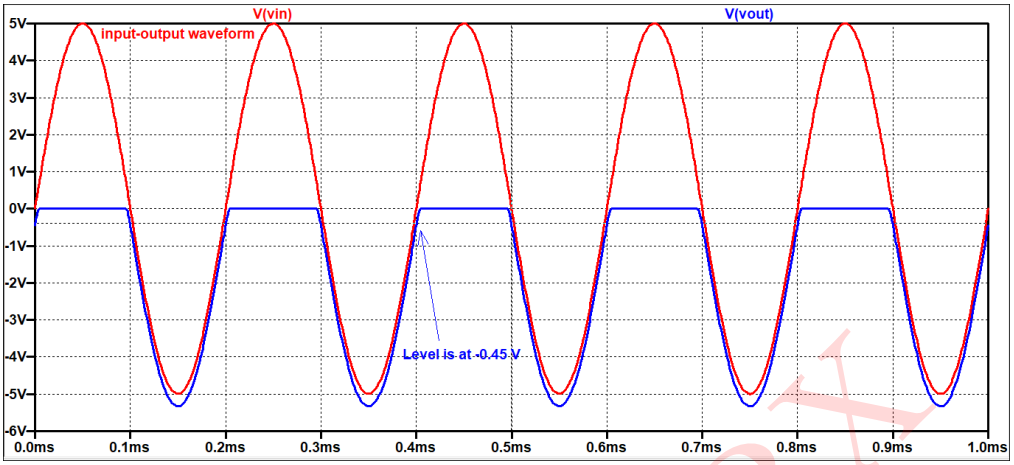

Figure 5: Input & Output waveforms

The VTC curve for the following circuit is given below in figure 6.

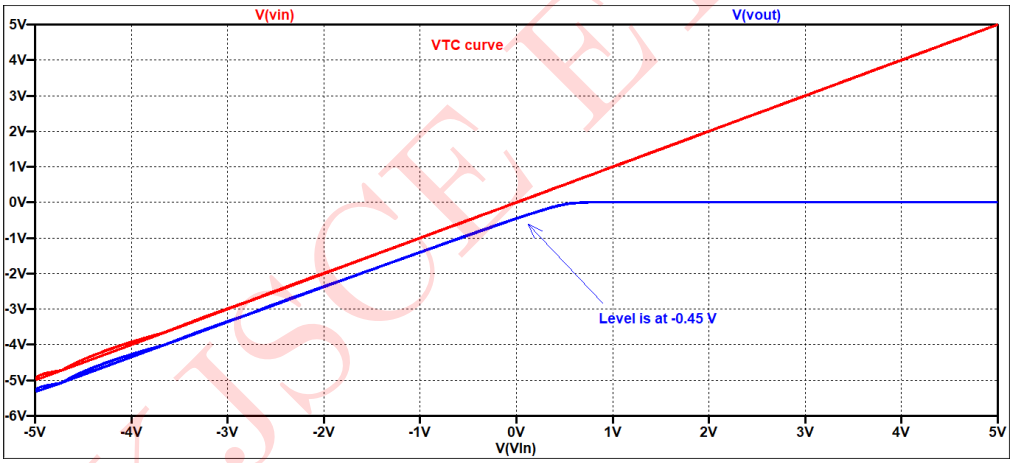

Figure 6: VTC Curve

Comparison of theoretical and simulated values:

Parameters	Theoretical Values	Simulated Values
Level of voltage clipped	-0.3 V	-0.45 V

Table 1: Numerical 1

Numerical 2: For the circuit shown in figure 7, plot:

Input V_{in}(t) and output V_{out}(t) waveforms

Given: V_{in}(t) = $40V_{p-p}$ sinusoidal signal with frequency of 1000 Hz.

For S_i diode: V_{DON} = 0.7 V

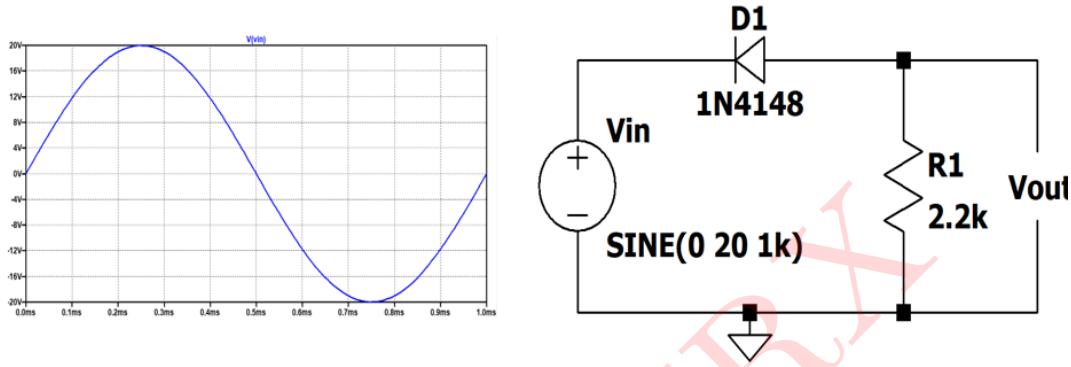

Figure 7: Circuit 2

Solution:

The given circuit 2 is a positive clipper circuit.

Case 1: During positive half cycle, the diode is OFF.

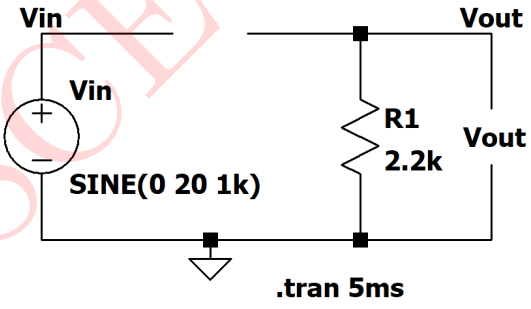

Figure 8: Diode is OFF

$\therefore V_o$ = 0 V ...(∵Diode is OFF)

This is the clipping level.

Diode will be ON when anode voltage will be greater than cathode voltage.

Case 2: During negative half cycle, the diode is ON, beyond the cathode voltage.

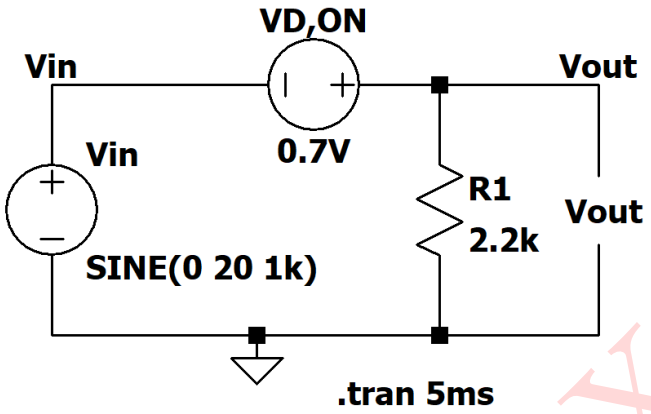

Figure 9: Diode is ON

Applying KVL to the input loop,

$V_{in} + V_{DON} - V_{out} = 0$

$V_{out} = V_{in} + V_{DON}$

$V_{out} = -20 + 0.7 = \mathbf{-19.3\ V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

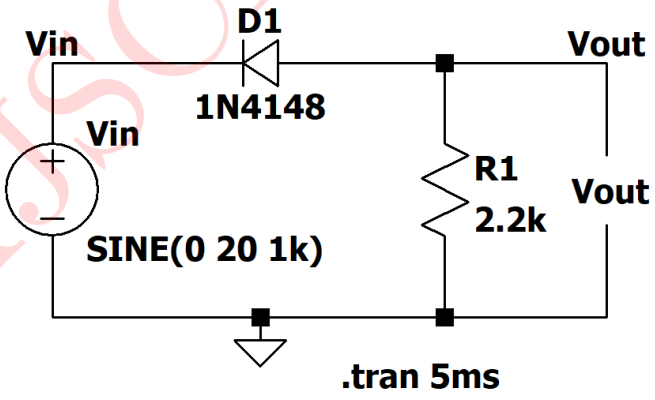

Figure 10: Circuit Schematic

The input and output waveforms are shown in figure 11.

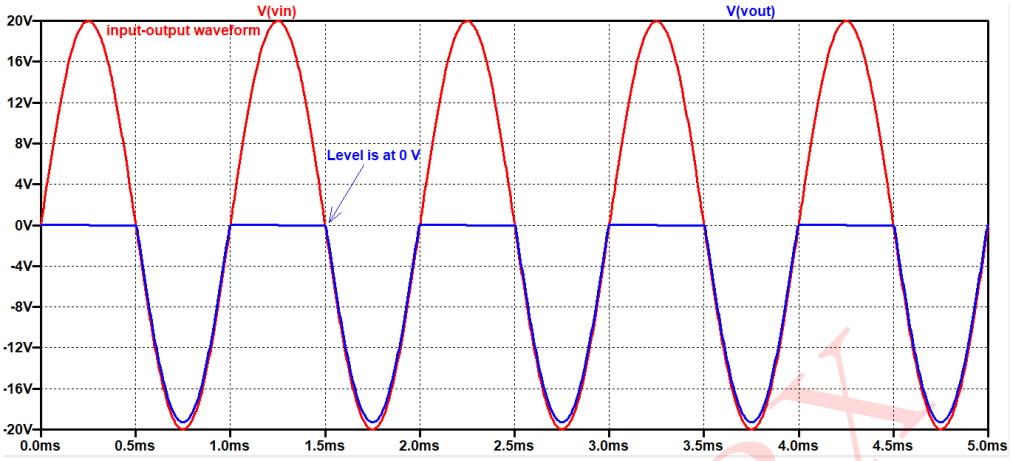

Figure 11: Input & Output waveforms

Comparison of theoretical and simulated values:

Parameters	Theoretical Values	Simulated Values
Level of outut voltage clipped	0 V	0 V

Table 2: Numerical 2

Numerical 3: For the circuit shown in figure 12, plot:

Input V_{in}(t) and output V_{out}(t) waveforms

Given: V_{in}(t) = 40 V_{p-p} square wave with frequency of 1000 Hz.

C = 10 μF, R = 10 kΩ, Diode D_1 is Si diode i.e. V_{D_1ON} = 0.7 V, V_1 = 5 V DC

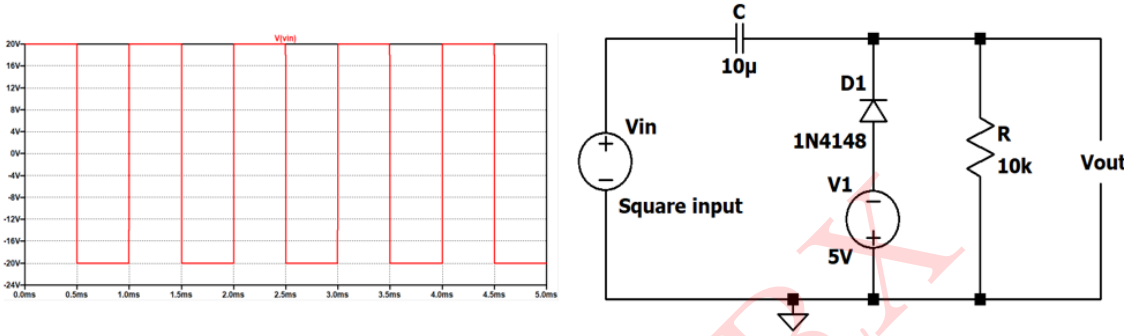

Figure 12: Circuit 3

Solution:

The given circuit 3 is a positive clamper with neagtive bias.

Since given diode is Si, V_{D_1ON} = 0.7 V

Assumption:

RC time constant is large enough to ensure that voltage across capacitor does not discharge significantly during the period diode is OFF.

Operation:

a) During negative half cycle, diode D is ON due to biasing voltage which is greater than V_{D_1ON}. The circuit becomes,

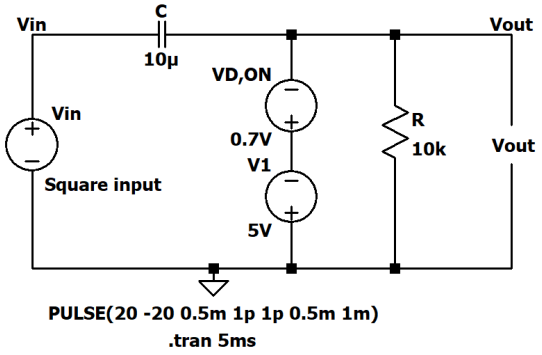

Figure 13: Diode is ON

Voltage across output will be,

$V_{out} = -V_{D_1ON} - V_1$

$V_{out} = -0.7 - 5 = -5.7$ V

At the same time, voltage across capacitor V_c charges upto $-V_{in}$.

Applying KVL to the input loop,

$V_{in} + V_C + V_{D_1ON} + V_1 = 0$

$V_C = -V_{in} - V_{D_1ON} - V_1$

$V_C = 20 - 0.7 - 5 = \mathbf{14.3\ V}$

b) During positive half cycle, diode D is OFF. The circuit becomes,

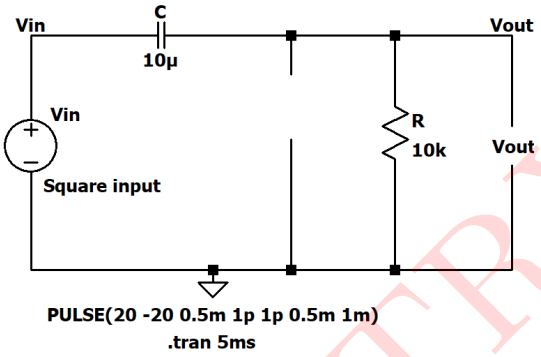

Figure 14: Diode is OFF

Note: During positive half cycle, capacitor C holds the charge $V_C = 14.3$ V and acts as a battery.

Applying KVL to the input loop,

$V_{in} + V_C - V_{out} = 0$

$V_{out} = V_{in} + V_C$

$V_{out} = 20 + 14.3 = \mathbf{34.3\ V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

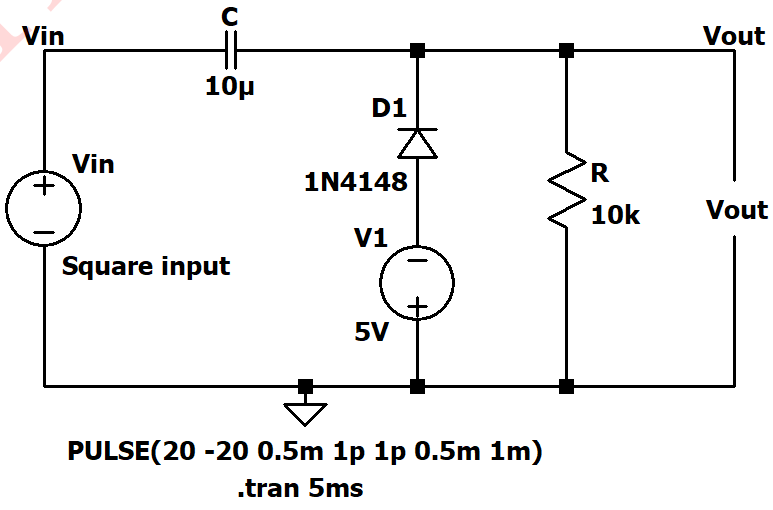

Figure 15: Circuit Schematic

The input and output waveforms are shown in figure 16.

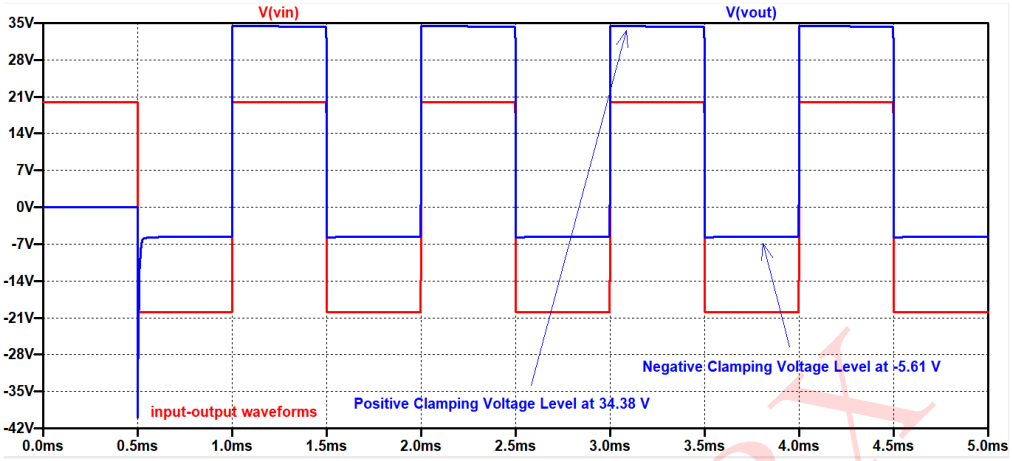

Figure 16: Input & Output waveforms

Comparison of theoretical and simulated values:

Parameters	**Theoretical Values**	**Simulated Values**
Positive Clamping Voltage	34.3 V	34.3885 V
Negative Clamping Voltage	−5.7 V	−5.6158 V

Table 3: Numerical 3

****