K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Design of single-stage Amplifier

Design 1

Design a single stage RC coupled JFET amplifier for the following $V_o = 2.5V$, $f_L \leq 20Hz$, $|A_V| \geq 10$. Calculate A_V, Z_i & Z_o of the amplifier. Select suitable transistor from datasheet. Use Mid Point Biasing technique.

Solution:

1) Data:

$|A_V| \geq 10$, $V_o = 2.5V$, $f_L \leq 20Hz$

2) Selection of JFET:

We select N-channel JFET BFW 11 from the data sheet with the following specifications:
$V_P = -2.5V$, $r_d = 50\Omega$, $I_{DSS} = 7mA$ & $g_{mo} = 5600\mu\mho$

3) Selection of biasing network

We select self bias circuit for our design

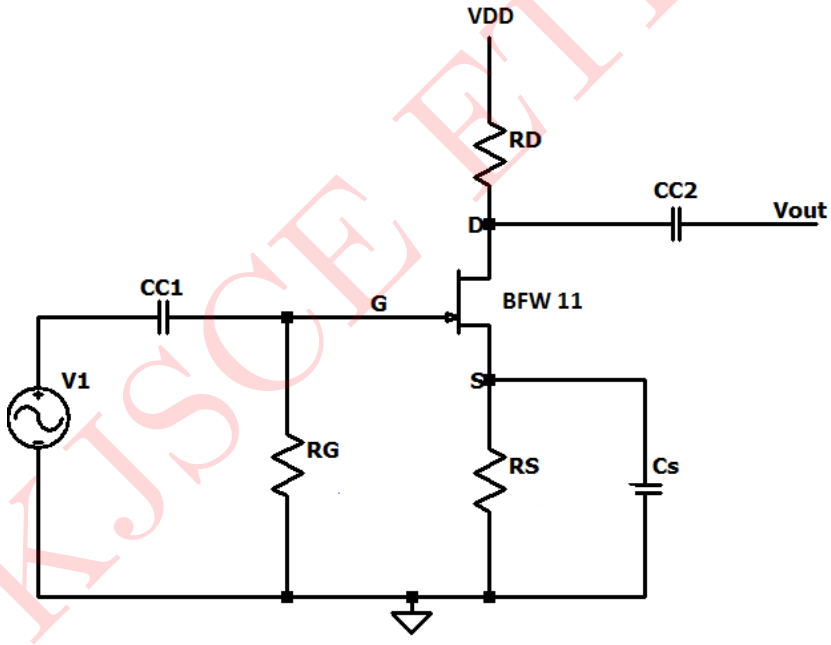

Figure 1: Circuit for Design 1

4) Selection of Q-Point:

i) Calculation of I_D

For mid point biasing, $I_D = \dfrac{I_{DSS}}{2}$

i.e. $I_D = \dfrac{7mA}{2}$

$\therefore \mathbf{I_D = 3.5mA}$

ii) Calculation of V_{GS}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

i.e. $V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) = -2.5\left(1 - \sqrt{\frac{3.5}{7}}\right)$

$\mathbf{V_{GS} = -0.732V}$

iii) Calculation of g_m

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = 5600 \times 10^{-6}\left(1 - \frac{(-0.732)}{(-2.5)}\right)$$

$\therefore \mathbf{g_m = 3.96m\mho}$

5) Calculation of R_S:

For self-bias,

$V_{GS} = -I_D R_s$

$$R_S = \frac{-V_{GS}}{I_D} = \frac{-(-0.732)}{3.5mA}$$

$\therefore R_S = 209\Omega$

Select $\mathbf{R_S = 220\Omega_{(std)}, 1/4W}$.....(HSV)

6) Selection of R_D:

$A_V = -g_m(r_d \parallel R_D)$

$$-10 = -3.96 \times 10^{-3}(50k \parallel R_D) = -3.96 \times 10^{-3}\left(\frac{50k\Omega \times R_D}{50k\Omega + R_D}\right)$$

Solving the above equation we get,

$\therefore R_D = 2.67k\Omega$

Select $\mathbf{R_D = 2.7k\Omega_{(std)}, 1/4W}$.....(HSV)

7) Selection of R_G:

Select $\mathbf{R_G = 1M\Omega_{(std)}, 1/4W}$

8) Selection of V_{DD}:

$V_{DS} \geq V_{o_{peak}} + \mid V_P \mid$.....(Condition for undistorted output)

$V_{DS} = 1.5(V_{o_{peak}} + \mid V_p \mid)$

$V_{DS} = 1.5(V_{o_{peak}} + 2.5)$

The value is multiplied by 1.5 to take care of saturation voltages, tolerance in resistance value, variation in supply voltage and device parameter variation.

$V_{o_{rms}} = 2.5V$

$\therefore V_{o_{peak}} = 2.5\sqrt{2}$

i.e. $V_{DS} = 1.5(2.5\sqrt{2} + 2.5) = 9.045V$

Select $\mathbf{V_{DS}} = \mathbf{9V}$

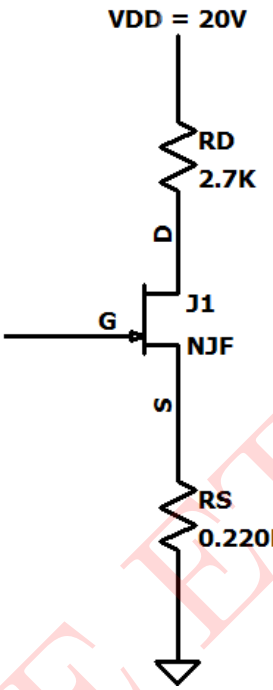

Figure 2: JFET Circuit D-S loop

Applying KVL to the D-S loop shown in figure 2 we get,

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$V_{DD} = V_{DS} + I_D(R_D + R_S)$

$V_{DD} = 9 + 3.5 \times 10^{-3}(2.7k + 220)$

$\therefore V_{DD} = 19.22V$

Select $\mathbf{V_{DD}} = \mathbf{20V}$

9) Selection of $\mathbf{C_S}$:

$f_L = 20Hz$

$X_{C_S} \leq 0.1R_S$

i.e. $\dfrac{1}{2\pi f_L C_S} \leq 0.1R_S$

i.e. $C_S \geq \dfrac{1}{2\pi f_L \times 0.1R_S} \geq \dfrac{1}{2\pi \times 20 \times 0.1 \times 220}$

$\therefore C_S \geq 361.715\mu F$

Select $\mathbf{C_S} = \mathbf{390\mu F/25V}$.....(H.S.V)

10) Selection of C_{C1}:

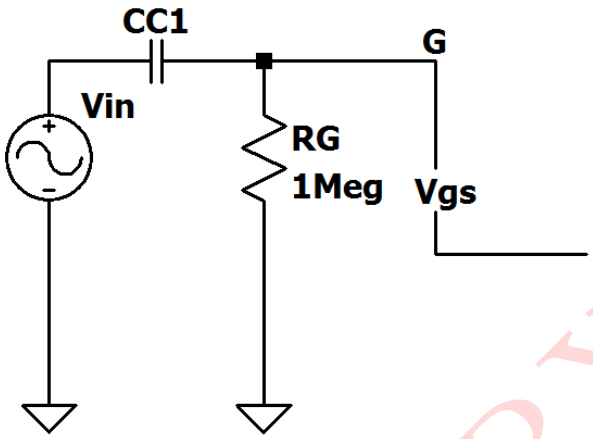

Figure 3: JFET Small Signal Equivalent Input Circuit

$$C_{C1} = \frac{1}{2\pi f_{L_{CC1}} R_{eq}}$$

$$f_{C_{C1}} = f_L = 20Hz$$

$$R_{eq} = R_G = 1M\Omega$$

$$C_{C1} = \frac{1}{2\pi \times 20 \times 1M\Omega} = 7.957nF$$

Select C_{C1} = 8.2nF/25V....(H.S.V)

11) Selection of C_{C2}:

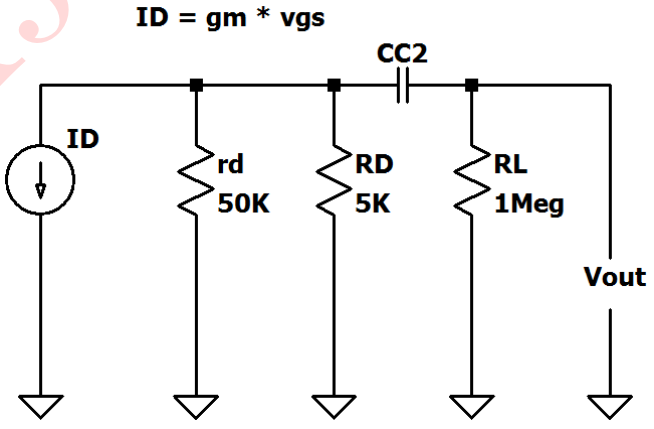

Figure 4: JFET Small Signal Equivalent Output Circuit

$$C_{C2} = \frac{1}{2\pi f_{L_{CC2}} R_{eq}}$$

$$f_{L_{CC2}} = f_L = 20Hz$$

$$R_{eq} = r_d || R_D + R_L$$

If R_L is not given,

Select $R_L = R_i(nextstage)$

$R_L = R_G = 1M\Omega$

$R_{eq} = 50k||2.7k + 1M\Omega$

$R_{eq} = 2.562k + 1M\Omega = 1.00256M\Omega$

$$C_{C2} = \frac{1}{2\pi \times 20 \times 1.00256M\Omega}$$

$C_{C2} = 7.937nF$

Select C_{C2} = 8.2nF/25V.....(H.S.V)

12) Designed circuit:

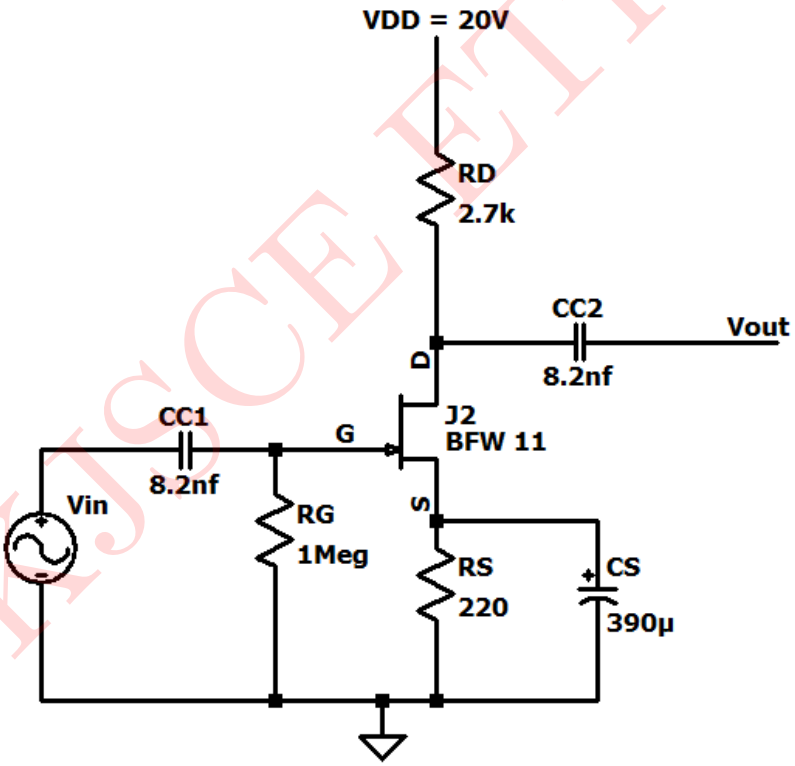

Figure 5: Designed JFET Amplifier Circuit using Mid-Point Biasing Technique

AC Analysis:

The small signal equivalent circuit is shown in figure 6

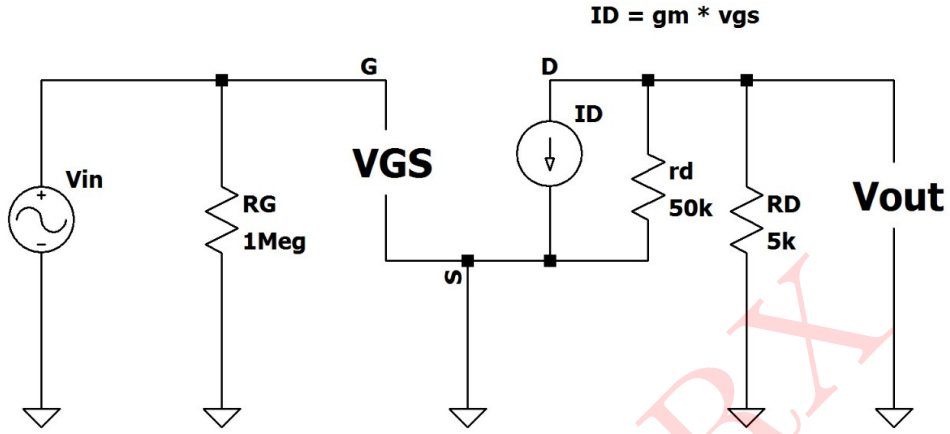

Figure 6: Small Signal Equivalent Circuit

Calculation of voltage gain (A_V)

$A_V = -g_m(R_D \parallel r_d) = -3.96 \times 10^{-3} \times (2.7k \parallel 50k)$

$\therefore \mathbf{A_V = -10.15}$

Calculation of Z_i & Z_o

From figure 2 we get,

$Z_i = R_G$

$\mathbf{Z_i = 1M\Omega}$

$Z_o = r_d \parallel R_D = 50k \parallel 2.7k$

$\mathbf{Z_o = 2.56k\Omega}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

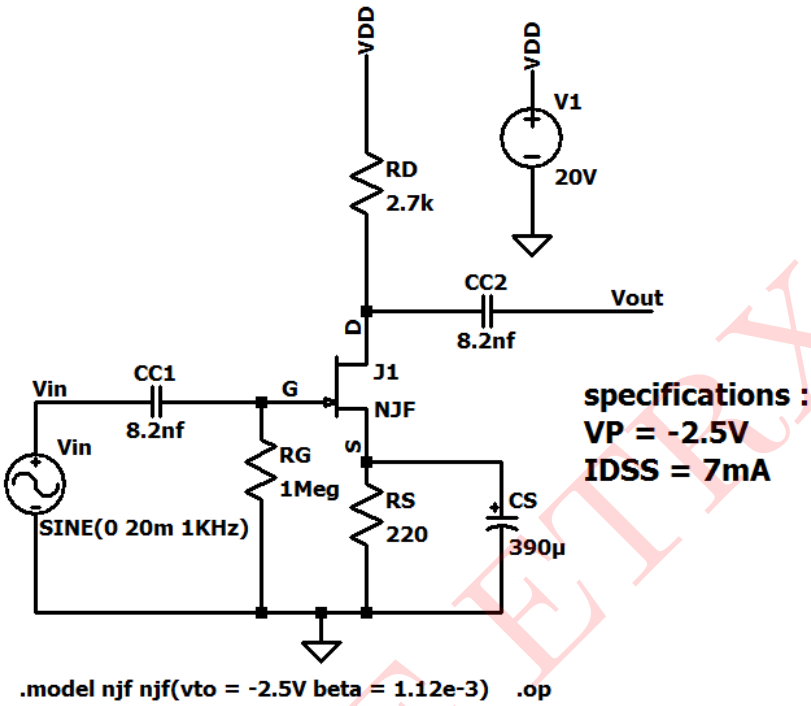

Figure 7: Circuit Schematic: Results

The input and output waveforms are shown in figure 4

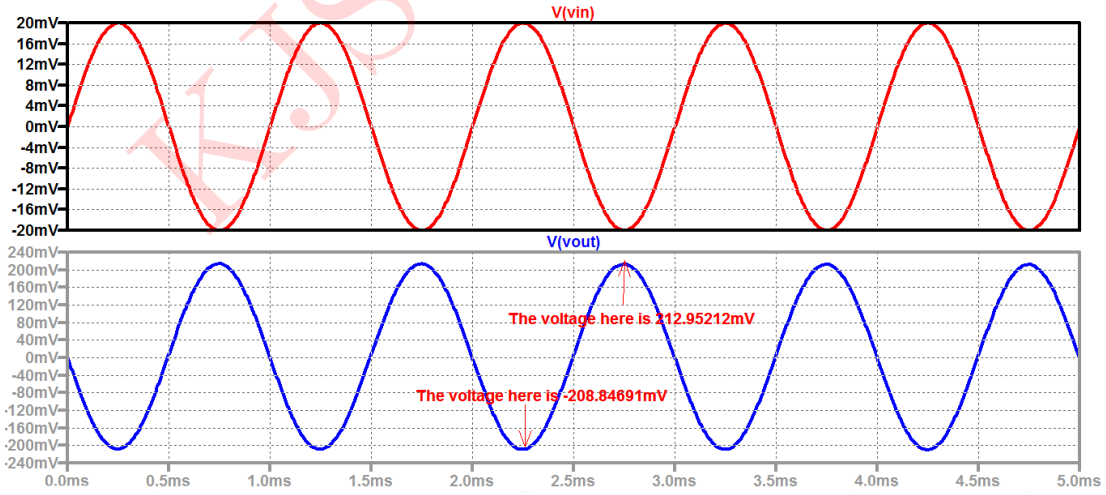

Figure 8: Input and Output Waveforms

Comparison between theoretical and simulated values is given below:

Parameters	**Simulated Values**	**Theoretical Values**
I_{DQ}	$3.4mA$	$3.5mA$
A_V	> -10	-10.15

Table 1: Design 1

****