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ELECTRONIC CIRCUITS
Design of Single-stage Amplifier

11^{th} **July, 2020**

Design 1:
Design a single stage RC coupled JFET amplifier for following specifications:
$V_o = 2V$, $f_L \leq 20Hz$, $\mid A_V \mid \geq 10$, $R_i \geq 1M\Omega$. Use mid-point biasing technique.
Calculate A_V, R_i and R_o of the amplifier circuit designed.

Solution:
1. Data: $V_o = 2V$, $f_L \leq 20Hz$, $\mid A_V \mid \geq 10$

2. Selection of transistor: We select N-channel JFET BFW11 from the datasheet which has the following specifications:

$g_m = 5600\mu A/V$, $V_P = -2.5V$, $r_d = 50k\Omega$, $I_{DSS} = 7mA$

3. Selection of Biasing network: Self-bias circuit is selected to give mid-band biasing. In this way, as the input swings negative and positive, we get maximum range of operation.

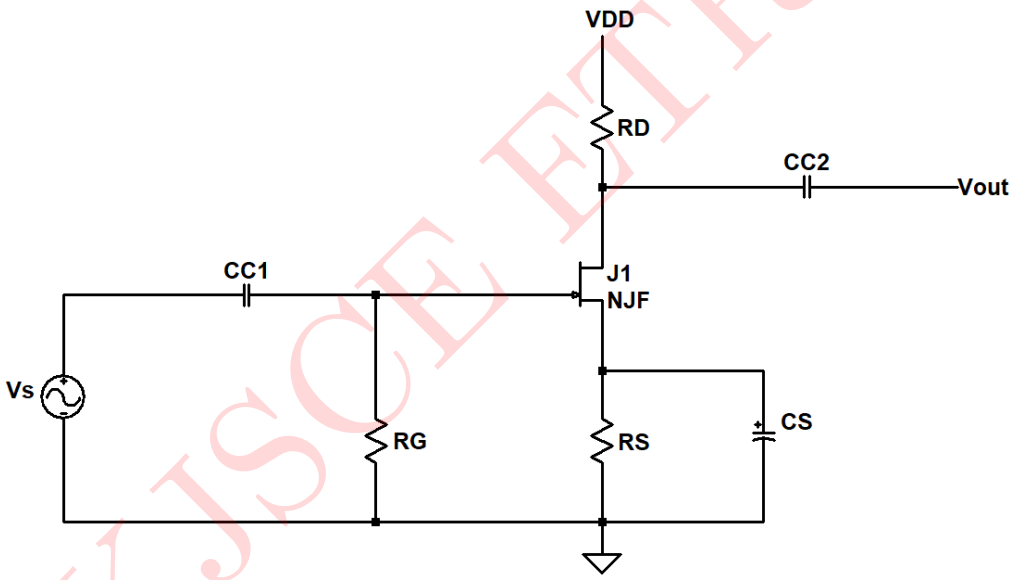

Figure 1: Circuit 1

4. Selection of Q-point ($\mathbf{V_{DS}}, \mathbf{I_D}$) :
i. For mid-point biasing:

$$I_D = \frac{I_{DSS}}{2}$$

$$\therefore I_D = \frac{7mA}{2} = 3.5\text{mA}$$

ii. In saturation region:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \quad \text{...for N-channel JFET}$$

$$\therefore V_{GS} = V_P \left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right] = -2.5\left[1 - \sqrt{\frac{1}{2}}\right] = -2.5(0.2929)$$

$$\therefore V_{GS} = -0.7322V$$

iii. $$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right] = 5600 \times 10^{-6}\left[1 - \frac{(-0.7322)}{(-2.5)}\right]$$

$$\therefore g_m = 3.960m\mho$$

5. Selection of $\mathbf{R_S}$:
For self bias of N-channel JFET:

$$V_{GS} = -I_D R_S$$

$$\therefore R_S = \frac{-V_{GS}}{I_D} = \frac{-(-0.7322)}{3.5mA}$$

$$\therefore R_S = 209\Omega$$

Selecting higher standard value for R_S, we get: $R_S = 220\Omega$, 0.25W

6. Selection of $\mathbf{R_D}$:

$$A_V = -g_m(r_d \parallel R_D)$$

$$\therefore -10 = -3.960 \times 10^{-3}\left[\frac{50k\Omega \times R_D}{50k\Omega + R_D}\right]$$

$$\therefore \frac{25.2525}{50 \times 10^3} = \frac{R_D}{50k\Omega + R_D}$$

$$\therefore (0.5051)(50k\Omega + R_D) = R_D$$

$$\therefore 25.2525 + 0.5051(R_D) = R_D$$

$$\therefore 25.2525 = 0.9494R_D$$

$$\therefore R_D = 2.6595k\Omega$$

We select $R_D = 2.7k\Omega$, 0.25W

7. Selection of $\mathbf{R_G}$: Select $R_G = 1\text{M}\Omega$, 0.25W

8. Selection of $\mathbf{V_{DD}}$: $V_{DS} \geq 1.5\ (V_{o_{peak}} + \mid V_P \mid)$

Since $V_D = 2V$ then $V_{o_{opeak}} = 2\sqrt{2}$ V

The value is multiplied by 1.5 to take care of the saturation voltages, variation in resistance, variation in supply voltage and device parameter variation.

$\therefore V_{DS} = 1.5(2\sqrt{2} + 2.5) = 1.5(5.3284)$

$\therefore V_{DS} = 8V$

Applying KVL to D-S loop:

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$\therefore V_{DD} - I_D(R_D + R_S) = V_{DS}$

$\therefore V_{DD} = V_{DS} + I_D(R_D + R_S)$

$\therefore V_{DD} = 8 + (3.5mA)(2.7k\Omega + 220\Omega)$

$\therefore V_{DD} = 20\text{V}$

9. Selection of C_S:

We know, $X_{C_S} \leq 0.1R_S$

$$\therefore \frac{1}{2\pi f_{L_{CS}} C_S} \leq 0.1R_S$$

$$\therefore C_S \geq \frac{1}{2\pi f_{L_{CS}}(0.1R_S)}$$

$$\therefore C_S \geq \frac{1}{2\pi \times 20 \times 0.1(220)} \quad \ldots f_{L_{CS}} = f_L = 20Hz$$

$\therefore C_S \geq 361.715\mu F$

Selecting higher standard value, $C_S = 390\mu F/25$ V

10. Selection of C_{C1}:

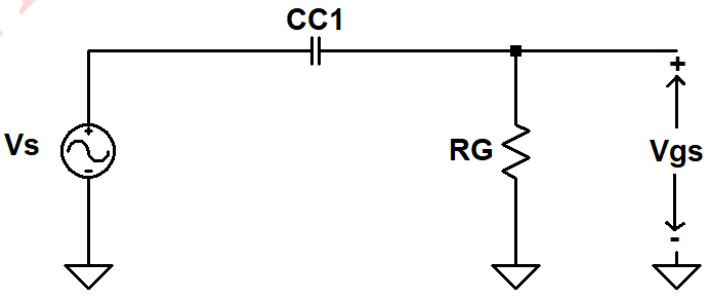

Figure 2: Small Signal low frequency equivalent circuit for C_{C1}

$$C_{C1} = \frac{1}{2\pi f_{L_{CC1}} R_{eq}} \quad \ldots(R_{eq} = R_G)$$

$$\therefore C_{C1} = \frac{1}{2\pi \times 20 \times 1M\Omega} \quad \ldots(f_{L_{CC1}} = f_L = 20Hz \ \& \ R_G = 1M\Omega)$$

$\therefore C_{C1} = 7.9577\text{nF}$

Selecting higher standard value,

$C_{C1} = 8.2\text{nF}/25\text{V}$

Selection of C_{C2}:

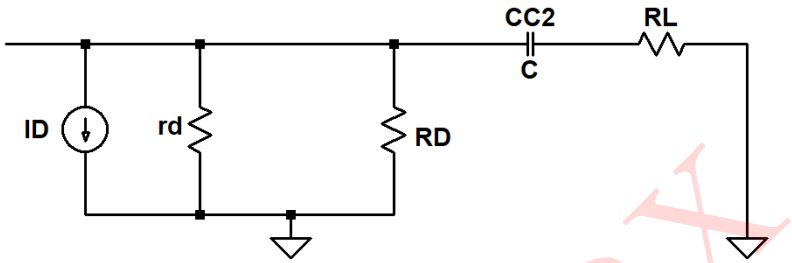

Figure 3: Small Signal low frequency equivalent circuit for C_{C2}

$$C_{C2} = \frac{1}{2\pi f_{L_{CC2}} R_{eq}} \quad ...(f_{L_{CC2}} = f_L = 20Hz)$$

$$R_{eq} = r_d \parallel R_D + R_L \quad ...(R_L = R_G = 1M\Omega)$$

$$R_{eq} = (50k\Omega \parallel 2.7k\Omega) + 1M\Omega$$

$$\therefore R_{eq} \approx 1M\Omega$$

$$\therefore C_{C2} = \frac{1}{2\pi \times 1M\Omega \times 20} = 7.9577\text{nF}$$

Selecting a higher standard value,

$C_{C2} = 8.2\text{nF}/25\text{V}$

The designed circuit is shown in figure 4:

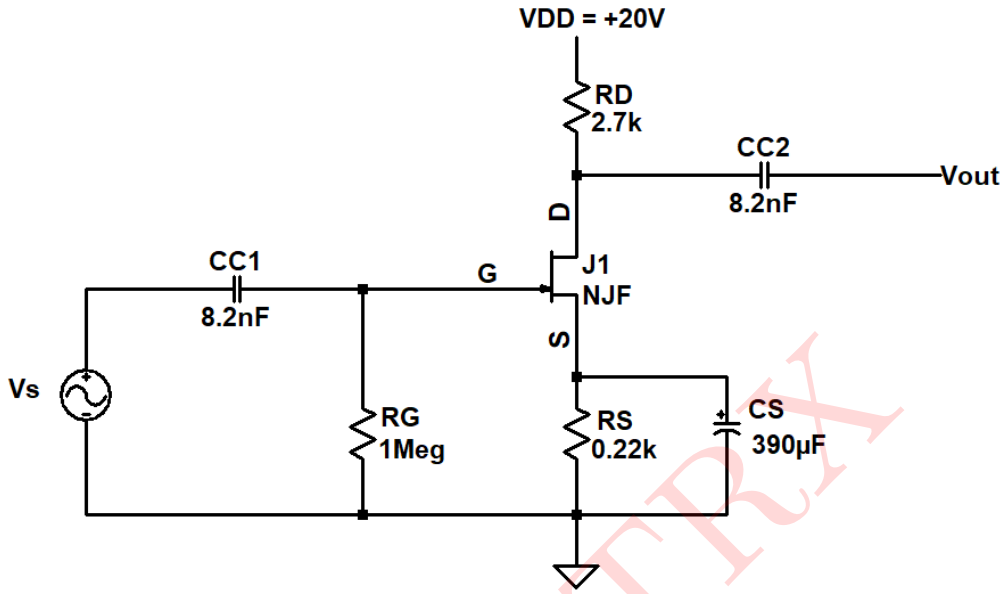

Figure 4: Designed circuit

A single stage common source N-channel JFET amplifier using mid-point biasing techniques is designed.

Small signal equivalent circuit is shown in figure 5:

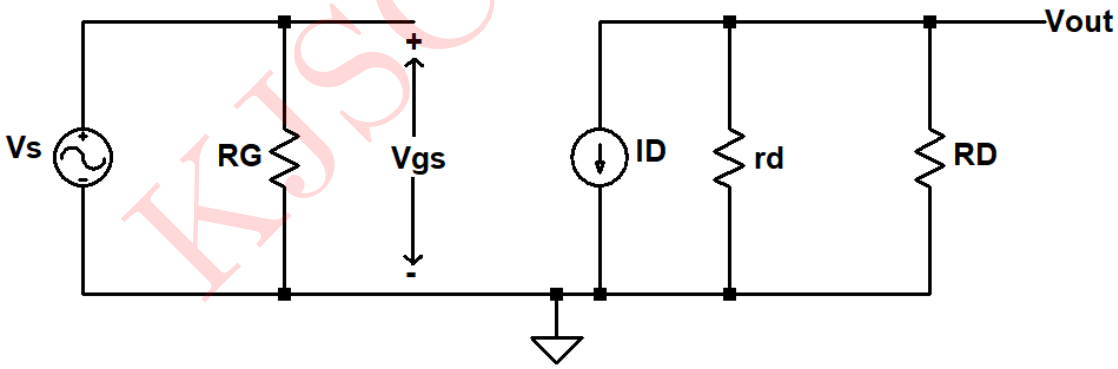

Figure 5: Small signal equivalent circuit

$I_D = g_m V_{GS}$

i. R_i (Input Resistance):

Here, $R_i = R_G = 1M\Omega$

$\therefore \mathbf{R_i = 1M\Omega}$

ii. R_o (Output Resistance):

$R_o = r_d \parallel R_D = 50k\Omega \parallel 2.7k\Omega = \mathbf{2.5617k\Omega}$

iii. A_V (Voltage gain):

$$A_V = \frac{V_{out}}{V_S}$$

$$V_{out} = -g_m V_{GS}(R_D \parallel r_d)$$

$$A_V = \frac{-g_m V_{GS}(R_D \parallel r_d)}{V_{GS}} \qquad ...(\because V_S = V_{GS})$$

$$\therefore A_V = -g_m(R_D \parallel r_d)$$

$$\therefore A_V = -(3.960 \times 10^{-3})(2.7k\Omega \parallel 50k\Omega)$$

$$\therefore \mathbf{A_V = -10.1443}$$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

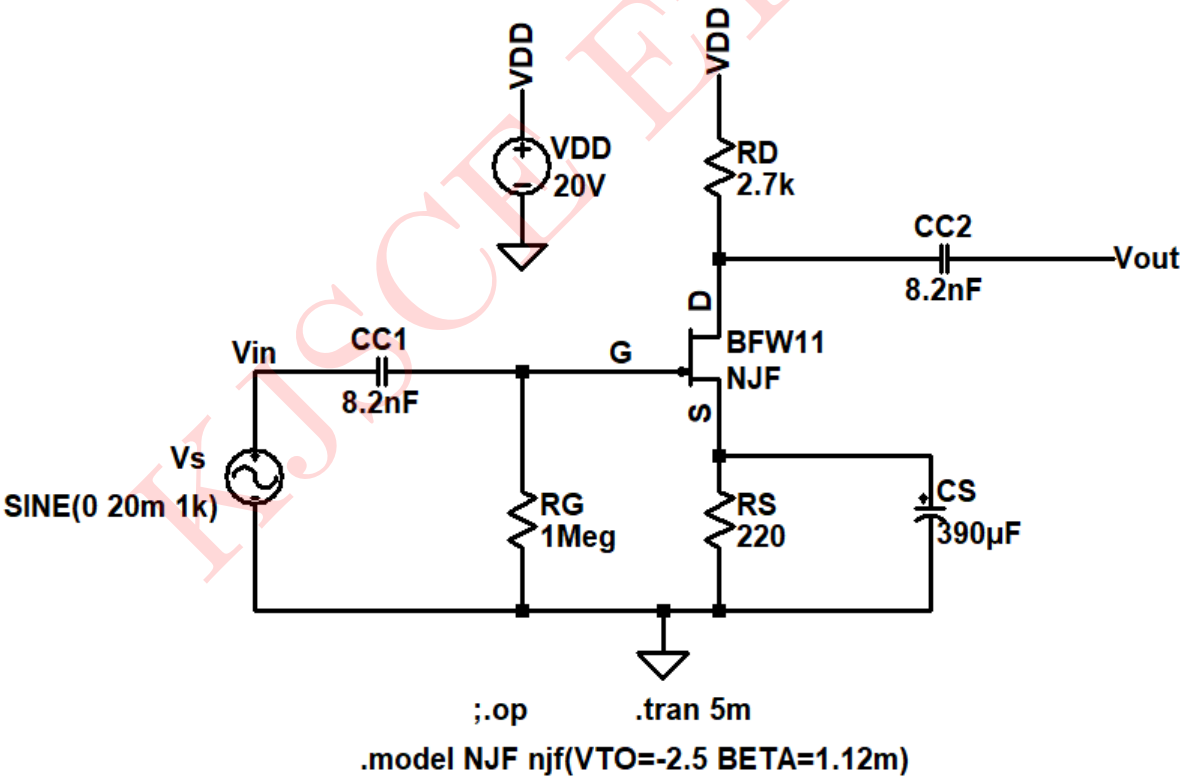

Figure 6: Circuit Schematic: Results

The input and output waveform is shown in figure 7:

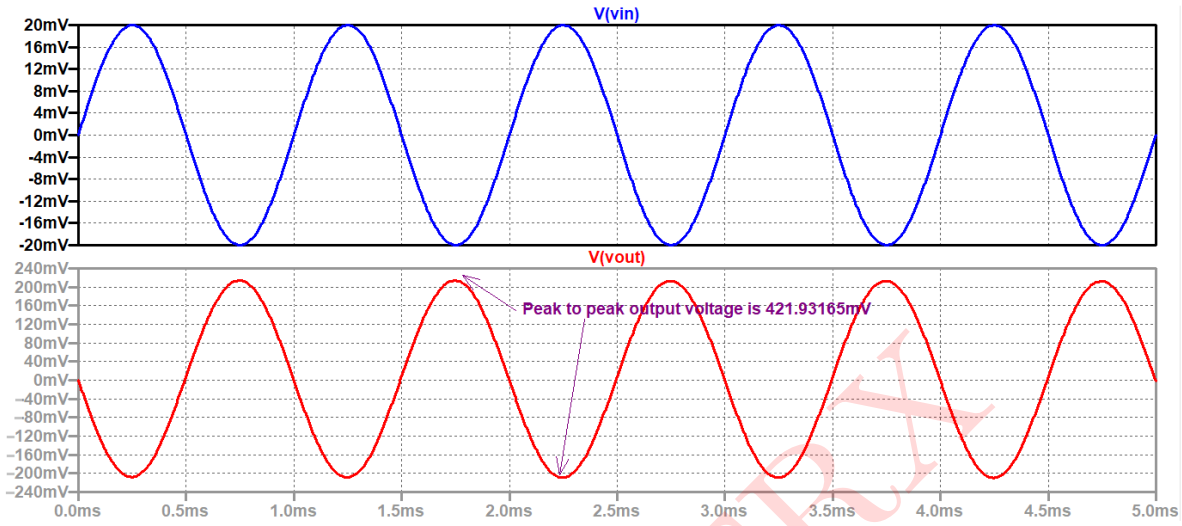

Figure 7: Input and output waveform

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
I_{DQ}	3.5mA	3.4204mA
A_V	> -10.14	-10.5

Table 1: Design 1