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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Design of single-stage Amplifier

Design 1: Design a single stage RC coupled BJT amplifier for following specifications: $V_o = 3$ V, $V_{CC} = 18$ V, $f_L \leq 20$ Hz, S ≤ 10, $|A_V| \geq 180$
Calculate A_V, Z_i & Z_o of the amplifier designed.

Solution:

Step 1: Data

$V_o = 3$ V, $V_{CC} = 18$ V, $f_L \leq 20$ Hz, S ≤ 10, $|A_V| \geq 180$

Step 2: Selection of transistor

Transistor selected is BC 147A with following specifications:

$h_{FE(max)} = 220$, $h_{ie} = 2.7$ kΩ, $h_{fe(min)} = 125$

Step 3: Selection of biasing network

Voltage divider biasing network is selected to keep Q point independent of variation in β and temperature.

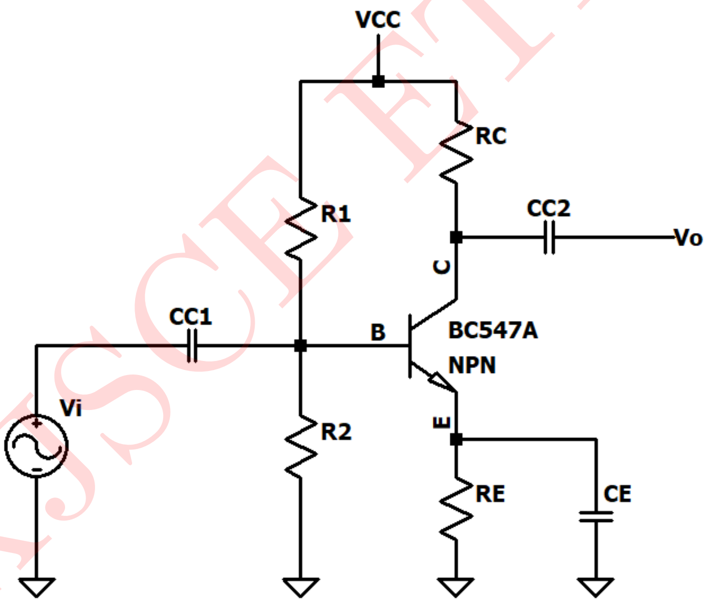

Figure 1: Circuit 1

Step 4: Selection of R_C

$$|A_V| = \frac{h_{fe(min)} R_C}{h_{ie}}$$

$$180 = \frac{125 \times R_C}{2.7 \times 10^3} = 3.888 \text{ k}\Omega$$

Selecting higher standard value of R_C to increase the gain.

$R_C =$ **3.19 kΩ, 1/4 W**

Step 5: Selection of Q point ($\mathbf{V_{CE}}$ & $\mathbf{I_C}$)

$V_{o\ peak} = \sqrt{2}V_o$

$V_{o\ peak} = \sqrt{2} \times 3$

$V_{o\ peak} = \mathbf{4.24\ V}$

$V_{CE} = 1.5\ (V_{o\ peak} + V_{CE}\ sat)$

The value is multiplied by 1.5 to take care of saturation voltages, variation in resistance variation is supply voltage and device parameter variation.

$V_{CE} = 1.5(4.24 + 0.25) = \mathbf{6.735\ V}$

We know, $I_{o\ peak} = \dfrac{V_{o\ peak}}{R_C}$

$I_{o\ peak} = \dfrac{3 \times \sqrt{2}}{2.7 \times 10^3} = \mathbf{1.571\ mA}$

$I_C \geq I_{o\ peak}$ (for undistorted output signal)

$I_C \geq 1.571\ \text{mA} = \mathbf{1.6\ mA}$

Step 6: Selection of $\mathbf{R_E}$

V_{RE} should be 10% of V_{CC}

$V_{RE} = \dfrac{V_{CC}}{10}$

$V_{RE} = \dfrac{18}{10} = \mathbf{1.8\ V}$

We know, $R_E = \dfrac{V_{RE}}{I_E}$

$$R_E = \frac{1.8}{1.6 \times 10^{-3}} = 1.125\ \text{k}\Omega \qquad ...(\because I_C \simeq I_E)$$

Selection lower standard value of R_E to improve stability.

$R_E = \mathbf{1.1\ k\Omega,\ 1/4\ W}$

Step 7: Selection of $\mathbf{R_1}$ & $\mathbf{R_2}$

$$\text{S} = \frac{1 + h_{FE\,(typ)}}{1 + h_{FE\,(typ)}\left(\dfrac{R_E}{R_B + R_E}\right)}$$

$$10 = \frac{1 + 220}{1 + 220\left(\dfrac{1.1 \times 10^3}{R_B + 1.1 \times 10^3}\right)}$$

$R_B = \mathbf{10.478\ k\Omega}$

$$R_B = \frac{R_1 \times R_2}{R_1 + R_2} \qquad ...(1)$$

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} \qquad ...(2)$$

Applying KVL to input B-E loop we get,

$V_B - I_B R_B - V_{BE} - I_E R_E = 0$

$V_B = \frac{I_C}{\beta} R_B + V_{BE} + V_{RE}$

$V_B = \frac{1.6 \times 10^{-3}}{220} \times 10.478 \times 10^3 + 0.7 + 1.8 = \mathbf{2.576\ V}$

$\frac{V_B}{V_{CC}} = \frac{R_2}{R_1 + R_2}$ ...(From 2)

$\frac{R_2}{R_1 + R_2} = 0.1431$ ...(3)

Substituting in equation 1,

$R_3 = R_1 \left(\frac{R_2}{R_1 + R_2} \right)$

$10.478 \times 10^3 = R_1 \times 0.1431 = 73.22\ \text{k}\Omega$

Selecting higher standard value for R_1, so that the circuit draws minimum current.

$R_1 = \mathbf{75\ k\Omega,\ 1/4\ W}$

$\frac{R_2}{R_1 + R_2} = 0.1431$ ...(From 3)

$\frac{R_2}{75 \times 10^3 + R_2} = 0.1431$

$R_2 = 0.1431 R_2 + 10.7325 \times 10^3$

$0.8569 R_2 = 10.7325 \times 10^3$

$R_2 = \frac{10.7325 \times 10^3}{0.8569} = 12.52\ \text{k}\Omega$

Selecting lower standard value for R_2,

$R_2 = \mathbf{12\ k\Omega,\ 1/4\ W}$

Step 8: Selection of coupling capacitors ($\mathbf{C_{C1}}$ & $\mathbf{C_{C2}}$)

a) C_{C1}

$C_{C1} = \frac{1}{2\pi R_{eq} f_L}$

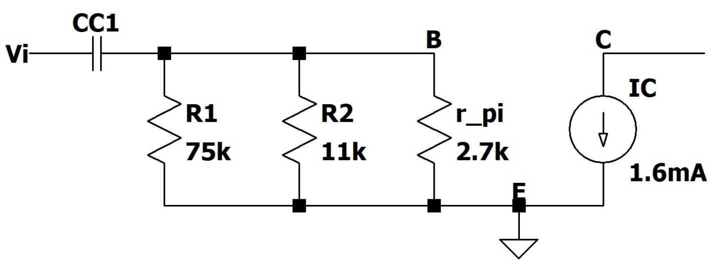

Figure 2: Small Signal Low Frequency Equivalent circuit for C_{C1}

$R_{eq} = R_1 \ || \ R_2 \ || \ h_{ie}$

$R_{eq} = 75 \times 10^3 \ || \ 12 \times 10^3 \ || \ 2.7 \times 10^3 = \mathbf{2.14\ k\Omega}$

$C_{C1} = \dfrac{1}{2\pi \times 2.14 \times 10^3 \times 20} = 3.71\ \mu\text{F}$

Selecting higher standard value for C_{C1},

$C_{C1} = \mathbf{4.7\ \mu F,\ 25\ V}$

b) C_{C2}

$C_{C2} = \dfrac{1}{2\pi R_{eq} f_L}$

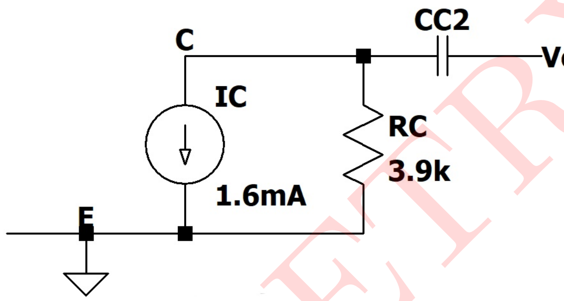

Figure 3: Small Signal Low Frequency Equivalent circuit for C_{C2}

$R_{eq} = R_C = 3.9\ \text{k}\Omega$

$C_{C2} = \dfrac{1}{2\pi \times 3.9 \times 10^3 \times 20} = 2.04\ \mu\text{F}$

Selecting higher standard value for C_{C2},

$C_{C2} = \mathbf{2.2\ \mu F,\ 25\ V}$

Step 9: Selection of bypass capacitor $\mathbf{C_E}$

To ensure complete bypass of R_E,

$X_{CE} < R_E$

$X_{CE} = \dfrac{R_E}{10}$

$X_{CE} = 0.1 \times R_E$

$X_{CE} = 0.1 \times 1.1 \times 10^3 = \mathbf{110\ \Omega}$

$C_E = \dfrac{1}{2\pi F_L X_{CE}}$

$C_E = \dfrac{1}{2\pi F_L \times 0.1 \times R_E}$

$C_E = \dfrac{1}{2\pi \times 20 \times 110} = \mathbf{72.34\ \mu F}$

Selecting higher standard value for C_E,

$C_E = \mathbf{75\ \mu F,\ 25\ V}$

Step 10: Redraw designed circuit

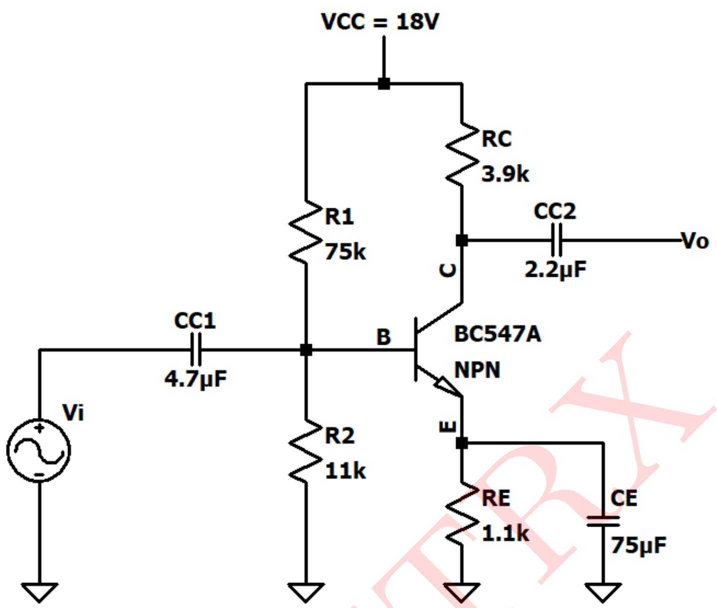

Figure 4: Designed Circuit

AC Analysis:

$g_m = \dfrac{I_C}{V_T}$

$g_m = \dfrac{1.6 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{61.538\ mA/V}$

$r_\pi = h_{ie} = \mathbf{2.7\ k\Omega}$

Small signal equivalent circuit:

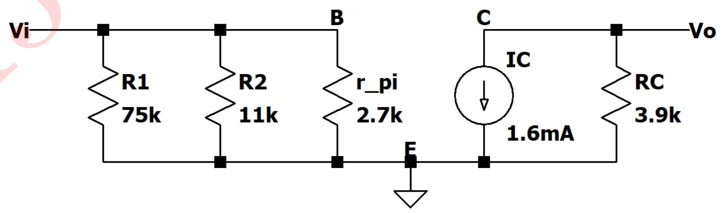

Figure 5: Small Signal Equivalent Circuit

$A_V = \dfrac{V_o}{V_i} = \dfrac{-g_m V_\pi R_C}{V_\pi}$

$A_V = -g_m R_C$

$A_V = -61.538 \times 10^{-3} \times 3.9 \times 10^3 = \mathbf{-239.9}$

$Z_i = (R_1 \ || \ R_2 \ || \ r_\pi)$

$Z_i = (75 \times 10^3 \ || \ 11 \times 10^3 \ || \ 2.7 \times 10^3)$

$Z_i = \mathbf{2.14\ k\Omega}$

$Z_o = R_C = \mathbf{3.9\ k\Omega}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

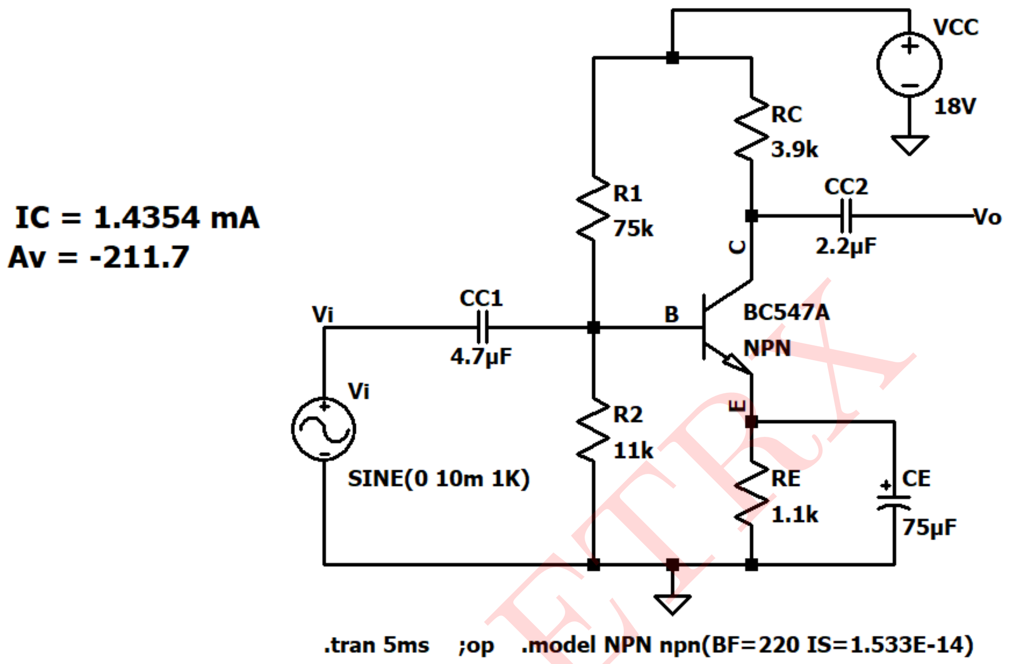

Figure 6: Circuit Schematic 1: Results

The input and output waveforms are shown in figure 7.

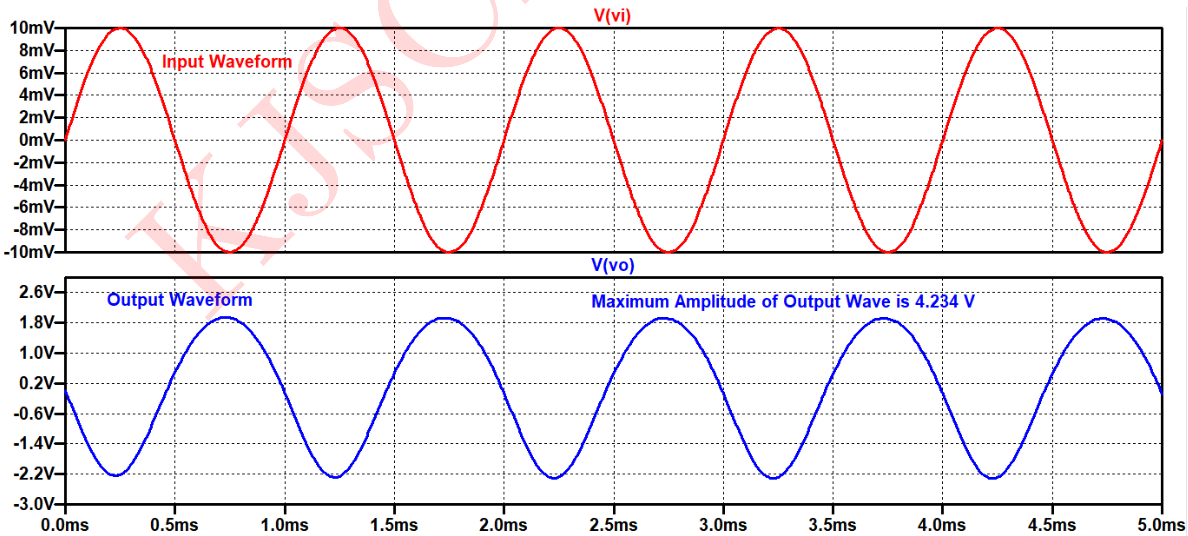

Figure 7: Input & Output waveforms

Comparison of theoretical and simulated values:

Parameters	**Theoretical Values**	**Simulated Values**
Voltage gain A_V	-180	-211.7
I_C	1.6 mA	1.4354 mA

Table 1: Design 1

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