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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Multi-transistor circuits

12^{th} **July, 2020**

Numerical 1:
For the circuit shown in figure 1, with transistor parameters $\beta_1 = \beta_2 = 120$ and $V_A = \infty$,
a. Determine the small-signal parameters g_m, r_π and r_o
b. Determine the overall small signal voltage gain $A_V = V_o/V_s$
c. Determine input resistance R_{is} and output resistance R_o

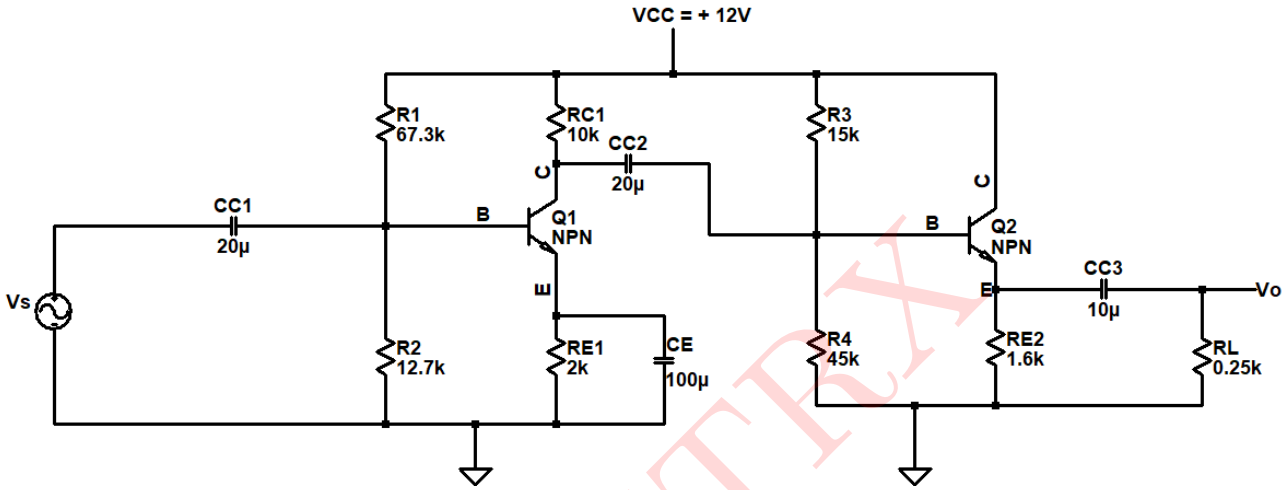

Figure 1: Circuit diagram

Solution: Circuit shown in figure 1 is a CE-CC cascade amplifier.

DC analysis: All capacitors are open-circuited and DC equivalent circuit of stage 1 is shown in figure 2.

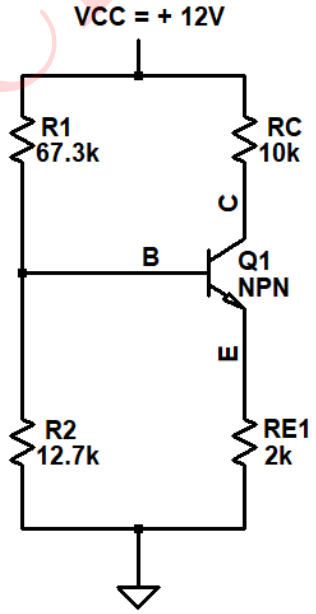

Figure 2: Stage 1 DC equivalent circuit

$$V_{TH} = \frac{12 \times 12.7}{67.3 + 12.7} = 1.905\text{V}$$

$$R_{TH} = 12.7k\Omega \parallel 67.3k\Omega = 10.6839\text{k}\Omega$$

Applying KVL to B-E loop:

$$V_{TH} - I_{B1}R_{TH} - V_{BE} - (\beta + 1)I_{B1}R_{E1} = 0$$

$$\therefore I_{BQ1} = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_{E1}} = \frac{1.905 - 0.7}{10.6839k\Omega + (121)(2k\Omega)}$$

$$\therefore I_{BQ1} = 4.769\mu A$$

$$I_{CQ1} = 0.5723mA \quad ...(\because I_{CQ1} = \beta I_{BQ1})$$

$$\therefore I_{EQ1} = (\beta + 1)I_{BQ1} = (121)(4.7691\mu A)$$

$$\therefore I_{EQ1} = 0.5770mA$$

Applying KVL to C-E loop:

$$12 - I_{CQ1}R_{C1} - V_{CE1} - I_{EQ1}R_{E1} = 0$$

$$\therefore V_{CEQ1} = 12 - (0.5723mA)(10k\Omega) - (0.5770mA)(2k\Omega)$$

$$\therefore V_{CEQ1} = 5.123V$$

Stage 2 DC equivalent circuit is shown in figure 3:

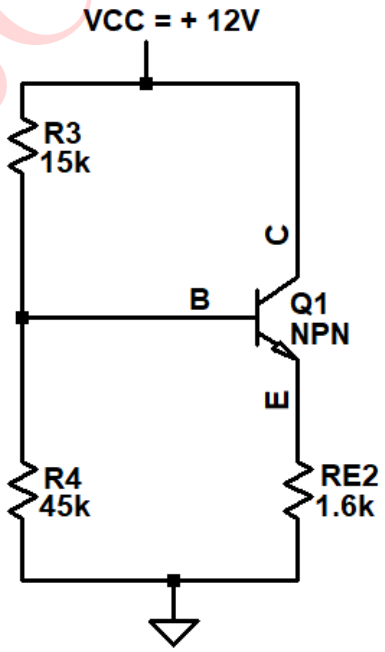

Figure 3: Stage 2 DC equivalent circuit

$$V_{TH} = \frac{12 \times 45}{15 + 45} = 9\text{V}$$

$$R_{TH} = 15k\Omega \parallel 45k\Omega = 11.25\text{k}\Omega$$

Applying KVL to B-E loop:

$$V_{TH} - I_{BQ2}R_{TH} - V_{BE} - (\beta + 1)I_{BQ2}R_{E2} = 0 \quad ...(\because I_{EQ2} = (\beta + 1)I_{BQ2})$$

$$\therefore I_{BQ2} = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_{E2}} = \frac{9 - 0.7}{11.25k\Omega + (121)(1.6k\Omega)}$$

$$\therefore I_{BQ2} = 40.5175\mu A$$

$$I_{CQ2} = \beta I_{BQ2} = (120)(40.5174\mu A)$$

$$\therefore I_{CQ2} = 4.8621mA$$

$$I_{EQ2} = (121)(40.5175\mu A) = 4.9026\text{mA}$$

Applying KVL to C-E loop:

$$12 - V_{CEQ2} - I_{EQ2}(R_{E2}) = 0$$

$$\therefore V_{CEQ2} = 12 - I_{EQ2}(R_{E2})$$

$$\therefore V_{CEQ2} = 12 - (4.9026mA)(1.6k\Omega)$$

$$\therefore V_{CEQ2} = 4.1558V$$

a. Small signal parameters:

For stage 1:

$$g_{m1} = \frac{I_{CQ1}}{V_T} = \frac{0.5723mA}{26mV} = 22.0115\text{mA/V}$$

$$r_{\pi 1} = \frac{\beta V_T}{I_{CQ1}} = \frac{120 \times 26mV}{0.5723mA} = 5.4517\text{k}\Omega$$

$$r_{o1} = \frac{V_A}{I_{CQ1}} = \infty \quad ...(\because V_A = \infty)$$

For stage 2:

$$g_{m2} = \frac{I_{CQ2}}{V_T} = \frac{4.8621mA}{26mV} = 187\text{mA/V}$$

$$r_{\pi 2} = \frac{\beta V_T}{I_{CQ2}} = \frac{120 \times 26mV}{4.8621mA} = 641.70\Omega$$

$$r_{o2} = \frac{V_A}{I_{CQ2}} = \infty \quad ...(\because V_A = \infty)$$

b. Small signal equivalent circuit of CE-CC amplifier is shown in figure 4.
All capacitors are short-circuited.

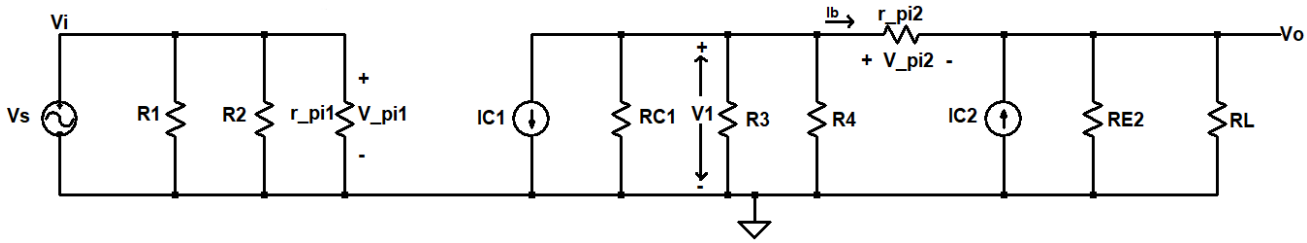

Figure 4: Small signal equivalent circuit

For stage 1: $A_{V1} = \dfrac{V_{o1}}{V_s}$

$V_s = V_{\pi 1}$

Deriving formula for V_1 :

$V_1 - V_{\pi 2} - (\beta + 1)I_b(R_{E2} \parallel R_L) = 0$

$V_1 = r_{\pi 2}I_b + (\beta + 1)I_b(R_{E2} \parallel R_L)$

$R = \dfrac{V_1}{I_b} = r_{\pi 2} + (\beta + 1)(R_{E2} \parallel R_L)$

$\therefore V_{o1} = -I_{C1}(R_{C1} \parallel R_3 \parallel R_4 \parallel r_{\pi 2} + (\beta + 1)(R_{E2} \parallel R_L))$

$\therefore V_{o1} = -g_{m1}V_{\pi 1}[R_{C1} \parallel R_3 \parallel R_4 \parallel r_{\pi 2} + (\beta + 1)(R_{E2} \parallel R_L)]$

$\therefore A_{V1} = -g_{m1}[R_{C1} \parallel R_3 \parallel R_4 \parallel r_{\pi 2} + (\beta + 1)(R_{E2} \parallel R_L)]$

$\therefore A_{V1} = -(22.015 \times 10^{-3})[10k\Omega \parallel 15k\Omega \parallel 45k\Omega \parallel 0.641 + (121)(1.6k\Omega \parallel 0.25k\Omega)]$

$\therefore A_{V1} = -97.3106$

For stage 2: $A_{V2} = \dfrac{V_o}{V_s}$

$V_o = (\beta + 1)I_b(R_{E2} \parallel R_L)$

$V_1 = I_b r_{\pi 2} + I_b(\beta + 1)(R_{E2} \parallel R_L)$

$\therefore A_{V2} = \dfrac{(\beta + 1)(R_{E2} \parallel R_L)}{r_{\pi 2} + (\beta + 1)(R_{E2} \parallel R_L)}$

$\therefore A_{V2} = \dfrac{(121)(0.2162k\Omega)}{0.641k\Omega + (121)(0.2162k\Omega)}$

$\therefore A_{V2} = 0.9761$

Overall gain: $A_{Vt} = A_{V1} * A_{V2}$

$\therefore A_{Vt} = (-97.3106)(0.9761)$

$\therefore \mathbf{A_{Vt} = -94.9849}$

c. Input resistance of CE-CC cascade amplifier is input resistance of CE amplifier.
$\therefore R_{is} = R_1 \parallel R_2 \parallel r_{\pi 1} = 67.3k\Omega \parallel 12.7k\Omega \parallel 5.4517k\Omega$
$\therefore \mathbf{R_{is} = 3.6097k\Omega}$

Output resistance of CE-CC cascade amplifier is the output resistance of CC

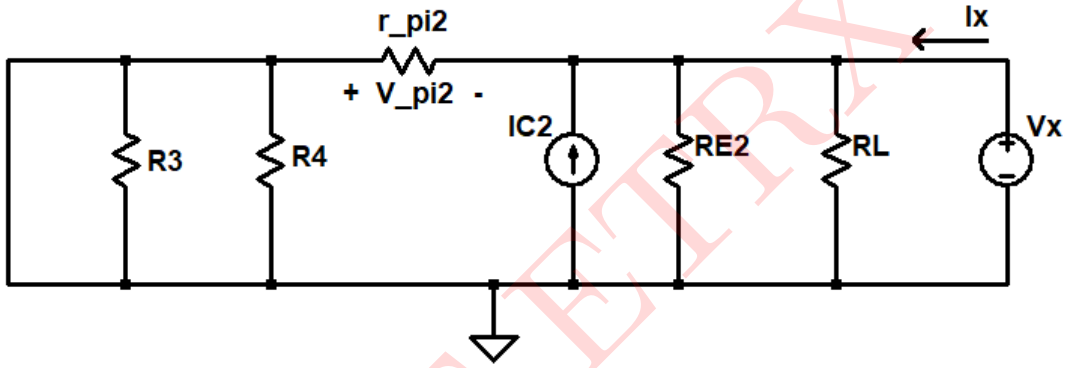

Figure 5: For calculating output resistance

$\therefore R_o = \dfrac{V_x}{I_x}$

$V_{\pi 2}$ is a function of V_x

$\therefore V_{\pi 2} = -V_x$

Applying KCL:
$I_x + g_m V_\pi = \dfrac{V_x}{R_{E2}} + \dfrac{V_x}{R_L} + \dfrac{V_x}{r_{\pi 2}}$

$\therefore \dfrac{I_x}{V_x} = \dfrac{1}{R_o} = g_{m2} + \dfrac{1}{R_{E2}} + \dfrac{1}{r_{\pi 2}} + \dfrac{1}{R_L}$

$\therefore R_o = 5.3476 \parallel 1.6k\Omega \parallel 0.641k\Omega \parallel 0.25k\Omega$

$\therefore \mathbf{R_o = 5.1764\Omega}$

SIMULATED RESULTS:

Above circuit was simulated in LTspice and results obtained are as follows:

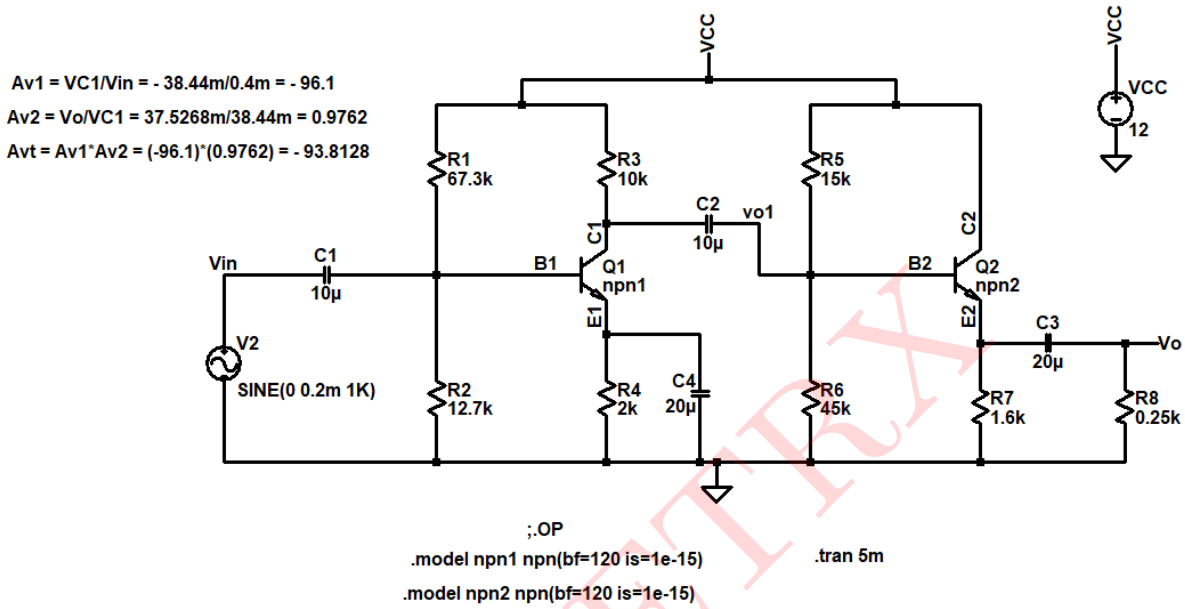

Figure 6: Circuit Schematic: Results

The input and output waveforms are shown in figures below:

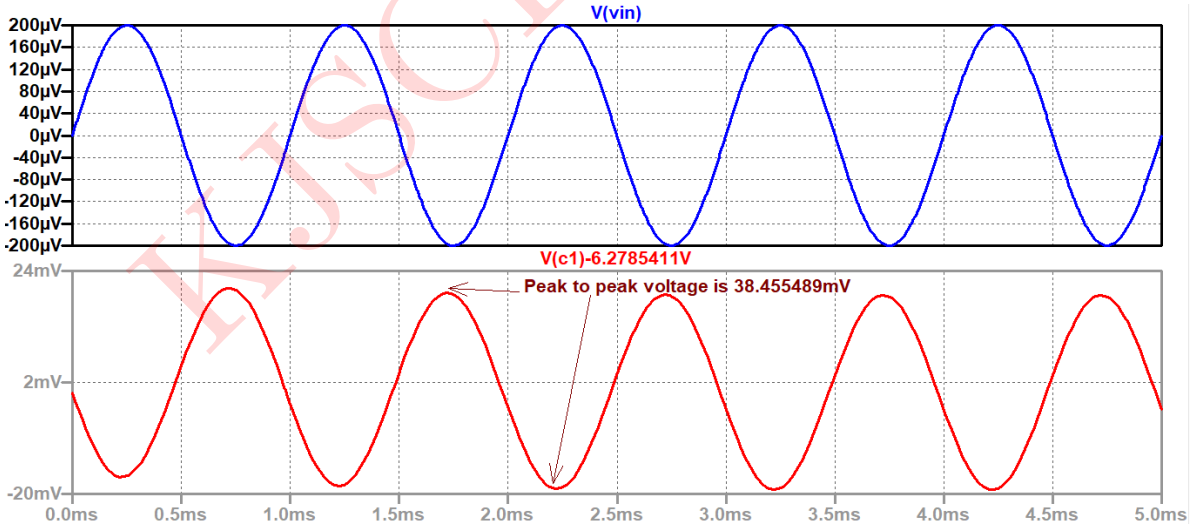

Figure 7: Input and output waveform for Stage 1 voltage gain

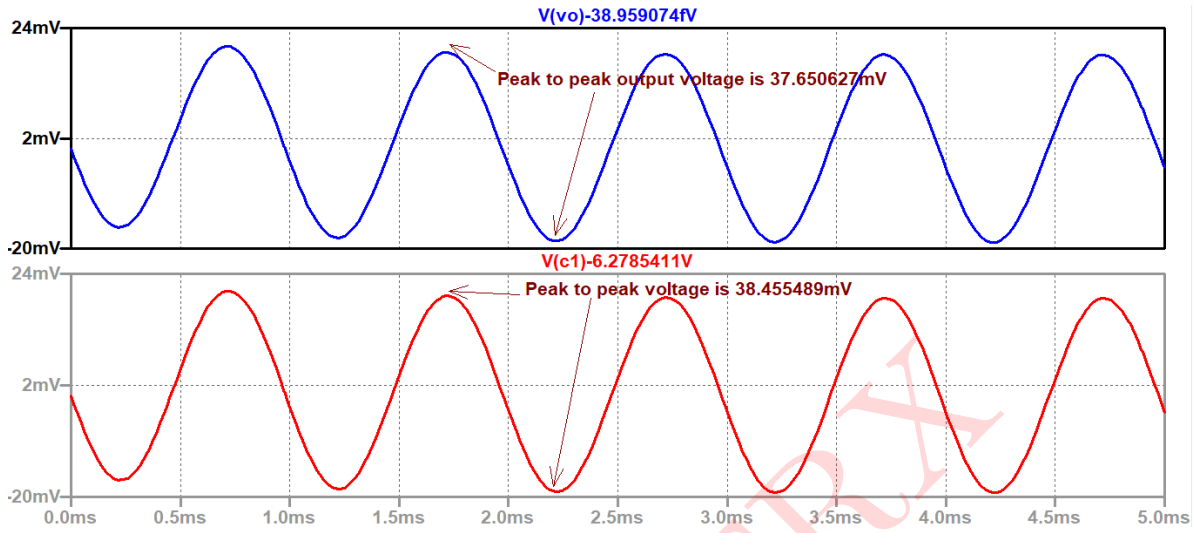

Figure 8: Input and output waveform for Stage 2 voltage gain

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
Q-point values I_{C1Q}, V_{CE1Q}	0.5723mA, 5.123V	0.5722mA, 5.1247V
Q-point values I_{C2Q}, V_{CE2Q}	4.8621mA, 4.1558V	4.8300mA, 4.2082V
Voltage gain of stage 1: A_{V1}	−97.3106	−96.1
Voltage gain of stage 2: A_{V2}	0.9761	0.9762
Overall voltage gain: A_{Vt}	−94.9849	−93.8128
Input impedance of Stage 1	3.6097kΩ	–
Output impedance of Stage 2	5.1764Ω	–
Output voltage	38mV	37.5450mV

Table 1: Numerical 1

Numerical 2:
A two stage circuit is shown in figure 9, MOSFET parameters are $V_{TN1} = V_{TN2} = 5V$, $k_{N1} = k_{N2} = 0.12mA/V^2$ & $\lambda_1 = \lambda_2 = 0$. Determine:
a. Q-point for both stages.
b. Draw mid-frequency equivalent circuit.
c. Calculate A_{V1} and A_{V2}
d. Calculate A_{Vt}
e. Calculate V_{out} if $V_s = 20$mV
f. Calculate Z_i and Z_o

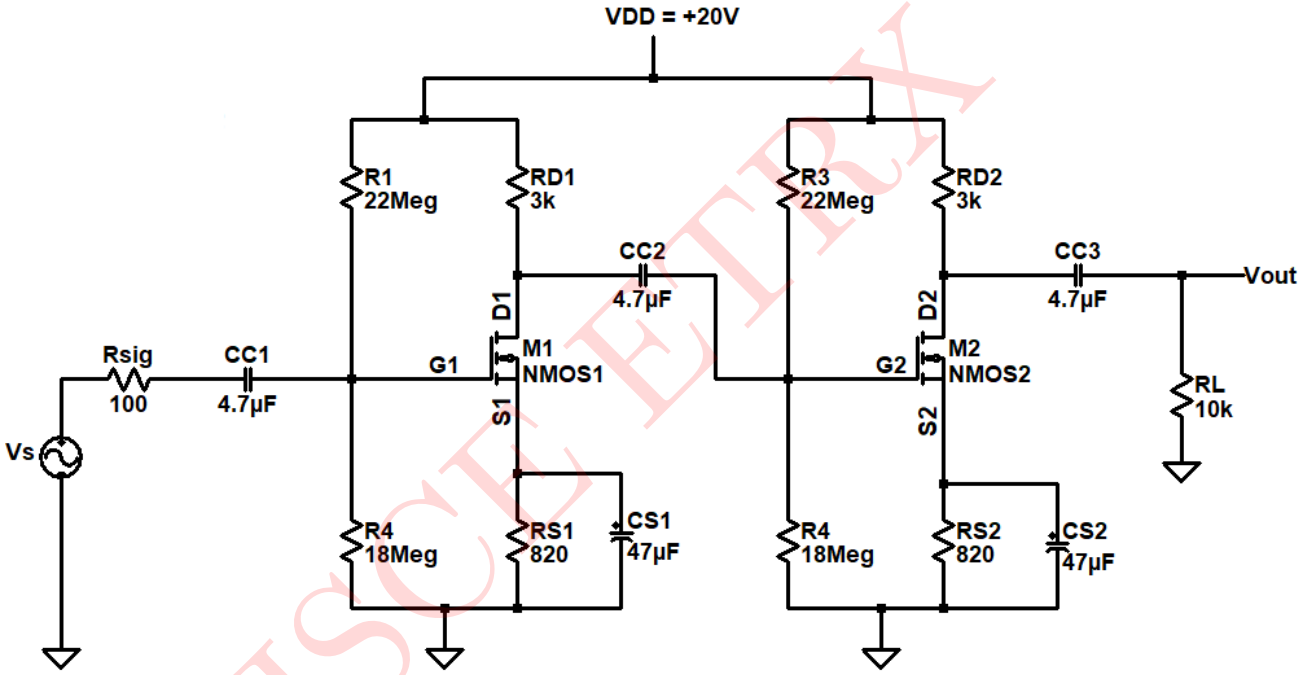

Figure 9: Circuit diagram

Solution: The circuit shown in figure 9 is a CS-CS cascaded MOSFET amplifier.

a. DC analysis: All capacitors are open-circuited and DC equivalent circuit of stage 1 is shown in figure 10.

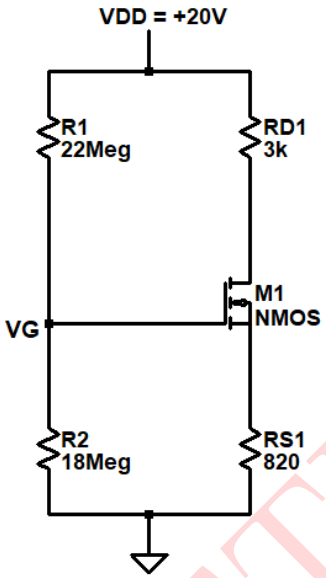

Figure 10: DC equivalent circuit

Since both the stages of given amplifier are symmetrical, DC analysis of single-stage is as shown:

$$V_{G1} = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{18M\Omega}{22M\Omega + 18M\Omega} \times 20$$

$$\therefore V_{G1} = 9V$$

$$V_{S1} = I_D R_{S1}$$

$$\therefore V_{GS1} = V_{G1} - V_{S1}$$

$$\therefore V_{GS1} = 9 - I_D(820) = 9 - I_D(0.82k\Omega)$$

$$\therefore 9 - I_D(0.82k\Omega) \quad ...(1)$$

For MOSFET in saturation region, $I_D = k_N(V_{GS} - V_{TN})^2$

Here, $I_{D1} = I_{D2} = I_D$ and $V_{TN1} = V_{TN2} = V_{TN}$

Similarly, $k_{N1} = k_{N2} = k_N$

$$I_D = k_N(V_{GS} - V_{TN})^2 \quad ...(2)$$

Substituting (2) in (1):
$V_{GS} = 9 - (0.82k\Omega)[k_N(V_{GS} - V_{TN})^2]$

$V_{GS} = 9 - (0.82k\Omega)[0.12 \times 10^{-3}(V_{GS} - 5)^2]$

$V_{GS} = 9 - (0.82k\Omega)[0.12 \times 10^{-3}(V_{GS}^2 + 25 - 10V_{GS})]$

$\therefore V_{GS} = 9 - 0.0984V_{GS}^2 + 0.984V_{GS} - 2.46$

$\therefore 0.0984V_{GS}^2 + 0.016V_{GS} - 6.54 = 0$

$\therefore V_{GS} = 8.07V, -8.234V$

Since, $V_{GS} > V_{TN}$
$\therefore \mathbf{V_{GS} = 8.07V}$

From (2):
$I_D = k_N(V_{GS} - V_{TN})^2$

$I_D = (0.12 \times 10^{-3})(8.07 - 5)^2$

$\therefore \mathbf{I_D = 1.13mA}$

Small signal parameters:
Small signal parameters will be same for both the stages.

$g_m = 2k_N(V_{GS} - V_{TN})$

$\therefore g_m = 2(0.12 \times 10^{-3})(8.07 - 5)$

$\therefore g_{m1} = g_{m2} = g_m = 0.7368mA/V$

b. Mid-frequency equivalent circuit is shown in figure 11

All the capacitors are short-circuited. The mid-frequency equivalent circuit for each stage is derived separately and are joined in such a way that, the output of first stage in the input of second stage.

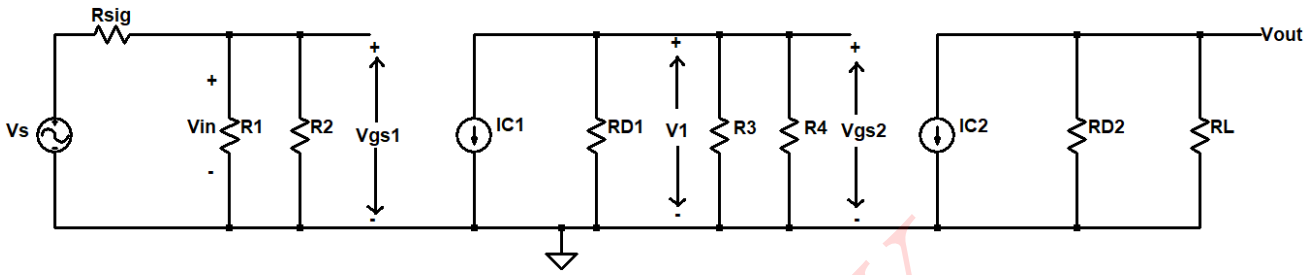

Figure 11: Mid-frequency equivalent circuit

c. For stage 1: Mid-band gain will be given as:

$$A_{V1} = \frac{V_1}{V_s}$$

$$V_1 = -I_{D1}(R_{D1} \parallel R_3 \parallel R_4)$$

$$\therefore V_1 = -g_{m1}V_{gs1}(R_{D1} \parallel R_3 \parallel R_4)$$

We know, $V_s = V_{gs1}$

$$A_{V1} = \frac{-g_m V_{gs1}(R_{D1} \parallel R_3 \parallel R_4)}{V_{gs1}}$$

$$\therefore A_{V1} = -g_{m1}(R_{D1} \parallel R_3 \parallel R_4)$$

$$\therefore A_{V1} = -(0.7368 \times 10^{-3})(3k\Omega \parallel 22M\Omega \parallel 18M\Omega)$$

$$\therefore A_{V1} = (-0.7368 \times 10^{-3})(2.999k\Omega)$$

$$\therefore \mathbf{A_{V1} = -2.209} \quad \text{...(3)}$$

For stage 2: $A_{V2} = \frac{V_{out}}{V_1}$

$$\therefore V_{out} = -I_{D2}(R_{D2} \parallel R_L)$$

$$\therefore V_{out} = -g_{m2}V_{gs2}(R_{D2} \parallel R_L)$$

$$V_1 = V_{gs2}$$

$$\therefore A_{V2} = \frac{-g_{m2}V_{gs2}(R_{D2} \parallel R_L)}{V_{gs2}}$$

$$\therefore A_{V2} = -g_{m2}(R_{D2} \parallel R_L)$$

$$\therefore A_{V2} = -(0.7368 \times 10^{-3})(3k\Omega \parallel 10k\Omega)$$

$$\therefore A_{V2} = (-0.7368 \times 10^{-3})(2.307k\Omega) = \mathbf{-1.7} \quad \text{...(4)}$$

d. Overall mid-band gain is given as:

$$A_V = \frac{V_{out}}{V_s} = \frac{V_{out}}{V_1} \times \frac{V_1}{V_{in}} \times \frac{V_{in}}{V_s}$$

where: $\frac{V_{out}}{V_1} = A_{V2}$ (gain for stage 2) & $\frac{V_1}{V_{in}} = A_{V1}$ (gain for stage 1)

From small signal equivalent circuit:

$$V_{in} = \frac{R_1 \parallel R_2}{R_{sig} + R_1 \parallel R_2} \times V_s$$

$$V_{in} = \left[\frac{18M\Omega \parallel 22M\Omega}{0.1k\Omega + 18M\Omega \parallel 22M\Omega}\right] \times V_s$$

$$\frac{V_{in}}{V_s} = \frac{9.9M\Omega}{0.1k\Omega + 9.9M\Omega} = \frac{9.9M\Omega}{9.9001M\Omega}$$

$$\therefore \frac{V_{in}}{V_s} \approx 1$$

$$\therefore A_{Vt} = A_{V2} \times A_{V1} \times \frac{V_{in}}{V_s}$$

$$\therefore A_{Vt} = (-1.7)(-2.209)(1) \quad \text{...(from (3), (4) and (5))}$$

$$\therefore \mathbf{A_{Vt} = 3.7553}$$

$$\therefore A_{Vt} \text{ (in dB)} = 20\log_{10}(3.7553)$$

$$\mathbf{A_{Vt} = 11.4929dB}$$

e. Output Voltage:

$$V_{out} = A_{Vt} \times V_{in}$$

Given: $V_{in} = 20mV$

$$\therefore V_{out} = (3.7553)(20mV)$$

$$\therefore \mathbf{V_{out} = 75.106mV}$$

f. Input Impedance:

$$Z_i = R_1 \parallel R_2 = 22M\Omega \parallel 18M\Omega$$

$$\therefore \mathbf{Z_i = 9.9M\Omega}$$

Output impedance:

$$Z_o = R_{D2} \parallel R_L = 3k\Omega \parallel 10k\Omega$$

$$\therefore \mathbf{Z_o = 2.3077k\Omega}$$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

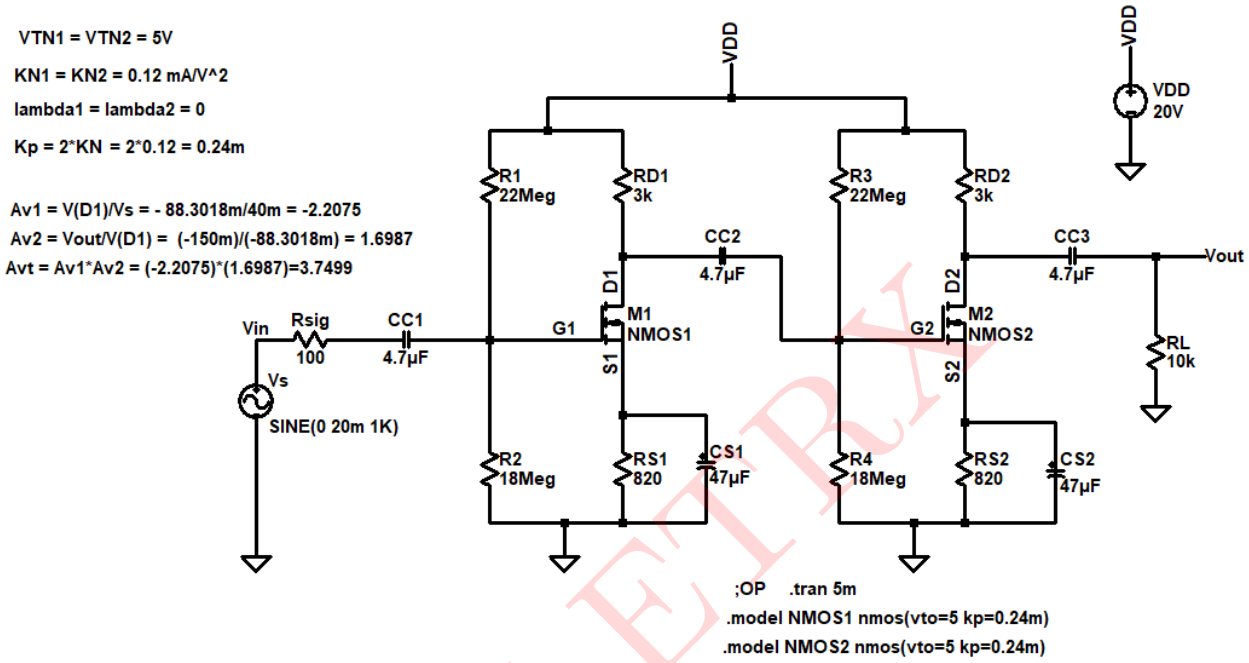

Figure 12: Circuit Schematic: Results

The input and output waveforms are shown in figures below:

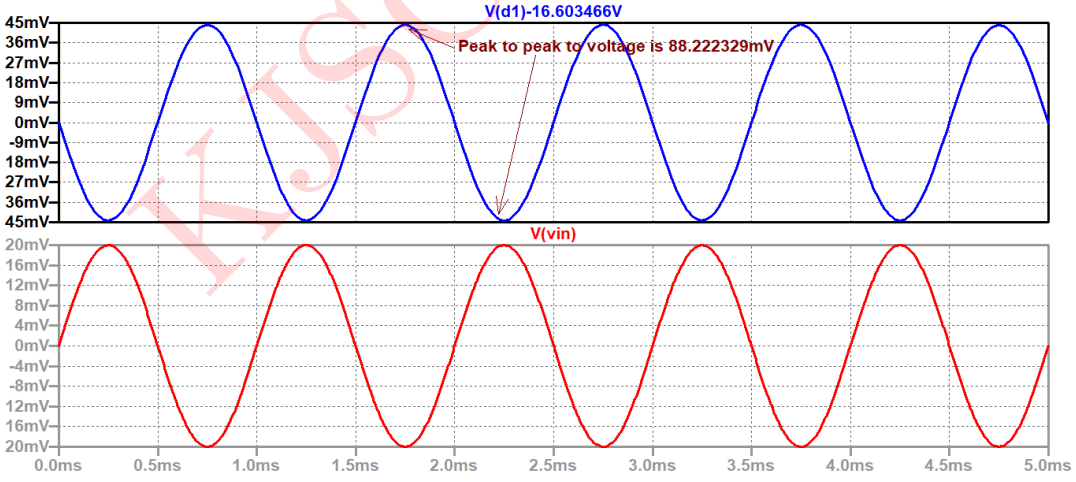

Figure 13: Input and output waveform for Stage 1 voltage gain

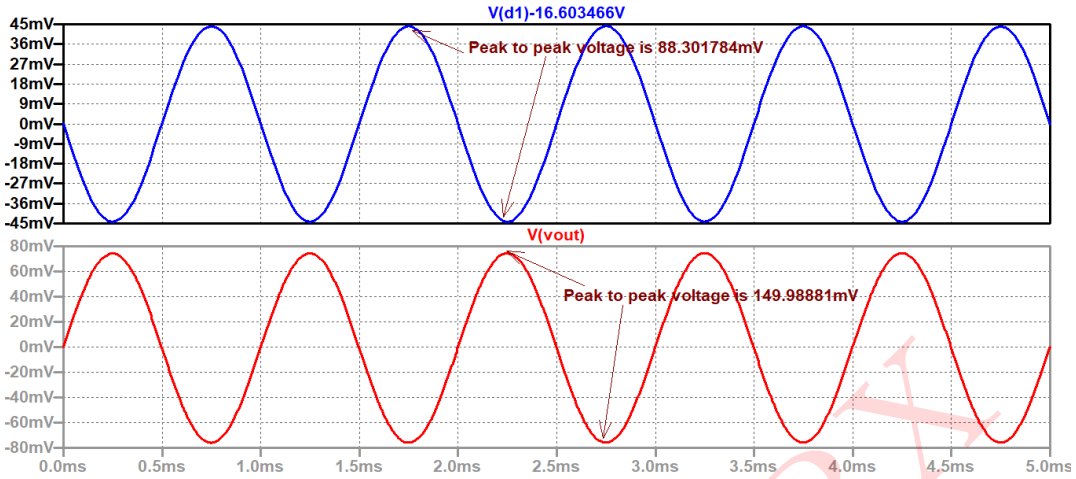

Figure 14: Input and output waveform for Stage 2 voltage gain

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
Q-point values I_{D1Q}, V_{GS1Q}	1.13mA, 8.07V	1.1322mA, 8.0716V
Q-point values I_{D2Q}, V_{GS2Q}	1.13mA, 8.07V	1.1322mA, 8.0761V
Voltage gain of stage 1: A_{V1}	-2.209	-2.2075
Voltage gain of stage 2: A_{V2}	-1.7	-1.6987
Overall voltage gain: A_{Vt}	11.4929	11.4804
Input impedance of Stage 1	9.9MΩ	–
Output impedance of Stage 2	2.3077kΩ	–
Output voltage	75.106mV	75mV

Table 2: Question 1

Numerical 3:
For each transistor in the circuit in figure 15, $\beta = 120$ and $V_{BE(ON)} = 0.7V$
Determine the quiescent base, collector and emitter currents in Q1 and Q2. Also determine V_{CEQ1} and V_{CEQ2}

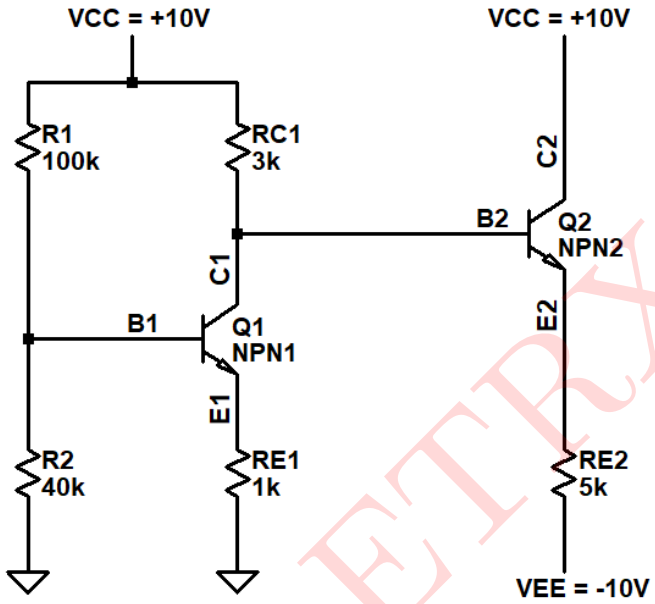

Figure 15: Circuit diagram

Solution: Circuit shown in figure 15 is a directly coupled cascade amplifier.

DC analysis: All capacitors are open-circuited and Thevenin's equivalent circuit for first transistor shown in figure 16:

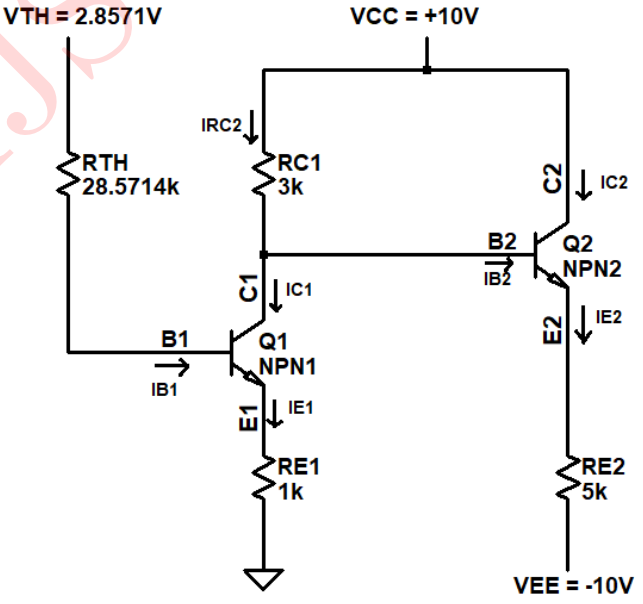

Figure 16: Thevenin's equivalent circuit

Applying KVL to B-E loop:

$V_{TH} - I_{B1}R_{TH} - V_{BE1} - I_{E1}R_{E1} = 0$

$\therefore V_{TH} - I_{B1}R_{TH} - V_{BE1} - (\beta+1)I_{B1}R_{E1} = 0 \quad ...(\because I_{E1} = (\beta+1)I_{B1})$

$\therefore I_{B1} = \dfrac{V_{TH} - V_{BE1}}{R_{TH} + (\beta+1)R_{E1}} = \dfrac{2.8571 - 0.7}{28.5714 + 121 \times 1}$

$\therefore I_{B1} = 14.4219\mu A$

$I_{C1} = \beta I_{B1} = 120 \times 14.4219\mu A$

$\therefore I_{C1} = 1.7306mA$

$I_{E1} = (\beta+1)I_{B1} = 121 \times 14.4219\mu A$

$I_{E1} = 1.7450mA$

$V_{E1} = I_{E1}R_{E1} = (1.7450mA)(1k\Omega)$

$\therefore V_{E1} = 1.7450V$

$V_{BE1} = V_{B1} - V_{E1}$

$V_{B1} = V_{BE1} + V_{E1} = 0.7 + 1.7450$

$\therefore V_{B1} = 2.4450V$

$V_{C1} = 10 - I_{RC1}(R_{C1})$ ...(1)

By KCL, $I_{RC1} = I_{C1} + I_{B2}$ ...(2)

$\therefore V_{C1} = 10 - (I_{B2} + I_{C1})R_{C1}$

Ignoring I_{B2},

$\therefore V_{C1} = 10 - I_{C1}R_{C1} = 10 - (1.7306mA)(3k\Omega)$

$\therefore V_{C1} = 4.8082V$

$V_{BE2} = V_{B2} - V_{E2}$

$\therefore V_{E2} = V_{B2} - V_{BE2}$

$V_{E2} = V_{C1} - V_{BE2} \quad (\because V_{C1} = V_{B2})$

$V_{E2} = 4.8082 - 0.7$

$\therefore V_{E2} = 4.1082V$

$$I_{E2} = \frac{V_{E2} - V_{EE}}{R_{E2}} = \frac{4.1082 + 10}{5k\Omega}$$

$$I_{E2} = 2.8216mA$$

$$I_{C2} = \frac{\beta}{\beta + 1} \times I_{E2} = \frac{120}{121} \times 2.8216 \times 10^{-3}$$

$$\therefore I_{C2} = 2.7983mA$$

$$I_{B2} = \frac{I_{E2}}{\beta + 1} = \frac{2.8216mA}{121}$$

$$\therefore I_{B2} = 23.319\mu A$$

Rewriting (1), we get:

$$V_{C1(new)} = 10 - (I_{C1} + I_{B2})R_{C1} \quad ...(\text{from}(2))$$

$$\therefore V_{C1(new)} = 10 - (1.7306mA + 23.319\mu A)(3k\Omega)$$

$$V_{C1(new)} = 4.7382V$$

$$\therefore V_{E2(new)} = V_{C1(new)} - V_{BE2} = 4.7382 - 0.7$$

$$V_{E2(new)} = 4.0382V$$

$$I_{E2(new)} = \frac{V_{E2(new)} - V_{EE}}{R_{E2}} = \frac{4.0382 + 10}{5k\Omega}$$

$$\therefore I_{E2(new)} = 2.8076mA$$

$$I_{C2(new)} = \frac{\beta}{\beta + 1} \times I_{E2(new)}$$

$$\therefore I_{C2(new)} = \frac{120}{121} \times 2.8076mA$$

$$\therefore I_{C2(new)} = 2.7844mA$$

$$I_{B2(new)} = \frac{I_{E2}}{1 + \beta} = \frac{2.8706mA}{121}$$

$$\therefore I_{B2(new)} = 23.2033\mu A$$

Also, $V_{C2} = 10V$

Applying KVL to C-E loop of Q1:
$10 - I_{RC1}R_{C1} - V_{CE1} - I_{E1}R_{E1} = 0$

$\therefore V_{CE1} = 10 - I_{RC1}R_{C1} - I_{E1}R_{E1}$

$V_{CE1} = 10 - (1.7539mA)(3k\Omega) - (1.7450mA)(1k\Omega)$

$V_{CE1} = 2.9933V$

Applying KVL to C-E loop of Q2:
$10 - V_{CE2} - I_{E2(new)}R_{E2} + 10 = 0$

$V_{CE2} = 20 - I_{E2(new)}R_{E2}$

$\therefore V_{CE2} = 20 - (2.8076mA)(5k\Omega) = 5.9620\text{V}$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

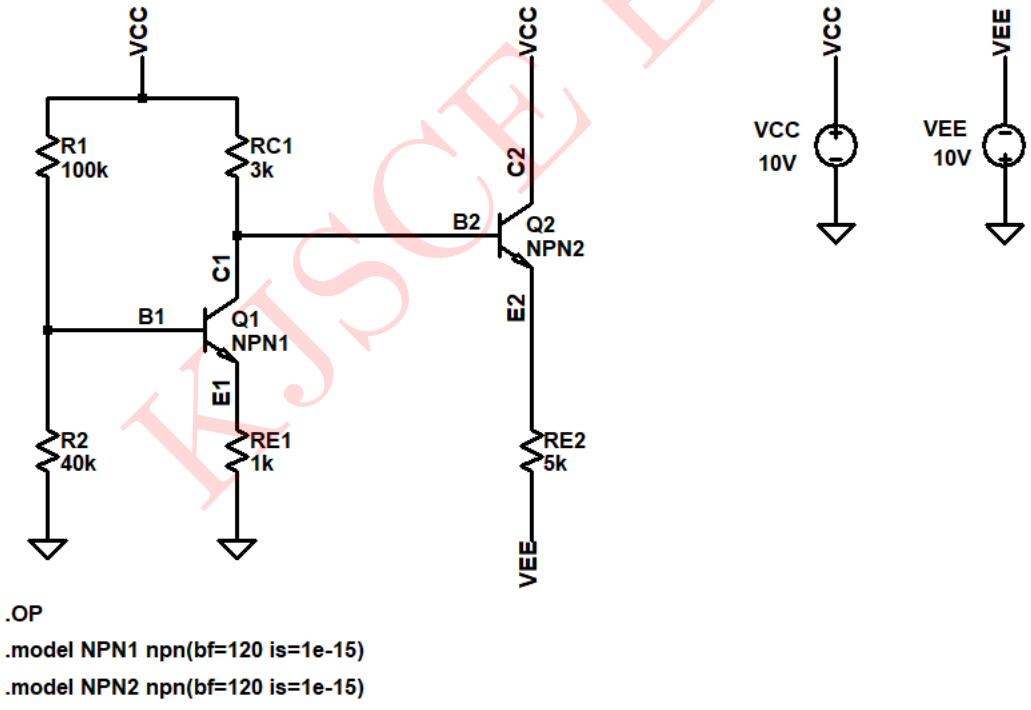

Figure 17: Circuit Schematic: Results

Comparsion between theoretical and simulated values:

Parameters	Theoretical value	Simulated value
I_{B1}	14.4219 μA	14.2315 μA
I_{C1}, I_{E1}	1.7306mA, 1.7450mA	1.7078mA, 1.7220mA
I_{B2}	23.2033 muA	23.2491 $u\mu A$
I_{C2}, I_{E2}	2.7844 mA, 2.8076mA	2.7899mA, 2.8131 mA
V_{C1}	4.7832V	4.8069 V
V_{C2}	10V	10V
V_{E1}	1.7450V	1.7220V
V_{E2}	4.0832V	4.0657V
V_{B1}	2.4450V	2.4505V
V_{B2}	4.7382V	4.8069V
V_{CE1}	2.9933V	3.0849V
V_{CE2}	5.9620V	5.9343V

Table 3: Numerical 3