K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Diode Applications

Numerical 1:
For the circuit shown in figure 1, Plot:
a. Input $V_{in}(t)$ and output $V_{out}(t)$ waveforms.
b. Voltage Transfer Characteristics.
Given: $V_{in}(t) = 10$Vp-p sinusoidal signal with frequency of 5000Hz. Use constant voltage model i.e. $V_{D(ON)} = 0.7$V, $V_B = 1$V, $R_1 = 1$kΩ

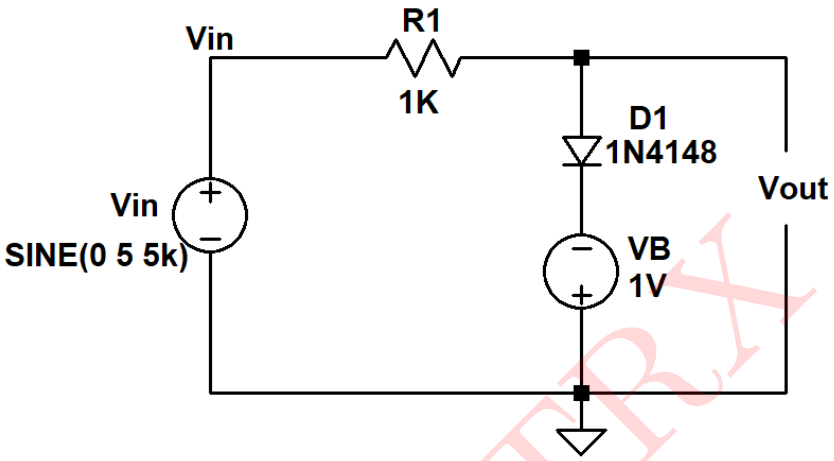

Figure 1: Circuit Diagram

Solution: The bias voltage V_B forward biases the diode D1
1. If $V_{in} < V_{D(ON)} - V_B$
i.e. $V_{in} < 0.7 - 1$

which is $V_{in} < -0.3V$, the diode D1 is reverse biased, since cathode of the diode is more positive than anode by 0.7V. Hence, the diode is off and the circuit reduces to circuit shown in figure 2:

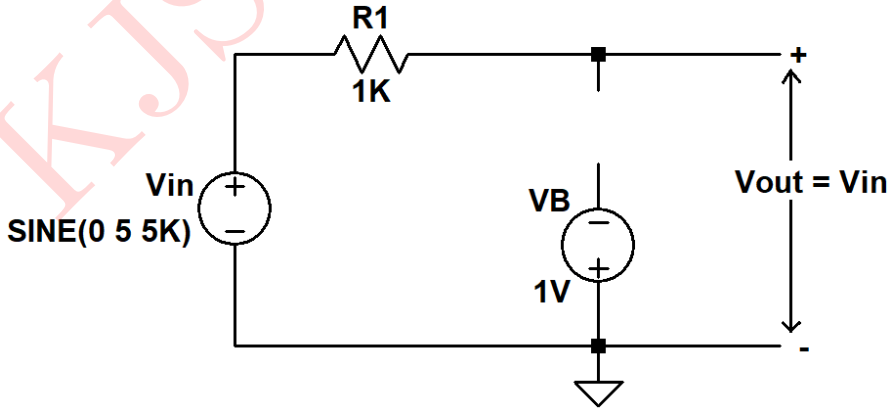

Figure 2: Diode is off

$\therefore \mathbf{V_{out} = V_{in}}$

2. If $V_{in} > V_{D(ON)} - V_B$
i.e. $V_{in} > 0.7 - 1$

which is $V_{in} > -0.3V$, the diode D1 is forward biased, since anode of the diode is more positive than cathode by 0.7V. Hence, the diode is on and the circuit reduces to circuit shown in figure 3:

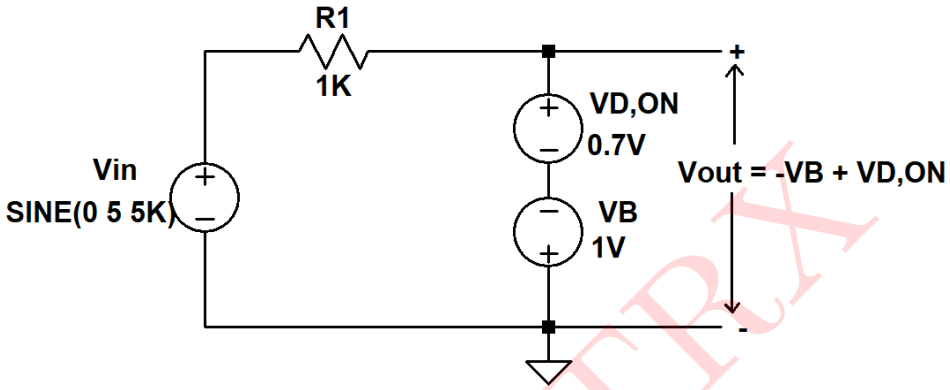

Figure 3: Diode is on

$\therefore \mathbf{V_{out} = -V_B + V_{D(ON)} = -1 + 0.7 = -0.3V}$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

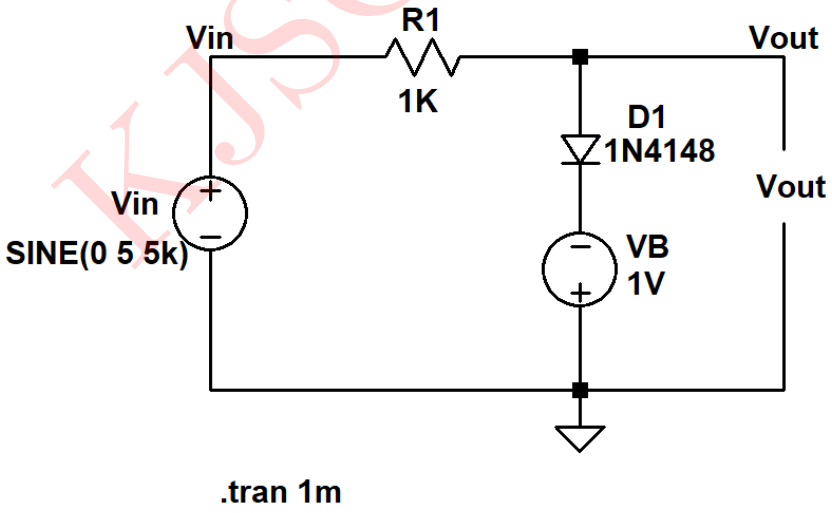

Figure 4: Circuit Schematic: Results

Input and Output waveforms are shown in figure 5:

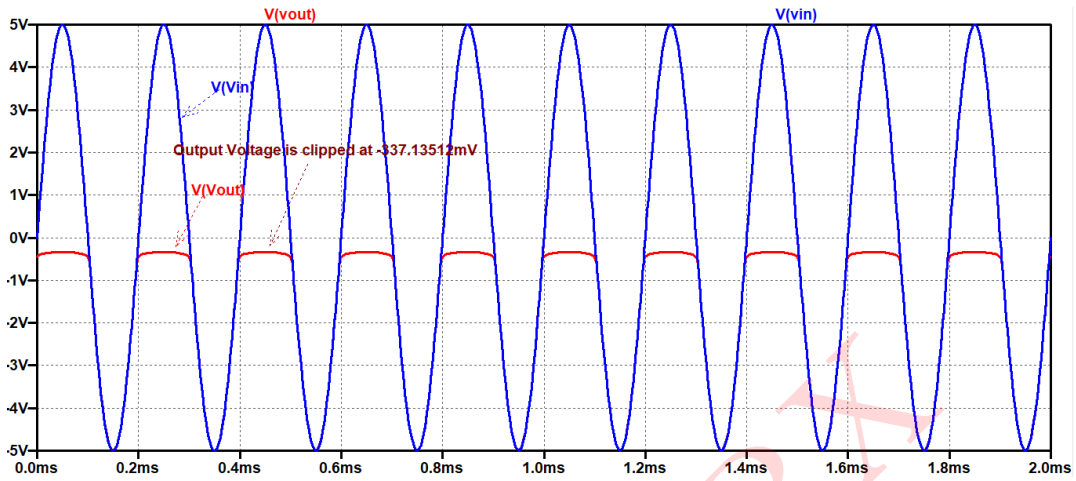

Figure 5: Input and output waveforms

Voltage Transfer characteristics is shown in figure 6:

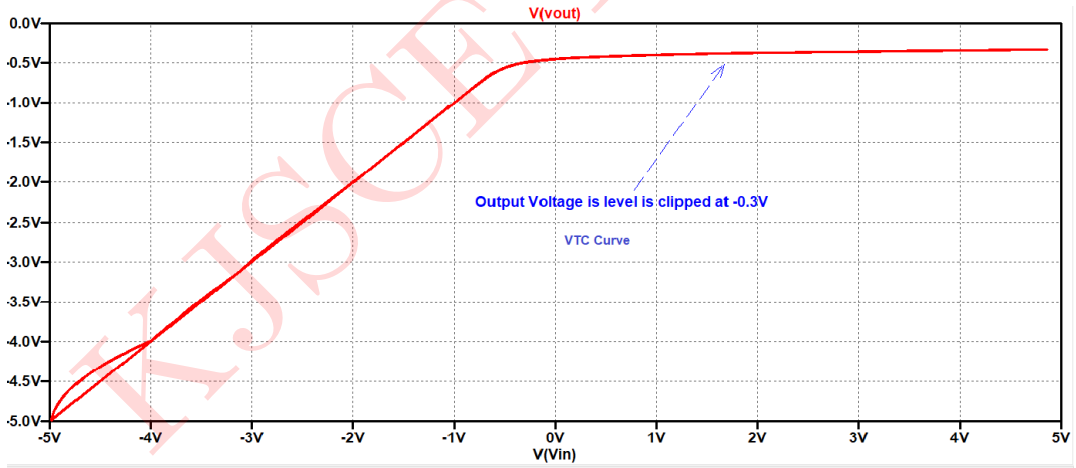

Figure 6: Voltage transfer characteristics

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
V_{out} clipped level	-0.3V	-0.337V

Table 1: Question 1

Numerical 2:
For the circuit shown in figure 7, plot input waveform $V_{in}(t)$ and output waveform $V_{out}(t)$

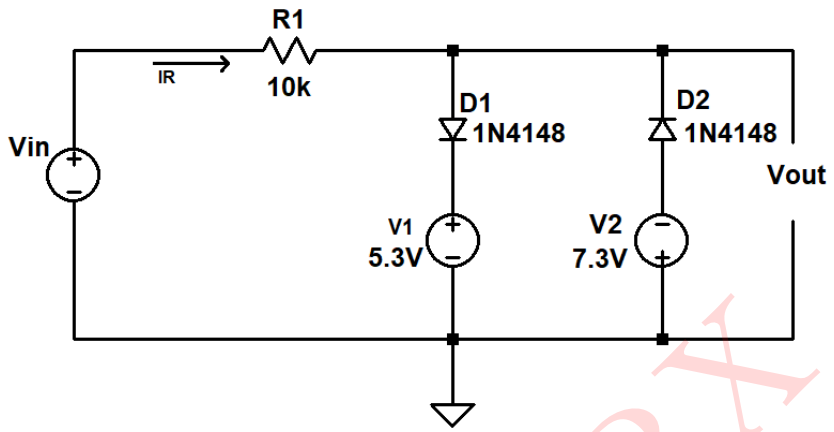

Figure 7: Circuit Diagram

Given: $V_{in}(t)$ = 20Vp-p triangular wave with frequency of 1000 Hz, $V_{D(ON)} = 0.7$V
Figure 8 represents input waveform:

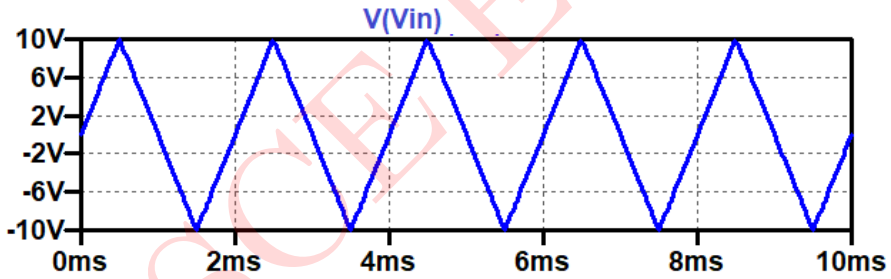

Figure 8: Input waveform

Solution: The bias voltage V_1 forward biases D1 diode and bias voltage V_2 reverse biases D2 diode.

A. For the positive half cycle: The diode D2 remains off for the entire positive half cycle since it is reverse biased (the cathode voltage is more positive than anode by 0.7V)

1. When $V_{in} < V_{D(ON)} + V_1$

i.e. $V_{in} < 0.7 + 5.3$

which is $V_{in} < 6V$, the diode D1 reverse biases since cathode is more positive than anode by 0.7V

$\therefore$ D1 is OFF and circuit reduces to as shown in figure 9:

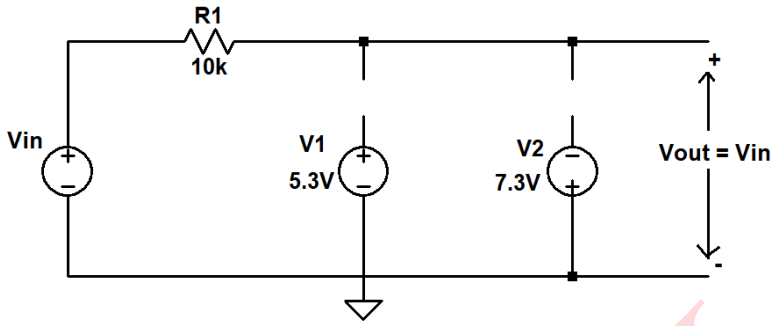

Figure 9: D1 and D2 are off

$\therefore \mathbf{V_{out} = V_{in}}$

2. When $V_{in} > V_{D(ON)} + V_1$

i.e. $V_{in} > 0.7 + 5.3$

which is $V_{in} > 6V$, the diode D1 forward biases since anode is more positive than cathode by 0.7V

$\therefore$ D1 is ON and circuit reduces to as shown in figure 10:

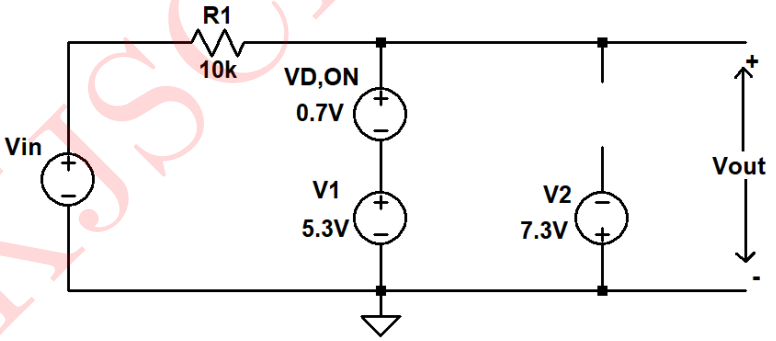

Figure 10: D1 is On and D2 is off

$\therefore V_{out} = V_1 + V_{D(ON)} = 5.3 + 0.7$

$\therefore \mathbf{V_{out} = 6V}$

B. For negative half cycle, the diode D1 remains OFF for the entire negative half cycle since it gets reverse biased (cathode is more positive than anode by 0.7V)

1. When $V_{in} < V_{D(ON)} + V_2$

i.e. $V_{in} < 0.7 + 7.3$

which is $V_{in} < 8V$, the diode D2 is reverse biased since cathode of D2 diode is more positive than anode by 0.7V

$\therefore$ D2 is OFF and the circuit reduces to as shown in figure 11:

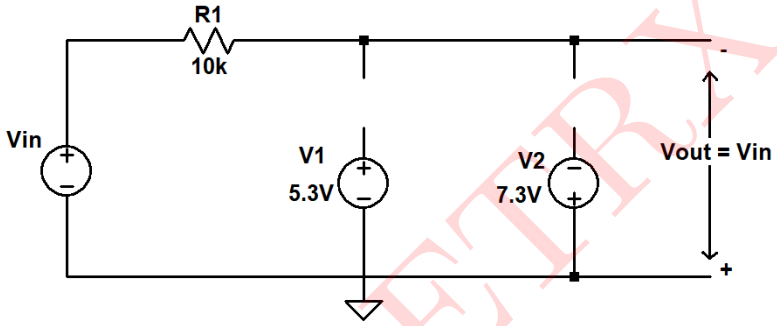

Figure 11: D1 and D2 are off

2. When $V_{in} > V_{D(ON)} + V_2$

i.e. $V_{in} > 0.7 + 7.3$

which is $V_{in} > 8V$, the diode D2 is forward biased since the anode is more positive than cathode by 0.7V

$\therefore$ D2 diode is ON and the circuit reduces to as shown in figure 12:

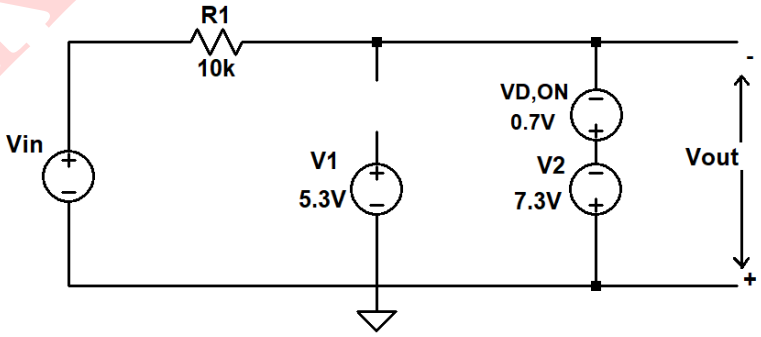

Figure 12: D1 is OFF and D2 is ON

$\therefore V_{out} = V_{D(ON)} + V_2 = 0.7 + 7.3$

$\therefore \mathbf{V_{out} = 8V}$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

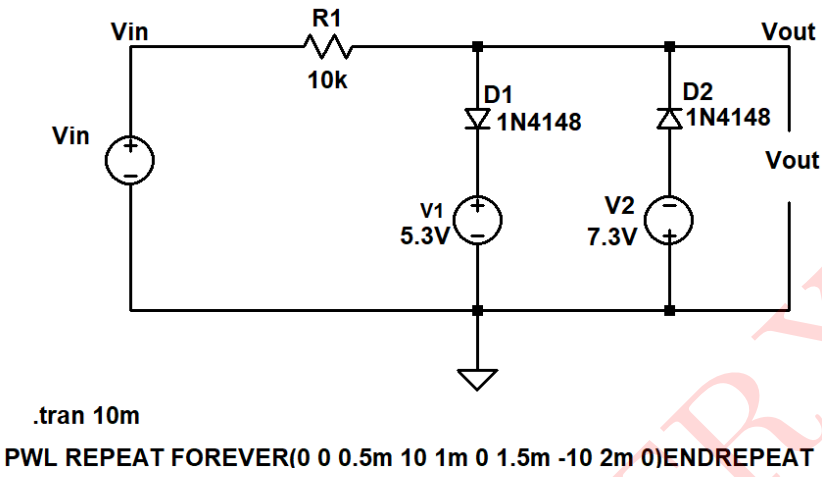

Figure 13: Circuit Schematic: Results

Input and Output waveforms are shown in figure 14:

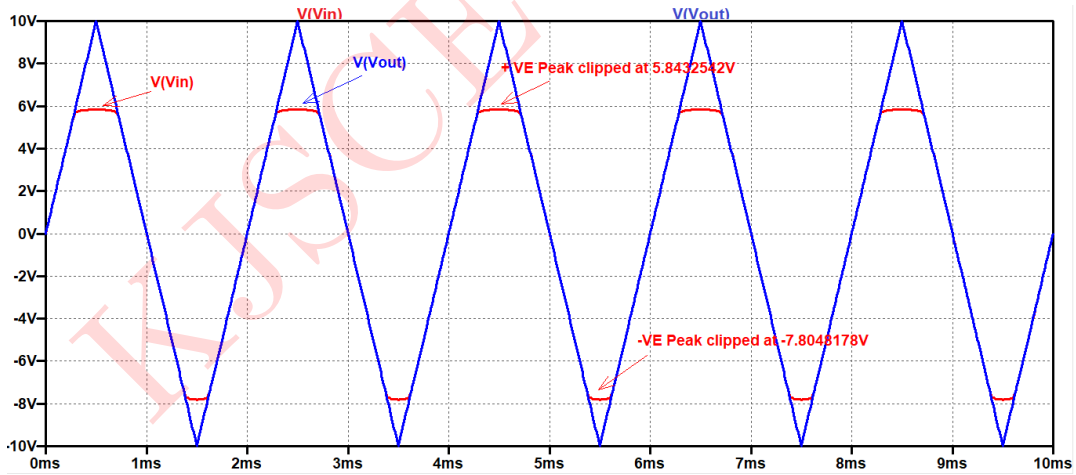

Figure 14: Input and output waveforms

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
For positive half cycle: V_{out} clipped level	6V	5.8438V
For negative half cycle: V_{out} clipped level	-8V	-7.8131V

Table 2: Question 2

Numerical 3:
For the circuit shown in figure 15, plot input waveform $V_{in}(t)$ and output waveform $V_{out}(t)$

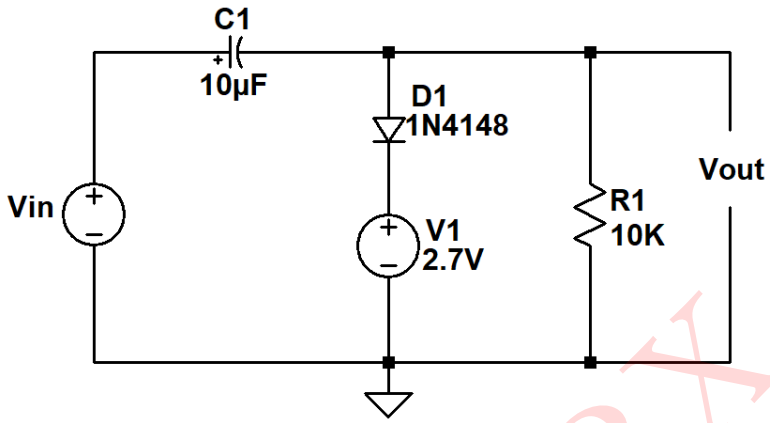

Figure 15: Circuit Diagram

Given: $V_{in}(t) = 10$ Vp-p square wave of frequency 1kHz, $C_1 = 10\mu F$, $R_1 = 10\text{k}\Omega$,
Diode D1 is Si diode i.e. $V_{D(ON)} = 0.7\text{V}$, $V_1 = 2.7\text{V}$
Figure 16 represents input waveform:

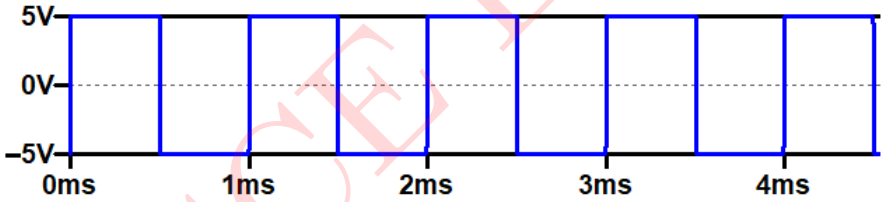

Figure 16: Input waveform

Solution:
Assumption: RC time constant is large enough than the time period of input signal large enough (than the time period of input signal) to ensure that voltage across capacitor does not discharge significantly during the period the diode is OFF.

Operations: 1. During the positive half cycle, the diode D1 is OFF
when $V_{in} < V_{D(ON)} + V_1$ i.e. when $V_{in} < 3V$
Since, diode D1 is reverse biased (cathode is more positive than anode by 0.7V)

The circuit reduces to as shown in figure 17:

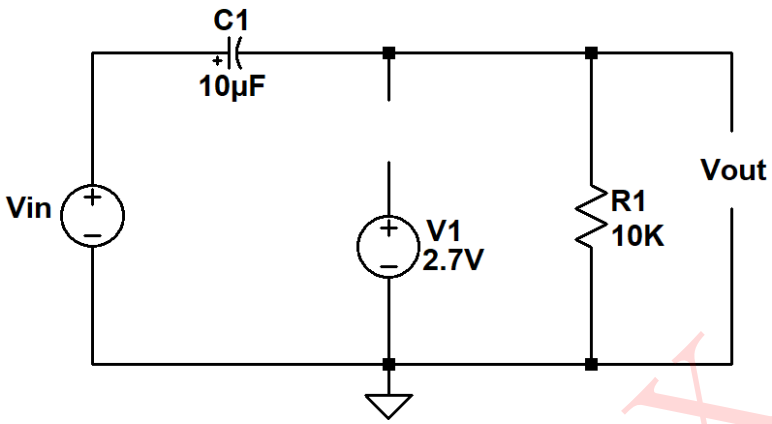

Figure 17: D1 is OFF

2. During the same positive half cycle, when $V_{in} > 3V$, diode D1 is ON as it is forward biased (anode is more positive than cathode by 0.7V)
The circuit reduces to as shown in figure 18:

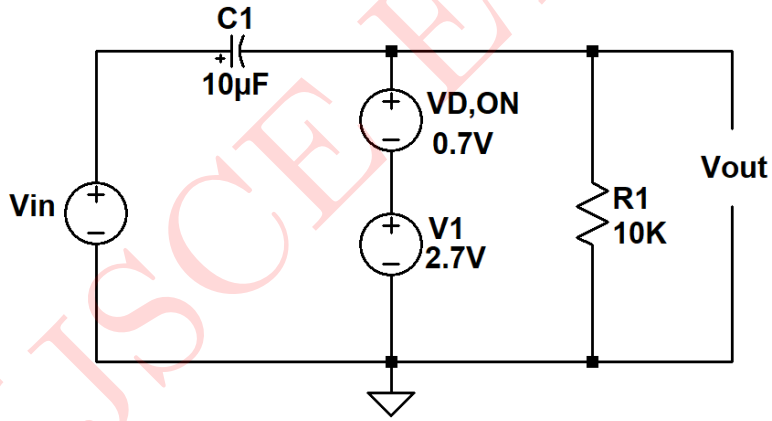

Figure 18: D1 is ON

$\therefore V_{out} = V_{D(ON)} + V_1 = 0.7 + 2.7$

$\therefore \mathbf{V_{out} = 3.4V}$

For the entire positive half cycle, the capacitor changes to voltage V_c given as:

$V_{in} - V_c - 0.7 - 2.7 = 0$

$\therefore V_c = V_m - 0.7 - 2.7$ ...($\because V_{in} = V_m$ for positive half cycle)

$\therefore V_c = 5 - 3 = \mathbf{2V}$

3. During the negative half cycle, diode D1 is OFF since it is reverse biased (cathode is more positive than anode by 0.7V). The circuit is shown in figure 19:

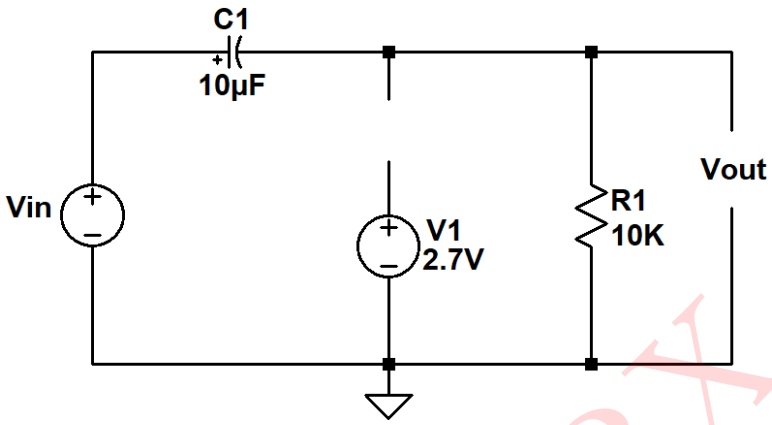

Figure 19: D1 is off

The capacitor C_1 acts like a battery having the charge $V_c = 2$V

Applying KVL, we get:

$V_{in} - V_c - V_{out} = 0$

For negative half cycle, $V_{in} = -V_m$

$\therefore -V_m - V_c - V_{out} = 0$

$\therefore V_{out} = -V_m - V_c$

$\therefore V_{out} = -5 - 2 = \mathbf{-7V}$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

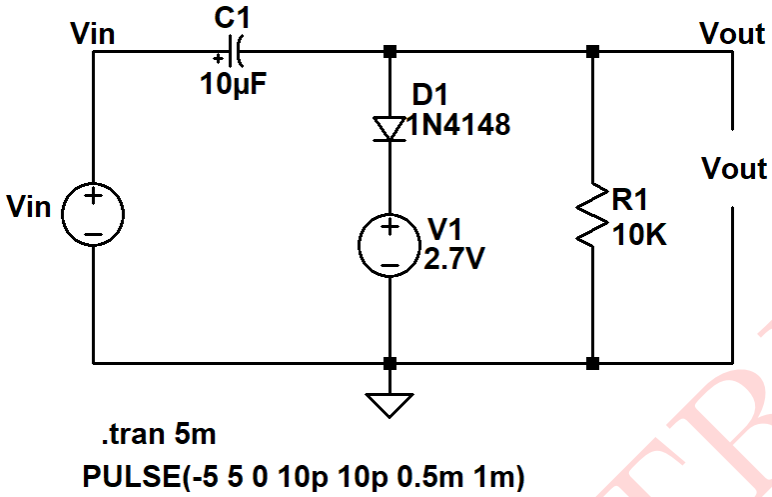

Figure 20: Circuit Schematic: Results

Input and Output waveforms are shown in figure 21:

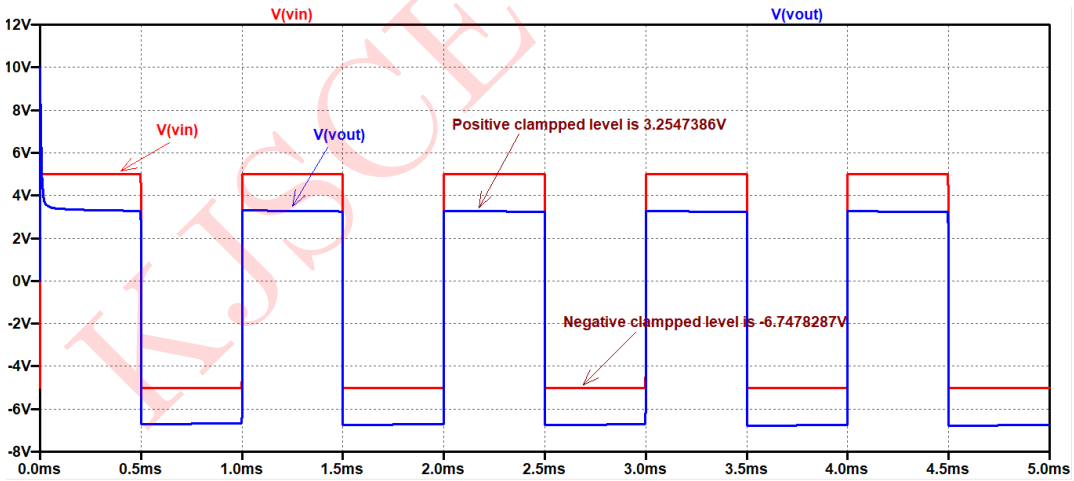

Figure 21: Input and output waveforms

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
Positive clamping voltage	3.4V	3.2557V
Negative clamping voltage	−7V	−6.7481V

Table 3: Question 3