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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Cascode Amplifier

Numerical 1: For the circuit shown in figure 1, Calculate 1^{st} and 2^{nd} stage DC parameters. Calculate voltage gain of 1^{st} and 2^{nd} stage and overall voltage gain in dB. Calculate input impedance, output impedance and output voltage.
Given: $\beta_1 = \beta_2 = 200$

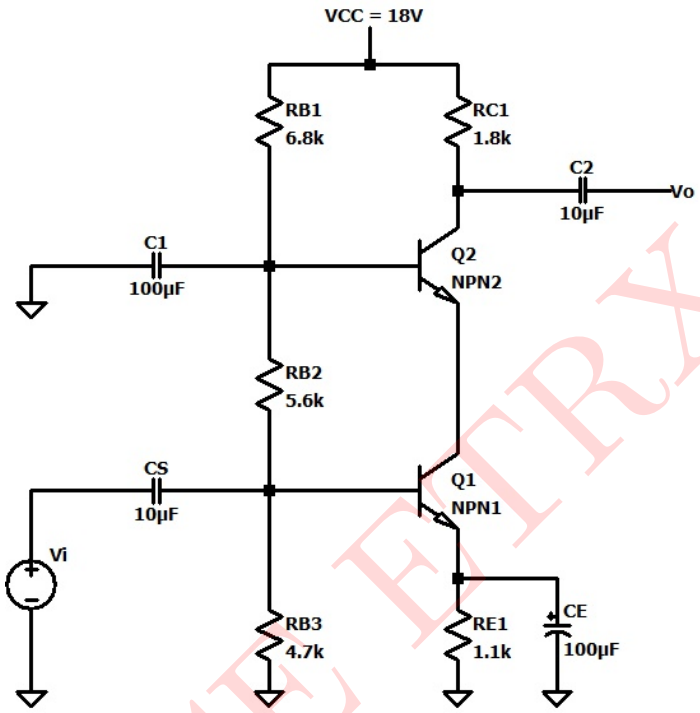

Figure 1: Circuit 1

Solution:

The given circuit 1 is a CE-CB cascade amplifier employing npn BJT.
For DC biasing, the capacitors acts as an open source.

DC Analysis:

$$V_{B_1} = \frac{R_{B_3}}{R_{B_1} + R_{B_2} + R_{B_3}} V_{CC} \quad \text{...(Voltage divider)}$$

$$V_{B_1} = \frac{4.7 \times 10^3}{6.8 \times 10^3 + 5.6 \times 10^3 + 4.7 \times 10^3} \times 18 = \mathbf{4.947\ V}$$

$$V_{B_2} = \frac{R_{B_2} + R_{B_3}}{R_{B_1} + R_{B_2} + R_{B_3}} V_{CC} \quad \text{...(Voltage divider)}$$

$$V_{B_2} = \frac{5.6 \times 10^3 + 4.7 \times 10^3}{6.8 \times 10^3 + 5.6 \times 10^3 + 4.7 \times 10^3} \times 18 = \mathbf{10.842\ V}$$

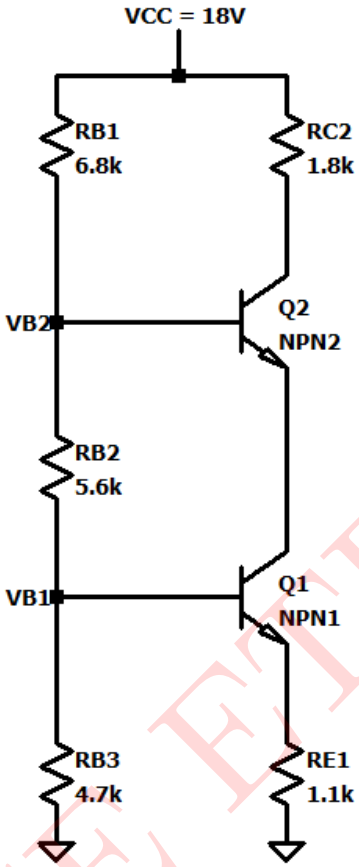

Figure 2: DC Equivalent circuit

Voltage across terminal E_1 can be given as,

$$V_{E_1} = V_{B_1} - V_{BE_1}$$
$$V_{E_1} = 4.947 - 0.7 = \mathbf{4.247\ V}$$

$$V_{E_2} = V_{B_2} - V_{BE_2}$$
$$V_{E_2} = 10.842 - 0.7 = \mathbf{10.142\ V}$$

V_{E_2} and V_{C_1} are connected to each other, so voltages are equal

$$V_{C_1} = V_{E_2} = \mathbf{10.142\ V}$$

$$I_{E_1} = \frac{V_{E_1}}{R_{E_1}}$$
$$I_{E_1} = \frac{4.947}{1.1} = \mathbf{3.86\ mA}$$

$$I_{B_1} = \frac{I_{E_1}}{1+\beta_1}$$
$$I_{B_1} = \frac{3.86 \times 10^{-3}}{1+200} = \mathbf{19.2\ \mu A}$$

$$I_{C_1} = \beta_1 I_{B_1}$$
$$I_{C_1} = 200 \times 19.2 \times 10^{-6} = \mathbf{3.84\ mA}$$

Terminal C_1 and terminal E_2 are connected together, so the current flowing through then will be same.

$$I_{E_2} = I_{C_1} = \mathbf{3.84\ mA}$$

$$I_{B_2} = \frac{I_{E_1}}{1+\beta_1}$$
$$I_{B_2} = \frac{3.84 \times 10^{-3}}{1+200} = \mathbf{19.1\ \mu A}$$

$$I_{C_2} = \beta I_{B_2}$$
$$I_{C_2} = 200 \times 19.1 \times 10^{-6} = \mathbf{3.82\ mA}$$

Voltage across terminal C_2 is given as,

$$V_{C_2} = V_{CC} - I_{C_2} R_{C_2}$$
$$V_{C_2} = 18 - 3.82 \times 10^{-3} \times 1.8 \times 10^{3} = \mathbf{11.124\ V}$$

AC Analysis:

Small signal parameters:

$$r_{\pi_1} = \frac{\beta_1 V_T}{I_{E_1}}$$
$$r_{\pi_1} = \frac{200 \times 26 \times 10^{-3}}{3.86 \times 10^{-3}} = \mathbf{1.347\ k\Omega}$$

$$r_{\pi_2} = \frac{\beta_2 V_T}{I_{E_2}}$$
$$r_{\pi_2} = \frac{200 \times 26 \times 10^{-3}}{3.84 \times 10^{-3}} = \mathbf{1.354\ k\Omega}$$

$$g_{m_1} = \frac{I_{C_1}}{V_T}$$
$$g_{m_1} = \frac{3.84 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{147.69\ mA/V}$$

$$g_{m_2} = \frac{I_{C_2}}{V_T}$$
$$g_m = \frac{3.82 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{146.92\ mA/V}$$

Small Signal Equivalent Circuit is shown in figure 4:

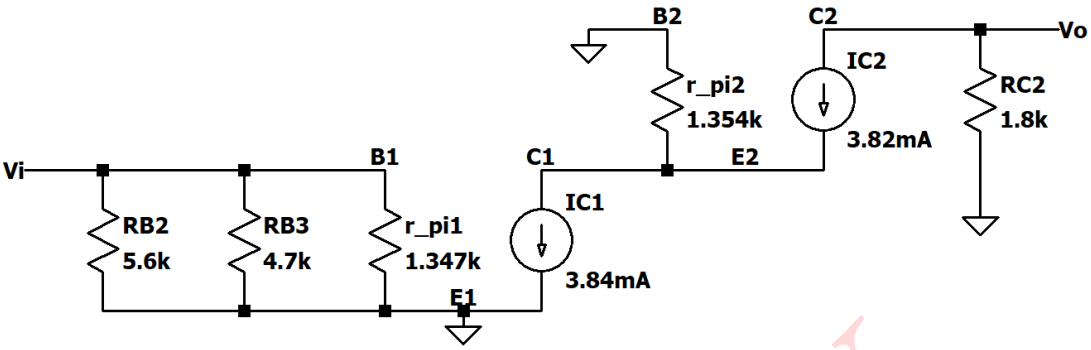

Figure 3: Small Signal Equivalent Circuit

Input impedance of stage 1:

$Z_i = (R_B \parallel r_{\pi_1})$

$Z_i = (R_{B_2} \parallel R_{B_3} \parallel r_{\pi_1})$

$Z_i = (5.6 \times 10^3 \parallel 4.7 \times 10^3 \parallel 1.347 \times 10^3) = \mathbf{882.045\ \Omega}$

Output impedance of stage 2:

$Z_o = R_{C_2} = \mathbf{1.8\ k\Omega}$

Stage 2 Voltage gain:

$$A_{V_2} = \frac{-g_{m_2} V_{\pi_2} (R_{C_2})}{V_{\pi_2}}$$

$A_{V_2} = -g_{m_2} R_{C_2}$

$A_{V_2} = -146.92 \times 10^{-3} \times 1.8 \times 10^3 = \mathbf{-264.456}$

Stage 1 voltage gain:

$$A_{V_1} = \frac{-g_{m_1} V_{\pi_1} \left(\frac{r_{\pi_2}}{1+\beta_2} \right)}{V_{\pi_1}}$$

$$A_{V_1} = -g_m \left(\frac{r_{\pi_2}}{1+\beta_2} \right)$$

$$A_{V_1} = -147.69 \times 10^{-3} \left(\frac{1.35 \times 10^3}{1+200} \right) = \mathbf{-0.994}$$

Overall voltage gain:

$A_{VT} = A_{V_1} \times A_{V_2}$

$A_{VT} = (-0.994) \times (-264.456) = \mathbf{262.869}$

A_{VT} in dB $= 20\log_{10}(|A_{VT}|)$

A_{VT} in dB $= 20\log_{10}(262.869) = \mathbf{48.3947\ dB}$

Output Voltage:

$V_o = A_{VT} V_i$

$V_o = 262.869 \times 5 \times 10^{-3} = \mathbf{1.314\ V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

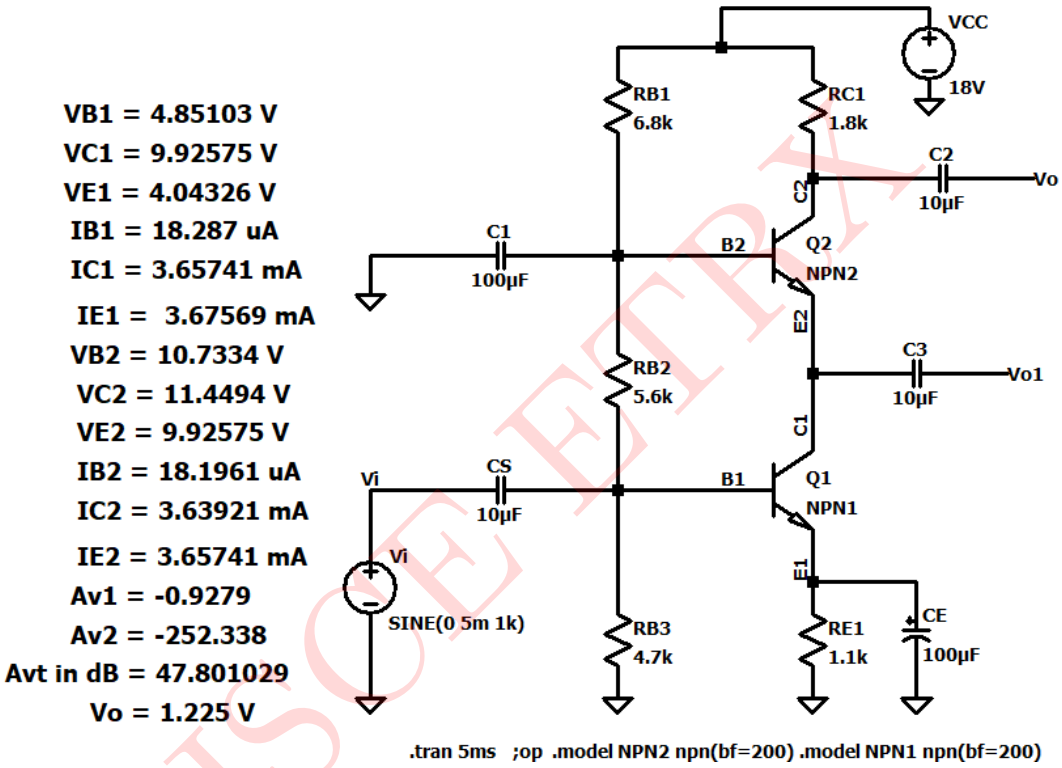

Figure 4: Circuit Schematic 1: Results

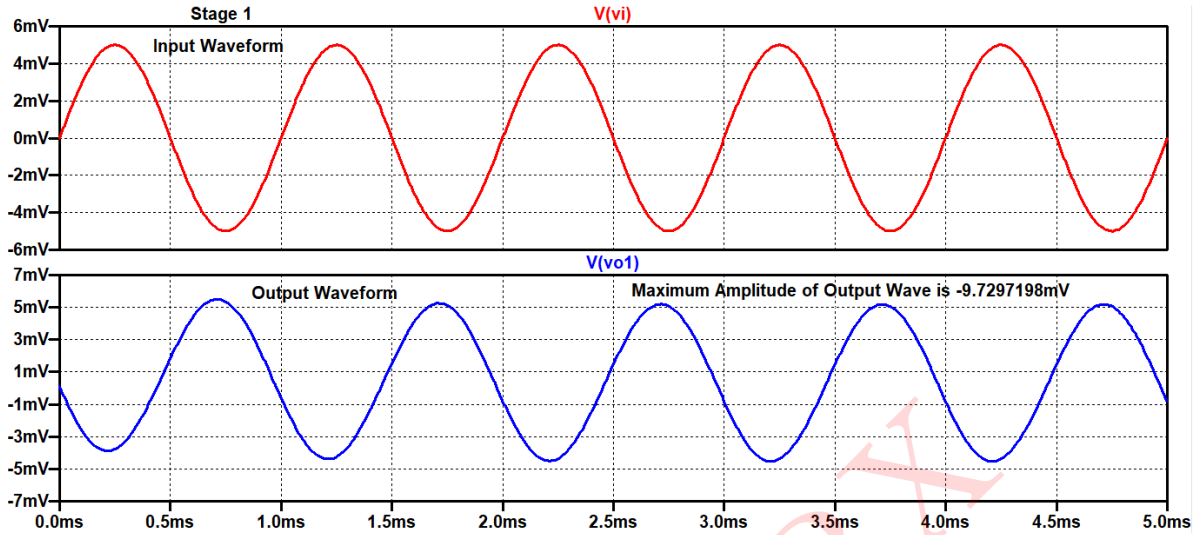

Figure 5: Input & Output waveforms for stage 1

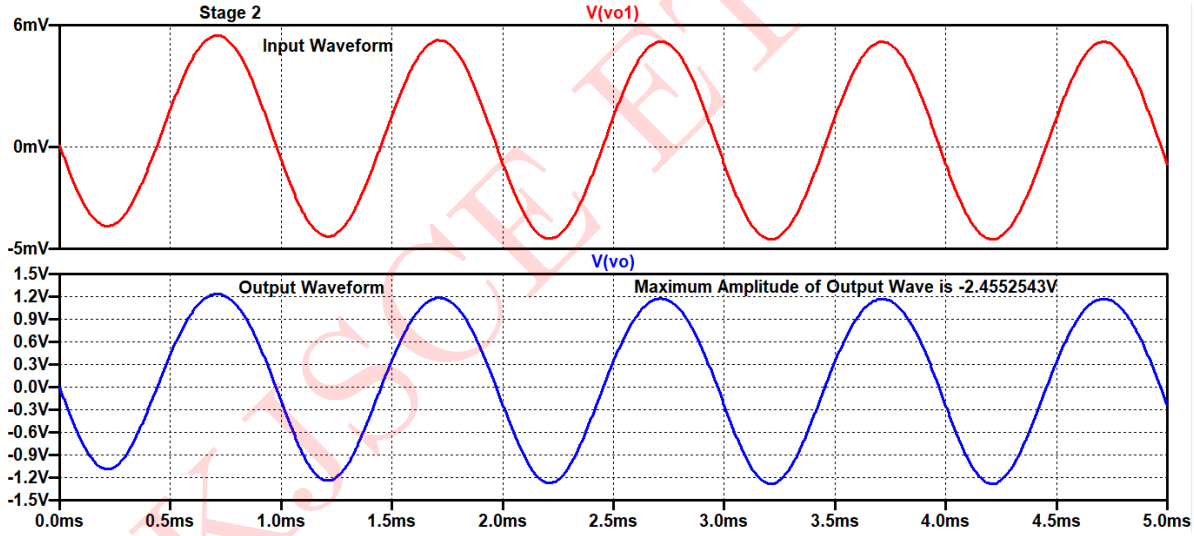

Figure 6: Input & Output waveforms for stage 2

Comparison of theoretical and simulated values:

Parameters	Theoretical Values	Simulated Values
I_{B_1}	19.2 μA	18.287 μA
I_{C_1}	3.84 mA	3.6574 μA
I_{E_1}	3.86 mA	3.6756 μA
I_{B_2}	19.1 μA	18.1961 μA
I_{C_2}	3.82 mA	3.6392 μA
I_{E_2}	3.84 mA	3.6571 μA
V_{C_1}	10.142 V	9.9257 V
V_{C_2}	11.124 V	11.4494 V
V_{E_1}	4.247 V	4.0432 V
V_{E_2}	10.142 V	9.9257 V
V_{B_1}	4.947 V	4.8510 V
V_{B_2}	10.842 V	10.7334 V
Voltage gain of stage 1: A_{V1}	-0.994	-0.9279
Voltage gain of stage 2: A_{V2}	-264.456	-252.338
Overall voltage gain: A_{VT} in dB	48.3947 dB	47.8010 dB
Input impedance of stage 1	882.045 Ω	–
Output impedance of stage 2	1.8 kΩ	–
Output Voltage	1.314 V	1.225 V

Table 1: Numerical 1

Numerical 2: The transistor parameters of the NMOS cascade circuit shown in figure 7 are, $V_{TN_1} = V_{TN_2} = 0.8$ V, $k_{n_1} = k_{n_2} = 3$ mA/V^2 and $\lambda_1 = \lambda_2 = 0$. Determine 1^{st} and 2^{nd} stage DC parameters. Determine 1^{st} and 2^{nd} stage voltage gain and overall voltage gain in dB. Calculate 1^{st} stage input impedance, 2^{nd} stage output impedance and output voltage.

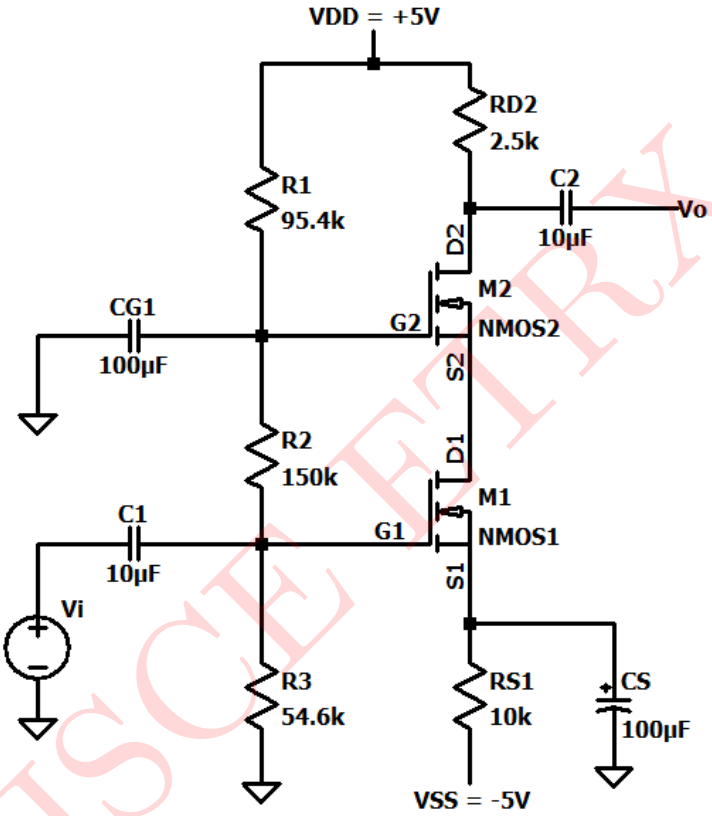

Figure 7: Circuit 2

Solution:

The given circuit 2 is a CS-CG cascade amplifier employing NMOS.

For DC biasing, the capacitors acts as an open source.

DC Analysis:

$$V_{G_1} = \frac{R_3}{R_1 + R_2 + R_3} V_{DD} \qquad \text{...(Voltage divider)}$$

$$V_{G_1} = \frac{54.6 \times 10^3 \times 5}{95.4 \times 10^3 + 150 \times 10^3 + 54.6 \times 10^3} = \mathbf{0.91\ V}$$

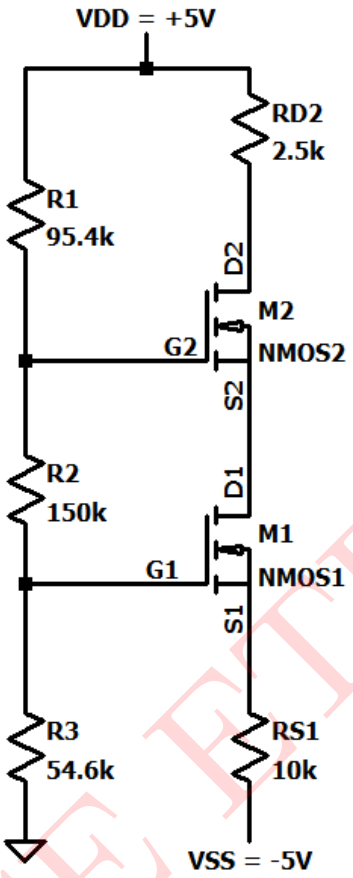

Figure 8: DC Equivalent circuit

$$V_{G_2} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} V_{DD}$$

$$V_{G_1} = \frac{150 \times 10^3 + 54.6 \times 10^3}{95.4 \times 10^3 + 150 \times 10^3 + 54.6 \times 10^3} \times 5 = \mathbf{3.41\ V}$$

Applying KVL to the gate source loop of the 1^{st} transistor,

$$V_G - V_{GS} - I_{D_1} R_S - V_{SS} = 0$$

$$I_{D_1} R_{S_1} = V_{G_1} - V_{GS_1} - V_{SS}$$

$$I_{D_1} = \frac{V_{G_1} - V_{GS_1} - V_{SS}}{R_{S_1}}$$

$$I_{D_1} = \frac{0.91 - V_{GS_1} + 5}{10 \times 10^3}$$

$$I_{D_1} = \frac{5.91 - V_{GS_1}}{10 \times 10^3}$$

From current equation,

$I_{D_1} = k_{n_1}(V_{GS_1} - V_{TN_1})^2$

$\frac{5.91 - V_{GS_1}}{10 \times 10^3} = 3 \times 10^{-3}(V_{GS_1} - 0.8)^2$

$5.91 - V_{GS_1} = 30(V_{GS_1}^2 - 1.6V_{GS_1} + 0.64)$

$5.91 - V_{GS_1} = 20V_{GS_1}^2 - 48V_{GS_1} + 19.2$

$30V_{GS_1}^2 - 47V_{GS_1} + 13.29 = 0$

$V_{GS_1} = \mathbf{1.196\ V}$ or $V_{GS_1} = \mathbf{0.37\ V}$

Let, $V_{GS_1} = 1.196$ V

$I_{D_1} = \frac{5.91 - 1.196}{10 \times 10^3} = \mathbf{0.471\ mA}$

Let, $V_{GS_1} = 0.37$ V

$I_{D_1} = \frac{5.91 - 0.37}{10 \times 10^3} = \mathbf{0.554\ mA}$

V_{GS_1} cannot be less than V_{TN} for NMOS,

$V_{GS_1} = \mathbf{1.196\ V}$

$I_{D_1} = \mathbf{0.471\ mA}$

As both the NMOS are identical,

$V_{GS_1} = V_{GS_2} = \mathbf{1.96\ V}$

Terminal D_1 is connected to S_2,

$I_{D_1} = I_{D_2} = \mathbf{0.471\ mA}$

Voltage across terminal S_2 can be given as,

$V_{S_2} = V_{G_2} - V_{GS_2}$

$V_{S_2} = 3.41 - 1.196 = \mathbf{2.214\ V}$

$V_{S_2} = V_{D_1} = \mathbf{2.214\ V}$

Voltage across terminal D_2 is given as,

$V_{D_2} = V_{DD} - I_{D_2}R_{D_2}$

$V_{D_2} = 5 - 0.471 \times 10^{-3} \times 2.5 \times 10^3 = \mathbf{3.822\ V}$

Voltage across terminal S_1 can be given as,

$V_{S_1} = V_{G_1} - V_{GS_1}$

$V_{S_1} = 0.91 - 1.196 = \mathbf{-0.286\ V}$

AC Analysis:

Small signal parameters:

$g_{m_1} = 2k_{n_1}(V_{GS_1} - V_{TN_1})$

$g_{m_1} = 2 \times 3 \times 10^{-3}(1.196 - 0.8) = \mathbf{2.376\ mA/V}$

$g_{m_2} = 2k_{n_2}(V_{GS_2} - V_{TN_2})$

$g_m = 2 \times 3 \times 10^{-3}(1.196 - 0.8) = \mathbf{2.376\ mA/V}$

Small Signal Equivalent Circuit is shown in figure 9:

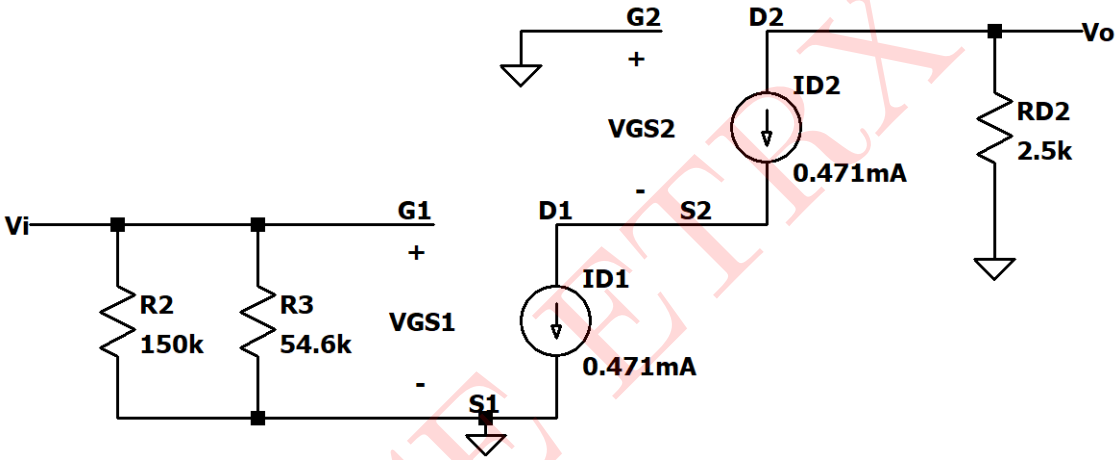

Figure 9: Small Signal Equivalent Circuit

Input impedance of stage 1:

$Z_i = R_G = (R_2 \ || \ R_3)$

$Z_i = (150 \times 10^3 \ || \ 54.6 \times 10^3) = \mathbf{40.029\ k\Omega}$

Output impedance of stage 2:

$Z_o = R_{D_2} = \mathbf{2.5\ k\Omega}$

Stage 2 Voltage gain:

$$A_{V_2} = \frac{-g_{m_2} V_{gs_2}(R_{D_2})}{-V_{gs_2}}$$

$A_{V_2} = g_{m_2} R_{D_2}$

$A_{V_2} = 2.376 \times 10^{-3} \times 2.5 \times 10^3 = \mathbf{5.94}$

Stage 1 voltage gain:

$$A_{V_1} = \frac{-g_{m_1} V_{gs_1} \left(\frac{1}{g_{m_2}}\right)}{V_{gs_1}} = -1 \qquad \ldots(\because g_{m_1} = g_{m_2})$$

Overall voltage gain:

$A_{VT} = A_{V_1} \times A_{V_2}$

$A_{VT} = (-1) \times (5.94) = \mathbf{-5.94}$

A_{VT} in dB $= 20\log_{10}(|A_{VT}|)$

A_{VT} in dB $= 20\log_{10}(5.94) = \mathbf{15.4757\ dB}$

Output Voltage:

$V_o = A_{VT}V_i$

$V_o = -5.94 \times 10 \times 10^{-3} = \mathbf{-0.0594\ V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

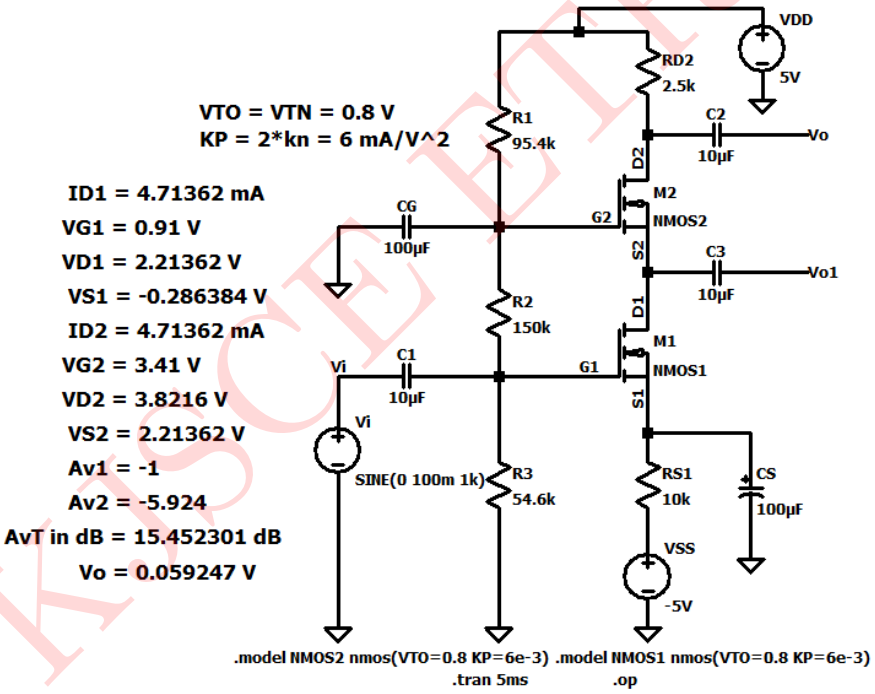

Figure 10: Circuit Schematic 2: Results

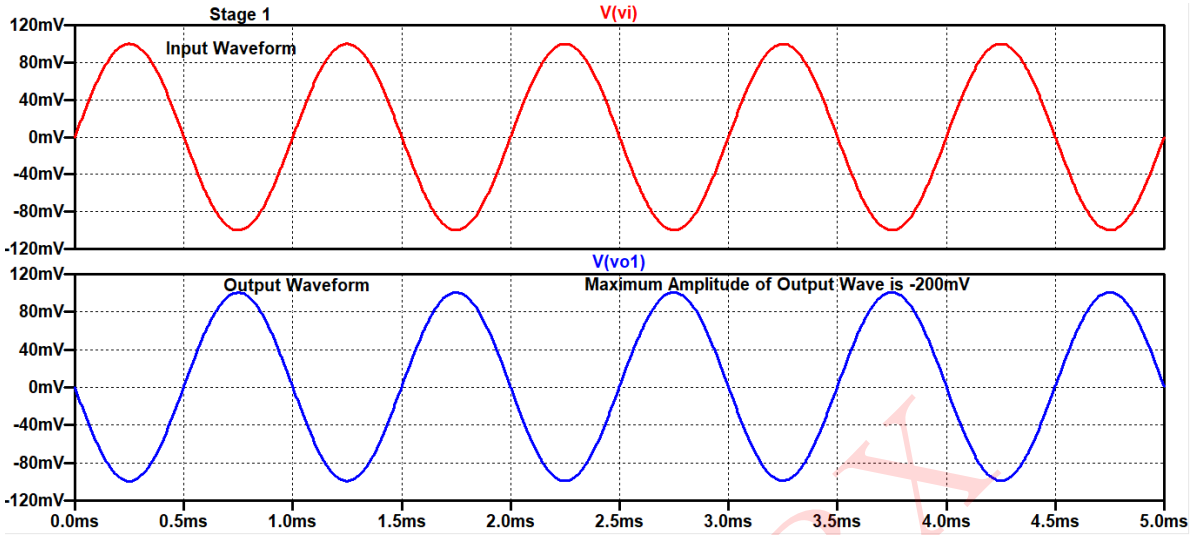

Figure 11: Input & Output waveforms for stage 1

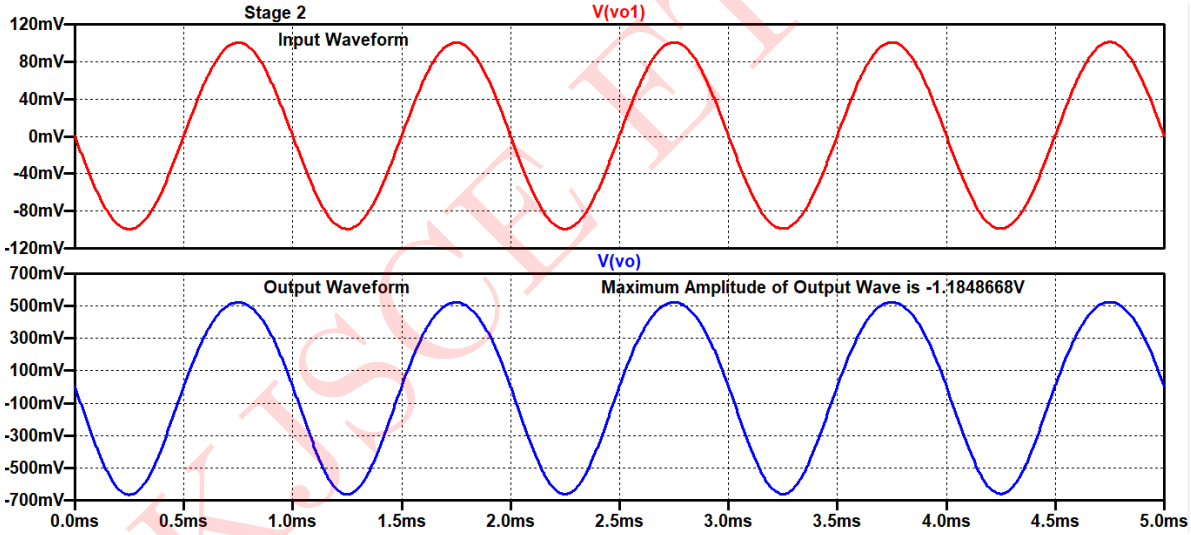

Figure 12: Input & Output waveforms for stage 2

Comparison of theoretical and simulated values:

Parameters	Theoretical Values	Simulated Values
I_{D_1}	0.471 mA	0.4713 mA
V_{G_1}	0.91 V	0.91 V
V_{D_1}	2.214 V	2.2136 V
V_{S_1}	−0.286 V	−0.2863 V
I_{D_2}	0.471 mA	0.4713 mA
V_{G_2}	3.41 V	3.41 V
V_{D_2}	3.822 V	3.8216 V
V_{S_2}	2.214 V	2.2136 V
Voltage gain of stage 1: A_{V1}	−1	−1
Voltage gain of stage 2: A_{V2}	5.94	5.924
Overall voltage gain: A_{VT} in dB	15.4757 dB	15.4523 dB
Input impedance of stage 1	40.029 kΩ	–
Output impedance of stage 2	2.5 kΩ	–
Output Voltage	−0.0594 V	−0.05924 V

Table 2: Numerical 2

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