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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Single Stage FET Amplifier

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Numerical

1. For the network shown in figure 1

a) Find V_{GSQ} , I_{DQ} , V_{DS}

b) Find A_v , R_i , R_o

Given: $R_G = 1\text{M}\Omega$, $R_D = 1.8\text{k}\Omega$, $R_S = 240\Omega$, $V_{DD} = 12\text{V}$, $R_L = 10\text{k}\Omega$, $r_d = 50\text{k}\Omega$,
 $V_P = -3\text{V}$, $I_{DSS} = 8\text{mA}$, $C_{C1} = C_{C2} = 10\mu\text{F}$

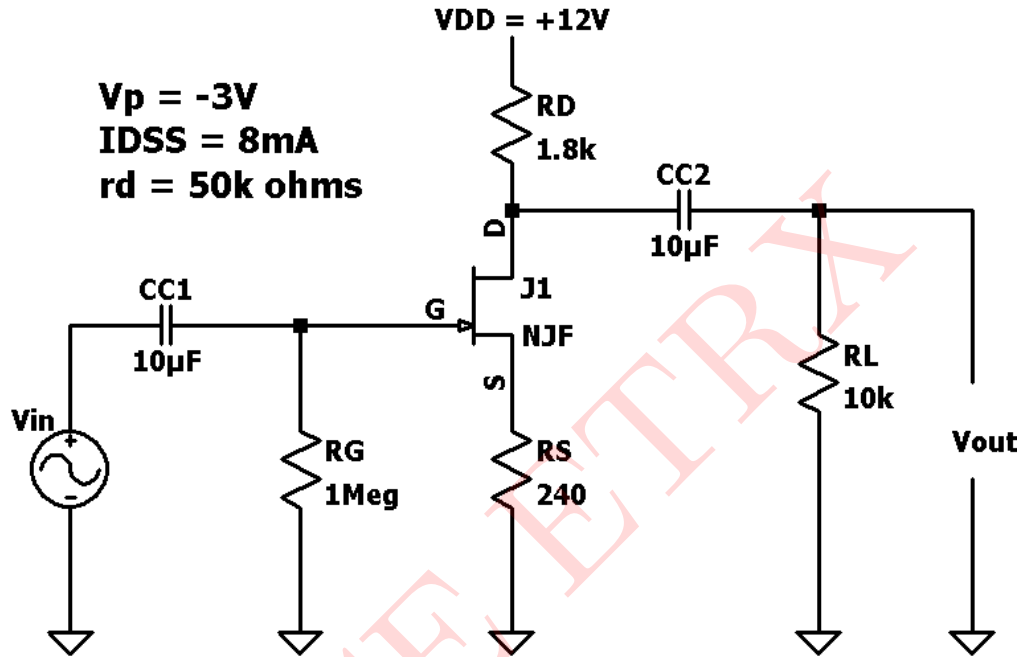


Figure 1: Circuit 1

Solution:

The above circuit is a self biased JFET amplifier

DC Analysis:

Assuming JFET is working in saturation region, $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$

also,

$$V_G = 0$$

$$V_S = I_D R_S$$

$$V_{GS} = -I_D R_S$$

$$V_{GS} = -I_D (240) \text{ ——— (1)}$$

$$I_D = 8 \times 10^3 \left(1 + \frac{V_{GS}}{3}\right)^2 \text{ ——— (2)}$$

Solving Equations (1) and (2)

$$V_{GS} = -8 \times 10^{-3} \times 240 \left(1 + \frac{2V_{GS}}{3} + \frac{(V_{GS})^2}{9} \right)$$

$$V_{GS} = -1.92 \left(1 + \frac{2V_{GS}}{3} + \frac{(V_{GS})^2}{9} \right)$$

$$V_{GS} = -1.92 - 1.28V_{GS} - 0.2133(V_{GS})^2$$

$$0.2133(V_{GS})^2 + 2.28V_{GS} + 1.92 = 0$$

$$V_{GS} = -0.9215V \text{ or } -9.76V$$

$$V_{GS} = -\mathbf{0.9215V} \quad \because (V_{GS} > V_P)$$

$$I_D = 8 \times 10^{-3} \left(1 - \frac{0.9215}{3} \right)^2$$

$$I_{DQ} = \mathbf{3.849 \text{ mA}}$$

Applying KVL to the drain source loop:

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$V_{DS} = 12 - (3.840 \times 1.8) - (3.84 \times 240)$$

$$V_{DS} = \mathbf{4.1664V}$$

Small signal parameters:

$$g_m = \frac{2I_{DSS}}{|V_P|} \left(1 - \frac{V_{GS}}{V_P} \right)$$

$$g_m = \frac{2 \times 8 \times 10^{-3}}{3} \left(1 - \frac{-0.9215}{-3} \right)$$

$$g_m = \mathbf{3.6951 \text{ mA/V}}$$

Small signal equivalent circuit:

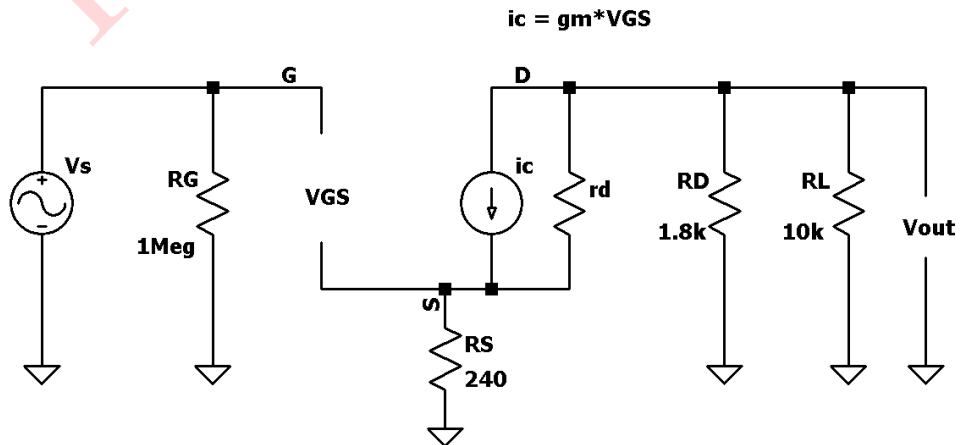


Figure 2: Small signal equivalent circuit

Input Resistance (R_i) = $1\text{M}\Omega$

Output Resistance (R_o) = $R_D \parallel r_d \parallel R_L$

Output Resistance (R_o) = $1.8 \times 10^3 \parallel 50 \times 10^3 \parallel 10 \times 10^3$

Output Resistance (R_o) = $1.48 \text{ k}\Omega$

Voltage Gain (A_v) = $\frac{-(R_D \parallel r_o \parallel R_S)}{\frac{1}{g_m} + R_S}$

$$A_v = \frac{-11.48 \times 10^3}{\frac{1}{3.695} + 240}$$

$$A_v = -2.898$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows

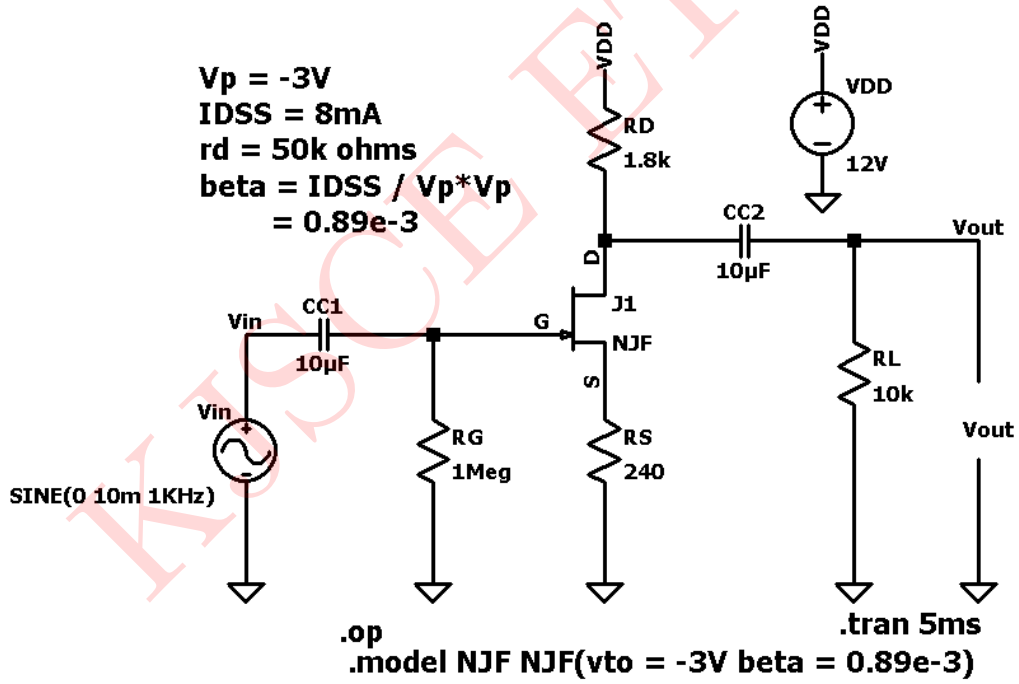


Figure 3: Circuit Schematic

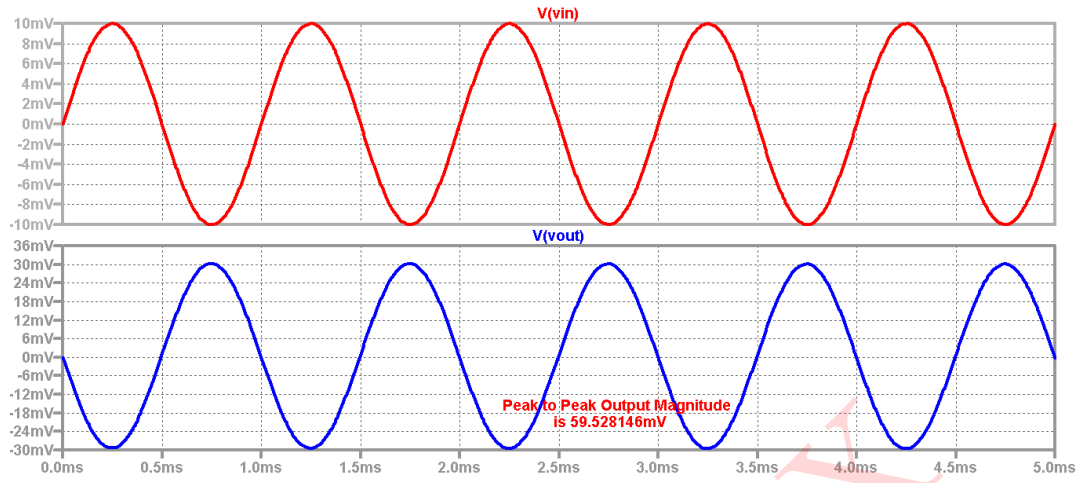


Figure 4: Input Output Waveform

Comparsion between simulated and theoretical values :

Parameters	Simulated	Theoretical
I_{DQ}	3.842mA	3.840mA
V_{GSQ}	-0.9221V	-0.9215
V_{DSQ}	4.1615V	4.1664V
A_v	-2.976	-2.898

Table 1: Numerical 1

2. For the network shown in figure 5

Find Z_i , Z_o , V_{out}

Given: $R_1 = 40\text{M}\Omega$, $R_2 = 10\text{M}\Omega$, $R_S = 1.2\text{k}\Omega$, $V_{DD} = 12\text{V}$, $R_D = 3.3\text{k}\Omega$, $r_d = 40\text{k}\Omega$, $V_{DD} = 30\text{V}$, $V_{GS(th)} = 3\text{V}$, $C_{C1} = C_{C2} = 22\mu\text{F}$, $C_S = 100\mu\text{F}$, $k_n = 0.4 \times 10^{-3}\text{mA/V}^2$

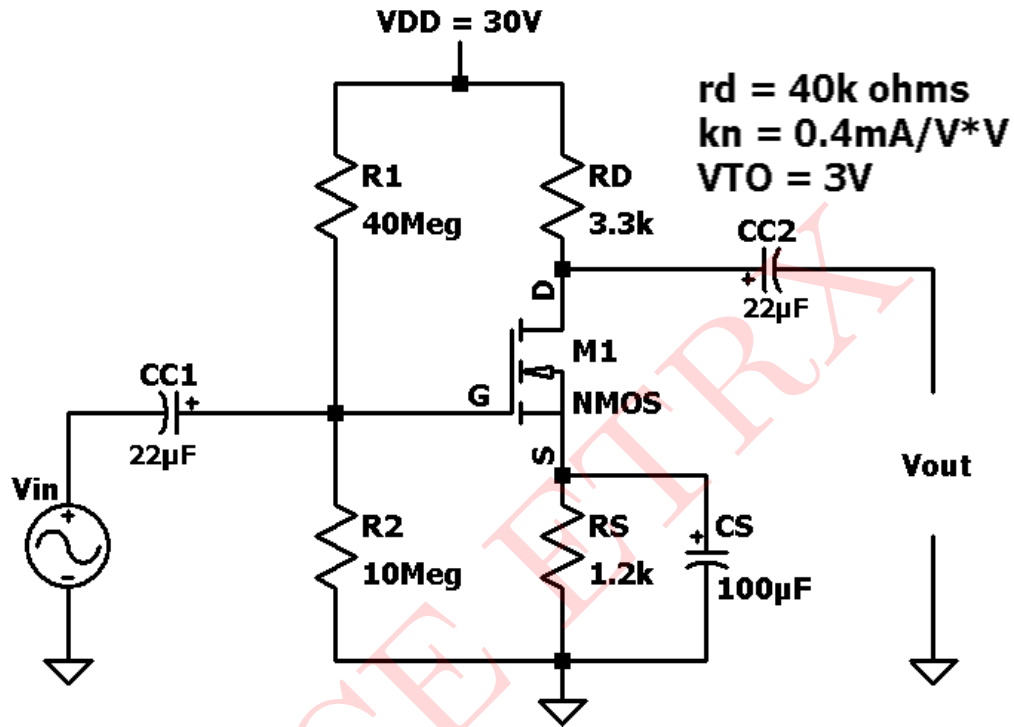


Figure 5: Circuit 2

Solution:

The above circuit is NMOS - CS amplifier

DC Analysis:

Assuming JFET is working in saturation region

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$$

$$V_G = \frac{10}{40 + 10} \times 30$$

$$V_G = 6\text{V}$$

$$V_{GS} = V_G - V_S$$

$$\therefore V_S = I_D R_S$$

$$V_{GS} = 6 - I_D R_S$$

$$V_{GS} = 6 - I_D(1.2 \times 10^3) \text{ ——— (1)}$$

Assuming given NMOS is in Saturation region

$$I_D = k_n(V_{GS} - V_{GS(th)})^2$$

$$I_D = 0.4 \times 10^{-3}(V_{GS} - 3)^2 \text{ ——— (2)}$$

Solving equation (1) and (2)

$$V_{GS} = 6 - (1.2 \times 10^3 \times 0.4 \times 10^{-3})((V_{GS})^2 - 6V_{GS} + 9)$$

$$V_{GS} = 6 - 0.48V_{GS}^2 + 2.88V_{GS} - 4.32$$

$$0.48V_{GS}^2 - 1.88V_{GS} - 1.68 = 0 \quad V_{GS} = 4.667V \text{ or } -0.75V$$

$$V_{GS} = \mathbf{4.667V} \quad \because (V_{GS} > V_{TH})$$

$$I_{DQ} = 0.4 \times 10^{-3}(4.667 - 3)^2$$

$$I_{DQ} = \mathbf{1.111mA}$$

Small signal parameters:

$$g_m = 2k_n(V_{GS} - V_{GS(th)})$$

$$g_m = 2 \times 0.4 \times 10^{-3}(4.667 - 3)$$

$$g_m = \mathbf{1.3336 \text{ mA/V}}$$

$$r_d = \mathbf{40 \text{ k}\Omega} \text{ (Given)}$$

Small signal equivalent circuit:

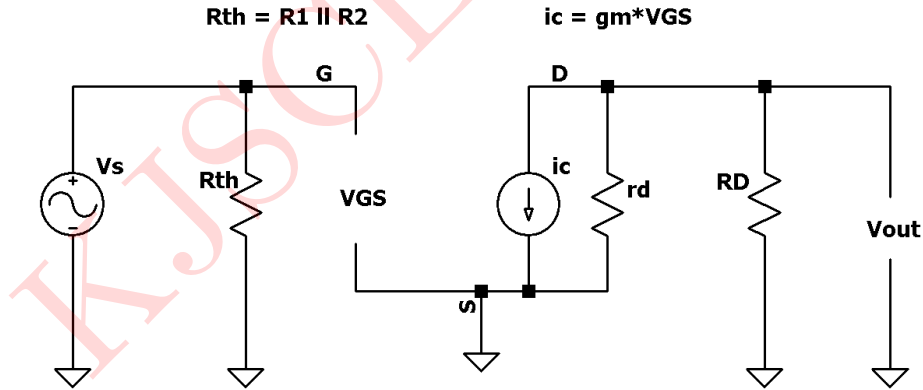


Figure 6: Small signal equivalent circuit

$$Z_i = R_1 || R_2 = 40 \times 10^6 || 10 \times 10^6$$

$$Z_i = \mathbf{8M\Omega}$$

$$Z_o = r_d || R_D = 40 \times 10^3 || 3.3 \times 10^3$$

$$Z_o = \mathbf{3048.498 \Omega}$$

$$A_v = -gm(r_o || R_D)$$

$$A_v = -1.3336 \times (40 \times 10^3 || 3.3 \times 10^3)$$

$$A_v = \mathbf{-4.0654} \text{ (Negative sign indicates 180° out of phase between input and output)}$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows

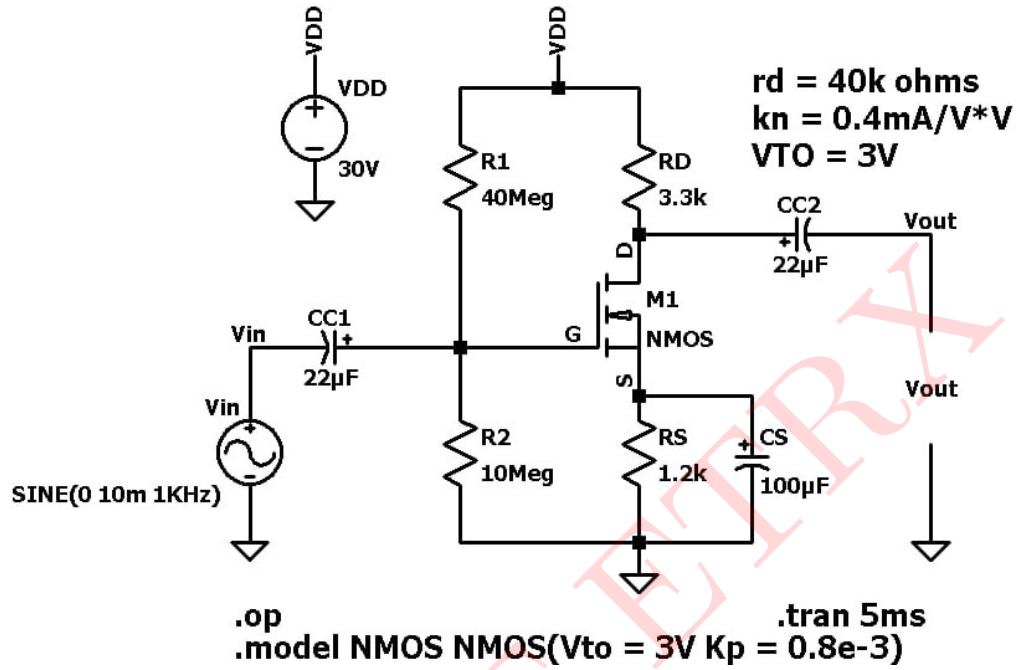


Figure 7: Circuit Schematic

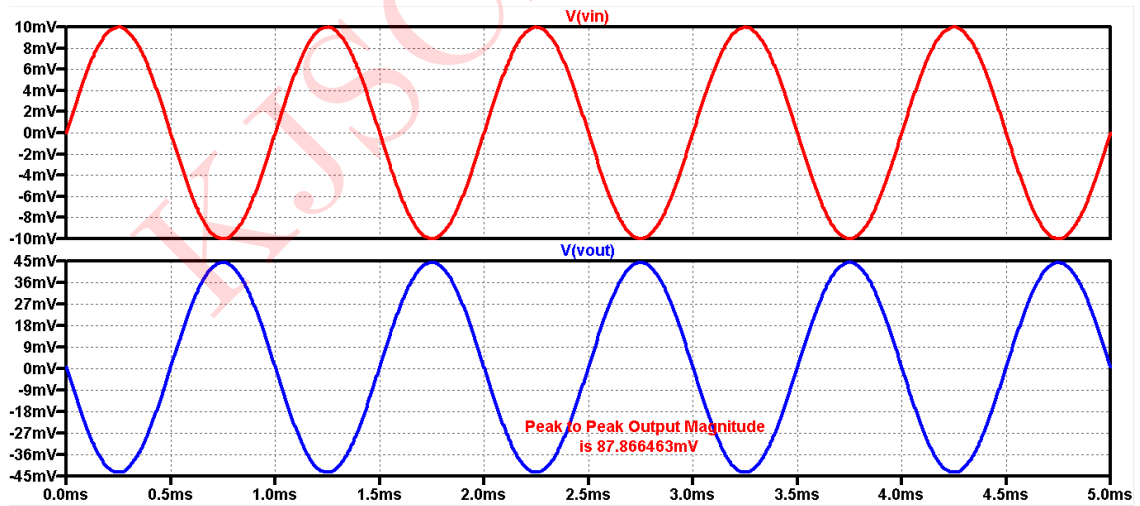


Figure 8: Input Output Waveform

Comparsion between simulated and theoretical values :

Parameters	Simulated	Theoretical
I_{DQ}	1.111mA	1.111mA
V_{GSQ}	4.667V	4.667V
A_v	-4.393	-4.0654

Table 2: Numerical 2

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