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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
DC BIASING CIRCUITS

6^{th} **June, 2020** **Numerical**

1. For the network shown in Figure 1 below: a) Determine I_{CQ}, V_{CEQ} b) Find V_B, V_C, V_E and V_{BC}. Given, $\beta = 120$

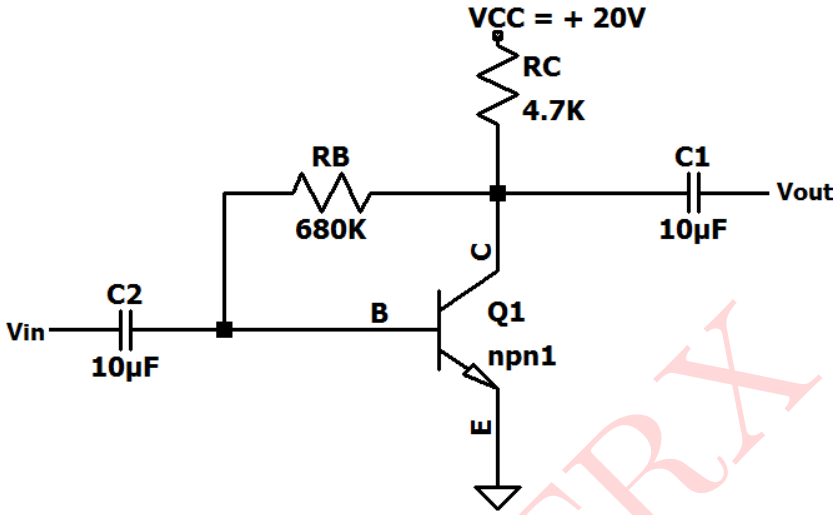

Figure 1: Circuit 1

Solution: In DC analysis, the capacitors act as open circuit.

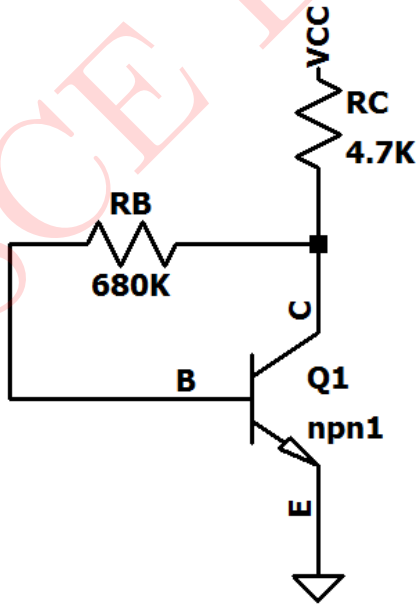

Figure 2: DC equivalent circuit

Since, f = 0, $\quad \therefore X_c = \dfrac{1}{2\pi f_c} = \infty$

Applying KVL to the input base-emitter loop

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$

$$I_B = \frac{20V - 0.7V}{680k\Omega + (120)(4.7k\Omega)} = \frac{19.3V}{1.244M\Omega} \qquad (V_{BE} = 0.7 \text{ V})$$

$$\therefore I_B = 15.51\mu A$$

$$I_{CQ} = \beta I_B = 120 \times 15.51\mu A$$

$$\therefore I_{CQ} = \mathbf{1.86\ mA}$$

Applying KVL to the output common emitter loop

$$V_{CEQ} = V_{CC} - I_C R_C$$

$$V_{CEQ} = 20V - 1.86mA \times 4.7k\Omega$$

$$V_{CEQ} = \mathbf{11.26\ V}$$

$$V_B = V_{BE} = \mathbf{0.7\ V} \qquad (\text{Since } V_{EE} = 0)$$

$$V_{CE} = V_{CEQ} = 11.26 \text{ V}$$

$$\therefore V_C = \mathbf{11.26\ V} \qquad (V_E = \mathbf{0\ V})$$

$$V_{BC} = V_B - V_C = 0.7 \text{ V} - 11.26 \text{ V}$$

$$V_{BC} = \mathbf{-10.56\ V}$$

SIMULATED RESULTS:
Above circuit is simulated using LTspice and the results are presented below:

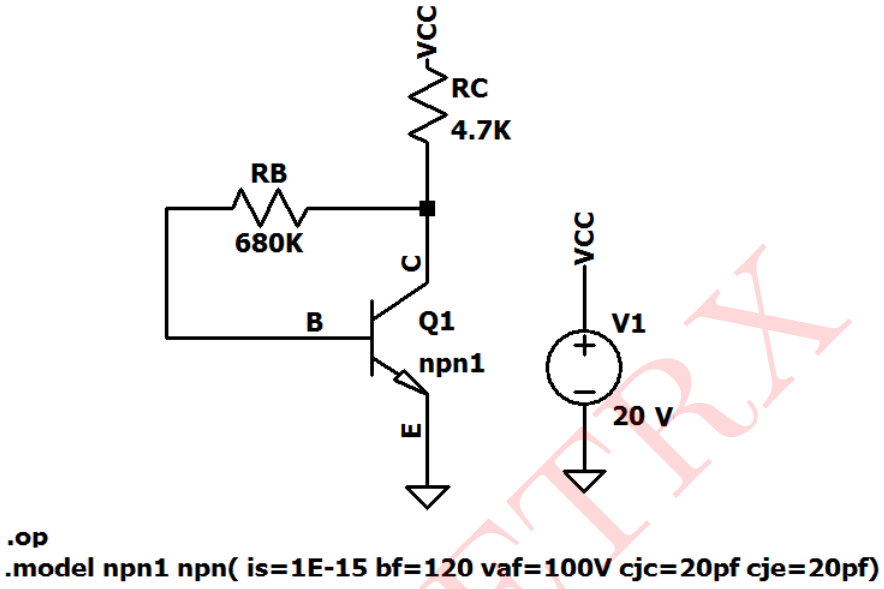

Figure 3: Circuit schematic: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
I_B	15.51 μA	14.47 μA
I_C	1.86 mA	1.949 mA
V_C	11.26 V	10.768 V
V_B	0.7 V	0.729 V
V_E	0 V	0 V

Table 1: Numerical 1

2. Determine the voltage V_{CB} and the current I_B for the common base configuration of Figure 4 given below. given that $\beta = 60$

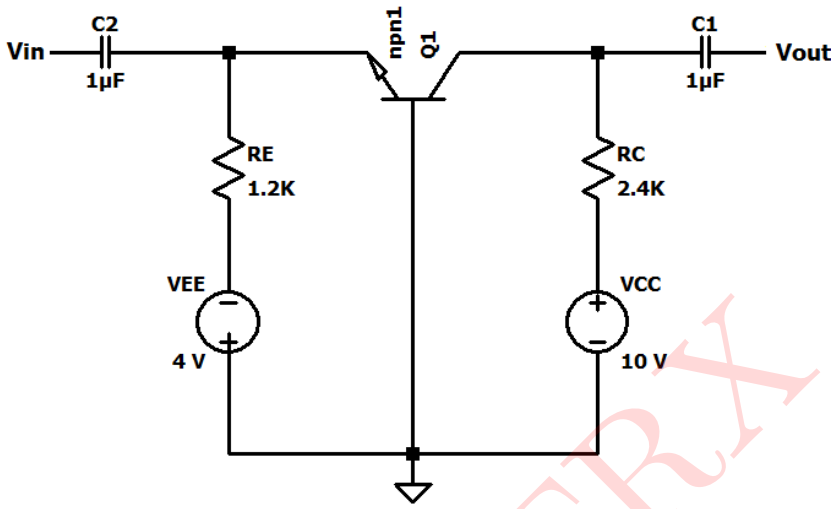

Figure 4: Circuit 2

Solution :
In DC analysis, the capacitors act as open circuit.

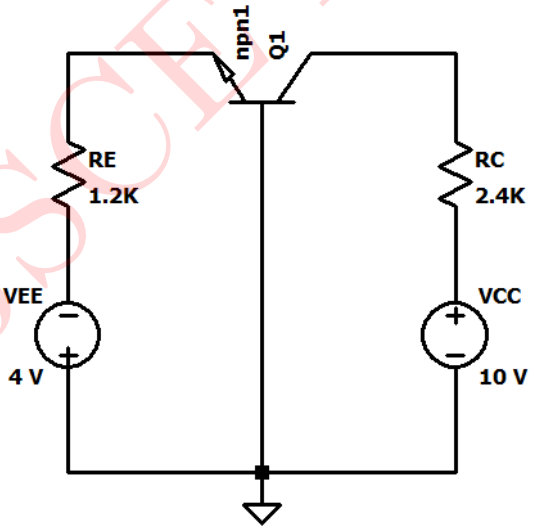

Figure 5: DC equivalent circuit

Since, f = 0, $\quad \therefore X_c = \dfrac{1}{2\pi f_c} = \infty$

Applying KVL to the input base-emitter loop

$-V_{EE} + I_E R_E + V_{BE} = 0$

$\therefore I_E = \dfrac{V_{EE} - V_{BE}}{R_E}$

Substituting values:

$$I_E = \frac{4V - 0.7V}{1.2k\Omega} = 2.75\text{mA}$$

Applying KVL to the output circuit gives

$$-V_{CB} + I_C R_C - V_{CC} = 0$$

$$V_{CB} = V_{CC} - I_C R_C \text{ with } I_C \approx I_E$$

$$V_{CB} = 10V - 2.75mA \times 2.4k\Omega$$

$$V_{CB} = \mathbf{3.4V}$$

$$I_B = \frac{I_C}{\beta}$$

$$I_B = \frac{2.75mA}{60}$$

$$I_B = \mathbf{45.8\ \mu A}$$

SIMULATED RESULTS:

Above circuit is simulated using LTSpice and the results are presented below

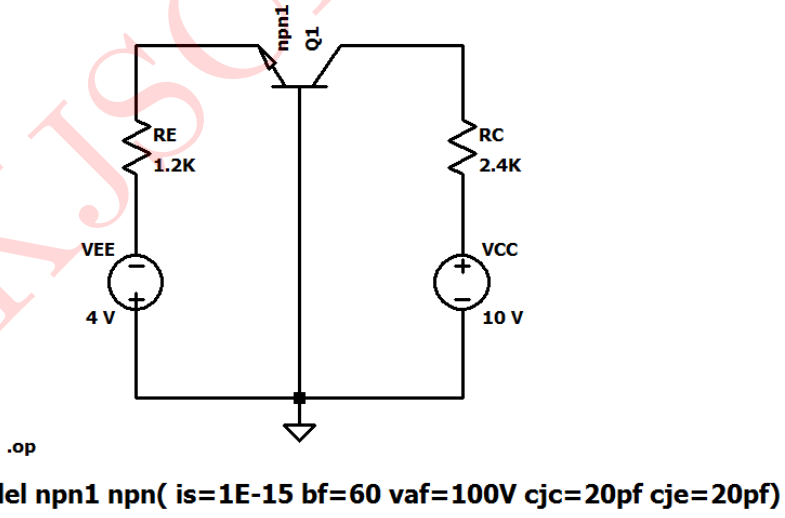

Figure 6: Circuit schematic: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
I_B	45.8 μA	43.0305 μA
I_E	2.75 mA	2.717 mA

Table 2: Numerical 2

3. Determine I_B, I_C, V_{CE} and stability factor for the circuit shown in Figure 7. Given, $\beta = 100$.

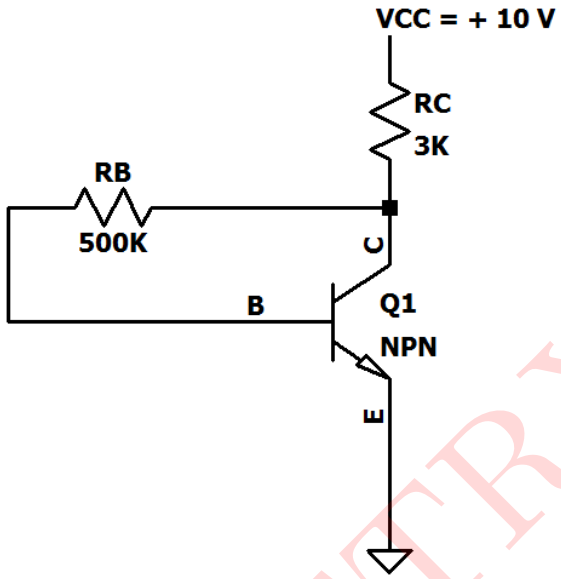

Figure 7: Circuit 3

Solution:
The above circuit is a self-bias circuit.

Applying KVL to the input base-emitter loop:

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - (\beta + 1)I_B R_C - I_B R_B - V_{BE} = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{(\beta + 1)R_C}$$

$$I_B = \frac{10 - 0.7}{500 \times 10^3 + 101 \times 3 \times 10^3}$$

$$\therefore I_B = \mathbf{11.58\mu A}$$

$$I_{CQ} = \beta I_B = 100 \times 11.58\mu A$$

$$\therefore I_{CQ} = \mathbf{1.158\ mA}$$

Applying KVL to the output common emitter loop:

$$V_C = V_{CC} - (I_B + I_C)R_C$$

$$V_C = 10 - (11.58 \times 10^{-6} + 1.158 \times 10^{-3)3} \times 10^3$$

$$\therefore V_C = 6.49\ \text{V}$$

$$V_E = (I_B + I_C)R_E$$

$V_E = (I_B + I_C) \times 0 \qquad$ (Since $R_E = 0 \quad \Omega$)

$V_{CE} = V_C - V_E = 6.49 - 0$

$\therefore V_{CE} =$ **6.49 V**

Stability factor:

$$\mathrm{S} = \frac{\beta + 1}{1 + \beta\left(\frac{R_C}{R_C + R_B}\right)}$$

$$\therefore S = \frac{100 + 1}{1 + \left(\frac{100 \times 3 \times 10^3}{500 \times 10^3 + 3 \times 10^3}\right)}$$

$\therefore S =$ **63.26**

SIMULATED RESULTS:

Above circuit is simulated using LTspice and the results are presented below:

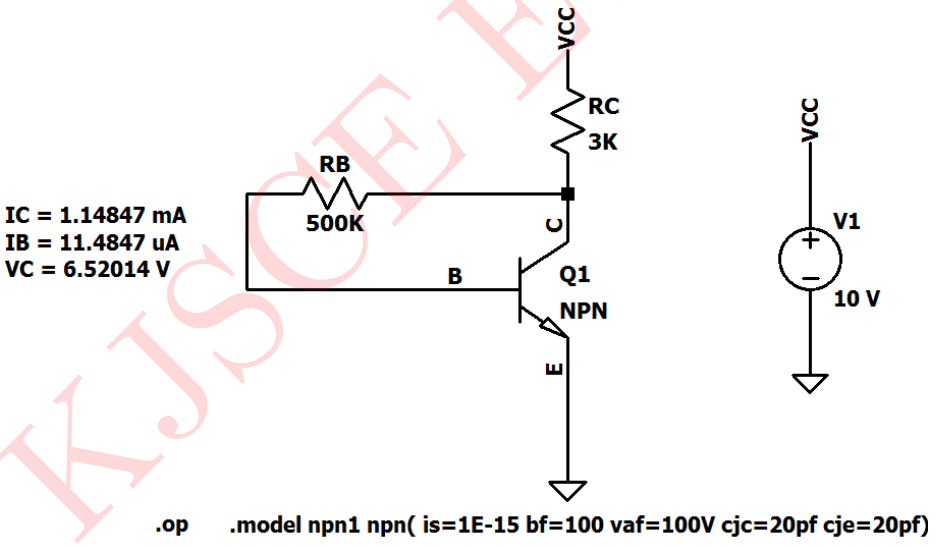

Figure 8: Circuit schematic: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
I_B	11.58 μA	11.4847 μA
I_C	1.158 mA	1.14847 mA
V_C	6.49 V	6.52 V

Table 3: Numerical 3

4. For the circuit shown in Figure 9, find I_C, V_{CE} and stability factor. Given, $\beta = 120$

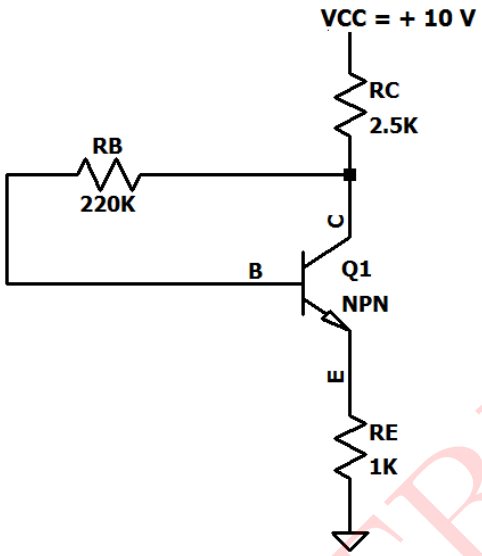

Figure 9: Circuit 4

Solution:

The above configuration is collector to base bias.

Applying KVL to the input base-emitter loop:

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} - (I_B + I_C)R_E = 0$$

$$V_{CC} - (\beta + 1)I_B R_C - I_B R_B - V_{BE} - (\beta + 1)I_B R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)(R_C + R_E)}$$

$$I_B = \frac{10 - 0.7}{220 \times 10^3 + 101 \times (2.5 + 1) \times 10^3}$$

$$\therefore I_B = 16.21\mu A$$

$$I_{CQ} = \beta I_B = 100 \times 16.21\mu A$$

$$\therefore I_{CQ} = \mathbf{1.621\ mA}$$

Applying KVL to the output common emitter loop

$$V_C = V_{CC} - (I_B + I_C)R_C$$

$$V_C = 10 - (16.21 \times 10^{-6} + 1.621 \times 10^{-3}) \times 2.5 \times 10^3$$

$$\therefore V_C = 5.9069\ \text{V}$$

$V_E = (I_C + I_B)R_E$

$V_E = (16.21 \times 10^{-6} + 1.621 \times 10^{-3}) \times 10^3$

$\therefore V_E = 1.637$ V

$V_{CE} = V_C - V_E$

$V_{CE} = 5.9069$ V $- 1.637$ V

$\therefore V_{CE} =$ **4.2699 V**

Stability factor:

$$\mathrm{S} = \frac{\beta + 1}{1 + \beta\left(\frac{R_E + R_C}{R_B + R_C + R_E}\right)}$$

$$S = \frac{100 + 1}{1 + 100 \times \left(\frac{1k + 2.5k}{220k + 2.5k + 1k}\right)}$$

$\therefore S =$ **39.36**

SIMULATED RESULTS:
Above circuit is simulated using LTspice and the results are presented below:

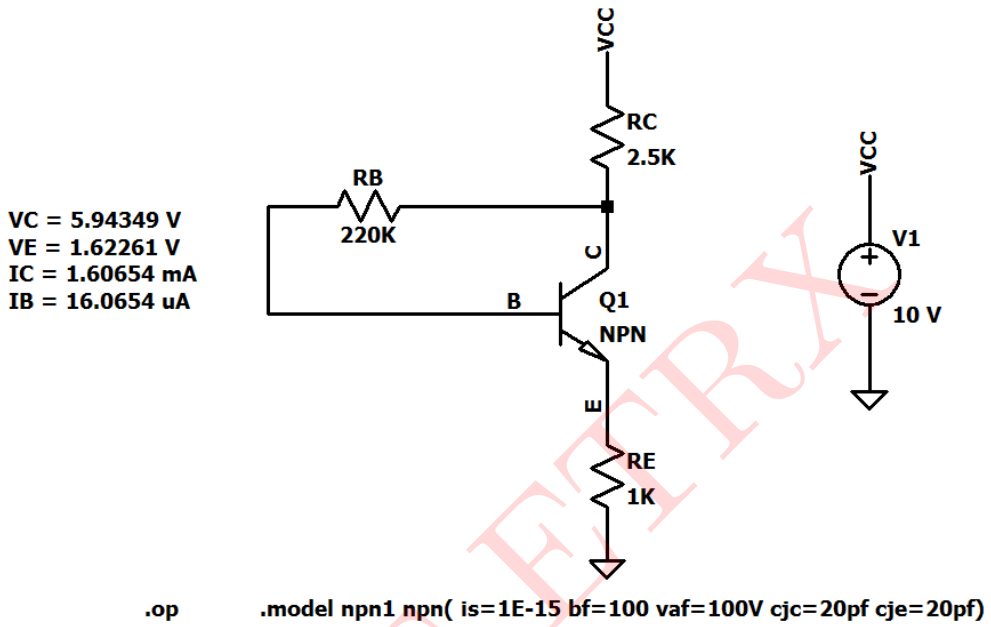

Figure 10: Circuit schematic: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
I_B	16.21 μA	16.6054 μA
I_C	1.621 mA	1.6065 mA
V_C	5.9069 V	5.94349 V
V_E	1.637 V	1.62261 V

Table 4: Numerical 4

5. For the voltage feedback network shown in Figure 11, determine I_C, V_C, V_E and V_{CE}
Given: $\beta = 100$

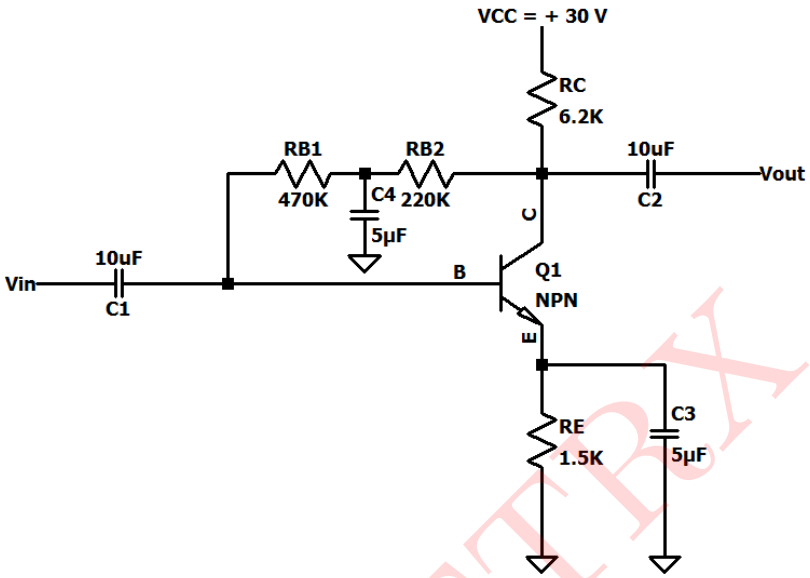

Figure 11: Circuit 5

Solution:
In DC analysis, the capacitors act as open circuit.

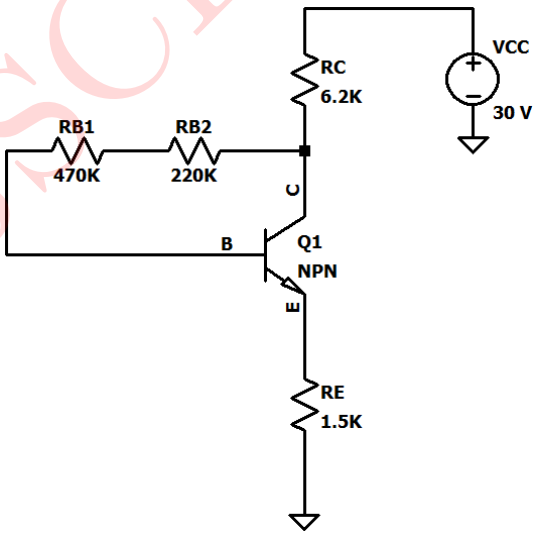

Figure 12: DC equivalent circuit

Since, f = 0, $\quad \therefore X_c = \dfrac{1}{2\pi f_c} = \infty$

Applying KVL to the input base-emitter loop:

$$V_{CC} - (I_B + I_C)R_C - I_B(R_{B_1} + R_{B_2}) - (I_B + I_C)R_E - V_{BE} = 0$$

$$V_{CC} - (\beta + 1)I_B R_C - I_B(R_{B_1} + R_{B_2}) - (\beta + 1)I_B R_E - V_{BE} = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{(R_{B_1} + R_{B_2}) + (\beta + 1)(R_C + R_E)}$$

$$I_B = \frac{30 - 0.7}{(470k + 220k) + 101 \times (6.2k + 1.5k)}$$

$$\therefore I_B = 19.96\mu A$$

$$I_C = \beta I_B = 100 \times 19.963\mu A$$

$$\therefore I_C = \mathbf{1.9963\ mA}$$

Applying KVL to the output common emitter loop:

$$V_C = V_{CC} - (I_B + I_C)R_C$$

$$V_C = 30 - (19.963 \times 10^{-6} + 1.9963 \times 10^{-3}) \times (6.2 \times 10^3)$$

$$\therefore V_C = \mathbf{17.501\ V}$$

$$V_E = (I_B + I_C)R_E$$

$$V_E = (19.963 \times 10^{-6} + 1.9963 \times 10^{-3}) \times 1.5 \times 10^3$$

$$\therefore V_E = \mathbf{3.0239\ V}$$

$$V_{CE} = V_C - V_E = 17.501\ \text{V} - 3.0239\ \text{V}$$

$$\therefore V_{CE} = \mathbf{14.4771\ V}$$

SIMULATED RESULTS:
Above circuit is simulated using LTspice and the results are presented below:

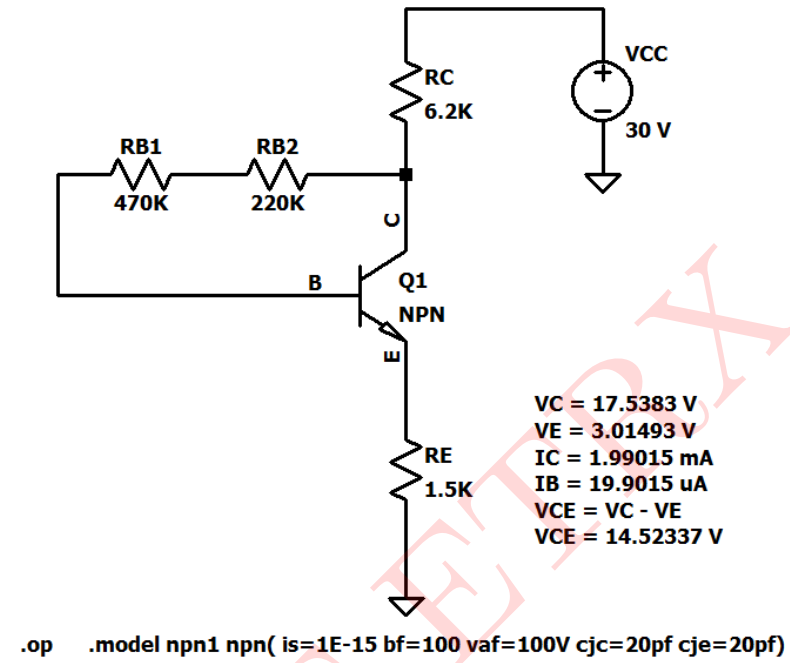

Figure 13: Circuit schematic: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
I_B	19.963 μA	19.9015 μA
I_C	1.9963 mA	1.99015 mA
V_{CE}	14.4771 V	14.52337 V
V_E	3.0239 V	3.01493 V

Table 5: Numerical 5

6. For the network shown in Figure 14, determine I_B, I_C, V_{CE} and V_C
Given: $\beta = 120$

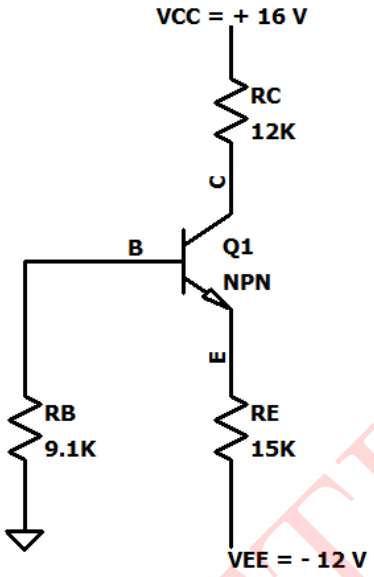

Figure 14: Circuit 6

Solution:

Applying KVL to the input base-emitter loop:

$$-I_B R_B - V_{BE} - (1+\beta) I_B R_E + V_{EE} = 0$$

$$\therefore I_B = \frac{V_{EE} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$I_B = \frac{12 - 0.7}{9.1 \times 10^3 + 121 \times 15 \times 10^3}$$

$$\therefore I_B = \mathbf{6.1945 \mu A}$$

$$I_C = \beta I_B = 120 \times 6.1948 \mu A$$

$$\therefore I_C = \mathbf{0.74337\ mA}$$

Applying KVL to the output common emitter loop

$$V_{CE} = V_{CC} - I_C R_C - (I_B + I_C) R_E + V_{EE}$$

$$\therefore V_{CE} = \mathbf{7.83598\ V}$$

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 16 - (0.743374 \times 10^{-3} \times 12 \times 10^3)$$

$$\therefore V_C = \mathbf{7.0795\ V}$$

SIMULATED RESULTS:
Above circuit is simulated using LTspice and the results are presented below:

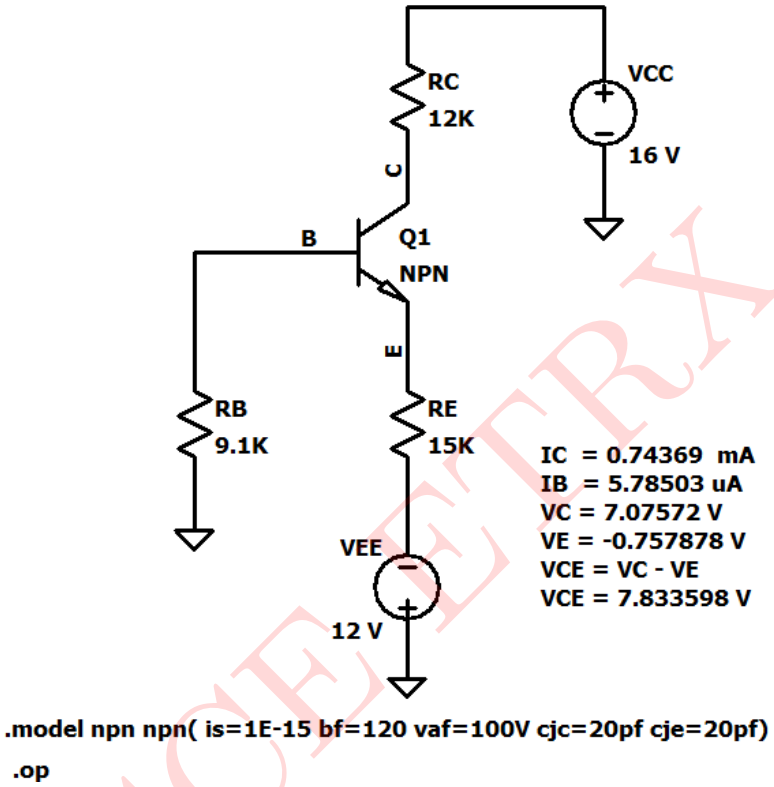

Figure 15: Circuit schematic: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
I_B	6.1948 μA	5.7850 μA
I_C	0.74337 mA	0.74369 mA
V_{CE}	7.83598 V	7.83359 V
V_C	7.0795 V	7.07572 V

Table 6: Numerical 6

7. In the circuit shown in Figure 14, the transistor parameters are: $V_{TN} = 0.8V$ and $k_n = 0.5$ mA/V^2. Calculate V_{GS}, I_D and V_{DS}

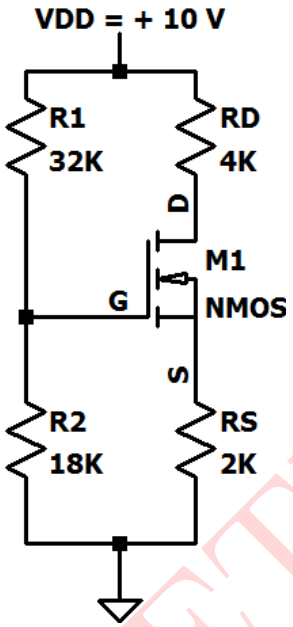

Figure 16: Circuit 7

Solution:

The above Circuit 7 is a voltage divider bias circuit.

Applying Thevenin's equivalent at the gate terminal

$R_G = R_1 || R_2 = 32\text{k}||18\text{k}$

$\therefore R_G = 11.52k\Omega$

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{18k}{32k + 18k} \times 10$$

$\therefore V_G = 3.6V$

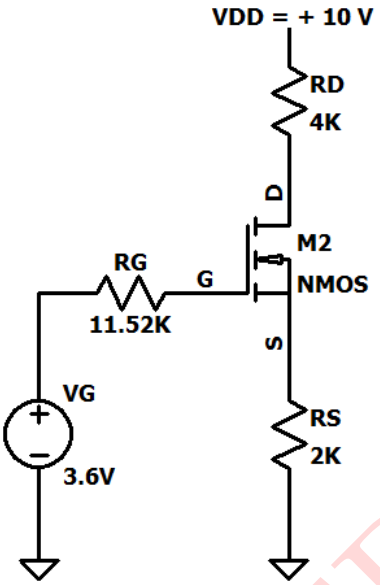

Figure 17: Thevenin's equivalent circuit

$V_{GS} = V_G - V_S$

$V_S = I_D R_S = I_D(2k)$

$\therefore V_{GS} = 3.6 - I_D(2k)$ ..... (1)

We know, $I_D = k_n(V_{GS} - V_T)^2$

$\therefore I_D = 0.5 \times 10^{-3} \times (V_{GS} - 0.8)^2$ ..... (2)

Substituting the value of I_D from equation (2) in equation (1), we get

$V_{GS} = 3.6 - 0.5 \times 2(V_{GS} - 0.8)^2$

$\therefore V_{GS} = 3.6 - (V_{GS} - 0.8)^2$

$\therefore V_{GS} = 3.6 - (V_{GS}^2 - 1.6V_{GS} + 0.64)$

$\therefore V_{GS}^2 - 0.6V_{GS} - 2.96 = 0$

$\therefore V_{GS} = 1.4464$ V or 2.0464 V

Since, $|V_{GS}| < |V_{TN}|$,

$\therefore V_{GS} =$ **2.0464 V**

From equation (1), $I_D = 0.5 \times 10^{-3} \times (2.0464 - 0.8)^2$

$\therefore I_D =$ **0.77675 mA**

Applying KVL to the output drain-source loop

$V_{DS} = V_{DD} - I_D(R_D + R_S) = 10 - 0.77675(4k + 2k) \times 10^{-3}$

$\therefore V_{DS} =$ **5.3395 V**

SIMULATED RESULTS:
Above circuit is simulated using LTspice and the results are presented below:

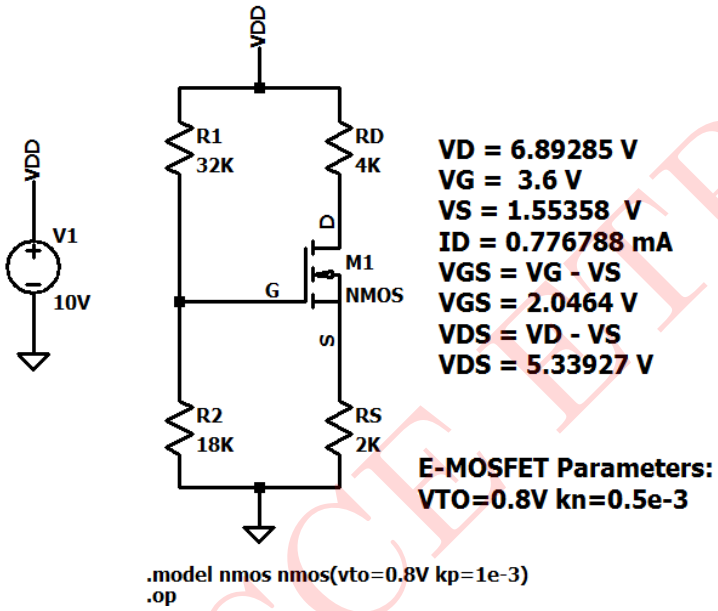

Figure 18: Circuit schematic: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
V_G	3.6 V	3.6 V
V_{GS}	2.0464 V	2.04642 V
V_{DS}	5.3395 V	5.33927 V
I_D	0.77675 mA	0.776788 mA

Table 7: Numerical 7

8. For the transistor in the circuit shown in Figure 17, the parameters are:
   $V_{TN} = 0.4V$, $k'_n = 0.120\ \mu A/V^2$ and $\frac{W}{L} = 25$
   Determine V_{GS}, I_D and V_{DS}

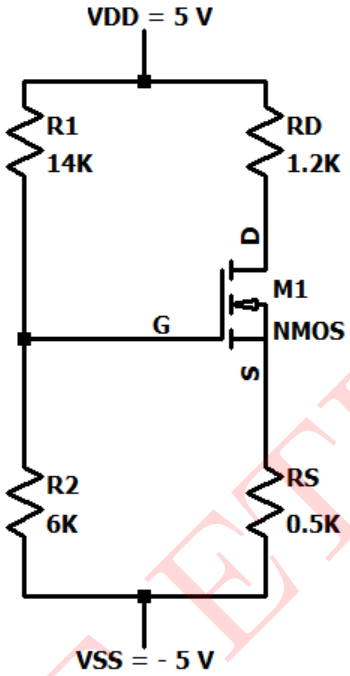

Figure 19: Circuit 8

Solution:

The above Circuit 1 is a voltage divider bias circuit.

Applying Thevenin's equivalent at the Gate terminal

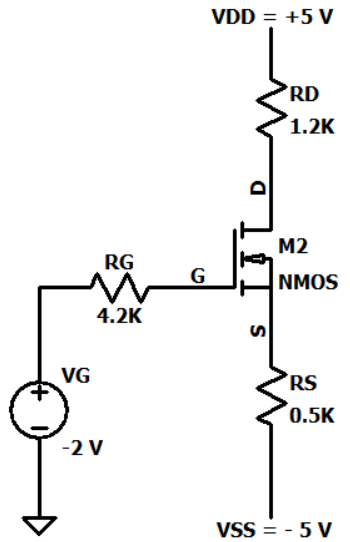

Figure 20: Thevenin's equivalent circuit

$R_G = R_1||R_2 = 14\text{k}||6\text{k}$

$\therefore R_G = 4.2k\Omega$

$$V_G = \left[\frac{R_2}{R_1 + R_2} \times (V_{DD} + V_{SS})\right] - 5 = \left[\frac{6k}{14k + 6k} \times 10\right] - 5$$

$\therefore V_G = -2V$

$V_{GS} = V_G - V_S$

$V_S = I_D R_S - 5$

$\therefore V_{GS} = -2 - [I_D(0.5k) - 5]$

$\therefore V_{GS} = 3 - I_D(0.5k)$ ..... (1)

$k_n = k'_n \times \frac{W}{L} = 120 \times 10^{-6} \times 25 = 3mA/V^2$

We know, $I_D = k_n(V_{GS} - V_T)^2$

$\therefore I_D = 3 \times 10^{-3} \times (V_{GS} - 0.4)^2$ ..... (2)

Substituting the value of I_D from equation (2) in equation (1), we get

$V_{GS} = 3 - \times 10^{-3} \times 0.5 \times 10^3 \times (V_{GS} - 0.4^2)$

$\therefore V_{GS} = 3 - 1.5 \times (V_{GS} - 0.4)^2$

$\therefore V_{GS} = 3 - 1.5V_{GS}^2 + 1.2V_{GS} - 0.24$

$\therefore 1.5V_{GS}^2 - 0.2V_{GS} - 2.76 = 0$

$\therefore V_{GS} = 1.42476V$ or $-1.2914V$

Since, $|V_{GS}| < |V_{TN}|$,

$\therefore V_{GS} =$ **1.42476 V**

From equation (1), $I_D = 3 \times 10^{-3} \times (1.42476 - 0.4)^2 =$ **3.15039 mA**

Applying KVL to the output drain-source loop

$V_{DS} = V_{DD} - I_D(R_D + R_S) - (-5) = 10 - 3.15039(1.2k + 0.5k) \times 10^{-3}$

$\therefore V_{DS} =$ **4.644 V**

SIMULATED RESULTS:

Above circuit is simulated using LTspice and the results are presented below:

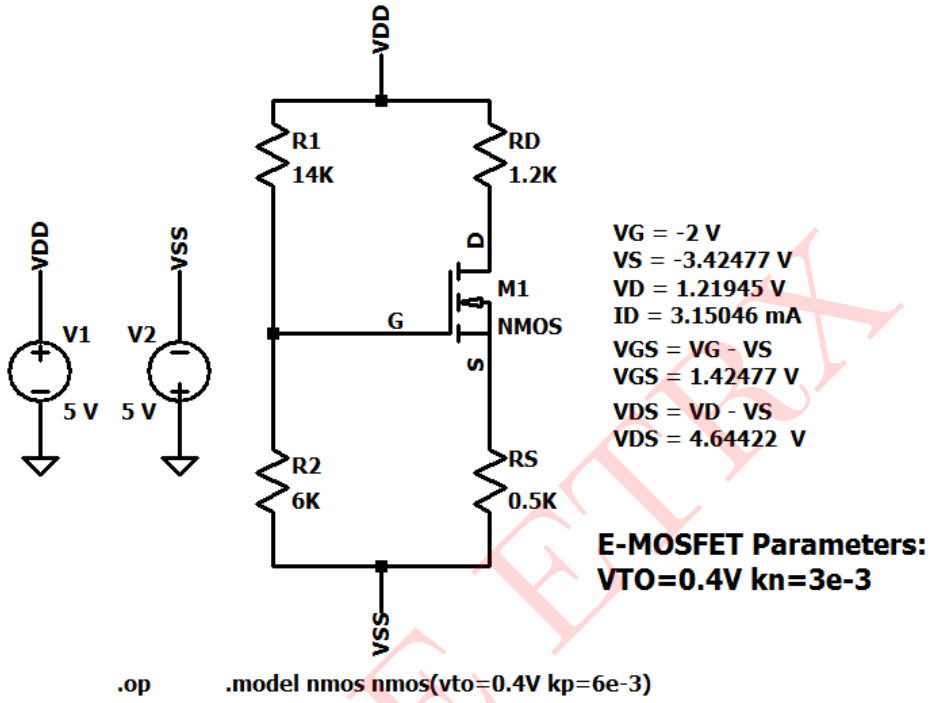

Figure 21: Circuit schematic: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
V_G	3.6 V	3.6 V
V_{GS}	2.0464 V	2.04642 V
V_{DS}	5.3395 V	5.33927 V
I_D	0.77675 mA	0.776788 mA

Table 8: Numerical 8

9. For the circuit shown in Figure 20, calculate V_{GS}, I_D and V_{DS}
Given: $V_P = -3$ V and $I_{DSS} = 12$mA

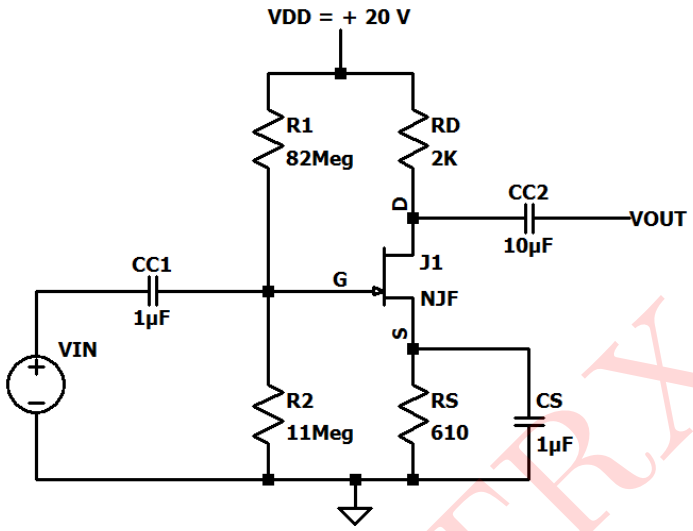

Figure 22: Circuit 9

Solution:

In DC analysis, the capacitors act as open circuit.

Since f = 0, $\quad \therefore X_c = \dfrac{1}{2\pi f_c} = \infty$

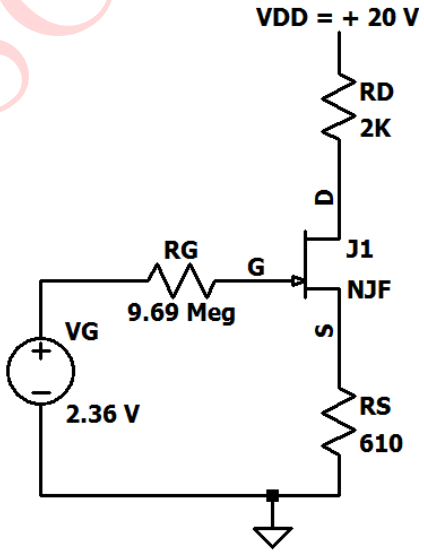

Figure 23: DC equivalent circuit

$R_G = R_1||R_2 = 82\text{M}||11\text{M} = 9.69\ \text{M}\Omega$

$$V_G = \left[\frac{R_2}{R_1 + R_2} \times V_{DD}\right] = \left[\frac{11M\Omega}{(11M + 52M)\Omega} \times 20\right]$$

$\therefore V_G = 2.36V$

$V_{GS} = V_G - V_S$

$V_S = I_D R_S = I_D(610)$

$\therefore V_{GS} = 2.36 - I_D(610)$ ..... (1)

Assuming that the JFET is working in saturation region

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 12mA\left(1 + \frac{V_{GS}}{-3}\right)^2$$ .....(2)

Substituting the value of I_D from equation (2) in equation (1), we get

$$V_{GS} = 2.36 - 7.32 \times \left(1 + \frac{2V_{GS}}{3} + \frac{V_{GS}^2}{9}\right)$$

$\therefore 0.8133V_{GS}^2 + 5.88V_{GS} + 4.96 = 0$

$\therefore V_{GS} = -0.975\ \text{V}$ or $-6.25\ \text{V}$

Since, $V_{GS} > V_P$,

$\therefore V_{GS} = \mathbf{-0.975\ V}$

From equation (2):

$$I_D = 12mA\left(1 - \frac{-0.975}{-3}\right)^2$$

$\therefore I_D = \mathbf{5.4675\ mA}$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$\therefore V_{DS} = 20 - 5.4675 \times 10^{-3}(2k + 610)$

$\therefore V_{DS} = \mathbf{5.729825\ V}$

SIMULATED RESULTS:
Above circuit is simulated using LTspice and the results are presented below:

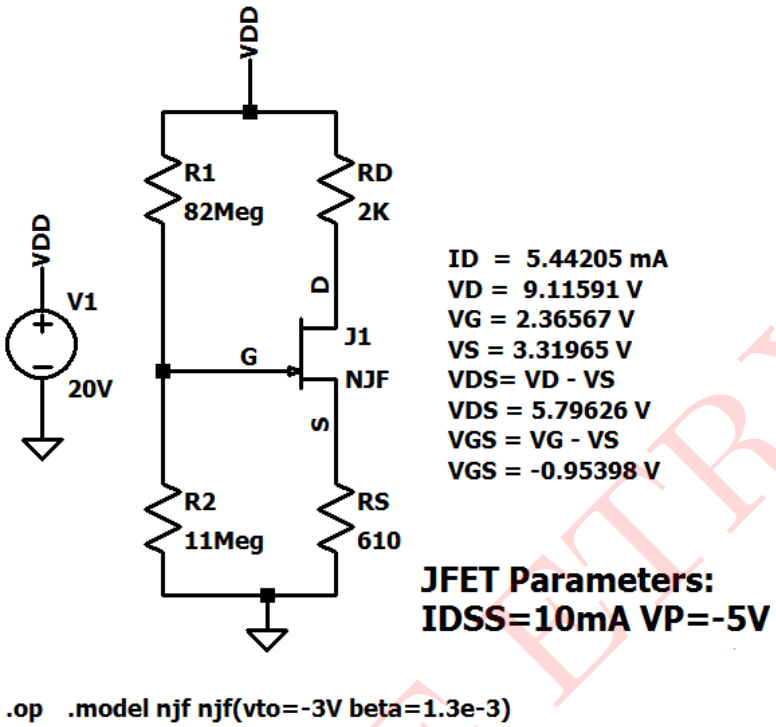

Figure 24: Circuit schematic: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
I_D	5.4675 mA	5.44205 mA
V_{GS}	-0.975 V	-0.95398 V
V_{DS}	5.729825 V	5.79626 V

Table 9: Numerical 9

10. For the circuit shown in Figure 23, find V_{GS}, I_D and V_{DS}
Given: $V_{GS}(th) = 5$ V, $V_{GS}(on) = 10$ V and $I_D(on) = 3$ mA

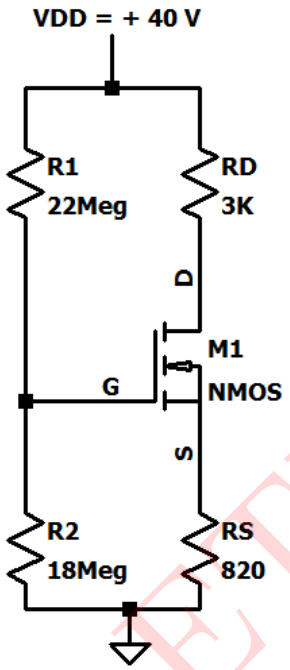

Figure 25: Circuit 10

Solution:

Circuit 10 is a voltage divider bias circuit.

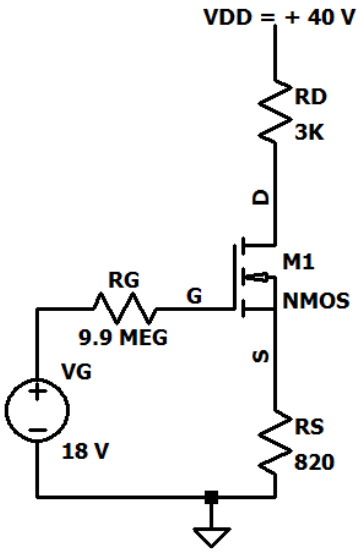

Figure 26: DC equivalent circuit

$R_G = R_1 || R_2 = 22\text{M}||18\text{M} = 9.9\ \text{M}\Omega$

$$V_G = \left[\frac{R_2}{R_1 + R_2} \times V_{DD}\right] = \left[\frac{18M\Omega}{(22M + 18M)\Omega} \times 40\right]$$

$\therefore V_G = 18V$

For E-NMOS transistor, $k_n = \dfrac{I_D(on)}{[V_{GS}(on) - V_{GS}(th)]^2}$

$\therefore k_n = \dfrac{3}{[10-5]^2} = 0.12\ \text{mA}/V^2$

$V_{GS} = V_G - V_S$

$V_S = I_D R_S = I_D(820)$

$\therefore V_{GS} = 18 - I_D(820)$ ..... (1)

Assuming that the given E-NMOS transistor is working in saturation region

$I_D = k_n[V_{GS} - V_{GS}(th)]^2$

$\therefore I_D = 0.12 \times 10^{-3}(V_{GS} - 5)^2$ ..... (2)

Substituting the value of I_D from equation (2) in equation (1), we get

$V_{GS} = 18 - 820 \times 0.12 \times 10^{-3} \times (V_{GS} - 5)^2$

$\therefore 0.0984V_{GS}^2 + 0.016V_{GS} - 15.54 = 0$

$\therefore V_{GS} = 12.48\ \text{V}$ or $-12.64\ \text{V}$

Since, $V_{GS} < V_{GS}(th)$,

$\therefore V_{GS} = \mathbf{12.48\ V}$

From equation (2):

$I_D = k_n(V_{GS} - 5)^2 = 0.12 \times 10^{-3} \times (12.48 - 5)^2$

$\therefore I_D = \mathbf{6.72\ mA}$

Applying KVL to the output drain- source loop

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$\therefore V_{DS} = 40 - 6.72 \times 10^{-3}(3k + 820)$

$\therefore V_{DS} = \mathbf{14.32\ V}$

SIMULATED RESULTS:
Above circuit is simulated using LTspice and the results are presented below:

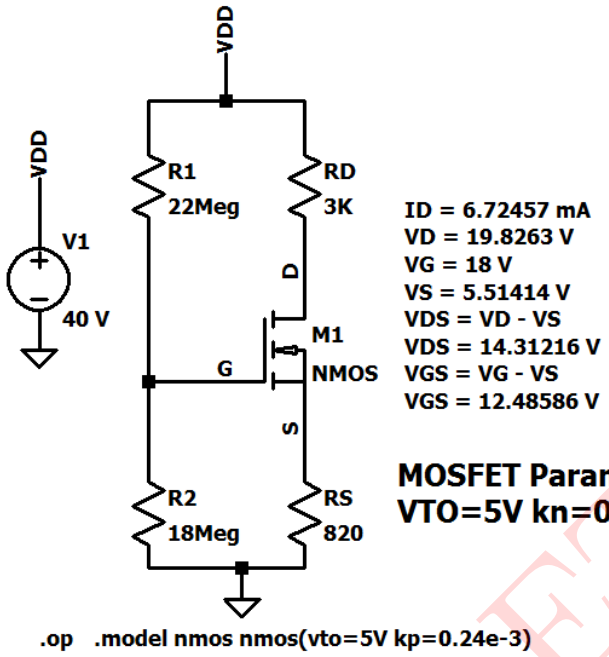

Figure 27: Circuit schematic: Results

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
I_D	6.72 mA	6.72457 mA
V_{GS}	12.48 V	12.48586 V
V_{DS}	14.32 V	14.31216 V

Table 10: Numerical 10

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