K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Diode Application

Numerical 1:
For the circuit shown below in figure 1, plot
a) Input $V_{in}(t)$ and output $V_{out}(t)$ waveforms
b) VTC curve
Given: $V_{in}(t) = 10V_{p-p}$ Sinusoidal signal with frequency of 5000Hz
$V_{D_{ON}} = 0.7$V
$V_{B_1} = 1$V DC, $V_{B_2} = 1$V DC, $R_1 = 1$kΩ

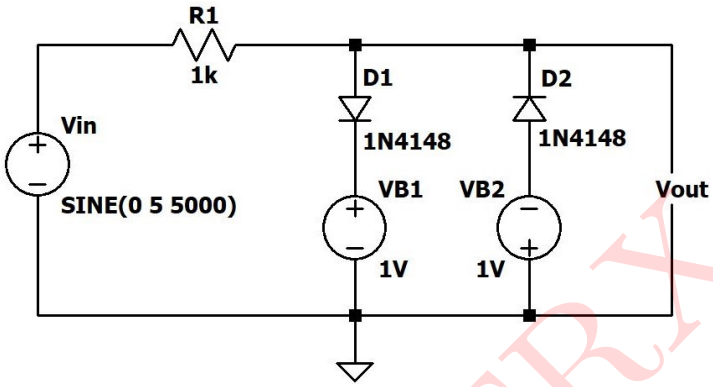

Figure 1: Circuit 1

Solution:

Assuming constant voltage models for diodes D_1 and D_2
When input voltage V_{in} is greater than $(V_{D_{1_{ON}}} + V_{B_1})$ i.e 0.7V + 1V = 1.7V, diode D_1 is ON and D_2 is OFF.
$\therefore V_{out} = V_{D_{1_{ON}}} + V_{B_1} = 0.7 + 1 = \mathbf{1.7V}$
$\therefore$ figure 1 reduces to,

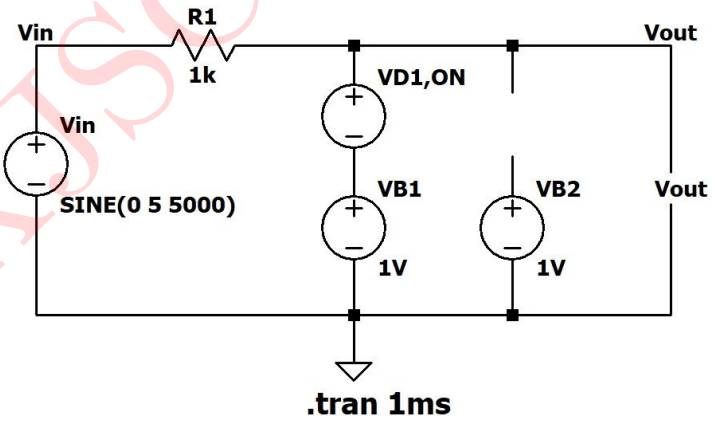

Figure 2: diode D_1 is ON and diode D_2 is OFF

When input voltage V_{in} is less than $(-V_{D_{2_{ON}}} - V_{B_2})$ i.e $-0.7V - 1V = -1.7V$, diode D_2 is ON and D_1 is OFF.

$\therefore V_{out} = -V_{D_{2_{ON}}} - V_{B_2} = -0.7 - 1 = \mathbf{-1.7V}$

$\therefore$ figure 1 reduces to,

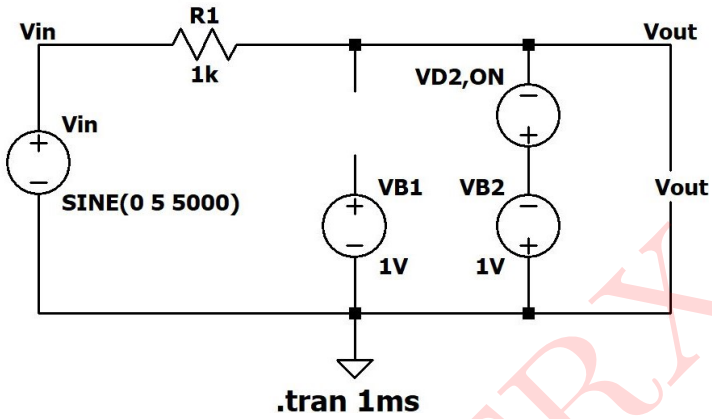

Figure 3: diode D_2 is ON and diode D_1 is OFF

When V_{in} is less than $(V_{B_1} + V_{D_{1_{ON}}})$ and also greater than $(-V_{D_{2_{ON}}} - V_{B_2})$, both diodes D_1 and D_2 are OFF.

$\therefore V_{out} = V_{in}$

$\therefore$ figure 1 reduces to,

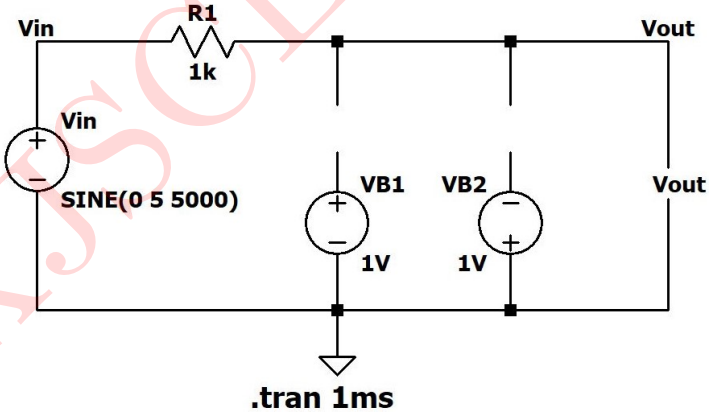

Figure 4: diode D_1 and diode D_2 are OFF

SIMULATED RESULTS:
Above circuit is simulated in LTspice and results are as follows:

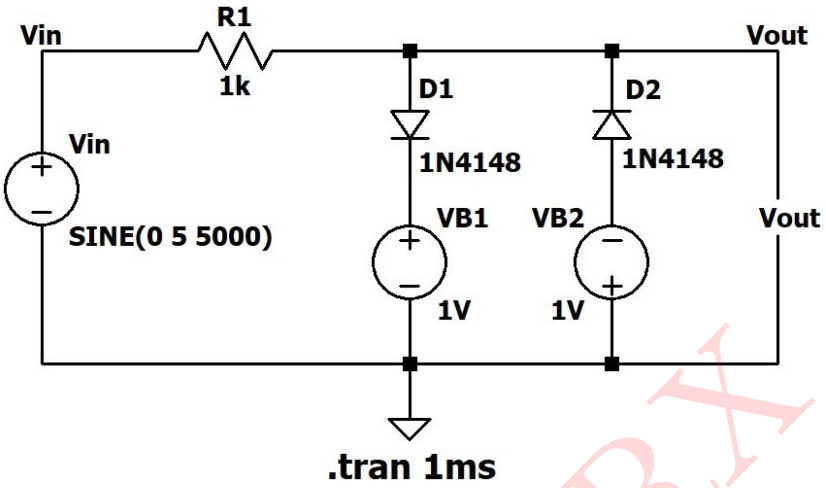

Figure 5: Circuit Schematic

The input and output waveforms are shown in figure 6.

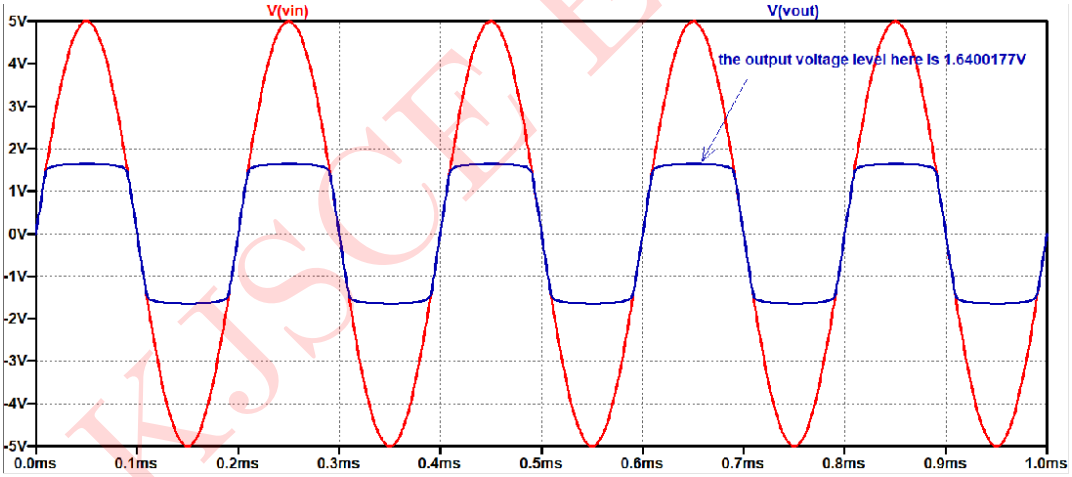

Figure 6: Input-Output waveforms

The VTC curve for the following circuit is given below in figure 7.

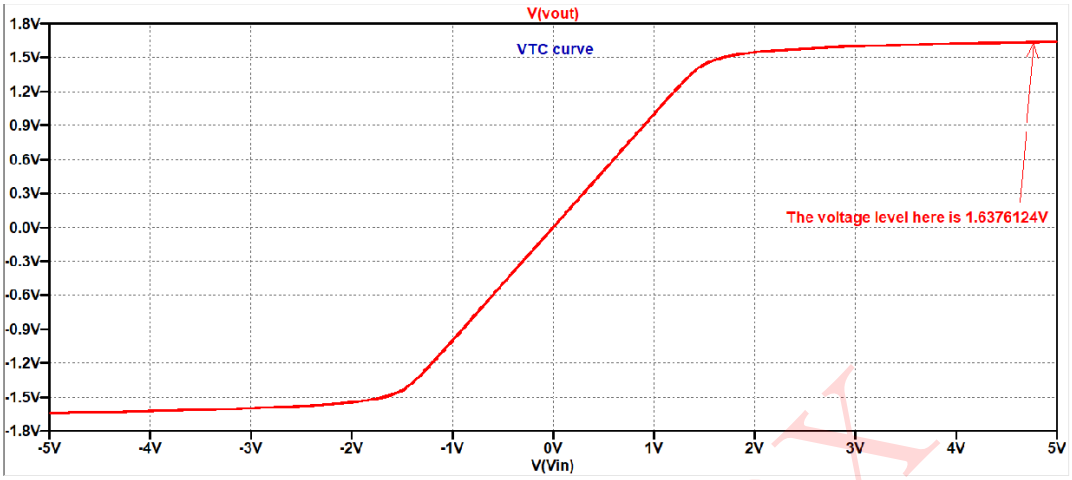

Figure 7: VTC curve

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
Clipped output voltage level	±1.7V	±1.640017

Table 1: Question 1

Numerical 2:
For the circuit shown below in figure 8,
Plot: Input $V_{in}(t)$ and output $V_{out}(t)$ waveforms
Given: $V_{in}(t)$ is a square wave as shown in figure 9

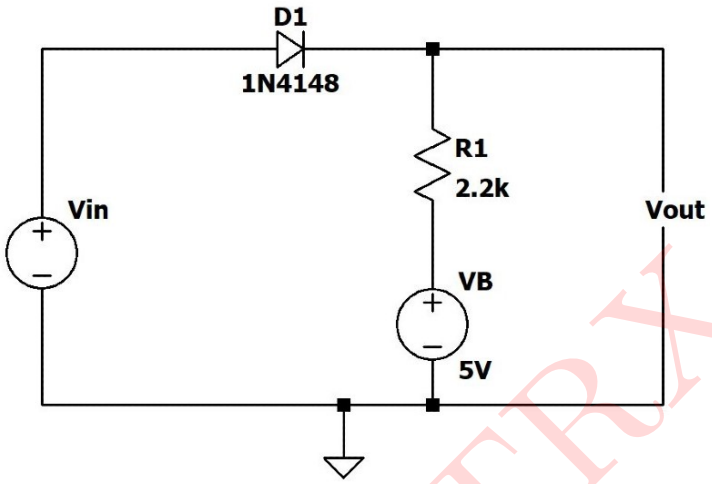

Figure 8: Circuit 2

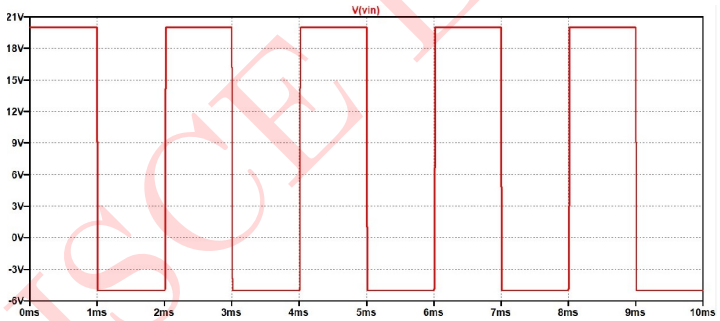

Figure 9: Square wave input

Solution:

Assuming constant voltage model for diode D_1,
When input voltage V_{in} is greater than $(V_{D_{1_{ON}}} + V_B)$ i.e 0.7V + 5V = 5.7V, diode D_1 is ON.
$\therefore V_{out} = V_{in} - V_{D_{ON}}$

∴ figure 8 reduces to,

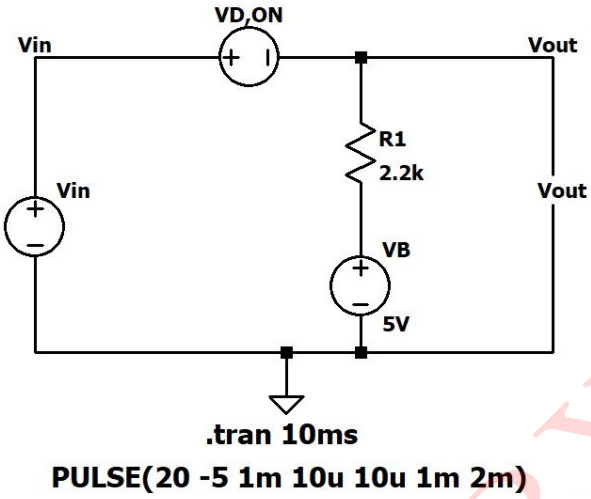

Figure 10: diode D_1 is ON

∴ $V_{out} = V_{in} - V_{D_{ON}}$
i.e $V_{out} = V_m - V_{D_{ON}} = 20.0.7 = \mathbf{19.3V}$
i.e output tracks input but with a shift of $V_{D_{ON}}$ i.e 0.7V

When V_{in} is less than $(V_{D_{ON}} + V_B)$ i.e 0.7V + 5V = 5.7V, diode D_1 is OFF.
∴ figure 8 reduces to,

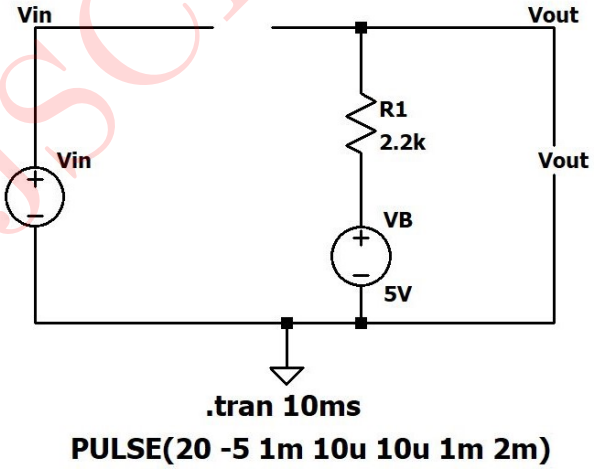

Figure 11: diode D_1 is OFF

∴ $V_{out} = V_B$
i.e $V_{out} = \mathbf{5V}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

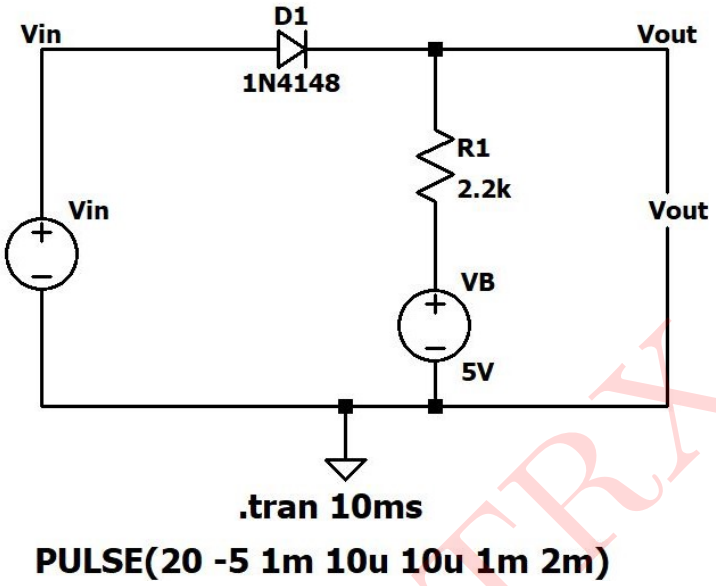

Figure 12: Circuit Schematic

The input and output waveforms are shown in figure 13.

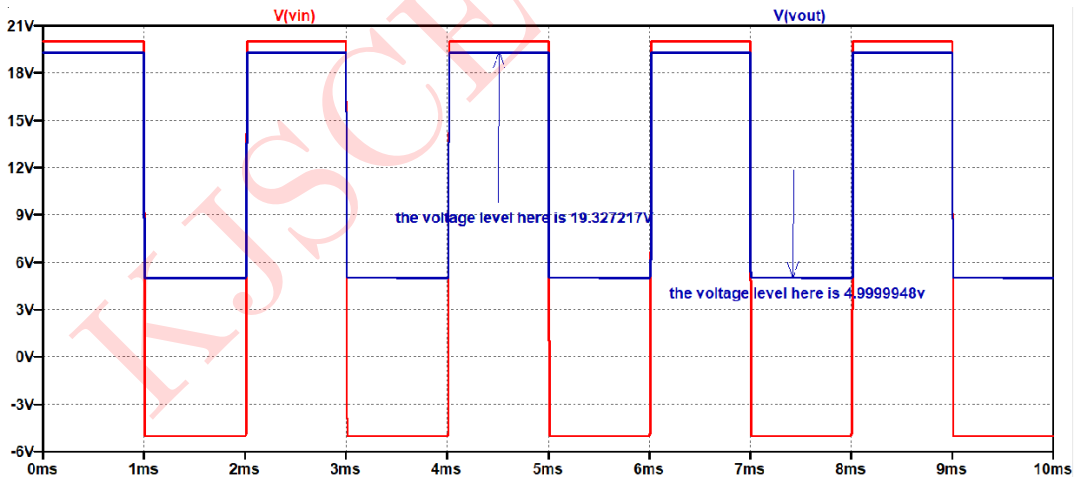

Figure 13: Input-Output waveforms

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
Clipped maximum output voltage level	19.3V	19.3272V
Clipped minimum output voltage level	5V	4.999V

Table 2: Question 2

Numerical 3:

For the circuit shown below in figure 14,

Plot: Input $V_{in}(t)$ and output $V_{out}(t)$ waveforms

Given: $10V_{p-p}$ square wave of frequency 1000Hz

C = 10μF and R = 10kΩ, diode D_1 is Si diode i.e $V_{D_{ON}} = 0.7$V, $V_1 = 2.7$V DC

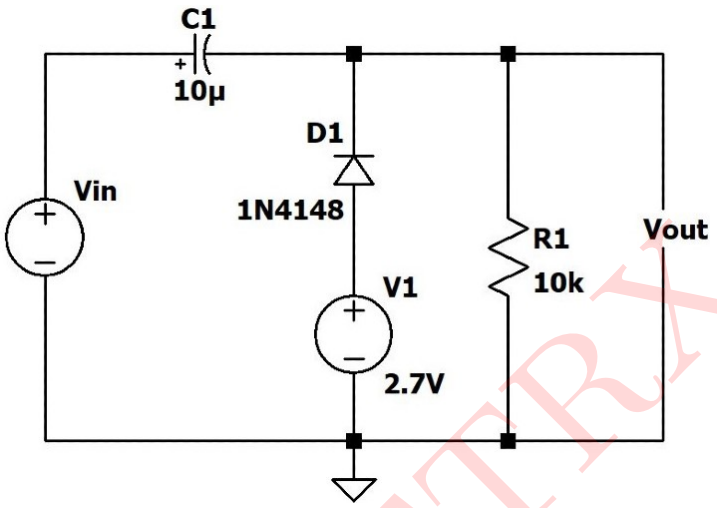

Figure 14: Circuit 3

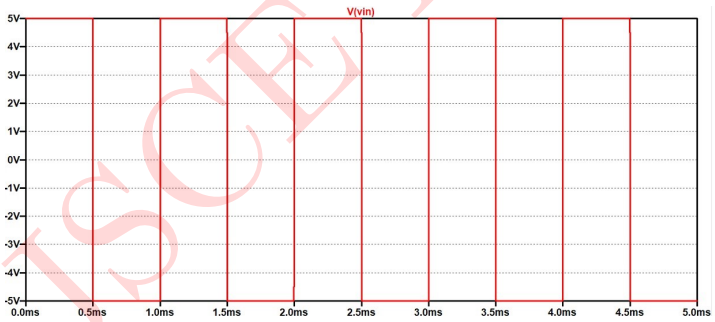

Figure 15: Square wave input

Solution:

Since given diode D_1 is Si diode, we will use constant voltage model i.e $V_{D_{ON}} = 0.7$V

Given: $V_{in} = 10V_{p-p}$ i.e $V_m = 5$V

Assumption: RC time constant is large enough(than time period of input signal) to ensure that voltage across capacitor does not discharge significantly during the period diode is off.

Operation:

a) During negative half cycle, D_1 is ON when $V_{in} < (-V_{D_{ON}} + V_1)$ i.e $V_{in} < (-0.7\text{V} + 2.7\text{V})$ i.e $V_{in} < 2$V

$\therefore$ figure 14 reduces to,

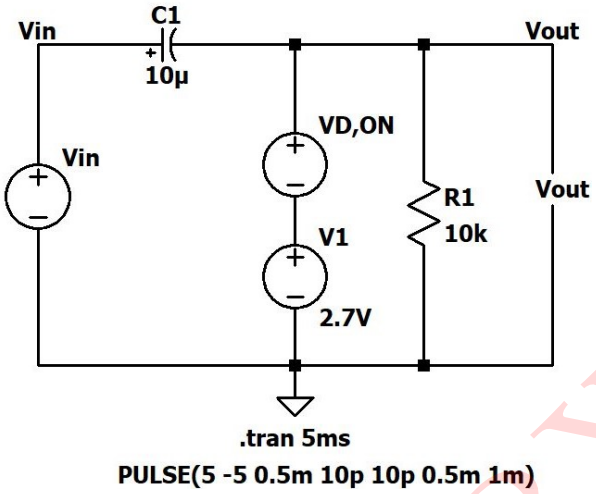

Figure 16: diode D_1 is ON

$\therefore V_{out} = V_{D_{ON}} + V_1 = -0.7V + 2.7V = \mathbf{2V}$
i.e $V_{out} = 2$V during negative half cycle

b) At the same time, voltage across capacitor V_C charges upto $-V_m$
KVL gives us:
$V_{in} + V_C + V_{D_{ON}} - V_1 = 0$
$V_C = -V_{in} - V_{D_{ON}} + V_1$ ($\because$ In negative half cycle, $V_{in} = V_m$)
$V_C = -(-V_m) - 0.7 + 2.7 = 5 - 0.7 + 2.7 = \mathbf{7V}$
i.e $V_C = 7$V is voltage across capacitor C_1 during positive half cycle

c) During positive half cycle, diode D_1 is OFF for entire positive half cycle
$\therefore$ figure 14 reduces to,

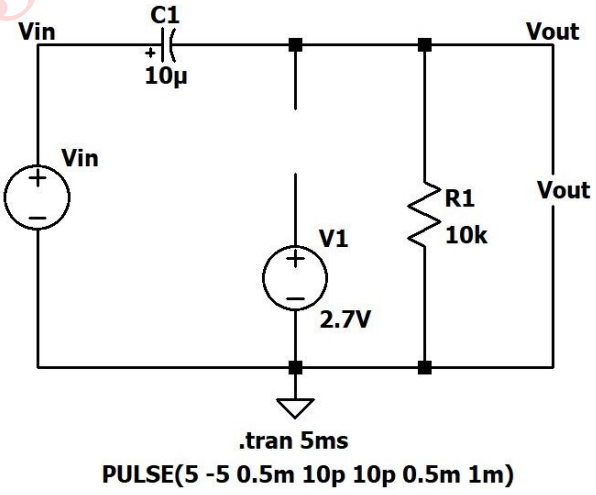

Figure 17: diode D_1 is OFF

During positive half cycle, capacitor C_1 holds the charge $V_C = 7$V and acts as a battery
$\therefore$ KVL ggives us:
$V_{in} + V_C - V_{out} = 0$
$\therefore V_{out} = V_{in} + V_C$
$V_{out} = V_m + V_C$ ($\because$ In positive half cycle, $V_{in} = V_m$)
$V_{out} = 5 + 7 = \mathbf{12V}$
i.e $V_{out} = 12$V during positive half cycle

SIMULATED RESULTS:
Above circuit is simulated in LTspice and results are as follows:

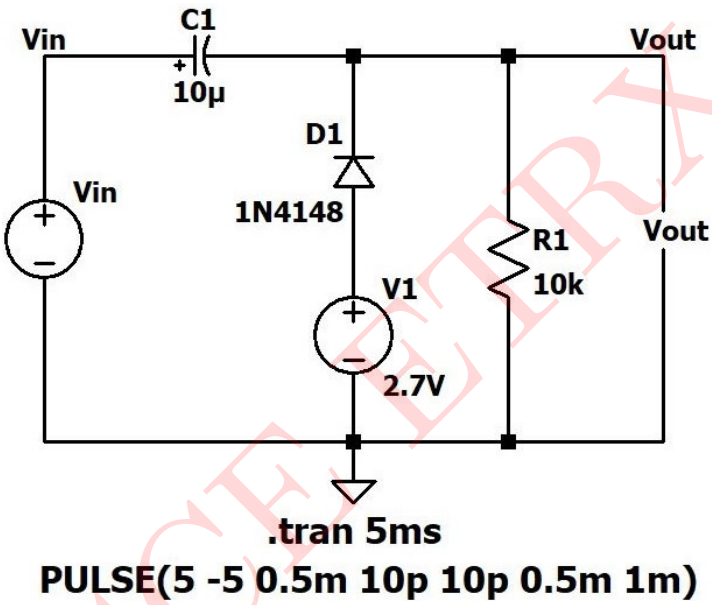

Figure 18: Circuit Schematic

The input and output waveforms are shown in figure 19.

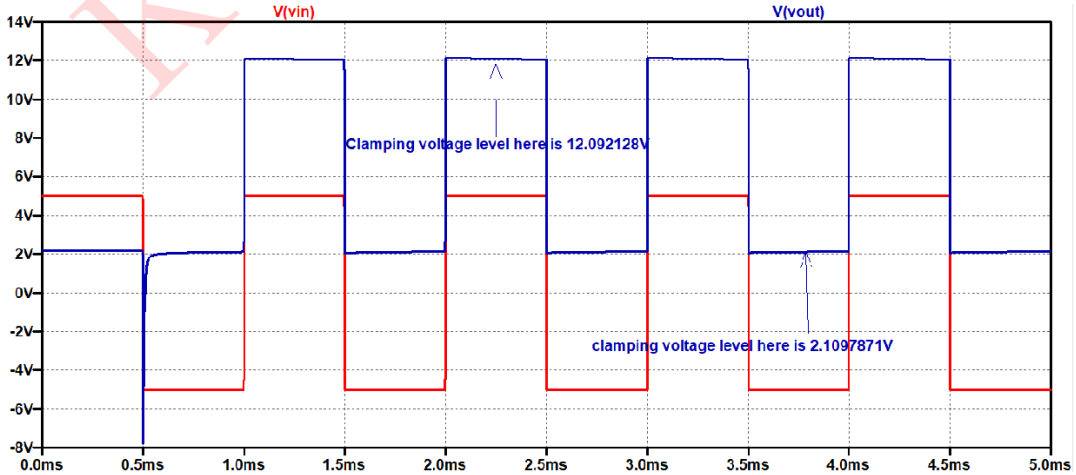

Figure 19: Input-Output waveforms

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
Upper level of clamped output voltage	12V	12.0921V
Lower level of clamped output voltage	2V	2.1097V

Table 3: Question 3

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