

K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
DC Biasing Circuits

Numerical 1:

Determine the following for the fixed-bias configuration as shown in figure 1. Given: $\beta = 50$

- I_{BQ} and I_{CQ}
- V_{CEQ}
- V_B and V_C
- V_{BC}

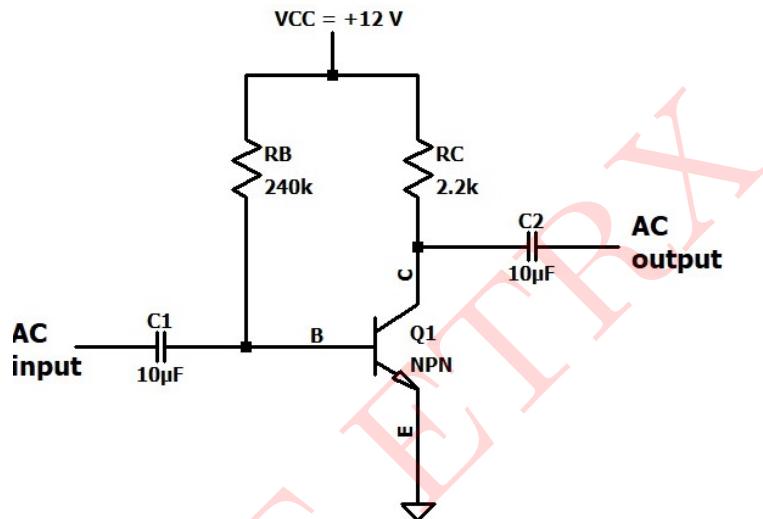


Figure 1: Circuit 1

Solution: The given circuit 1 is a Fixed-bias configuration

For dc biasing, the capacitors acts as an open source.

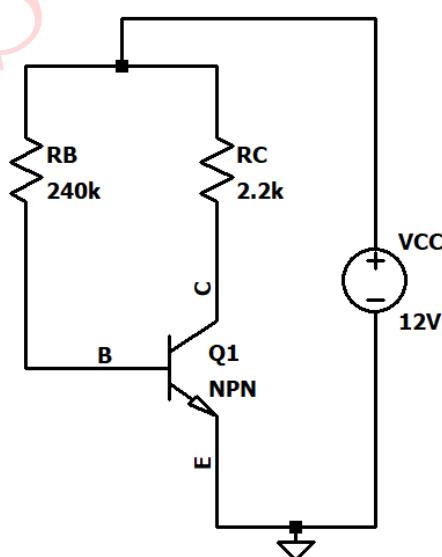


Figure 2: Circuit Schematic 1: DC Biasing

I_{BQ} & I_{CQ} :

I_{BQ} can be calculated by applying KVL to the base-emitter loop.

$$V_{CC} - I_{BQ}R_B - V_{BE} = 0$$

$$I_{BQ}R_B = V_{CC} - V_{BE}$$

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_{BQ} = \frac{12 - 0.7}{240k}$$

$$I_{BQ} = \mathbf{47.08 \mu A}$$

We know, $I_{CQ} = \beta \times I_{BQ}$

$$I_{CQ} = 50 \times 47.08 \times 10^{-6}$$

$$I_{CQ} = \mathbf{2.35 mA}$$

V_{CEQ} :

V_{CEQ} can be calculated by applying KVL to the collectore-emitter loop.

$$V_{CC} - I_C R_C - V_{CEQ} = 0$$

$$V_{CEQ} = V_{CC} - I_C R_C$$

$$V_{CEQ} = 12 - 2.35 \times 10^{-3} \times 2.2 \times 10^3$$

$$V_{CEQ} = \mathbf{6.83 V}$$

V_B & V_C :

$$V_B = V_{BE} + V_E$$

But, the emitter terminal is connected to ground. Therefore, $V_E = 0$

$$V_B = V_{BE}$$

$$V_B = \mathbf{0.7 V}$$

Also, $V_C = V_{CEQ}$ ($\because V_E = 0$)

$$V_C = \mathbf{6.83 V}$$

V_{BC} :

$$V_{BC} = V_B - V_C$$

$$V_{BC} = 0.7 - 6.83$$

$$V_{BC} = \mathbf{-6.13 V}$$

The negative sign indicates that the base-collector junction is reverse biased.

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below.

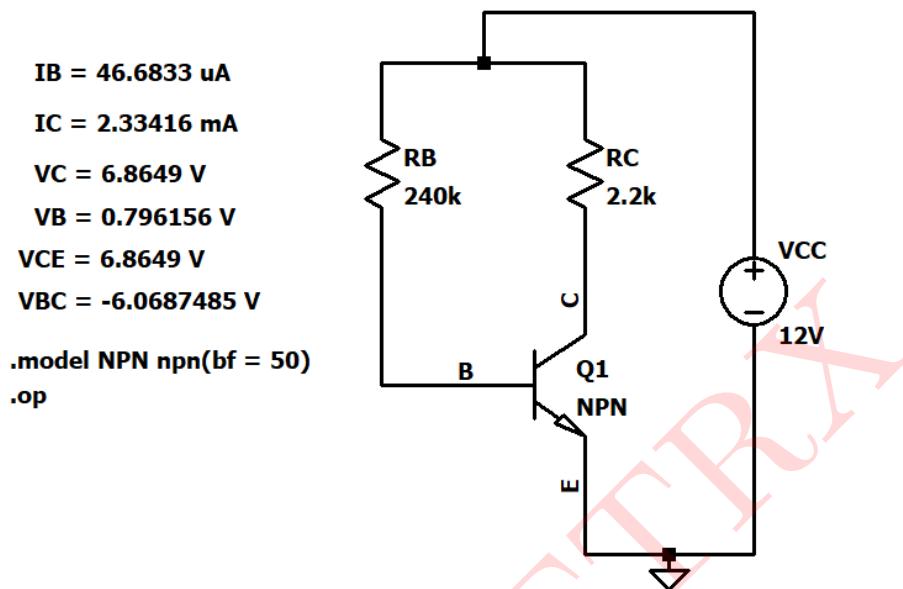


Figure 3: Circuit Schematic 1: Result

Comparison of theoretical and simulated values:

DC Parameters	Theoretical Values	Simulated Values
I_{BQ}	$47.08 \mu\text{A}$	$46.68 \mu\text{A}$
I_{CQ}	2.35 mA	2.33 mA
V_{CEQ}	6.83 V	6.86 V
V_B	0.7 V	0.79 V
V_C	6.83 V	6.86 V
V_{BC}	-6.13 V	-6.06 V

Table 1: Numerical 1

Numerical 2:

For the emitter-bias network shown in figure 4 determine:

I_B , I_C , V_{CE} , V_C , V_E , V_B , V_{BC} Given: $\beta = 50$

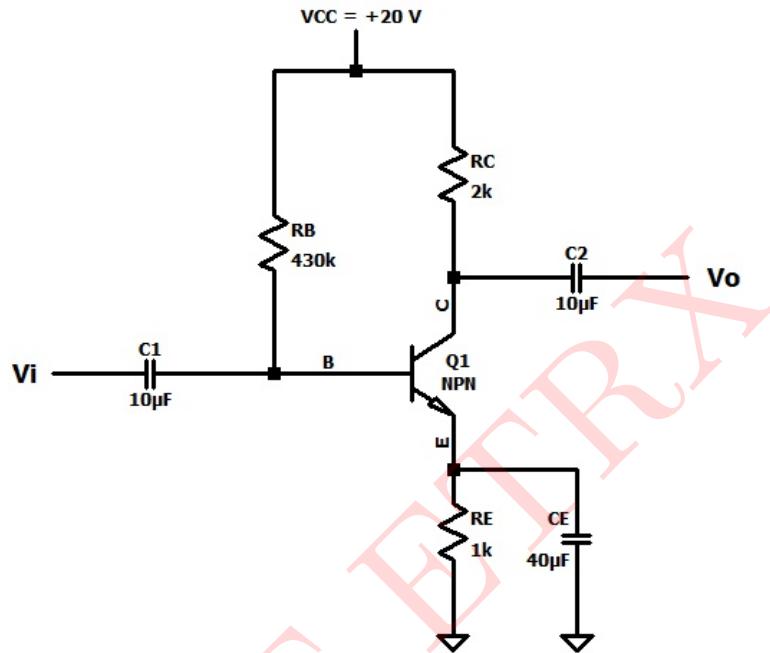


Figure 4: Circuit 2

Solution: The given circuit is an emitter-bias configuration.

For dc biasing, the capacitors act as an open source.

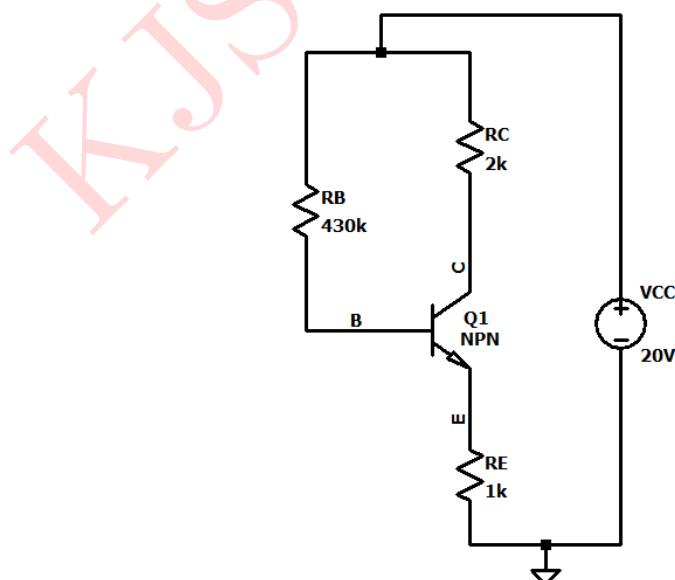


Figure 5: Circuit Schematic 2: DC Biasing

I_B :

I_B can be calculated by applying KVL to the base-emitter loop.

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (1 + \beta) I_B R_E = 0$$

$$I_B R_B + (1 + \beta) I_B R_E = V_{CC} - V_{BE}$$

$$I_B = \frac{12 - 0.7}{430K + (1 + 50)1k}$$

$$I_B = 40.1 \mu\text{A}$$

I_C :

$$I_C = \beta \times I_B$$

$$I_C = 50 \times 40.1 \times 10^{-6}$$

$$I_C = 2.01 \text{ mA}$$

$$I_E = 2.01 \text{ mA} \quad (\because I_E \simeq I_C)$$

V_{CE} :

V_{CE} can be calculated by applying KVL to the collector-emitter loop.

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = 20 - 2.01 \times 10^{-3} \times 2 \times 10^3 \times 2.01 \times 10^{-3} \times 1 \times 10^3$$

$$V_{CE} = 13.97 \text{ V}$$

V_C :

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 20 - 2.01 \times 10^{-3} \times 2 \times 10^3$$

$$V_C = 15.98 \text{ V}$$

V_E :

$$V_E = I_E R_E$$

$$V_E = 2.01 \times 10^{-3} \times 1 \times 10^3$$

$$V_E = 2.01 \text{ V}$$

V_B :

$$V_B = V_{BE} + V_E$$

$$V_B = 0.7 + 2.01$$

$$V_B = 2.71 \text{ V}$$

V_{BC} :

$$V_{BC} = V_B - V_C$$

$$V_{BC} = 2.71 - 15.98$$

$$V_{BC} = -13.27 \text{ V}$$

The negative sign indicates that the base-collector junction is reverse biased.

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below.

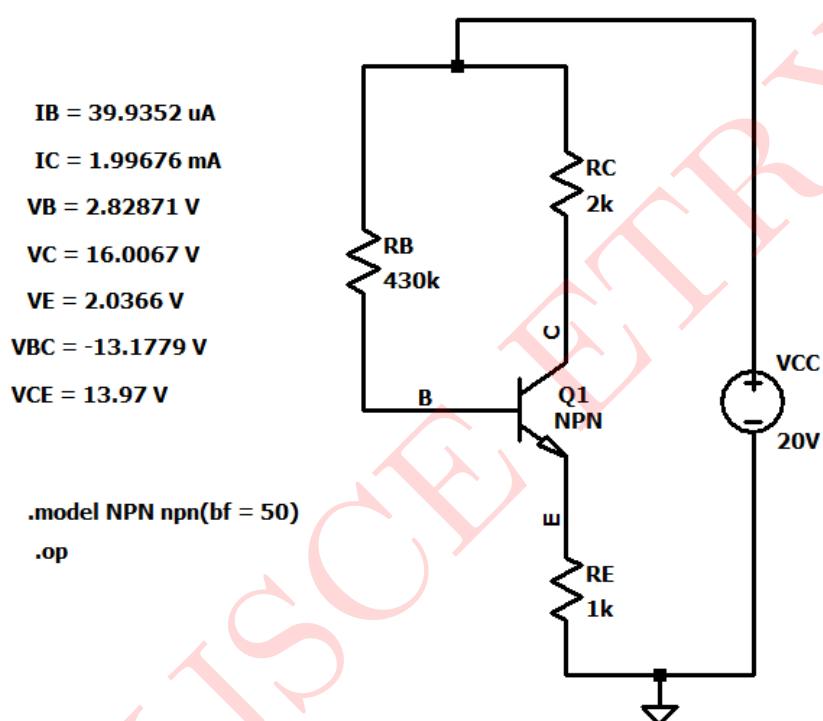


Figure 6: Circuit Schematic 2: Result

Comparison of theoretical and simulated values:

DC Parameters	Theoretical Values	Simulated Values
I_B	$40.1 \mu\text{A}$	$39.93 \mu\text{A}$
I_C	2.01 mA	1.99 mA
V_{CE}	13.97 V	13.97 V
V_C	15.98 V	16 V
V_E	2.01 V	2.03 V
V_B	2.71 V	2.82 V
V_{BC}	-13.27 V	-13.17 V

Table 2: Numerical 2

Numerical 3:

For the circuit 3 shown below, find I_C , V_{CE} and Stability factor.

Given: $\beta = 100$

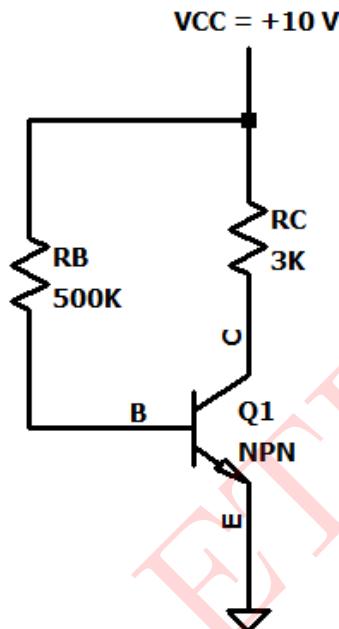


Figure 7: Circuit 3

Solution : The given circuit 3 is a Fixed-bias configuration

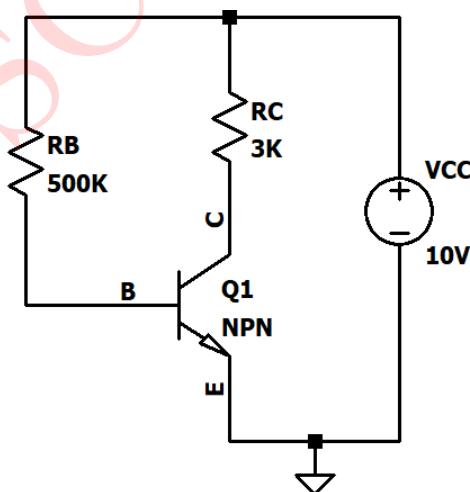


Figure 8: Circuit Schematic 3: DC Biasing

I_C :

I_B can be calculated by applying KVL to the input base-emitter loop.

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{10 - 0.7}{500 \times 10^3} = \mathbf{18.6 \mu A}$$

We know, $I_C = \beta I_B$

$$I_C = 100 \times 18.6 \times 10^{-6} = \mathbf{1.86 \text{ mA}}$$

V_{CE} :

V_{CE} can be calculated by applying KVL to the output collector-emitter loop.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = 10 - 1.86 \times 10^{-3} \times 3 \times 10^3 = \mathbf{4.42 \text{ V}}$$

S :

Stability factor for a fixed bias configuration is given as:

$$S = \beta + 1$$

$$S = 100 + 1 = \mathbf{101}$$

SIMULATED RESULT:

Above circuit is simulated in LTsSpice. The results are presented below.

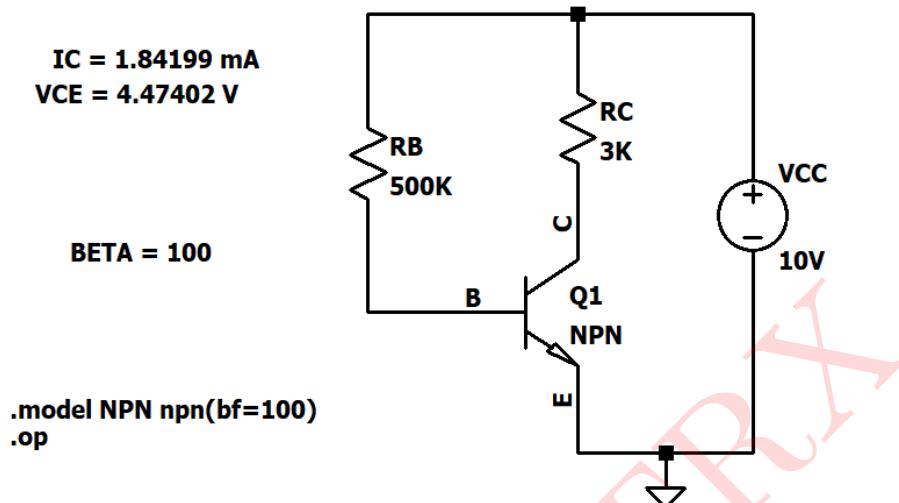


Figure 9: Circuit Schematic 3: Result

Comparison of theoretical and simulated values:

DC Parameters	Theoretical Values	Simulated Values
I_C	1.86 mA	1.84 mA
V_{CE}	4.42 V	4.47 V

Table 3: Numerical 3

Numerical 4:

For the fixed bias circuit shown in figure 10 determine I_C & V_{CE}

Given: $\alpha = 0.98$, $I_{CBO} = 10 \mu\text{A}$, $R_C = 4 \text{ k}\Omega$, $R_B = 820 \text{ k}\Omega$, $V_{CC} = 12 \text{ V}$

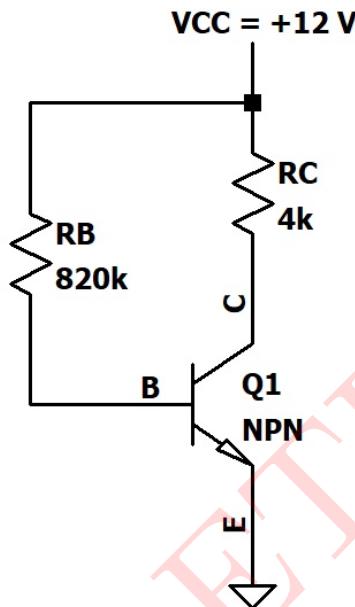


Figure 10: Circuit 4

Solution: The given circuit is a fixed bias configuration

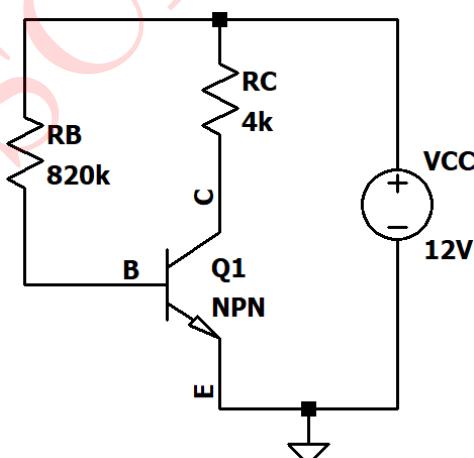


Figure 11: Circuit Schematic 4: DC Biasing

To find device current, we should know β

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\beta = \frac{0.98}{1 - 0.98} = 49$$

I_C :

I_B can be calculated by applying KVL to the input base-emitter loop.

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{12 - 0.7}{820 \times 10^3} = 13.78 \mu\text{A}$$

We know, $I_C = \beta I_B + (\beta + 1) I_{CBO}$

$$I_C = 49 \times 13.78 \times 10^{-6} + (49 + 1) \times 10 \times 10^{-6} = 1.17 \text{ mA}$$

V_{CE} :

V_{CE} can be calculated by applying KVL to the output collector-emitter loop.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = 12 - 1.17 \times 10^{-3} \times 4 \times 10^3 = 7.32 \text{ V}$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below.

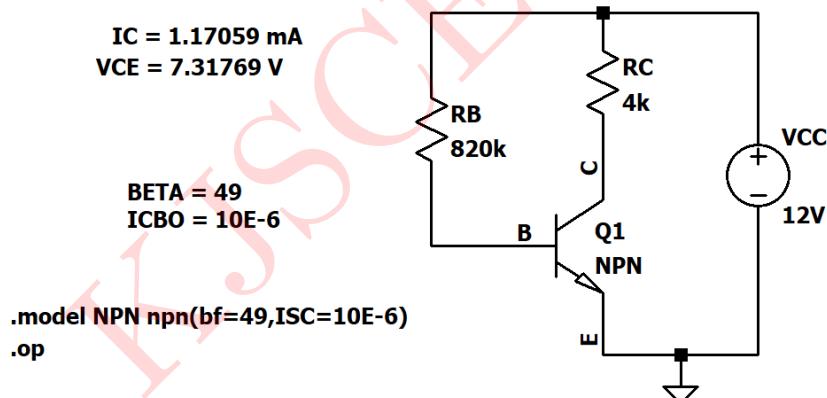


Figure 12: Circuit Schematic 4: Result

Comparison of theoretical and simulated values:

DC Parameters	Theoretical Values	Simulated Values
I_C	1.17 mA	1.17 mA
V_{CE}	7.32 V	7.31 V

Table 4: Numerical 4

Numerical 5:

Determine the following for the fixed-bias configuration as shown in figure 13:

I_{BQ} , I_{CQ} , V_{CEQ} , V_C , V_B , V_E Given: $\beta = 90$

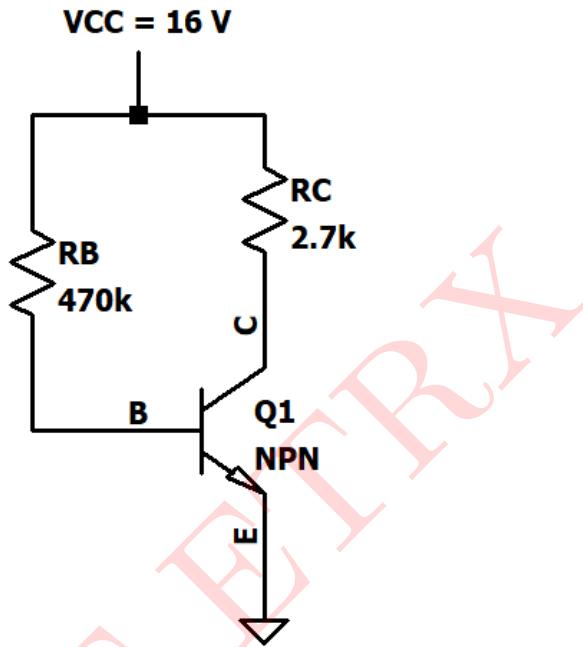


Figure 13: Circuit 5

Solution : The given circuit 5 is a Fixed-bias configuration

I_{BQ} :

I_{BQ} can be calculated by applying KVL to the input base-emitter loop.

$$V_{CC} - I_{BQ}R_B - V_{BE} = 0$$

$$I_{BQ}R_B = V_{CC} - V_{BE}$$

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_{BQ} = \frac{16 - 0.7}{470 \times 10^3} = 32.55 \mu A$$

I_{CQ} :

$$I_{CQ} = \beta I_{BQ}$$

$$I_{CQ} = 90 \times 32.55 \times 10^{-6} = 2.92 \text{ mA}$$

V_{CEQ} :

V_{CEQ} can be calculated by applying KVL to the output collector-emitter loop.

$$V_{CC} - I_{CQ}R_C - V_{CEQ} = 0$$

$$V_{CEQ} = V_{CC} - I_{CQ}R_C$$

$$V_{CEQ} = 16 - 2.92 \times 10^{-3} \times 2.7 \times 10^3 = 8.116 \text{ V}$$

V_C :

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 16 - 2.92 \times 10^{-3} \times 2.7 \times 10^3 = 8.116 \text{ V}$$

V_B :

$$V_B = V_{BE} + V_E$$

But, the emitter terminal is connected to ground.

$$\therefore V_E = 0 \quad \dots(1)$$

$$V_B = V_{BE} = 0.7 \text{ V}$$

V_E :

$$V_E = 0 \quad \dots(\text{from 1})$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below.

IBQ = 32.3365 μA
ICQ = 2.91029 mA
VCEQ = 8.14224 V
VC = 8.14224 V
VB = 0.801862 V
VE = 0 V
BETA = 90
.model NPN npn(bf=90)
.op

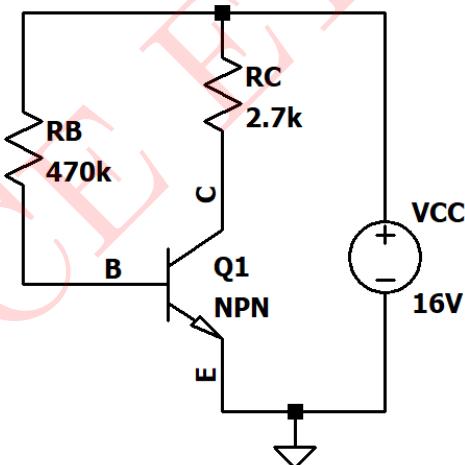


Figure 14: Circuit Schematic 5: Results

Comparison of theoretical and simulated values:

DC Parameters	Theoretical Values	Simulated Values
I_{BQ}	$32.55 \mu\text{A}$	$32.3365 \mu\text{A}$
I_{CQ}	2.92 mA	2.91029 mA
V_{CEQ}	8.116 V	8.1422 V
V_C	8.116 V	8.1422 V
V_B	0.7 V	0.8018 V
V_E	0 V	0 V

Table 5: Numerical 5

Numerical 6:

Determine the following for the emitter-stabilized circuit as shown in figure 15:

I_{BQ} , I_{CQ} , V_{CEQ} , V_C , V_B , V_E Given: $\beta = 100$

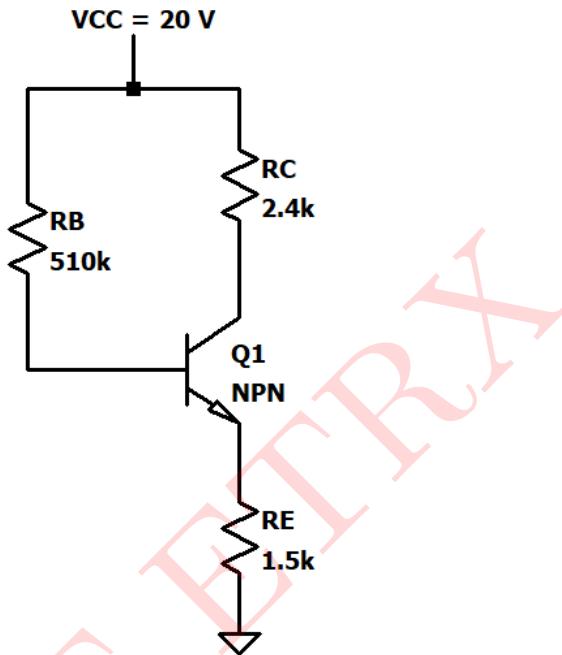


Figure 15: Circuit 6

Solution : The given circuit 6 is an emitter-bias configuration

I_{BQ} :

I_{BQ} can be calculated by applying KVL to the input base-emitter loop.

$$V_{CC} - I_{BQ}R_B - V_{BE} - I_E R_E = 0$$

$$I_{BQ}R_B + (1 + \beta)I_B R_E = V_{CC} - V_{BE} \quad (\because I_E = (1 + \beta)I_B)$$

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta)R_E}$$

$$I_{BQ} = \frac{20 - 0.7}{510 \times 10^3 + (1 + 100) \times 1.5 \times 10^3} = 29.17 \mu A$$

I_{CQ} :

$$I_{CQ} = \beta I_{BQ}$$

$$I_{CQ} = 100 \times 29.17 \times 10^{-6} = 2.91 \text{ mA}$$

$$\text{Also, } I_E = (1 + \beta)I_B$$

$$I_E = 101 \times 29.17 \times 10^{-6} = 2.94 \text{ mA}$$

V_{CEQ} :

V_{CEQ} can be calculated by applying KVL to the output collector-emitter loop.

$$V_{CC} - I_C R_C - V_{CEQ} - I_E R_E = 0$$

$$V_{CEQ} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CEQ} = 20 - 2.91 \times 10^{-3} \times 2.4 \times 10^3 - 2.94 \times 10^{-3} \times 1.5 \times 10^3 = \mathbf{8.606 \text{ V}}$$

V_C :

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 20 - 2.91 \times 10^{-3} \times 2.4 \times 10^3 = \mathbf{13.016 \text{ V}}$$

V_B :

$$V_B = V_{BE} + V_E$$

$$V_B = 0.7 + I_E R_E$$

$$V_B = 0.7 + 2.94 \times 10^{-3} \times 1.5 \times 10^3 = \mathbf{5.11 \text{ V}}$$

V_E :

$$V_E = I_E R_E$$

$$V_E = 2.94 \times 10^{-3} \times 1.5 \times 10^3 = \mathbf{4.41 \text{ V}}$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below.

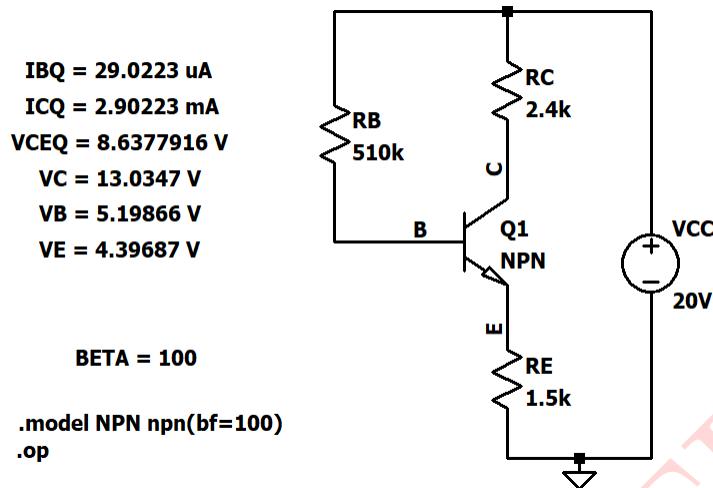


Figure 16: Circuit Schematic 6: Results

Comparison of theoretical and simulated values:

DC Parameters	Theoretical Values	Simulated Values
I_{BQ}	$29.17 \mu\text{A}$	$29.0223 \mu\text{A}$
I_{CQ}	2.91 mA	2.90223 mA
I_E	2.94 mA	2.93125 mA
V_{CEQ}	8.606 V	8.6377 V
V_C	13.016 V	13.0347 V
V_B	5.11 V	5.1986 V
V_E	4.41 V	4.3968 V

Table 6: Numerical 6

Numerical 7:

Consider the circuit shown in figure 17

- Determine R_{TH} , V_{TH} , I_{BQ} and V_{ECQ} for $\beta = 90$
- Determine the percentage change in I_{CQ} and V_{CEQ} if β is changed to $\beta = 150$

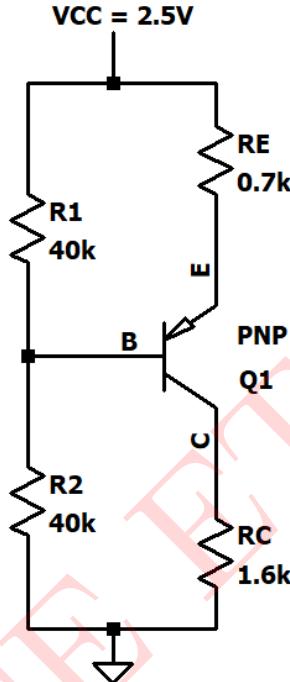


Figure 17: Circuit 7

Solution : The given circuit 7 is a voltage divider bias configuration employing pnp BJT transistor.

From Thevenin's Equivalent circuit:

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

$$V_B = \frac{2.5 \times 40 \times 10^3}{40 \times 10^3 + 40 \times 10^3} = 1.25 \text{ V}$$

or, $V_{TH} = 1.25 \text{ V}$

$$R_B = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_B = \frac{40 \times 10^3 \times 40 \times 10^3}{40 \times 10^3 + 40 \times 10^3} = 20 \text{ k}\Omega$$

or, $R_{TH} = 20 \text{ k}\Omega$

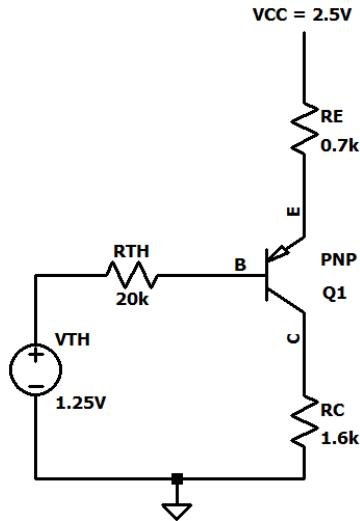


Figure 18: Thevenin's Equivalent Circuit

a. For $\beta = 90$:

I_{BQ} can be calculated by applying KVL to the input base-emitter loop,

$$V_{CC} - I_E R_E - V_{EB} - I_{BQ} R_{TH} - V_{TH} = 0$$

$$I_{BQ} R_{TH} + (1 + \beta) I_B R_E = V_{CC} - V_{EB} - V_{TH}$$

$$I_{BQ} = \frac{V_{CC} - V_{EB} - V_{TH}}{R_{TH} + (1 + \beta) R_E}$$

$$I_{BQ} = \frac{2.5 - 0.7 - 1.25}{20 \times 10^3 + 91 \times 0.7 \times 10^3} = 6.57 \mu A$$

We know, $I_{CQ} = \beta I_{BQ}$

$$I_{CQ} = 90 \times 6.57 \times 10^{-6} = 0.59 \text{ mA}$$

V_{ECQ} can be calculated by applying KVL to the output collector-emitter loop,

$$V_{CC} - I_E R_E - V_{EC} - I_C R_C = 0$$

$$V_{ECQ} = V_{CC} - I_E R_E - I_C R_C$$

$$V_{ECQ} = 2.5 - 0.59 \times 10^{-3} \times 0.7 \times 10^3 - 0.59 \times 10^{-3} \times 1.6 \times 10^3 \quad \dots (I_C \simeq I_E)$$

$$V_{ECQ} = 1.143 \text{ V}$$

b. β is changed from 90 to 150

I_{BQ} can be calculated by applying KVL to the input base-emitter loop,

$$V_{CC} - I_E R_E - V_{EB} - I_{BQ} R_{TH} - V_{TH} = 0$$

$$I_{BQ} R_{TH} + (1 + \beta) I_B R_E = V_{CC} - V_{EB} - V_{TH}$$

$$I_{BQ} = \frac{V_{CC} - V_{EB} - V_{TH}}{R_{TH} + (1 + \beta) R_E}$$

$$I_{BQ} = \frac{2.5 - 0.7 - 1.25}{20 \times 10^3 + 151 \times 0.7 \times 10^3} = 4.37 \mu A$$

We know, $I_{CQ} = \beta I_{BQ}$

$$I_{CQ} = 150 \times 4.37 \times 10^{-6} = 0.65 \text{ mA}$$

V_{ECQ} can be calculated by applying KVL to the output collector-emitter loop,

$$V_{CC} - I_E R_E - V_{EC} - I_C R_C = 0$$

$$V_{ECQ} = V_{CC} - I_E R_E - I_C R_C$$

$$V_{ECQ} = 2.5 - 0.65 \times 10^{-3} \times 0.7 \times 10^3 - 0.65 \times 10^{-3} \times 1.6 \times 10^3 \quad \dots (I_C \simeq I_E)$$

$$V_{ECQ} = 1.005 \text{ V}$$

Percent change in I_{CQ} and V_{ECQ} :

$$\%I_{CQ} = \frac{I_{CQ}(\beta = 150) - I_{CQ}(\beta = 90)}{I_{CQ}(\beta = 90)} \times 100$$

$$\%I_{CQ} = \frac{0.65 \times 10^{-3} - 0.59 \times 10^{-3}}{0.59 \times 10^{-3}} \times 100$$

$$\%I_{CQ} = 10.169\%$$

i.e Percent change in I_{CQ} increases.

$$\%V_{ECQ} = \frac{V_{ECQ}(\beta = 150) - V_{ECQ}(\beta = 90)}{V_{ECQ}(\beta = 90)} \times 100$$

$$\%V_{ECQ} = \frac{-1.143 + 1.005}{1.143} \times 100$$

$$\%V_{ECQ} = -12.073\%$$

i.e Percent change in V_{ECQ} decreases.

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below.

Comparison of theoretical and simulated values:

DC Parameters	Theoretical Values	Simulated Values
V_{TH}	1.25 V	1.32 V
R_{TH}	20 k Ω	20 k Ω

Table 7: Numerical 7

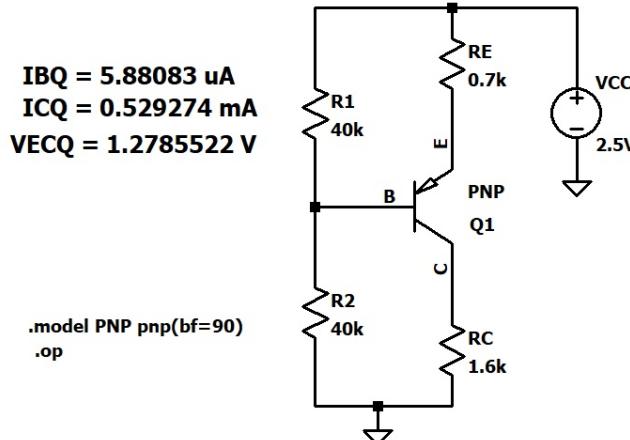


Figure 19: Circuit Schematic 7: Results

$$\beta = 90$$

DC Parameters	Theoretical Values	Simulated Values
I_{BQ}	$6.57 \mu\text{A}$	5.8808 mA
I_{CQ}	0.59 mA	0.5292 mA
V_{ECQ}	1.143 V	1.2785 V

Table 8: Numerical 7: a

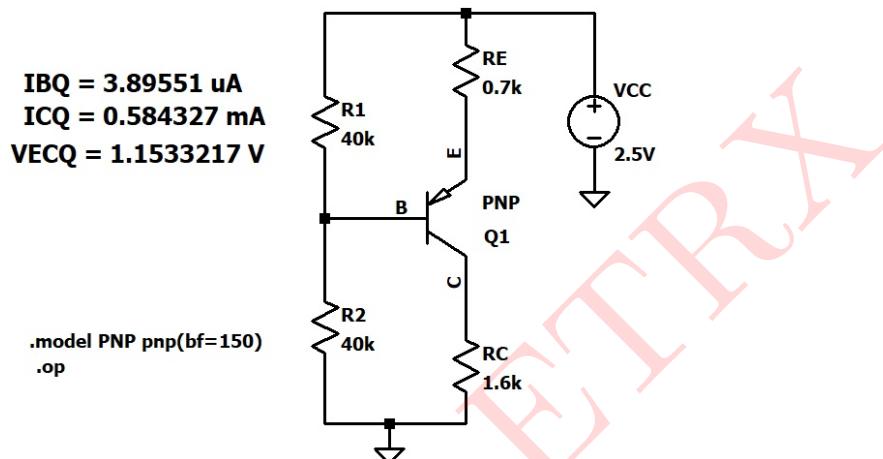


Figure 20: Circuit Schematic 7: Results

$$\beta = 150$$

DC Parameters	Theoretical Values	Simulated Values
I_{CQ}	0.65 mA	0.5843 mA
V_{ECQ}	1.005 V	1.1533 V
I_{BQ}	$4.37 \mu\text{A}$	$3.8955 \mu\text{A}$

Table 9: Numerical 7: b

Numerical 8:

Determine the Q-point values for the circuit 8. Given: $\beta = 50$

Repeat the same if all resistor values are reduced by a factor of 3.

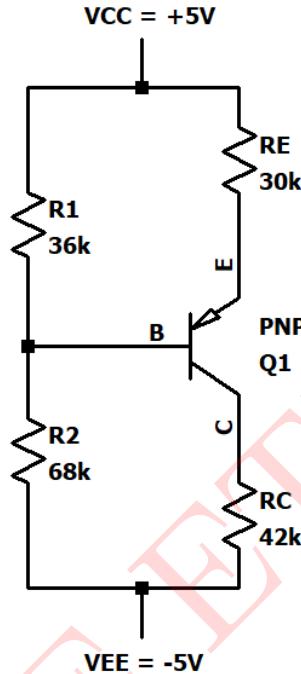


Figure 21: Circuit 8

Solution : The given circuit 8 is a voltage divider bias configuration employing pnp BJT transistor.

Q-points:

From Thevenin's equivalent circuit shown in figure 22,

$$R_{TH} = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_{TH} = \frac{36 \times 10^3 \times 68 \times 10^3}{36 \times 10^3 + 68 \times 10^3} = 23.54 \text{ k}\Omega$$

$$V_{TH} = \frac{R_2 \times (V_{CC} - V_{EE})}{R_1 + R_2} + V_{EE}$$

$$V_{TH} = \frac{68 \times 10^3 (5 + 5)}{36 \times 10^3 + 68 \times 10^3} - 5 = 1.538 \text{ V}$$

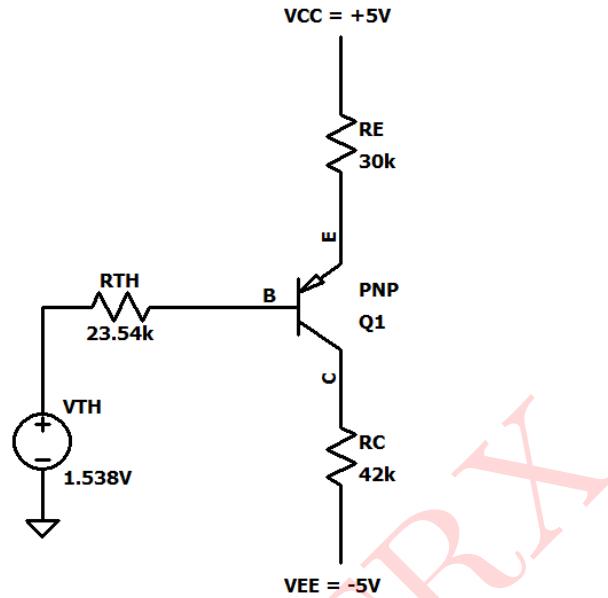


Figure 22: Thevenin's Equivalent Circuit

I_{BQ} can be calculated by applying KVL to the input base-emitter loop,

$$V_{CC} - I_E R_E - V_{EB} - I_{BQ} R_{TH} - V_{TH} = 0$$

$$I_{BQ} R_{TH} + (1 + \beta) I_B R_E = V_{CC} - V_{EB} - V_{TH}$$

$$I_{BQ} = \frac{V_{CC} - V_{EB} - V_{TH}}{R_{TH} + (1 + \beta) R_E}$$

$$I_{BQ} = \frac{5 - 0.7 - 1.538}{23.54 \times 10^3 + 51 \times 42 \times 10^3} = 1.77 \mu A$$

We know, $I_{CQ} = \beta I_{BQ}$

$$I_{CQ} = 50 \times 1.77 \times 10^{-6} = 8.85 \times 10^{-5} A$$

V_{ECQ} can be calculated by applying KVL to the output collector-emitter loop,

$$V_{CC} - I_E R_E - V_{EC} - I_C R_C - V_{EE} = 0$$

$$V_{ECQ} = V_{CC} - I_E R_E - I_C R_C - V_{EE}$$

$$V_{ECQ} = 5 - 8.85 \times 10^{-5} \times 30 \times 10^3 - 8.85 \times 10^{-5} \times 42 \times 10^3 + 5$$

$$V_{ECQ} = 3.628 V$$

$$\text{Q point} = (V_{ECQ}, I_{CQ}) = (3.628 V, 8.85 \times 10^{-5} A)$$

All the resistor values are reduced by 3.

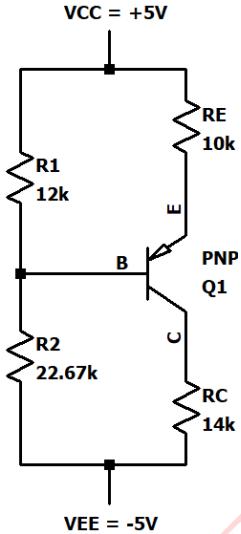


Figure 23: Circuit 9

From Thevenin's equivalent circuit shown in figure 24,

$$R_{TH} = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_{TH} = \frac{12 \times 10^3 \times 22.67 \times 10^3}{12 \times 10^3 + 22.67 \times 10^3} = 7.85 \text{ k}\Omega$$

$$V_{TH} = \frac{R_2 \times (V_{CC} - V_{EE})}{R_1 + R_2} + V_{EE}$$

$$V_{TH} = \frac{22.67 \times 10^3 (5 + 5)}{12 \times 10^3 + 2267 \times 10^3} - 5 = 1.538 \text{ V}$$

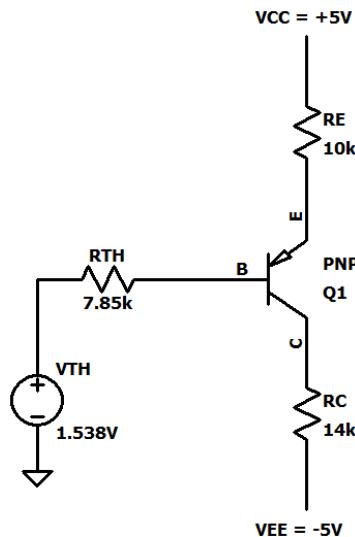


Figure 24: Thevenin's Equivalent Circuit

I_{BQ} can be calculated by applying KVL to the input base-emitter loop,

$$V_{CC} - I_E R_E - V_{EB} - I_{BQ} R_{TH} - V_{TH} = 0$$

$$I_{BQ}R_{TH} + (1 + \beta)I_B R_E = V_{CC} - V_{EB} - V_{TH}$$

$$I_{BQ} = \frac{V_{CC} - V_{EB} - V_{TH}}{R_{TH} + (1 + \beta)R_E}$$

$$I_{BQ} = \frac{5 - 0.7 - 1.538}{7.85 \times 10^3 + 51 \times 10 \times 10^3} = 5.33 \mu A$$

We know, $I_{CQ} = \beta I_{BQ}$

$$I_{CQ} = 50 \times 5.33 \times 10^{-6} = 2.665 \times 10^{-4} A$$

V_{ECQ} can be calculated by applying KVL to the output collector-emitter loop,

$$V_{CC} - I_E R_E - V_{EC} - I_C R_C = 0$$

$$V_{ECQ} = V_{CC} - I_E R_E - I_C R_C - V_{EE}$$

$$V_{ECQ} = 5 - 2665 \times 10^{-4} \times 10 \times 10^3 - 2.665 \times 10^{-4} \times 14 \times 10^3 - 5$$

$$V_{ECQ} = 3.604 V$$

$$Q \text{ point} = (V_{ECQ}, I_{CQ}) = (3.604 V, 2.665 \times 10^{-4} A)$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below.

Comparison of theoretical and simulated values:

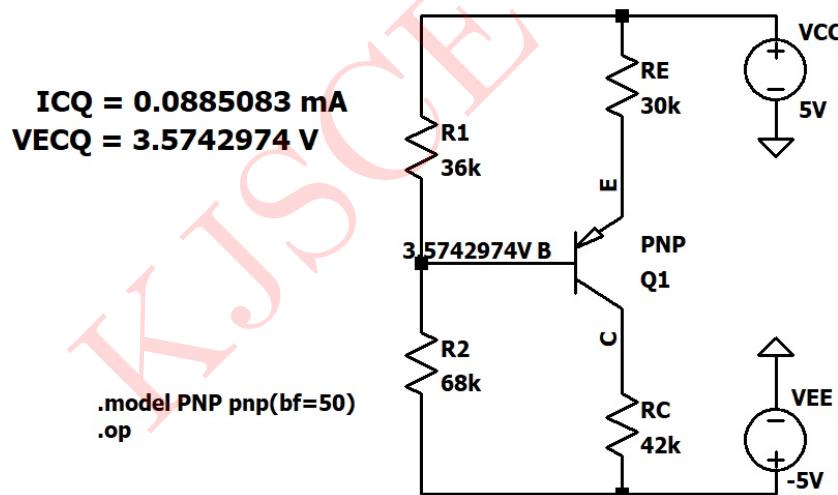


Figure 25: Circuit Schematic 8: Results

DC Parameters	Theoretical Values	Simulated Values
I_{CQ}	0.0885 mA	0.0885 mA
V_{ECQ}	3.628 V	3.5742 V

Table 10: Numerical 8

ICQ = 0.262775 mA
VECQ = 3.6408467 V

.model PNP pnp(bf=50)
.op

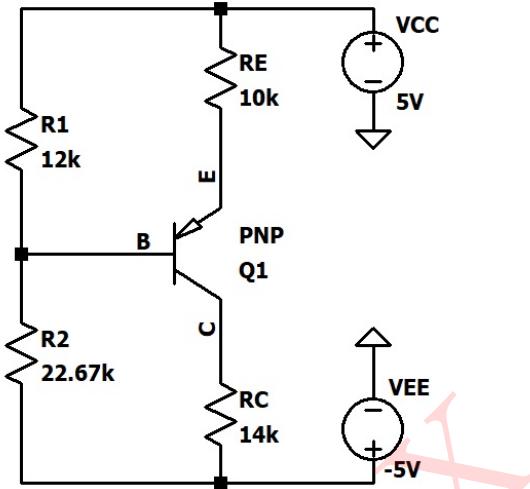


Figure 26: Circuit Schematic 9: Results

DC Parameters	Theoretical Values	Simulated Values
I_{CQ}	0.2665 mA	0.2627 mA
V_{ECQ}	3.604 V	3.6408 V

Table 11: Numerical 8:

Numerical 9:

The parameters of the NMOS amplifier are: $V_{DD} = 15 \text{ V}$, $R_1 = 600 \text{ k}\Omega$, $R_2 = 400 \text{ k}\Omega$, $R_L = 20 \text{ k}\Omega$, $R_{SR1} = 100 \Omega$, $R_{SR2} = 900 \Omega$, $R_D = 2.5 \text{ k}\Omega$, $C_1 = C_2 = C_S \simeq \infty$, $|V_M| \simeq \infty$, $k_n = 1 \text{ mA/V}^2$ & $V_T = 1.5 \text{ V}$

Calculate V_{GS} , I_D & V_{DS}

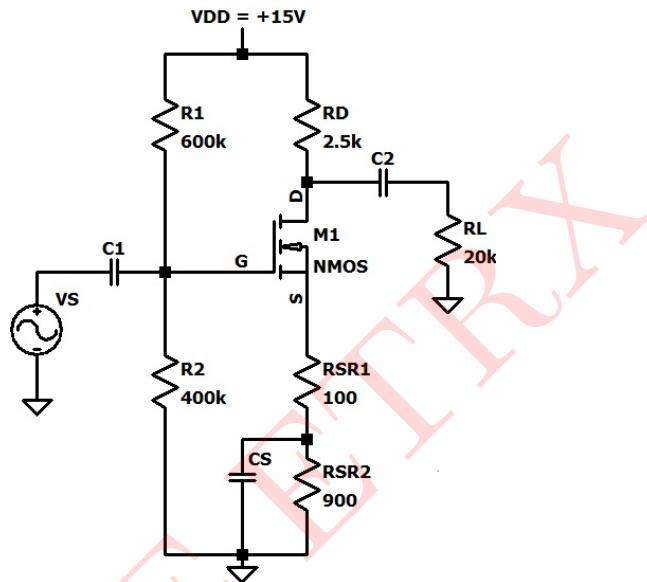


Figure 27: Circuit 10

Solution:

The given circuit 10 is a voltage divider bias configuration employing NMOS.

For DC biasing, the capacitors acts as an open circuited.

Also, R_{SR1} & R_{SR2} will be in series,

$$R_{SR1} + R_{SR2} = R_S$$

$$R_S = 100 + 900 = 1000 \Omega = 1 \text{ k}\Omega$$

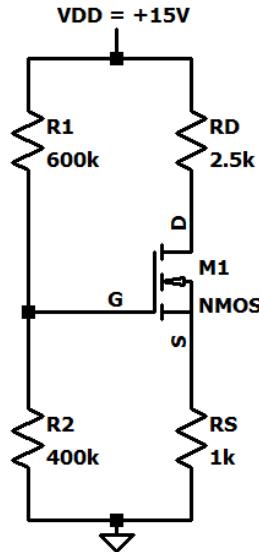


Figure 28: DC Equivalent circuit

From Thevenin's equivalent circuit shown in figure 29,

$$R_G = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_G = \frac{600 \times 10^3 \times 400 \times 10^3}{600 \times 10^3 + 400 \times 10^3} = 240\text{k}\Omega$$

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{15 \times 400 \times 10^3}{600 \times 10^3 + 400 \times 10^3} = 6 \text{ V}$$

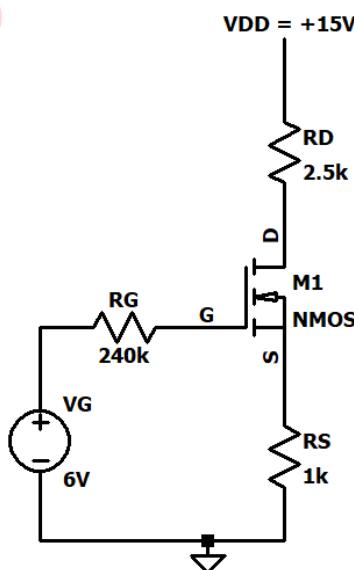


Figure 29: Thevenin's Equivalent Circuit

V_{GS} can be calculated by applying KVL to the input gate-source loop,

$$V_G - I_G R_G - V_{GS} - I_D R_S = 0$$

$$V_{GS} = V_G - I_D R_S$$

$$\dots (\because I_G = 0)$$

$$V_{GS} = 6 - I_D \times 1 \times 10^3 \quad \dots(1)$$

From current equation,

$$I_D = k_n(V_{GS} - V_T)^2$$

$$I_D = 1 \times 10^{-3}(6 - I_D \times 1 \times 10^3 - 1.5)^2 \quad \dots(\text{from 1})$$

$$I_D = 1 \times 10^{-3}(4.5 - I_D \times 1 \times 10^3)^2$$

$$I_D = 1 \times 10^{-3}(20.25 - 9 \times 10^3 \times I_D + 1 \times 10^6 \times I_D^2)$$

$$I_D = 20.25 \times 10^{-3} - 9I_D + 1 \times 10^3 \times I_D^2$$

$$1 \times 10^3 \times I_D^2 - 10 \times I_D + 20.25 \times 10^{-3} = 0$$

$$I_D = \mathbf{7.17 \text{ mA}} \text{ or } I_D = \mathbf{2.82 \text{ mA}}$$

Let, $I_D = 7.17 \text{ mA}$

$$V_{GS} = 6 - 7.17 \times 10^{-3} \times 1 \times 10^3$$

$$V_{GS} = 6 - 7.17 = \mathbf{-1.17 \text{ V}}$$

Let, $I_D = 2.82 \text{ mA}$

$$V_{GS} = 6 - 2.82 \times 10^{-3} \times 1 \times 10^3$$

$$V_{GS} = 6 - 2.82 = \mathbf{3.18 \text{ V}}$$

V_{GS} cannot be negative for mosfet.

$$\therefore I_D = \mathbf{2.82 \text{ mA}} \text{ & } V_{GS} = \mathbf{3.18 \text{ V}}$$

V_{DS} can be calculated by applying KVL to the output drain-source loop,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$V_{DS} = 15 - 2.82 \times 10^{-3} \times 2.5 \times 10^3 - 2.82 \times 10^{-3} \times 1 \times 10^3 = \mathbf{5.13 \text{ V}}$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

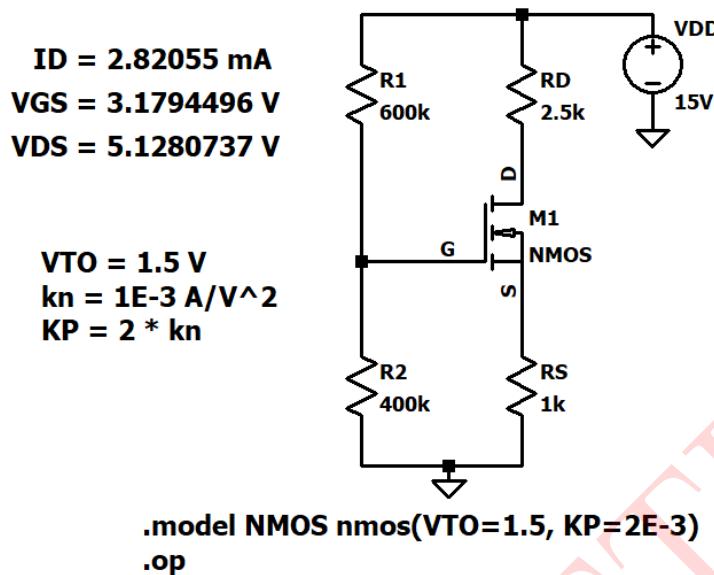


Figure 30: Circuit Schematic 10: Results

Comparison of theoretical and simulated values:

DC Parameters	Theoretical Values	Simulated Values
I_D	2.82 mA	2.8205 mA
V_{GS}	3.18 V	3.1794 V
V_{DS}	5.13 V	5.128 V

Table 12: Numerical 9

Numerical 10:

The parameters of the PMOS amplifier shown in figure 31 are:

$V_{DD} = 15 \text{ V}$, $R_1 = 500 \text{ k}\Omega$, $R_2 = 800 \text{ k}\Omega$, $R_L = 20 \text{ k}\Omega$, $R_{SR1} = 100 \Omega$, $R_{SR2} = 900 \Omega$, $R_D = 2.5 \text{ k}\Omega$, $C_1 = C_2 = C_S = \infty$, $|V_M| \simeq \infty$, $k_n = 1 \text{ mA/V}^2$ & $V_T = -2 \text{ V}$.

Calculate I_D , V_{SG} & V_{SD}

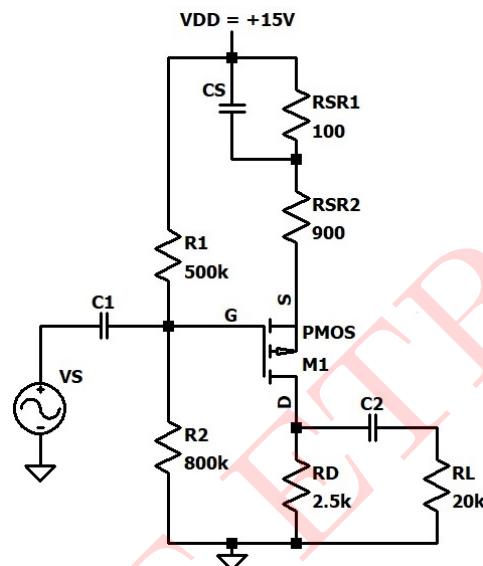


Figure 31: Circuit 11

Solution:

The given circuit 11 is a voltage divider bias configuration employing PMOS.

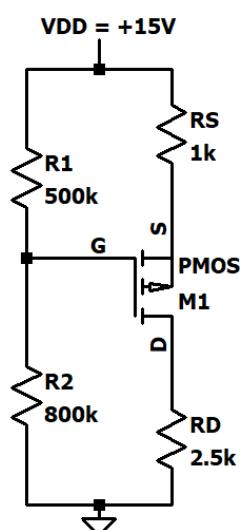


Figure 32: DC Equivalent circuit

From figure 32, R_{SR1} & R_{SR2} will be in series,

$$R_{SR1} + R_{SR2} = R_S$$

$$R_S = 100 + 900 = \mathbf{1000 \Omega = 1 k\Omega}$$

From Thevenin's equivalent circuit shown in figure 33,

$$R_G = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_G = \frac{500 \times 10^3 \times 800 \times 10^3}{500 \times 10^3 + 800 \times 10^3} = \mathbf{307.69 k\Omega}$$

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{15 \times 800 \times 10^3}{500 \times 10^3 + 800 \times 10^3} = \mathbf{9.23 V}$$

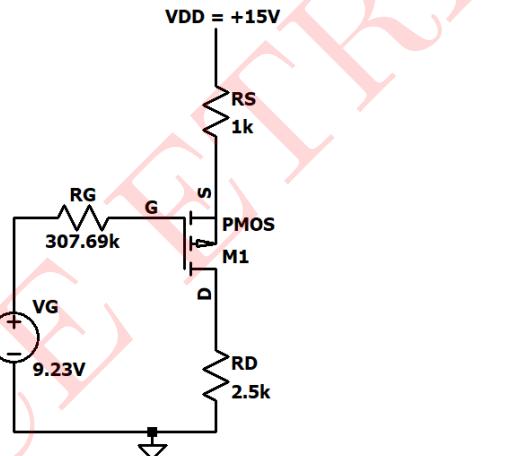


Figure 33: Thevenin's Equivalent Circuit

V_{SG} can be calculated by applying KVL to the input gate-source loop,

$$V_{DD} - I_D R_S - V_{SG} - I_G R_G - V_G = 0$$

$$V_{SG} = V_{DD} - I_D R_S - V_G$$

$$V_{SG} = 5.77 - I_D \times 1 \times 10^3$$

...($\because I_G = 0$)

...(1)

From current equation,

$$I_D = k_n(V_{SG} + V_T)^2$$

$$I_D = 1 \times 10^{-3}(5.77 - I_D \times 1 \times 10^3 - 2)^2 \quad \dots(\text{from 1})$$

$$I_D = 1 \times 10^{-3}(3.77 - I_D \times 1 \times 10^3)^2$$

$$I_D = 1 \times 10^{-3}(14.2129 - 7.54 \times 10^3 \times I_D + 1 \times 10^6 \times I_D^2)$$

$$I_D = 14.2129 \times 10^{-3} - 7.54 I_D + 1 \times 10^3 \times I_D^2$$

$$1 \times 10^3 \times I_D^2 - 8.54 \times I_D + 14.2129 \times 10^{-3} = 0$$

$$I_D = \mathbf{6.27 \text{ mA}} \text{ or } I_D = \mathbf{2.26 \text{ mA}}$$

Let, $I_D = 6.27 \text{ mA}$

$$V_{SG} = 5.77 - 6.27 \times 10^{-3} \times 1 \times 10^3$$

$$V_{SG} = 5.77 - 6.27 = -0.5 \text{ V}$$

Let, $I_D = 2.26 \text{ mA}$

$$V_{SG} = 5.77 - 2.26 \times 10^{-3} \times 1 \times 10^3$$

$$V_{SG} = 5.77 - 2.26 = 3.51 \text{ V}$$

V_{SG} cannot be negative for mosfet.

$$\therefore I_D = 2.26 \text{ mA} \text{ & } V_{SG} = 3.51 \text{ V}$$

V_{SD} can be calculated by applying KVL to the output drain-source loop,

$$V_{DD} - I_D R_D - V_{SD} - I_D R_S = 0$$

$$V_{SD} = V_{DD} - I_D R_S - I_D R_D$$

$$V_{SD} = 15 - 2.26 \times 10^{-3} \times 1 \times 10^3 - 2.26 \times 10^{-3} \times 2.5 \times 10^3 = 7.09 \text{ V}$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

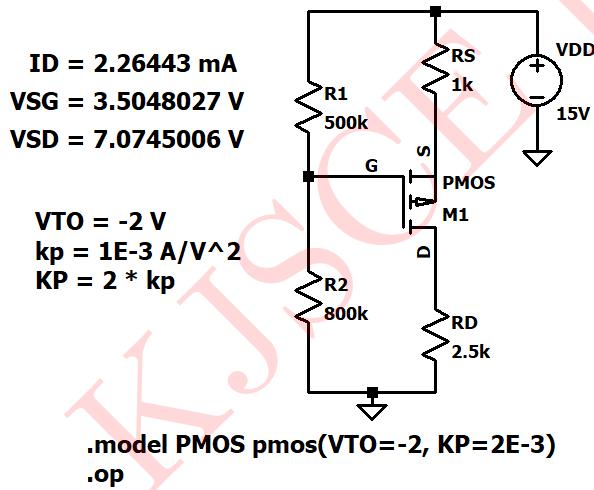


Figure 34: Circuit Schematic 11: Results

Comparison of theoretical and simulated values:

DC Parameters	Theoretical Values	Simulated Values
I_D	2.26 mA	2.2644 mA
V_{GS}	3.51 V	3.5048 V
V_{DS}	7.01 V	7.0745 V

Table 13: Numerical 10
