K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
DC Biasing Circuit

Numerical 1: Determine V_C and V_B for the network shown in figure 1. Given $\beta = 120$.

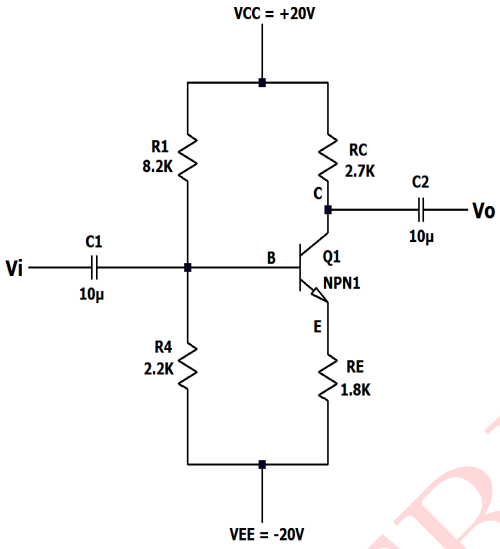

Figure 1: Circuit 1

Solution: The above circuit is a voltage divider bias configuration

DC equivalent circuit: For DC analysis, f = 0 so $X_C = \dfrac{1}{2\pi fc} = \infty$. Thus capacitor act as open circuit.

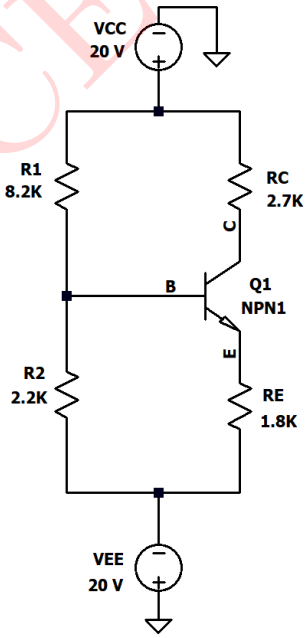

Figure 2: Circuit with capacitor open circuited

Determining Thevenin equivalent circuit:-
First, we find R_{TH} :-

$R_{TH} = R_1 \ || \ R_2 = 8.2k\Omega \ || \ 2.2k\Omega = 1.73k\Omega$

Finding out V_{TH} :-

$$V_{TH} = \left(\frac{V_{CC} + V_{EE}}{R_1 + R_2}\right) R_2 - V_{EE} \qquad \text{(where } V_{EE} = 20V \text{)}$$

$$V_{TH} = \left(\frac{20 + 20}{8.2k + 2.2k}\right) 2.2k - 20 = \frac{40}{10.4k} \times 2.2k - 20 = \mathbf{-11.53846V}$$

Thevenin equivalent circuit :-

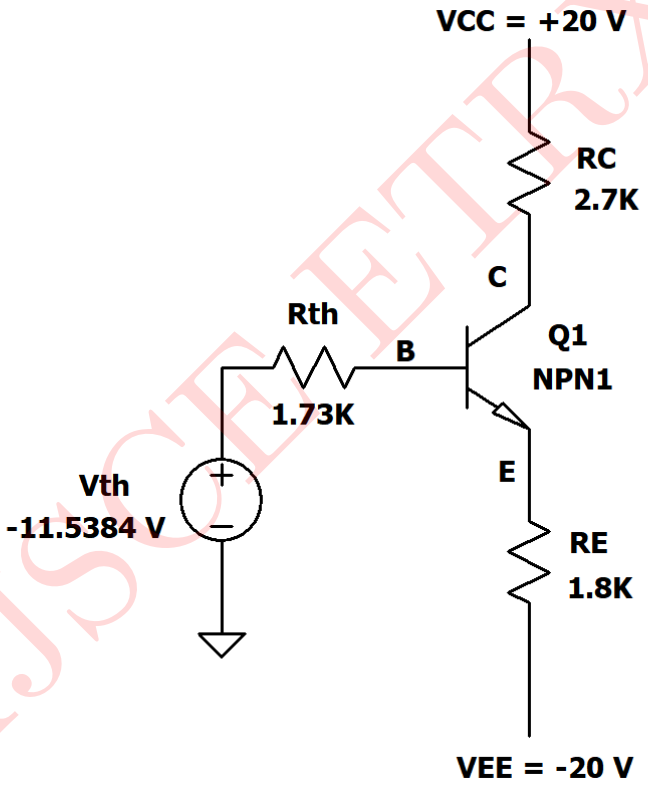

Figure 3: Thevenin Equivalent circuit

Applying KVL to the emitter - base loop:

$-V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E + V_{EE} = 0$

We know, $I_E = (\beta + 1) I_B$

$V_{EE} - V_{TH} - I_B R_{TH} - V_{BE} - (1 + \beta) I_B R_E = 0$

$$I_B = \frac{V_{EE} - V_{TH} - V_{BE}}{R_{TH} + (1 + \beta) R_E} = \frac{7.77}{1.73k + (121)(1.8k)} = \mathbf{35.07\mu A}$$

$I_C = \beta I_B = 120 \times 35.07 \times 10^{-6} = \mathbf{4.2mA}$

$I_E = (1 + \beta) I_B = 121 \times 35.07 \times 10^{-6} = \mathbf{4.24mA}$

$V_C = V_{CC} - I_C R_C = 20 - 4.2 \times 10^{-3}(2.7 \times 10^3) = \mathbf{8.6V}$

$V_B = -V_{TH} - I_B R_{TH} = -11.53 - (35.07 \times 10^{-6})(1.73 \times 10^{-3}) = \mathbf{-11.59V}$

SIMULATED RESULTS

Above circuit is simulated in LTspice and the result is as follows:

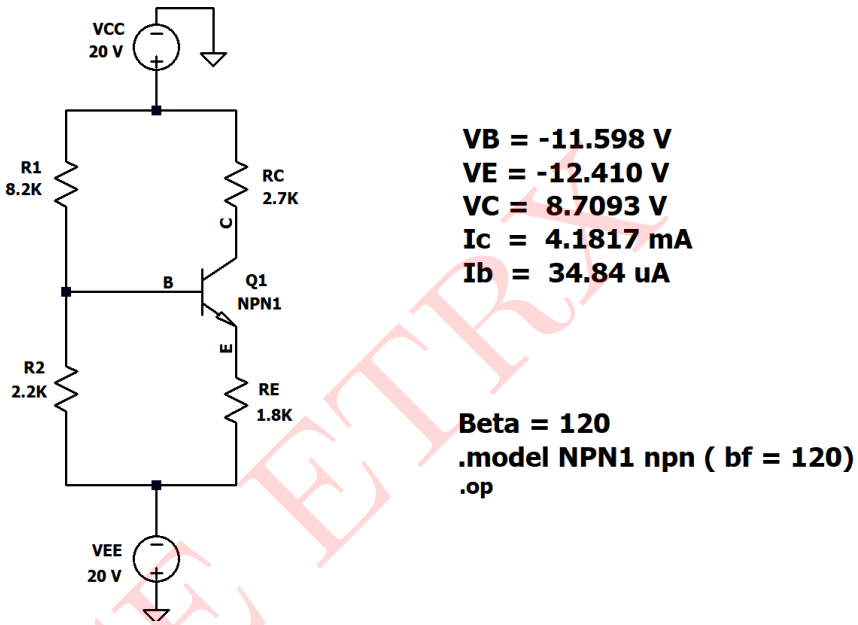

Figure 4: Circuit schematic: Results

Comparison between Theoretical and Simulated values :-

Parameter	Theoretical	Simulated
I_B	$35.07\mu A$	$34.87\mu A$
I_C	4.2 mA	4.182 mA
V_B	$-11.59V$	$-11.598V$
V_C	8.6 V	8.7 V

Table 1: Numerical 1

Numerical 2: Determine V_{CE} for the voltage divider bias configuration, given in figure 5.

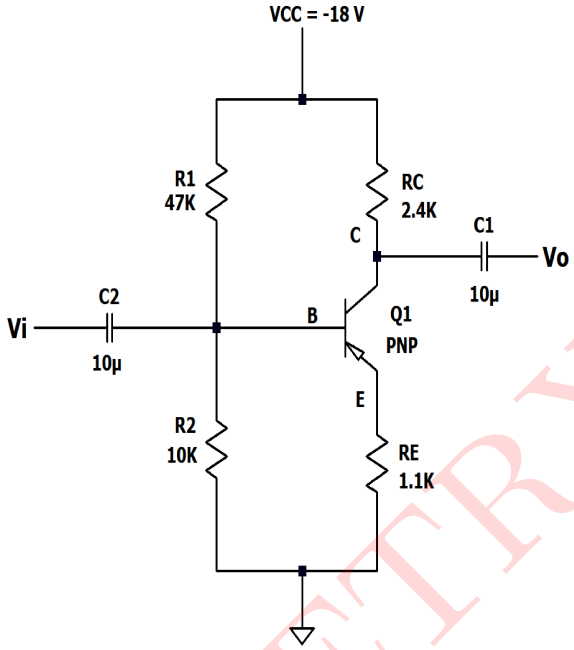

Figure 5: circuit 2

Solution: The above circuit is a voltage divider bias configuration

DC equivalent circuit : For DC analysis, f = 0 so $X_C = \dfrac{1}{2\pi fc} = \infty$. Thus capacitor act as open circuit

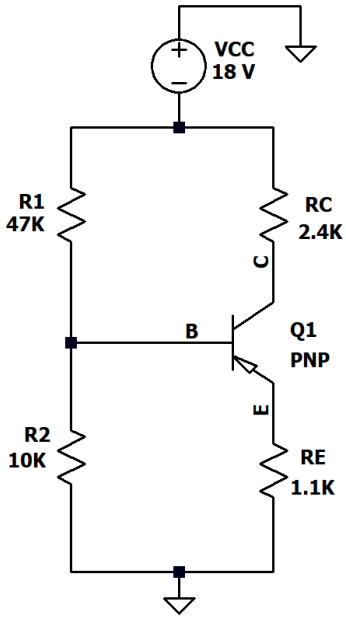

Figure 6: Circuit after capacitors are open circuited

Determining Thevenin equivalent circuit:

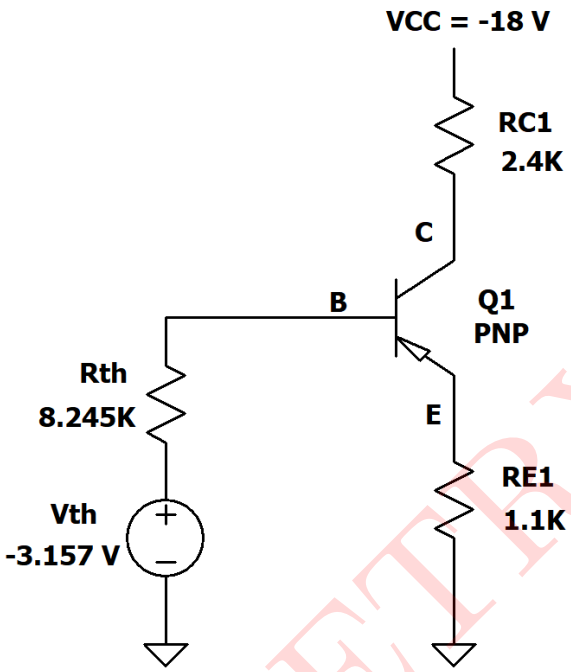

Figure 7: Thevenin Equivalent circuit

Where, $V_{TH} = \dfrac{V_{CC} \times R_2}{R_1 + R_2} = \dfrac{-18 \times 10k}{10k + 47k} = \mathbf{-3.157V}$

And $R_{TH} = R_1 \parallel R_2 = \mathbf{8.2456k\Omega}$

Finding V_E, I_E and V_{CE} :-

Applying Kirchoff's law,

$V_B - V_E = V_{BE}$

$V_E = V_B - V_{BE}$

Here $V_B = V_{TH}$

$V_E = -3.157 - 0.7 = \mathbf{-2.457V}$

$I_E = \dfrac{V_E}{R_E} = \dfrac{2.457}{1.1k} = \mathbf{2.2336mA}$

Applying KVL to collector - emitter loop:-

$I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$

$I_E \approx I_C$

$V_{CE} = -V_{CC} + I_C(R_C + R_E) = -18 + (2.24 \times 10^{-3})(2.4k + 1.1k) = -18 + 7.84 = \mathbf{-10.16V}$

SIMULATED RESULTS:
Above circuit is simulated in LTspice and the result is as follows:

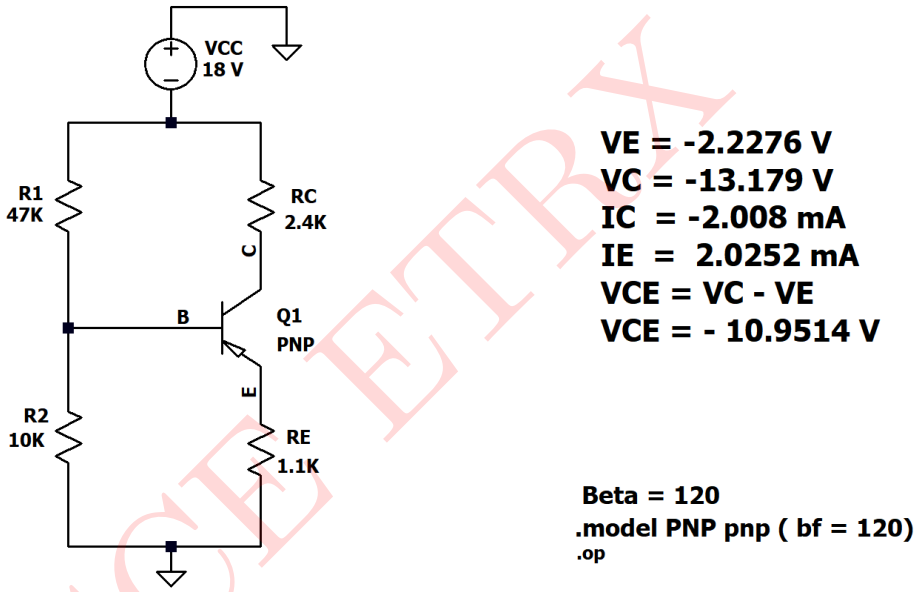

Figure 8: Circuit schematic results

Comparison between Theoretical and practical value :-

Parameter	Theoretical	Simulated
V_E	-2.457 V	-2.2268 V
V_{CE}	-10.16 V	-10.95 V
I_E	2.2336 mA	2.024 mA

Table 2: Numerical 2

Numerical 3: For the circuit shown below determine I_C, V_C, V_E and V_{CE}. Given $\beta = 100$

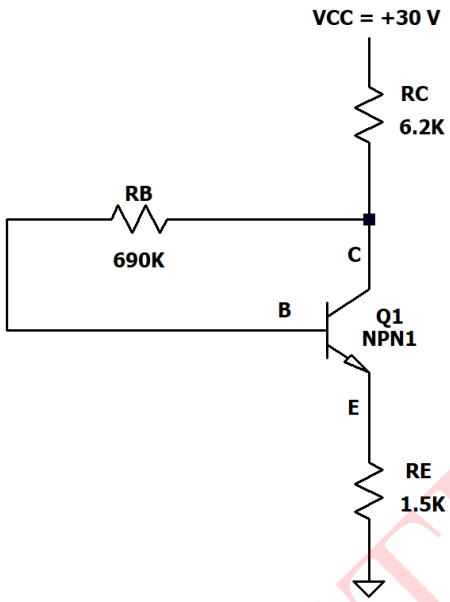

Figure 9: Circuit 3

Solution: The given circuit is a collector to base bias circuit employing npn bjt transistor.

DC equivalent circuit:

From figure 9,

Current passing through R_C is $(I_C + I_B)$

Current passing through R_B is I_B

Current passing through R_E is $(I_C + I_B)$

DC analysis:

Applying KVL to the input loop.

$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} - (I_B + I_C)R_E = 0$

But $I_C = \beta I_B$

$V_{CC} - (I_B + \beta I_B)R_C - I_B R_B - V_{BE} - (I_B + \beta I_B)R_E = 0$

$V_{CC} - I_B(1+\beta)R_C - I_B R_B - V_{BE} - I_B(1+\beta)R_E = 0$

$V_{CC} - V_{BE} = I_B[(1+\beta)R_C + R_B + R_E(1+\beta)] = I_B[R_B + (1+\beta)(R_E + R_C)]$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)} = \frac{30 - 0.7}{690 \times 10^3 + (1+100)(6.2+1.5)10^3} = \frac{29.3}{(690 + 777.7) \times 10^3}$$

$I_B = \mathbf{19.96\mu A}$

But $I_C = \beta I_B = 100 \times 19.96 \times 10^{-6} = \mathbf{1.996mA}$

Finding V_C:

Applying KVL to collector - emitter loop.

$V_C = V_{CC} - (I_B + I_C)R_C = 30 - (19.96 \times 10^{-6} + 1.996 \times 10^{-3})(6.2 \times 10^3)$

$V_C = 30 - 12.498 = \mathbf{17.50V}$

$V_E = (I_B + I_C)R_E = (19.96 \times 10^{-6} + 1.996 \times 10^{-3})(1.5 \times 10^3)\mathbf{3.023V}$

$V_{CE} = V_C - V_E = 17.50 - 3.023 = \mathbf{14.476V}$

SIMULATED RESULTS

Above circuit is simulated in LTspice and the result is as follows:

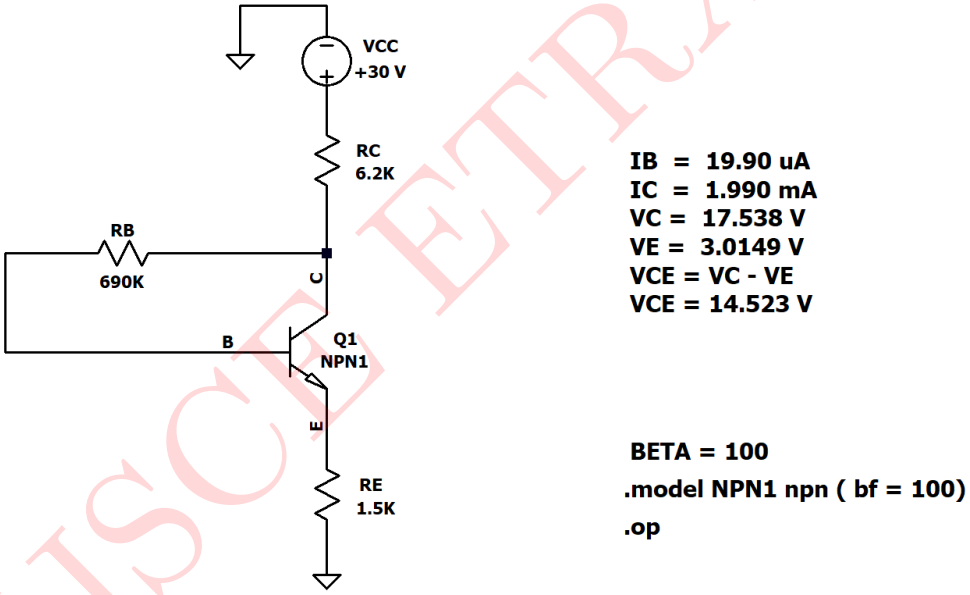

Figure 10: Circuit schematic: Results

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
I_B	19.90μA	19.96μA
I_C	1.990 m A	1.996 mA
V_C	17.538V	117.5V
V_E	3.0149 V	3.023 V
V_{CE}	14.523 V	14.476 V

Table 3: Numerical 3

Numerical 4: Calculate DC collector current I_C and voltage V_C for the bias circuit shown below. Given $\beta = 75$

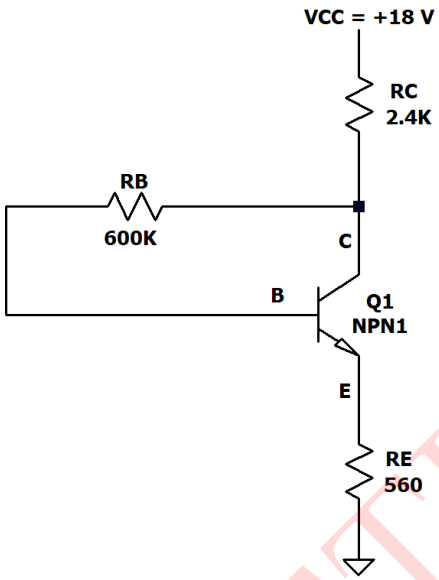

Figure 11: Circuit 4

Solution: The given circuit is a collector to base bias circuit employing npn bjt transistor.

DC equivalent circuit:

From figure 11,

Current passing through R_C is $(I_C + I_B)$

Current passing through R_B is I_B

Current passing through R_E is $(I_C + I_B)$

DC analysis:-

Applying KVL to the input loop.

$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} - (I_B + I_C)R_E = 0$

But $I_C = \beta I_B$

$V_{CC} - (I_B + \beta I_B)R_C - I_B R_B - V_{BE} - (I_B + \beta I_B)R_E = 0$

$V_{CC} - I_B(1+\beta)R_C - I_B R_B - V_{BE} - I_B(1+\beta)R_E = 0$

$V_{CC} - V_{BE} = I_B[(1+\beta)R_C + R_B + R_E(1+\beta)] = I_B[R_B + (1+\beta)(R_E + R_C)]$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)} = \frac{18 - 0.7}{600 \times 10^3 + (1+75)(2.4 + 0.56)10^3} = \frac{17.3}{824.96 \times 10^3}$$

$I_B = \mathbf{20.97\mu A}$

But $I_C = \beta I_B = 75 \times 20.97 \times 10^{-6} = \mathbf{1.57mA}$

Finding V_{CE}:

$V_{CE} = V_{CC} - (I_B + I_C)(R_C + R_E) = 18 - (20.9 \times 10^{-6} + 1.57 \times 10^{-3})(2.4 + 0.56)10^3$

$V_{CE} = 18 - 4.709 = \mathbf{13.290V}$

SIMULATED RESULTS

Above circuit is simulated in LTspice and the result is as follows:

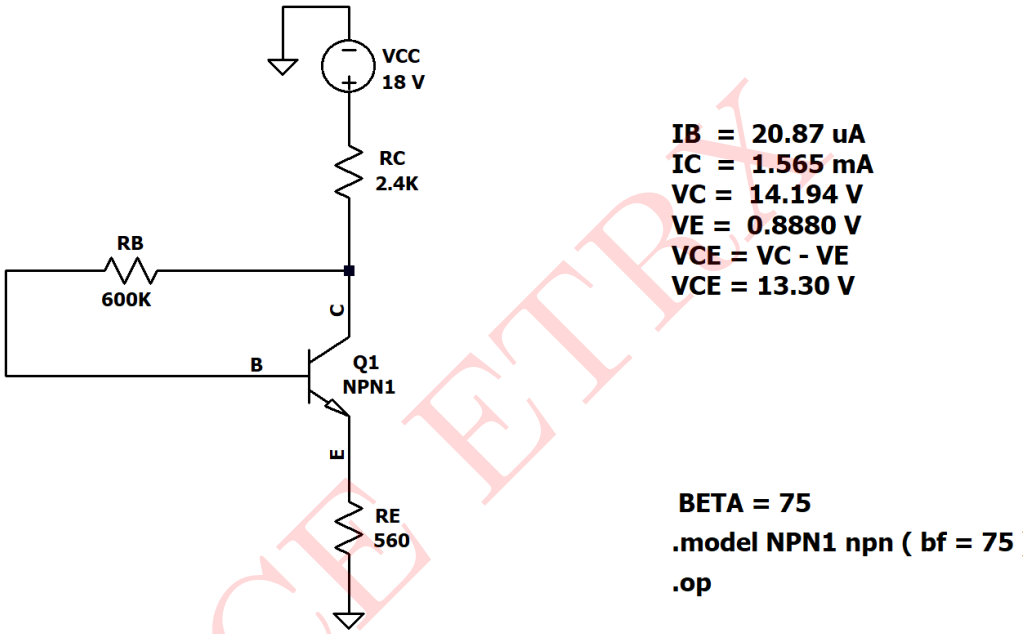

Figure 12: Circuit schematic: Results

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
I_B	$20.87\mu A$	$20.97\mu A$
I_C	1.565 mA	1.57 mA
V_{CE}	13.30 V	13.29 V

Table 4: Numerical 4

Numerical 5: For the network given below determine: I_B, I_C, V_E, V_{CE}. Given $\beta = 130$

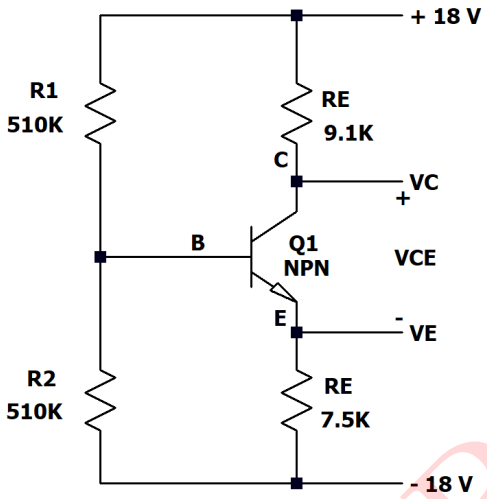

Figure 13: Circuit 5

Solution: The given circuit is a voltage divider bias configuration.

DC equivalent circuit:

Refer to figure 13 for DC equivalent circuit.

Finding Thevenin's equivalent circuit:

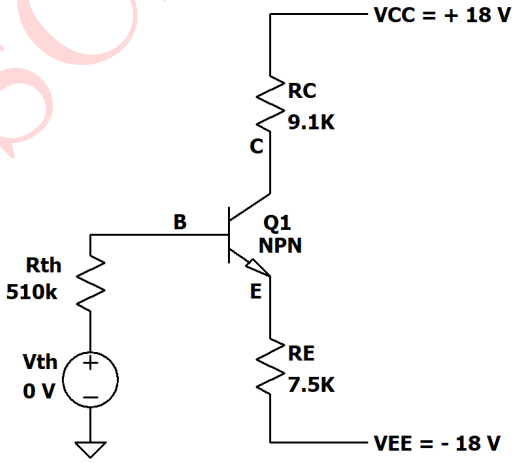

Figure 14: Thevenin's equivalent circuit

Where, $R_{TH} = R_1 \ || \ R_2 = 510k \ || \ 510k = \mathbf{255k\Omega}$

$$V_{TH} = \left(\frac{V_{CC} - V_{EE}}{R_1 + R_2}\right) R_2 + V_{EE} \qquad \text{(here, } V_{EE} = -18V\text{)}$$

$$V_{TH} = \left(\frac{18 + 18}{510k + 510k}\right) 510k - 18 = 18 - 18 = \mathbf{0}$$

Applying KVL to base- emitter loop:

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E - V_{EE} = 0$$

But $I_E = (\beta + 1) I_B$ and $V_{TH} = 0$

$$-I_B R_{TH} - V_{BE} - (1 + \beta) R_E I_B - V_{EE} = 0$$

$$V_{BE} + V_{EE} = -I_B [R_{TH} (1 + \beta) R_E]$$

$$I_B = -\frac{[V_{BE} + V_{EE}]}{R_{TH} + (1 + \beta) R_E} = -\frac{-18 + .07}{[255k + (131)7.5k]} = \frac{17.3}{1237.5 \times 10^3} = \mathbf{13.97\mu A}$$

Now, $I_C = \beta I_B = 130 \times 13.97 \times 10^{-6} = \mathbf{1.81mA}$

$$V_E - I_E R_E - V_{EE} = 0$$

$$V_E = (1 + \beta) I_B R_E + V_{EE} = 131(13.97 \times 10^{-6})(7.5 \times 10^3) + (-18) = 13.725 - 18 = \mathbf{-4.3V}$$

Applying KVL to the collector-emitter loop:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E - V_{EE} = 0$$

$$V_{CE} = V_{CC} - V_{EE} - I_C R_C - (1 + \beta) I_B R_E$$

$$V_{CE} = 18 + 18 - (1.81 \times 10^{-3})(9.1 \times 10^3) - 131(13.97 \times 10^{-6})7500 = 19.529 - 13.725 = \mathbf{5.803V}$$

SIMULATED RESULTS

Above circuit is simulated in LTspice and the result is as follows:

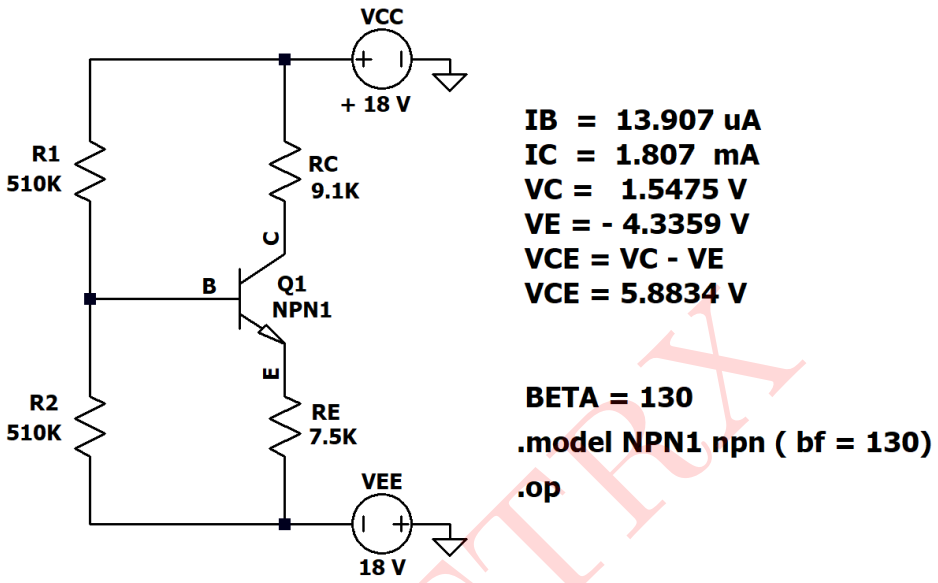

Figure 15: Circuit schematic: Results

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
I_B	13.907μA	13.97μA
I_C	1.807 m A	1.81 mA
V_E	$-4.33V$	$-4.3V$
V_{CE}	5.88 V	5.803 V

Table 5: Numerical 5

Numerical 6: For the network given below determine: I_E, V_C, V_{CE}. Given $\beta = 120$

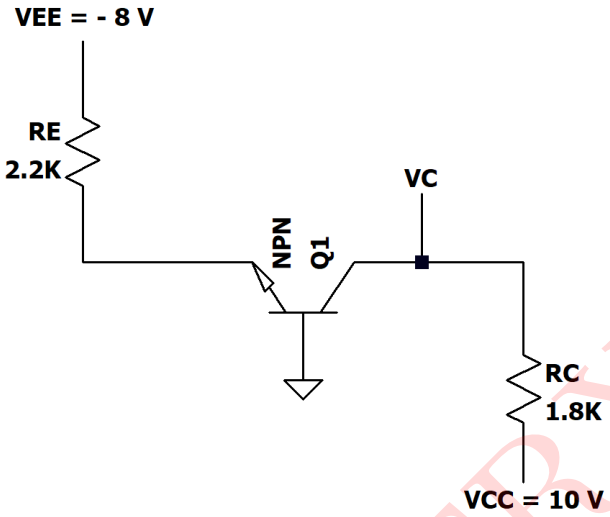

Figure 16: Circuit 6

Solution:

Refer to figure 16 for DC equivalent circuit.

Applying KVL to the base - emitter loop:

$$-V_{BE} - I_E R_E - V_{EE} = 0 \tag{1}$$

$$I_E = -\frac{V_{EE} - V_{BE}}{R_E} = \frac{8 - 0.7}{2.2 \times 10^3} = \frac{7.3}{2.2 \times 10^3} = \mathbf{3.318mA}$$

$$V_{CC} - I_C R_C - V_C = 0$$

$$V_C = 10 - (3.318 \times 10^{-3})(1.8 \times 10^3) = V_C = \mathbf{4.0276V} \qquad (\text{As } I_C \approx I_E)$$

Applying KVL to the collector - emitter loop:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E - V_{EE} = 0$$

$$V_{CE} = V_{CC} - V_{EE} - I_E(R_E + R_C) = 10 + 8 - (3.318 \times 10^{-3})(1.8 + 2.2)10^3 = \mathbf{4.728V}$$

(As $I_C \approx I_E$)

SIMULATED RESULTS

Above circuit is simulated in LTspice and the result is as follows:

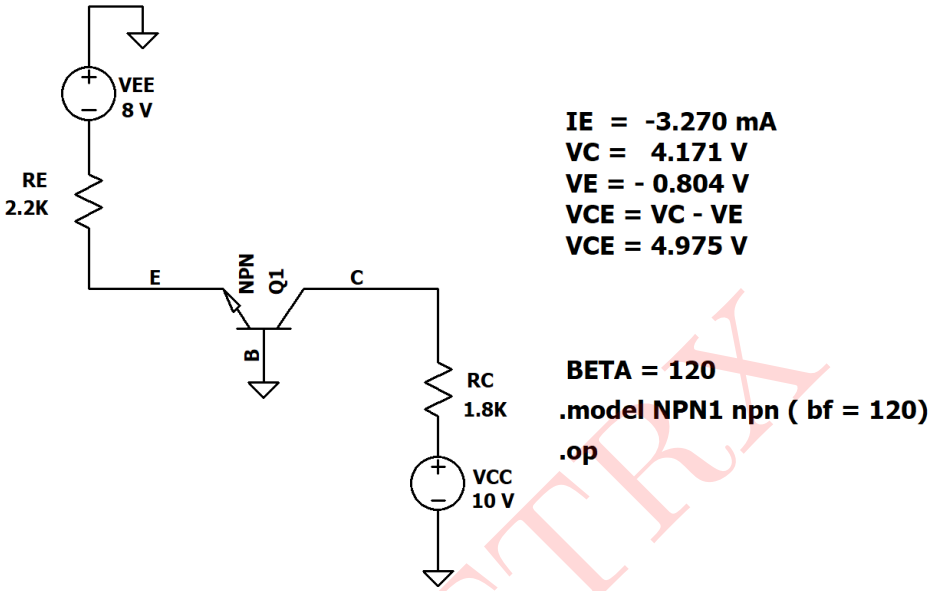

Figure 17: Circuit schematic: Results

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
I_E	3.318 mA	3.270 mA
V_C	4.027 V	4.171 V
V_{CE}	4.728 V	4.97 V

Table 6: Numerical 6

Numerical 7: Consider the circuit shown below, the transistor parameters are $V_{TP} = -0.8V$ and $K_P = 0.5mA/V^2$. Determine I_D, V_{GS}, V_{SD}

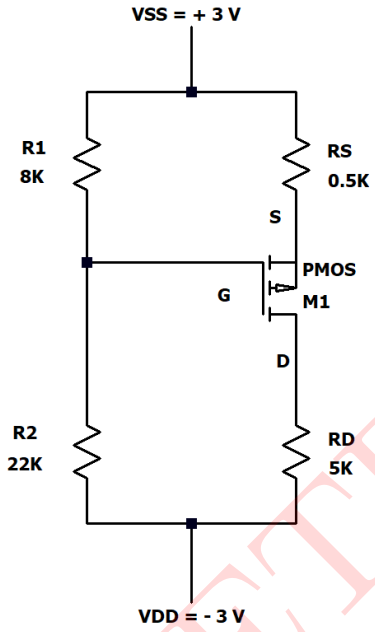

Figure 18: Circuit 7

Solution: The given circuit is a voltage divider configuration employing a Enhancement type PMOSFET.

Refer to figure 18 for DC equivalent circuit.

Thevenin's equivalent circuit:

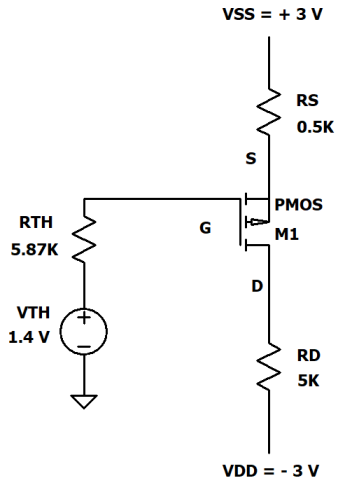

Figure 19: Thevenin's equivalent circuit

Where, $R_G = R_{TH} = R_1 \ || \ R_2 = 8k \ || \ 22k = \mathbf{5.87k\Omega}$

$$V_{TH} = \left(\frac{V_{SS} - V_{DD}}{R_1 + R_2}\right) R_2 + V_{EE}$$

$$V_{TH} = \left(\frac{3+3}{8k+22k}\right) 22k - 3 = \mathbf{1.4V}$$

Applying KVL to Source - Gate loop:

$$V_{SS} - I_S R_S - V_{SG} - I_G R_G - V_{TH} = 0$$

$$\therefore I_S R_S = -V_{GS} - V_{TH} + V_{SS} - R_G R_G$$

But $I_G = 0$ and $V_{GS} = -V_{GS}$ and $I_S \approx I_D$

$$I_D R_S = V_{GS} - V_{TH} + V_{SS}$$

$$I_D = -\frac{V_{GS} - V_{TH} + V_{SS}}{R_S} = -\frac{V_{GS} - 1.4 + 3}{0.5 \times 10^3}$$

$$I_D = -\frac{V_{GS} + 1.6}{1.6 \times 10^3} \qquad .....(1)$$

Also for PMOS of enhancement type, in saturation region.

$$I_D = k_P(V_{GS} - V_{TP})^2 \qquad \text{Where } V_{TP} = -0.8V$$

$$I_D = k_P(V_{GS}^2 - 2V_{GS}V_{TP} + V_{TP}^2) = 0.5 \times 10^{-3}(V_{GS}^2 + 2 \times 0.8V_{GS} + V_{TP}^2)$$

$$I_D = 0.5 \times 10^{-3}(V_{GS}^2 + 1.6V_{GS} + 0.64) \qquad .....(2)$$

From (1) and (2);

$$\frac{V_{GS} + 1.6}{0.5 \times 10^3} = 0.5 \times 10^{-3}(V_{GS}^2 + 1.6V_{GS} + 0.64)$$

$$\therefore V_{GS} + 1.6 = 0.25(V_{GS}^2 + 1.6V_{GS} + 0.64)$$

$$\therefore 0.25V_{GS}^2 + 0.4V_{GS} \times 0.16 - 1.6 - V_{GS} = 0$$

$$\therefore 0.25V_{GS}^2 + 0.4V_{GS} - V_{GS} - 1.44 = 0$$

$$V_{GS} = 3.88V \text{ or } -1.48V$$

Since $|V_{GS}| < |V_P|$

$$V_{GS} = -1.48V$$

$$V_{SG} = 1.48V$$

$$I_D = \frac{V_{GS} + 1.6}{0.5 \times 10^3} = \frac{0.12}{0.5 \times 10^3} = \mathbf{0.24mA}$$

Applying KVL for source Drain loop,

$$V_{SS} - I_S R_S - V_{SD} - I_D R_D - V_{DD} = 0$$

$$\therefore I_S \approx I_D$$

$V_{SD} = V_{SS} - V_{DD} - I_D(R_D + R_S) = 3 + 3 - (0.2 \times 100^{-3})(5.5 \times 10^3) = \mathbf{5V}$

SIMULATED RESULTS

Above circuit is simulated in LTspice and the result is as follows:

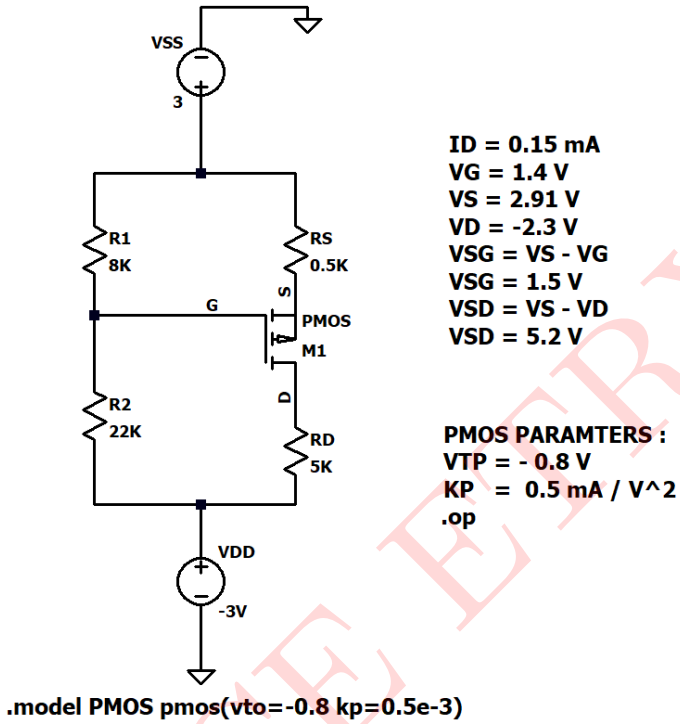

Figure 20: Circuit schematic: Results

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
I_D	0.2 mA	0.15 mA
V_{SG}	1.48 V	1.5V
V_{SD}	5 V	5.2 V

Table 7: Numerical 7

Numerical 8: Consider the circuit shown in figure 21, Determine I_{DQ}, V_{GSQ}, V_{DSQ}, where $V_P = -5V$ and $I_{DSS} = 10mA$

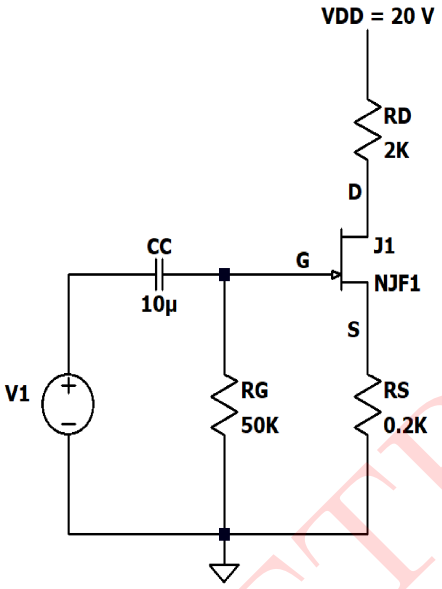

Figure 21: Circuit 8

Solution: DC Analysis

For DC analysis $f = 0 \therefore X_C = \dfrac{1}{2\pi fc} = \infty$

$\therefore$ Capacitor acts as a open circuit

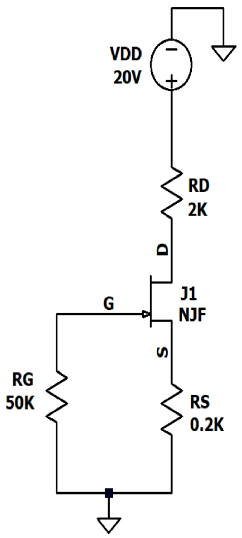

Figure 22: Thevenin's equivalent circuit

Applying KVL to Gate - Source loop:

$-I_S R_S - V_{GS} - I_G R_G = 0$

But for JFET; $I_G = 0$

$\therefore V_{GS} = -I_S R_S$ and $I_S = I_D$

$V_{GS} = I_D R_S = -0.2 \times 10^3 \times I_D$ .....(1)

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10 \times 10^{-3}\left(1 - \frac{V_{GS}}{5}\right)^2$ .....(2)

From (1) and (2);

$\frac{-V_{GS}}{0.2 \times 10^3} = 10 \times 10^{-3}\left(1 + \frac{V_{GS}}{5}\right)^2$

$\therefore V_{GS} = 2\left(1 + \frac{2V_{GS}}{5} + \frac{V_{GS}^2}{25}\right)$

$\therefore 2 + \frac{4V_{GS}}{5} + \frac{2V_{GS}^2}{25} + V_{GS} = 0$

$\therefore 2 + \frac{9V_{GS}}{5} + \frac{2V_{GS}^2}{25} = 0$

On solving, we get;

$V_{GS} = -1.17$ or $-21.32V$

Since $|V_{GS}| > |V_P|$

$V_{GS} = -1.17V$

$I_{DQ} = \frac{V_{GS}}{-0.2 \times 10^3} = \mathbf{5.85mA}$

Applying KVL to the Source Drain loop,

$V_{DD} - I_S R_S - V_{DS} - I_D R_D = 0$

$\therefore I_D = I_S$

$\therefore V_{DSQ} = 20 - (5.8 \times 10^{-3})(2k + 0.2k) = \mathbf{7.24V}$

SIMULATED RESULTS

Above circuit is simulated in LTspice and the result is as follows:

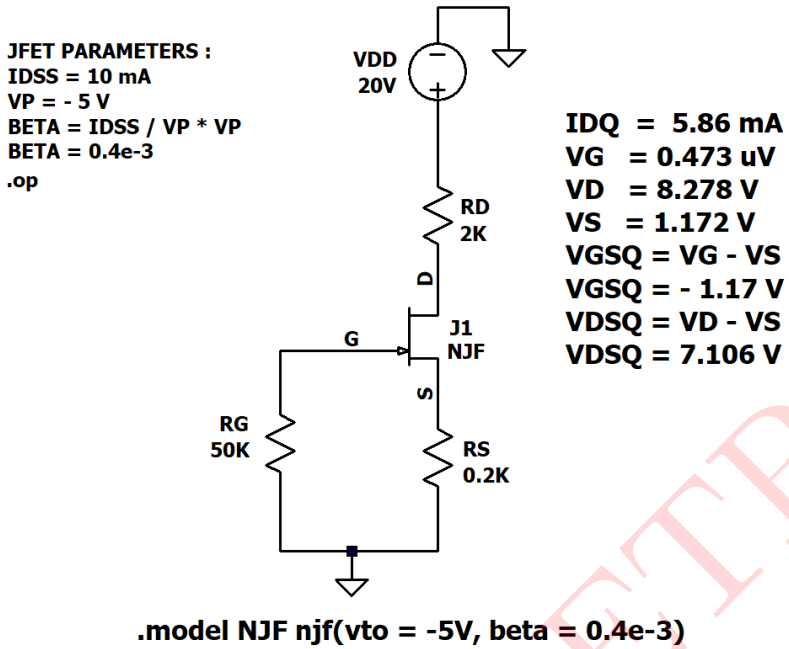

Figure 23: Circuit schematic: Results

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
I_{DQ}	5.85 mA	5.86 mA
V_{GSQ}	$-1.17V$	$-1.17V$
V_{DSQ}	7.24V	7.1 V

Table 8: Numerical 8

Numerical 9: The MOS biasing circuit shown below in figure 1 has $R_D = k\Omega$, $R_{SR} = 500\Omega$, $R_1 = 400k\Omega$, $R_2 = 60k\Omega$, $V_{DD} = 12V$ MOS parameters are $k_n = 0.5mA/V^2$, $V_t = -1.5V$. Determine I_D, V_{GS} and V_{DS}

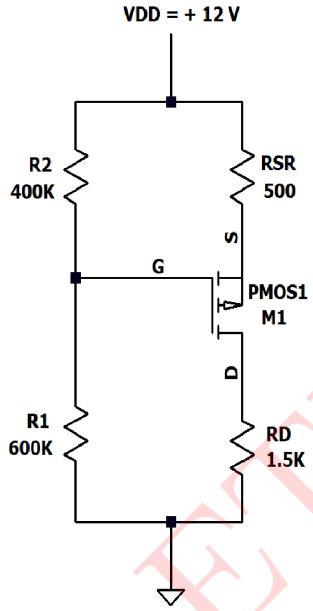

Figure 24: Circuit 9

Solution: The above circuit is a voltage divider biasing configuration employing a Enhancement type NMOS

DC Equivalent circuit:

Refer to Figure 24 for DC equivalent circuit

Thevenin's equivalent circuit:

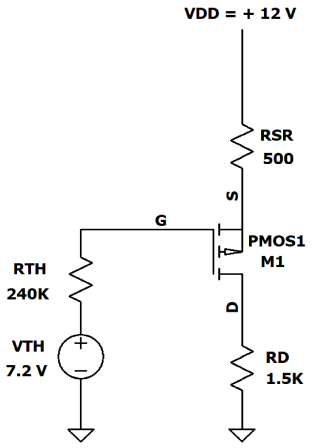

Figure 25: Thevenin's equivalent circuit

Here, $R_{TH} = R_G = R_1 \ || \ R_2 = 600k \ || \ 400k = \mathbf{240k\Omega}$

and $V_G = V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \mathbf{7.2V}$

DC analysis:

Applying KVL to the Gate - Source loop,

$V_{DD} - I_S R_{SR} - V_{GS} - I_G R_G - V_G = 0$

For mosfet, $I_G = 0$ and $I_D \approx I_S$

$12 - I_D R_{SR} - V_{SG} - 7.2 = 0$

$V_{SG} = \frac{4.8 - V_{SG}}{500}$

$V_{SG} = -V_{GS}$

$\therefore I_D = \frac{4.8 + V_{GS}}{500}$ 1

Above for enhancement type PMOS, in saturation region,

$I_D = k_n(V_{GS} - V_t)^2 \quad$ (Where $V_t = -1.5V$)

$I_D = 0.5 \times 10^{-3}(V_{GS} + 1.5)^2$ 2

From 1 and 2, we get,

$\frac{4.8 + V_{GS}}{500} = 0.5 \times 10^{-3}(V_{GS}^2 + 3V_{GS} + 2.25)$

$4.8 + V_{GS} = 0.25(V_{GS}^2 + 3V_{GS} + 2.25)$

$\therefore 0.25V_{GS}^2 + 0.75V_{GS} + 0.55625 - V_{GS} - 4.8 = 0$

$\therefore 0.25V_{GS}^2 - 0.25V_{GS} - 4.2375 = 0$

On solving we get,

$V_{GS} = -3.647V$ and $V_{GS} = 4.64V$

As $|V_{GS}| > |V_t|$

$\therefore V_{GS} = \mathbf{-3.65V}$

Substituting value of V_{GS} in 2 we get,

$I_D = 0.5 \times 10^{-3}(-3.65 + 1.5)^2 = \mathbf{2.3mA}$

Applying KVL to the Source - Drain loop:

$V_{DD} - I_S R_{SR} + V_{DS} - I_D R_D = 0$

For NMOS, $I_D \approx I_S$

$V_{DD} - I_D(R_{SR} + R_D) = -V_D S$

$12 - (2.3 \times 10^{-3})(500 + 1500) = -V_{DS}$

$V_{DS} = \mathbf{-7.4V}$

SIMULATED RESULTS

Above circuit is simulated in LTspice and the result is as follows:

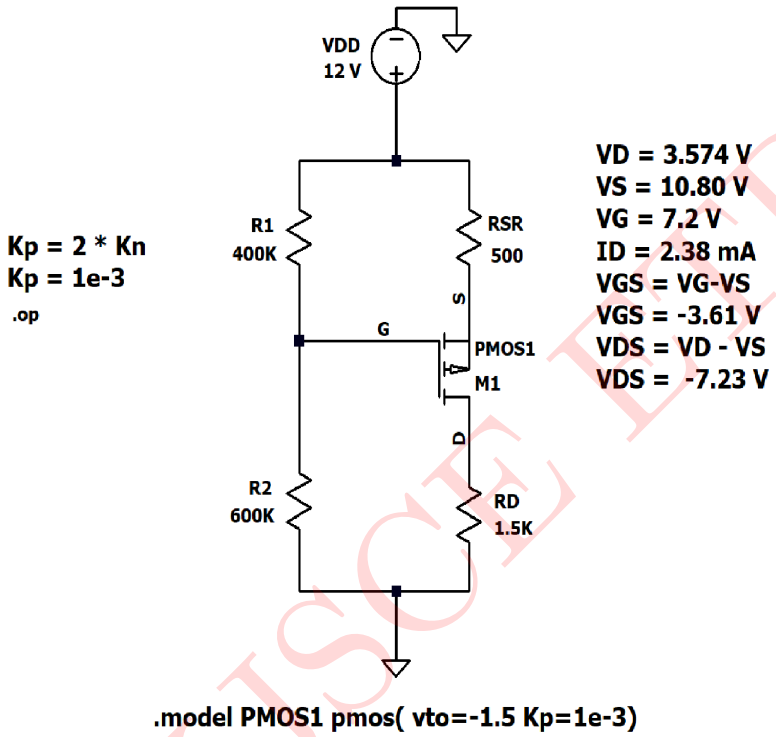

Figure 26: Circuit schematic: Results

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
I_D	2.38 mA	2.3mA
V_{GS}	$-3.61V$	$-3.65V$
V_{DS}	7.23V	7.4 V

Table 9: Numerical 9

Numerical 10: Determine the values of I_B adnd V_E in the given circuit

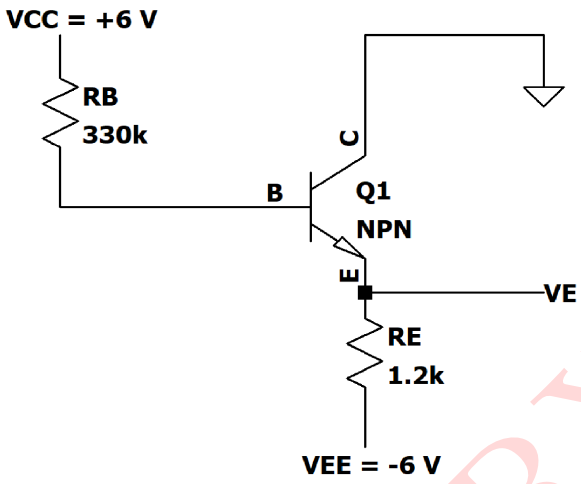

Figure 27: Circuit 10

Solution: Applying KVL to the input loop from V_{CC} to $-V_{EE}$

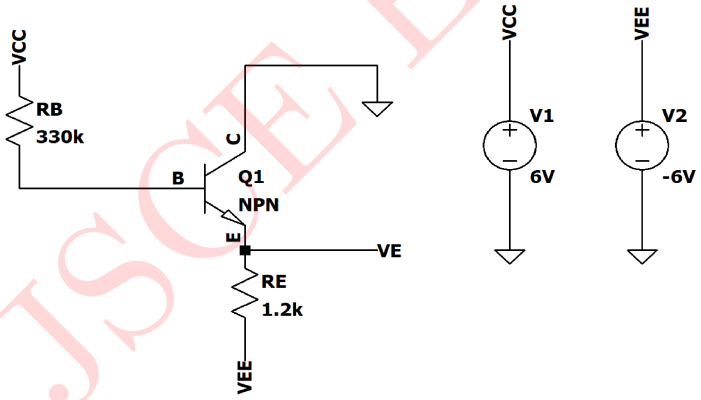

Figure 28: Thevenin's equivalent circuit

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (1+\beta) I_B R_E + V_{EE} = 0$$

$$\therefore I_B = \frac{V_{CC} + V_{EE} - V_{BE}}{R_B + (1+\beta) R_E} = \frac{6 + 6 - 0.7}{330 \times 10^3 + 121 \times 1.2 \times 10^3} = \mathbf{23.72\mu A}$$

We know that $I_E = (1+\beta) I_B = (1+120) 23.72 \times 10^{-6} = \mathbf{2.87mA}$

Applying KVL to the emiter loop,

$$V_E - I_E R_E + V_{EE} = 0$$

$$V_E = I_E R_E - V_{EE} = (2.87 \times 10^{-3})(1.2 \times 10^3) - 6 = \mathbf{-2.547V}$$

SIMULATED RESULTS

Above circuit is simulated in LTspice and the result is as follows:

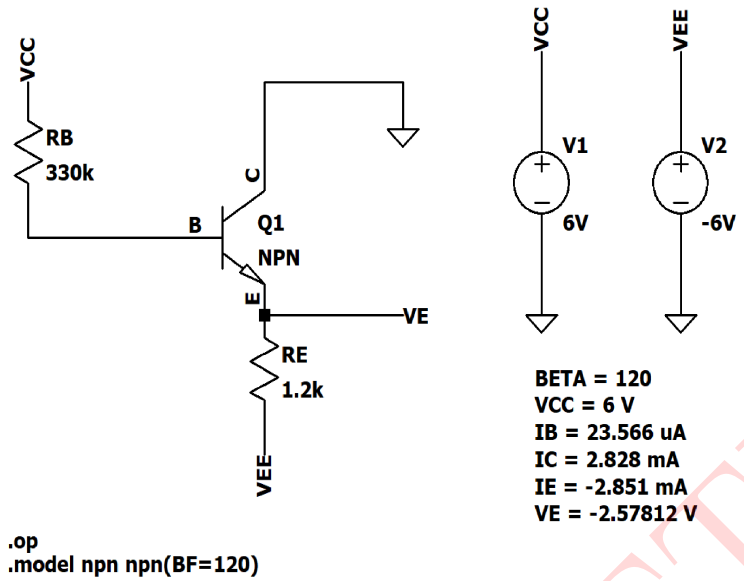

Figure 29: Circuit schematic: Results

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
I_B	$23.72\mu A$	$23.566\mu A$
V_E	$-2.547V$	$-2.57812V$
I_E	2.87 mA	2.851 mA

Table 10: Numerical 10

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