K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Single Stage FET Amplifier

Numerical 1: For the circuit shown in figure 1, Determine I_{DQ}, V_{GSQ}, V_{DS}, A_V, R_i and R_o. Given: $I_{DSS} = 10$ mA, $V_p = -4.5$ V

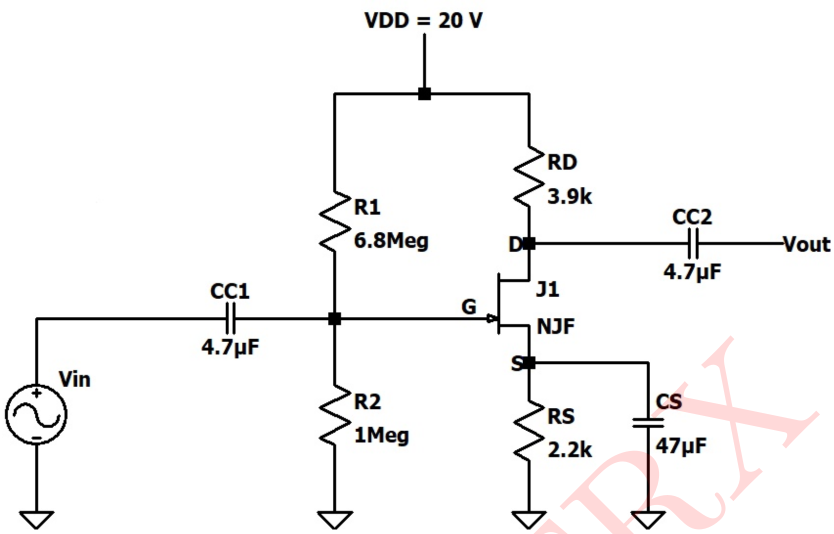

Figure 1: Circuit 1

Solution:

The given circuit 1 is a voltage divider bias configuration employing N-channel JFET.

For DC biasing, the capacitors will act as an open source.

DC Analysis:

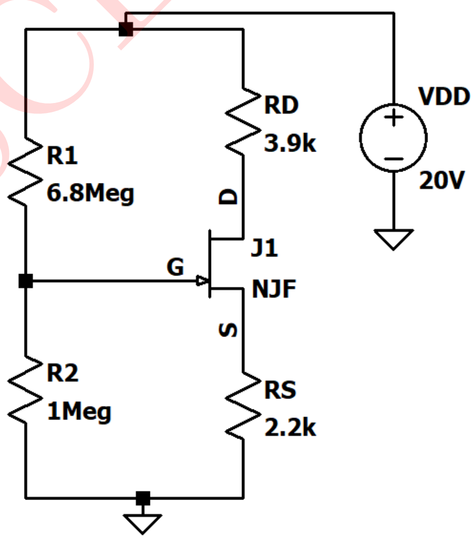

Figure 2: DC Biasing Circuit

$$R_G = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_G = \frac{6.8 \times 10^6 \times 1 \times 10^6}{6.8 \times 10^6 + 1 \times 10^6} = \mathbf{0.87}\ \mathbf{M\Omega}$$

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$$

$$V_G = \frac{1 \times 10^6}{6.8 \times 10^6 + 1 \times 10^6} \times 20 = \mathbf{2.5641\ \ V}$$

Thevenin's Equivalent circuit:

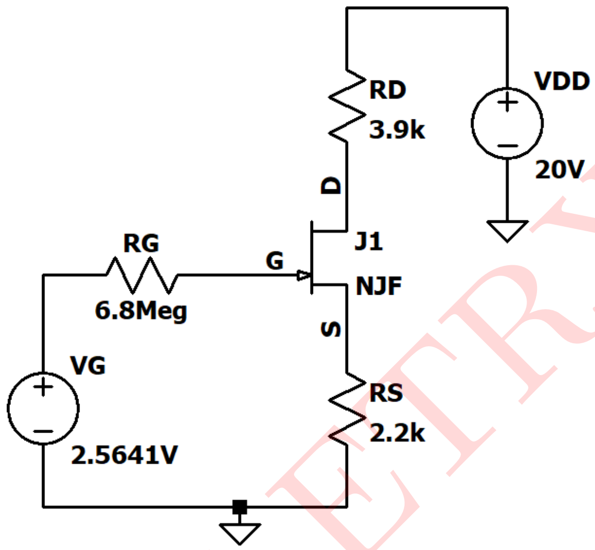

Figure 3: Thevenin's Equivalent circuit

Applying KVL to the gate-source loop,

$$V_G - I_G R_G - V_{GS} - I_D R_S = 0$$

$$I_D R_S = V_G - V_{GS} \qquad \text{...}(\because I_G = 0)$$

$$I_D = \frac{V_G - V_{GS}}{R_S} \qquad \text{...(1)}$$

Current equation is given as,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\frac{V_G - V_{GS}}{R_S} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \text{...(from 1)}$$

$$\frac{2.5641 - V_{GS}}{2.2 \times 10^3} = 10 \times 10^{-3}\left(1 + \frac{V_{GS}}{4.5}\right)^2$$

$$\frac{2.5641 - V_{GS}}{2.2 \times 10^3} = \frac{10 \times 10^{-3}}{20.25}(4.5 + V_{GS})^2$$

$$51.923 - 20.25V_{GS} = 22(20.25 + 9V_{GS} + V_{GS}^2)$$

$$51.923 - 20.25V_{GS} = 445.5 + 198V_{GS} + 22V_{GS}^2$$

$$22V_{GS}^2 + 218.25V_{GS} + 393.577 = 0$$

$$V_{GS} = -2.369 \ \& \ V_{GS} = -7.551$$

let, $V_{GS} = -2.369$

$$I_D = \frac{2.5641 + 2.369}{2.2 \times 10^3} = \mathbf{2.2423\ mA}$$

let, $V_{GS} = -7.551$

$$I_D = \frac{2.5641 + 7.551}{2.2 \times 10^3} = \mathbf{4.597\ mA}$$

Since Q-point should lie in the middle of the transfer characteristic,

$I_{DQ} = \mathbf{2.2423\ mA}$

$V_{GSQ} = -\mathbf{2.369\ V}$

Applying KVL to the drain-source loop,

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$V_{DS} = V_{DD} - I_D R_D - I_D R_S$

$V_{DS} = 20 - 2.24 \times 10^{-3} \times 3.9 \times 0^3 - 2.24 \times 10^{-3} \times 2.2 \times 10^3 = \mathbf{6.336\ V}$

AC Analysis:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = \frac{2 \times 10 \times 10^{-3}}{4.5}\left(1 - \frac{(-2.364)}{(-4.5)}\right)$$

$$g_m = \frac{2 \times 10 \times 10^{-3}}{4.5}\left(1 - \frac{2.364}{4.5}\right)$$

$g_m = 4.44 \times 10^{-3}(0.47) = \mathbf{2.0863}\ mA/V^2$

$r_d = \infty$

Small Signal Equivalent Circuit:

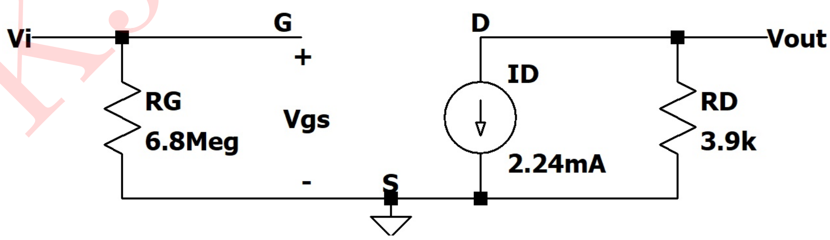

Figure 4: Small Signal Equivalent Circuit

Input Resistance:

$R_i = R_G$

$R_i = \mathbf{0.87\ M\Omega}$

Output resistance:

Let, $V_i = 0$

$V_{GS} = 0$ V

$g_m V_{gs} = 0$ mA

$R_o = R_D$

$R_o = \mathbf{3.9\ k\Omega}$

Voltage Gain:

Output voltage V_o = voltage developed across R_o

$V_o = -g_m V_{gs} R_D$

but, $V_{gs} = V_i$

$V_o = -g_m V_i R_D$

$\dfrac{V_o}{V_i} = -g_m R_D$

$A_V = -g_m R_D$

$A_V = -2.0868 \times 10^{-3} \times 3.9 \times 10^3 = \mathbf{-8.1385}$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

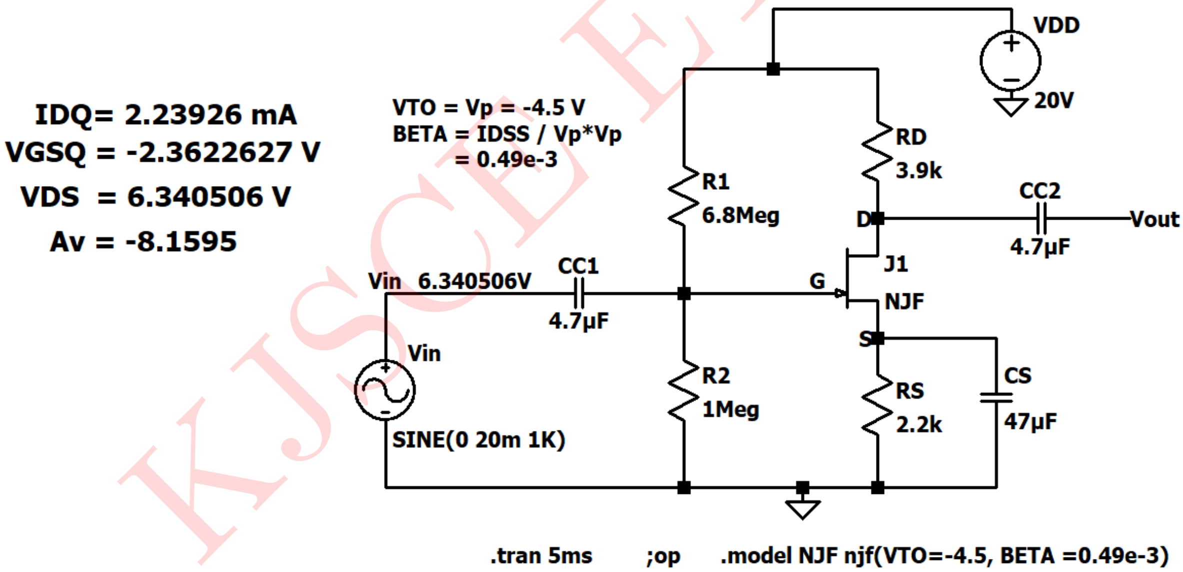

Figure 5: Circuit Schematic 1: Results

The input and output waveforms are shown in figure 6.

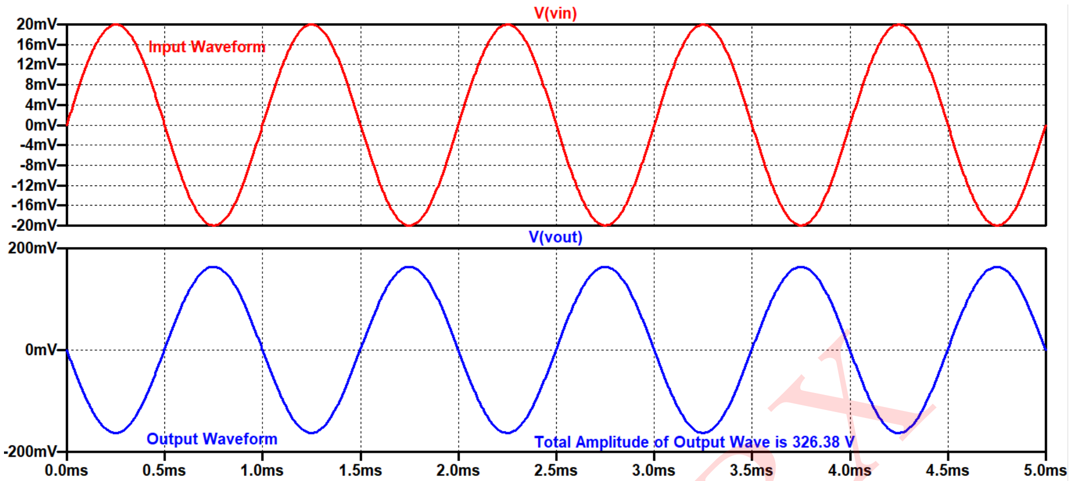

Figure 6: Input & Output waveforms

Comparison of theoretical and simulated values:

Parameters	Theoretical Values	Simulated Values
I_{DQ}	2.24 mA	2.2392 mA
V_{GSQ}	-2.369 V	-2.3622 V
V_{DS}	6.336 V	6.3405 V
A_V	-8.1385	-8.1595

Table 1: Numerical 1

Numerical 2: The parameters of circuit shown in figure 7 are: $R_S = 4$ kΩ, $R_1 = 850$ kΩ, $R_2 = 350$ kΩ and $R_L = 4$ kΩ. The transistor parameters are $V_{TP} = -1.2$ V, $k_p^{'} = 40\ \mu A/V^2$, W/L = 80 and $\lambda = 0.05\ V^{-1}$

a) Determine I_{DQ}, V_{SGQ} and V_{SDQ}.

b) Find the small-signal voltage gain $A_V = V_o/V_i$

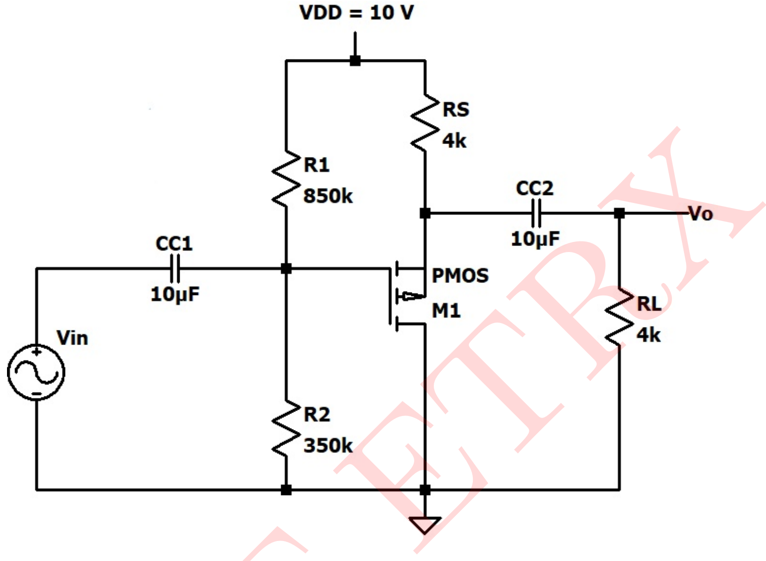

Figure 7: Circuit 2

Solution:

The given circuit 2 is a voltage divider bias configuration employing PMOS.

For DC biasing, the capacitors will act as an open source.

DC Analysis:

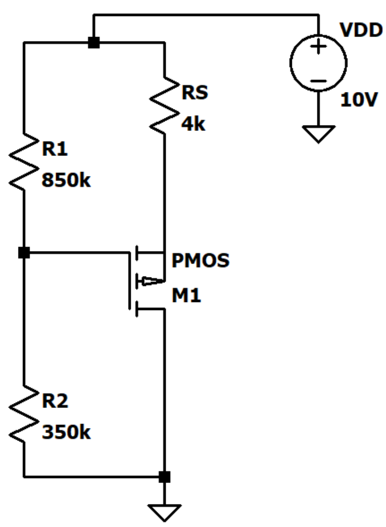

Figure 8: DC Biasing Circuit

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$$V_G = \frac{10 \times 350 \times 10^3}{850 \times 10^3 + 350 \times 10^3} = \mathbf{2.9167\ V}$$

$$R_G = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_G = \frac{850 \times 10^3 \times 350 \times 10^3}{850 \times 10^3 + 350 \times 10^3} = \mathbf{247.9167\ k\Omega}$$

Thevenin's Equivalent circuit:

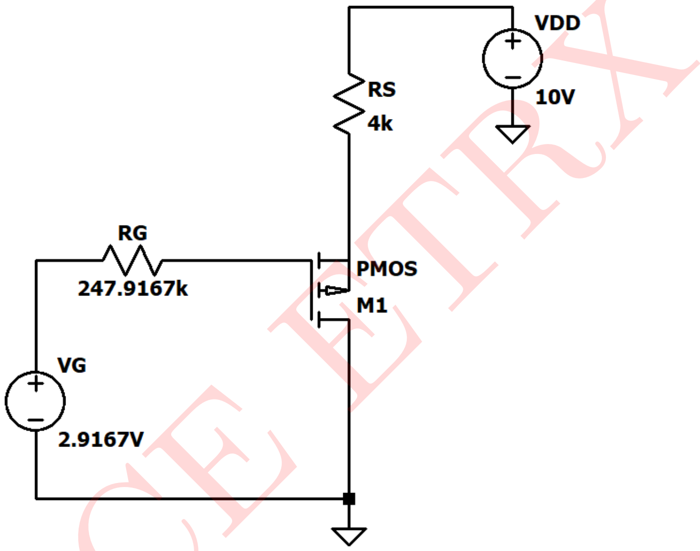

Figure 9: Thevenin's Equivalent circuit

$$k_p = \frac{k_p'}{2} \times \frac{W}{L}$$

$$k_p = \frac{40 \times 10^{-6}}{2} \times 80 = \mathbf{1.6\ mA}/V^2 \qquad ...(1)$$

Applying KVL to the source-gate loop,

$$V_{DD} - I_D R_S - V_{SG} - I_G R_G - V_G = 0$$

$$V_{SG} = V_{DD} - I_D R_S - V_G \qquad ...(\because I_G = 0)$$

$$V_{SG} = 10 - I_D \times 4 \times 10^3 - 2.9167$$

$$V_{SG} = 7.0933 - I_D \times 4 \times 10^3 \qquad ...(2)$$

Applying KVL to the source-drain loop,

$$V_{DD} - I_D R_S - V_{SD} = 0$$

$$V_{SD} = V_{DD} - I_D R_S$$

$$V_{SD} = 10 - I_D \times 4 \times 10^3 \qquad ...(3)$$

From current equation,

$I_D = k_p[(V_{SG} + V_{TP})^2(1 + \lambda V_{SD})]$

$I_D = 1.6 \times 10^{-3}[(7.0833 - I_D \times 4 \times 10^3 - 1.2)^2(1 + 10 - I_D \times 4 \times 10^3)]$ ...(from 1,2 and 3)

$I_D = 1.6 \times 10^{-3}[(5.8833 - I_D \times 4 \times 10^3)^2(11 - I_D \times 4 \times 10^3)]$

$I_D = 1.6 \times 10^{-3}[(34.6132 - 47.0664 \times 10^3 I_D + 16 \times 10^6 I_D^2)(11 - I_D \times 4 \times 10^3)]$

$I_D = 1.6 \times 10^{-3}[380.7452 - 517.7304 \times 10^3 I_D + 176 \times 10^6 I_D^2 - 138.4528 \times 10^3 I_D +$
$188.2656 \times 10^6 I_D^2 - 64 \times 10^9 I_D^3]$

$I_D = 1.6 \times 10^{-3}[380.7452 - 656.1832 \times 10^3 I_D + 364.2656 \times 10^6 I_D^2 - 64 \times 10^9 I_D^3]$

$I_D = 609.1923 \times 10^{-3} - 1049.8931 I_D + 582.8249 \times 10^3 I_D^2 - 102.4 \times 10^6 I_D^3$

$102.4 \times 10^6 I_D^3 - 582.8249 \times 10^3 I_D^2 + 1050.5931 I_D - 609.1923 \times 10^{-3} = 0$

$I_D =$ **2.73 mA** or $I_D =$ **1.58 mA** or $I_D =$ **1.37 mA**

Let, $I_D = 2.73$ mA

$V_{SG} = 7.0833 - 2.73 \times 10^{-3} \times 4 \times 10^3 = \mathbf{-3.8367\ V}$

Let, $I_D = 1.58$ mA

$V_{SG} = 7.0833 - 1.58 \times 10^{-3} \times 4 \times 10^3 = \mathbf{0.7633\ V}$

Let, $I_D = 1.37$ mA

$V_{SG} = 7.0833 - 1.37 \times 10^{-3} \times 4 \times 10^3 = \mathbf{1.6033\ V}$

We know, $V_{GS} = -V_{SG}$

V_{GS} cannot be positive for p-mosfet an V_{GS} should be less than V_{TP}

$V_{SGQ} = \mathbf{1.6033\ V}$

$I_{DQ} = \mathbf{1.37\ mA}$

$V_{SDQ} = 10 - 1.37 \times 10^{-3} \times 4 \times 10^3 = 4.52$ V

AC Analysis:

$$g_m = \frac{\partial I_D}{\partial V_{SG}}$$

$$g_m = \frac{\partial}{\partial V_{SG}}[k_p(V_{SG} + V_{TP})^2(1 + \lambda V_{SD})]$$

$$g_m = k_p \frac{\partial}{\partial V_{SG}}[(V_{SG} + V_{TP})^2(1 + \lambda V_{SD})]$$

$g_m = k_p[(1 + \lambda V_{SD})2(V_{SG} + V_{TP})]$

$g_m = 1.6 \times 10^{-3}[2(1 + 0.226)(1.6033 - 1.2)]$

$g_m = 1.6 \times 10^{-3}[0.98] = \mathbf{1.582\ mA/V}$

Small Signal Equivalent Circuit,

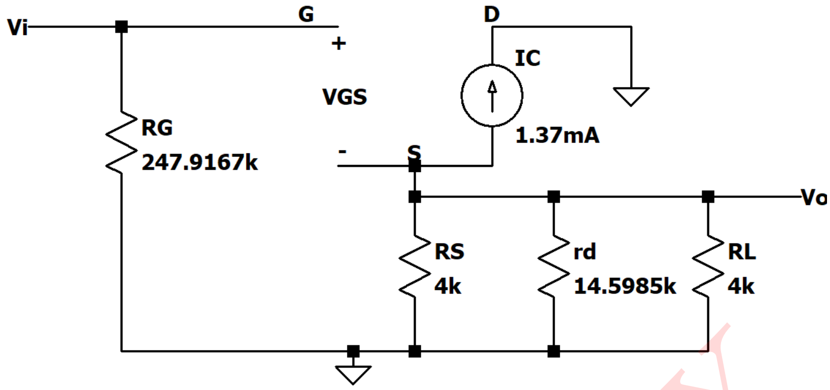

Figure 10: Small Signal Equivalent Circuit

Output voltage V_o = voltage developed across $(r_d \ || \ R_S \ || \ R_L)$

$V_o = g_m V_{gs}(r_d \ || \ R_S \ || \ R_L)$ ...(4)

$V_i = V_{gs} + V_o$

$V_{gs} = V_i - V_o$

Substituting this in equation 4,

$V_o = g_m(V_i - V_o)(r_d \ || \ R_S \ || \ R_L)$

$V_o = g_m V_i(r_d \ || \ R_S \ || \ R_L) - g_m V_o(r_d \ || \ R_S \ || \ R_L)$

$V_o + g_m V_o(r_d \ || \ R_S \ || \ R_L) = g_m V_i(r_d \ || \ R_S \ || \ R_L)$

$V_o(1 + g_m(r_d \ || \ R_S \ || \ R_L)) = g_m V_i(r_d \ || \ R_S \ || \ R_L)$

$$\frac{V_o}{V_i} = A_V = \frac{g_m(r_d \ || \ R_S \ || \ R_L)}{1 + g_m(r_d \ || \ R_S \ || \ R_L)}$$

$$A_V = \frac{1.5822 \times 10^{-3}(14.5985 \times 10^3 \ || \ 4 \times 10^3 \ || \ 4 \times 10^3)}{1 + 1.5822 \times 10^{-3}(14.5985 \times 10^3 \ || \ 4 \times 10^3 \ || \ 4 \times 10^3)}$$

$$A_V = \frac{1.5822 \times 10^{-3} \times 1.759 \times 10^3}{1 + 1.5822 \times 10^{-3} \times 1.759 \times 10^3} = \mathbf{0.7356}$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

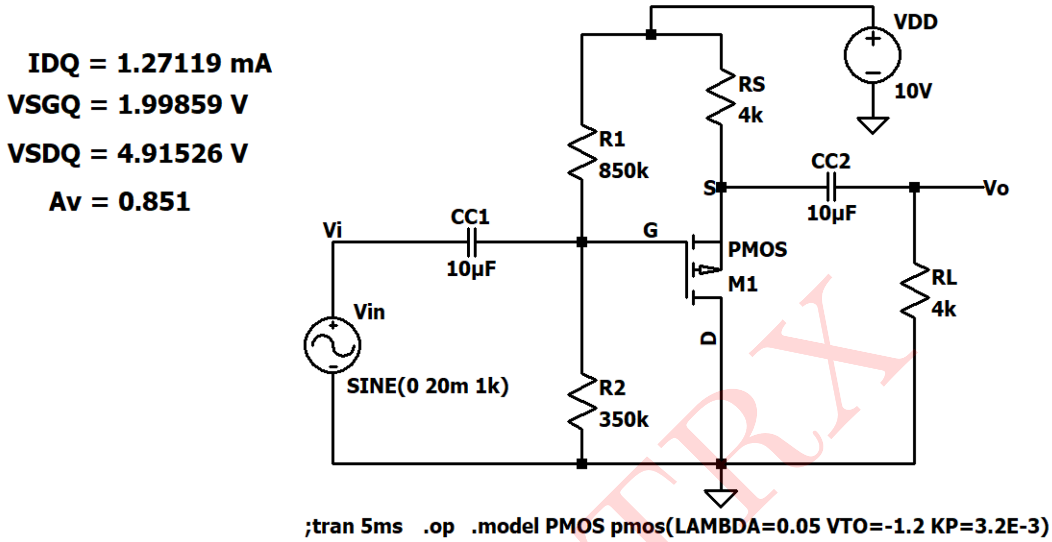

Figure 11: Circuit Schematic 2: Results

The input and output waveforms are shown in figure 12.

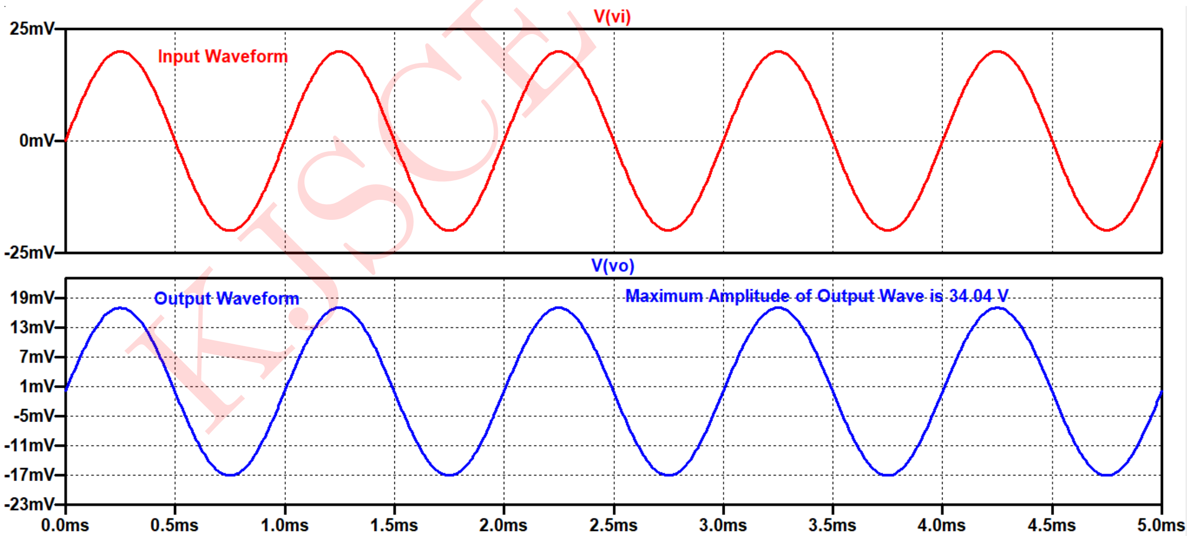

Figure 12: Input & Output waveforms

Comparison of theoretical and simulated values:

Parameters	Theoretical Values	Simulated Values
I_{DQ}	1.37 mA	1.2711 mA
V_{SGQ}	1.6033 V	1.9985 V
V_{SDQ}	4.52 V	4.9152 V
A_V	0.7356	0.851

Table 2: Numerical 2

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