K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Single Stage FET Amplifier

Numerical 1:

For the circuit shown in figure 1, determine

a. I_{DQ}, V_{GSQ} & V_{DSQ}

b. A_V, R_i & R_o

JFET having $I_{DSS} = 8mA$ & $V_p = -4V$

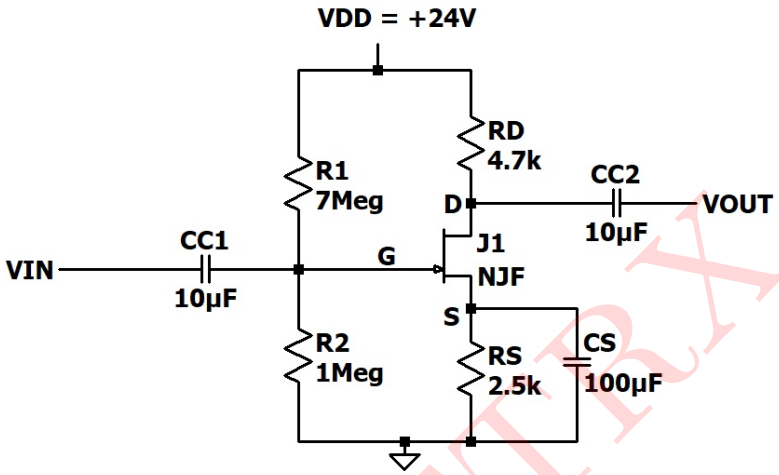

Figure 1: Circuit 1

Solution: The above circuit 1 is a common source JFET amplifier employing a n-channel JFET in voltage divider bias configuration

DC Analysis:

All capacitors acts as open circuited, since f = 0

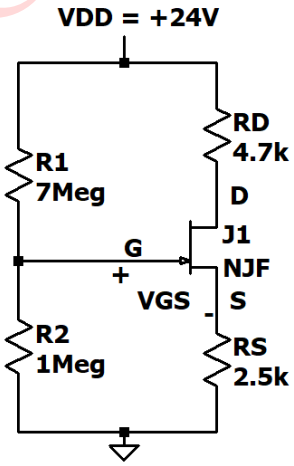

Figure 2: DC Equivalent Circuit

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$$
$$= \frac{1M\Omega}{1M\Omega + 7M\Omega} \times 24V = \mathbf{3V}$$

$$V_S = I_D R_S$$
$$V_{GS} = 3 - I_D R_S$$
$$V_{GS} = 3 - I_D(2.5k\Omega) \quad \text{.....(1)}$$

Assuming JFET is working in saturation region,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$
$$= (8mA)\left(1 + \frac{V_{GS}}{4}\right)^2 \quad \text{.....(2)}$$

Substituting equation (2) in equation (1), we get

$$V_{GS} = 3 - (20)\left(1 + \frac{V_{GS}}{2} + \frac{V_{GS}^2}{16}\right)$$
$$= 3 - 20 - 10V_{GS} - 1.25V_{GS}^2$$
$$1.25V_{GS}^2 + 11V_{GS} + 17 = 0$$
$$V_{GS} = -2V \quad \text{or} \quad V_{GS} = -6.8V$$

Since $V_{GS} > V_p$ for saturation,

$$\therefore V_{GSQ} = \mathbf{-2V}$$

Applying KVL to input Gate Source loop,

$$V_{GS} = 3 - I_D R_S$$
$$I_D = \frac{3 - V_{GS}}{R_S}$$
$$I_D = \frac{3 - (-2)}{2.5k\Omega}$$
$$I_{DQ} = \mathbf{2mA}$$

Applying KVL to outer Drain Source loop,

$$V_{DD} - I_D R_S - V_{DS} - I_D R_S = 0$$
$$V_{DS} = 24 - I_D(R_D + R_S)$$
$$V_{DS} = 24 - (2mA)(4.7k\Omega + 2.5k\Omega)$$
$$V_{DSQ} = \mathbf{9.6V}$$

Small Signal Analysis:

$$g_m = \frac{2I_{DSS}}{|V_p|}\left(1 - \frac{V_{GS}}{V_p}\right)$$
$$= \frac{2 \times 8mA}{|4V|}\left(1 - \frac{(-2V)}{-4V}\right)$$
$$= \mathbf{2mA/V}$$

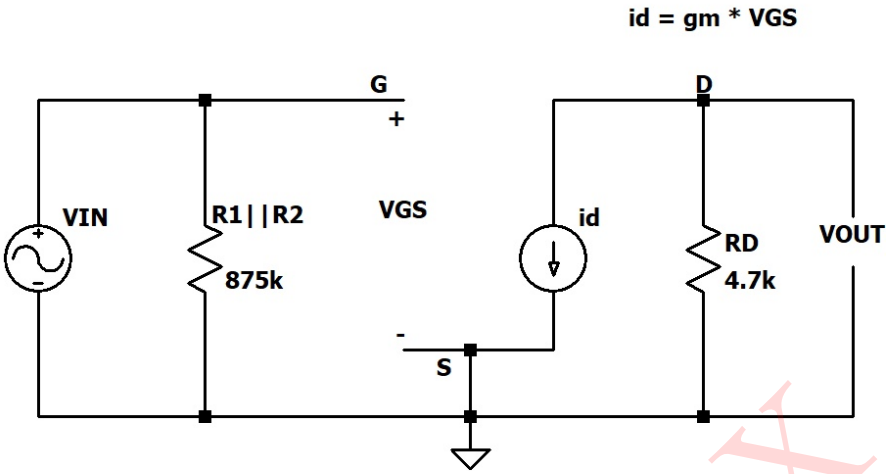

Figure 3: Small Signal Equivalent Circuit

Small Signal Voltage Gain (A_V)**:**

$A_V = -g_m R_D$

$= (-2mA/V)(4.7k\Omega)$

$= \mathbf{-9.4}$

Negative sign of A_V indicates that the output wavform is 180° out of phase with input waveform

Input and Ouput Impedance:

Input Impedance (R_i) = $R_1 \parallel R_2$

$R_i = 1M\Omega \parallel 7M\Omega = \mathbf{875k\Omega}$

Ouput Impedance (R_o) = R_D

$R_o = \mathbf{2k\Omega}$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

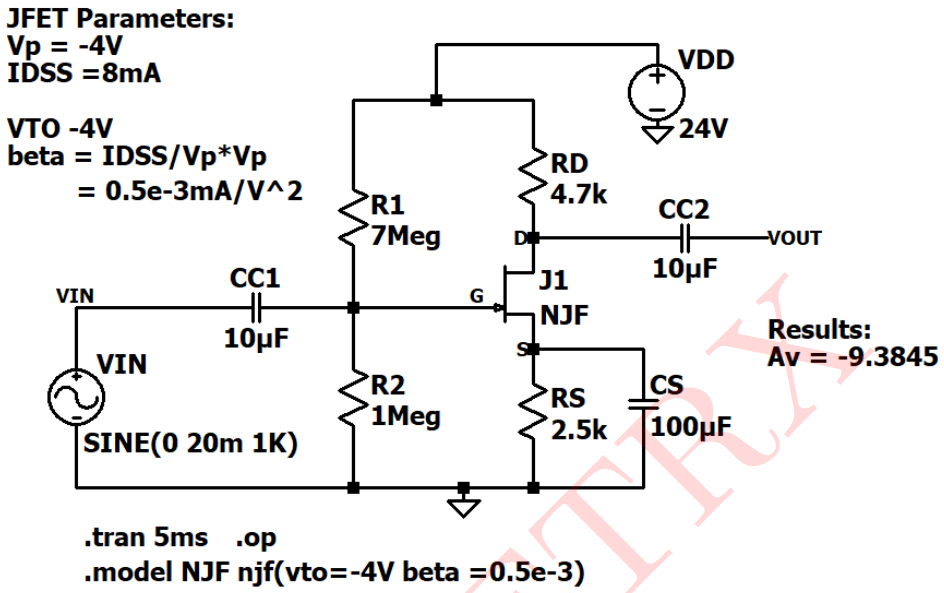

Figure 4: Circuit Schematic

The input and output waveform are shown in figure 5

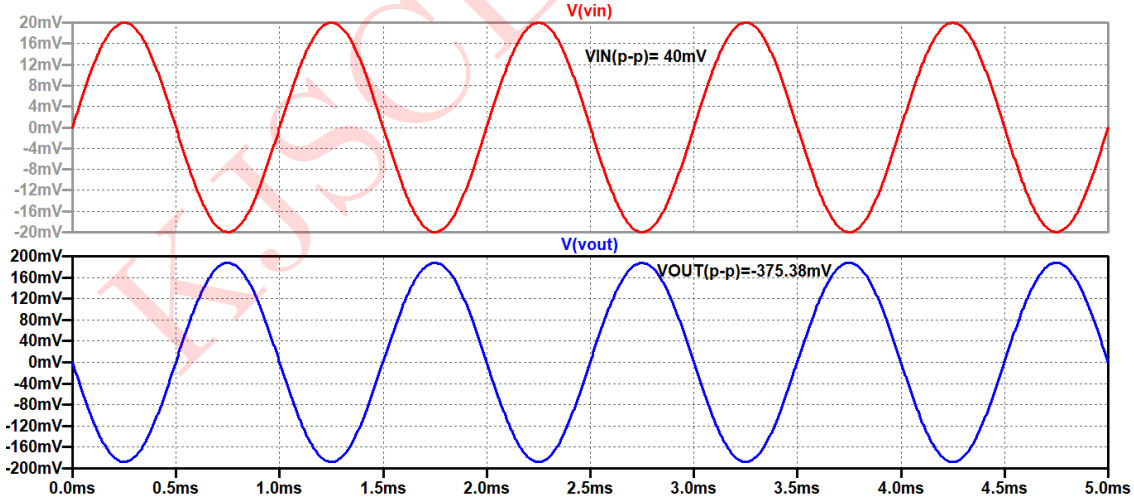

Figure 5: $V_{IN}(t)$ & $V_{OUT}(t)$

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
V_{GSQ}	$-2V$	$-2V$
V_{DSQ}	$9.6V$	$9.6V$
I_{DQ}	$2mA$	$2mA$
A_V	-9.4	-9.3845

Table 1: Numerical 1

Numerical 2:

Determine Z_i, Z_o & A_V for the amplifier given in figure 6. Given $k_n = 0.3mA/V^2$

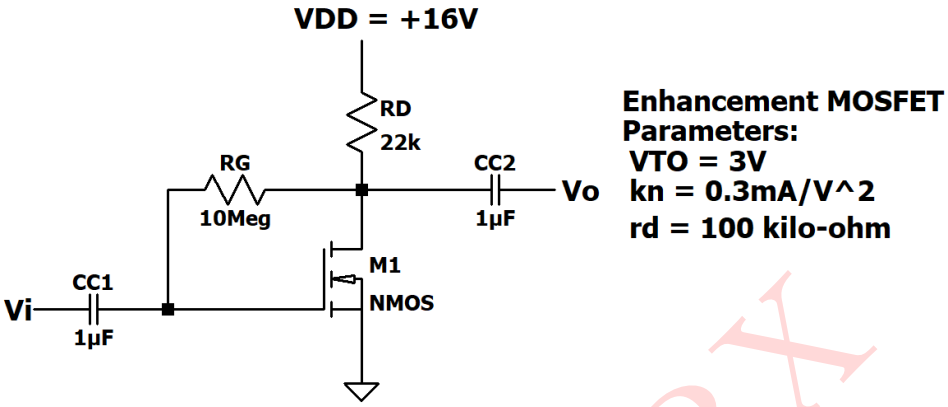

Figure 6: Circuit 2

Solution: The above circuit 2 is a common source enhancement type n-channel MOSFET amplifier in drain feedback configuration

DC Analysis:

We remove all the capacitors as frequency is 0 and thus they are open circuited.

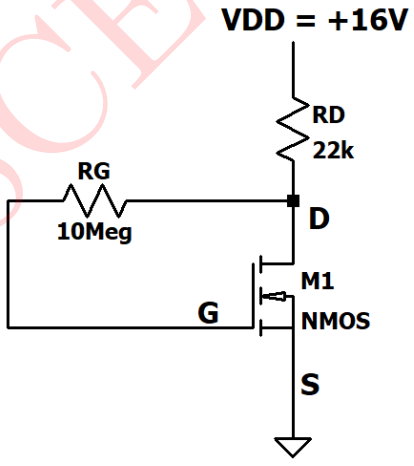

Figure 7: DC Equivalent Circuit

Since, $I_G = 0$

$\therefore V_{GS} \approx V_{DS}$

Applying KVL to Drain Source loop,

$V_{DS} = V_{DD} - I_D R_D$

$V_{GS} = 16 - I_D(22k\Omega)$ [Since, $V_{GS} \approx V_{DS}$] .....(1)

$I_D = k_n(V_{GS} - V_{TN})^2$

$= (0.3mA/V^2)(V_{GS} - 3V)^2$ .....(2)

Substituting equation (2) in equation (1),

$V_{GS} = 16 - 6.6(V_{GS}^2 - 6V_{GS} + 9)$

$= 16 - 6.6V_{GS}^2 + 39.6V_{GS} - 59.4$

$6.6V_{GS}^2 - 38.6V_{GS} + 43.4 = 0$

$\therefore V_{GS} = 4.3292V \quad \text{or} \quad V_{GS} = 1.5187V$

$\because V_{GS} > V_{TN}$

Thus, $V_{GSQ} = \mathbf{4.3297V}$

From equation (1),

$$I_{DQ} = \frac{16 - V_{GSQ}}{22k\Omega}$$

$$= \frac{16 - 4.3297}{22k\Omega}$$

$$= \mathbf{0.53046mA}$$

Given that $r_d = 100k\Omega$

Also, $r_d = \frac{1}{\lambda I_{DQ}} \implies \lambda = \mathbf{0.01885V^{-1}}$

Small Signal Analysis:

$g_m = 2k_n(V_{GSQ} - V_{TN})$

$= 2 \times (0.3mA/V^2)(4.3297 - 3)$

$= \mathbf{0.7978mA/V}$

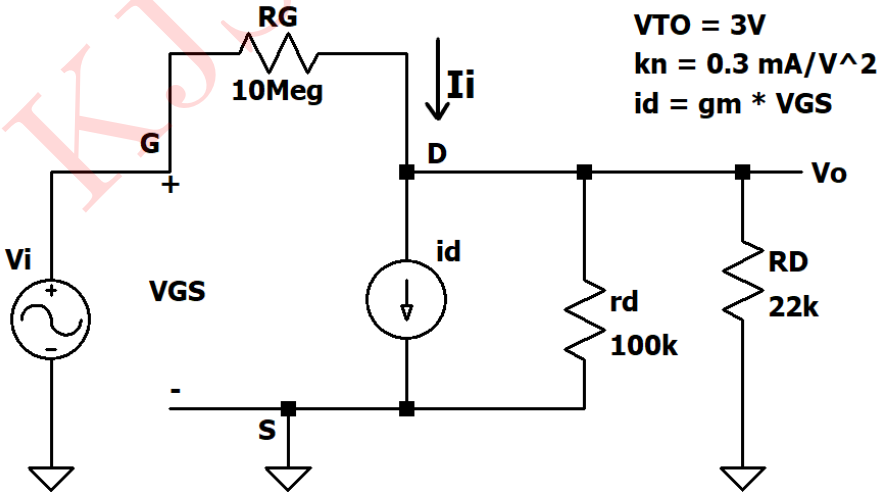

Figure 8: Small Signal Equivalent Circuit

From the figure 3 we can observe,

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \parallel R_D}$$

$$= g_m V_i + \frac{V_o}{r_d \parallel R_D} \qquad [\text{Since, } V_{GS} = V_i]$$

$$I_i - g_m V_i = \frac{V_o}{r_d \parallel R_D}$$

$$V_o = (r_d \parallel R_D)(I_i - g_m V_i)$$

$$I_i = \frac{V_i - V_o}{R_G} = \frac{V_i - (r_d \parallel R_D)(I_i - g_m V_i)}{R_G}$$

$$I_i R_G = V_i - (r_d \parallel R_D) I_i + (r_d \parallel R_D)\, g_m V_i$$

$$V_i[1 + g_m(r_d \parallel R_D)] = I_i[R_G + r_d \parallel R_D]$$

$$\frac{V_i}{I_i} = \frac{R_G + (r_d \parallel R_D)}{1 + g_m(r_d \parallel R_D)}$$

Input and Ouput Impedance:

$$\text{Input Impedance } (Z_i) = \frac{V_i}{I_i}$$

$$\begin{aligned}
\therefore Z_i &= \frac{R_G + (r_d \parallel R_D)}{1 + g_m(r_d \parallel R_D)} \\
&= \frac{10M\Omega + (100k\Omega \parallel 22k\Omega)}{1 + (0.7978mA/V)(100k\Omega \parallel 22k\Omega)} \\
&= \frac{10M\Omega}{15.38655} \\
&= \mathbf{649.918k\Omega}
\end{aligned}$$

For Ouput Impedance (Z_o), we substitute $V_i = 0V$, $V_{GS} = 0$ & $g_m V_{GS} = 0$, with a short circuit from gate to ground

$$\begin{aligned}
Z_o &= R_G \parallel r_d \parallel R_D \\
&= 10M\Omega \parallel 100k\Omega \parallel 22k\Omega \\
&= 99.009k\Omega \parallel 22k\Omega \\
&= \mathbf{18k\Omega}
\end{aligned}$$

Small Signal Voltage Gain ($\mathbf{A_V}$):

$$A_V = \frac{V_o}{V_i}$$

From the small signal equivalent circuit,

Applying KCL at D,

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \parallel R_D}$$

$$I_i = \frac{V_i - V_o}{R_G} \qquad [\text{Since, } V_i = V_{gs}]$$

$$\frac{V_i - V_o}{R_G} = g_m V_i + \frac{V_o}{r_d \parallel R_D}$$

$$V_i \left[\frac{1}{R_G} - g_m\right] = V_o \left[\frac{1}{R_G} + \frac{1}{r_d \parallel R_D}\right]$$

$$\because \frac{1}{R_G} \approx \text{very small}$$

$$\left[\frac{1}{R_G} - g_m\right] \approx -g_m$$

$$\therefore V_i(-g_m) = V_o\left[\frac{1}{R_G} + \frac{1}{r_d \parallel R_D}\right]$$

$$\frac{V_o}{V_i} = \frac{-g_m}{\dfrac{1}{R_G \parallel r_d \parallel R_D}}$$

$$\begin{aligned}\therefore A_V = \frac{V_o}{V_i} &= -g_m(R_G \parallel r_d \parallel R_D) \\ &= -(0.7978mA/V)(10M\Omega \parallel 100k\Omega \parallel 22k\Omega) \\ &= -(0.7978mA/V)(99.009k\Omega \parallel 22k\Omega) \\ &= -(0.7978mA/V)(18k\Omega) \\ &= \mathbf{-14.3604}\end{aligned}$$

Negative sign of A_V indicates that the output wavform is 180° out of phase with input waveform

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

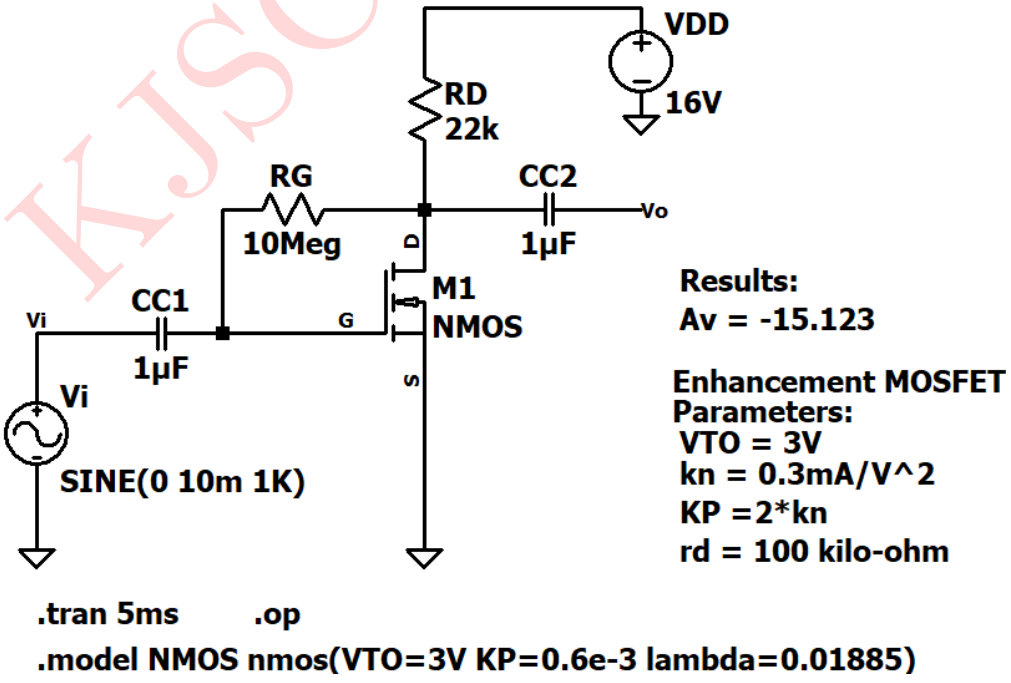

Figure 9: Circuit Schematic

The input and output waveform are shown in figure 10

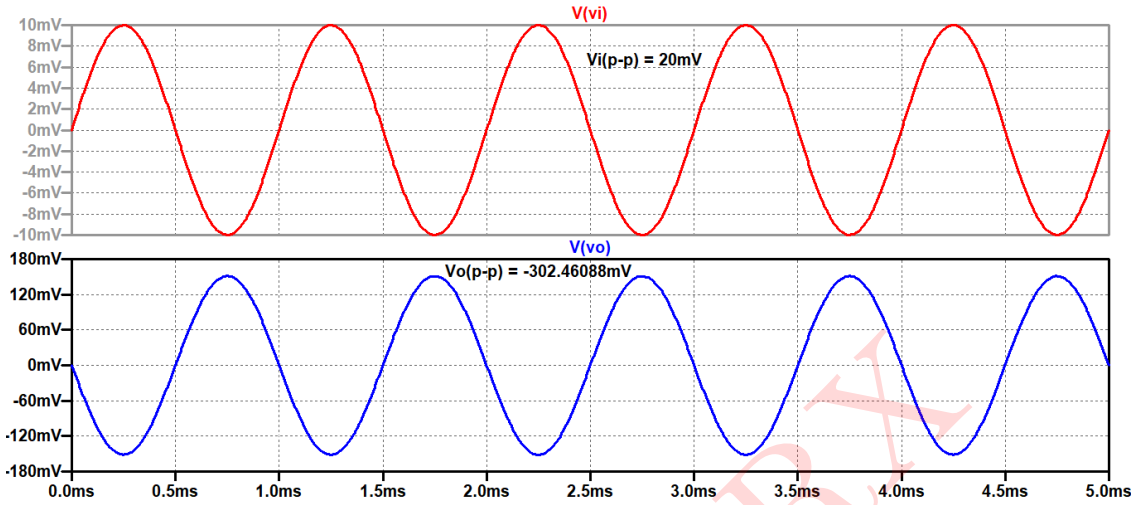

Figure 10: $V_{IN}(t)$ & $V_{OUT}(t)$

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
I_{DQ}	$0.53046mA$	$0.532648mA$
V_{GSQ}	$4.3297V$	$4.28175V$
A_V	-14.3604	-15.123

Table 2: Numerical 2

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