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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Cascode Amplifier

12^{th} **July, 2020** **Numericals**

Numerical 1: A two stage circuit is shown in figure 1. Its BJT parameters are $\beta_1 = \beta_2 = 200$ and $V_{BE1} = V_{BE2} = 0.7$

a. Calculate DC parameters i.e. V_{B1}, V_{B2}, V_{E1}, V_{E2} ,V_{C1}, V_{C2}

b. Calculate Input impedance of the circuit.

c. Calculate output impedance of the circuit.

d. Calculate voltage gain of the circuit.

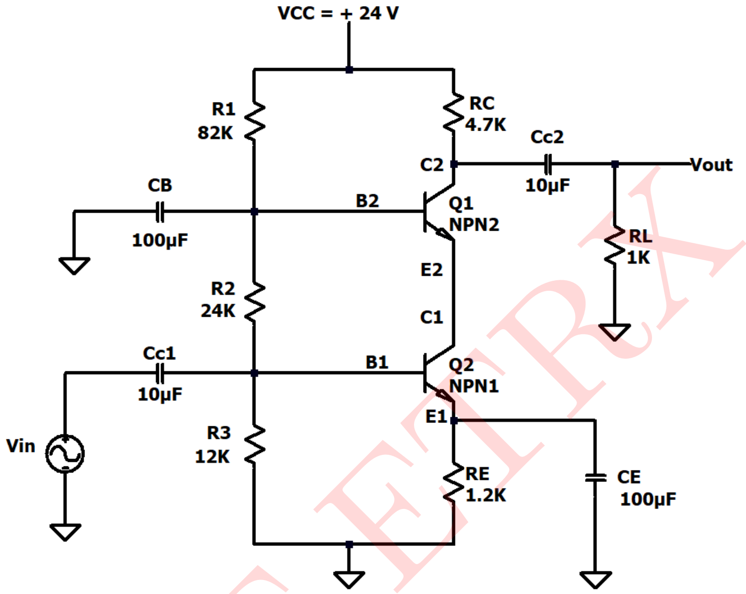

Figure 1: Circuit 1

Solution:

DC ANALYSIS:

$f = 0$, thus $X_C = \infty$, So we replace each capacitor with short circuit,

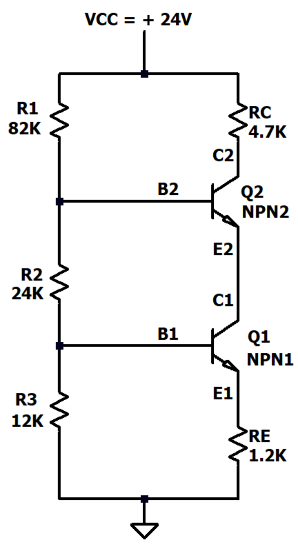

Figure 2: DC Equivalent Circuit

Assuming, I_{B1}, I_{B2} are very small

so, $I_{C1} = I_{C2} = I_{E1} = I_{E2}$

Now, $V_{B1} = \dfrac{R_3}{R_1 + R_2 + R_3} \times V_{CC} = \dfrac{12k}{82k + 24k + 12k} \times 24 = \mathbf{2.44V}$

And, $V_{B2} = \dfrac{R_2 + R_3}{R_2 + R_3 + R_1} \times V_{CC} = \dfrac{24k + 12k}{24k + 12k + 82k} \times 24 = \mathbf{7.322V}$

$V_{BE1} = V_{B1} - V_{E1}$

$V_{E1} = V_{B1} - V_{BE1} = 2.44 - 0.7 = \mathbf{1.74V}$

$V_{E1} = I_{E1}R_E$

$\therefore I_{E1} = \dfrac{1.74}{1.2 \times 10^3} = \mathbf{1.45mA}$

$I_{C1} = I_{C2} = I_{E1} = I_{E2} = \mathbf{1.45mA}$

$V_{C2} = V_{CC} - I_C R_C = 24 - (1.45 \times 10^{-3})(4.7 \times 10^3) = \mathbf{17.185V}$

$V_{E2} = V_{B2} - V_{BE2} = 7.322 - 0.7 = \mathbf{6.622V}$

$V_{E2} = V_{C1} = \mathbf{6.622V}$

$V_{CE1} = V_{C1} - V_{E1} = 6.622 - 1.74 = \mathbf{4.882V}$

$V_{CE2} = V_{C2} - V_{E2} = 17.185 - 6.622 = \mathbf{10.563V}$

Small Signal Parameters:

Since $I_{CQ1} = I_{CQ2}$

$r_\pi = r_{\pi 1} = r_{\pi 2}$

$r_\pi = \dfrac{\beta V_T}{I_{CQ}} = \dfrac{200 \times 26 \times 10^{-3}}{1.45 \times 10^{-3}} = \mathbf{3.586k\Omega}$

$g_m = g_{m1} = g_{m2}$

$g_m = \dfrac{I_{CQ}}{V_T} = \dfrac{1.45 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{55.76mA/V}$

Mid frequency AC equivalent circuit:

All the capacitors are replaced by short circuits and DC sources are replaces by open circuit.

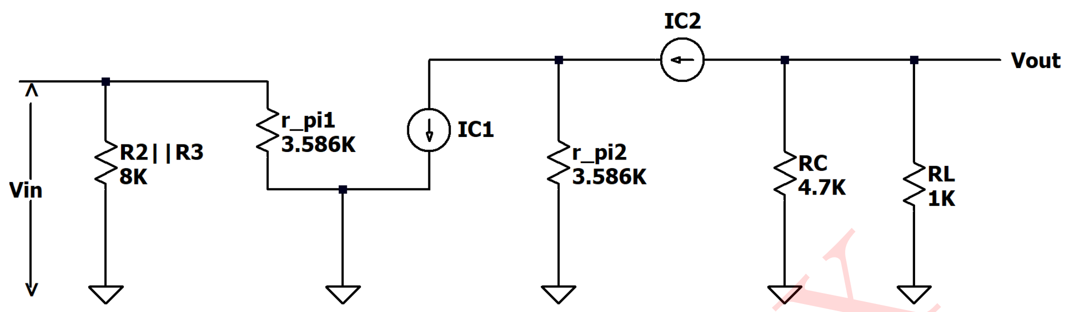

Figure 3: AC mid frequency Equivalent Circuit

Input impedance:

$Z_i = R_1 \ || \ R_3 \ || \ r_{\pi 1} = 24k \ || \ 12k \ || \ 3.589k = \mathbf{2.4760k\Omega}$

Output impedance:

$Z_o = R_C \ || \ R_L = 4.7k \ || \ 1k = \mathbf{824.56\Omega}$

Finding out A_{VT}:

$A_{VT} = A_{V1} \times A_{V2}$

Where, A_{V1} is the gain of CE stage and A_{V2} is the gain of CB stage

Now, $A_{V1} = \frac{-g_m r_\pi}{1+\beta} = \frac{-55.76 \times 10^{-3} \times 3.586 \times 10^{3}}{1+200} = \mathbf{-0.994}$

Also, $A_{V2} = g_m(R_C \ || \ R_L) = 55.76 \times 10^{-3}(1k \ || \ 4.7k) = \mathbf{45.977}$

$A_{VT} = A_{V1} \times A_{V2} = -0.994 \times 45.977 = \mathbf{-45.7}$

SIMULATED RESULTS:
Above circuit is simulated in LTspice and the result is as follows:

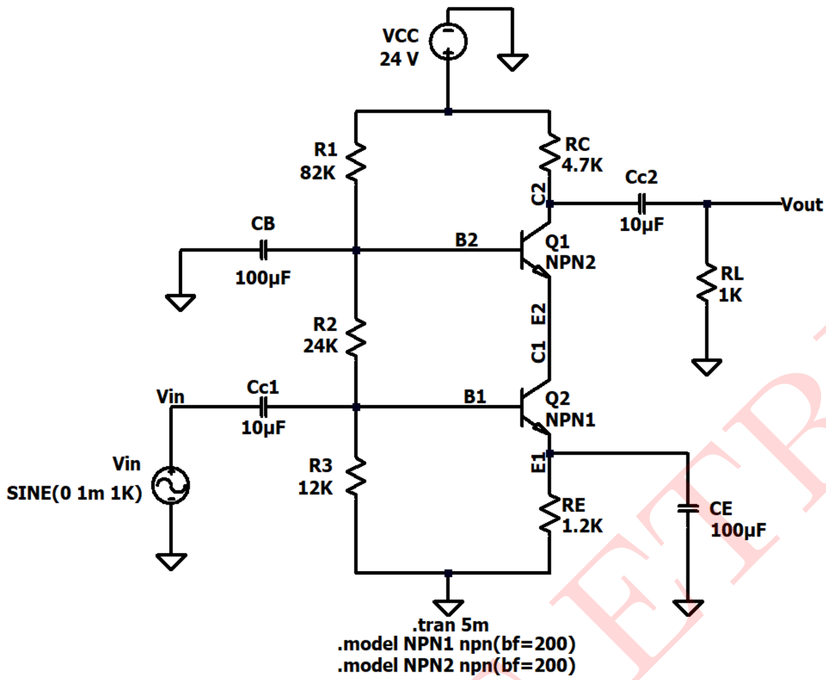

Figure 4: Circuit Schematic

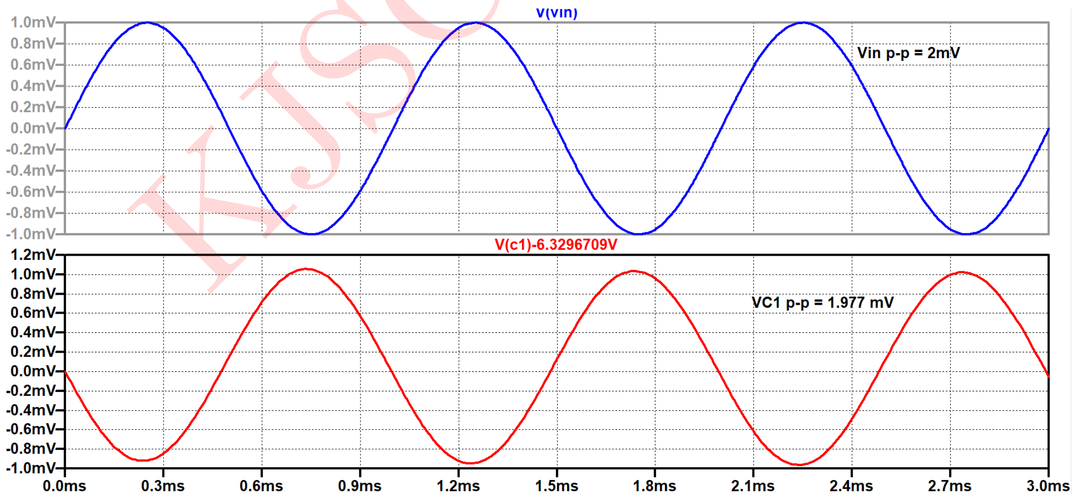

Figure 5: Input output waveform for stage 1

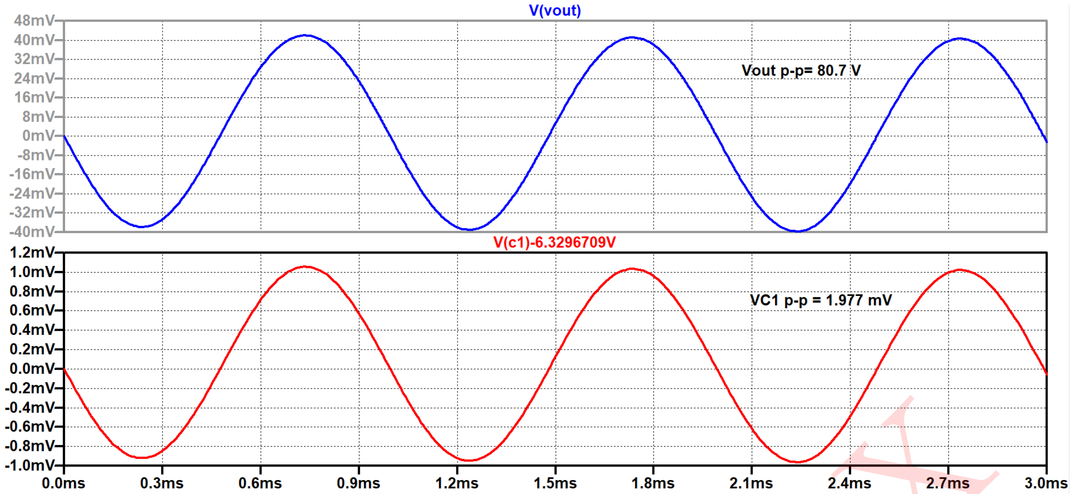

Figure 6: Input output waveform for stage 2

Comparison between Theoretical and Simulated values :-

Parameter	Theoretical	Simulated
I_{C1}	1.45mA	1.3mA
I_{C2}	1.45mA	1.3mA
I_{E1}	1.45mA	1.3mA
I_{E2}	1.45mA	1.3mA
V_{C1}	6.622V	6.33V
V_{C2}	17.185V	18.03V
V_{E1}	6.622V	6.33V
V_{E2}	3.736V	3.943V
V_{B1}	2.44V	2.319V
V_{B2}	7.322V	7.11V
V_{CE1}	4.882V	4.79V
V_{CE2}	10.563V	11.7V
voltage gain of first stage	-0.994	-0.9884
voltage gain of second stage	45.977	40.82
overall voltage gain	-45.7	-40.4
input impedance	$2.476k\Omega$	$-$
output impedance	824.56Ω	$-$

Table 1: Numerical 1

Numerical 2 : A two stage circuit is shown in figure 7. Its EMOS parameters are $k_{n1} = k_{n2} = 1mA/V^2$ and $V_{TN1} = V_{TN2} = 1V$

a. Calculate DC parameters i.e. V_{G1}, V_{G2}, V_{GS1}, V_{GS2} ,V_{D1}, V_{D2}, V_{S1}, V_{DS1}, V_{DS2}, I_{D1}, I_{D2}

b. Calculate input impedance of the circuit.

c. Calculate output impedance of the circuit.

d. Calculate voltage gain of the circuit.

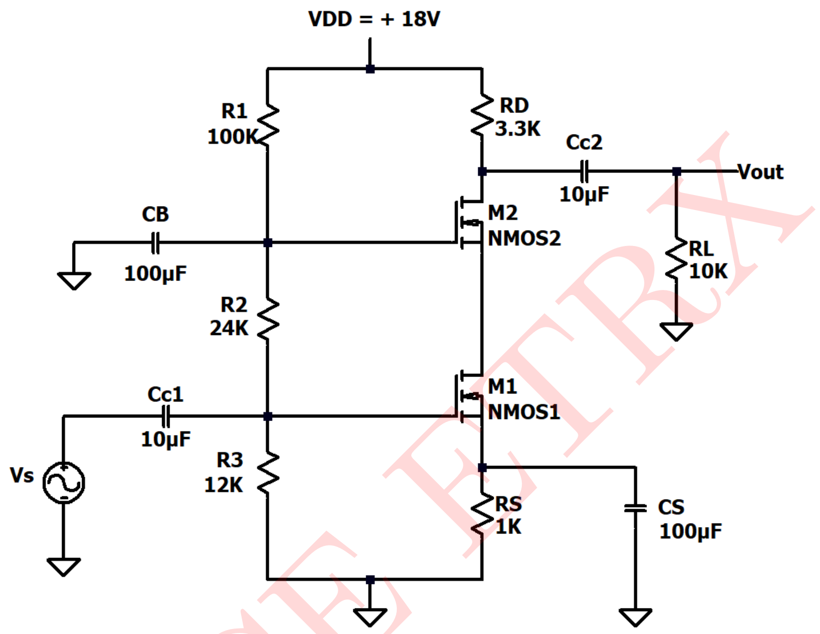

Figure 7: Circuit 2

Solution:

DC ANALYSIS:

$f = 0$, thus $X_C = \infty$, So we replace each capacitor with short circuit,

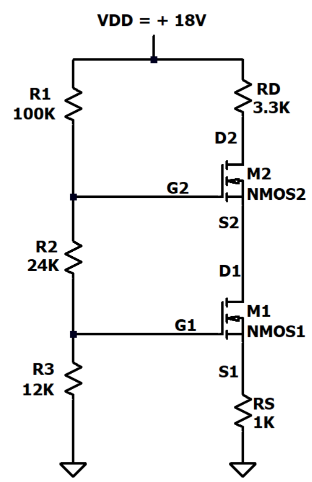

Figure 8: DC Equivalent Circuit

$$V_{G1} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{DD} = \frac{12k}{100k + 24k + 12k} \times 18 = \mathbf{1.588V}$$

$$V_{G2} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{DD} = \frac{12k + 24k}{100k + 24k + 12k} \times 18 = \mathbf{4.764V}$$

$$V_{GS1} = V_{G1} - V_{S1} = 1.588 - I_{D1}R_S = 1.588 - 1000I_{D1} \qquad .....1$$

$$I_{D1} = k_{n1}(V_{GS1} - V_{TN1})^2 = 1 \times 10^{-3}(V_{GS1} - 1)^2 \qquad .....2$$

$$\therefore V_{GS1} = 1.588 - (V_{GS1} - 1)^2$$

$$V_{GS1} = 1.588 - (V_{GS1}^2 - 2V_{GS1} + 1)$$

$$\therefore V_{GS1}^2 - V_{GS1} - 0.588 = 0$$

$\therefore V_{GS1} = -0.415V$ or $1.415V$

But $V_{GS1} > V_D$

$$\therefore V_{GS1} = 1.415V$$

$$I_{D1} = 1 \times 10^{-3}(1.415 - 1)^2 = (0.415)^2 \times 10^{-3} = \mathbf{0.172mA}$$

$$I_{D1} = I_{D2} = \mathbf{0.172mA}$$

$$V_{D2} = V_{DD} - I_{D2}R_D = 18 - (0.172 \times 10^{-3})(3.3 \times 10^3) = \mathbf{17.432V}$$

$$V_{S1} = I_{D1}R_S = \mathbf{0.172V}$$

$$V_{GS1} = V_{GS2} = \mathbf{1.415V}$$

Now, $V_{GS2} = V_{G2} - V_{S2}$

$$V_{S2} = V_{G2} - V_{GS2} = 4.764 - 1.415 = \mathbf{3.349V}$$

$$V_{DS2} = V_{D2} - V_{S2} = \mathbf{14.083V}$$

$$V_{D1} = V_{S2} = \mathbf{3.349V}$$

$$V_{DS1} = V_{D1} - V_{S1} = 3.349 - 0.172 = \mathbf{3.177V}$$

Small Signal Parameters:

$g_{m1} = g_{m2} = 2k_n(V_{GS} - V_{TN}) = 2 \times 1 \times 10^{-3}(1.415 - 1) = \mathbf{0.83mA/V}$

Mid frequency AC equivalent circuit:

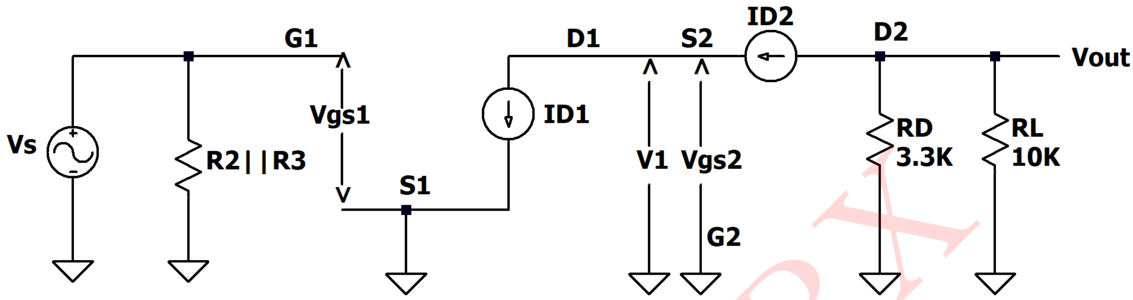

Figure 9: AC mid frequency Equivalent Circuit

Here, $g_{m2}V_{gs2} = g_{m1}V_{gs1}$

$R_G = R_2 \; || \; R_3$

Input impedance:

$Z_i = R_G = R_2 \; || \; R_3 = 24k \; || \; 12k = \mathbf{8k\Omega}$

Output impedance:

$Z_o = R_D \; || \; R_L = 3.3k \; || \; 10k = \mathbf{2.481k\Omega}$

Finding out A_{VT}:

$A_{VT} = A_{V1} \times A_{V2}$

Now, $A_{V1} = \dfrac{V_1}{V_S} = \dfrac{-V_{gs2}}{V_{gs1}} = \mathbf{-1}$

Also, $A_{V2} = \dfrac{V_o}{V_1} = \dfrac{-g_m V_{gs2} R_D \; || \; R_L}{-V_{gs2}} = g_m(R_D \; || \; R_L) = 0.83 \times 10^{-3}(33k||10k) = \mathbf{2.059}$

$A_{VT} = A_{V1} \times A_{V2} = -1 \times 2.059 = \mathbf{-2.059}$

SIMULATED RESULTS:
Above circuit is simulated in LTspice and the result is as follows:

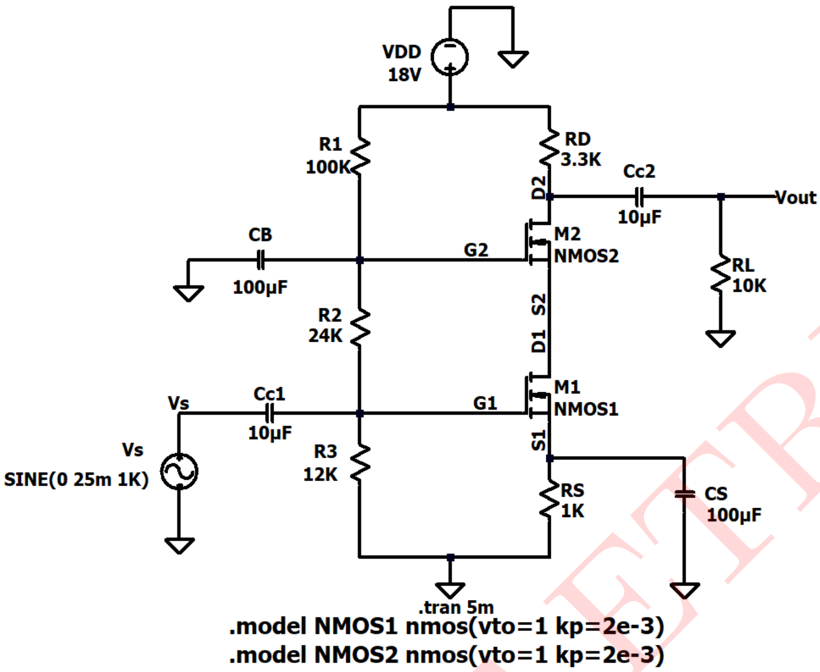

Figure 10: Circuit Schematic

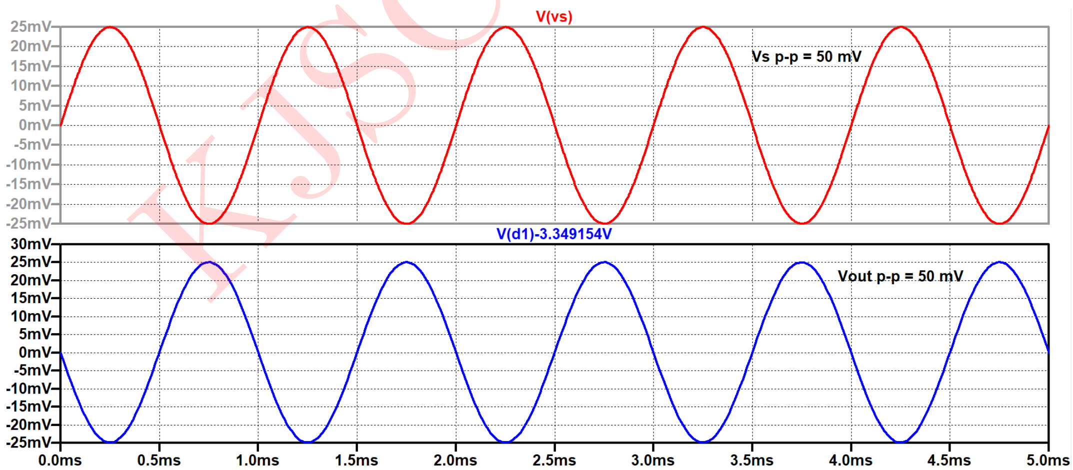

Figure 11: Input output waveform for stage 1

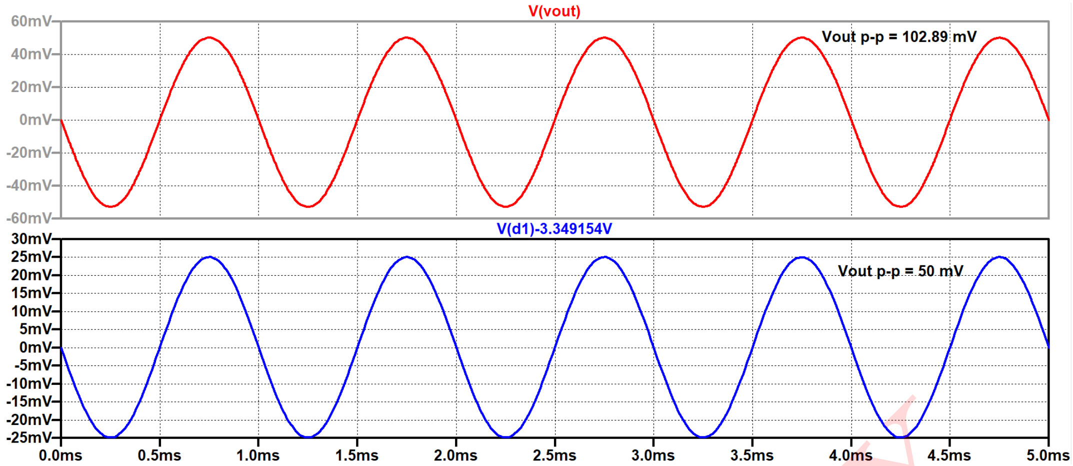

Figure 12: Input output waveform for stage 2

Comparison between Theoretical and Simulated values :-

Parameter	Theoretical	Simulated
V_{G1}	1.588V	1.588V
V_{D1}	3.349V	3.2V
V_{S1}	0.172V	0.0244V
I_{D1}	0.172mA	0.172mA
V_{GS1}	1.415V	1.415V
V_{G2}	4.764V	4.764V
V_{D2}	17.4324V	17.43V
V_{S2}	3.349V	3.2V
I_{D2}	0.172mA	0.172mA
V_{GS2}	1.415V	1.415V
voltage gain of first stage	-1	-1
voltage gain of second stage	2.059	2.058
overall voltage gain	-2.059	-2.058
input impedance	$8k\Omega$	$-$
output impedance	2.481Ω	$-$

Table 2: Numerical 2

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