K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
DC Biasing Circuits

Numerical 1:
Determine the following for the common gate configuration shown in figure 1: V_{GSQ}, I_{DQ}, V_D, V_G, V_S, V_{DS}

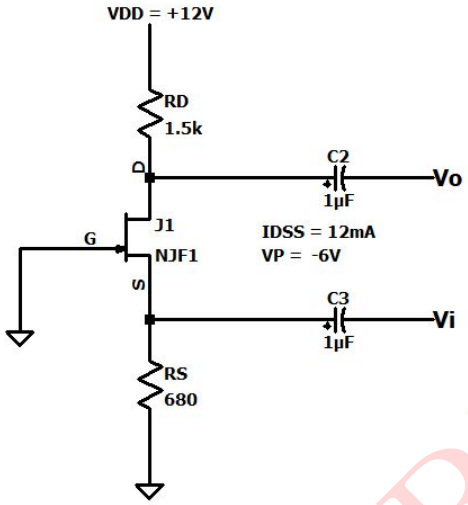

Figure 1: Circuit 1

Solution:
To find these parameters we will perform DC analysis so all capacitors are open circuited.

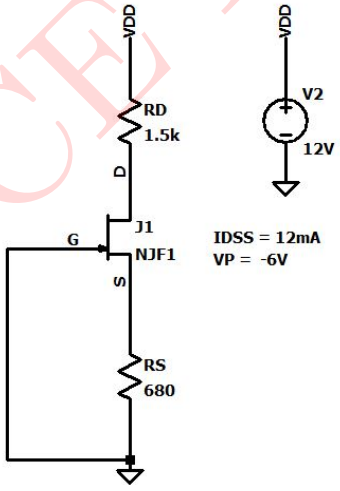

Figure 2: DC Equivalent Circuit

$$V_{GS} = -I_D R_S$$

$$I_D = -\frac{V_{GS}}{R_S}$$

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = (12mA)\left(1 - \frac{V_{GS}}{-6}\right)^2$$

$$\frac{-V_{GS}}{R_S} = (12mA)\left(1 + \frac{V_{GS}}{6}\right)^2$$

$$\frac{-V_{GS}}{680} = (12mA)\left(1 + \frac{V_{GS}}{6}\right)^2$$

$$\frac{-V_{GS}}{680} = (12 \times 10^{-3})\left(1 + \frac{V_{GS}}{3} + \frac{{V_{GS}}^2}{36}\right)$$

$$\frac{-V_{GS}}{680} = 0.012 + 4V_{GS} \times 10^{-3} + \frac{{V_{GS}}^2}{3} \times 10^{-3}$$

$$0 = 0.012 + 5.47V_{GS} \times 10^{-3} + \frac{{V_{GS}}^2}{3} \times 10^{-3}$$

$$0 = 0.012 + (5.47 \times 10^{-3})V_{GS} + (0.33 \times 10^{-3}){V_{GS}}^2$$

$V_{GS} = -2.602$ or $V_{GS} = -13.97$

We reject the value V_{GS} = -13.97 because magnitude of V_{GS} cannot be greater than V_P

V_{GS} = **-2.602V**

$$I_{DQ} = \frac{-V_{GS}}{R_S} = \frac{2.602}{680} = 3.826 \times 10^{-3}A = \mathbf{3.83mA}$$

$V_D = V_{DD} - I_D R_D$

= 12V - (3.8mA)(1.5k)

= 12V - 5.7V = **6.3V**

V_G = **0**

$V_S = I_D R_S = (3.8mA)(680\Omega)$ = **2.58V**

$V_{DS} = V_D - V_S = 6.3V - 2.58V$ = **3.72V**

SIMULATED RESULTS:

The above circuit is simulated in LTspice whose results are given below.

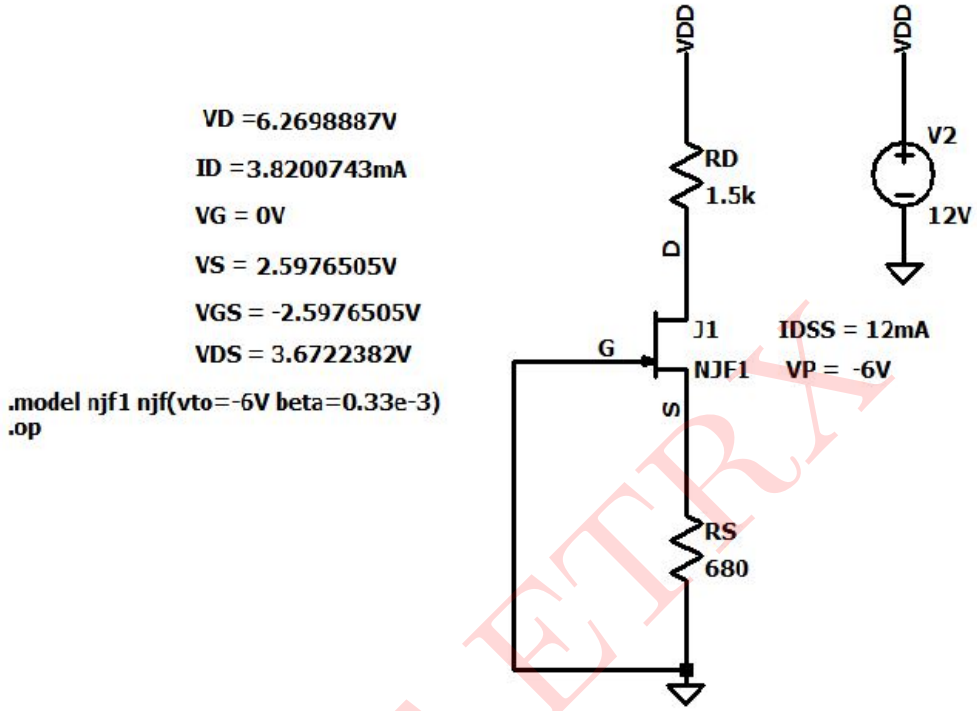

Figure 3: Circuit Schematic: Result

Comparison between theoretical and simulated value

Parameters	Theoretical values	Simulated values
V_{GS}	-2.602V	-2.597V
I_{DQ}	3.83mA	3.820mA
V_D	6.3V	6.269V
V_G	0V	0V
V_S	2.58V	2.597V
V_{DS}	3.72V	3.672V

Table 1: Question 1

Numerical 2:
Determine the following for the network shown in figure 4 : V_{GSQ}, I_{DQ}, V_D, V_{DS}, V_S, V_{DG}

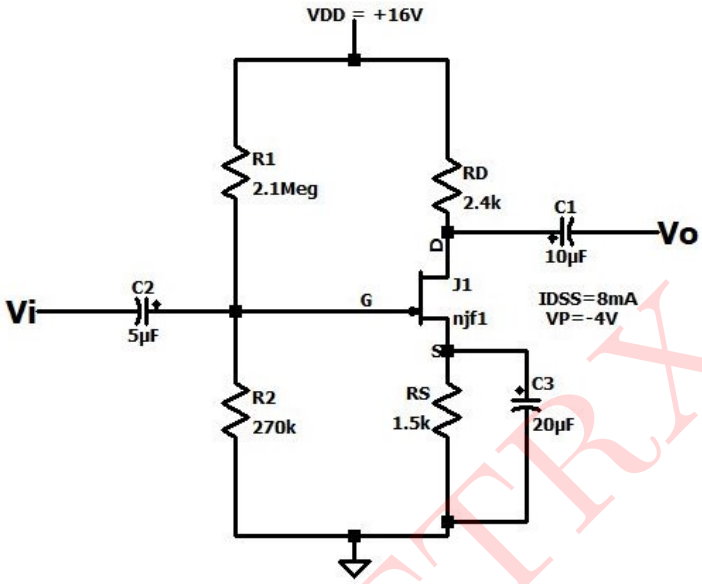

Figure 4: Circuit 2

Solution:
To find the parameters we will perform DC analysis so all capacitors are open circuited.

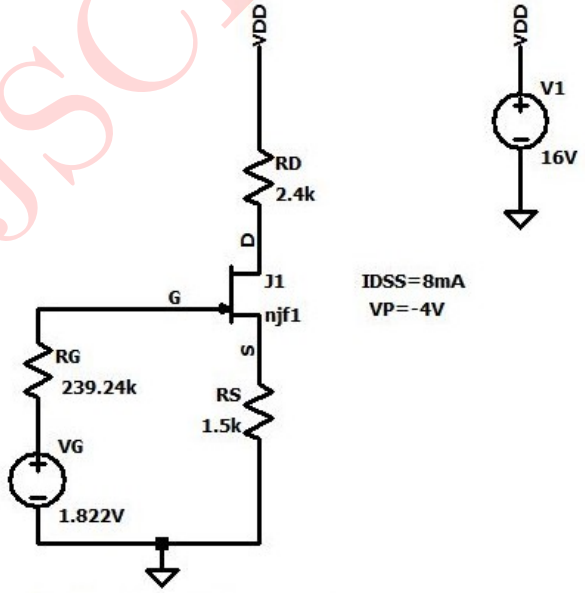

Figure 5: Circuit Schematic

$$R_G = \frac{R_1 R_2}{R_1 + R_2}$$
$$= \frac{270k\Omega \times 2.1M\Omega}{270k\Omega + 2.1M\Omega} = 239.24k\Omega$$

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$$
$$= \frac{270k\Omega}{2.1M\Omega + 270k\Omega} \times 16V = 1.822V$$

Applying KVL to gate source circuit,

$V_G - V_{GS} - I_D R_S = 0$

$V_{GS} = V_G - I_D R_S$

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{1.822 - V_{GS}}{1.5k\Omega}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\frac{1.822 - V_{GS}}{1.5k} = 8mA\left(1 - \frac{V_{GS}}{-4}\right)^2$$

$$\frac{1.822 - V_{GS}}{1.5} = 8 \times 10^{-3}\left(1 + \frac{V_{GS}}{4}\right)^2$$

$$\frac{1.822 - V_{GS}}{1.5} \times 10^{-3} = 8 \times 10^{-3}\left(1 + \frac{V_{GS}}{2} + \frac{{V_{GS}}^2}{16}\right)$$

$$\frac{1.822 - V_{GS}}{1.5} \times 10^{-3} = 8\left(1 + \frac{V_{GS}}{2} + \frac{{V_{GS}}^2}{16}\right)$$

$$1.822 - V_{GS} = 12\left(1 + \frac{V_{GS}}{2} + \frac{{V_{GS}}^2}{16}\right)$$

$1.822 - V_{GS} = 12 + 6V_{GS} + 0.75{V_{GS}}^2$

$0 = 10.178 + 7V_{GS} + 0.75{V_{GS}}^2$

$0.75{V_{GS}}^2 + 7V_{GS} + 10.178 = 0$

$V_{GS} = -1.801V$ or $V_{GS} = -7.53V$

We reject the value $V_{GS} = -7.53V$ because magnitude of V_{GS} cannot be greater than V_p.

$V_{GS} = \mathbf{-1.801V}$

$$I_D = \frac{1.822 - V_{GS}}{1.5k}$$

$$I_D = \frac{1.822 + 1.801}{1.5 \times 10^3} = \mathbf{2.4153mA}$$

$$V_D = V_{DD} - I_D R_D$$
$$= -16V - (2.4mA)(2.4k\Omega) = \mathbf{10.24V}$$

$$V_S = I_D R_S = (2.4mA)(1.5k) = \mathbf{3.6V}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 16V - (2.4mA)(2.4k\Omega + 1.4k\Omega) = \mathbf{6.64V}$$

$$V_{DG} = V_D - V_G$$
$$= 10.24 - 1.82 = \mathbf{8.42V}$$

SIMULATED RESULTS:

The above circuit is simulated in LTspice whose results are given below:

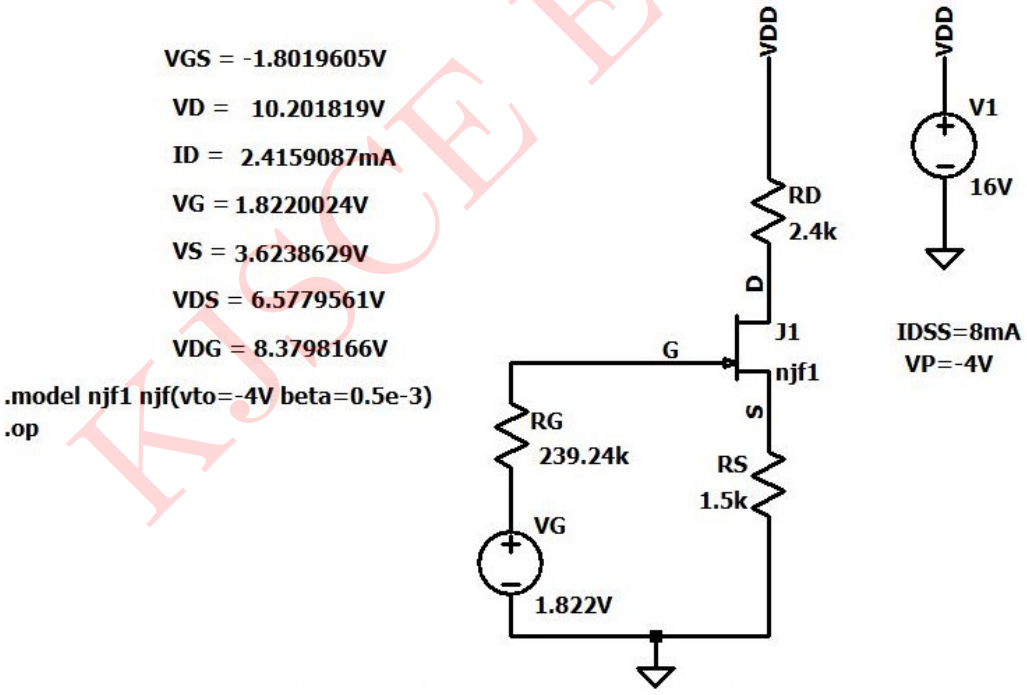

Figure 6: Circuit Schematic: Result

Comparison between theoretical and simulated value:

Parameter	Theoretical values	Simulated values
V_{GS}	-1.801V	-1.8019V
I_D	2.4153mA	2.415mA
V_D	10.24V	10.201V
V_S	3.6V	3.624V
V_{DS}	6.64V	6.5779V
V_{DG}	8.42V	8.3798V

Table 2: Question 2

Numerical 3:
For the fixed-bias of figure given below, determine: I_D and V_{DS}

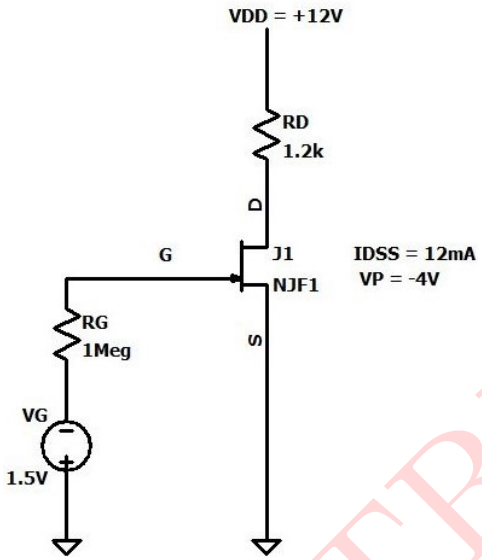

Figure 7: Circuit 3

Solution:
The above circuit is a fixed-bias configuration consisting of a N-channel JFET

Applying KVL to the gate-source loop i.e input loop,

$-V_G - V_{GS} = 0$

$V_{GS} = -V_G = -1.5V$

For JFET,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= (12mA)\left(1 - \frac{(-1.5)}{-4}\right)^2$$

$$= (12 \times 10^{-3})\left(1 - \frac{1.5}{4}\right)^2 = \mathbf{4.69mA}$$

Applying KVL to drain-source loop i.e output loop,

$V_{DD} - I_D R_D - V_{DS} = 0$

$V_{DS} = V_{DD} - I_D R_D$

$= 12 - 4.69 \times 10^{-3} \times 1.2 \times 10^3 = \mathbf{6.372V}$

SIMULATED RESULTS:

The above circuit is simulated in LTspice whose results are given below:

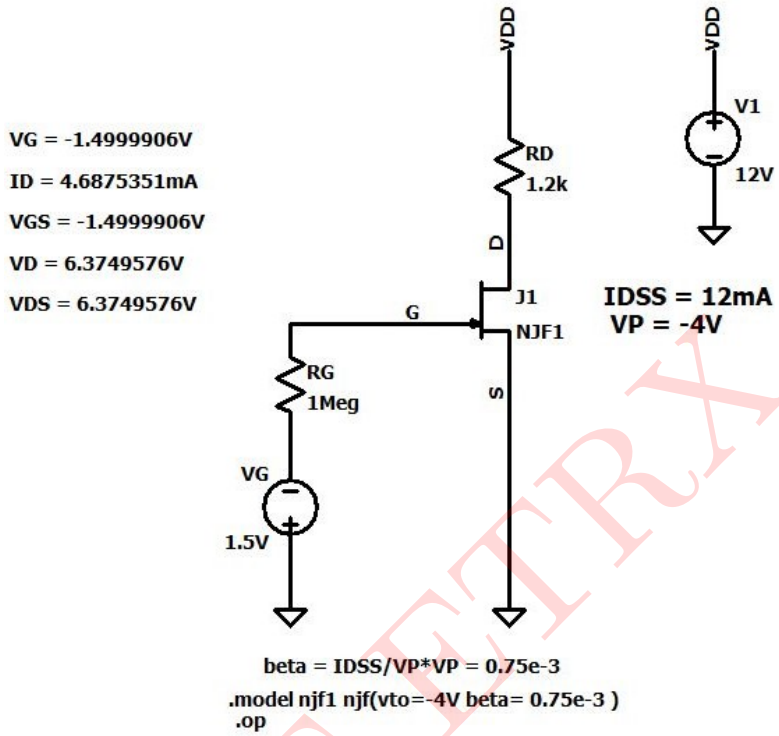

Figure 8: Circuit Schematic: Result

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
V_{GS}	-1.5V	-1.499V
I_D	4.69mA	4.687mA
V_{DS}	6.372V	6.374V

Table 3: Question 3

Numerical 4:
For the circuit given below, determine: I_D, V_{DS}, V_{GS} and V_D

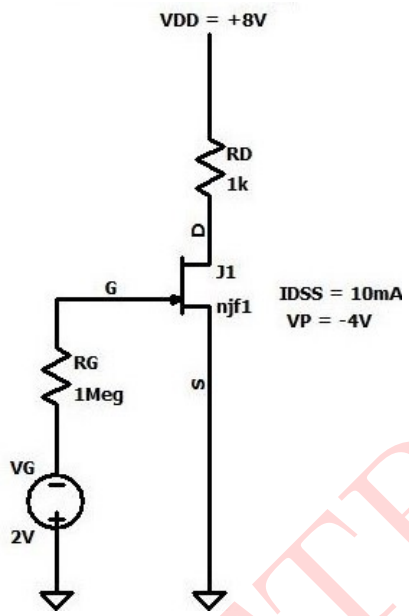

Figure 9: Circuit 4

Solution:
The above circuit is a fixed-bias configuration consisting of a N-channel JFET
In JFET the current through gate is minimised,

$I_G = 0$

$R_G I_G = 0$

Applying KVL to the gate-source loop i.e input loop,

$-V_G - V_{GS} = 0$

$V_{GS} = -V_G = -2V$

For JFET,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= (10mA)\left(1 - \frac{(-2)}{-4}\right)^2$$

$$= (10 \times 10^{-3})\left(1 - \frac{2}{4}\right)^2 = \mathbf{2.5mA}$$

Applying KVL to drain-source loop i.e output loop,

$V_{DD} - I_D R_D - V_{DS} = 0$

$V_{DS} = V_{DD} - I_D R_D$

$= 8 - 2.5 \times 10^{-3} \times 1 \times 10^{3} = 5.5V$

$V_D = V_{DS} = \mathbf{5.5V}$

SIMULATED RESULTS:

The above circuit is simulated in LTspice whose results are given below:

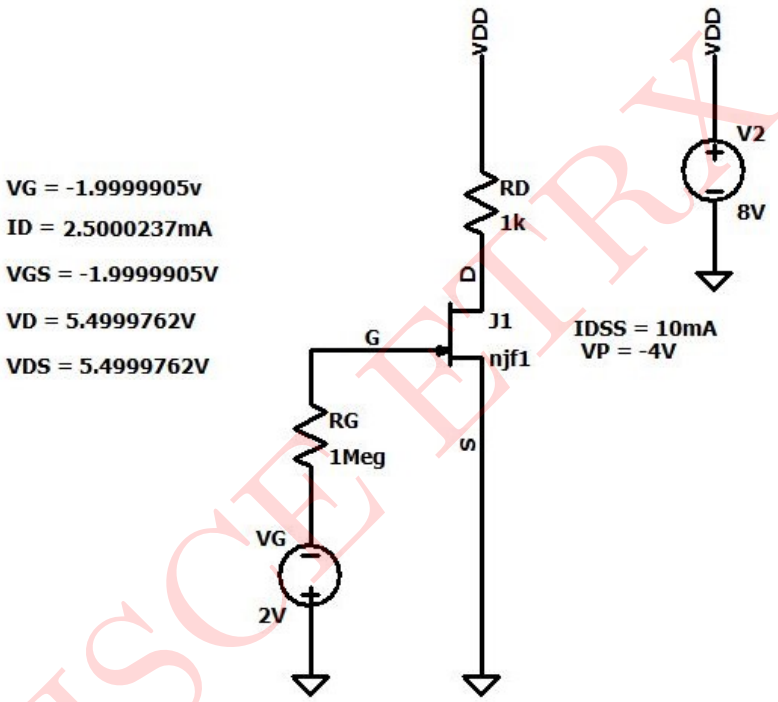

Figure 10: Circuit Schematic: Result

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
V_{GS}	-2V	-1.999V
I_D	2.5mA	2.50mA
V_D	5.5V	5.499V
V_{DS}	5.5V	5.499V

Table 4: Question 4

Numerical 5:
For the circuit given below, $\beta = 125$. Find I_{CQ} and V_{CEQ}

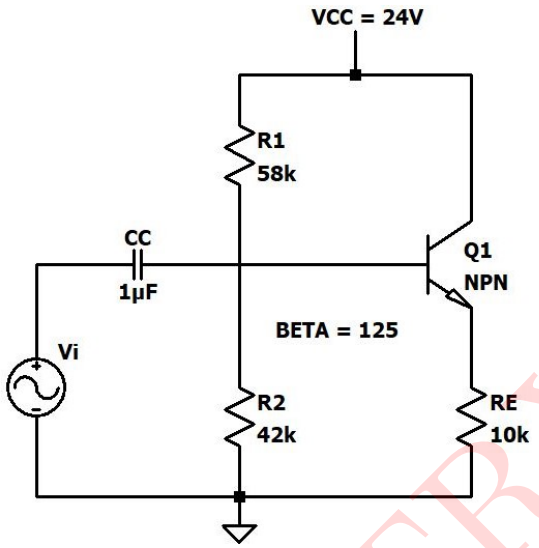

Figure 11: Circuit 5

Solution:
The above circuit is a voltage-bias configuration consisting of a npn BJT.

To determine R_B and V_{TH}

$$R_B = R_1||R_2 = \frac{R_1 R_2}{R_1 + R_2} = \frac{58k \times 42k}{58k + 42k} = \frac{609k}{25k} = \mathbf{24.36k\Omega}$$

$$V_{TH} = \frac{R_2 \times V_{CC}}{R_1 + R_2} = \frac{42k \times 24k}{42k + 24k} = \mathbf{10.08V}$$

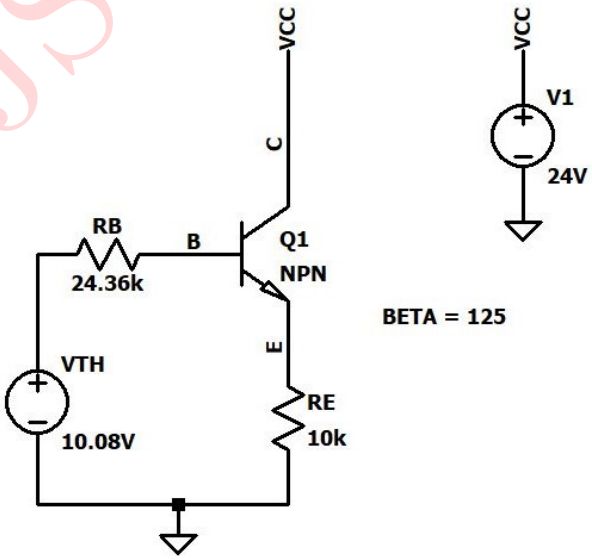

Figure 12: Thevenin's equivalent Circuit

Applying KVL in the base-emitter i.e input loop

$V_{TH} - I_B R_B - V_{BE} - I_E R_E = 0$

$V_{TH} - I_B R_B - V_{BE} - [(1+\beta) I_B] R_E = 0$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$I_B = \frac{10.08 - 0.7}{24.36K + (126)(10k)} = 7.303 \times 10^{-6} A = 7.303 \mu A$$

$I_C = \beta I_B = (125)(7.303 \mu A) = \mathbf{0.913m}A$

Applying KVL to collector-emitter loop i.e output loop,

$V_{CC} - V_{CE} - I_E R_E = 0$

$V_{CC} - V_{CE} - I_C R_E = 0 \qquad (\because I_C = I_E)$

$24 - V_{CE} - (0.913mA)(10k\Omega) = 0$

$V_{CE} = 24 - 9.13 = \mathbf{14.87V}$

SIMULATED RESULTS:

The above circuit is simulated in LTspice whose results are given below:

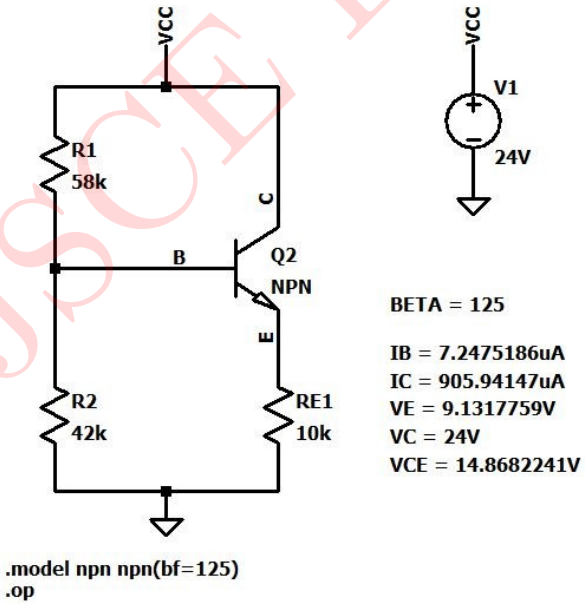

Figure 13: Circuit Schematic: Results

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
I_C	0.913mA	0.90594mA
V_{CE}	14.87V	14.8682V

Table 5: Question 5

Numerical 6:
For the circuit given below in figure 14, determine $V_{GSQ}, I_{DQ}, V_{DS}, V_D, V_G, V_S$

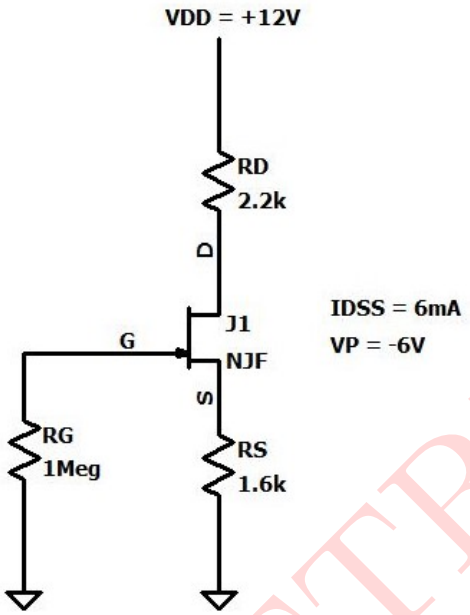

Figure 14: Circuit 6

Solution:
The above circuit is a fixed-bias configuration consisting of N-channel JFET.
In JFET the current through gate is negligible,
i.e $I_G = 0$
$R_G I_G = 0$

Applying KVL to the gate-source loop i.e input loop,
$-V_{GS} - I_D R_S = 0$
$V_{GS} = -I_D R_S = -I_D(1.6k\Omega)$
$$I_D = \frac{-V_{GS}}{1.6k\Omega}$$

For JFET, the drain current is given by
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$\frac{-V_{GS}}{1.6k} = 6mA\left(1 - \frac{V_{GS}}{-6}\right)^2$$
$$\frac{-V_{GS}}{1.6k} = 6mA\left(1 + \frac{V_{GS}}{6}\right)^2$$
$$\frac{-V_{GS}}{1.6k} = 6mA\left(1 + \frac{V_{GS}}{3} + \frac{{V_{GS}}^2}{36}\right)$$
$$\frac{-V_{GS}}{1.6} \times 10^{-3} = 6 \times 10^{-3}\left(1 + \frac{V_{GS}}{3} + \frac{{V_{GS}}^2}{36}\right)$$

$$\frac{-V_{GS}}{1.6} = 6\left(1 + \frac{V_{GS}}{3} + \frac{{V_{GS}}^2}{36}\right)$$

$$-V_{GS} = 9.6\left(1 + \frac{V_{GS}}{3} + \frac{{V_{GS}}^2}{36}\right)$$

$$-V_{GS} = 9.6 + 3.2V_{GS} + 0.266{V_{GS}}^2$$

$$0 = 9.6 + 4.2V_{GS} + 0.266{V_{GS}}^2$$

$$V_{GS} = -2.774V \text{ or } V_{GS} = -13.01V$$

We reject the value $V_{GS} = -13.01V \quad \because |V_{GS}| < |V_P|$

$$V_{GS} = -2.774V$$

$$I_D = \frac{-V_{GS}}{1.6k\Omega} = \frac{-2.774V}{1.6k\Omega} = \mathbf{1.7337mA}$$

$$\begin{aligned} V_D &= V_{DD} - I_D R_D \\ &= 12 - (1.73mA)(2.2k\Omega) \\ &= 12 - 3.314 = \ \mathbf{8.18V} \end{aligned}$$

$$\begin{aligned} V_S &= I_D R_S \\ &= 12 - (1.73mA)(1.6k\Omega) = \mathbf{2.768V} \end{aligned}$$

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ &= 12 - (1.73mA)(2.2k\Omega + 1.6k\Omega) \\ &= 12 - 6.574 = \ \mathbf{5.426V} \end{aligned}$$

$$V_G = \ \mathbf{0}V$$

SIMULATED RESULTS:
The above circuit is simulated in LTspice whose results are given below:

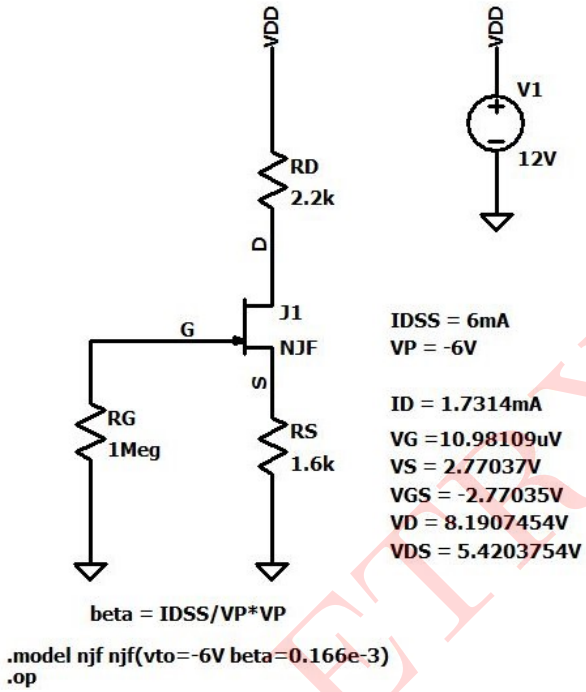

Figure 15: Circuit Schematic: Results

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
I_D	1.733mA	1.7314mA
V_{GS}	-2.774V	-2.77037V
V_D	8.18V	8.1907V
V_S	2.768V	2.7703V
V_{DS}	5.426V	5.4204V
V_G	0V	0.00001V

Table 6: Question 6

Numerical 7:
The transistor given in the circuit below in figure 16, has parameters $I_{DSS} = 8mA$ and $V_P = -4V$. Determine V_G, I_{DQ}, V_{GSQ} and V_{DSQ}

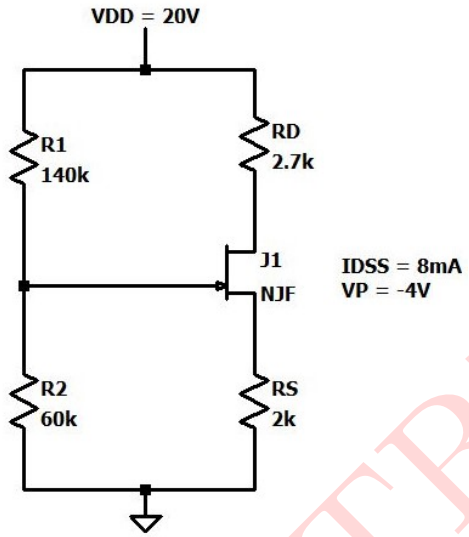

Figure 16: Circuit 7

Solution:
The above circuit is a voltage-bias configuration consisting of N-channel JFET.

To determine R_G and V_{TH},

i.e $R_G = \dfrac{R_1 \times R_2}{R_1 + R_2} = \dfrac{140k \times 60k}{140k + 60k} = \mathbf{42k\Omega}$

$V_{TH} = \dfrac{R_2}{R_1 + R_2} \times V_{DD} = \dfrac{60}{140 + 60} \times 20V = \mathbf{6V}$

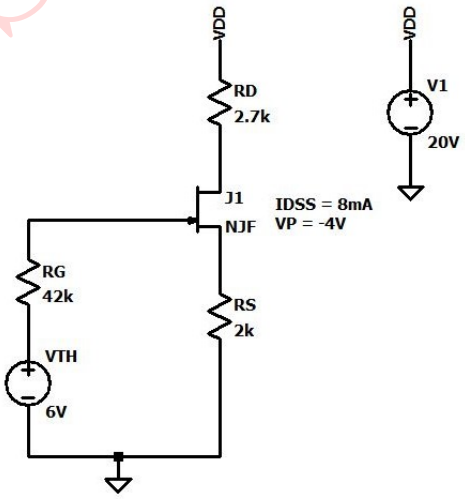

Figure 17: Thevenin's equivalent circuit

In JFET, current through gate is zero, i.e $I_G = 0$

Applying KVL in gate-source loop i.e input loop,

$V_{TH} - I_G R_G - I_D R_S = 0 \qquad (\because I_G = 0, I_G R_G = 0)$

$V_{TH} - V_{GS} - I_D R_S = 0$

$V_{GS} = V_{TH} - I_D R_S$

$V_{GS} = 6V - I_D(2k\Omega)$

$\therefore I_D = \dfrac{6 - V_{GS}}{2k\Omega}$

In JFET,

$I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2$

$I_D = 8mA\left(1 - \dfrac{V_{GS}}{-4}\right)^2$

$I_D = 8mA\left(1 + \dfrac{V_{GS}}{4}\right)^2$

$\dfrac{6 - V_{GS}}{2k\Omega} = 8mA\left(1 + \dfrac{V_{GS}}{4}\right)^2$

$6 - V_{GS} = (2 \times 10^{-3})(8 \times 10^{-3})\left(1 + \dfrac{V_{GS}}{4}\right)^2$

$6 - V_{GS} = 16\left(1 + \dfrac{V_{GS}}{2} + \dfrac{{V_{GS}}^2}{16}\right)$

$6 - V_{GS} = 16 + 8V_{GS} + {V_{GS}}^2$

$0 = 16 - 6 + 8V_{GS} + V_{GS} + {V_{GS}}^2$

$0 = 10 + 9V_{GS} + {V_{GS}}^2$

$V_{GS} = -1.298V$ or $V_{GS} = -7.7015V$

We reject the value $V_{GS} = -7.7015V \qquad \because |V_{GS}| < |V_P|$

$\therefore V_{GS} = \mathbf{-1.298V}$

$I_D = \dfrac{6 - V_{GS}}{2k\Omega} = \dfrac{6 - (-1.293)}{2 \times 10^3} = \mathbf{3.649mA}$

Applying KVL to drain source loop i.e output loop,

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$V_{DS} = V_{DD} - I_D R_D - I_D R_S$

$= 20V - (3.649mA)(2.7k\Omega) - (3.649mA)(2k\Omega) = \mathbf{2.8497V}$

$V_{TH} = V_G = \mathbf{6V}$

SIMULATED RESULTS:
The above circuit is simulated in LTspice whose results are given below:

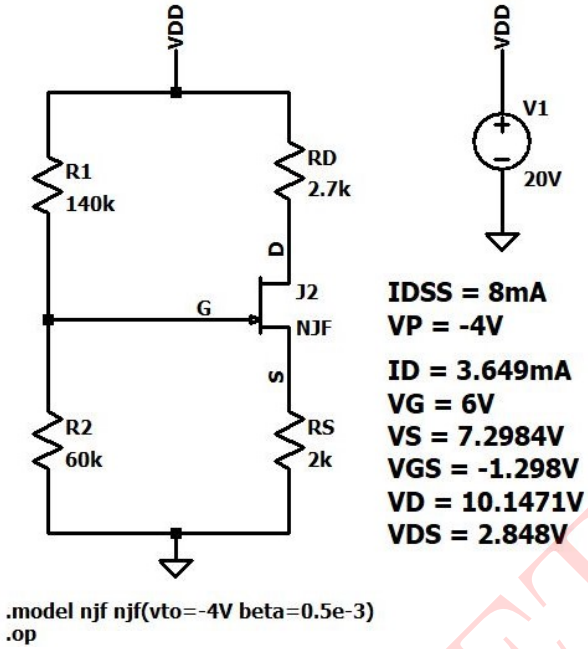

Figure 18: Circuit Schematic: Results

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
I_D	3.649mA	3.6492mA
V_{GS}	-1.298V	-1.29844V
V_{DS}	2.8497V	2.84366V
V_G	6V	6V

Table 7: Question 7

Numerical 8:
Consider the circuit given below in figure 19. The quiescent value of V_{DS} is found to be $V_{DSQ} = 5V$. If $I_{DSS} = 10mA$, determine I_{DQ}, V_{GSQ} and V_P

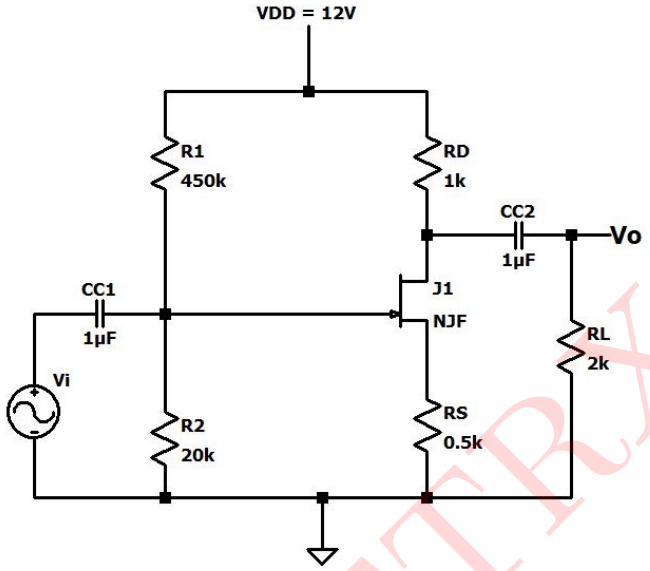

Figure 19: Circuit 8

Solution:
The above circuit 8 is a voltage-biased network consisting of a N-channel JFET.

For DC analysis all capacitors will be open circuited.

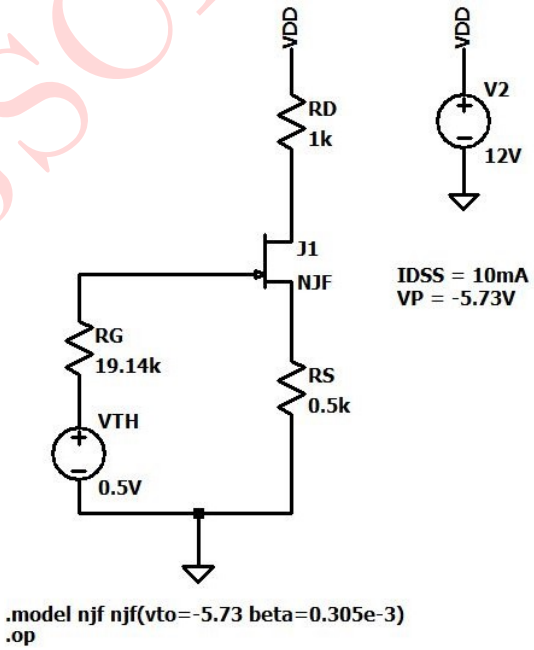

Figure 20: Thevenin's equivalent circuit

To find R_G and V_{TH}:

$$R_G = \frac{R_1 R_2}{R_1 + R_2} = \frac{450k\Omega \times 20k\Omega}{450k\Omega + 20k\Omega} = \mathbf{19.14k\Omega}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{20k\Omega}{450k\Omega + 20k\Omega} \times 12V = \mathbf{0.51V}$$

Applying KVL to the drain-source loop i.e output loop,

i.e $V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$12 - I_D(1k\Omega) - 5V - I_D(0.5k\Omega) = 0$

$7 - 1.5 I_D \times 10^3 = 0$

$1.5 \times 10^3 I_D = 7$

$$I_D = \frac{7}{1.5 \times 10^3} = \mathbf{4.66mA}$$

Applying KVL to the gate-source loop i.e input loop,

$V_{TH} - I_G R_G - V_{GS} - I_D R_S = 0 \qquad (\because I_G = 0, I_G R_G = 0)$

$\therefore V_{TH} - V_{GS} - I_D R_S = 0$

$V_{GS} = V_{TH} - I_D R_S$

$= 0.51V - (4.66mA)(0.5k\Omega) = 0.51 - 2.33 = \mathbf{-1.82V}$

For JFET,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$4.66mA = 10mA\left(1 + \frac{1.82}{V_P}\right)^2$$

$$4.66 \times 10^{-3} = 10 \times 10^{-3}\left(1 + \frac{V_{GS}}{6}\right)^2$$

$$1 = \frac{10}{4.66}\left(\frac{V_P + 1.82}{V_P}\right)^2$$

$$1 = 2.145\frac{(V_P + 1.82)^2}{{V_P}^2}$$

${V_P}^2 = 2.145(V_P + 1.82)^2$

${V_P}^2 = 2.145({V_P}^2 + 3.64V_P + 3.3124)$

${V_P}^2 = 2.145{V_P}^2 + 7.8078V_P + 7.10598$

$0 = 1.145{V_P}^2 + 7.8078V_P + 7.10598$

$V_P = -1.08V$ or $V_P = -5.73V$

We reject the value $V_P = -1.08V \qquad \because |V_{GS}| < |V_P|$

$\therefore V_P = \mathbf{-5.73V}$

SIMULATED RESULTS:

The above circuit is simulated in LTspice whose results are given below:

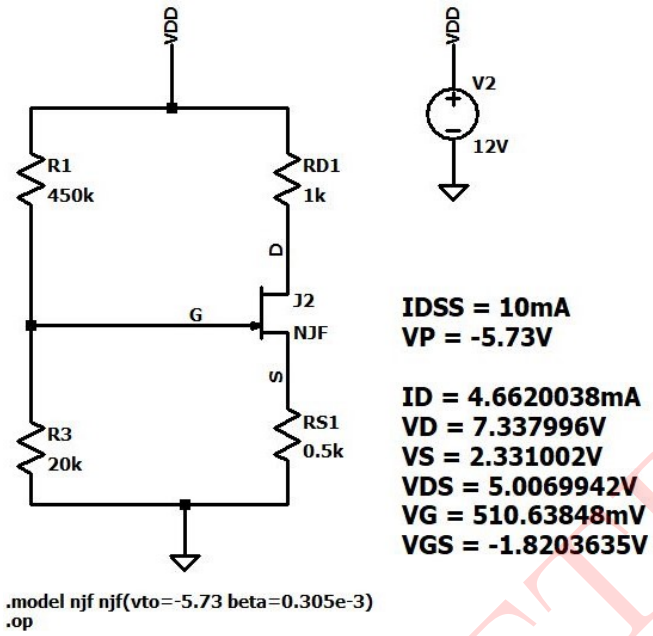

Figure 21: Circuit Schematic: Results

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
I_D	4.66mA	4.66200mA
V_{GS}	-1.82V	-1.8206V

Table 8: Question 8

Numerical 9:
The emitter follower for the circuit given below in figure 22 has $R_1 = 100k\Omega$, $R_2 = 150k\Omega$, $R_E = 750\Omega$, $R_L = 20k\Omega$, $R_C = 200\Omega$, $V_{CC} = 15V$ and $V_{BE} = 0.7V$. Assume that $\beta_F = 100$. Find the Q-point defined by I_B, I_C and V_{CE}

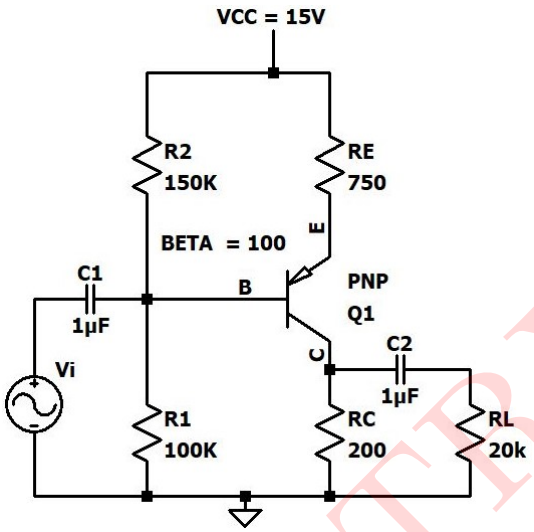

Figure 22: Circuit 9

Solution:
The above figure 22 is a circuit consisting of voltage bias configuration.

To find the parameters we need to perform DC analysis and for that we require a DC equivalent circuit.

For DC analysis all capacitors will be open circuited.

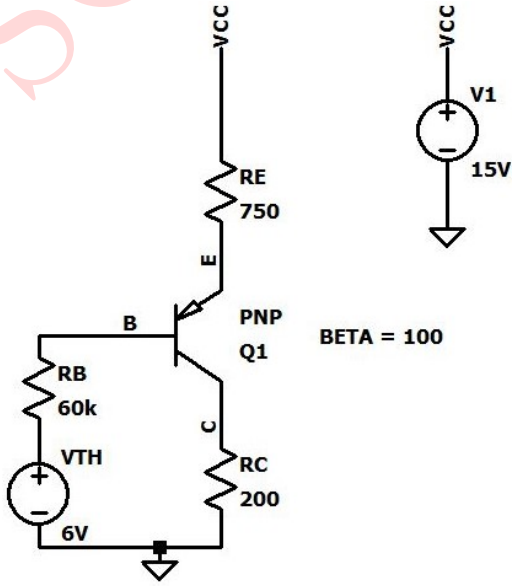

Figure 23: Thevenin's equivalent circuit

To find R_B and V_{TH}:

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{100k\Omega \times 150k\Omega}{100k\Omega + 150k\Omega} = \mathbf{60k\Omega}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{100k\Omega}{100k\Omega + 150k\Omega} \times 15V = \mathbf{6V}$$

Applying KVL to the emitter-base loop,

i.e $V_{CC} - I_E R_E - V_{EB} - I_B R_B - V_{TH} = 0$

$15V - (1+\beta) I_B (750\Omega) - 0.7V - I_B (60k\Omega) = 0$

$$\therefore I_B = \frac{15V - 0.76V}{75750 + 60k} = \mathbf{61.14\mu A}$$

$$\therefore I_C = \beta I_B = 100(61 - 14\mu A) = \mathbf{6.114mA}$$

Applying KVL to the emitter-collector loop,

$V_{CC} - I_E R_E - V_{EC} - I_C R_C = 0$

$\therefore V_{EC} = V_{CC} - (1+\beta) I_B R_E - I_C R_C$

$\therefore V_{EC} = 15V - (101)(61.14 \times 10^{-6})750 - (6.114 \times 10^{-3})(200)$

$= 15 - 4.63 - 1.2228 = \mathbf{9.147V}$

$\therefore V_{CE} = \mathbf{-9.147V}$

SIMULATED RESULTS:

The above circuit is simulated in LTspice whose results are given below:

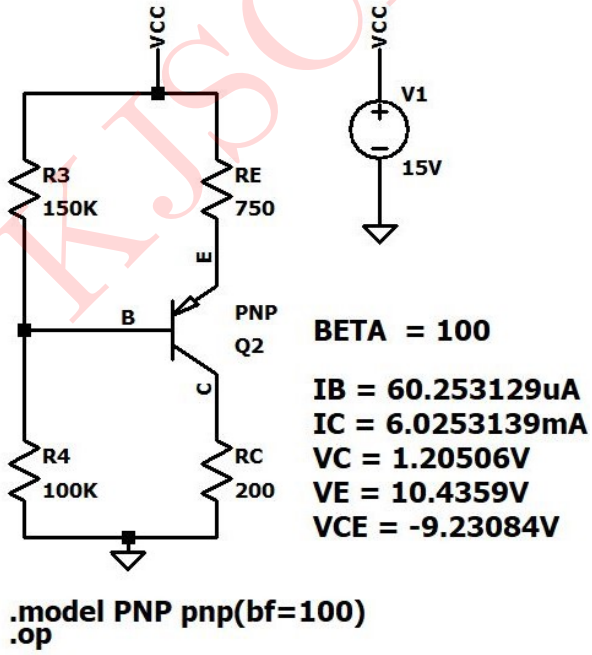

Figure 24: Circuit Schematic: Results

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
I_B	61.14μA	60.253μA
I_C	6.114mA	6.0253mA
V_{CE}	-9.147V	-9.23079V

Table 9: Question 9

Numerical 10:
The NMOS biasing circuit given below in figure 25 has $R_D = 1.5k\Omega$, $R_G = 500k\Omega$ and $V_{DD} = 12V$. The MOS parameters are $k_n = 0.5mA/V^2$, $V_{GS_{th}} = 1V$ and $\lambda = 0.01$. Determine the drain current I_D, the gate to source voltage V_{GS} and the drain to source voltage V_{DS}

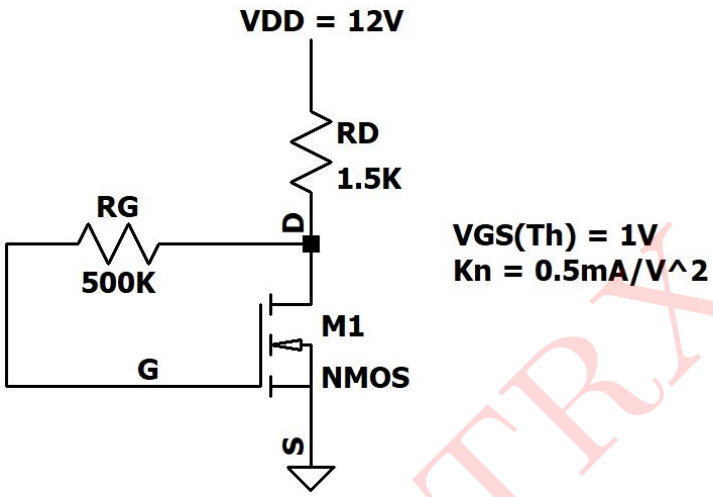

Figure 25: Circuit 10

Solution:

The above circuit in figure 25 is drain feedback bias consisting of N-channel E-MOSFET. The gate current is zero, $I_G = 0$

$\therefore$ resistance R_G is redundant

$\therefore V_{GS} = V_{DS} = V_{DD} - I_D R_D$

$\therefore V_{GS} = 12 - I_D(1.5k)$

$$I_D = \frac{12 - V_{GS}}{1.5k}$$

In MOSFET,

i.e $I_D = k_n(V_{GS} - V_{GS_{th}})^2(1 + \lambda V_{DS})$

$$\frac{12 - V_{GS}}{1.5k} = k_n(V_{GS} - 1)^2(1 + \lambda V_{DS})$$

$$\frac{12 - V_{GS}}{1.5k} = 0.5m({V_{GS}}^2 - 2V_{GS} + 1)(1 + 0.01V_{GS})$$

$$12 - V_{GS} = (0.5m)(1.5k)({V_{GS}}^2 - 2V_{GS} + 1)(1 + 0.01V_{GS})$$

$$12 - V_{GS} = 0.75(0.01{V_{GS}}^3 + 0.98{V_{GS}}^2 - 1.99V_{GS} + 1)$$

$$12 - V_{GS} = (7.5 \times 10^{-3}){V_{GS}}^3 + 0.735{V_{GS}}^2 - 1.4925V_{GS} + 0.75$$

$$\therefore (7.5 \times 10^{-3}){V_{GS}}^3 + 0.735{V_{GS}}^2 - 1.4925V_{GS} - 11.25 = 0$$

$V_{GS} = -98.51V$ or $V_{GS} = 4.1665V$ or $V_{GS} = -3.65V$

$V_{GS} = \mathbf{4.1665V} \qquad (\because |V_{GS}| > |V_t|)$

$$\because I_D = \frac{12 - V_{GS}}{1.5k} = \frac{12 - 4.166}{1.5k} = \mathbf{5.22mA}$$

$V_{DS} = V_{GS} = \mathbf{4.1665V}$

SIMULATED RESULTS:
The above circuit is simulated in LTspice whose results are given below:

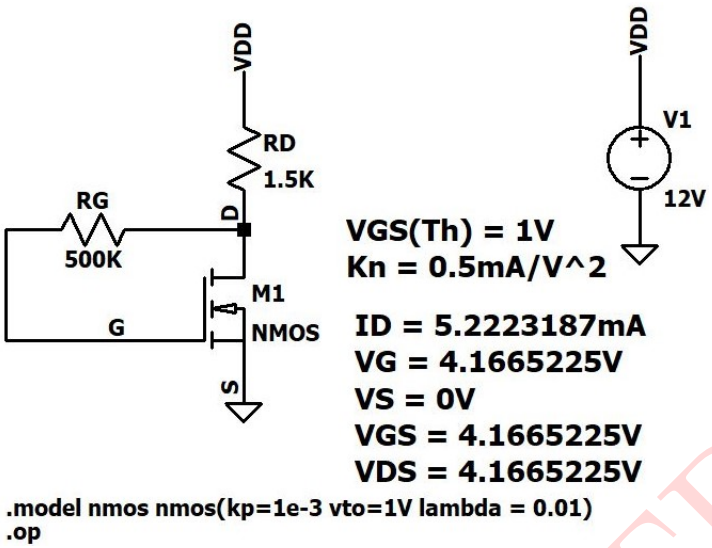

Figure 26: Circuit Schematic: Results

Comparison between theoretical and simulated values:

Parameters	Theoretical values	Simulated values
I_D	5.22mA	5.22231mA
V_{GS}	4.1665V	4.16652V
V_{DS}	4.1665V	4.16652V

Table 10: Question 10

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