K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
CASCADE AMPLIFIER DESIGN

16^{th} **July, 2020** **Numericals**

1. Design a two stage RC coupled cascade amplifier for the following specifications:
   $A_V \geq 1800$, $V_o(rms) = 2.4$ V, $S \leq 10$, $f_L \geq 25$ Hz
   Use transistor BC147A from data-sheet

Solution:
Step 1: Circuit diagram

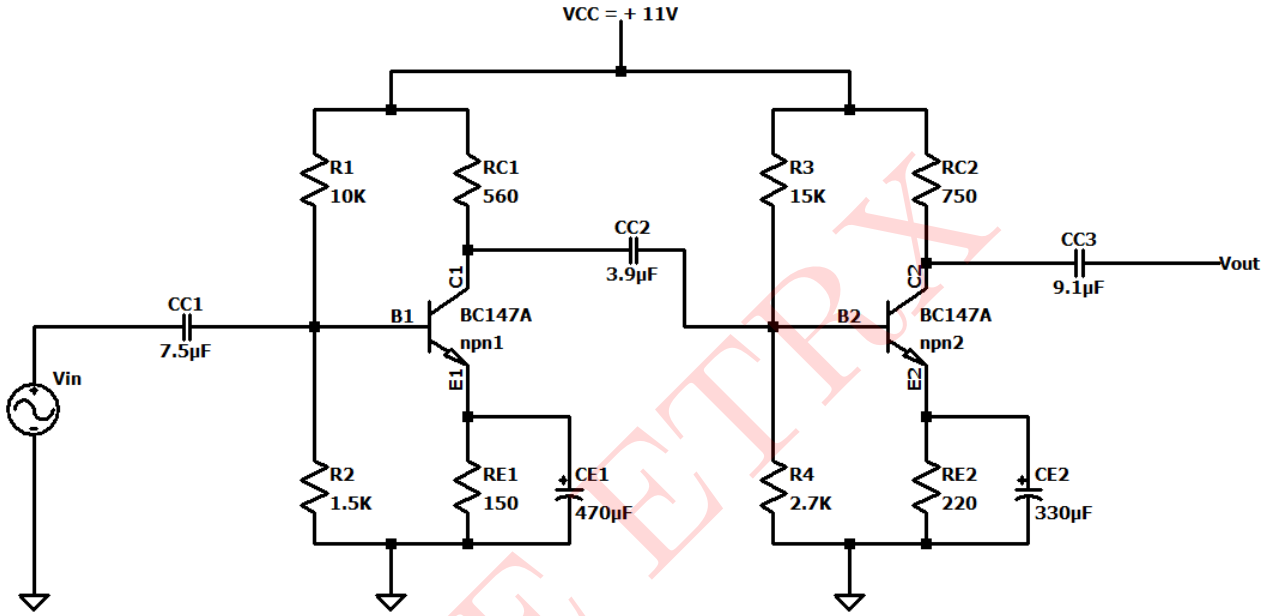

Figure 1: Circuit diagram and selection of transistor

Transistor BC147A:
$h_{fe}(min) = 125$
$h_{fe}(max) = 260$
$h_{fe}(typ) = 220$
$h_{ie} = 2.7$ kΩ
$h_{FE}(typ) = 180$
$h_{FE}(min) = 115$
$h_{FE}(max) = 220$
$V_{CE}(sat) = 0.25$ V

We use voltage divider biasing because it provides stability of Q-point against variations in β or stability of Q-point against variation in temperature

Step 2: Given data
$A_V \geq 1800$
$V_{orms} = 2.4$ V
$S \leq 10$
$f_L \geq 25$ Hz

Step 3: Selection of voltage gains
$A_{V_T} = A_{V_1} \times A_{V_2} = 1800$

$A_{V_1} = 0.5 \times A_{V_2}$

$\therefore$ we get, $A_{V_1} = 30$, $A_{V_2} = 60$

Design of 2nd stage
Step 4: Calculation of $\mathbf{R_{C_2}}$

$$|A_{V_2}| = \frac{h_{fe}(typ) \times R_{C_2}}{h_{ie}} = \frac{220 \times R_{C_2}}{2.7k}$$

$$60 = \frac{220 \times R_{C_2}}{2.7k}, \therefore R_{C_2} = 736.3636\Omega$$

Selecting HSV, $R_{C_2} = 750\Omega$, 1/4 W

Step 5: Selection of Q-point ($\mathbf{V_{CEQ}}, \mathbf{I_{CQ}}$)

$V_o(peak) = V_o(rms) \times \sqrt{2}$

$V_o(peak) = 2.4 \times \sqrt{2} = 3.394$ V

$V_{CEQ_2} = 1.5 \times [V_o(peak) + V_{CE}(sat)]$

The value is multiplied by 1.5 to take care of saturation voltages, variation in resistance, variation in supply voltage and variation in device parameters.

$V_{CEQ_2} = 1.5 \times [3.394 + 0.25] = 5.466$ V

We select $V_{CEQ_2} = 5.5$ V

$$I_o(peak) = \frac{V_o(peak)}{R_{C_2}} = \frac{3.394}{750}$$

$\therefore I_o(peak) = 4.52533$ mA

$I_{CQ_2} \geq I_o(peak)$ (for undistorted output signal)

$\therefore I_{CQ_2} = 4.6$ mA

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{4.6 \times 10^{-3}}{180}$$

$\therefore I_{BQ_2} = 25.556\ \mu$A

Step 6: Selection of DC power supply $\mathbf{V_{CC}}$
In order to achieve maximum symmetrical output swing, always select Q-point at the center of DC load line
i.e. $V_{CC} \geq 2V_{CEQ_2}$, i.e. $V_{CC} \geq 2 \times 5.5$

Selecting HSV, $V_{CC} = 11$ V

$I_{EQ_2} = I_{CQ} + I_{BQ} = 4.62556$ mA

Step 7: Calculation of $\mathbf{R_{E_2}}$
For proper operation, $V_{RE_2} = 10\%$ of $V_{CC} = 0.1V_{CC}$

$\therefore V_{RE_2} = 1.1$ V

$V_{RE_2} = R_{E_2} \times I_{EQ_2}$

$$\therefore R_{E_2} = \frac{V_{RE_2}}{I_{EQ_2}} \approx \frac{V_{RE_2}}{I_{CQ_2}} = \frac{1.1}{4.6 \times 10^{-3}} = 2.3913\Omega$$

Selecting LSV, $R_{E_2} = 220\Omega$, 1/4 W

$V_{E_2} = I_{EQ} \times R_{E_2} = 1.0176$ V

Step 8: Calculation of biasing resistors (R_3 and R_4)

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_{E_2}}{R_{E_2}+R_{B_2}}\right)}$$

$\beta = h_{FE}(typ) = 180$

$$10 = \frac{181}{1+180\left(\frac{220}{220+R_{B_2}}\right)}$$

$$R_{th_2} = R_{B_2} = R_3||R_4 = \frac{R_3 \times R_4}{R_3+R_4} \quad \text{.....(1)}$$

$$V_{th_2} = V_{B_2} = \frac{R_4}{R_3+R_4} \times V_{CC} \quad \text{.....(2)}$$

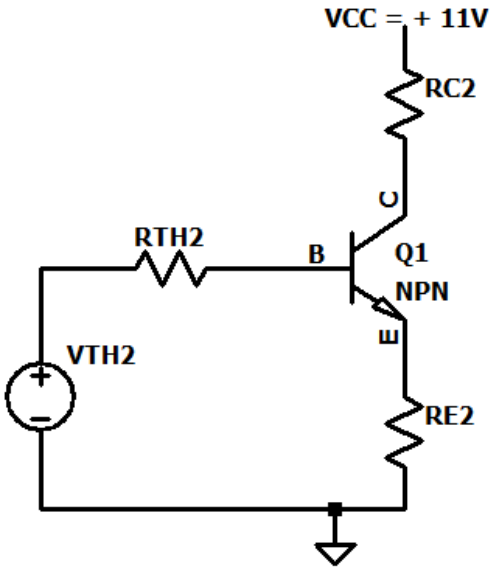

Figure 2: DC equivalent circuit for stage 2

Applying KVL at B-E loop of Q_2

$$V_{B_2} - I_{BQ_2}R_{B_2} - V_{BE_2} - I_{EQ_2}R_{E_2} = 0$$

$$V_{B_2} = V_{BE_2} + \frac{I_{CQ_2} \times R_{B_2}}{\beta} + I_{CQ_2}R_E$$

$$V_{B_2} = 0.7 + \frac{4.6 \times 10^{-3}}{180} \times 2.0957k + (4.6 \times 10^{-3} \times 220)$$

$$\therefore V_{B_2} = 1.712 \text{ V}$$

From equation (2), $\frac{R_4}{R_3 + R_4} \times 11 = 1.712$

$$\therefore \frac{R_4}{R_3 + R_4} = 0.1556 \qquad \text{.....(3)}$$

Put equation (3) in equation (1)

$$R_3 \times 0.1556 = 2.0957k$$

$$\therefore R_3 = 13.4685 \text{ k}\Omega$$

Selecting HSV, $R_3 = 15$ kΩ, 1/4 W

From equation (3), $\frac{R_4}{15k + R_4} = 0.1556$

$$\therefore R_4 = 2.76409 \text{ k}\Omega$$

Selecting LSV, $R_4 = 2.7$ kΩ, 1/4 W

Design of 1st stage
Step 9: Selection of R_{C_1}

$$|A_{V_2}| = \frac{h_{fe}(typ) \times R_{C_2}}{h_{ie}} = \frac{220 \times 750}{2.7k} = 61.11$$

$$A_{V_1} = \frac{A_{V_T}}{A_{V_2}} = \frac{1800}{61.11} = 29.45508$$

Let $A_{V_1} = 30$

$$A_{V_1} = \frac{h_{fe}(typ) \times R_{L_1}}{h_{ie}}$$

$$R_{L_1} = R_{C_1}||R_3||R_4||h_{ie} = R_{C_1}||15k||2.7k||2.7k = R_{C_1}||1.2385k$$

$$\therefore 30 = \frac{220 \times R_{C_1} \times 1.2385k}{2.7k \times (R_{C_1} + 1.2385k)}$$

$$\therefore 368.1818 = \frac{R_{C_1} \times 1.2385k}{R_{C_1} + 1.2385k}$$

$$\therefore R_{C_1} = 523.9349$$

Selecting HSV, $R_{C_1} = 560\Omega$, 1/4 W

Step 10: Calculation of $\mathbf{R_{E_1}}$

$V_{CEQ_1} = V_{CEQ_2} = 5.5$ V

$V_{RE_1} = V_{RE_2} = 1.1$ V

$V_{RC_1} = V_{RC_2}, \therefore I_{CQ_1} \times R_{C_1} = I_{CQ_2} \times R_{C_2}$

$$I_{CQ_1} = \frac{I_{CQ_2} \times R_{C_2}}{R_1} = \frac{4.6 \times 10^{-3} \times 750}{560}$$

$\therefore I_{CQ_1} = 6.1607$ mA

$$I_{BQ_1} = \frac{I_{CQ_1}}{\beta} = 34.226\ \mu\text{A}$$

$I_{EQ_1} = I_{CQ} + I_{BQ} = 6.1949$ mA

$V_{RE_1} = I_{EQ_1} \times R_{E_1} = 1.1$ V

$$R_{E_1} = \frac{V_{RE_1}}{I_{EQ_1}} = \frac{1.1}{6.1949 \times 10^{-3}} = 177.565\Omega$$

Selecting LSV, $R_{E_1} = 150\Omega$, 1/4 W

$V_{E_1} = I_{EQ_1} \times R_{E_1} = 0.929$ V

Step 11: Calculation of biasing resistors $\mathbf{R_1}$ and $\mathbf{R_2}$:

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_{E_1}}{R_{B_1}+R_{E_1}}\right)}$$

$R_{B_1} = R_1 || R_2$

$\beta = h_{FE}(typ) = 180$

$$10 = \frac{181}{1+180\left(\frac{150}{150+R_{B_1}}\right)}$$

$R_{B_1} = 1.4289$ kΩ

$$R_{B_1} = \frac{R_1 \times R_2}{R_1 + R_2} = 1.4289k \qquad \text{.....(4)}$$

$$V_{th_1} = V_{B_1} = \frac{R_2}{R_1 + R_2} \times 11 \qquad \text{.....(5)}$$

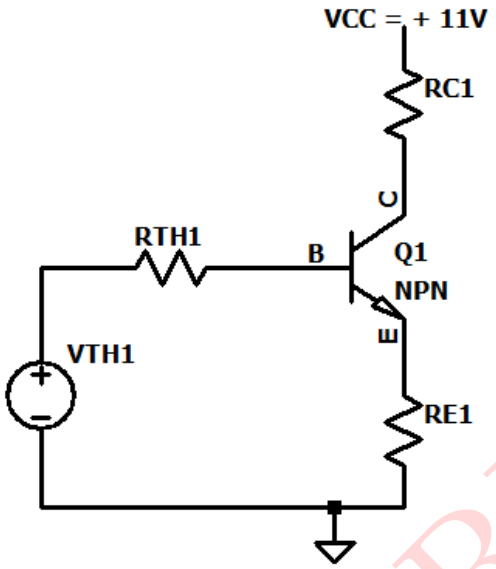

Figure 3: DC equivalent circuit for stage 1

Applying KVL at B-E loop of Q_1

$$V_{B_1} - V_{BE_1} - I_{BQ_1}R_{B_1} - I_{EQ_1}R_{E_1} = 0$$

$$V_{B_1} = V_{BE_1} + \frac{I_{CQ_1}}{\beta}R_{B_1} + I_{CQ_1}R_{E_1}$$

$$V_{B_1} = 0.7 + \frac{6.1607 \times 10^{-3}}{180} \times 1.4289k + (6.1607 \times 10^{-3} \times 150)$$

$$\therefore V_{B_1} = 1.673 \text{ V}$$

From equation (5), $\frac{R_2}{R_1 + R_2} \times 11 = 1.673$

$$\therefore \frac{R_2}{R_1 + R_2} = 0.15209 \qquad \text{.....(6)}$$

Put equation (6) in equation (4), we get,

$$R_1 \times 0.15209 = 1.4289k$$

$$\therefore R_1 = 9.395 \text{ k}\Omega$$

Selecting HSV, $R_1 = 10$ kΩ, 1/4 W

From equation (6), $\frac{R_2}{10k + R_2} = 0.15209$

$$\therefore R_2 = 1.7937 \text{ k}\Omega$$

Selecting LSV, $R_2 = 1.5$ kΩ, 1/4 W

Step 12: Calculation of coupling capacitors:
a) Calculation of C_{C1}:

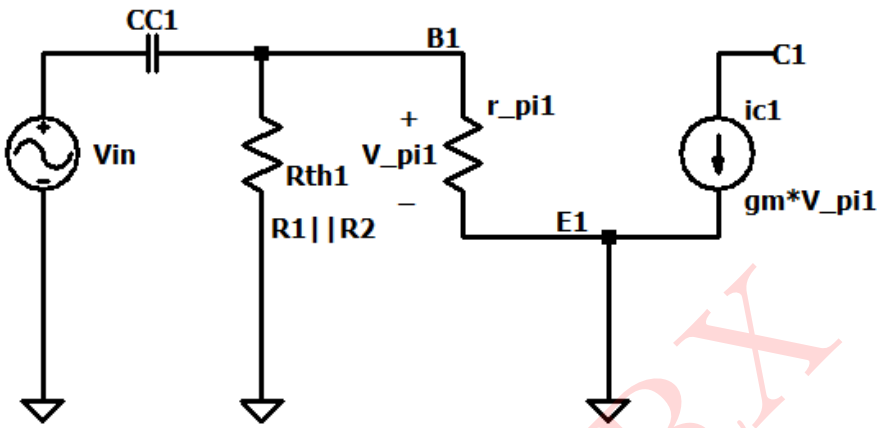

Figure 4: Small-signal equivalent for C_{C1}

$$C_{C1} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = R_1||R_2||h_{ie} = 10k||1.5k||2.7k$$

$$\therefore R_{eq} = 879.32\Omega$$

$$C_{C1} = \frac{1}{2\pi \times 879.32 \times 25} = 7.2399\ \mu\text{F}$$

Selecting HSV, $C_{C1} = 7.5\ \mu$F, 25 V

b) Calculation of C_{C2}:

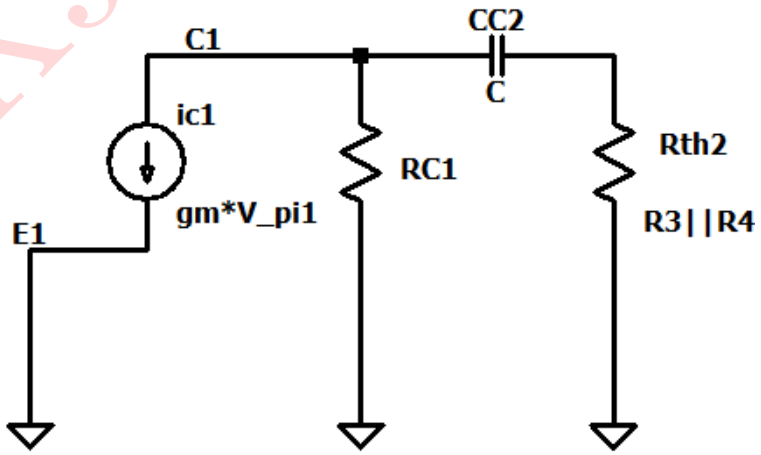

Figure 5: Small-signal equivalent for C_{C2}

$$C_{C2} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = R_{C_1} + (R_3||R_4||h_{ie}) = 560 + (15k||2.7k||2.7k)$$

$$R_{eq} = 1.7985 \text{ k}\Omega$$

$$C_{C2} = \frac{1}{2\pi \times 1.7985k \times 25} = 3.5397 \ \mu\text{F}$$

Selecting HSV, $C_{C2} = 3.9 \ \mu\text{F}/25$ V

b) Calculation of C_{C3}:

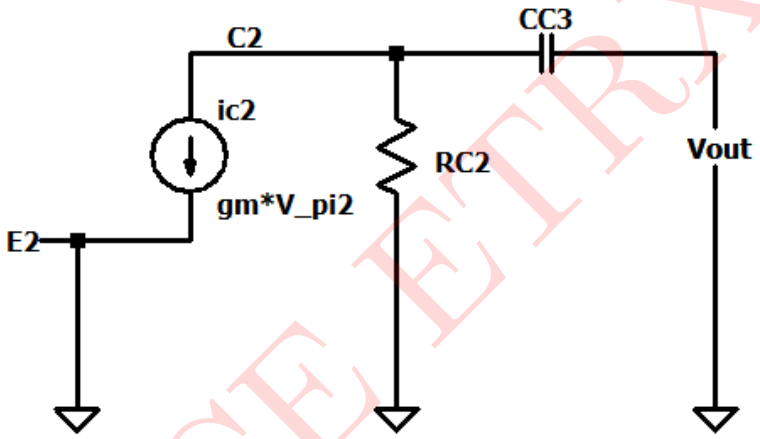

Figure 6: Small-signal equivalent for C_{C3}

$$C_{C3} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = R_{C_2} = 750\Omega$$

$$C_{C_3} = \frac{1}{2\pi \times 750 \times 25} = 8.488 \ \mu\text{F}$$

Selecting HSV, $C_{C3} = 9.1 \ \mu\text{F}$ / 25 V

Step 13: Calculation of bypass capacitors C_{E_1} and C_{E_2}:
a) Calculation of C_{E_1}:
$X_{CE_1} = 0.1R_{E_1}$

$$\frac{1}{2\pi f_L C_{E_1}} = 0.1R_{E_1}$$

$$\therefore C_{E_1} = \frac{1}{2\pi f_L \times 0.1 \times R_{E_1}} = \frac{1}{2\pi \times 25 \times 0.1 \times 150} = 424.4 \ \mu\text{F}$$

Selecting HSV, $C_{E_1} = 470 \ \mu\text{F}$ / 25 V

b) Calculation of C_{E_2}:
$X_{CE_2} = 0.1R_{E_2}$

$$\frac{1}{2\pi f_L C_{E_2}} = 0.1R_{E_2}$$

$$\therefore C_{E_2} = \frac{1}{2\pi f_L \times 0.1 \times R_{E_2}} = \frac{1}{2\pi \times 25 \times 0.1 \times 220} = 289.37\ \mu\text{F}$$

Selecting HSV, $C_{E_1} = 330\ \mu$F / 25 V

Step 14: Complete designed cicruit:

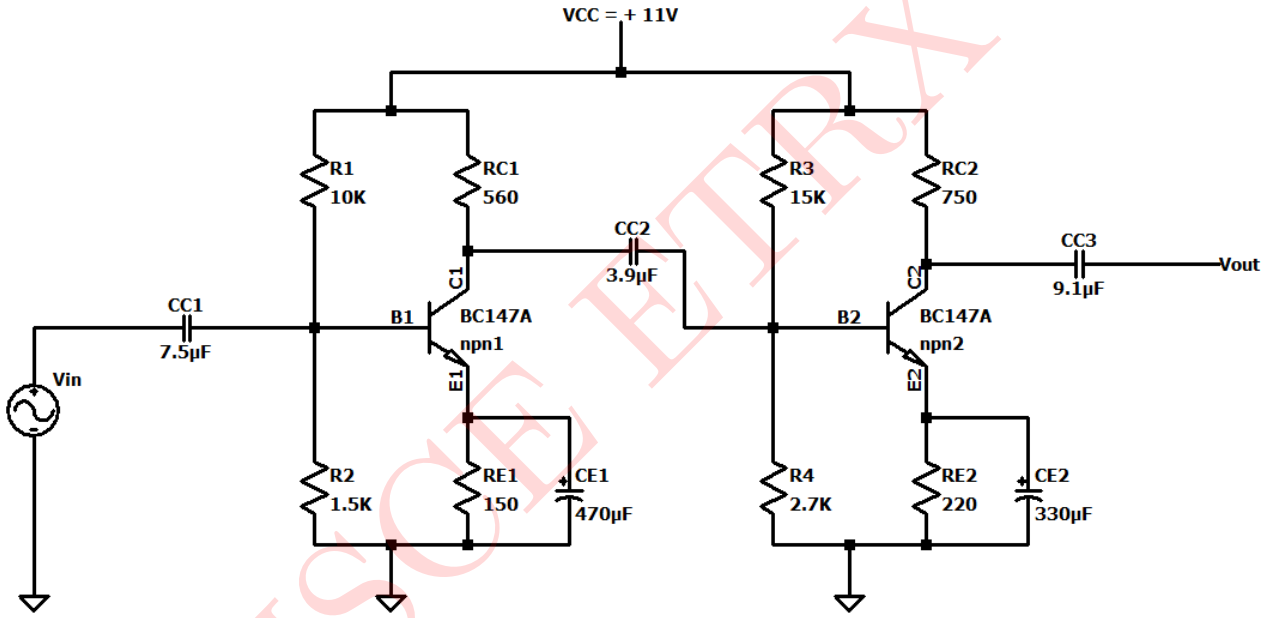

Figure 7: Designed circuit

Small-signal parameters:

$$r_{\pi_1} = \frac{\beta_1 V_T}{I_{C_1}} = 759.65\Omega$$

$$r_{\pi_2} = \frac{\beta_2 V_T}{I_{C_2}} = 101739\ \text{k}\Omega$$

$$g_{m_1} = \frac{I_{C_1}}{V_T} = \frac{6.1607 \times 10^{-3}}{26 \times 10^{-3}} = 236.95\ \text{mA/V}$$

$$g_{m_2} = \frac{I_{C_2}}{V_T} = \frac{4.6 \times 10^{-3}}{26 \times 10^{-3}} = 176.9\ \text{mA/V}$$

The mid-band AC equivalent circuit is shown in Figure 8

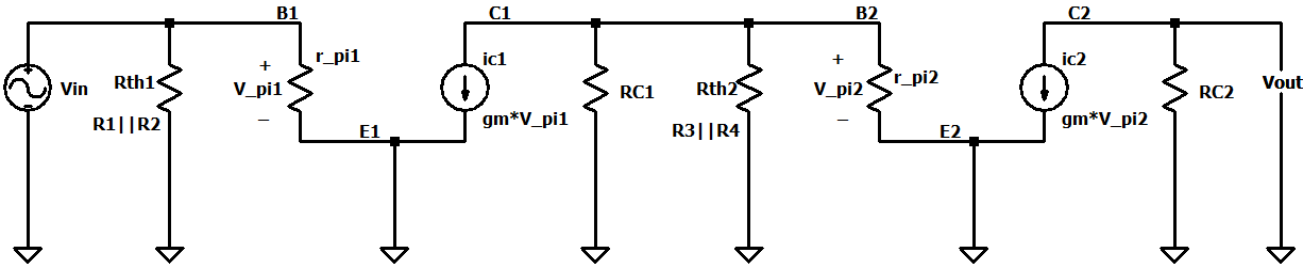

Figure 8: Mid frequency equivalent circuit

Input impedance $Z_i = R_{th}||r_{\pi_1} = 1.3k||759.65$

$\therefore Z_i = \mathbf{479.47\Omega}$

Output impedance $Z_o = R_{C_2} = \mathbf{750\Omega}$

$$A_{V_1} = \frac{V_1}{V_{in}} = \frac{-g_{m_1} V_{\pi_1} (R_{C_1}||R_3||R_4||r_{\pi_2})}{V_{\pi_1}}$$

$$A_{V_1} = -g_{m_1}(R_{C_1}||R_3||R_4||r_{\pi_2}) = (236.95 \times 10^{-3})||(560||15k||2.7k||1.01739k)$$

$\therefore A_{V_1} = -73.9155$

$$A_{V_2} = \frac{-g_{m_2} V_{\pi_2} R_{C_2}}{V_{\pi_2}} = -g_{m_2} R_{C_2}$$

$\therefore A_{V_2} = -176.9 \times 10^{-3} \times 750 = -132.675$

$A_{V_T} = A_{V_1} \times A_{V_2} = -73.9155 \times -132.675 = 9806.7389$

$|A_{V_T}|$ (in dB) $= 20log_{10}A_{V_T} = 20log(9806.7389)$

$\therefore |A_{V_T}|$ (in dB) $= \mathbf{79.83049\ dB}$

SIMULATED RESULTS:

Above circuit is simulated using LTspice and the results are presented below:

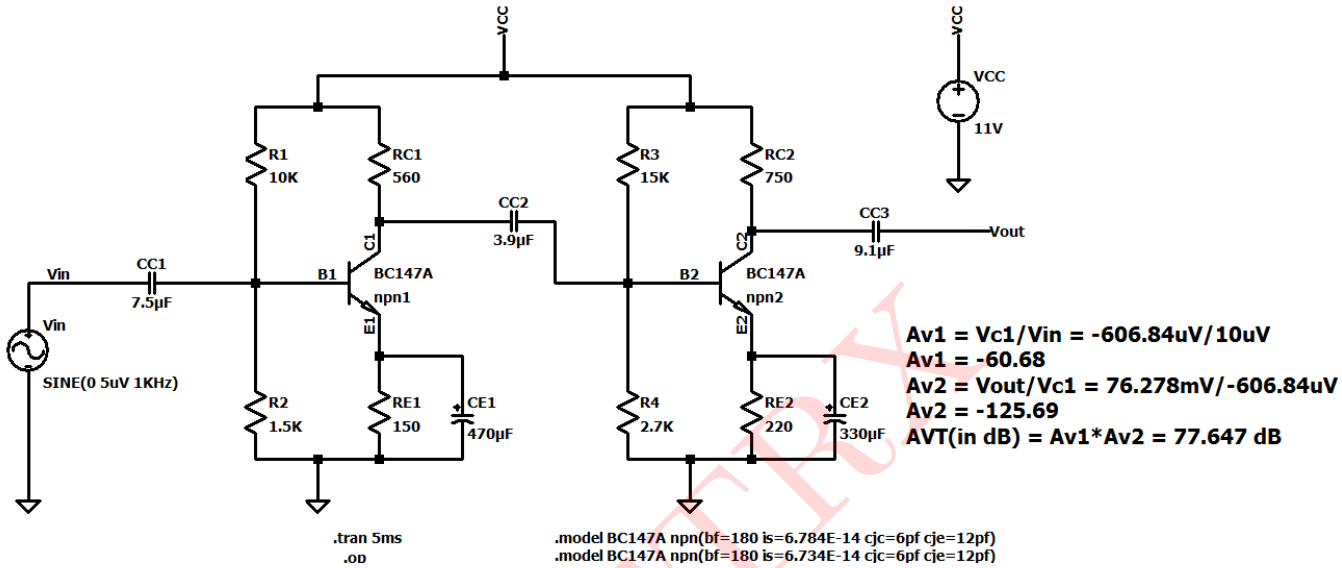

Figure 9: Circuit schematic

The input and output waveforms for voltage gain A_{V_1} are shown in Figure 10

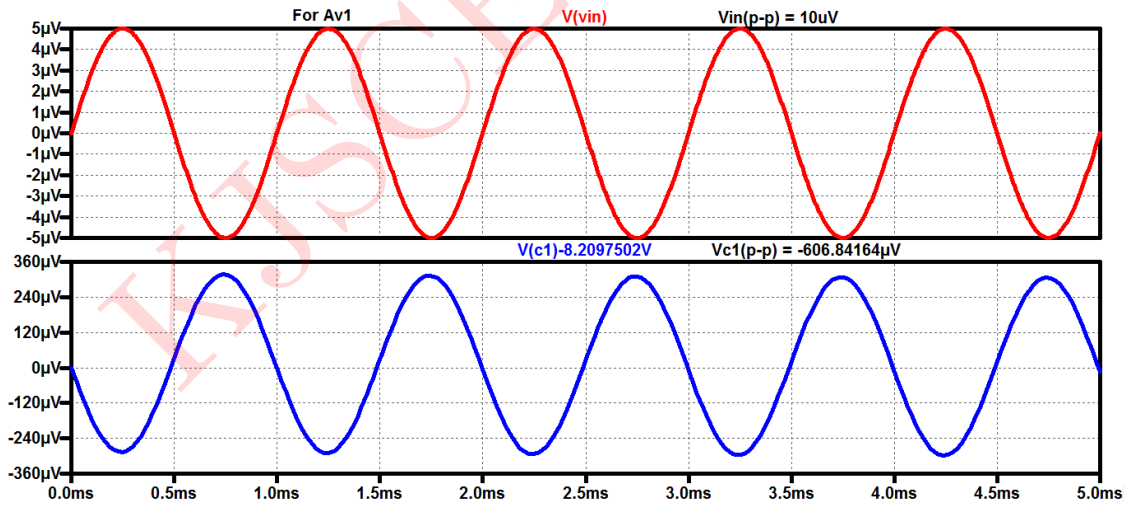

Figure 10: Input and output waveforms for voltage gain A_{V_1}

The input and output waveforms for voltage gain A_{V_2} are shown in Figure 11

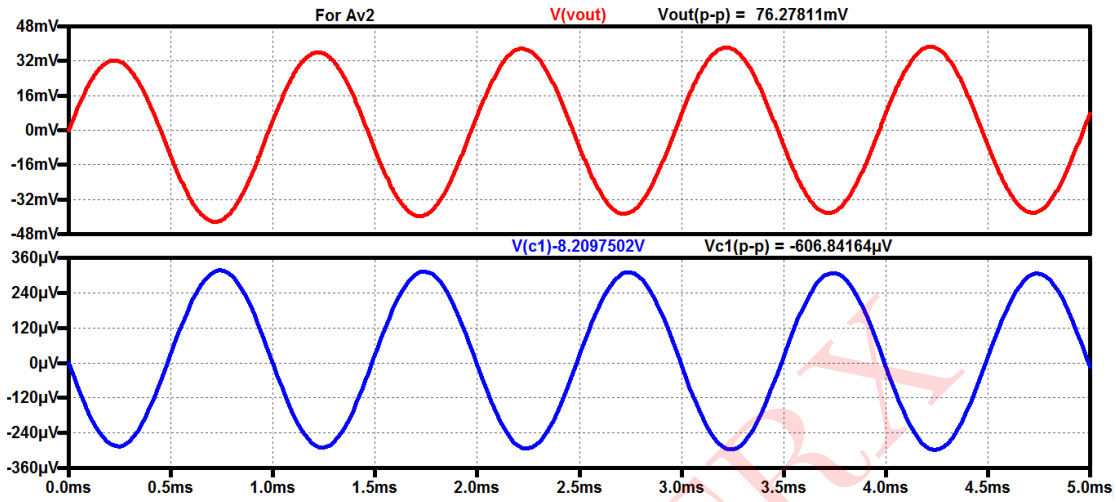

Figure 11: Input and output waveforms for voltage gain A_{V_2}

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
I_{B_1}	34.226 μA	29.68 μA
I_{C_1}	6.1607 mA	4.98259 mA
I_{E_1}	6.1949 mA	5.01027 mA
V_{E_1}	0.929 V	0.75154 V
V_{B_1}	1.673 V	1.39868 V
I_{B_2}	25.556 μA	24.5497 μA
I_{C_2}	4.6 mA	4.41895 mA
I_{E_2}	4.62556 mA	4.4435 mA
V_{E_2}	1.0176 V	0.97757 V
V_{B_2}	1.712 V	1.62179 V
Voltage gain of 1^{st} stage (A_{V_1})	-73.9955	-60.68
Voltage gain of 2^{nd} stage (A_{V_2})	-132.675	-125.69
Overall voltage gain A_{V_T}	79.83 dB	77.647 dB
Input impedance of 1^{st} stage	479.47 Ω	–
Output impedance of 2^{nd} stage	750 Ω	–

Table 1: Numerical 1

2. Design a two stage RC coupled cascade amplifier for the following specifications:
$A_V \geq 500$, $V_{CC} = 16$ V, $S \leq 10$ and $R_i \geq 1$ MΩ
Select a suitable transistor from data-sheet

Solution: Above requirements can be fulfilled by CS-CE stage. We select CS as 1^{st} stage since $R_i \geq 1$ MΩ
Step 1: Circuit diagram

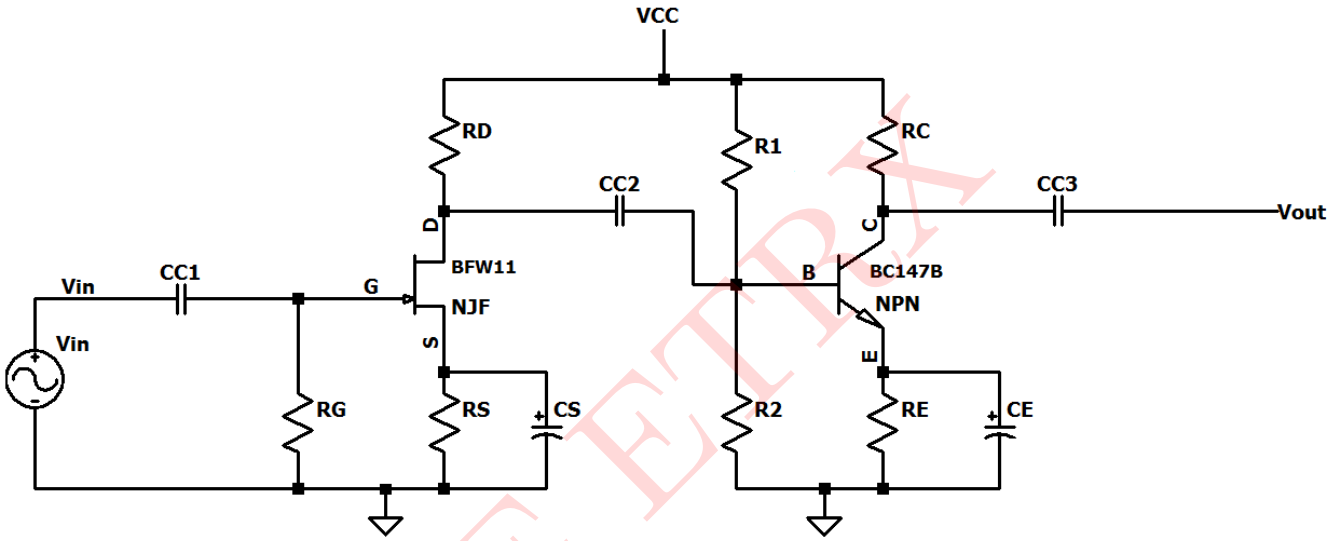

Figure 12: Circuit diagram and selection of transistor

Select BC147B:
$h_{fe}(typ) = 330$
$h_{FE}(typ) = \beta = 290$
$h_{ie} = 4.5$ kΩ
$V_{CE}(sat) = 0.25$ V

Select BFW11:
$I_{DSS} = 7$ mA
$V_P = -2.5$ V
$g_{m_o} = 5400\ \mu/\Omega$
$r_d = 50$ kΩ

Step 2: Selection of gains:
$A_V \geq 500$

Let $A_{V_1} = 4$ (since gain of JFET amplifier is less)

$$\therefore A_{V_2} = \frac{500}{4} = 125$$

Design of 2nd stage

Step 3: Selection of $\mathbf{R_C}$

$$|A_{V_2}| = \frac{h_{fe}(typ) \times R_C}{h_{ie}}$$

$$\therefore 125 = \frac{330 \times R_C}{4.5k}$$

$$\therefore R_C = 1.7045 \text{ k}\Omega$$

Selecting HSV, $R_C = 1.8$ kΩ, 1/4 W

Step 4: Selection of Q-point ($\mathbf{V_{CEQ}}, \mathbf{I_{CQ}}$)

$V_{CC} = 16$ V

Let $V_{CEQ} = \frac{V_{CC}}{2} = 8$ V

$V_{RE} = 0.1 \times V_{CC} = 1.6$ V

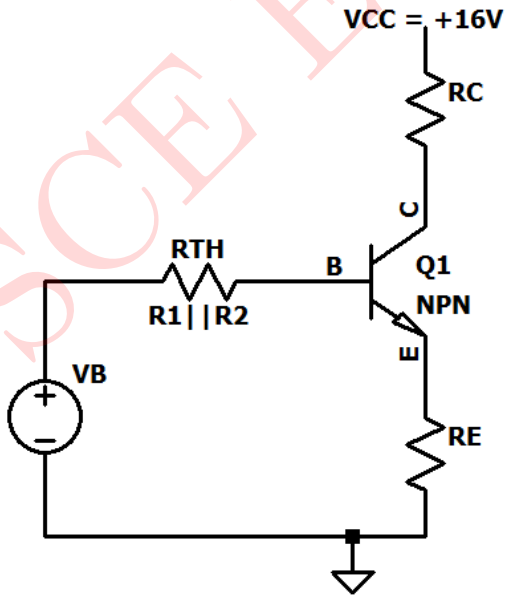

Figure 13: DC equivalent circuit for BJT

Applying KVL to C-E loop of BJT

$$V_{CC} - V_{R_C} - V_{CEQ} - V_{R_E} = 0$$

$$\therefore V_{R_C} = V_{CC} - V_{CEQ} - V_{R_E} = 16 - 8 - 1.6$$

$$\therefore V_{R_C} = 6.4 \text{ V}$$

$$I_{CQ} = \frac{V_{R_C}}{R_C} = \frac{6.4}{1.8k} = 3.556 \text{ mA}$$

Step 5: Selection of R_E

$$R_E = \frac{V_{R_E}}{I_{CQ}} = \frac{1.6}{3.556 \times 10^{-3}} = 449.94\ \Omega$$

Selecting LSV, $R_E = 420\ \Omega$, 1/4 W

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{3.556 \times 10^{-3}}{290} = 12.26\ \mu\text{A}$$

$$I_{EQ} = I_{BQ} + I_{CQ} = 3.568\ \text{mA}$$

Step 6: Selection of biasing resistors R_1 and R_2

$S \leq 10$

Let $S = 9$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B+R_E}\right)}$$

$$9 = \frac{1+290}{1+290\left(\frac{420}{R_B+420}\right)}$$

$$\therefore R_B = 3.9145\ \text{k}\Omega$$

$$R_B = R_1||R_2 = \frac{R_1 \times R_2}{R_1+R_2} = 3.46889\ \text{k}\Omega \qquad \text{.....(1)}$$

$$V_B = V_{th} = \frac{R_2}{R_1+R_2} \times V_{CC} \qquad \text{.....(2)}$$

Applying KVL at B-E loop of BJT:

$$V_B - I_{BQ}R_B - V_{BE} - I_{EQ}R_E = 0$$

$$V_B = \frac{I_{CQ} \times R_B}{\beta} + V_{BE} + I_{CQ}R_E$$

$$\therefore V_B = \frac{3.556 \times 10^{-3} \times 3.4689k}{290} + 0.7 + (3.556 \times 10^{-3} \times 420)$$

$$\therefore V_B = 2.236\ \text{V}$$

From equation (2), $V_B = 2.236 = \frac{R_2}{R_1+R_2} \times V_{CC} \therefore \frac{R_2}{R_1+R_2} = 0.13975$ .....(2)

$$V_E = I_{EQ} \times R_E = 3.568 \times 10^{-3} \times 420 = 1.4985\ \text{V}$$

Put (3) in (1)

$$R_1 \times 0.13975 = 3.4689k$$

$$\therefore R_1 = 24.822\ \text{k}\Omega$$

Selecting HSV, $R_1 = 27\ \text{k}\Omega$, 1/4 W

From equation (3), $\frac{R_2}{27k + R_2} = 0.13975$

$\therefore R_2 = 4.386$ kΩ

Selecting HSV (only for CS-CE case), $R_2 = 4.7$ kΩ, 1/4 W

Design of 1st stage

Step 7: Selection of Q-point ($\mathbf{I_{DQ}}, \mathbf{I_{GSQ}}$)

Using mid-point biasing, $I_{DQ} = \frac{I_{DSS}}{2} = \frac{7 \times 10^{-3}}{2} = 3.5$ mA

$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

We get, $V_{GSQ} = -0.732$ V

$g_{m_1} = g_{m_o} \times \left(1 - \frac{V_{GSQ}}{V_P}\right) = 5600 \times 10^{-6} \times \left(1 - \frac{-0.732}{-2.5}\right)$

$\therefore g_{m_1} = 3.96$ mA/V

Step 8: Selection $\mathbf{R_D}$

$|A_{V_2}| = \frac{h_{fe}(typ) \times R_C}{h_{ie}} = \frac{330 \times 1.8k}{4.5k} = 132$

$|A_{V_1}| = g_m[R_D||r_d||R_1||R_2||h_{ie}]$

$R_{L_1} = r_d||R_1||R_2||h_{ie} = 50k||27k||4.7k||4.5k$

$\therefore R_{L_1} = 2.03166$ kΩ

$|A_{V_1}| = g_m[R_D||2.216k]$

$\therefore 3.8 = 3.96 \times 10^{-3} \times \frac{R_D \times 2.03166k}{R_D + 2.03166k}$

$\therefore R_D = 1.818$ kΩ

Selecting HSV, $R_D = 2.2$ kΩ, 1/4 W

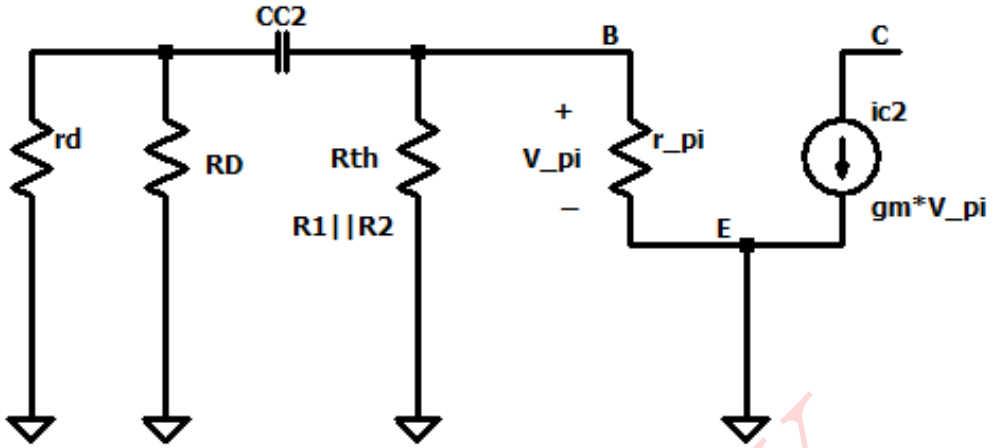

Figure 14: Small-signal equivalent circuit for selection of R_D

Step 9: Selection of $\mathbf{R_S}$

$V_{GSQ} = -I_{DQ} \times R_S$

$\therefore -0.732 = -3.5 \times 10^{-3} \times R_S$

$\therefore R_S = 209.14\Omega$

Selecting LSV, $R_S = 180\Omega$, 1/4 W

Step 10: Selection of $\mathbf{R_G}$

Since $R_1 = 1$ MΩ, to prevent loading we take $R_G \geq 1$ MΩ

Let $R_G = 1.2$ MΩ, 1/4 W

Step 11: Selection of coupling capacitors C_{C1}, C_{C2} and C_{C3}

a) Calculation of C_{C1}:

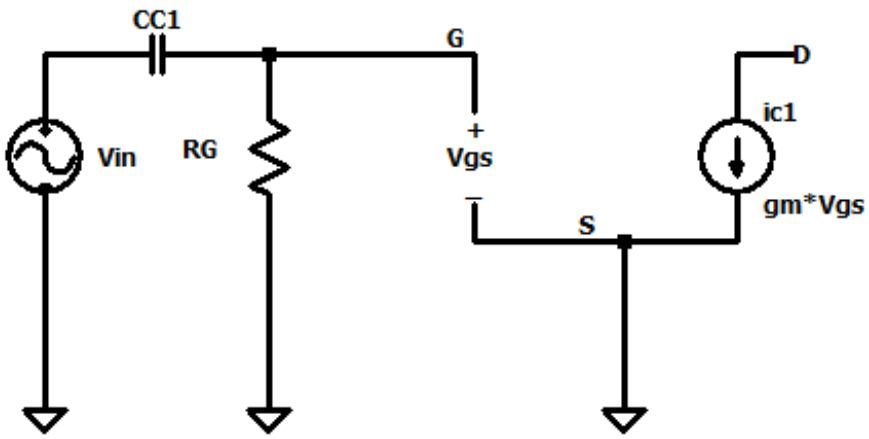

Figure 15: Small-signal equivalent for C_{C1}

Since f_L is not given, we consider audio frequency $f_L = 20$ Hz

$$C_{C1} = \frac{1}{2\pi R_G f_L}$$

$$C_{C1} = \frac{1}{2\pi \times 1.2 \times 10^6 \times 20} = 6.63 \text{ nF}$$

Selecting HSV, $C_{C1} = 6.8$ nF, 50 V

b) Calculation of C_{C2}:

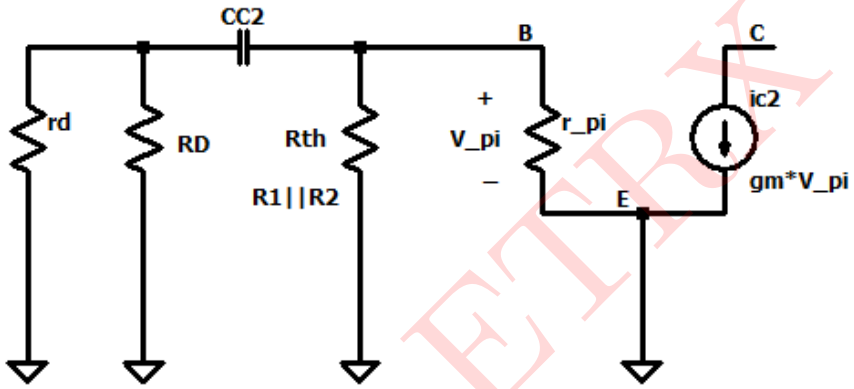

Figure 16: Small-signal equivalent for C_{C2}

$$C_{C2} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = (r_d||R_D) + (R_1||R_2||h_{ie}) = 2.107k + 2.11848k$$

$$R_{eq} = 4.22548 \text{ k}\Omega$$

$$C_{C2} = \frac{1}{2\pi \times 4.22548k \times 20} = 1.88327 \ \mu\text{F}$$

Selecting HSV, $C_{C2} = 2.2$ μF/50 V

b) Calculation of C_{C3}:

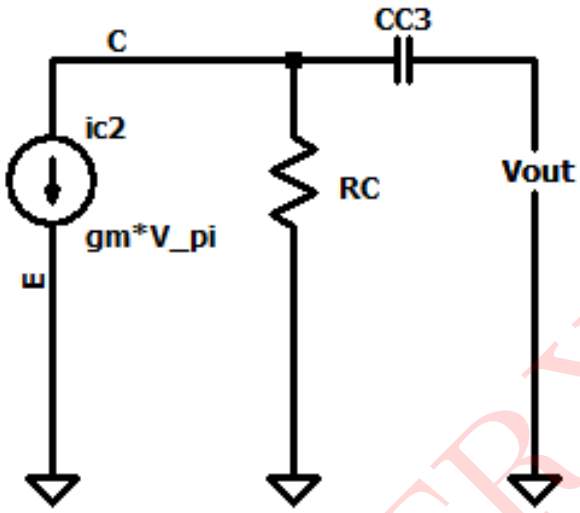

Figure 17: Small-signal equivalent for C_{C3}

$$C_{C3} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = R_C = 1.8 \text{ k}\Omega$$

$$C_{C_3} = \frac{1}{2\pi \times 1.8k \times 20} = 4.42 \ \mu\text{F}$$

Selecting HSV, $C_{C3} = 4.7 \ \mu\text{F}$ / 50 V

Step 12: Calculation of bypass capacitors C_{E_1} and C_{E_2}:

a) Calculation of C_S:

$$C_S = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = \left(\frac{1}{g_m} || R_S\right) = \left(\frac{1}{3.96 \times 10^{-3}}\right) || 180$$

$$\therefore R_{eq} = 105.09 \ \Omega$$

$$C_S = \frac{1}{2\pi \times 105.09 \times 20} = 75.72 \ \mu\text{F}$$

b) Calculation of C_E:

$X_{CE} = 0.1 R_E$

$$\therefore C_E = \frac{1}{2\pi f_L \times 0.1 \times R_E} = \frac{1}{2\pi \times 20 \times 0.1 \times 420} = 189.47 \ \mu\text{F}$$

Selecting HSV, $C_E = 220 \ \mu\text{F}$ / 50 V

Step 13: Small-signal analysis

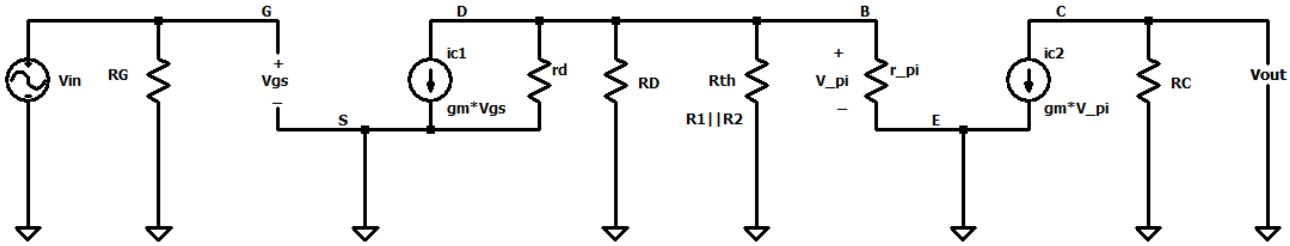

Figure 18: Small-signal equivalent circuit

$$Z_i = R_G = 1.2 \text{ M}\Omega$$

$$Z_o = R_C = 1.8 \text{ k}\Omega$$

$$g_{m_2} = \frac{I_{CQ}}{V_T} = \frac{3.556 \times 10^{-3}}{26 \times 10^{-3}}$$

$$\therefore g_{m_2} = 136.769 \text{ mA/V}$$

$$A_{V_1} = \frac{V_1}{V_{in}}$$

$$A_{V_2} = \frac{V_{out}}{V_1}$$

$$A_{V_T} = A_{V_1} \times A_{V_2}$$

$$A_{V_2} = \frac{-g_{m_2} V_\pi R_C}{V_\pi} = -g_{m_2} R_C$$

$$\therefore A_{V_2} = -136.769 \times 10^{-3} \times 1.8k = -246.184$$

$$A_{V_1} = \frac{-g_{m_1} V_{gs} (r_d || R_D || R_{th} || r_\pi)}{V_{gs}} = -g_{m_1} (r_d || R_D || R_{th} || r_\pi)$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{290 \times 26 \times 10^{-3}}{3.556 \times 10^{-3}} = 2.120359 \text{ k}\Omega$$

$$A_{V_1} = -3.96 \times 10^{-3} (50k || 2.2k || 27k || 4.7k || 2.123059k)$$

$$\therefore A_{V_1} = -3.3119889$$

$$A_{V_T} = A_{V_1} \times A_{V_2} = -3.3119889 \times -246.184 = 815.358$$

$$|A_{V_T}| \text{ (in dB)} = 20 log A_{V_T} = 20 log(815.358)$$

$$\therefore |A_{V_T}| \text{ (in dB)} = \mathbf{58.226 \text{ dB}}$$

Step 14: Complete designed cicruit:

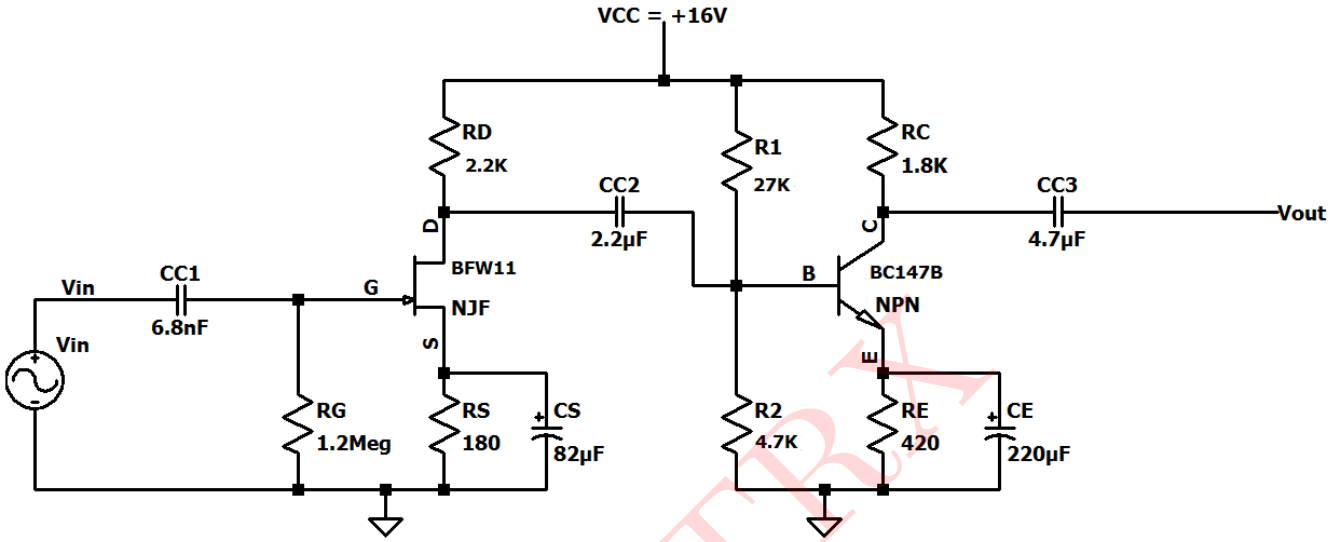

Figure 19: Designed circuit

SIMULATED RESULTS:

Above circuit is simulated using LTspice and the results are presented below:

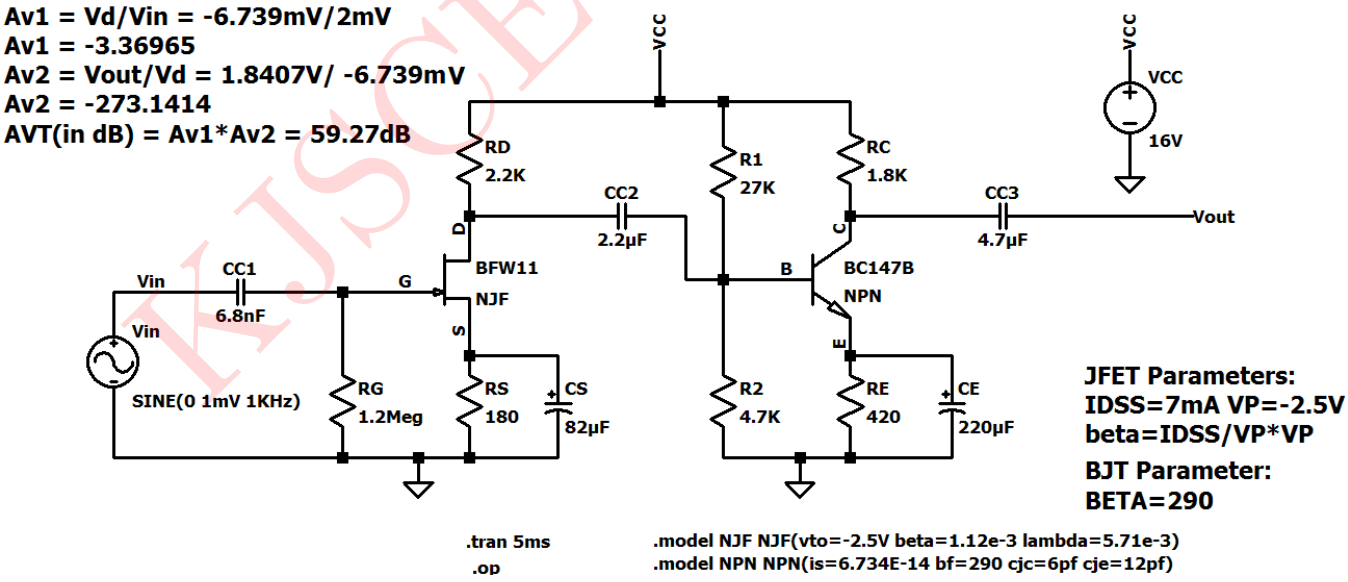

Figure 20: Circuit schematic

The input and output waveforms for voltage gain A_{V_1} are shown in Figure 21

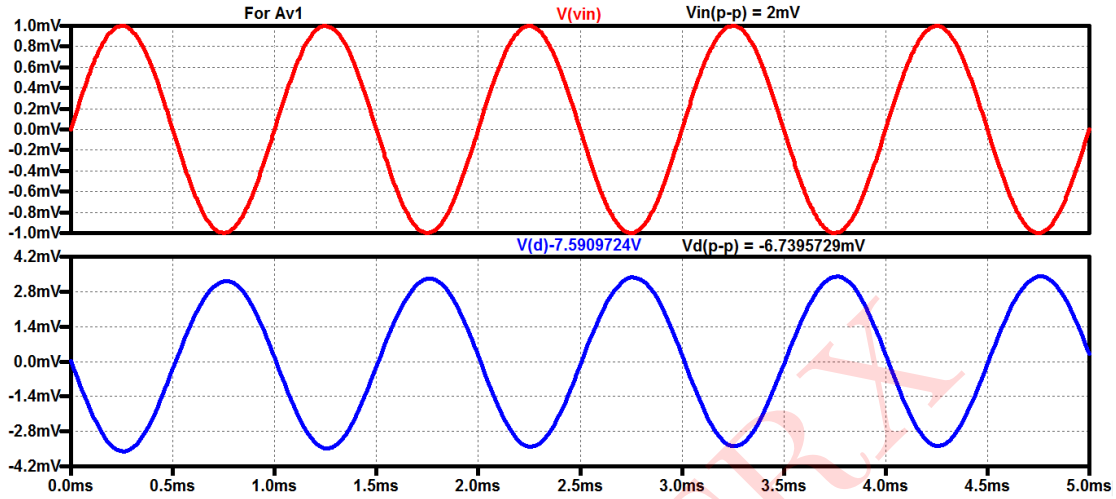

Figure 21: Input and output waveforms for voltage gain A_{V_1}

The input and output waveforms for voltage gain A_{V_2} are shown in Figure 22

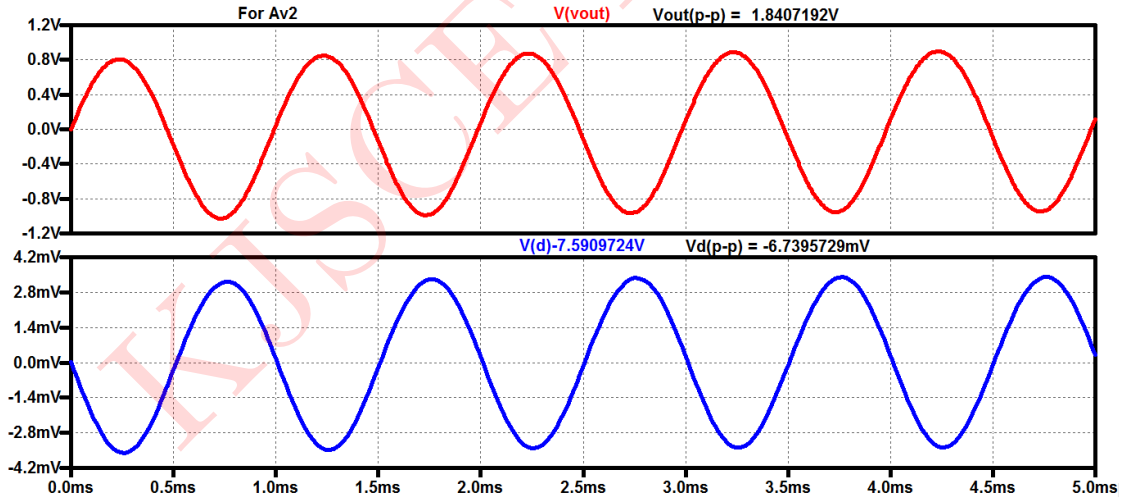

Figure 22: Input and output waveforms for voltage gain A_{V_2}

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
I_{DQ}	3.5 mA	3.82229 mA
V_{GSQ}	−0.732 V	−0.688 V
I_C	3.556 mA	3.97642 mA
I_B	12.26 μA	13.7118 μA
I_E	3.568 mA	3.9903 mA
V_E	1.4985 V	1.67586 V
V_B	2.236 V	2.31735 V
Voltage gain of 1^{st} stage (A_{V_1})	−3.311988	−3.36965
Voltage gain of 2^{nd} stage (A_{V_2})	−246.184	−273.1414
Overall voltage gain A_{V_T}	58.2269 dB	59.27 dB
Input impedance of 1^{st} stage	1.2 MΩ	–
Output impedance of 2^{nd} stage	1.8 kΩ	–

Table 2: Numerical 2