K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
DC Biasing Circuits

1. Analyse the circuit shown in Figure 1 using a voltage divider bias and determine the change in the Q-point with variations in β when the circuit contains an emitter resistor. For the circuit given in Figure1, R1 = 56kΩ, R2 = 12.2kΩ, R_C = 2kΩ, R_E = 0.4kΩ, $C_C = 1\mu F$, V_{CC} = 10V, $V_{BE_{(ON)}}$ = 0.7V and β = 100

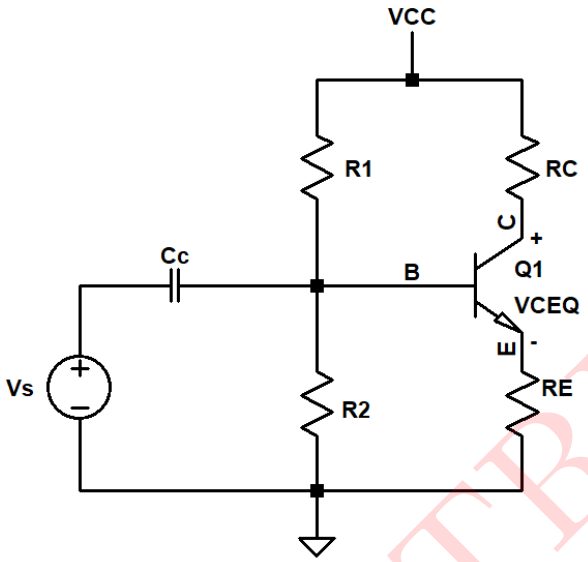


Figure 1: Circuit Diagram

Solution: Figure 1 is a voltage divider bias circuit.
To find Q-point, all the capacitors are open circuited.
Using Thevenins's equivalent circuit (refer Figure 2), we have:

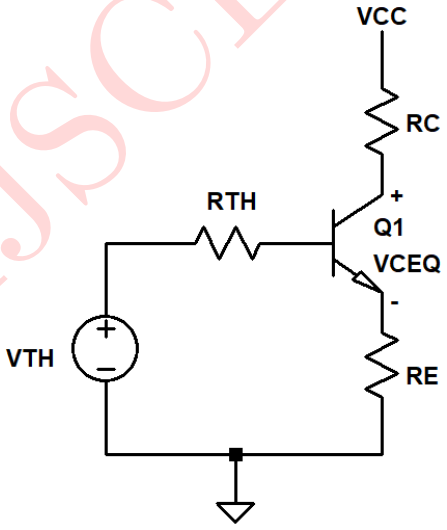


Figure 2: Thevenin's Equivalent circuit

$$R_{TH} = R_1 \parallel R_2 = 56\text{k}\Omega \parallel 12.2\text{k}\Omega = 10\text{k}\Omega$$

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{12.2k\Omega}{56k\Omega + 12.2k\Omega}\right)(10) = 1.79\text{V}$$

Applying KVL to B-E loop, we obtain:

$$I_{BQ} = \frac{V_{TH} - V_{BE_{(ON)}}}{R_{TH} + (1+\beta)R_E} = \frac{1.79 - 0.7}{10k\Omega + (101)(0.4k\Omega)} = 21.6\mu\text{A}$$

The collector current is: $I_{CQ} = \beta I_{BQ} = (100)(21.6)\mu\text{A}$

$\therefore I_{CQ} = 2.16\text{mA}$

Apply KVL to C-E loop,

$V_{CEQ} = V_{CC} - I_{CQ}R_C$ - $I_{EQ}R_E$ = 10 - (2.16mA)(2kΩ) - (2.18mA)(0.4kΩ)

$V_{CEQ} = 4.81\text{V}$

Above results show that, the transistor is biased in the active region.

Since, $V_{CE} > V_{BE_{(ON)}}$

Similarly, if we increase the β value of the transistor to 150 or decrease β to 50, by repeating above steps we get the following results:

β	50	100	150
	$I_{BQ} = 35.9\mu\text{A}$	$I_{BQ} = 21.6\mu\text{A}$	$I_{BQ} = 15.5\mu\text{A}$
	$I_{CQ} = 1.80\text{mA}$	$I_{CQ} = 2.16\text{mA}$	$I_{CQ} = 2.32\text{mA}$
	$V_{CEQ} = 5.67\text{V}$	$V_{CEQ} = 4.81\text{V}$	$V_{CEQ} = 4.40\text{V}$

Table 1: Variance of β

SIMULATED RESULTS:

Above circuit was simulated in LTspice and results obtained are:

Case 1: $\beta = 50$

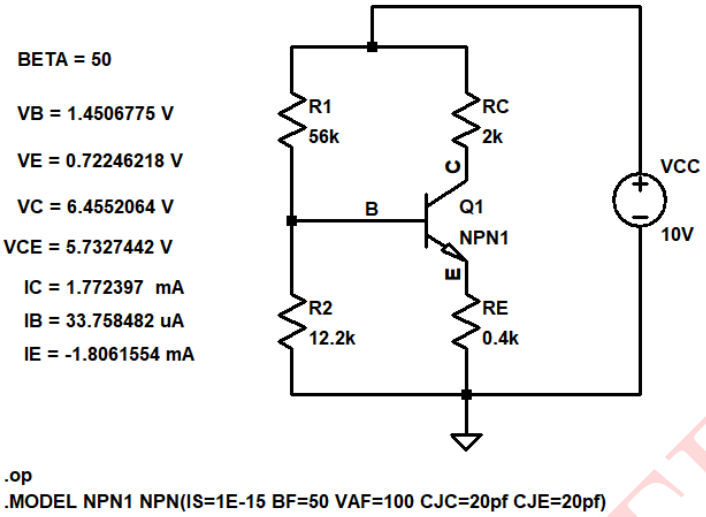


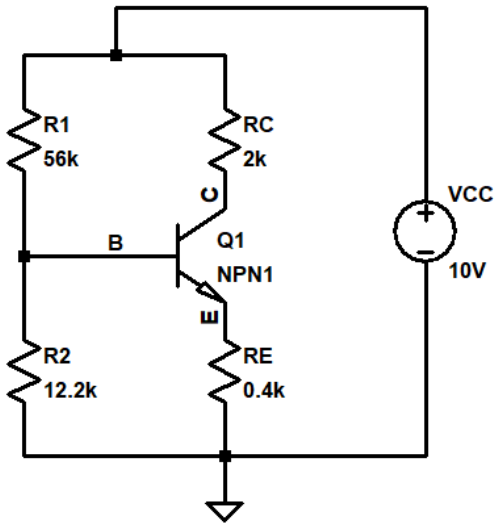
Figure 3: Circuit Schematic: Results for $\beta = 50$

Comparison between theoretical and simulated values:

Parameter	Theoretical	Simulated
I_{CQ}	1.800mA	1.772mA
I_{BQ}	35.90μA	33.758μA
V_{CEQ}	5.682V	5.733V

Table 2: Question 1

Case 2: $\beta = 100$:

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.op
.MODEL NPN1 NPN(IS=1E-15 BF=100 VAF=100 CJC=20pf CJE=20pf)
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Figure 4: Circuit Schematic: Results for $\beta = 100$

Comparison between theoretical and simulated values:

Parameter	Theoretical	Simulated
I_{CQ}	2.16mA	2.112mA
I_{BQ}	21.6μA	20.27μA
V_{CEQ}	4.81V	4.923V

Table 3: Question 1

Case 3: $\beta = 150$

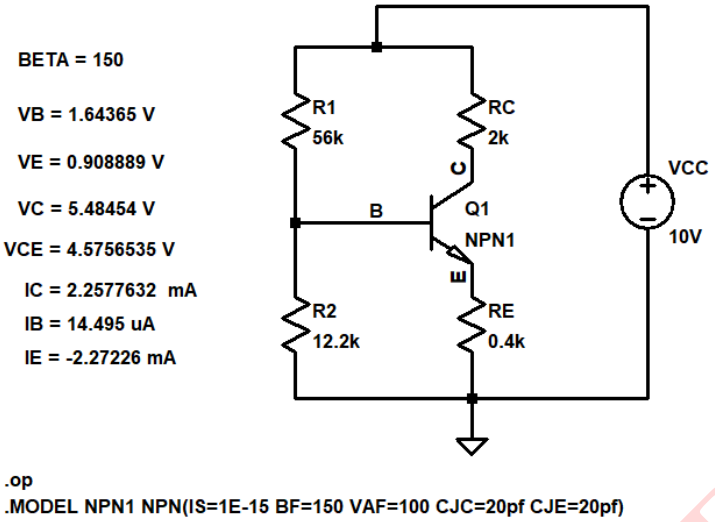

Figure 5: Circuit Schematic: Results for $\beta = 150$

Comparsion between theoretical and simulated values:

Parameter	Theoretical	Simulated
I_{CQ}	2.325mA	2.258mA
I_{BQ}	15.50μA	14.495μA
V_{CEQ}	4.414V	4.576V

Table 4: Question 1

2. Find the Q-point and V_{DS} for circuit shown in figure 6:
(I_{DSS} = 10mA, V_P = -4V)

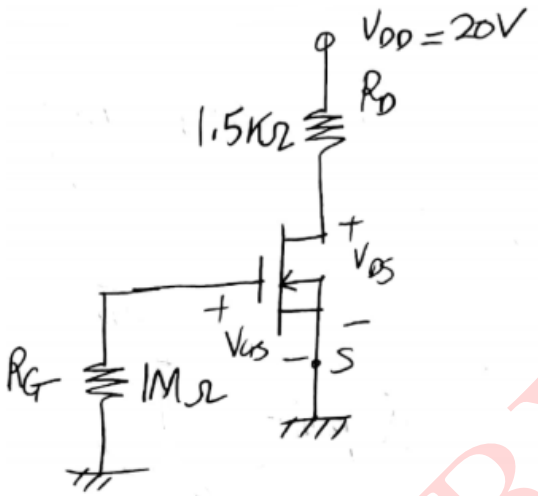

Figure 6: Circuit Diagram

Solution: $V_{GS} = V_G - V_S$

From figure 6, $V_S = 0$

Also, $V_G = I_G R_G$ ...($I_G = 0$ for MOSFET)

$\therefore V_G = 0 \implies V_{GSQ} = 0$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}(1-0)^2 = I_{DSS}$$

i.e. $I_{DQ} = I_{DSS} = 10\text{mA}$

Q-point $\equiv (V_{GSQ}, I_{DQ}) \equiv$ **(0, 10mA)**

$V_{DS} = V_{DD} - I_D R_D = 20 - 10\text{mA}\times 1.5\text{k}\Omega =$ **5V**

3. For the FET amplifier circuit shown in figure 7, find the drain current and gate to source voltage. Given: R1 = 2.1MΩ, R2 = 270kΩ, R_D = 2.4kΩ, R_{S1} = 300Ω, R_{S2} = 1.2kΩ, V_{DD} = 16V, I_{DSS} = 8mA, $|V_P|$ = 4V

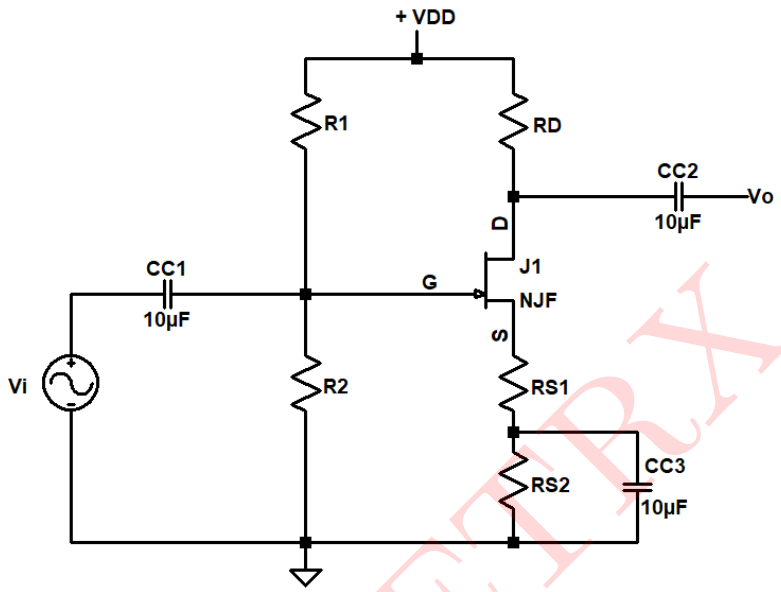

Figure 7: FET Amplifier

Solution: Figure 7 is a voltage divider bias circuit employing n-channel JFET. For DC abalysis, all the capacitors are short circuited as shown in figure 8:

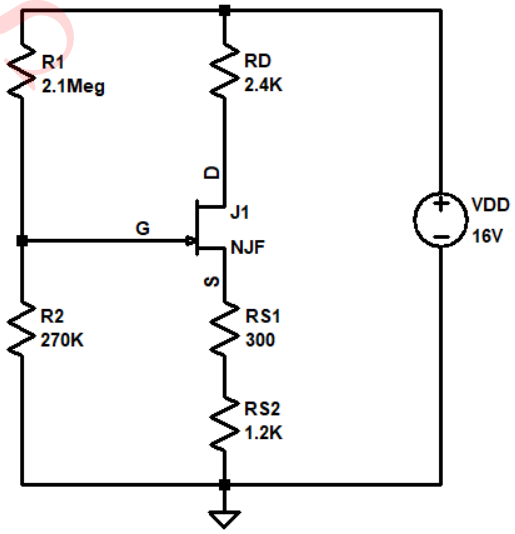

Figure 8: DC analysis

Using voltage divider concept,

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \left[\frac{270k\Omega}{2.1M\Omega + 270k\Omega} \times 16\right] = 1.822\text{V}$$

Applying KVL to the G-S loop:

$$V_{GS} = V_G - I_D R_S = 1.822 - 1500 I_D \implies I_D = \frac{1.822 - V_{GS}}{1500} \quad ...(1)$$

In saturation region,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \quad ...(2)$$

Substituting Equation (1) in equation (2), we get:

$$\frac{1.822 - V_{GS}}{1500} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\frac{1.822 - V_{GS}}{1500} = 8 \times 10^{-3}\left[1 - \frac{V_{GS}}{4}\right]^2$$

$$\frac{1.822 - V_{GS}}{1500} = 8 \times 10^{-3}\left[1 + \frac{V_{GS}^2}{16} + \frac{V_{GS}}{2}\right]$$

$$1.822 - V_{GS} = 12\left[1 - \frac{V_{GS}^2}{16} + \frac{V_{GS}}{2}\right]$$

$$1.822 - V_{GS} = 12 - \frac{3V_{GS}^2}{4} + 6V_{GS}$$

$$0.75V_{GS}^2 + 7V_{GS} + 10.178 = 0 \qquad \therefore V_{GS} = -1.8V,\ -7.53V$$

Q-point should lie inside the transfer characteristics, i.e. $(V_{GS} > V_P)$

$$\therefore V_{GS} = -1.8\text{V}$$

$$\therefore I_D = \frac{1.822 + 1.8}{1500} = 2.415\text{mA} \qquad ...\text{using (1)}$$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

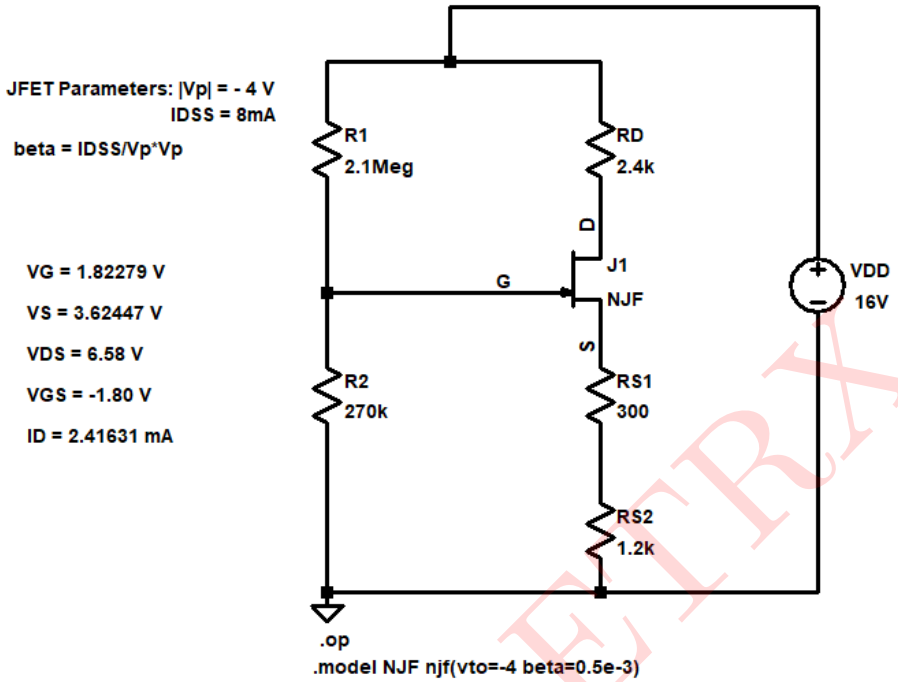

Figure 9: Circuit schematic: Results

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated Value
V_G	1.822V	1.8228V
I_D	2.415mA	2.4163mA
V_{GS}	-1.8V	-1.80V

Table 5: Question3

4. For the E-MOSFET circuit shown in figure 3 , calculate V_G, I_D, V_{GS} and V_{DS} **[10]**
R1 = 22MΩ, R2 = 18MΩ, R_D = 3kΩ, R_S = 0.82kΩ, V_{DD} = 40V, $V_{GS_{(TH)}}$ = 5V
$V_{GS_{(ON)}}$ = 10V, $I_{D_{(ON)}}$ = 3mA

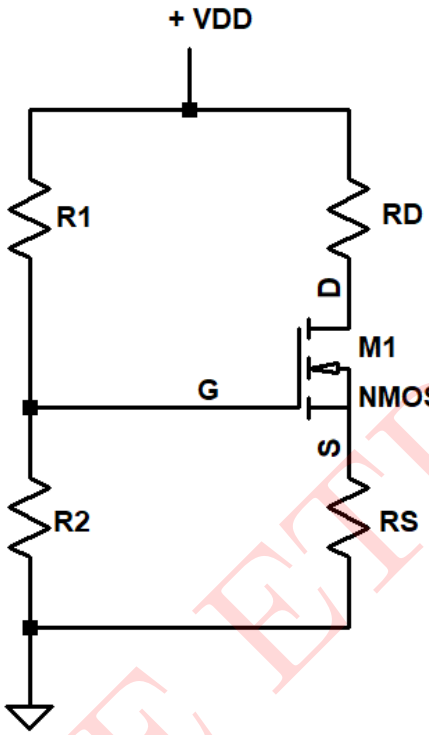

Figure 10: Circuit Diagram

Solution: Figure 10 is a voltage divider bias circuit employing enhancement mode n-channel MOSFET.

$$\therefore V_G = \frac{R_2}{R_1 + R_2} \times 100 = \frac{18M\Omega}{22M\Omega + 18M\Omega} \times 40 = 18V$$

Applying KVL to G-S loop,

$$V_G - V_{GS} - I_D R_S = 0$$

$$V_{GS} = 18 - 820(I_D) \qquad \therefore I_D = \frac{18 - V_{GS}}{820} \qquad ...(1)$$

For E-MOSFET, we know:

$$k_n = \frac{I_{D(ON}}{[V_{GS(ON)} - V_{GS(TH)}]^2} = \frac{3 \times 10^{-3}}{(10-5)^2}\ 0.13\text{mA}/V^2$$

In saturation region,

$$I_D = k_n[V_{GS} - V_{GS(TH)}]^2 \qquad ...(2)$$

Substituting equation (1) in equation (2), we get:

$$\frac{18 - V_{GS}}{820} = 0.12 \times 10^{-3}[V_{GS} - 5]^2$$

$$\frac{18 - V_{GS}}{820} = 0.12 \times 10^{-3}[V_{GS}^2 - 10V_{GS} + 25]$$

$$18 - V_{GS} = 0.0984[V_{GS}^2 - 10V_{GS} + 25]$$

$$18 - V_{GS} = 0.0984V_{GS}^2 - 0.984V_{GS} + 2.46$$

$$0.0984V_{GS}^2 + 0.016V_{GS} - 15.54 = 0$$

$$\therefore V_{GS} = 12.5V, -12.65V$$

For $V_{GS} = 12.5$V,

Applying KVL to D-S loop,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 40 - \frac{18 - V_{GS}}{820}(3 + 0.82) \times 10^3$$

Putting $V_{GS} = 12.5$V, we get:

$$V_{DS} = 14.38\text{V}$$

For $V_{GS} = -12.65$V,

Applying KVL to D-S loop,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 40 - \left(\frac{18 + 12.65}{820}\right) 3.82 \times 10^3$$

$$V_{DS} = -102.78\text{V}$$

Practically, V_{DS} is positive. Hence, $V_{DS} = 14.38$V

$$\therefore V_{GS} = 12.5\text{V}$$

$$\therefore I_D = \frac{18 - V_{GS}}{820} = \frac{18 - 12.5}{820} = 6.725\text{mA} \qquad \text{...from (1)}$$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

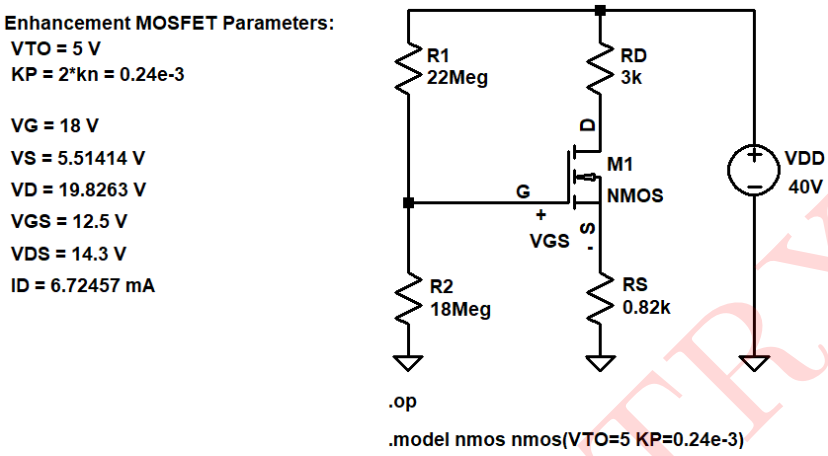

Figure 11: Circuit Schematic: Results

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
V_G	18V	18V
V_{GS}	12.5V	12.5V
V_{DS}	14.38V	14.3V
I_D	6.725mA	6.7246mA

Table 6: Question 4

5. For the network shown in figure 12, determine I_{DQ}, V_{GSQ}, V_{DS} and V_D
Given: $I_{DSS} = 8\text{mA}$, $V_P = 4\text{V}$, $R_D = 2.2\text{k}\Omega$, $R_S = 0.51\text{k}\Omega$, $R_G = 1\text{M}\Omega$

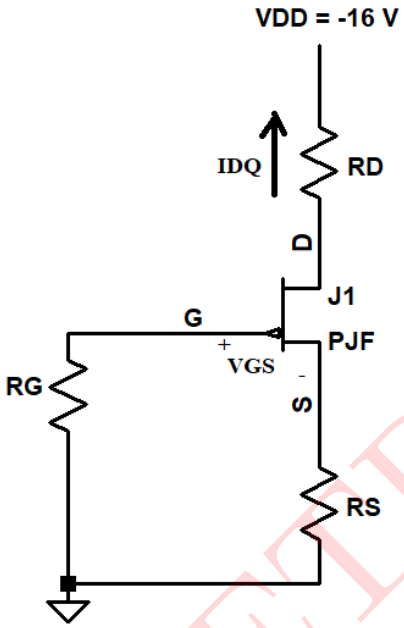

Figure 12: Circuit Diagram

Solution: Figure 12 is a self-bias configuration employing p-channel JFET.

For JFET, $I_G = 0\text{A}$

Applying KVL to G-S loop:

$$-V_{GS} + 0.51I_{SQ} = 0$$

$$-V_{GS} + 0.51I_{DQ} = 0 \qquad \because I_{DQ} = I_{SQ}$$

$$\therefore I_{DQ} = \frac{V_{GS}}{0.51} \qquad \ldots(1)$$

In saturation region,

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\frac{V_{GS}}{0.51} = 8\left[1 - \frac{V_{GS}}{4}\right]^2 \qquad \ldots\text{using (1)}$$

$$\frac{V_{GS}}{0.51} = 8 + \frac{V_{GS}^2}{2} - 4V_{GS}$$

$$0.5V_{GS}^2 - 4V_{GS} - 1.961V_{GS} + 8 = 0$$

$$0.5V_{GS}^2 - 5.961V_{GS} + 8 = 0$$

$\therefore V_{GS} = 10.38\text{V}, 1.541\text{V}$

For $V_{GS} = 10.38\text{V}$, $I_{DQ} = \dfrac{10.38}{0.51} = 20.353\text{mA}$

For $V_{GS} = 1.541$, $I_{DQ} = \dfrac{1.541}{0.51} = 3.022\text{mA}$

Since, $I_{DQ} \leq I_{DSS}$

$\therefore I_{DQ} = \mathbf{3.022mA}$ and $V_{GSQ} = \mathbf{1.541V}$

Applying KVL to D-S loop:

$-18 - V_{DS} + I_{DQ}(R_D + R_S) = 0$

$V_{DS} = -18 + I_{DQ}(R_D + R_S)$

$V_{DS} = -18 + 3.022 \times 10^{-3}(2.71 \times 10^{3}) = \mathbf{-9.8104V}$

$V_{GS} = V_G - V_S \quad \therefore V_S = -1.54122 \quad (\because V_G = 0)$

Also, $V_{DS} = V_D - V_S$

$\therefore V_D = V_{DS} + V_S = -9.8104 - 1.54122$

$\therefore V_D = \mathbf{-11.3516\ V}$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

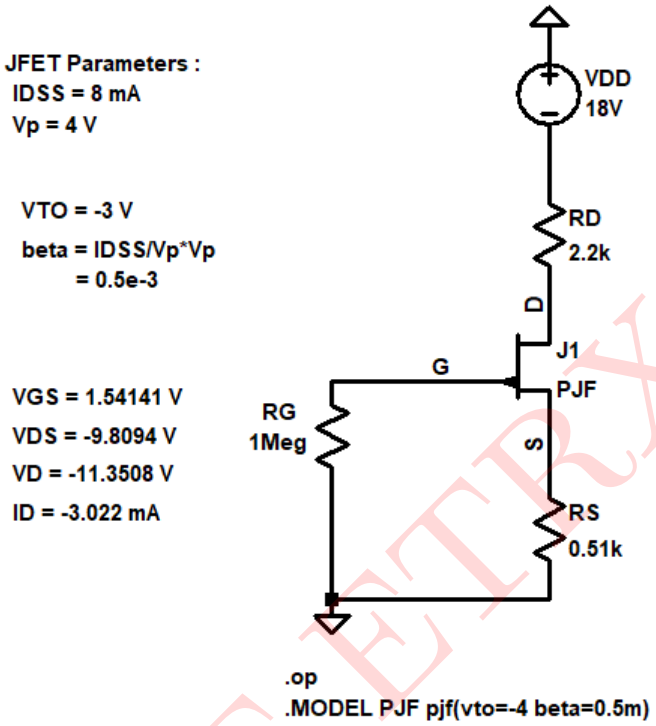

Figure 13: Circuit Schematic: Results

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
V_{GSQ}	1.541V	1.54141V
I_{DQ}	3.022mA	3.02237mA
V_{DSQ}	−9.8103V	−9.8104V
V_D	−11.3516V	−11.3508V

Table 7: Question 5

6. For the network shown in figure 14, determine I_{DQ}, V_{GSQ}, V_{DS} and V_D
Given: $R_D = 2k\Omega$, $R_G = 1M\Omega$, $V_{GS(TH)} = -3\text{V}$, $V_{GS(ON)} = -7\text{V}$, $I_{D(ON)} = 4\text{mA}$

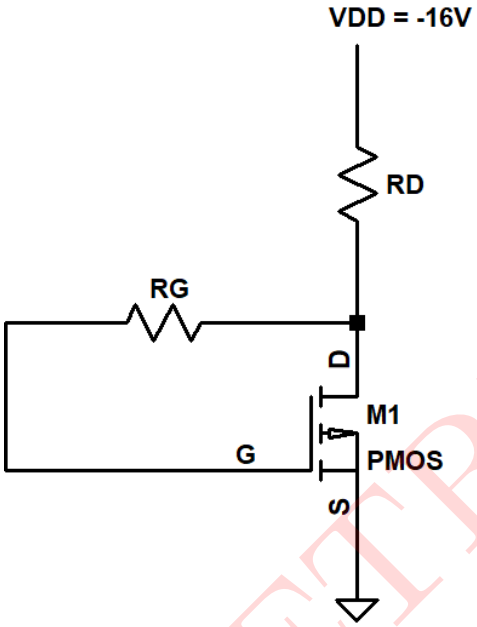

Figure 14: Circuit Diagram

Solution: Figure 14 is a drain-gate feedback configuration employing p-channel MOSFET.

Applying KVL to D-S loop,

$$-16 + 2I_{DQ} - V_{DS} = 0$$

$$V_{DS} = -16 + 2I_{DQ}$$

For drain-gate feedback configuration, $V_{DS} = V_{GS}$

$$\therefore V_{GS} = -16 + 2I_{DQ}$$

$$\therefore I_{DQ} = \frac{V_{GS} + 16}{2} \qquad \ldots(1)$$

We know, $k_P = \dfrac{I_{D(ON)}}{\left[V_{GS(ON)} - V_{GS(TH)}\right]^2}$

$$k_P = \frac{4 \times 10^{-3}}{[-7+3]^2} = 0.25\text{mA}/V^2$$

For saturation region,

$I_D = k_P(V_{GS} + V_{GS(TH)})^2$

$\frac{V_{GS} + 16}{2} = 0.25[V_{GS} + 3]^2$ ...using (1)

$V_{GS} + 16 = 0.5[V_{GS} + 3]^2$

$V_{GS} + 16 = 0.5[V_{GS}^2 + 9 + 6V_{GS}]$

$V_{GS} + 16 = 0.5V_{GS}^2 + 4.5 + 3V_{GS}$

$0.5V_{GS}^2 + 2V_{GS} - 11.5 = 0$

$\therefore V_{GS} = 3.196\text{V}, -7.196\text{V}$

Since, $V_{GS} < V_P$

$\therefore V_{GS} = \mathbf{-7.196V}$

$\therefore I_{DQ} = \frac{V_{GS} + 16}{2}$ ...using(1)

$I_{DQ} = \frac{-7.196 + 16}{2} = \mathbf{4.402mA}$

$V_{DS} = V_{GS} = \mathbf{-7.196V}$

$V_{DS} = V_D - V_S \implies V_D = \mathbf{-7.196V}$ $(\because V_S = 0V)$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

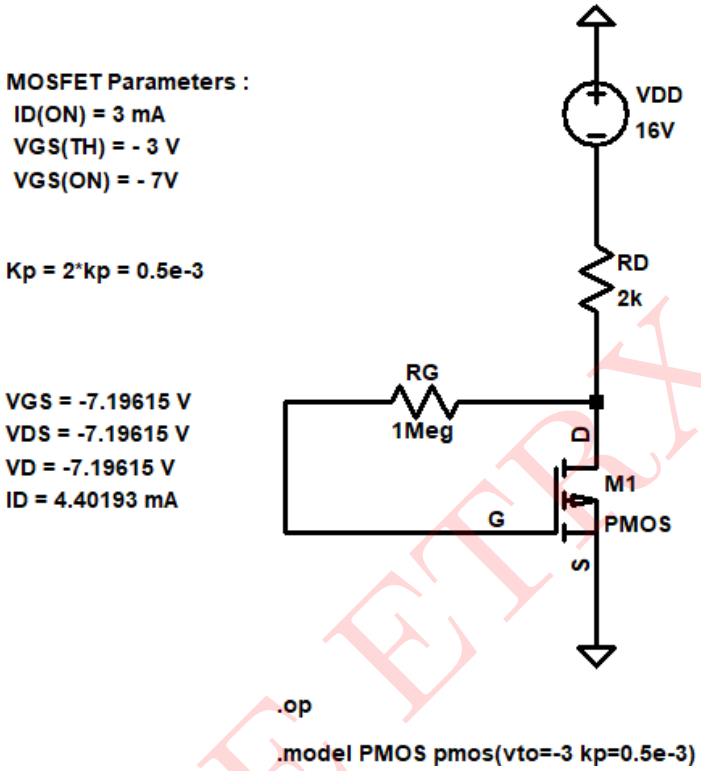

Figure 15: Circuit Schematic: Results

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
V_{GSQ}	$-7.196V$	$-7.19615V$
I_{DQ}	4.402mA	4.40193mA
V_{DS}	-7.196V	-7.19615V
V_D	-7.196V	-7.19615V

Table 8: Question 6

7. The current gain of the transistor shown in circuit of figure 16 is $\beta = 100$
Determine V_B and I_{EQ}
Given: $R_1 = 20k\Omega$, $R_2 = 15k\Omega$, $R_E = 1k\Omega$

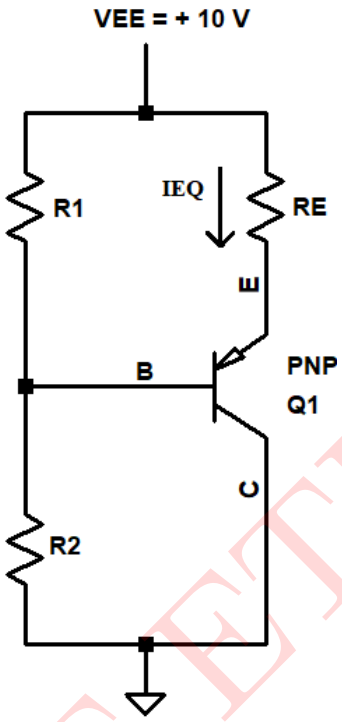

Figure 16: Circuit Diagram

Solution: The circuit shown in figure 16 is a voltage divider configuration employing PNP BJT.

$$\therefore V_B = \frac{R_2}{R_1 + R_2} \times V_{EE} = \left[\frac{15}{15 + 20}\right] \times 10 = \mathbf{4.286V}$$

Applying KVL to E-B loop:

$$V_B + V_{BE} + I_E R_E - 10 = 0$$

$$\therefore I_E = \frac{10 - V_B - V_{BE}}{R_E} = \frac{10 - 4.286 - 0.7}{1k\Omega} = \mathbf{5.014mA}$$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

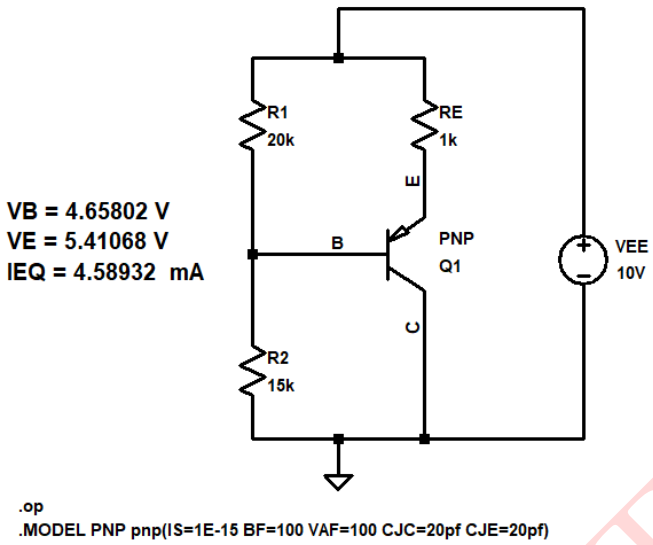

Figure 17: Circuit Schematic: Results

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
V_B	4.286V	4.6580V
I_{EQ}	5.014mA	4.58932mA

Table 9: Question 7

8. For circuit shown in figure 18, let $\beta = 125$. Find I_{CQ} and V_{CEQ}
Given: $R_1 = 58k\Omega$, $R_2 = 42k\Omega$, $R_E = 10\text{k}\Omega$

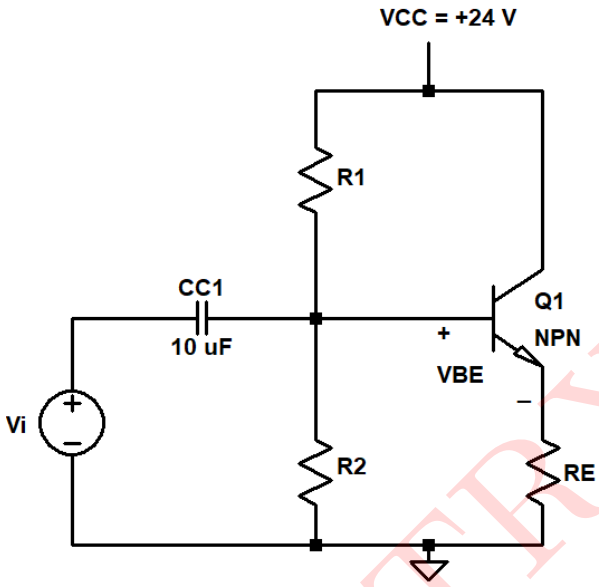

Figure 18: Circuit Diagram

Solution: Figure 18 is a voltage divider configuration employing npn BJT. The DC equivalent circuit is given as:

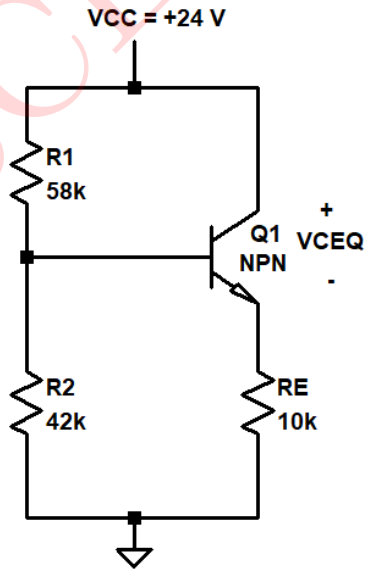

Figure 19: DC equivalent circuit

$$\therefore V_B = \left[\frac{R_2}{R_1 + R_2}\right] \times V_{CC} = \left[\frac{42k\Omega}{42k\Omega + 58k\Omega}\right] \times 24 = 10.08\text{V}$$

Applying KVL to the B-E loop:

$V_B - V_{BE} - I_E R_E = 0$

$\therefore I_E = \dfrac{V_B - V_{BE}}{R_E} = \dfrac{10.08 - 0.7}{10k\Omega} = 0.938\text{mA}$

We know, $I_{CQ} = \left(\dfrac{\beta}{\beta+1}\right) I_E = \dfrac{125}{126} \times 0.938 \times 10^{-3} = \mathbf{0.9306mA}$

Applying KVL to the C-E loop:

$24 - V_{CEQ} - I_E R_E = 0$

$V_{CEQ} = 24 - (0.938mA)(10k\Omega) = \mathbf{14.62V}$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

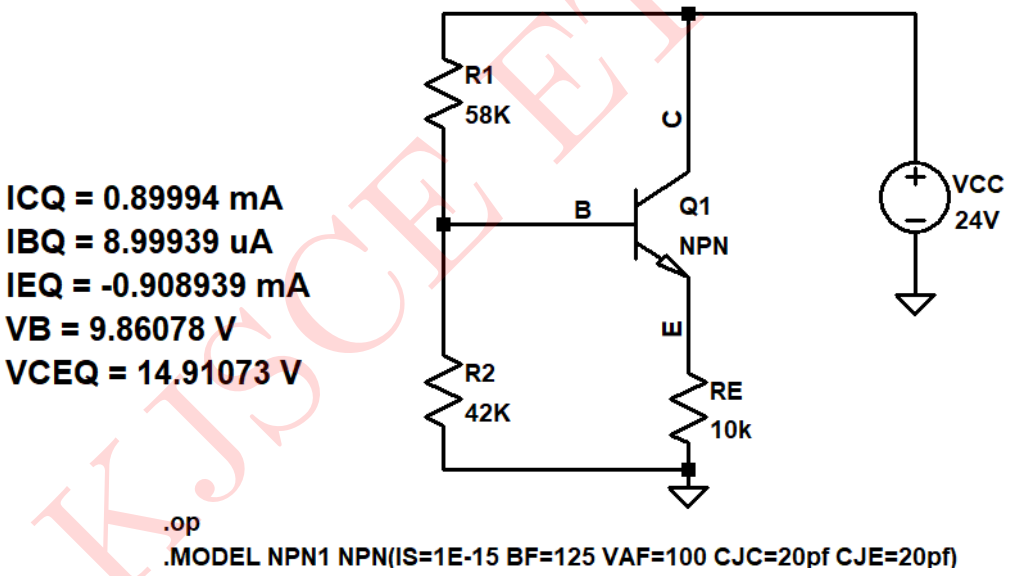

Figure 20: Circuit Schematic: Results

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
V_B	10.08V	9.86078V
V_{CEQ}	14.62V	14.91073V
I_{EQ}	0.938mA	0.908939mA
I_{CQ}	0.9306mA	0.89994mA

Table 10: Question 8

9. The parameters of the transistor shown in Figure 21 are $\beta = 150$, $V_{BE} = 0.7$V
Given: $V_{CC} = 15$V, $V_B = 5$V, $R_B = 200$kΩ, $R_E = 1.5$kΩ and $R_E = 500$Ω
Determine:
a. Base current I_B
b. Collector current I_C
c. Collector to Emitter voltage V_{CE}

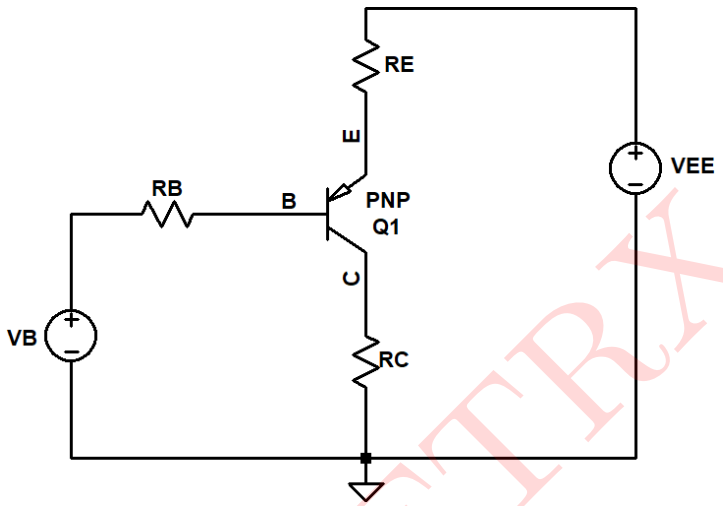

Figure 21: Circuit Diagram

Solution: Circuit shown in figure 21 is a fixed bias configuration employing PNP BJT.

Applying KVL to the B-E loop:

$15 - 500I_E - V_{BE} - 200I_B - 5 = 0$

$15 - 500(\beta + 1)I_B - 0.7 - 200I_B - 5 = 0 \qquad ...(\because I_E = (\beta + 1)I_B)$

$\therefore I_B = \dfrac{15 - 0.7 - 5}{[500(151) + 200]} = \mathbf{0.12285}\mu A$

$I_C = \beta I_B = 150 \times 1.2285 \times 10^{-7} = 1.823 \times 10^{-5} A = \mathbf{0.01823}$mA

$I_E = (1 + \beta)I_B = 151 \times 1.2285 \times 10^{-7}$

$\therefore I_E = 1.855 \times 10^{-5}$A $= 0.01855$mA

Applying KVL to the C-E loop:

$15 - 500I_E - V_{EC} - 1.5I_C = 0$

$V_{EC} = 15 - (500 \times 10^3 \times 1.855 \times 10^{-5}) - (1.5 \times 10^3 \times 1.823 \times 10^{-5})$

$V_{EC} = 5.6977$V

$\therefore V_{CE} = \mathbf{-5.6977V}$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

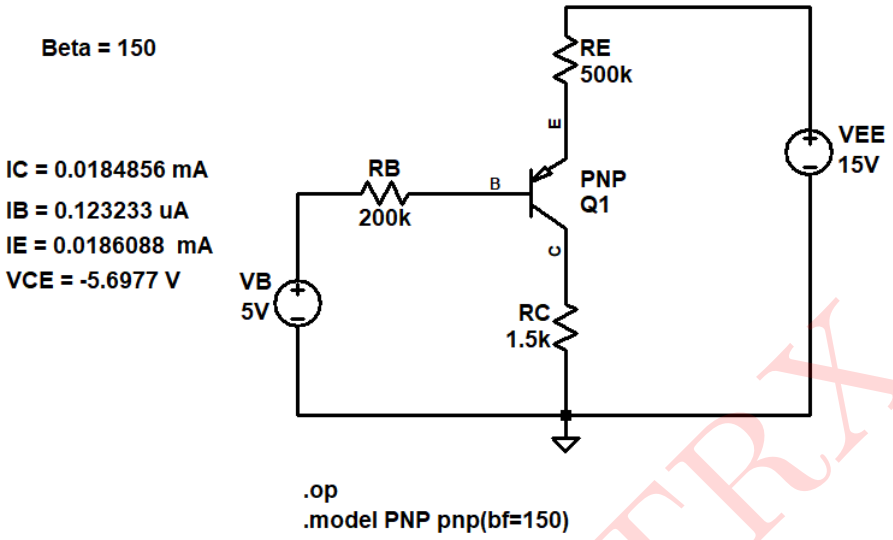

Figure 22: Circuit Schematic: Results

Comparsion between theoretical and simulated values:

Parameter	Simulated value	Theoretical value
I_C	0.01849mA	0.01823mA
I_B	$0.1232\mu A$	$0.12285\mu A$
I_E	0.01861mA	0.01855mA
V_{CE}	−5.6977V	−5.6977V

Table 11: Question 9

10. The parameters of the PNP BJT circuit shown in figure 23 are as follows: $R_C = 10\text{k}\Omega$, $R_E = 1\text{k}\Omega$, $V_{CC} = 15\text{V}$, $V_{EE} = 5\text{V}$, $V_{EB} = 0.6\text{V}$ and $\alpha = 0.992$. Calculate I_B, I_C, I_E and V_{CB} at Q-point. Consider $V_{CE(sat)} = 0.025\text{V}$ if needed.

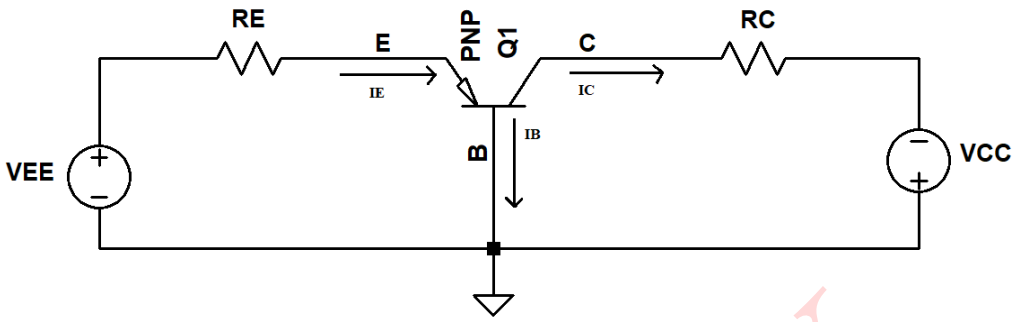

Figure 23: Circuit Diagram

Solution: Circuit shown in figure 23 is a common base BJT amplifier.

Assuming the transistor in the active region, applying KVL to the B-E loop:

$$V_{EE} - I_E R_E - V_{EB(ON)} = 0$$

$$\therefore I_E = \frac{V_{EE} - V_{EB(ON)}}{R_E} = \frac{5 - 0.6}{1k\Omega} = \mathbf{4.4mA}$$

$$I_C = \alpha I_E = 0.992 \times 4.4 \times 10^{-3} = \mathbf{4.365mA}$$

Applying KVL to the C-E loop:

$$5 - I_E R_E - V_{EC} - R_C I_C + 15 = 0$$

$$\therefore V_{EC} = 5 - 4.4 - 43.65 + 15 = -28.05\text{V}$$

V_{EC} cannot be negative, which means that the transistor is in saturation region.

Applying KVL to the C-E loop:

$$5 - I_E R_E - V_{CE(sat)} - R_C I_C + 15 = 0$$

$$\therefore I_C = \frac{20 - 4.4 - 0.025}{10} = \mathbf{1.558mA}$$

We know, $I_E = I_B + I_C$

$$\therefore I_B = I_E - I_C = 4.4\text{mA} - 1.558\text{mA} = \mathbf{2.842mA}$$

Applying KVL to the B-C loop:

$-15 + I_C R_C + V_{BC} = 0$

$V_{BC} = 15 - I_C R_C = 15 - (1.558 \times 10^{-3} \times 10 \times 10^3) = -0.58\text{V}$

$\therefore V_{CB} = \mathbf{0.58V}$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

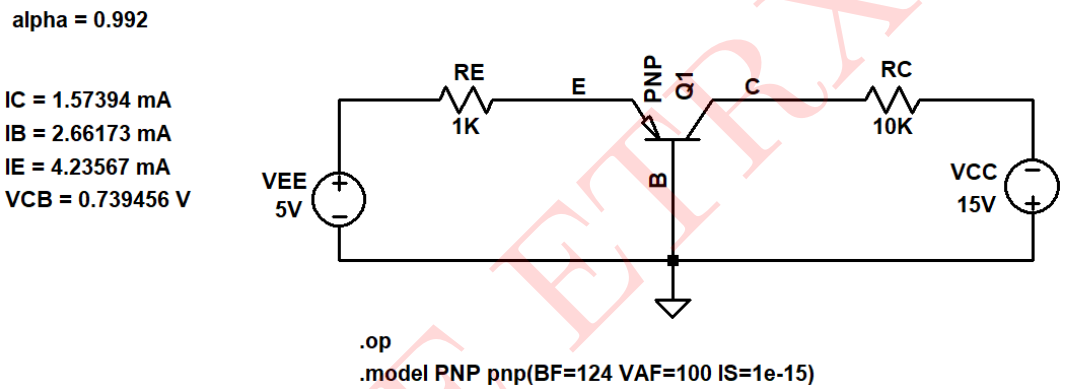

Figure 24: Circuit Schematic: Results

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
I_E	4.4mA	4.23567mA
I_C	1.558mA	1.57934mA
I_B	2.842mA	2.66173mA
V_{CB}	0.58V	0.7394V

Table 12: Question 10