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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Diode Application

28^{th} **June, 2020**

Numerical 1 : For the circuit shown below in figure 1, plot:
a) Input $V_{in}(t)$ and output $V_{out}(t)$ waveform
b) VTC curve
Given : $V_{in}(t) = 10V$ p-p sinusoidal signal with frequency of 5000 Hz. Use constant voltage model i.e. $V_{D,ON} = 0.7V$, $V_B = 1V$, $R_1 = 1k\Omega$

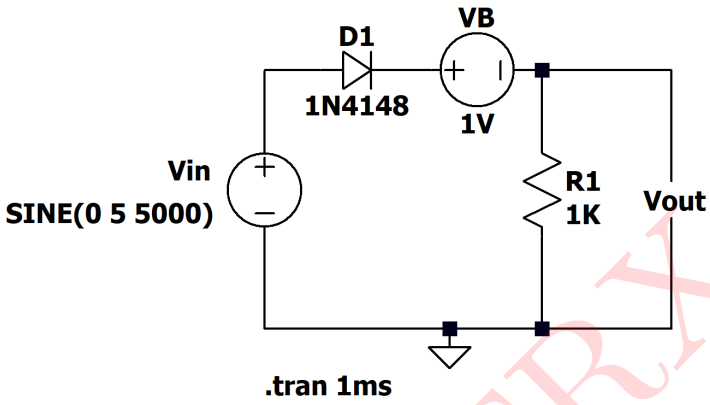

Figure 1: Circuit 1

Solution: Assuming constant voltage model for D_1

$V_{in} = 10V$ p-p

so $V_m = 5V$

Case 1: If $V_{in} > (V_{D,ON} + V_B)$

i.e. $V_{in} > (0.7 + 1)$, diode D_1 is ON (as anode voltage of the diode which connected to V_{in} is greater than cathode voltage by 0.7 otherwise it would turn off)

So the circuit becomes

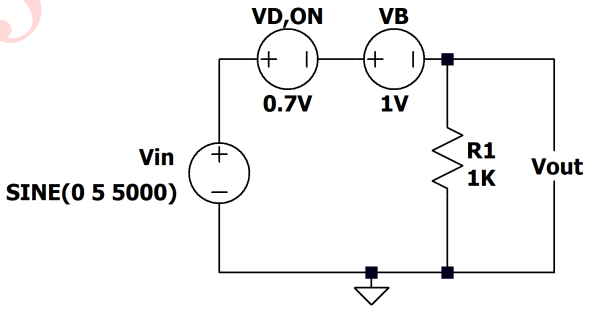

Figure 2: When diode D_1 is ON

By applying KVL,

$V_{out} + V_B + V_{D,ON} - V_{in} = 0$

$\therefore V_{out} = V_{in} - (V_B + V_{D,ON}) = 5 - (1 + 0.7) =$ **3.3V**

i.e the output will track the input but with a shift of $(V_{D,ON} + V_B) = 1.7V$

Case 2: If $V_{in} < (V_{D,ON} + V_B)$

i.e. $V_{in} < (0.7 + 1)$, diode D_1 is OFF

$\therefore$ if $V_{in} < 1.7V$ diode will be off

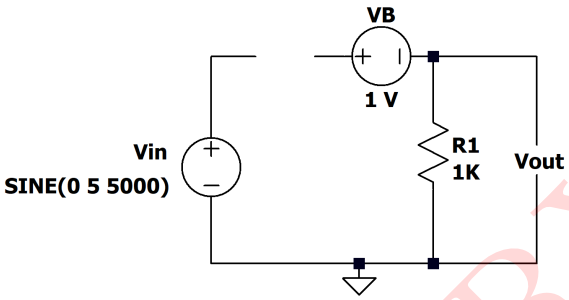

Figure 3: When diode D_1 is OFF

So here, $V_{out} = 0V$

Thus, the circuit is a negative biased series negative clipper

SIMULATED RESULT:
Above circuit is simulated in LTspice and the result is as follows:

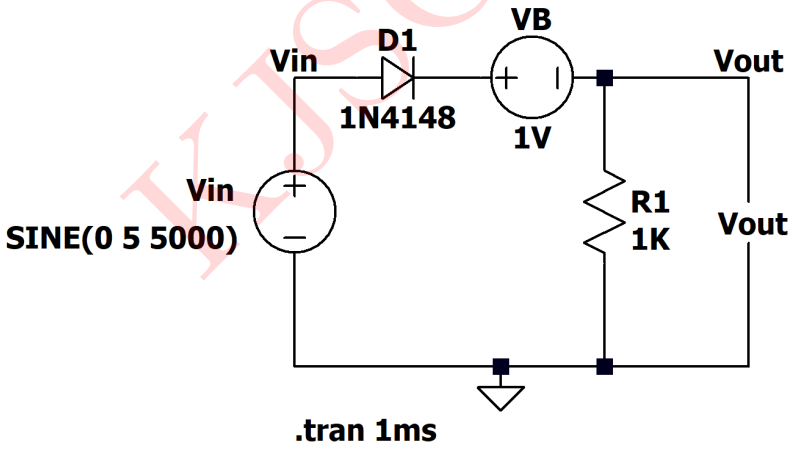

Figure 4: Circuit Schematic

The input and output waveforms are shown in figure 5.

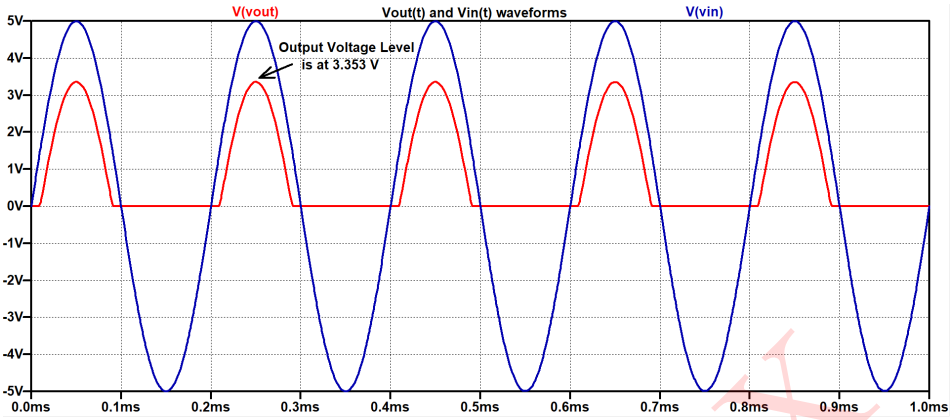

Figure 5: Input output waveform

The VTC curve for the following circuit is shown in the figure 6.

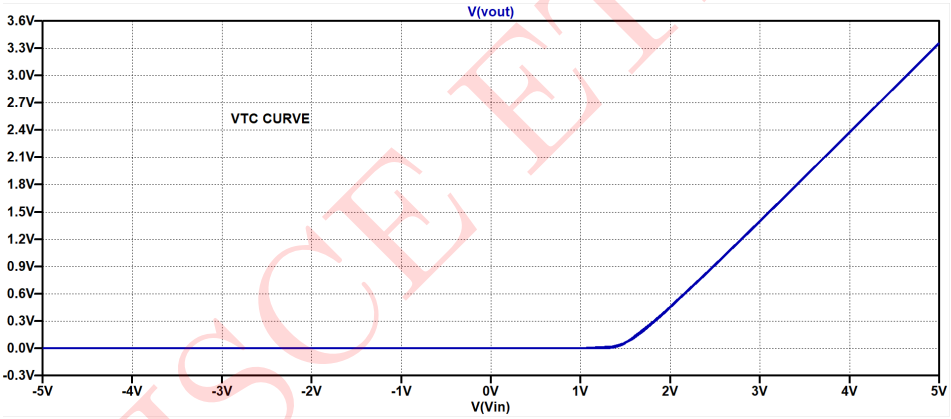

Figure 6: VTC curve

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
clipped output voltage value	3.35 V	3.3V

Table 1: Numerical 1

Numerical 2: For the circuit shown below in figure 8,
Plot : Input $V_{in}(t)$ and output $V_{out}(t)$ waveform
Given : $V_{in}(t) = 20V$ p-p square wave signal with frequency of 1000 Hz and Si diode

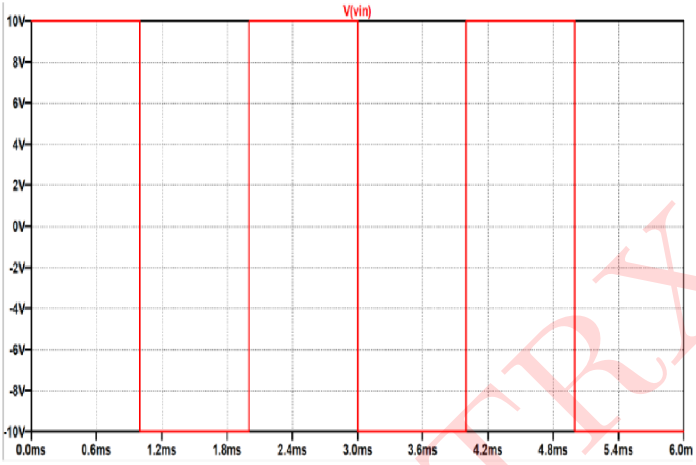

Figure 7: Input Waveform

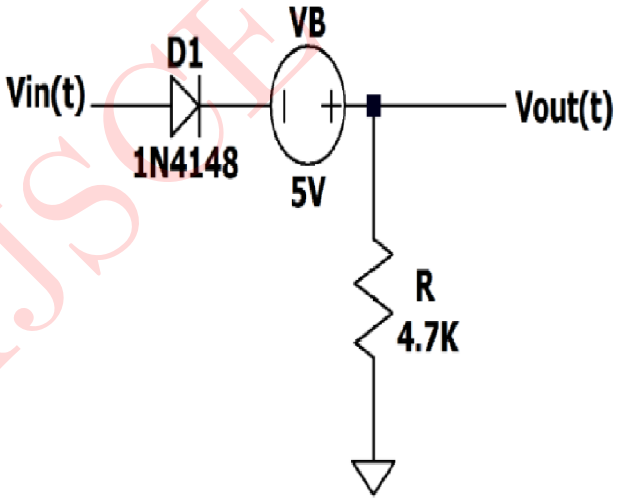

Figure 8: Circuit 2

Solution:
The given diode D_1 is a silicon diode so $V_{D,ON} = 0.7V$

$V_{in} = 20V$ p-p

So $V_m = 10V$ (Where $V_{in} = \pm V_m$)

Case 1: When, $V_{in} > (V_{D,ON} - V_B)$

i.e When $V_{in} > (0.7 - 5)$, diode D_1 is ON

[Because when the diode voltage of the diode which is connected to V_{in} is greater

than the cathode voltage which is connected to V_B by 0.7, the diode turns ON otherwise it will be OFF.]

So when $V_{in} > -4.3V$, D_1 turns on and the circuit becomes;

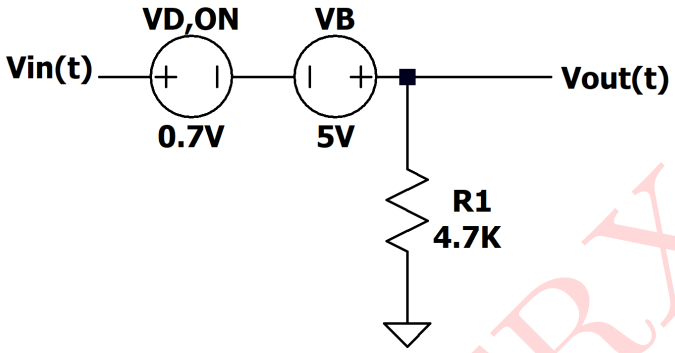

Figure 9: When diode D_1 is ON

By applying KVL,

$V_{out} - V_B + V_{D,ON} - V_{in} = 0$

$\therefore V_{out} = V_{in} - (V_{D,ON} - V_B)$

For positive half cycle $V_{in} = V_m = 10V$

so, $V_{out} = 10 - (0.7 - 5) = \mathbf{14.3V}$

i.e the output will track the input but with a shift of $(V_{D,ON} - V_B) = 4.3V$

Case 2: If $V_{in} < (V_{D,ON} - V_B)$

i.e. $V_{in} < (0.7 - 5)$, diode D_1 is OFF

$\therefore$ if $V_{in} < -4.3V$ diode will be off and the ciruit becomes

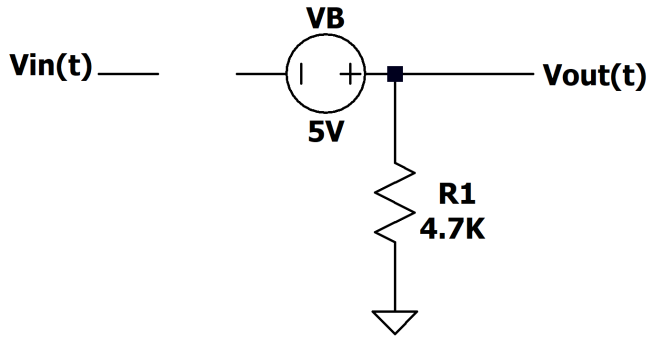

Figure 10: When diode D_1 is OFF

Thus, the circuit is a negative biased negative series clipper

SIMULATED RESULT:

Above circuit is simulated in LTspice and the result is as follows:

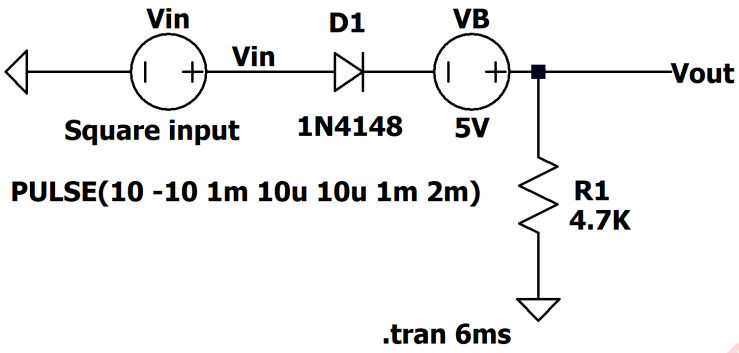

Figure 11: Circuit Schematic

The input and output waveforms are shown in figure 12.

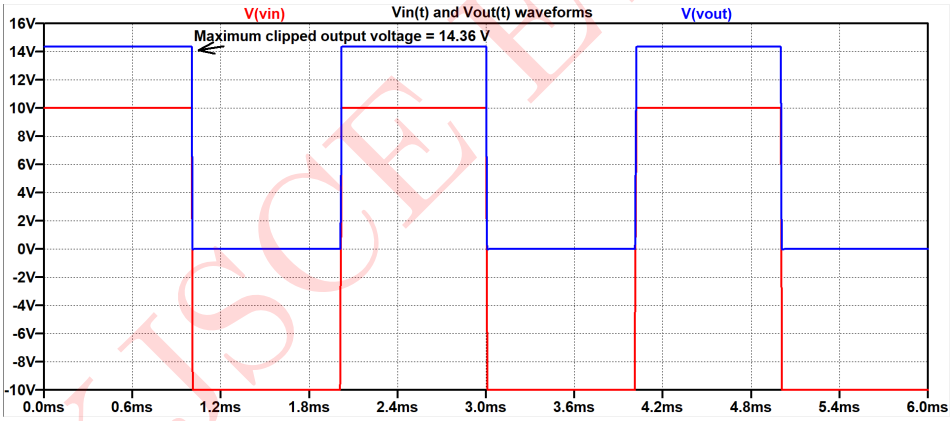

Figure 12: Input output waveform

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
Value at which output is clipped	$-4.36V$	$-4.3V$

Table 2: Numerical 2

Numerical 3: For the circuit shown below in figure 14,
Plot : Input $V_{in}(t)$ and output $V_{out}(t)$ waveform
Given : $V_{in}(t)$ is a square wave signal with frequency of 1000 Hz (amplitude given in input image) $C = 1\mu F$, $R_1 = 100K\Omega$, diode D_1 is Si diode i.e. $V_{D,ON} = 7V$,$V_B = 5V$ DC

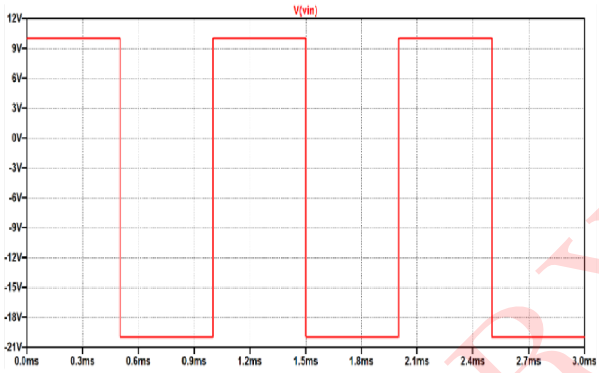

Figure 13: Input Signal

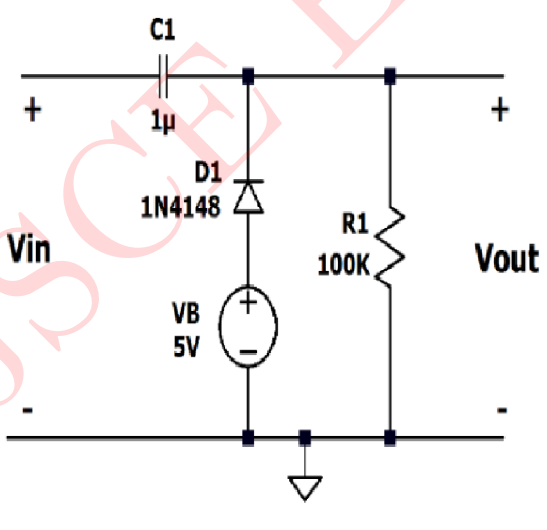

Figure 14: Circuit 3

Solution:
The given diode D_1 is a silicon diode so $V_{D,ON} = 0.7V$

For positive half cycle, $V_m = 10V$

For negative half cycle, $V_m = -20V$

Assumption: Here, RC time constant $= 100 \times 10^3 \times 1 \times 10^{-6} = 0.1sec.$ The RC time constant is large enough than the time period of the input signal to ensure that voltages across capacitor does not discharge significantly during the period the diode is OFF.

Operation:

a) During negative half cycle:

Here, $V_{in} = V_m = -20V$

When $V_{in} < (-V_{D,ON} + V_1)$, the diode D_1 is ON.

i.e when $V_{in} < (-0.7 + 5)$, D_1 turns ON.(Because the anode voltage of the diode is greater than the cathode voltage.)

so, when $V_{in} < 4.3V$, the circuit becomes;

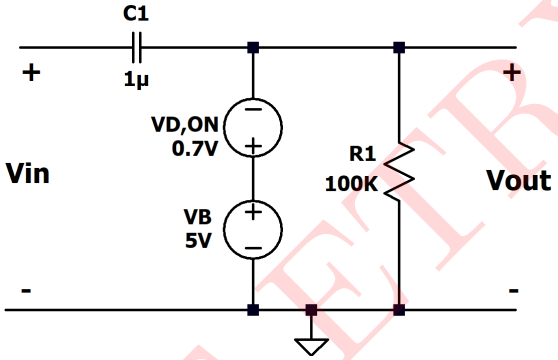

Figure 15: When diode D_1 is ON

By applying KVL,

$V_{out} - V_B + V_{D,ON} = 0$

$\therefore V_{out} = -V_{D,ON} + V_B = -0.7 + 5 = \mathbf{4.3V}$ (during negative half cycle)

b) At the same time, voltage across capacitor V_C charges upto $-V_m$

By applying KVL,

$V_{in} + V_C + V_{D,ON} - V_B = 0$

$\therefore V_C = -V_{in} - V_{D,ON} + V_B$

But $V_{in} = V_m = -20V$ for negative half cycle

$\therefore V_C = -(-20) - 0.7 + 5 = 20 + 5 - 0.7 = \mathbf{24.3V}$ (voltage across capacitor C during negative half cycle)

c) During positive half cycle:

Diode D_1 is OFF for the entire positive half cycle as it get reverse biased.

So, the circuit becomes:

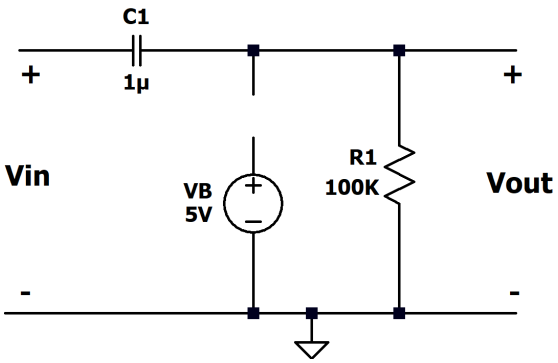

Figure 16: When diode D_1 is OFF

Thus, capacitor C holds the charge **24.3V** and acts as a battery.

On applying KVL

$V_{in} + V_C - V_{out} = 0$

$V_{out} = V_{in} + V_C$

But for positive half cycle, $V_{in} = V_m = 10V$

$V_{out} = 10 + 24.3 = \mathbf{34.3V}$ (for positive half cycle)

SIMULATED RESULTS:
Above circuit is simulated in LTspice and the result is as follows:

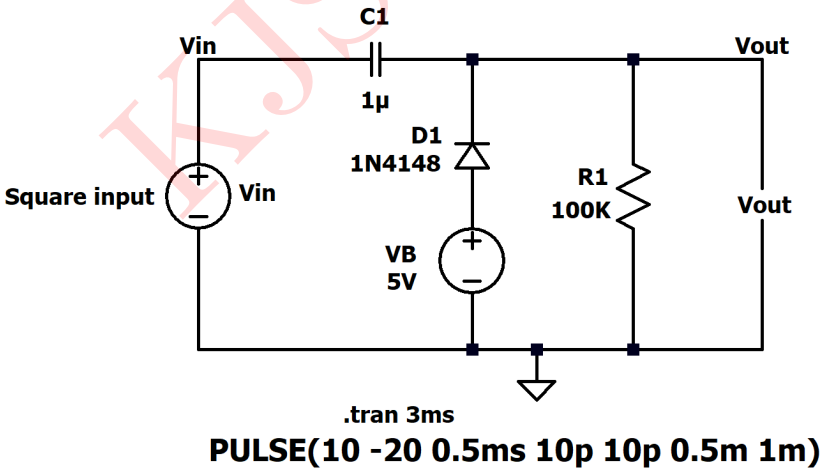

Figure 17: Circuit Schematic

The input and output waveforms are shown in figure 18.

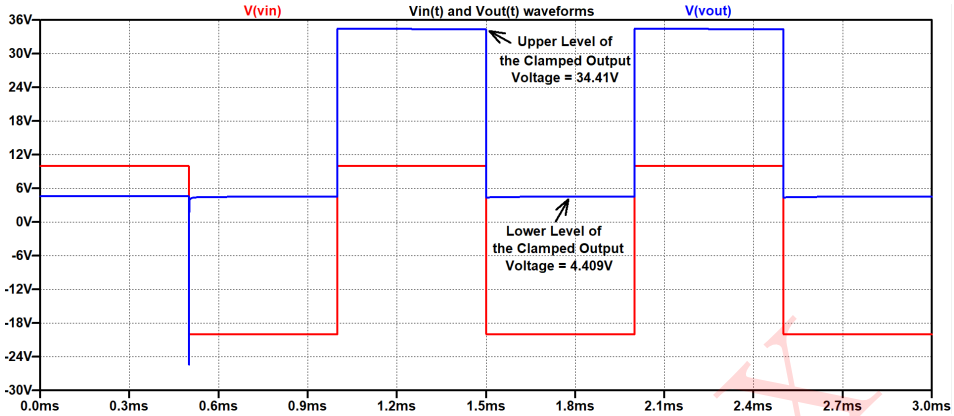

Figure 18: Input output waveform

Comparison between Theoretical and Simulated values :-

Parameter	Simulated	Theoretical
Upper level of the positive clamped output voltage	34.41V	34.3V
Lower level of the positive clamped output voltage	4.409V	4.3V

Table 3: Numerical 3

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