**K. J. SOMAIYA COLLEGE OF ENGINEERING**
**DEPARTMENT OF ELECTRONICS ENGINEERING**
**ELECTRONIC CIRCUITS**
**Diode Application**

**Numerical 1:**
For the circuit shown in figure 1, Plot
a) Input $V_{in}(t)$ and output $V_{out}(t)$ waveform
b) VTC Curve
Given: $V_{in} = 10$ Vp-p sinusoidal signal with frequency of 500Hz.
Use constant voltage model i.e. $V_{D_{on}} = 0.7V$, $V_B = 1V$ and $R_1 = 1k\Omega$

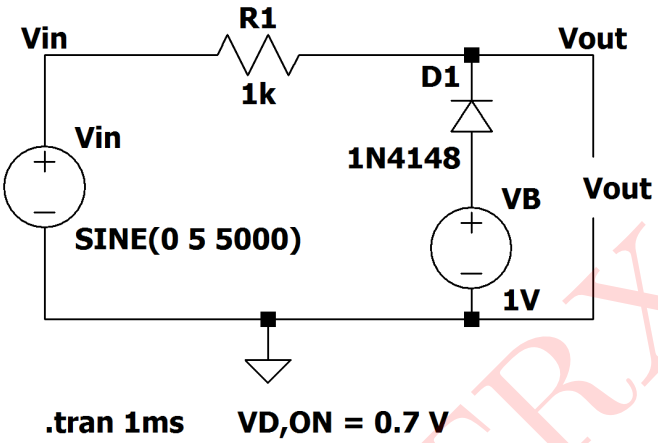


Figure 1: Circuit 1

**Solution:**

Assuming constant voltage model($V_{D_{on}} = 0.7V$) for the diode $D_1$, bias voltage $V_B$ forward biases the diode $D_1$

$\rightarrow$ If $V_{in} < (-V_{D1_{on}} + V_B)$, diode $D_1$ is ON(as cathode voltage is greater than anode voltage) and hence circuit reduces to the circuit shown in figure 2

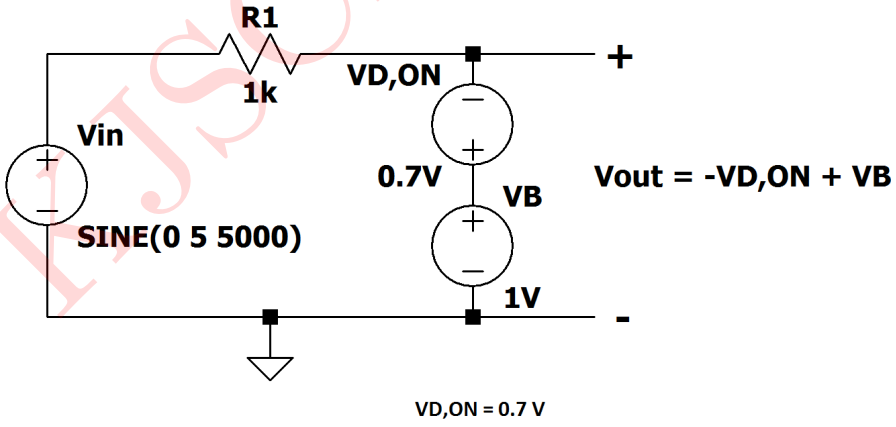


Figure 2: When diode is ON

$V_{out} = -V_{D1_{on}} + V_B = -0.7 + 1 = 0.3V$

$\boldsymbol{V_{out} = 0.3V}$

→ If $V_{in} > (-V_{D1_{on}} + V_B)$, diode $D_1$ is OFF(as anode voltage is greater than cathode voltage) and hence circuit reduces to the circuit shown in figure 3

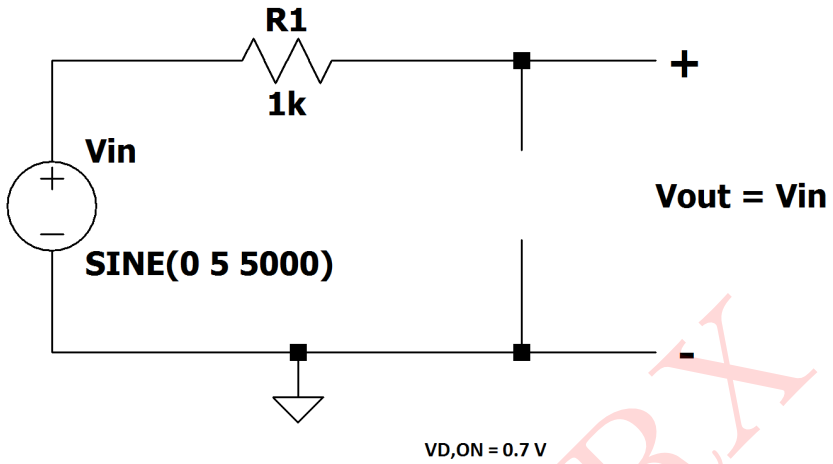


Figure 3: When diode is OFF

$\therefore \boldsymbol{V_{out} = V_{in}}$ [i.e. output follows the input]

**SIMULATED RESULTS:**
Above circuit was simulated in LTSpice and results are presented below:

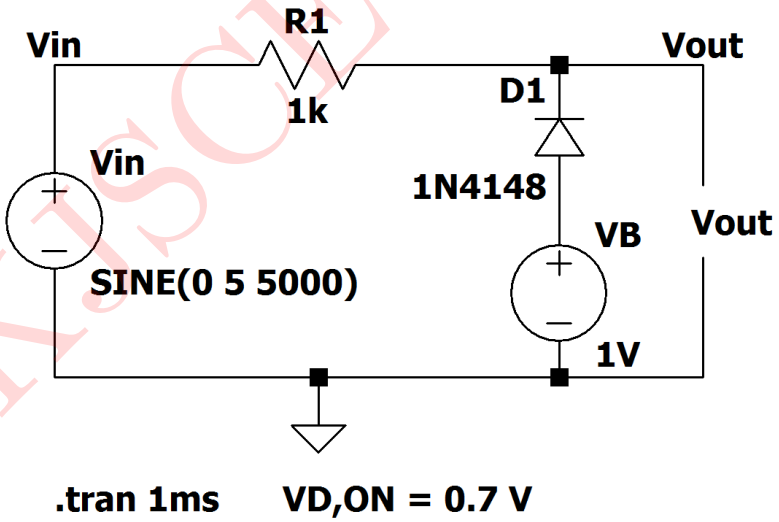


Figure 4: Circuit Schematic 1

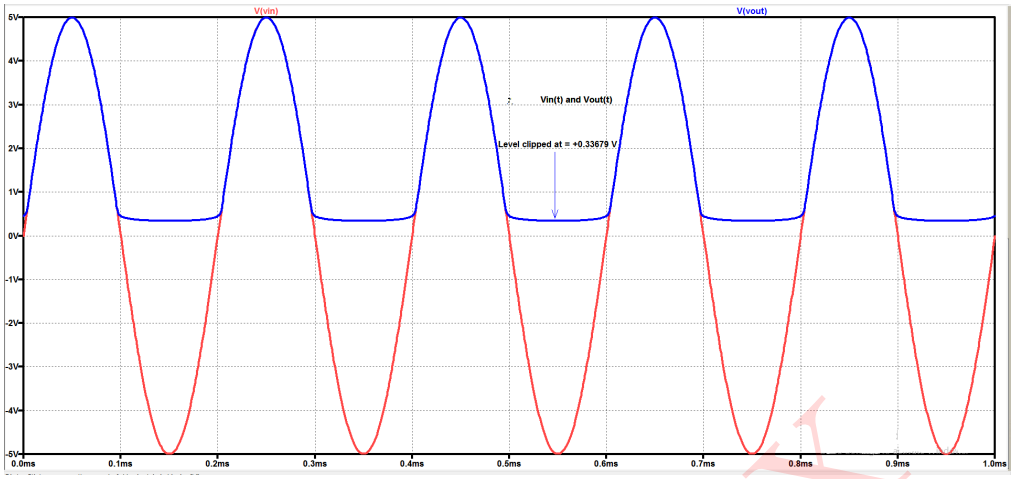


Figure 5: Input & Output waveform

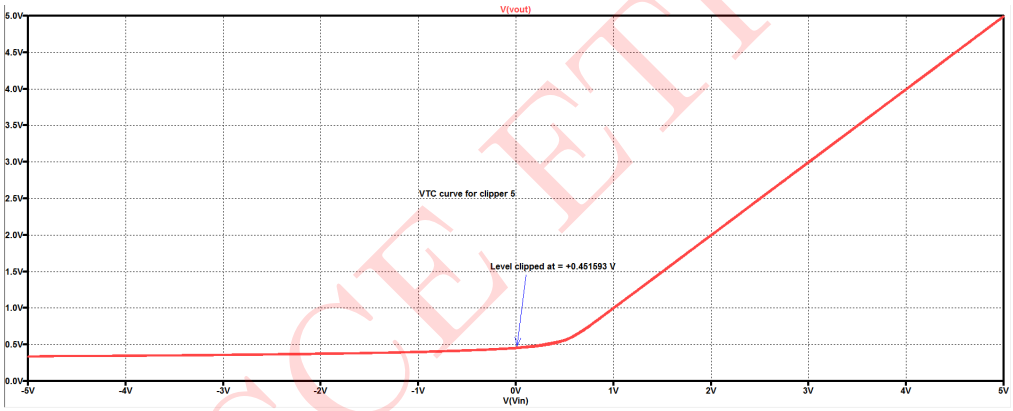


Figure 6: VTC Curve

From the above waeforms, we could conclude that the clipper circuit was a negative biased shunt(parallel) clipper.

**Comparison of Theoretical and Simulated Values:**

| Parameters | Theoretical | Simulated |
|---|---|---|
| level of clipped voltage | $0.3V$ | $0.33V$ |

Table 1: Question 1

**Numerical 2:**
For the circuit shown in figure 8, Plot: Input $V_{in}(t)$ and output $V_{out}(t)$ waveforms
Given: $V_{in}(t) = 16$ Vp-p sinusoidal signal with frequency of 1000Hz.

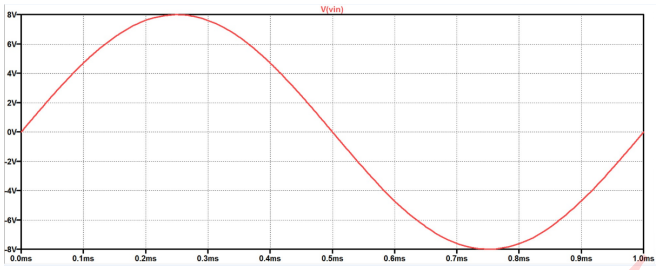


Figure 7: Input

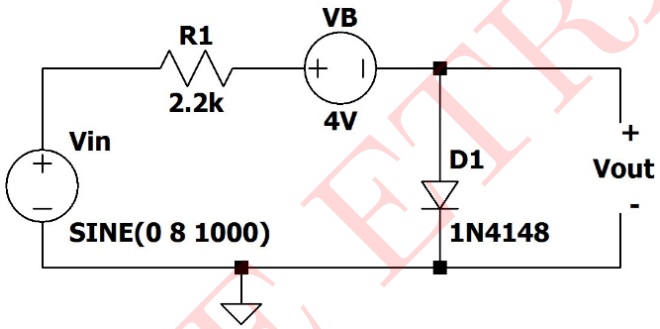


Figure 8: Circuit 2

**Solution:**

The given diode $D_1$ is silicon diode, hence $V_{D1_{on}} = 0.7V$

$\rightarrow$ If $V_{in} > (V_{D1_{on}} + V_B)$, i.e. $V_{in} > 4.7V$ diode $D_1$ is ON(as anode voltage is greater than cathode voltage) and hence circuit reduces to the circuit shown in figure 9

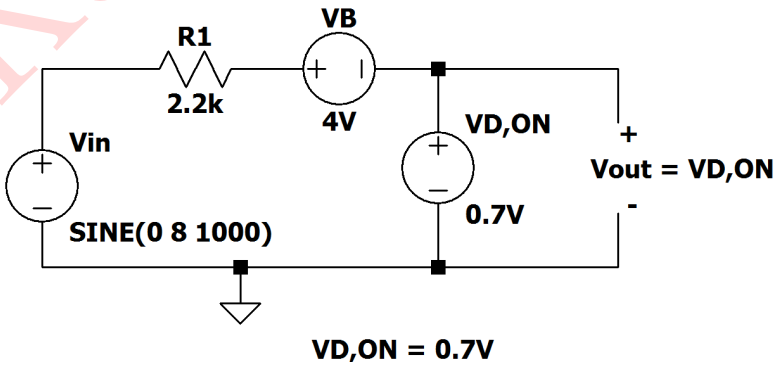


Figure 9: When diode is ON

$V_{out} = V_{D1_{on}} = 0.7V$

$\boldsymbol{V_{out} = 0.7V}$

$\rightarrow$ If $V_{in} < (V_{D1_{on}} + V_B)$, i.e. $V_{in} < 4.7V$ diode $D_1$ is OFF and hence circuit reduces to the circuit shown in figure 10

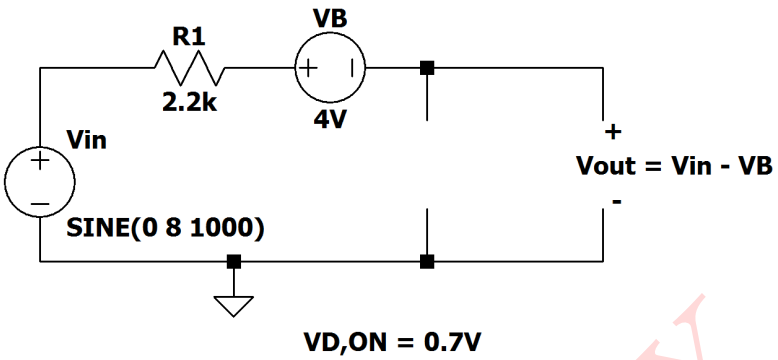


Figure 10: When diode is OFF

Applying KVL to the input loop:

$V_{in} - IR_1 - V_B - V_{out} = 0$

$V_{out} = V_{in} - V_B$

$V_{out} = V_{in} - 4$

Minimum value of $V_{out}$ is when $V_{in} = -8V$

$V_{out} = -8 - 4 = -12V$

$\therefore \boldsymbol{V_{out} = -12V}$

**SIMULATED RESULTS:**

Above circuit was simulated in LTSpice and results are presented below:

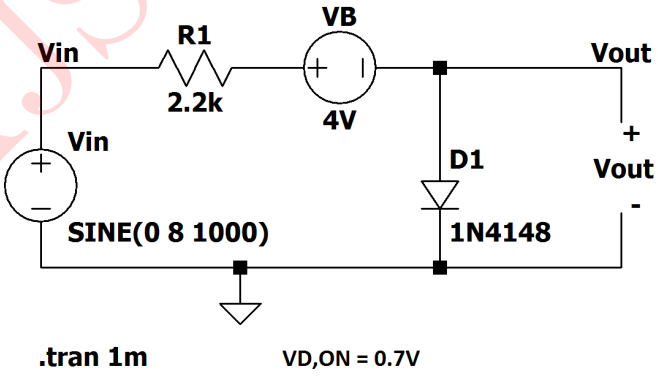


Figure 11: Circuit Schematic 2

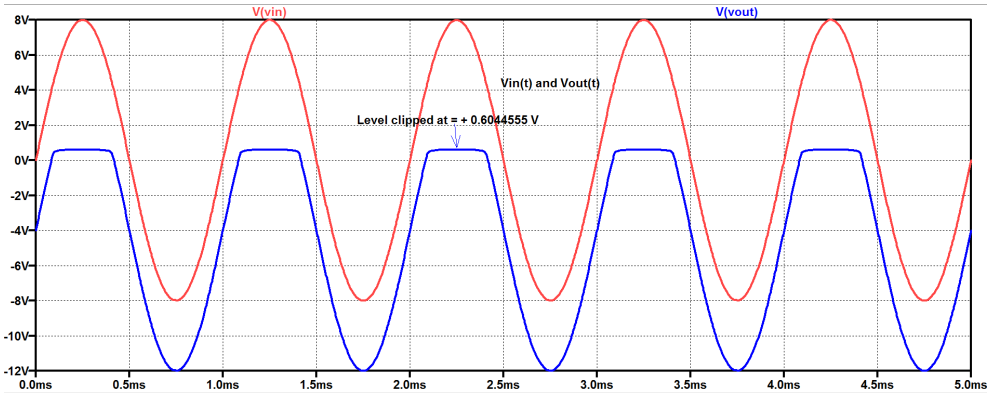


Figure 12: Input & Output waveform

**Comparison of Theoretical and Simulated Values:**

| Parameters | Theoretical | Simulated |
|---|---|---|
| Minimum level of clipped voltage | $0.7V$ | $0.604V$ |

Table 2: Question 2

**Numerical 3:**
For the circuit shown in figure 14, Plot: Input $V_{in}(t)$ and output $V_{out}(t)$ waveforms
Given: $V_{in}(t) = 16$ Vp-p square wave with frequency of 1000Hz. $C_1 = 10\mu$F, $R_1 = 10k\Omega$, diode $D_1$ is Silicon diode hence, $V_{D1_{ON}} = 0.7V$ & $V_B = 2.7V$

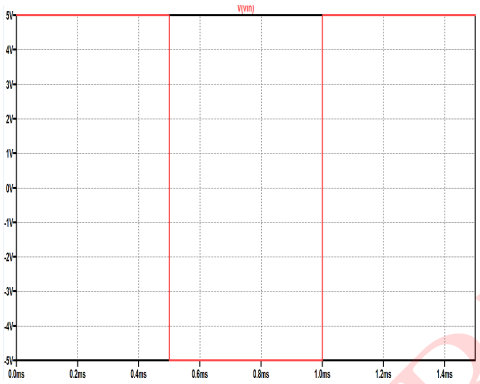

Figure 13: Input waveform

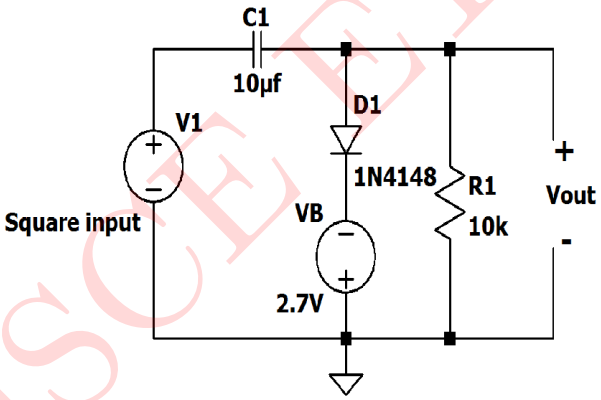


Figure 14: Circuit 3

**Solution:**

The given diode $D_1$ is silicon diode, hence $V_{D1_{ON}} = 0.7V$

Also, $V_{in} = 10$ Vp-p i.e. $V_{max} = 5V$

Assumptions:-

$RC = 10 \times 10^3 \times 10 \times 10^{-6} = 0.1s = 100ms$

Time period of input signal = 1ms

RC time constant is large enought(than time period of input signal) to source that voltage across capacitor does not discharge significantly during the period, The diode is OFF

→ If $V_{in} > (V_{D1_{ON}} - V_B)$, i.e. $V_{in} > -2V$ diode $D_1$ is ON(as anode voltage is greater than cathode voltage) and hence circuit reduces to the circuit shown in figure 15

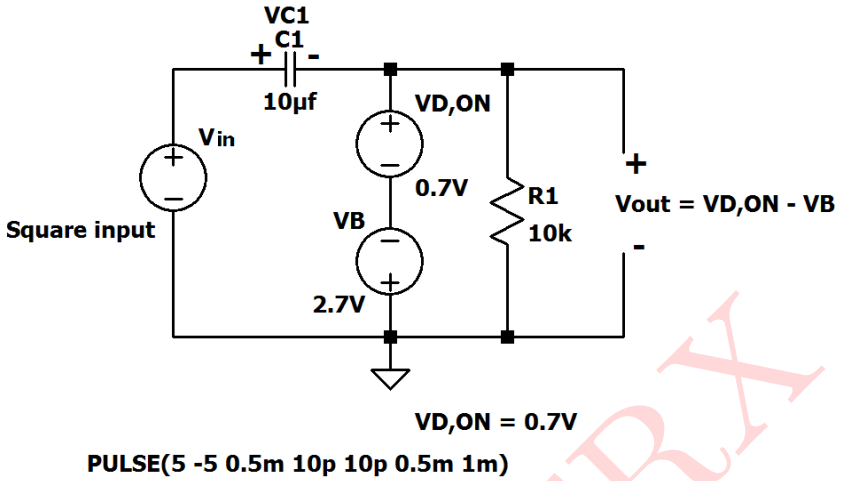


Figure 15: When diode is ON

$V_{out} = V_{D1_{ON}} - V_B = 0.7V - 2.7V = -2V$

$\boldsymbol{V_{out} = -2V}$

At the same time, $C_1$ charges and voltage across capacitor $V_{C_1}$ reaches upto $V_{max}$

Applying KVL to the input loop:-

$V_{in} - V_{C_1} - V_{D1_{on}} + V_B = 0$

$V_{C_1} = V_{in} - 0.7 + 2.7 = V_{max} + 2 = 5 + 2 = 7V$

i.e. Voltage across capacitor during positive half cycle

→ If $V_{in} < (V_{D1_{ON}} - V_B)$, i.e. $V_{in} < -2V$ diode $D_1$ is OFF and hence circuit reduces to the circuit shown in figure 16

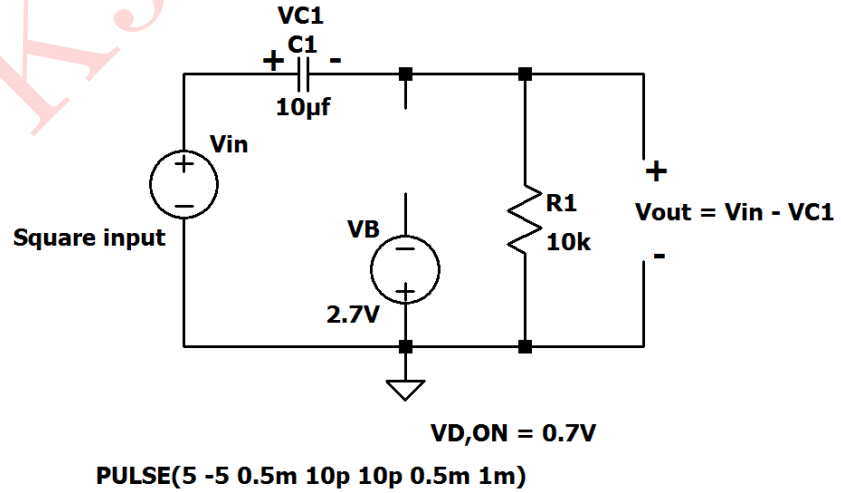


Figure 16: When diode is OFF

During negative half cycle, capacitor holds the charges, $V_{C_1} = 7V$ and act as battery

Applying KVL to the input loop:

$-V_{in} - V_{C_1} - V_{out} = 0$

$V_{out} = -V_{in} - V_{C_1}$

$V_{out} = -V_{in} - 7$

Minimum value of $V_{out}$ is when $V_{in} = -5V$

$V_{out} = -5 - 7 = -12V$

$\therefore \boldsymbol{V_{out} = -12V}$

**SIMULATED RESULTS:**

Above circuit was simulated in LTSpice and results are presented below:

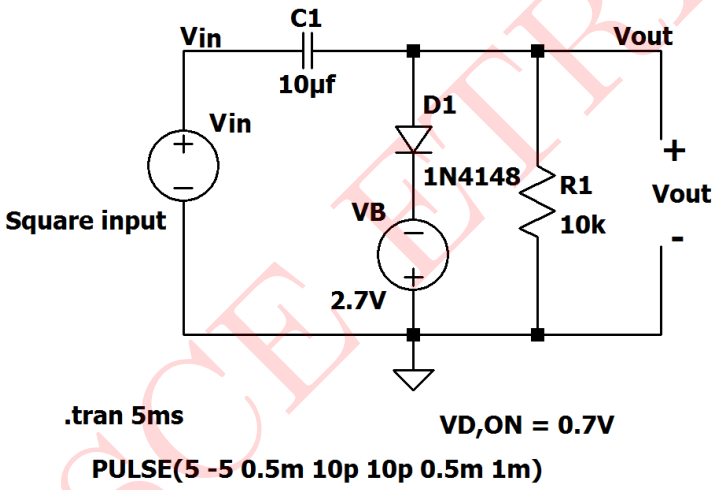


Figure 17: Circuit Schematic 3

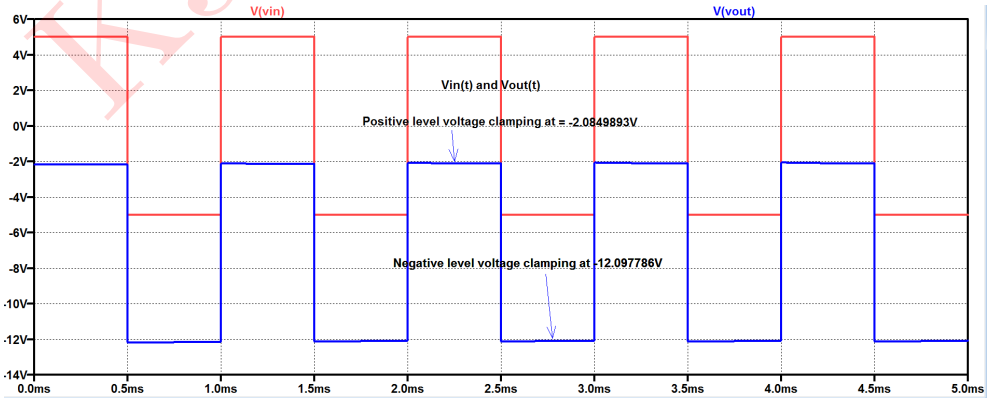


Figure 18: Input & Output waveform

Since, the output waveform is shifted down of the x-axis, the given circuit is negative clamper.

**Comparison of Theoretical and Simulated Values:**

| Parameters | Theoretical | Simulated |
|---|---|---|
| Positive level voltage clamping | $-2V$ | $-2.084V$ |
| Negative level voltage clamping | $-12V$ | $-12.09V$ |

Table 3: Question 3

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