K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
DIODE APPLICATION

29^{th} **June, 2020** **Numericals**

1. For the circuit shown in Figure 1, plot
   a) Input $V_{in}(t)$ and output $V_{out}(t)$ waveforms
   b) VTC curve
   Given: $V_{in}(t) = 10V_{p-p}$ sinusoidal signal with frequency 5000 Hz
   Use constant voltage model i.e. $V_{D,on} = 0.7$ V, $V_B = 1$ V, $R_1 = 1k\Omega$

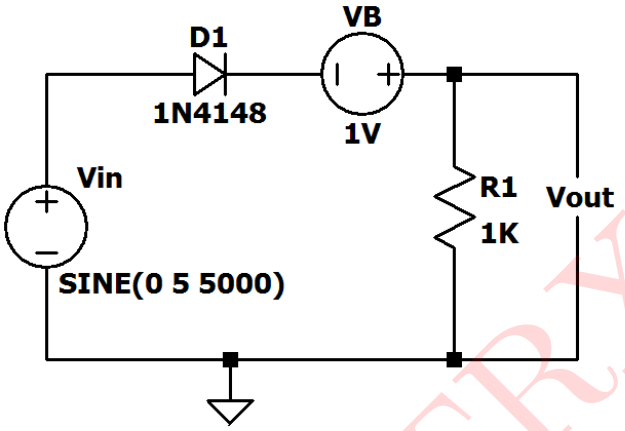

Figure 1: Clipper circuit

Solution:
$V_{in} = V_m sin\omega t = 5sin(2\pi 5000t) = 5sin(10000\pi t)$

Assuming a constant voltage model for D_1

Case 1: If $V_{in} > (V_{D,on} - V_B)$

i.e. $V_{in} > (0.7 - 1)$

i.e. $V_{in} > (-0.3)$

The diode D_1 is ON, hence Circuit 1 reduces to Circuit 2.

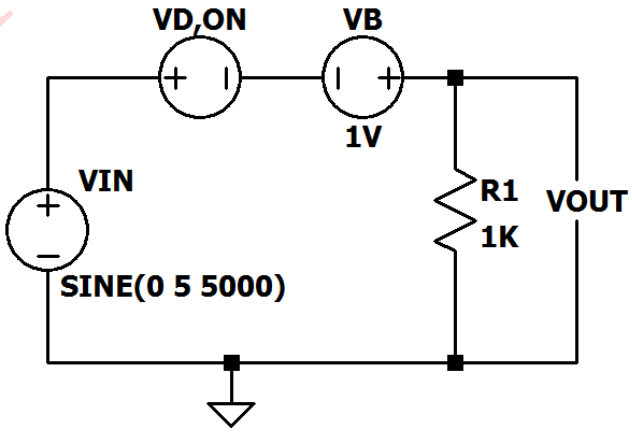

Figure 2: Circuit 2

Applying KVL,

$V_{in} - V_{D,on} + V_B - V_{out} = 0$

$\therefore V_{out} = V_{in} - (V_{D,on} - V_B)$

$\therefore V_{out} = 5 - (0.7 - 1) = 5.3$ V

$\therefore$ Output tracks input, but with a shift $(V_{D,on} - V_B)$

Case 2: If $V_{in} < (V_{D,on} - V_B)$

i.e $V_{in} < (0.7 - 1)$

i.e $V_{in} < (-0.3)$

The diode D_1 is OFF, hence the circuit reduces to Circuit 3.

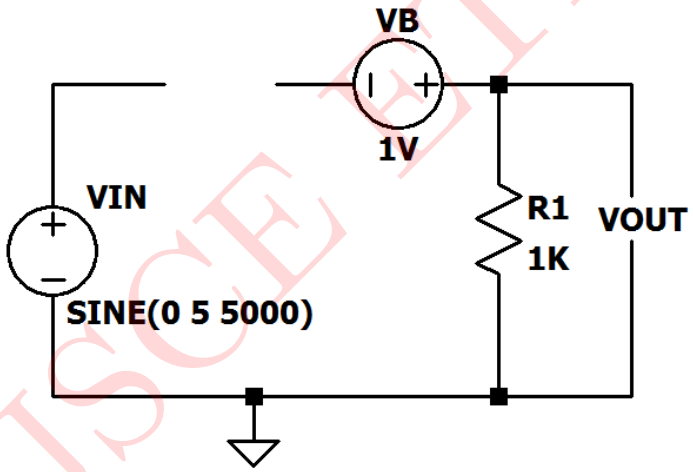

Figure 3: Circuit 3

In Circuit 3, we can observe that $V_{out} = 0$ V

SIMULATED RESULTS:
Above circuit is simulated using LTspice and the results are presented below:

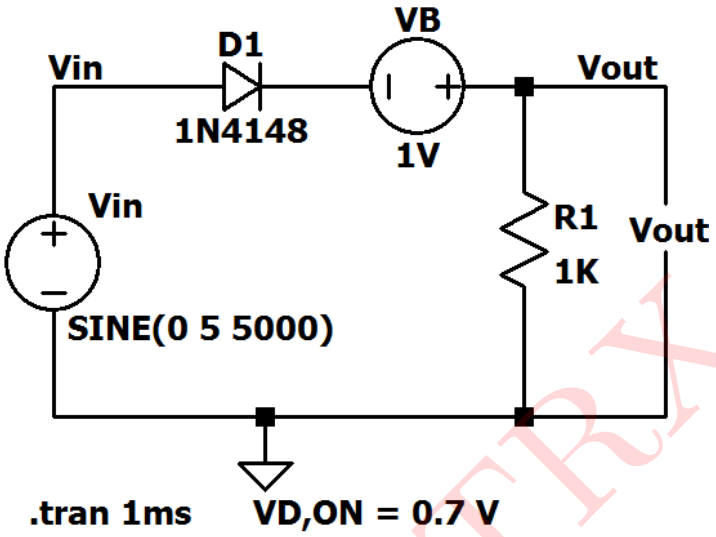

Figure 4: Circuit schematic

The input and output waveforms are shown in Figure 5.

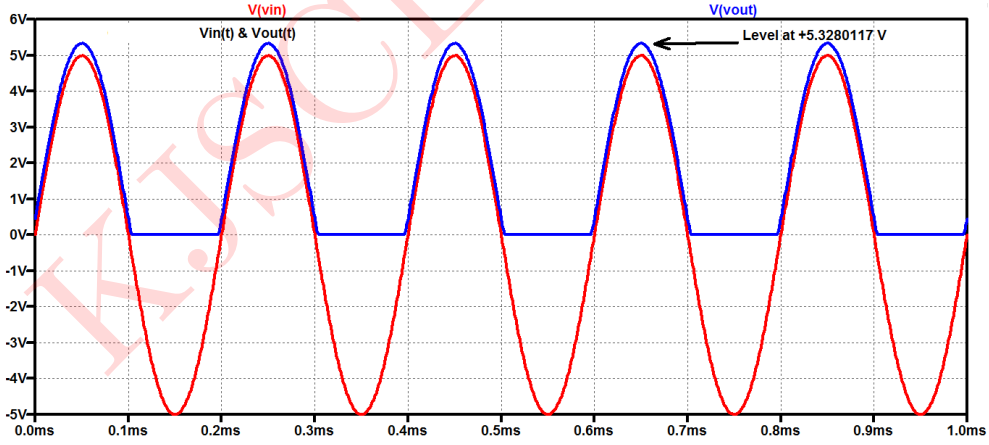

Figure 5: Input and output waveforms

The VTC curve is given below in Figure 6.

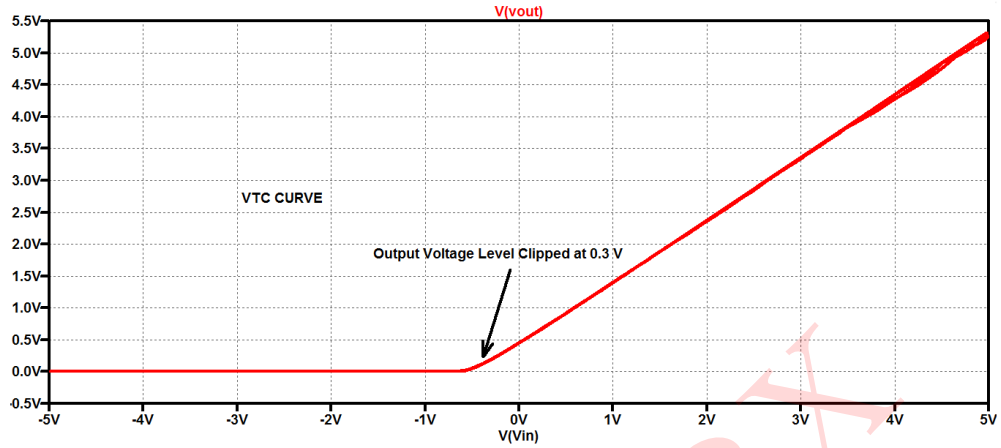

Figure 6: VTC curve

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
Level of clipped voltage	0.3 V	0.3280 V

Table 1: Table 1

2. For the circuit shown in Figure 7, plot input $V_{in}(t)$ and output $V_{out}(t)$ waveforms
Given: $V_{in}(t) = 20V_{p-p}$ square wave signal with frequency 1000 Hz and D_1 is a silicon diode

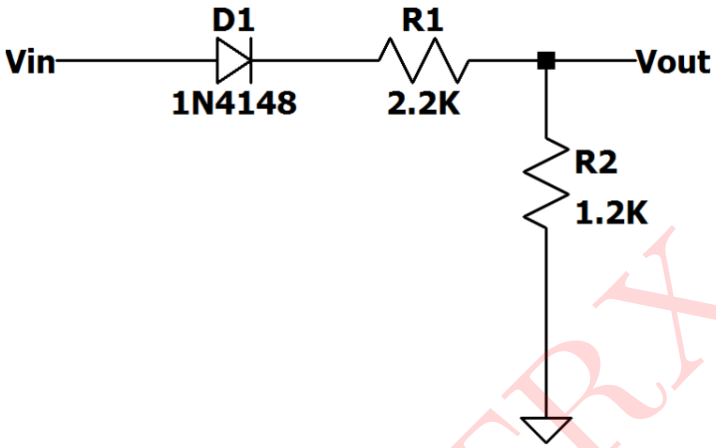

Figure 7: Clipper circuit

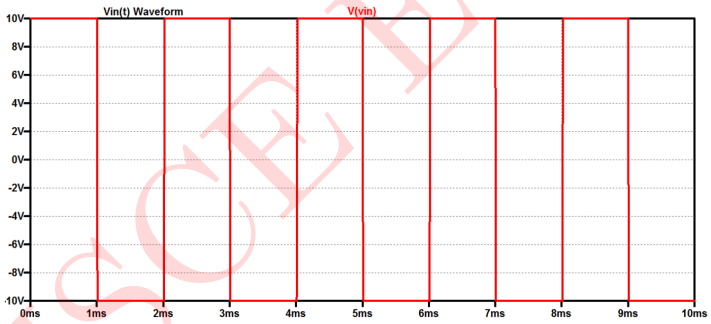

Figure 8: Input signal

Solution:
The given diode D_1 is a silicon diode, $\therefore V_{D,on} = 0.7$ V

$V_{in} = 20V_{p-p}$, $\therefore V_m = 10$ V

Case 1: When $V_{in} > (V_{D,on} - V_B)$

i.e. when $V_{in} > (0.7V)$, the diode D_1 is ON(because the anode voltage of the diode which is connected to V_{in} is greater than cathode voltage by 0.7, hence the diode will turn on)

$\therefore$ When $V_{in} > 0.7$ V, D_1 turns ON and the clipper circuit reduces to Circuit 4.
Applying KVL,

$$V_{in} - V_{D,on} - (I \times R_1) - (I \times R_2) = 0$$

$$\therefore I = \frac{V_{in} - V_{D,on}}{R_1 + R_2}$$

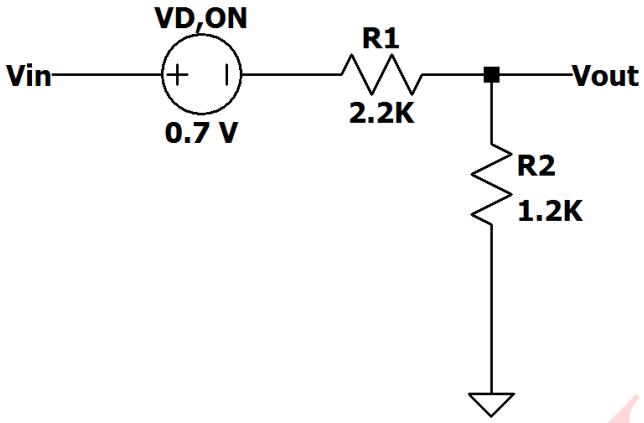

Figure 9: Circuit 4

$$\therefore I \times R_2 = V_{out} = \frac{V_{in} - V_{D,on}}{R_1 + R_2} \times R_2$$

$$\therefore V_{out} = \frac{10 - 0.7}{1.2k + 2.2k} \times 1.2k$$

$$\therefore V_{out} = 3.283 \text{ V}$$

Case 2: When $V_{in} < V_{D,on}$

i.e. when $V_{in} < 0.7$, the diode D_1 will be OFF

Hence the clipper circuit reduces to Circuit 5.

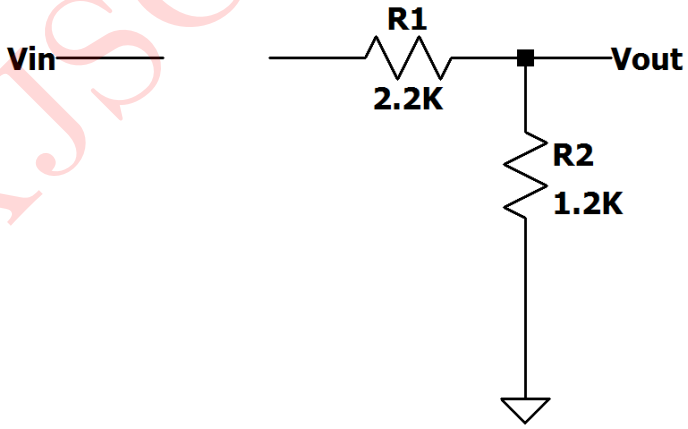

Figure 10: Circuit 5

In Circuit 5, we can observe that $V_{out} = 0$ V

SIMULATED RESULTS:
Above circuit is simulated using LTspice and the results are presented below:

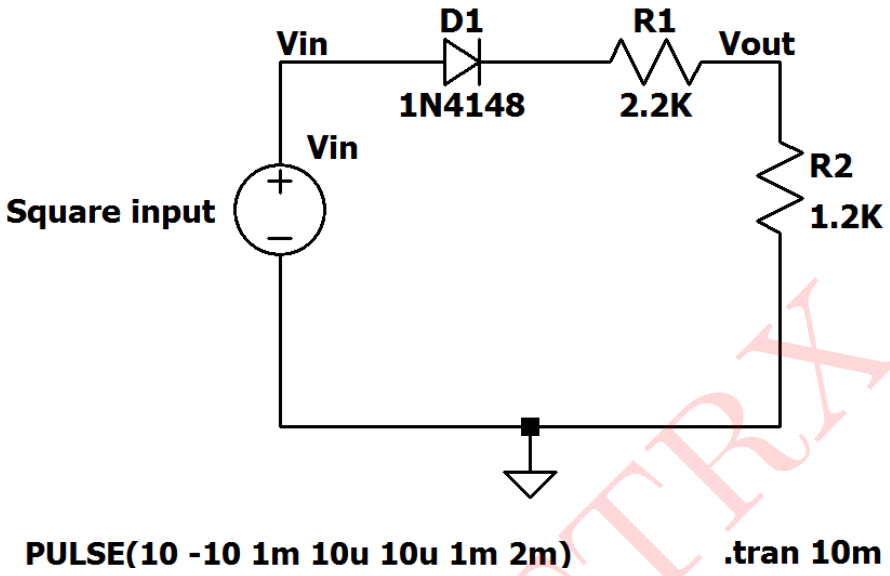

Figure 11: Circuit schematic

The input and output waveforms are shown in Figure 12.

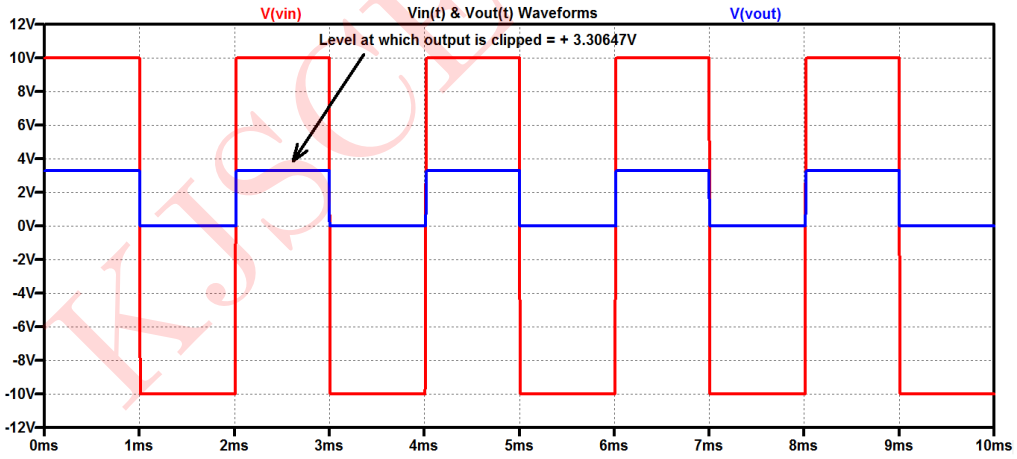

Figure 12: Input and output waveforms

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
Level of clipped voltage	3.283 V	3.30647 V

Table 2: Table 2

3. For the circuit shown in Figure 1, plot input $V_{in}(t)$ and output $V_{out}(t)$ waveforms
Given: $V_{in}(t) = 40V_{p-p}$ sinusoidal wave of frequency 1000 Hz
$C_1 = 10\mu F$ and $R_1 = 10k\Omega$
Diode D_1 is silicon diode, i.e. $V_{D,on} = 0.7$ V, $V_B = 10$ V DC

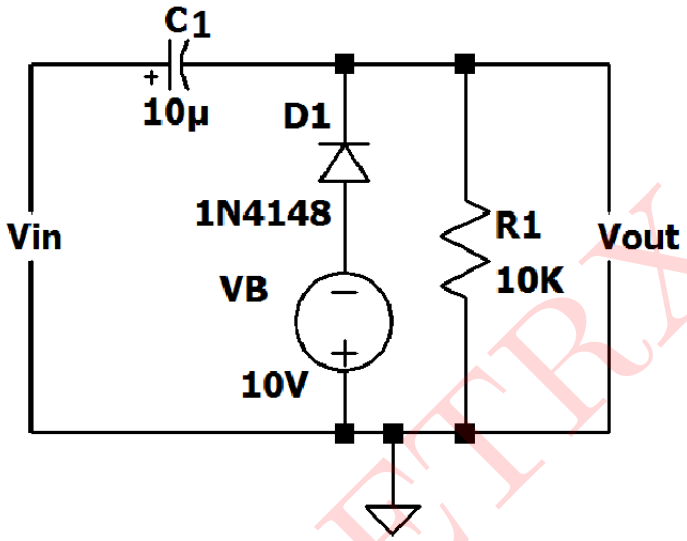

Figure 13: Clamper circuit

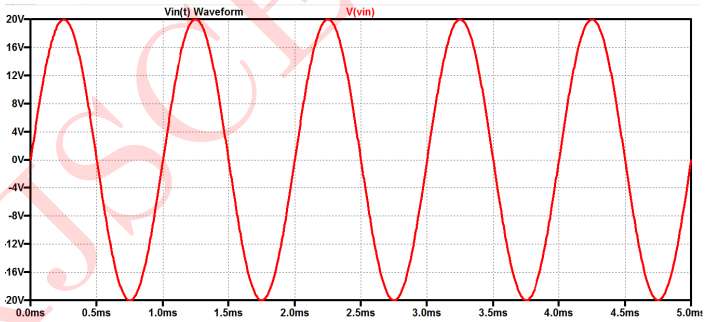

Figure 14: Input signal

Solution:
Since the given diode D_1 is a silicon diode, $\therefore V_{D,on} = 0.7$ V

Given: $V_{in} = 40V_{p-p}$, $\therefore V_m = 20$ V

Operation:
a) During negative half cycle, D_1 is ON.

When $V_{in} < (-V_{D,on} + V_B)$, i.e. $(-0.7 + 10)$ V, i.e. 9.3 V,
Figure 13 reduces to Figure 15.

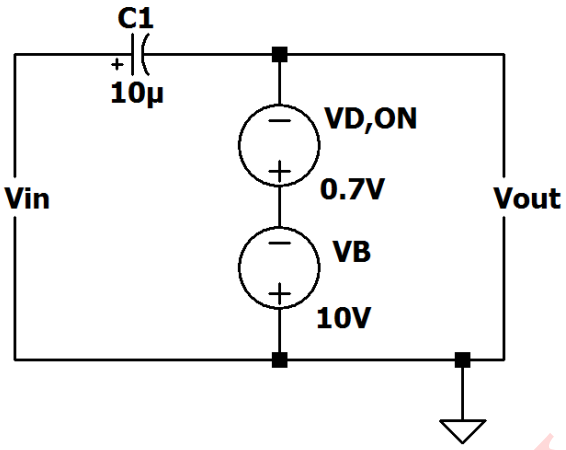

Figure 15: When diode D_1 is ON

Here, $V_{out} = -V_{D,on} - V_B = -0.7 - 10$

$\therefore V_{out} = -10.7$ V

b) At the same time, voltage across capacitor V_C changes to $-V_m$

Applying KVL,

$V_{in} - V_C - V_{D,on} + V_B = 0$

$\therefore V_C = V_{in} + V_{D,on} + V_B$ (for negative half cycle)

$\therefore V_C = -V_m + V_{D,on} + V_B = -9.3$ V

c) During positive half cycle, diode D_1 is OFF for the entire positive half cycle, hence Figure 13 reduces to Figure 16.

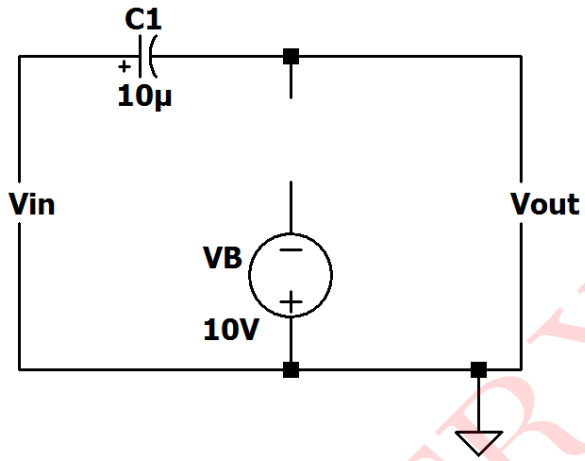

Figure 16: When diode D_1 is OFF

During positive half cycle, capacitor C_1 holds the charge $V_C = -9.3$ V and acts as a battery.

Applying KVL,

$V_{in} - V_C - V_{out} = 0$

$\therefore V_{out} = V_{in} - V_C$

$\therefore V_{out} = 20 - (-9.3) = 29.3$ V (for positive half cycle)

SIMULATED RESULTS:
Above circuit is simulated using LTspice and the results are presented below:

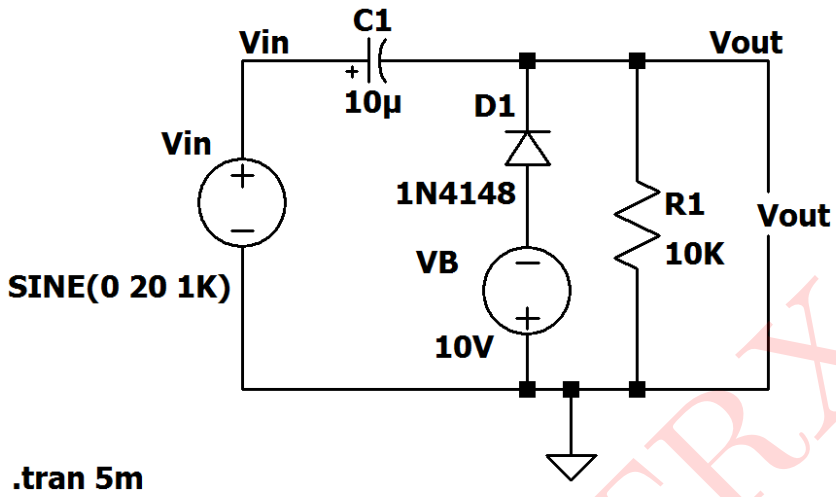

Figure 17: Circuit schematic

The input and output waveforms are shown in Figure 18.

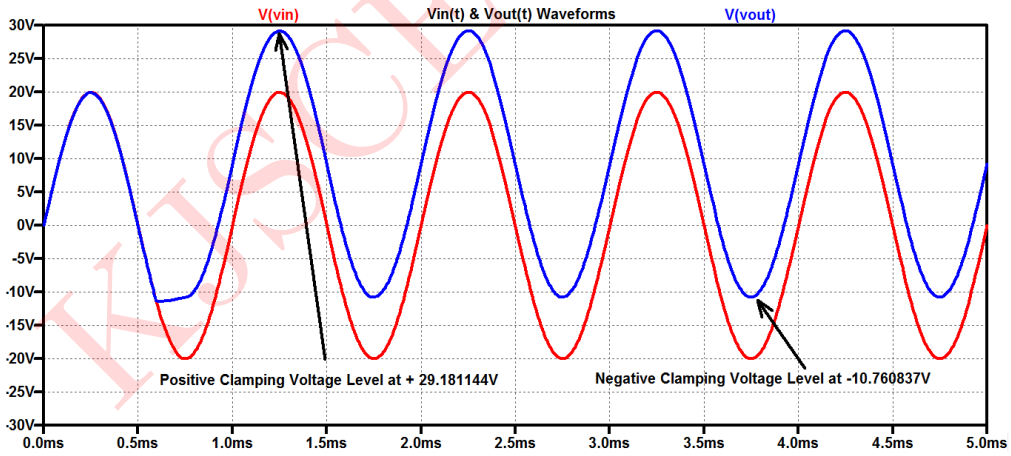

Figure 18: Input and output waveforms

The output waveform is shifted above the axis, hence the circuit is a biased positive clamper.

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
Positive clamping voltage level	29.3 V	29.18114 V
Negative clamping voltage level	-10.7 V	-10.76083 V

Table 3: Table 3