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DESIGN OF SINGLE STAGE AMPLIFIER

 25^{th} June, 2020 Numerical

1. Design a single stage RC coupled BJT amplifier for following specifications:

$$V_{o_{rms}} = 5 \text{ V}, f_L \le 20 \text{ Hz}, S \le 10, |A_V| \ge 120$$

Calculate A_V , Z_i and Z_o of the amplifier you have designed

Solution:

Step 1: Given data

$$V_{o_{rms}}=5$$
 V, $f_L\leq 20$ Hz, S \leq 10, $|A_V|\geq 120$

Step 2: Selection of transistor

Transistor selected is BC147B with following specifications:

$$h_{FE}(min) = 200$$

$$h_{FE}(typ) = 290$$

$$h_{FE}(max) = 450$$

$$h_{ie} = 4.5 \text{ k}\Omega$$

$$h_{fe}(min) = 240$$

$$h_{fe}(typ) = 330$$

$$h_{fe}(max) = 500$$

$$\dot{V}_{CE}(sat) = 0.25 \text{ V}$$

Step 3: Selection of biasing network

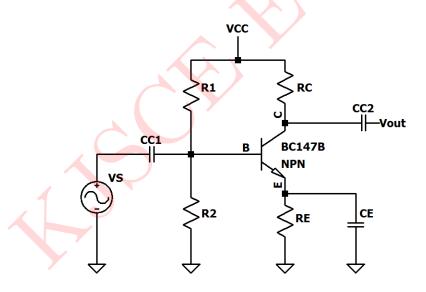


Figure 1: Circuit 1

Step 4: Selection of R_L

$$|A_V| = \frac{h_{fe}(min) \times R_C}{h_{ie}}$$

$$\therefore 120 = \frac{240 \times R_C}{4.5k}$$

$$\therefore R_C = 2.25 \text{ k}\Omega$$

We select a higher standard value of R_C to increase the gain.

Hence, we select $R_C = 2.4 \text{ k}\Omega, \frac{1}{4}W$

Step 5: Selection of Q-point (V_{CEQ}, I_{CQ})

If V_{CC} is not given, we take $V_{CEQ} \ge 1.5 \times [V_{o_{peak}} + V_{CE}(sat)]$

$$V_{o_{neak}} = V_{o_{rms}} \times \sqrt{2} = 5\sqrt{2} = 7.07106 \text{ V}$$

$$V_{CEQ} \ge 1.5 \times [7.07106 + 0.25]$$

$$\therefore V_{CEQ} \ge 10.98159 \text{ V}$$
, i.e. $V_{CEQ} = 11 \text{ V}$

$$I_{o_{peak}} = \frac{V_{o_{peak}}}{R_C} = \frac{7.07106}{2.4k} = 2.946 \text{ mA}$$

 $I_{CQ} \geq I_{o_{peak}}$ (for undistorted output signal)

$$I_{CQ} \ge 2.946 \text{ mA}, \therefore I_{CQ} = 3 \text{ mA}$$

Step 6: Selection of DC power supply (V_{CC})

Selecting Q-point at center of DC load line for maximum output swing

$$V_{CC} \ge 2V_{CEQ} \ge 2 \times 11 \text{ V}$$

$$V_{CC} \ge 22 \text{ V}$$

Selecting HSV, $V_{CC} = 23 \text{ V}$

Step 7: Calculation of R_E

For proper operation, $V_{RE} = 10\%$ of $V_{CC} = 0.1V_{CC}$

$$\therefore V_{RE} = 2.3 \text{ V}$$

$$V_{RE} = R_E \times I_{EQ}$$

$$\therefore R_E = \frac{V_{RE}}{I_{EQ}} = \frac{V_{RE}}{I_{CQ}} = \frac{2.3}{3 \times 10^{-3}} = 766.667 \text{ k}\Omega$$

Step 8: Calculation of biasing resistors R_1 and R_2

$$S = \frac{1+\beta}{1+\beta \left(\frac{R_E}{R_E + R_B}\right)}$$

$$\beta = h_{fe}(max) = 450$$

$$10 = \frac{1 + 450}{1 + 450 \left(\frac{680}{680 + R_B}\right)}$$

$$V_{th} = V_B = \frac{R_2}{R_1 + R_2} \times V_{CC} \qquad \dots (2)$$

Applying KVL at B-E loop of Q_1

$$V_B - I_{BQ}R_B - V_{BE} - I_{EQ}R_E = 0$$

$$V_B = V_{BE} + \left(\frac{I_{CQ}}{\beta} \times R_B\right) + I_{CQ}R_E$$

$$V_B = 0.7 + \frac{3 \times 10^{-3}}{450} \times 6258.775 + (3 \times 10^{-3} \times 680)$$

$$V_B = 2.781725 \text{ V}$$

From equation (2),
$$V_B = 2.7817 = \frac{R_2}{R_1 + R_2} \times 23$$

$$\therefore \frac{R_2}{R_1 + R_2} = 0.12094$$

: Equation (1) becomes: $R_! \times 0.12094 = 6258.7755$

$$\therefore R_1 = 51.75 \text{ k}\Omega$$

Selecting HSV so that circuit draws minimum current

$$\therefore R_1 = 56 \text{ k}\Omega, \frac{1}{4}W$$

$$\therefore \frac{R_2}{56k + R_2} = 0.12094$$

$$\therefore R_2 = 7.704 \text{ k}\Omega$$

Selecting LSV, $R_2 = 7.5 \text{ k}\Omega, \frac{1}{4}W$

Step 9: Selection of bypass capacitor C_E

$$X_{CE} = \frac{R_E}{10} = 0.1R_E$$

$$\therefore \frac{1}{2\pi f_L C_E} = 0.1 R_E$$

$$\therefore C_E = \frac{1}{2\pi f_L \times 0.1 \times R_E} = \frac{1}{2\pi \times 20 \times 0.1 \times 680} = 117.02569 \ \mu\text{F}$$

Selecting HSV, $C_E=120~\mu\mathrm{F}$ /25 V

Step 10: Selection of coupling capacitor

a)
$$C_{C1} = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = R_1 ||R_2||h_{ie} = 56k||7.5k||4.5k$$

$$\therefore R_{eq} = 2.6779 \text{ k}\Omega$$

$$C_{C1} = \frac{1}{2\pi \times 2.6779 \times 10^3 \times 20} = 2.9716 \mu F$$

Selecting HSV, $C_{C1} = 3.3 \mu F / 25 V$

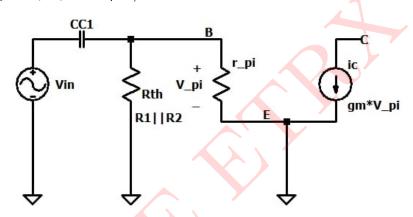


Figure 2: Low frequency equivalent circuit for C_{C1}

b)
$$C_{C2} = \frac{1}{2\pi R_{eq} f_L} = \frac{1}{2\pi R_C f_L}$$

$$\therefore C_{C2} = \frac{1}{2\pi \times 2.4 \times 10^3 \times 20} = 3.3157 \mu F$$

Selecting HSV, $C_{C2} = 3.9 \mu F / 25 V$

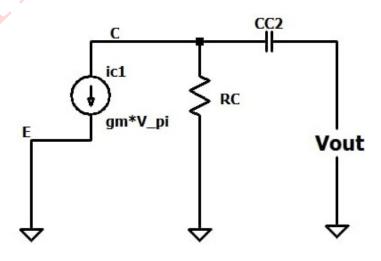


Figure 3: Low frequency equivalent circuit for C_{C2}

Small-signal analysis:

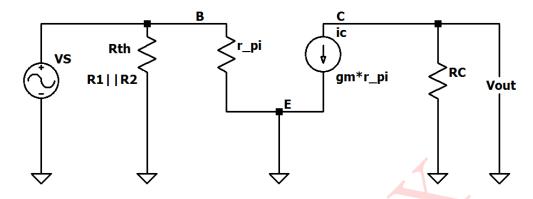


Figure 4: Small-signal equivalent circuit

Small-signal parameters:

$$g_m = \frac{I_{CQ}}{V_T} = \frac{3mA}{26mV} = 115.38 \frac{mA}{V}$$

Verification of gain A_V :

$$A_V = -g_m R_C = -115.38 \frac{mA}{V} \times 2.4 \text{ k}\Omega$$

$$A_V = -276.912$$

$$Z_i = R_1 ||R_2|| r_\pi = 2.677 \text{ k}\Omega$$

$$Z_o = R_C = 2.4 \text{ k}\Omega$$

The complete designed circuit is shown in Figure 4.

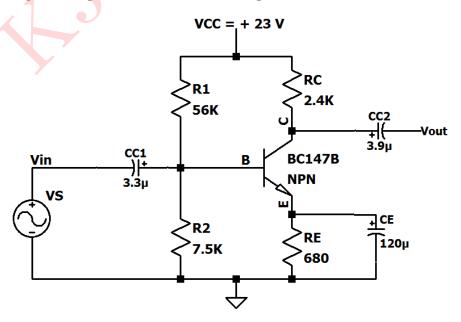
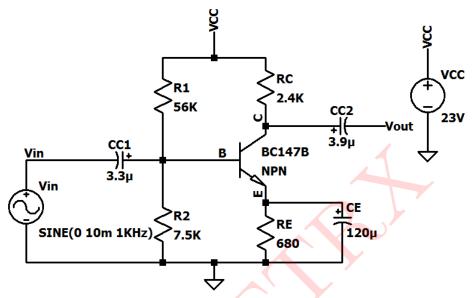


Figure 5: Designed circuit

SIMULATED RESULTS:

Above circuit is simulated using LTspice and the results are presented below:



.op .tran 5ms .model NPN NPN(is=6.734E-14 bf=450 cjc=6pf cje=12pf)

Figure 6: Circuit schematic

The input and output waveforms for are shown in Figure 7.

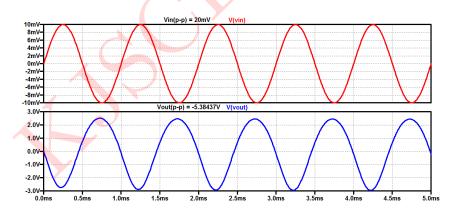


Figure 7: Circuit schematic

Comparison of theoretical and simulated values:

Parameters	Theoretical	Simulated
Voltage gain $ A_V $	≥ 120	269.218
I_{CQ}	3 mA	2.8 mA

Table 1: Numerical 1