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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Cascode Amplifier

12^{th} **July, 2020**

Numerical 1:
Consider cascode circuit as shown in figure 1, let $\beta = 100$, $V_{BE(ON)} = 0.7V$ and $V_A = \infty$ for each transistor. Given: $V_{CC} = 9V$ and $R_L = 10k\Omega$
Find DC parameters, A_{V1}, A_{V2}, Z_i and Z_o

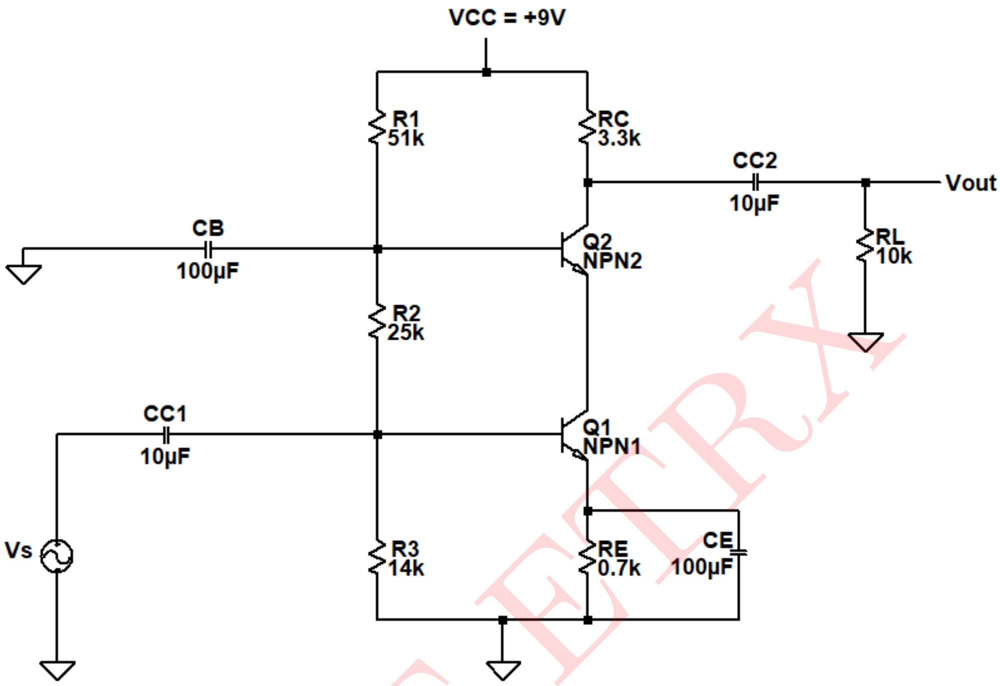

Figure 1: Circuit diagram

Solution: Circuit shown in figure 1 is a CE-CB cascode amplifier.

DC Analysis: All capacitors are open circuited and DC equivalent circuit is shown in figure 2:

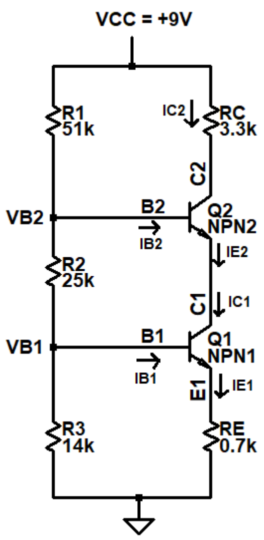

Figure 2: DC equivalent circuit

For stage 1:

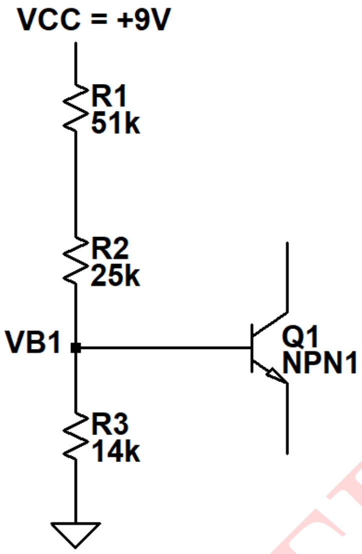

Figure 3: Stage 1 DC equivalent circuit

$$V_{B1} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{CC}$$

$$\therefore V_{B1} = \frac{14k\Omega}{51k\Omega + 25k\Omega + 14k\Omega} \times 9$$

$$\therefore V_{B1} = 1.4V$$

$V_{BE1} = 0.7V$ ...(given)

$$\therefore V_{BE1} = V_{B1} - V_{E1}$$

$$\therefore V_{E1} = V_{B1} - V_{BE1} = 1.4 - 0.7$$

$$\therefore V_{E1} = 0.7V$$

Also, $I_{E1} = \frac{V_{E1}}{R_E}$

$$\therefore I_{E1} = \frac{0.7}{0.7k\Omega} = 1\text{mA}$$

$$\therefore I_{B1} = I_{B2} = \frac{I_{E1}}{(1+\beta)}$$

$$\therefore I_{B1} = I_{B2} = 9.9\mu A$$

Assuming I_{B1}, I_{B2} very small and $I_{E1} \approx I_{E2} \approx I_{C1} \approx I_{C2}$

$$\therefore I_{E1} = I_{E2} = I_{C2} = I_{C1} = 1mA$$

For Stage 2:

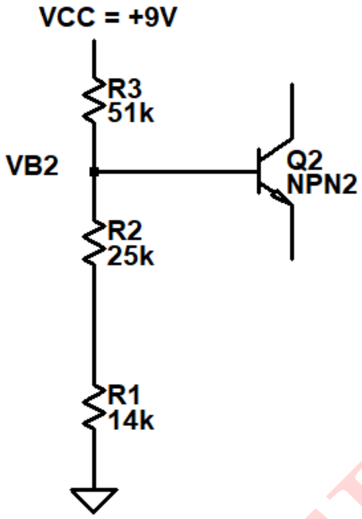

Figure 4: Stage 2 DC equivalent circuit

$$V_{B2} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{CC}$$

$$\therefore V_{B2} = \frac{25k\Omega + 14k\Omega}{51k\Omega + 25k\Omega + 14k\Omega} \times 9$$

$$\therefore V_{B2} = 3.9V$$

$V_{BE2} = 0.7V$ ...(given)

$$V_{BE2} = V_{B2} - V_{E2}$$

$$\therefore V_{E2} = V_{B2} - V_{BE2} = 3.9 - 0.7$$

$$\therefore V_{E2} = 3.2V$$

Applying KCL to C-E loop of stage 2:

$$V_{C2} = V_{CC} - I_{C2}R_C$$

$$\therefore V_{C2} = 9 - (1mA)(3.3k\Omega)$$

$$V_{C2} = 5.7V$$

Small signal parameters:

$$r_\pi = \frac{\beta V_T}{I_{CQ}} \quad ...(\text{assuming } r_{\pi1} = r_{\pi2} = r_\pi)$$

$$r_\pi = \frac{100 \times 26mV}{1mA}$$

$$r_\pi = 2.6k\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} \quad ...(\text{assuming } g_{m1} = g_{m2} = g_m)$$

$$\therefore g_m = \frac{1}{26} = 38.4615 \text{ mA/V}$$

Small signal equivalent circuit is shown in figure 5:

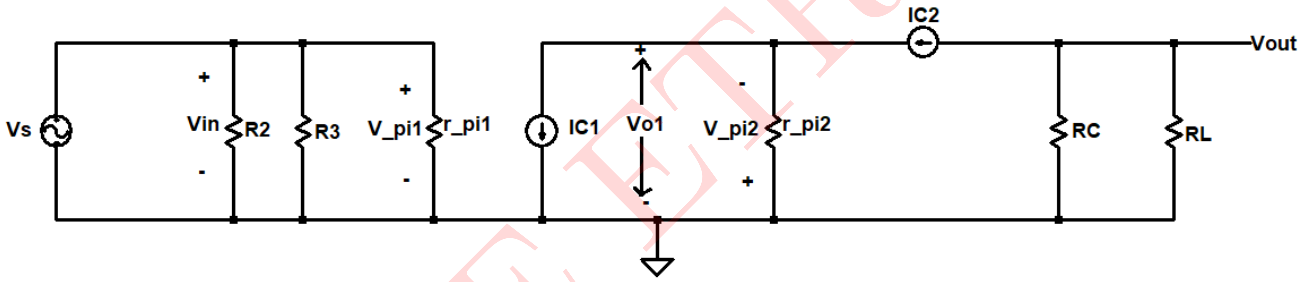

Figure 5: Small signal equivalent circuit

All capacitors are short-circuited.

For Stage 1: $A_{V1} = \dfrac{V_{o1}}{V_s}$

Here, $V_s = V_{in}$

$$V_{o1} = -g_{m1} V_{\pi1} \frac{r_{\pi2}}{(1+\beta)}$$

$(1+\beta)$ is due to resistance reflection rule which states that resistance looking into the base is $(1+\beta)$ times the total emitter resistance.

$$\therefore A_{V1} = \frac{-g_{m1} V_{\pi1} r_{\pi2}}{V_{\pi1}(1+\beta)} = \frac{-g_{m1} r_{\pi2}}{(1+\beta)} \quad ...(\because V_{in} = V_{\pi1})$$

$$\therefore A_{V1} = -38.4615mA \times \frac{2.6k\Omega}{101}$$

$$\therefore A_{V1} = -0.9901 \approx 1$$

For stage 2: $A_{V2} = \dfrac{V_{out}}{V_s}$

$$V_{out} = -g_{m2} V_{\pi2} (R_C \parallel R_L)$$

$$V_{o1} = -V_{\pi2}$$

$$\therefore A_{V2} = \frac{-g_{m2} V_{\pi2}(R_C \parallel R_L)}{-V_{\pi2}} = g_{m2}(R_C \parallel R_L)$$

$\therefore A_{V2} = (38.4615 \times 10^{-3})(3.3k\Omega \parallel 10k\Omega) = (38.4615 \times 10^{-3})(2.4812k\Omega)$

$\therefore A_{V2} = 95.4308$

$\therefore$ Overall gain $= A_{Vt} = A_{V1} \times A_{V2}$

$\therefore A_{Vt} = (-1)(95.4308)$

$\therefore \mathbf{A_{Vt} = -95.4308}$

A_{Vt} (in dB) $= 20\log_{10}(95.4308) =$ **39.5938**

Input impedance:
$Z_i = R_2 \parallel R_3 \parallel r_{\pi 1} = 25k\Omega \parallel 14k\Omega \parallel 2.6k\Omega$

$\therefore \mathbf{Z_i = 2.0160k\Omega}$

Output Impdeance:
$Z_o = R_C \parallel R_L = 3.3k\Omega \parallel 10k\Omega$

$\therefore \mathbf{Z_o = 2.4812k\Omega}$

Output Voltage $= V_{in} \times A_{Vt}$
$\therefore V_{out} = (10mV)(-95.4308)$

$\therefore V_{out} = -0.9543V$

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

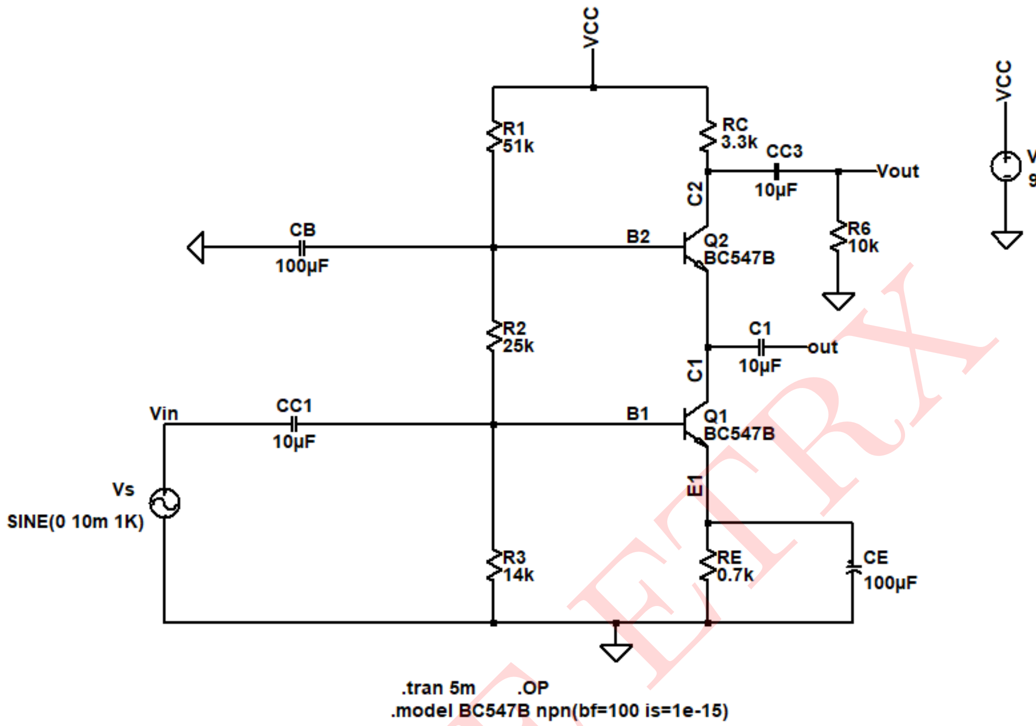

Figure 6: Circuit Schematic: Results

Input and output waveforms for each stage are shown below:

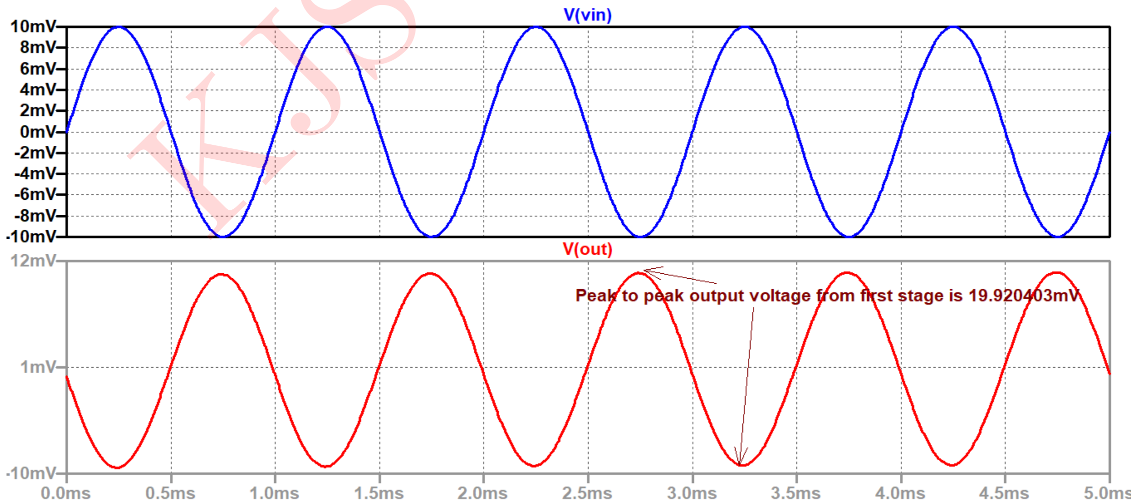

Figure 7: Input and output waveform for Stage 1

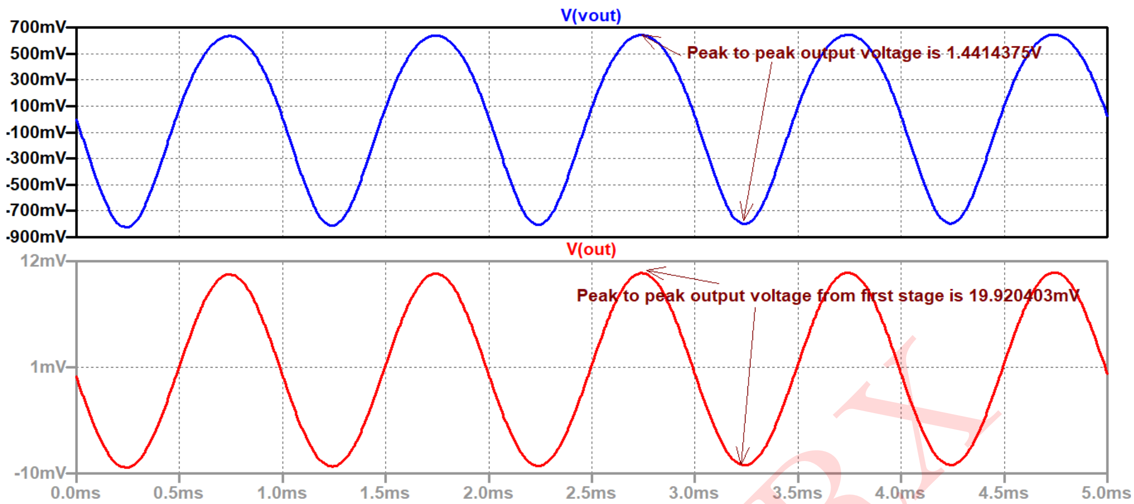

Figure 8: Input and output waveform for Stage 2

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
V_{B1}	1.4V	1.2493V
V_{C1}	3.2V	2.9046V
V_{E1}	0.7V	0.5415V
I_{C1}	1mA	0.7660mA
I_{B1}	$9.9\mu A$	$7.6596\mu A$
I_{E1}	1mA	0.7660 mA
V_{B2}	3.9V	3.67164V
V_{C2}	5.7V	6.4975V
V_{E2}	3.2V	2.9046V
I_{C2}	1mA	0.7660mA
I_{B2}	$9.9\mu A$	$7.5837\mu A$
I_{E2}	1mA	0.7660 mA
Voltage gain of stage 1: A_{V1}	-1	-0.996
Voltage gain of stage 2: A_{V2}	95.4308	72.075
Overall gain: A_{Vt} in dB	39.5938	37.1557
Input impedance of Stage 1	2.0160 kΩ	–
Output impedance of Stage 2	2.4812 kΩ	–
Output voltage	$-0.9543V$	$-0.7207V$

Table 1: Numerical 1

Numerical 2:
Consider CS-CG cascode amplifier as shown in figure 9. Let $k_{n1} = k_{n2} = 0.8mA/V^2$ & $V_{TN1} = V_{TN2} = 0.8V$; Determine:
a. DC parameters of the circuits i.e. V_{G1}, V_{S1}, V_{D1}, V_{GS1}, I_{D1}, V_{G2}, V_{S2}, V_{D2}, V_{GS2} & I_{D2}
b. Calculate input impedance of the circuit.
c. Calculate output impedance of the circuit.
d. Calculate voltage gain of the two stage circuit.

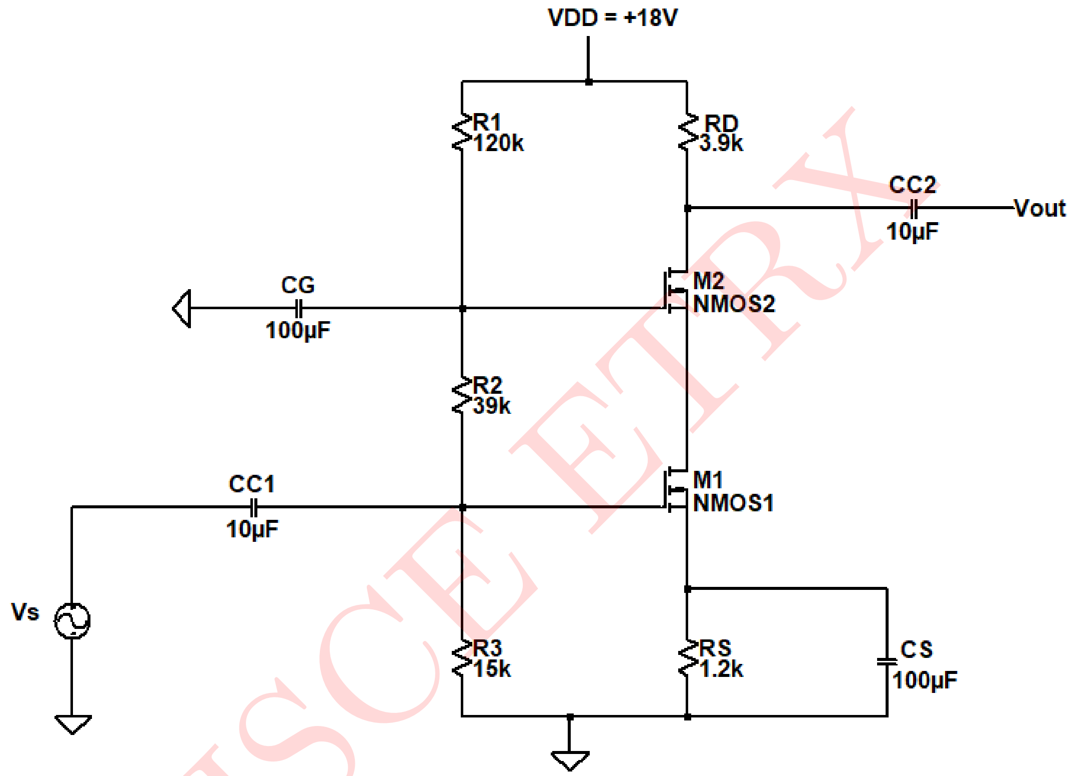

Figure 9: Circuit diagram

Solution: Circuit shown in figure 9 is a CS-CG cascade amplifier.

a. DC Analysis:
All capacitors are open circuited and DC equivalent circuit is shown in figure 10:

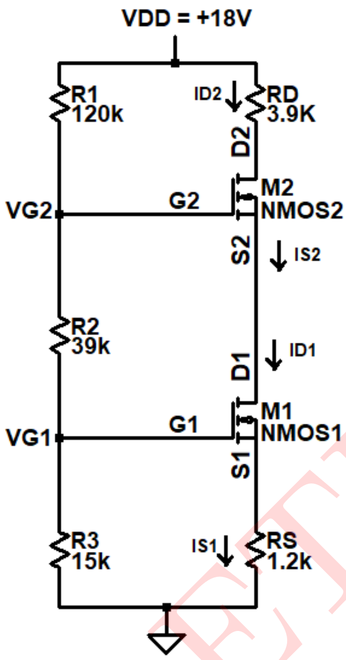

Figure 10: DC equivalent circuit

For stage 1:

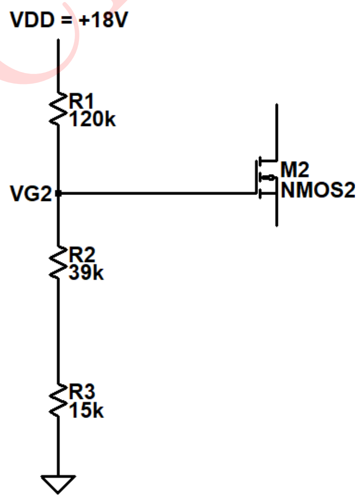

Figure 11: Stage 1 DC equivalent circuit

$$V_{G1} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{DD} = \frac{15k\Omega \times 18}{120k\Omega + 39k\Omega + 15k\Omega}$$

$\therefore \mathbf{V_{G1} = 1.5517V}$

For Stage 2:

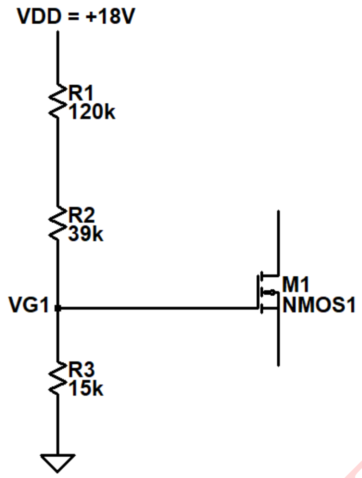

Figure 12: Stage 2 DC equivalent circuit

$$V_{G2} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{DD} = \frac{89k\Omega + 15k\Omega}{120k\Omega + 39k\Omega + 15k\Omega} \times 18$$

$\therefore \mathbf{V_{G2} = 5.5862V}$

$V_{GS1} = V_{G1} - V_{S1}$

$V_{S1} = R_S I_{D1} = (1.2k\Omega)I_{D1}$

$\therefore V_{GS1} = 1.5517 - (1.2k\Omega)I_{D1}$

$$\therefore I_{D1} = \frac{1.5517 - V_{GS1}}{1.2k\Omega} \qquad ...(1)$$

Assuming MOSFET in saturation, $I_{D1} = k_{n1}(V_{GS1} - V_{TN1})^2$

$\because k_{n1} = k_{n2} = k_n$, $V_{TN1} = V_{TN2} = V_{TN}$ and $V_{GS1} = V_{GS2} = V_{GS}$

$\therefore I_{D1} = (0.8 \times 10^{-3}[V_{GS} - 0.8]^2)$

$$\therefore \frac{1.5517 - V_{GS}}{1.2k\Omega} = (0.8 \times 10^{-3})[V_{GS} - 0.8]^2$$

$1.5517 - V_{GS} = 0.96[V_{GS}^2 + 0.64 - 1.6V_{GS}]$

$1.5517 - V_{GS} = 0.96V_{GS}^2 + 0.6144 - 1.536V_{GS}$

$\therefore 0.96V_{GS}^2 - 0.586V_{GS} - 0.9373 = 0$

$\therefore V_{GS} = 1.3060V, -0.7464V$

Since $V_{GS} > V_{TN}$

$\therefore \mathbf{V_{GS} = 1.3060V}$

Using (1), $I_{D1} = \dfrac{1.5517 - 1.3060}{1.2k\Omega}$

$\therefore \mathbf{I_{D1} = 0.20475mA}$

$\therefore \mathbf{I_{D1} \approx I_{D2} = 0.20475mA}$

$\therefore V_{S1} = I_D(R_S) = (0.20475mA)(1.2k\Omega)$

$\therefore \mathbf{V_{S1} = 0.2457V}$

Also, $V_{D2} = V_{DD} - I_{D2}R_D = 18 - (0.20475mA)(3.9k\Omega)$

$\therefore \mathbf{V_{D2} = 17.2015V}$

$V_{GS2} = V_{G2} - V_{S2}$

$\therefore V_{S2} = V_{G2} - V_{GS2}$

$V_{S2} = 5.5862 - 1.3060$

$\mathbf{V_{S2} = 4.2802V}$

Also, $\mathbf{V_{S2} = V_{D1} = 4.2802V}$

$\therefore V_{DS1} = V_{D1} - V_{S1} = 4.2802 - 0.2457$

$\therefore \mathbf{V_{DS1} = 4.0345V}$

$\therefore V_{DS2} = V_{D2} - V_{S2} = 17.2015 - 4.0802$

$\therefore \mathbf{V_{DS2} = 12.9213V}$

Small signal parameters:
$g_{m1} = g_{m2} = g_m$

$g_m = 2k_n[V_{GS} - V_{TN}]$

$g_m = 2(0.8 \times 10^{-3})[1.3060 - 0.8]$

$g_m = 1.6 \times 10^{-3}[1.3060 - 0.8]$

$\therefore g_m = 0.8096mA/V$

Small signal equivalent circuit is shown in figure 13:

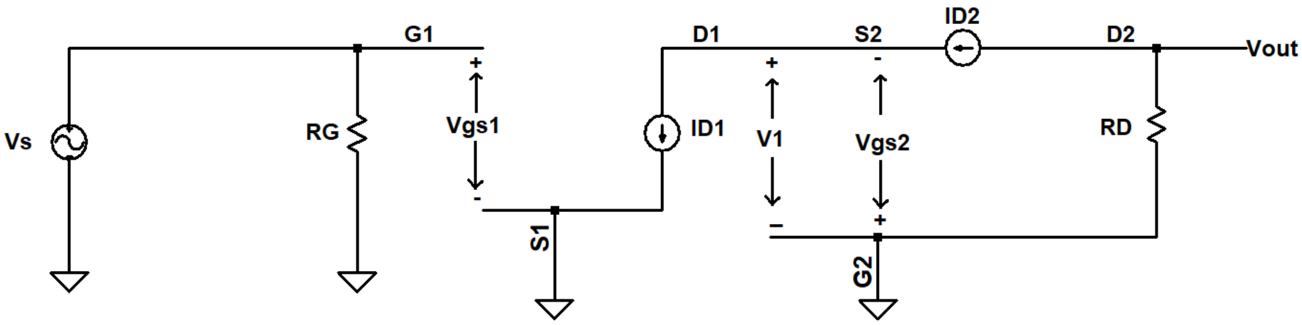

Figure 13: Small signal equivalent circuit

b. Input Impedance:
$Z_i = R_G = R_2 \parallel R_3$

$\mathbf{Z_i = 10.833k\Omega}$

c. Output Impedance:
$Z_o = R_o = \mathbf{3.9k\Omega}$

d. Voltage gain for stage 1, $A_{V1} = \dfrac{V_1}{V_s}$

$\therefore V_1 = -V_{gs2}$

Also, $V_s = V_{gs1}$

$\therefore A_{V1} = \dfrac{-V_{gs2}}{V_{gs2}} = -1 \qquad ...(\because V_{gs1} = V_{gs2})$

$\therefore \mathbf{A_{V1} = -1}$

Voltage gain for stage 2, $A_{V2} = \dfrac{V_{out}}{V_1}$

$\therefore V_{out} = -g_{m2} R_D V_{gs2}$

$\therefore V_1 = V_{gs2}$

$\therefore A_{V2} = \dfrac{-g_{m2} V_{gs2} R_D}{-V_{gs2}}$

$\therefore A_{V2} = g_{m2} R_D$

$\therefore A_{V2} = (0.8069 \times 10^{-3})(3.9k\Omega)$

$\therefore \mathbf{A_{V2} = 3.1574}$

Overall gain, $A_{Vt} = A_{V1} \times A_{V2}$

$\therefore A_{Vt} = (-1) \times 3.1574$

$\therefore \mathbf{A_{Vt} = -3.1574}$

A_{Vt} (in dB) $= 20\log_{10}(3.1574) = \mathbf{9.9866}$

Output voltage, $V_o = V_{in} \times A_{Vt}$

$\therefore V_o = (10mV)(-3.1574)$

$V_o = -31.574V$

Negative sign indicates that the output voltage is 180°out of phase with respect to input voltage.

SIMULATED RESULTS:
Above circuit was simulated in LTspice and results obtained are as follows:

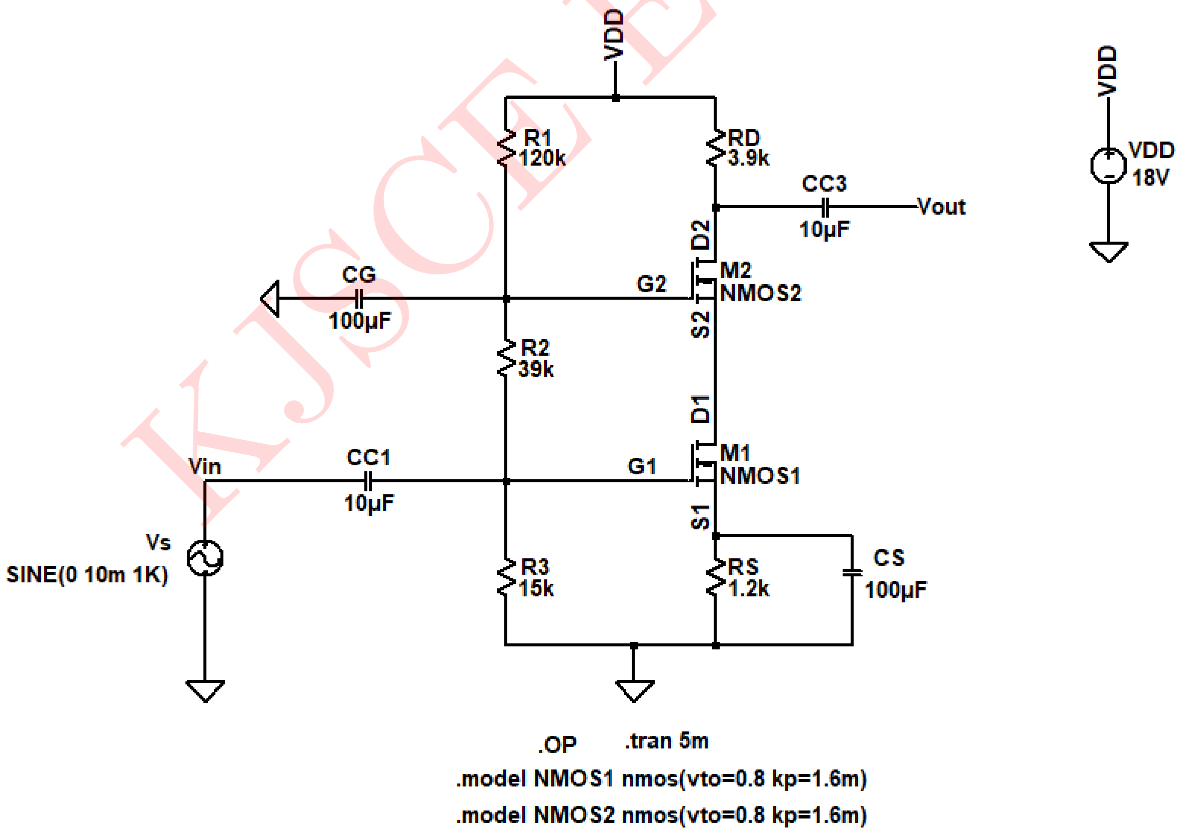

Figure 14: Circuit Schematic: Results

Input and output waveforms for each stage are shown below:

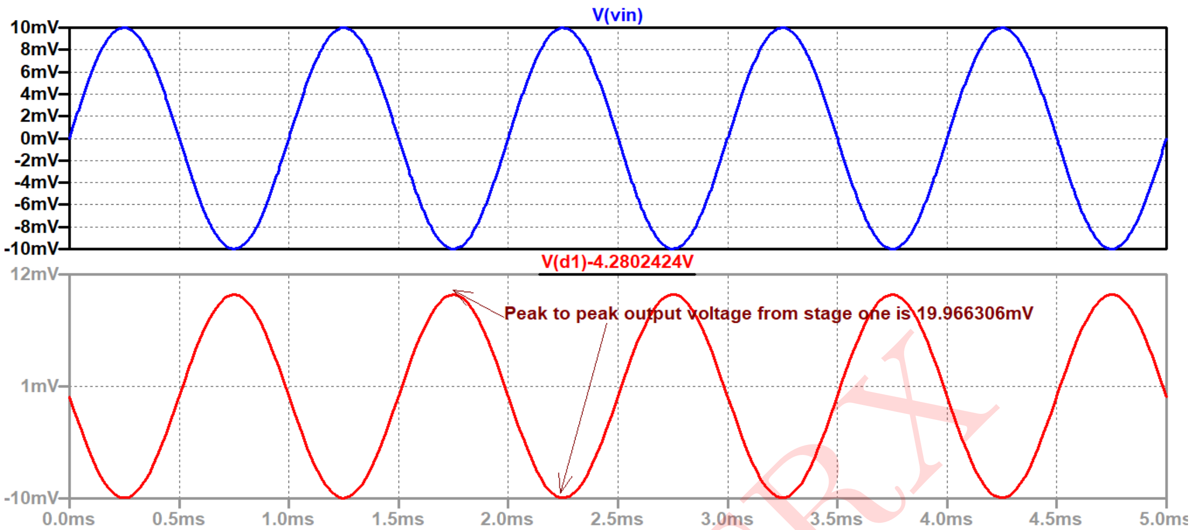

Figure 15: Input and output waveform for Stage 1

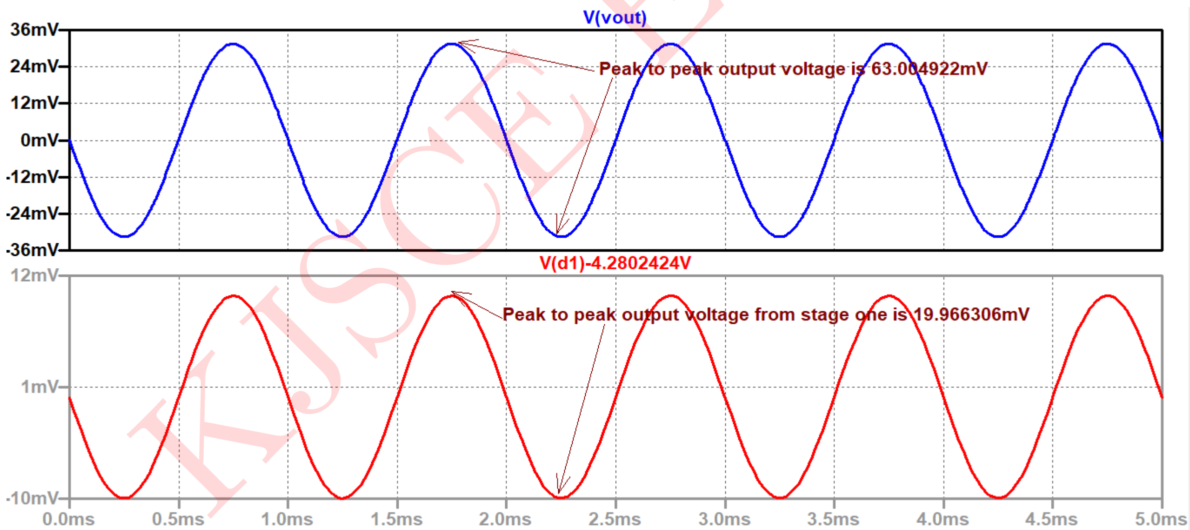

Figure 16: Input and output waveform for Stage 2

Comparsion between theoretical and simulated values:

Parameter	Theoretical value	Simulated value
V_{G1}	1.5517V	1.5517V
V_{D1}	4.2802V	4.2802V
V_{S1}	0.2457V	0.2458V
I_{D1}	0.2048mA	0.2048mA
V_{G2}	5.5862V	5.5862V
V_{D2}	17.2015V	17.2015V
V_{S2}	4.2802V	4.2802V
I_{D2}	0.2048mA	0.2048mA
Voltage gain of stage 1: A_{V1}	-1	-0.9916
Voltage gain of stage 2: A_{V2}	3.1574	3.1510
Overall gain: A_{Vt} in dB	9.9866	9.9690
Input impedance of Stage 1	10.833 kΩ	–
Output impedance of Stage 2	3.9k kΩ	–
Output voltage	$-31.574mV$	$-31.5100mV$

Table 2: Numerical 2