K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Cascade Amplifier Design

Numerical 1:

Design a two stage RC coupled cascade amplifier for following specifications: $A_v \geq 1700$, $V_{o_{rms}} = 2.5V$, $S \leq 10$, $f_L \geq 20Hz$. Use transistor BC147A from data sheet.

Solution:

1. Given Data:

$A_V \geq 1700$, $V_{o_{rms}} = 2.5V$, $S \leq 10$, $f_L \geq 20Hz$

2. Circuit Diagram and Selection of Transistor:

Transistor BC147A is selected with following specifications:

$h_{FE(min)} = 115$, $h_{FE(typ)} = 180$, $h_{FE(max)} = 220$
$h_{ie} = 2.7k\Omega$, $V_{CE(sat)} = 0.25V$
$h_{fe(min)} = 125$, $h_{fe(typ)} = 220$, $h_{fe(max)} = 260$

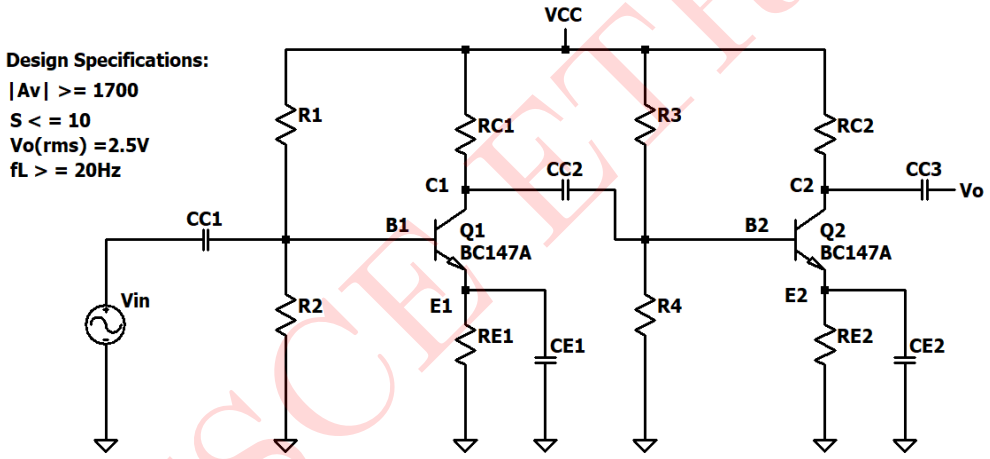

Figure 1: Circuit 1

3. Selection of Voltage gains:

$A_{V_T} = A_{V_1} A_{V_2} = 1700$

$A_{V_1} = 0.5A_{V_2} \Longrightarrow A_{V_T} = 0.5A_{V_2}^2$
i.e $1700 = 0.5A_{V_2}^2 \Longrightarrow A_{V_2} = 58.30$

$$A_{V_1} = \frac{A_{V_T}}{A_{V_2}} = \frac{1700}{58.3} = \mathbf{29.159}$$

Let $A_{V_2} = 59$ & $A_{V_1} = 29$

Design of 2nd stage:

4. Calculation of $\mathbf{R_{C_2}}$:

$$|A_{V_2}| = \frac{h_{fe(typ)\times R_{C_2}}}{h_{ie}} = \frac{220 \times R_{C_2}}{2.7k\Omega}$$

$$59 = \frac{220 \times R_{C_2}}{2.7k\Omega}$$

$$R_{C_2} = \mathbf{724\Omega}$$

Select $R_{C_2} = 750\Omega$, $\frac{1}{4}W$

We select a higher standard value to increase the gain.

5. Selection of Q point ($\mathbf{V_{CEQ_2}}$ & $\mathbf{I_{CQ_2}}$)

$$V_{o_{peak}} = V_{o_{rms}} \times \sqrt{2} = 2.5 \times \sqrt{2} = \mathbf{3.5355V}$$

$$V_{CEQ_2} = 1.5 \quad [V_{o_{peak}} + V_{CE_{(sat)}}]$$

The value is multiplied by 1.5 to take care of saturation voltages, variation in resistance, variation in supply voltage & variation in device parameter variation.

$$V_{CEQ_2} = 1.5(3.5355 + 0.25) = \mathbf{5.68V}$$

$$I_{o_{peak}} = \frac{V_{o_{peak}}}{R_{C_2}} = \frac{3.5355V}{750\Omega} = \mathbf{4.714mA}$$

$I_{CQ_2} \geq I_{o_{peak}}$ [For undistorted output signal]

Select $I_{CQ_2} = \mathbf{4.8mA}$

6. Selection of DC power supply $\mathbf{V_{CC}}$:

In order to achieve maximum symmetrical output swing, always select Q point at the center of DC load line.

i.e $V_{CC} \geq 2V_{CEQ_2}$

$V_{CC} \geq 2 \times 5.68V$

$V_{CC} \geq 11.36$

Select $V_{CC} = \mathbf{12V}$

7. Calculation of $\mathbf{R_{E_2}}$

For proper operation,

$V_{RE_2} = 10\%$ of V_{CC}

$V_{RE_2} = 0.1V_{CC} = 0.1 \times 12 = \mathbf{1.2V}$

$$V_{RE_2} = R_{E_2} \times I_{EQ_2}$$

$$R_{E_2} = \frac{V_{RE_2}}{I_{EQ_2}} \approx \frac{V_{RE_2}}{I_{CQ_2}}$$

$$R_{E_2} = \frac{1.2V}{4.8mA} = \mathbf{250\Omega}$$

Selecting a lower standard value

Select $R_{E_2} = \mathbf{220\Omega, \frac{1}{4}W}$

8. Calculation of Biasing Resistors R_3 & R_4

$$\text{S} = \frac{1 + h_{FE(typ)}}{1 + h_{FE(typ)}\left[\frac{R_{E_2}}{R_{E_2} + R_{B_2}}\right]}$$

$$R_{TH_2} = R_{B_2} = R_3 \parallel R_4$$

$$10 = \frac{1 + 180}{1 + 180\left[\frac{220}{220 + R_{B_2}}\right]}$$

$$R_{TH_2} = R_{B_2} = 2.095k\Omega = \frac{R_3 R_4}{R_3 + R_4} \quad \text{.....(1)}$$

$$V_{TH} = V_{B_2} = \frac{R_4 V_{CC}}{R_3 + R_4} \quad \text{.....(2)}$$

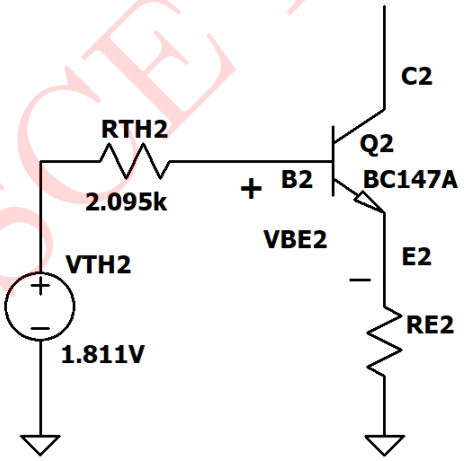

Figure 2: Thevenin's Equivalent Circuit for 2^{nd} stage

Applying KVL at B-E loop of Q_2,

$$V_{TH_2} - I_{BQ_2}R_{TH_2} - V_{BE_2} - I_{EQ_2}R_{E_2} = 0$$

$$V_{TH_2} = I_{BQ_2}R_{B_2} + V_{BE_2} + I_{EQ_2}R_{E_2}$$

$$= V_{BE_2} + \frac{I_{CQ_2}}{\beta}R_{B_2} + I_{CQ_2}R_{E_2}$$

$$= 0.7 + \frac{4.8mA}{180} \times 2.095k\Omega + (4.8mA \times 220\Omega)$$

$$= \mathbf{1.811V}$$

From equation (2),

$$V_{TH_2} = V_{B_2} = 1.811V = \frac{R_4}{R_3 + R_4} \times 12V$$

$$\frac{R_4}{R_3 + R_4} = 0.1509 \qquad \text{.....(3)}$$

Substituting equation (3) in equation (1),

$R_3 \times (0.1509) = 2.059k\Omega$

$R_3 = 13.6447k\Omega$

Selecting a higher standard value so that circuit draws minimum current,

Select $R_3 = \mathbf{15k\Omega}$, $\mathbf{\frac{1}{4}W}$

From equation (3),

$\frac{R_4}{15k\Omega + R_4} = 0.1509$

$R_4 = 2.6657k\Omega$

Selecting a lower standard value,

Select $R_4 = \mathbf{2.4k\Omega}$, $\mathbf{\frac{1}{4}W}$

Design of 1st stage:

9. Selection of R_{C_1}

$$|A_{V_2}| = \frac{h_{fe(typ)} \times R_{C_2}}{h_{ie}}$$
$$= \frac{220 \times 750}{2.7k\Omega}$$
$$= \mathbf{61.11}$$

$$A_{V_1} = \frac{A_{V_T}}{A_{V_2}} = \frac{1700}{61.11} = \mathbf{27.818}$$

Let $A_{V_1} = 28$

$$|A_{V_1}| = \frac{h_{fe(typ)} \times R_{L_1}}{h_{ie}}$$

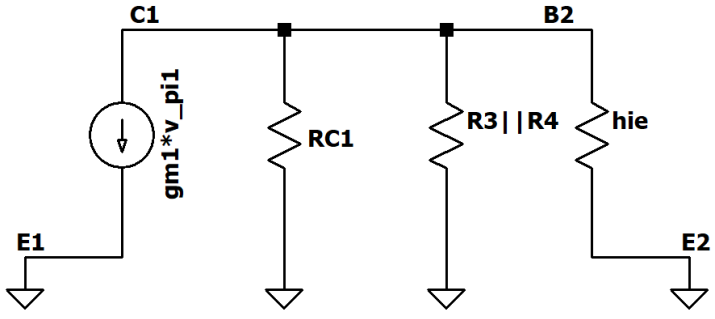

Figure 3: Small Signal Equivalent Circuit for selection of R_{C_1}

$$
\begin{aligned}
R_{L_1} &= R_{C_1} \parallel R_3 \parallel R_4 \parallel h_{ie} \\
&= R_{C_1} \parallel 15k\Omega \parallel 2.4k\Omega \parallel 2.7k\Omega \\
&= R_{C_1} \parallel 2.068k\Omega \parallel 2.7k\Omega \\
&= R_{C_1} \parallel 1.171k\Omega
\end{aligned}
$$

$$
\therefore 28 = \frac{220 \times R_{C_1} \times 1.171k\Omega}{2.7k\Omega(R_{C_1} + 1.171k\Omega)}
$$

$$
343.636 = \frac{R_{C_1} \times 1.171k\Omega}{R_{C_1} + 1.171k\Omega}
$$

$$
R_{C_1} = \mathbf{486.36\Omega}
$$

Select a higher standard value,

Select $R_{C_1} = \mathbf{510\Omega}$, $\mathbf{\frac{1}{4}W}$

10. Calculation of $\mathbf{R_{E_1}}$:

$V_{CEQ_1} = V_{CEQ_2} = 5.68V$

$V_{RE_1} = V_{RE_2} = 1.2V$

$V_{RC_1} = V_{RC_2}$

$\therefore I_{CQ_1} R_{C_1} = I_{CQ_2} R_{C_2}$

$$
\begin{aligned}
I_{CQ_1} &= \frac{I_{CQ_2} R_{C_2}}{R_{C_1}} \\
&= \frac{4.8mA \times 750\Omega}{510\Omega} \\
&= \mathbf{7.058mA}
\end{aligned}
$$

$$
V_{RE_1} = I_{EQ_1} R_{E_1} = \mathbf{1.2V}
$$

$$
R_{E_1} = \frac{V_{RE_1}}{I_{EQ_1}} \approx \frac{V_{RE_1}}{I_{CQ_1}}
$$

$$
R_{E_1} = \frac{1.2V}{7.058mA} = \mathbf{170.019\Omega}
$$

Select a lower standard value,

Select $R_{E_1} = \mathbf{150\Omega}$, $\mathbf{\frac{1}{4}W}$

11. Calaculation of Biasing Resistors ($\mathbf{R_1 + R_2}$):

$$
\mathrm{S} = \frac{1 + h_{FE(typ)}}{1 + h_{FE(typ)} \left[\frac{R_{E_1}}{R_{E_1} + R_{B_1}} \right]}
$$

$$
R_{B_1} = R_1 \parallel R_2
$$

$$
10 = \frac{1 + 180}{1 + 180 \left[\frac{150}{150 + R_{B_1}} \right]}
$$

i.e $R_{TH_1} = R_{B_1} = 1428.947\Omega$

$$R_{TH_1} = R_{B_1} = \frac{R_1 R_2}{R_1 + R_2} = 1428.947\Omega \quad \text{.....(4)}$$

$$V_{TH_1} = V_{B_1} = \frac{R_2}{R_1 + R_2} \times V_{CC} \quad \text{.....(5)}$$

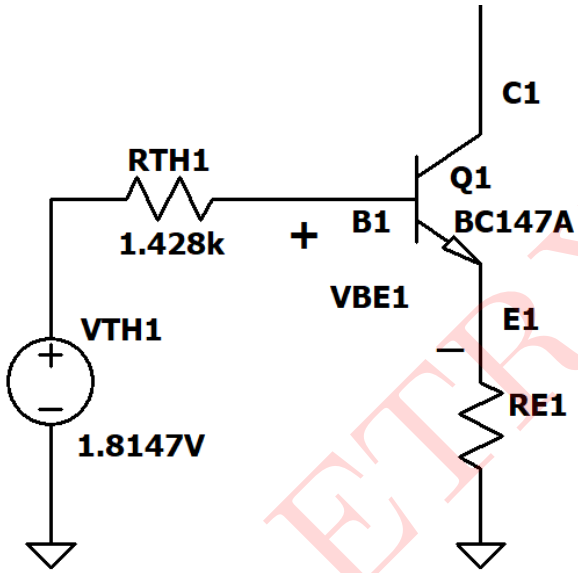

Figure 4: Thevenin's Equivalent Circuit for 1^{st} stage

Applying KVL at B-E loop of Q_1,

$$V_{TH_1} - V_{BE_1} - I_{BQ_1} R_{B_1} - I_{EQ_1} R_{E_1} = 0$$

$$V_{TH_1} = V_{BE_1} + \frac{I_{CQ_1}}{\beta} R_{B_1} + I_{CQ_1} R_{E_1}$$

$$= 0.7 + \frac{7.058mA}{180} \times (1428.947\Omega) + (7.058mA \times 150\Omega)$$

$$= \mathbf{1.8147V}$$

From equation (5),

$$V_{TH_1} = 1.8147V = \frac{R_2}{R_1 + R_2} \times 12V$$

$$\frac{R_2}{R_1 + R_2} = 0.1512 \quad \text{.....(6)}$$

Substituting equation (6) in equation (4),

$R_1 \times (0.1512) = 1428.947\Omega$

$R_1 = 9.45k\Omega$

Select a higher standard value,

Select $R_1 = \mathbf{10k\Omega}$, $\mathbf{\frac{1}{4}W}$

From equation(6),

$$\frac{R_2}{R_1 + R_2} = 0.1512$$

$$\frac{R_2}{10k + R_2} = 0.1512$$
$$R_2 = \mathbf{1.781k\Omega}$$

Select a lower standard value,

Select $R_2 = \mathbf{1.5k\Omega}$, $\mathbf{\frac{1}{4}W}$

12. Calculation of coupling capacitors:

a. Calculation of $\mathbf{C_{C_1}}$

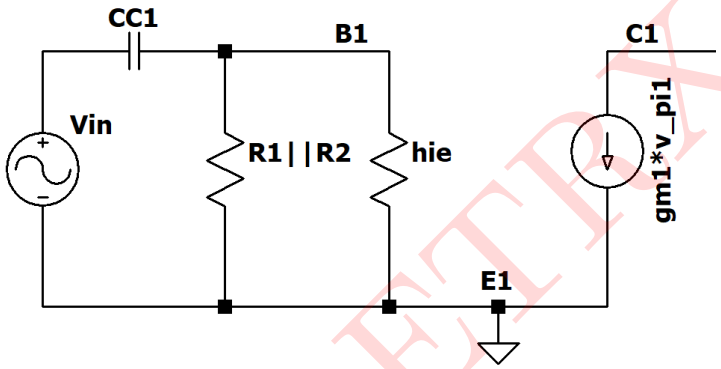

Figure 5: Small Signal Equivalent Circuit for C_{C_1}

$$C_{C_1} = \frac{1}{2\pi R_{eq} f_L}$$

$$\begin{aligned} R_{eq} &= R_1 \parallel R_2 \parallel h_{ie} \\ &= 10k\Omega \parallel 1.5k\Omega \parallel 2.7k\Omega \\ &= 1.304k\Omega \parallel 2.7k\Omega \\ &= 879.32\Omega \end{aligned}$$

$$C_{C_1} = \frac{1}{2\pi \times 879.32\Omega \times 20} = 9.049\mu F$$

Selecting a higher standard value

Select $C_{C_1} = \mathbf{10\mu F/24V}$

b. Calculation of $\mathbf{C_{C_2}}$:

$$C_{C_2} = \frac{1}{2\pi R_{eq} f_L}$$

$$\begin{aligned} R_{eq} &= R_{C_1} + R_3 \parallel R_4 \parallel h_{ie} \\ &= 510k\Omega + 15k\Omega \parallel 2.4k\Omega \parallel 2.7k\Omega \\ &= 510k\Omega + 2.068k\Omega \parallel 2.7k\Omega \\ &= 510k\Omega + 1.171k\Omega \\ &= 1.681k\Omega \end{aligned}$$

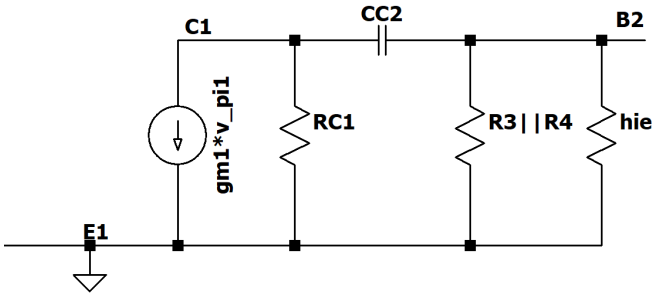

Figure 6: Small Signal Equivalent Circuit for C_{C_2}

$$C_{C_2} = \frac{1}{2\pi \times 1.681k\Omega \times 20Hz} = 4.733\mu F$$

Selecting a higher standard value,

Select $C_{C_2} = \mathbf{6.8\mu F/24V}$

c. Calculation of $\mathbf{C_{C_3}}$:

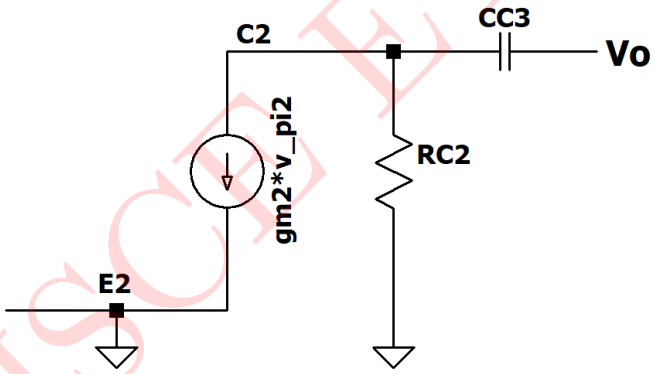

Figure 7: Small Signal Equivalent Circuit for C_{C_3}

$$C_{C_3} = \frac{1}{2\pi \times R_{eq} \times f_L}$$

$$R_{eq} = R_{C_2} = 750\Omega$$

$$C_{C_3} = \frac{1}{2\pi \times 750 \times 20}$$

$$= 10.61\mu F$$

Selecting a higher standard value,

Select $C_{C_3} = \mathbf{12\mu F/24V}$

13. Calculation of Bypass Capacitors:

a. $\mathbf{C_{E_1}}$:

$X_{CE_1} = \frac{R_{E_1}}{10}$ [To ensure complete bypass of R_E, $X_{CE} < R_E$]

i.e $\frac{1}{2\pi f_L C_{E_1}} = 0.1R_{E_1}$

$$C_{E_1} = \frac{1}{2\pi \times f_L \times 0.1R_{E_1}}$$
$$= \frac{1}{2\pi \times 20 \times 0.1 \times 150}$$
$$= 530.516\mu F$$

Selecting a higher standard value

Select $C_{E_1} = \mathbf{560\mu F/24V}$

b. CE_2:

$$X_{CE_2} = \frac{R_{E_2}}{10} \Longrightarrow X_{CE_2} = 0.1R_{E_2}$$

i.e $\frac{1}{2\pi f_L C_{E_2}} = 0.1R_{E_2}$

$$C_{E_2} = \frac{1}{2\pi f_L \times 0.1R_{E_2}}$$
$$= \frac{1}{2\pi \times 20 \times 0.1 \times 220}$$
$$= 361.715\mu F$$

Selecting a higher standard value

Select $C_{E_2} = \mathbf{470\mu F/24V}$

14. Complete Designed Circuit:

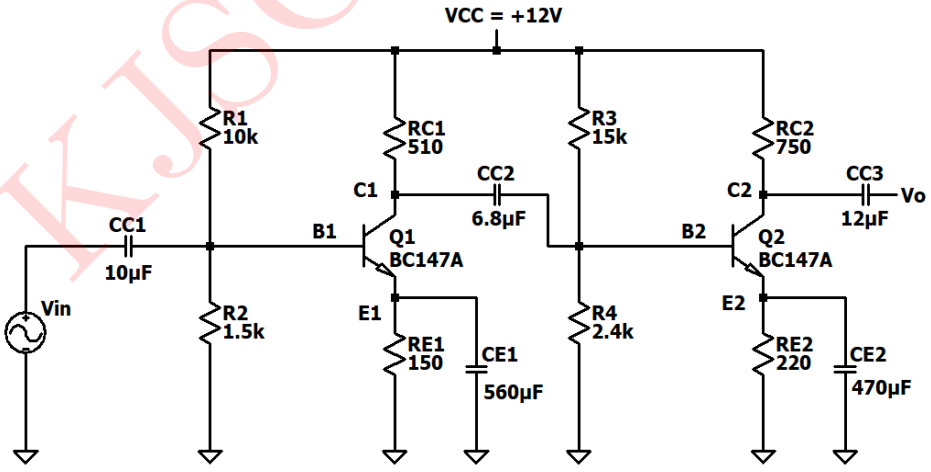

Figure 8: Designed Circuit

DC Analysis:

For 1st stage:

$R_{TH_1} = 10k\Omega \parallel 1.5k\Omega = 1.304k\Omega$

$V_{TH_1} = \frac{R_2}{R_1 + R_2} \times V_{CC} = 1.565V$

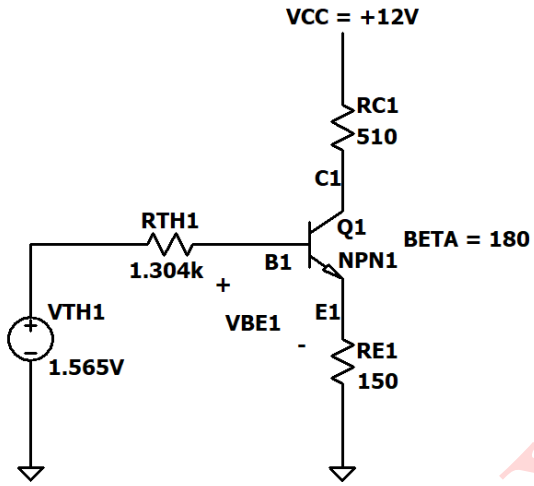

Figure 9: DC Equivalent Circuit for 1^{st} stage

Applying KVL at B-E loop of Q_1,

$V_{TH_1} - I_{B_1}R_{TH_1} - V_{BE_1} - I_{E_1}R_{E_1} = 0$

$V_{TH_1} - I_{B_1}R_{TH_1} - V_{BE_1} - (1+\beta_1)I_{B_1}R_{E_1} = 0$

$$I_{B_1} = \frac{V_{TH_1} - V_{BE_1}}{R_{TH_1} + (1+\beta_1)R_{E_1}}$$
$$= \frac{1.565 - 0.7}{1.304k\Omega + (181 \times 150)}$$
$$= \mathbf{30.399\mu A}$$

$I_{C_1} = \beta_1 I_{B_1} = 180 \times 30.399\mu A = \mathbf{5.47mA}$

$I_{E_1} = I_{C_1} + I_{B_1} = 5.47mA + 30.399\mu A = \mathbf{5.5mA}$

$V_{E_1} = I_{E_1}R_{E_1} = 5.5mA \times 150 = \mathbf{0.825V}$

$V_{BE} = 0.7V = V_{B_1} - V_{E_1} = \mathbf{1.525V}$

For 2^{nd} stage:

Applying KVL at B-E loop of Q_2,

$V_{TH_2} - I_{B_2}R_{TH_2} - V_{BE_2} - I_{E_2}R_{E_2} = 0$

$V_{TH_2} - I_{B_2}R_{TH_2} - V_{BE_2} - (1+\beta_2)I_{B_2}R_{E_2} = 0$

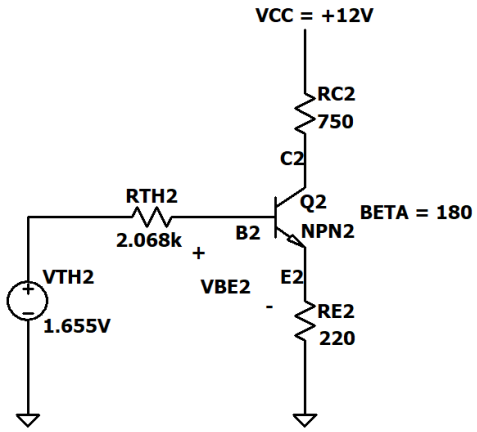

Figure 10: DC Equivalent Circuit for 2^{nd} stage

$$I_{B_2} = \frac{V_{TH_2} - V_{BE_2}}{R_{TH_2} + (1+\beta_2)R_{E_2}}$$

$$\begin{aligned} V_{TH_2} &= \frac{R_3}{R_3 + R_4} \times V_{CC} \\ &= \frac{2.4k\Omega}{15k\Omega + 2.4k\Omega} \times 12V \\ &= \mathbf{1.655V} \end{aligned}$$

$$R_{TH_2} = R_3 \parallel R_4 = 15k\Omega \parallel 2.4k\Omega = \mathbf{2.068k\Omega}$$

$$I_{B_2} = \frac{1.655 - 0.7}{2.068 + (181 \times 220)} = \mathbf{22.798\mu A}$$

$$I_{C_2} = \beta_2 I_{B_2} = 180 \times 22.798\mu A = \mathbf{4.1mA}$$

$$I_{E_2} = I_{C_2} + I_{B_2} = 4.1mA + 22.798\mu A = \mathbf{4.722mA}$$

$$V_{E_2} = I_{E_2} R_{E_2} = 4.722mA \times 220\Omega = \mathbf{1.0388V}$$

$$V_{BE_2} = 0.7V = V_{B_2} - V_{E_2} = \mathbf{1.7388V}$$

Small Signal Parameters:

$$g_{m_1} = \frac{I_{C_1}}{V_T} = \frac{5.47mA}{0.026V} = 210.384mA/V$$

$$r_{\pi_1} = \frac{\beta_1 V_T}{I_{C_1}} = \frac{180 \times 0.026V}{5.47mA} = 855.575\Omega$$

$$g_{m_2} = \frac{I_{C_2}}{V_T} = \frac{4.1mA}{0.026V} = 157.692mA/V$$

$$r_{\pi_2} = \frac{\beta_2 V_T}{I_{C_2}} = \frac{180 \times 26mV}{4,1mA} = 1.141k\Omega$$

Mid Frequency AC Equivalent Circuit:

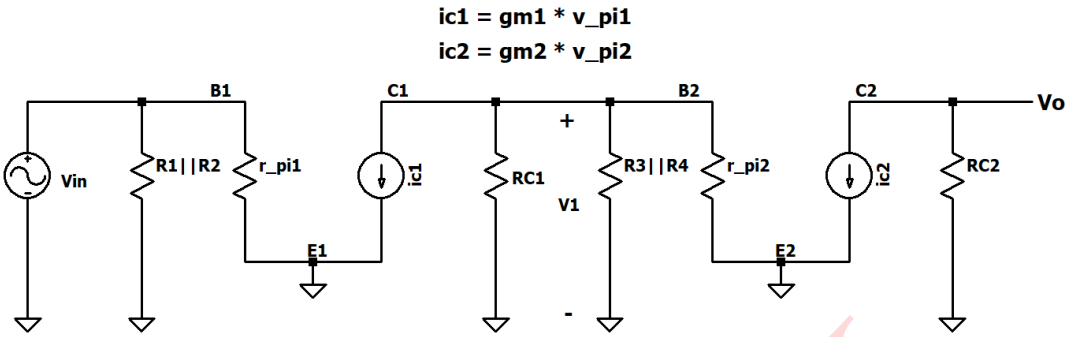

Figure 11: Small Signal Equivalent Circuit

Volatge gain of 1^{st} stage: $Av_1 = \dfrac{V_1}{V_{in}}$

$$Av_1 = \frac{V_1}{V_{in}} = \frac{-g_{m_1} V_{\pi_1} (R_{C_1} \parallel R_3 \parallel R_4 \parallel r_{\pi_2})}{V_{\pi_1}}$$

$$Av_1 = -g_{m_1} (R_{C_1} \parallel R_3 \parallel R_4 \parallel r_{\pi_2})$$

$$= -(210.384mA/V)(510 \parallel 15 \parallel 2.4 \parallel 1.141k\Omega)$$

$$= -(210.384mA/V)(301.155\Omega)$$

$$= \mathbf{-63.358}$$

Voltage gain of 2^{nd} stage: $Av_2 = \dfrac{V_o}{V_1}$

$$Av_2 = \frac{-g_{m_2} V_{\pi_2} R_{C_2}}{V_{\pi_2}}$$

$$= -g_{m_2} R_{C_2}$$

$$= -(157.692mA/V)(750\Omega)$$

$$= \mathbf{-118.269}$$

Overall Voltage Gain: $A_{V_T} = \dfrac{V_o}{V_{in}}$

$$Av_T = Av_1 \times Av_2$$

$$= (-63.358) \times (-118.269)$$

$$= \mathbf{7493.287} \quad (\geq 1700)$$

Av_T in dB $= 20 \log_{10}(Av_T) =$ **77.493**dB

Input Impedance of 1st stage: Z_i

$$Z_i = R_1 \parallel R_2 \parallel r_{\pi_1}$$

$$= 10k\Omega \parallel 1.5k\Omega \parallel 855.575\Omega$$

$$= \mathbf{516.67\Omega}$$

Output Impedance of 2nd stage: Z_o

$Z_o = R_{C_2}$

$Z_o = \mathbf{750\Omega}$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

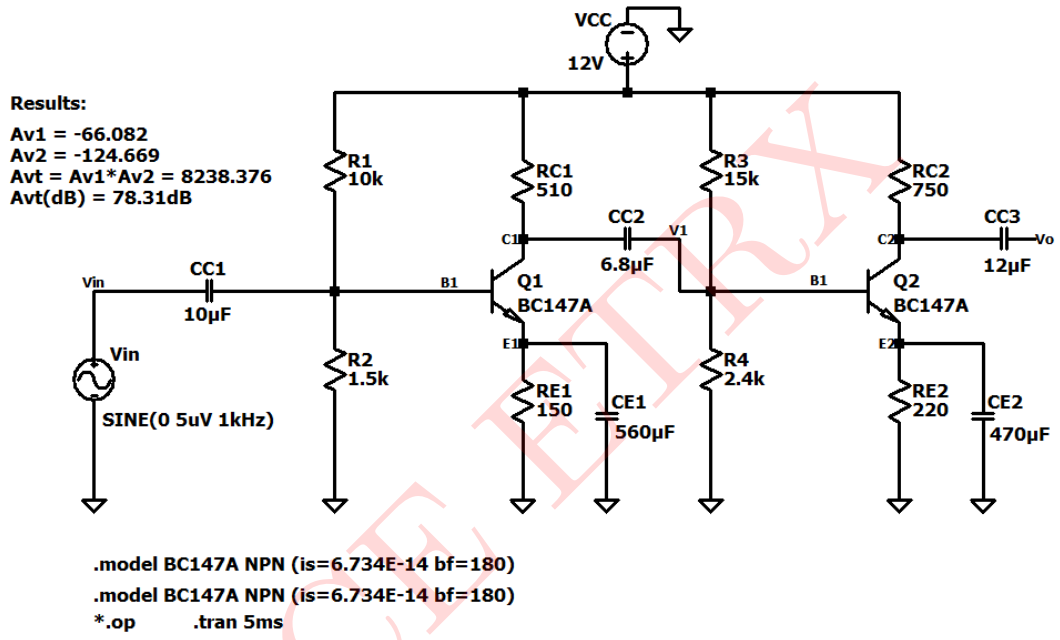

Figure 12: Circuit Schematic

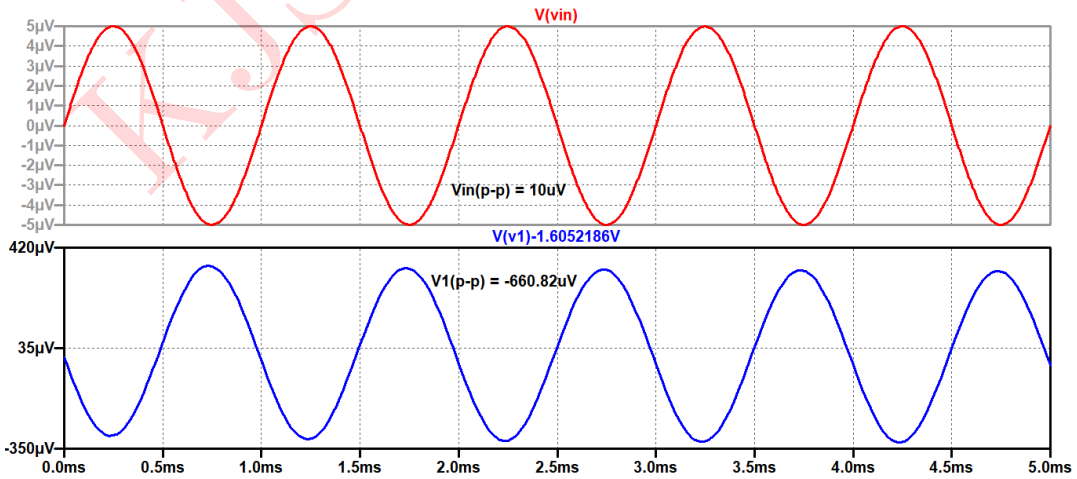

Figure 13: Input Output waveform of 1^{st} stage

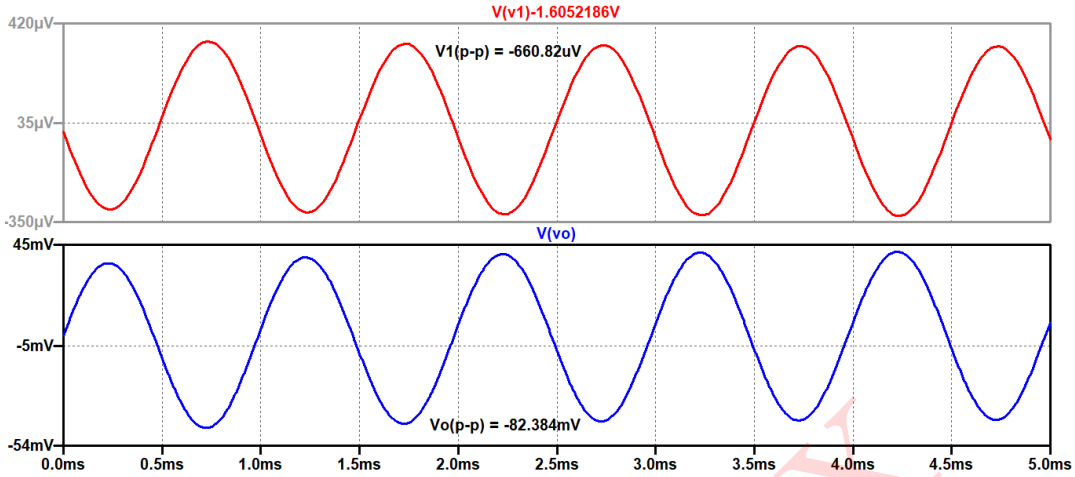

Figure 14: Input Output waveform of 2^{nd} stage

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
I_{B_1}, I_{B_2}	$30.399\mu A$, $22.798\mu A$	$32.12\mu A$, $24.14\mu A$
I_{C_1}, I_{C_2}	$5.47mA$, $4.1mA$	$5.78mA$, $4.34mA$
I_{E_1}, I_{E_2}	$5.5mA$, $4.722mA$	$5.81mA$, $4.37mA$
V_{E_1}, V_{E_2}	$0.825V$, $1.0388V$	$0.872V$, $0.9614V$
V_{B_1}, V_{B_2}	$1.525V$, $1.7388V$	$1.5233V$, $1.6052V$
Voltage gain of 1^{st} stage: Av_1	-63.358	-66.082
Voltage gain of 2^{nd} stage: Av_2	-118.269	-124.669
Overall Voltage gain: A_{V_T} in dB	77.493dB	78.31dB
Input Impedance of 1^{st} stage: Z_i	516.67Ω	–
Output Impedance of 2^{nd} stage: Z_o	750Ω	–

Table 1: Numerical 1

Numerical 2:

Design a two stage RC coupled cascade amplifier for following specifications: $A_v \geq 480$, $V_{CC} = 20V$, $S \leq 10$, $R_i \geq 1M\Omega$. Select a suitable transistor from data sheet

Solution:

Above requirements can be fulfilled by CS-CE stage

We select CS as 1^{st} stage since $R_i \geq 1M\Omega$

1. Circuit Diagram and Selection of Transistor:

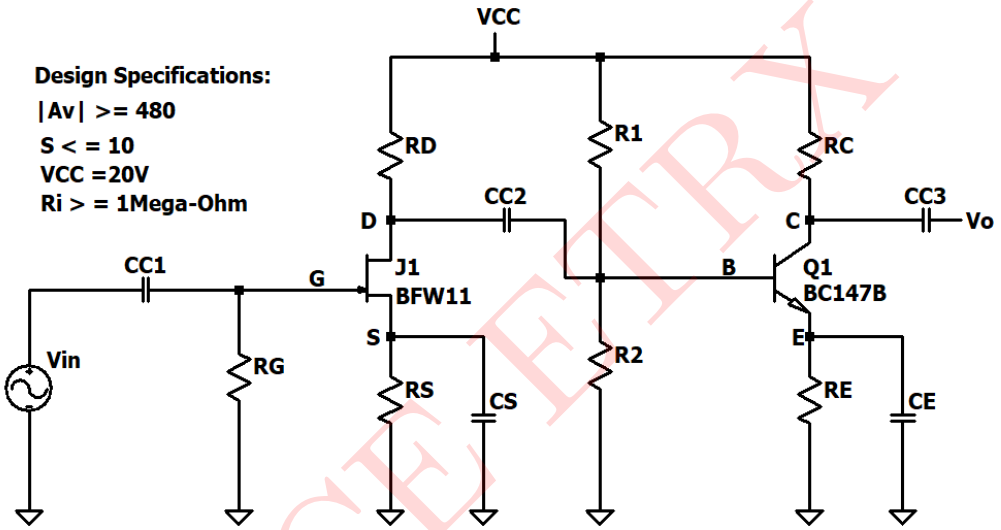

Figure 15: Circuit 1

Select BC147B since its $h_{fe(typ)}$ & h_{ie} is higher, its specifications are:

$h_{fe(typ)} = 330$, $h_{FE(typ)} = 290 = \beta$

$h_{ie} = 4.5k\Omega$, $V_{CE(sat)} = 0.25V$

Select BFW11, its specifications are:

$I_{DSS} = 7mA$, $g_{mo} = 5600\mu\mho$

$V_p = -2.5V$, $r_d = 50k\Omega$

3. Selection of gains:

$A_V \geq 480$

Let $Av_1 = 4$ [Since JFET amplifier gain is less]

i.e $Av_2 = \dfrac{480}{4} = 120$

Let $Av_2 = 125$

Design of 2nd stage:

3. Selection of $\mathbf{R_C}$:

$|A_{V_2}| = \frac{h_{fe(typ)\times R_C}}{h_{ie}}$

$125 = \frac{330 \times R_C}{4.5k\Omega}$

$R_C = \mathbf{1.704k\Omega}$

Selecting a higher standard value,

Select $R_C = \mathbf{1.8k\Omega}$, $\mathbf{\frac{1}{4}W}$

4. Selection of Q point ($\mathbf{V_{CEQ}}$ & $\mathbf{I_{CQ}}$)

$V_{CC} = 20V$

Let $V_{CEQ} = \frac{V_{CC}}{2} = 10V$

$V_{RE} = 0.1V_{CC} = 0.1 \times 20 = 2V$

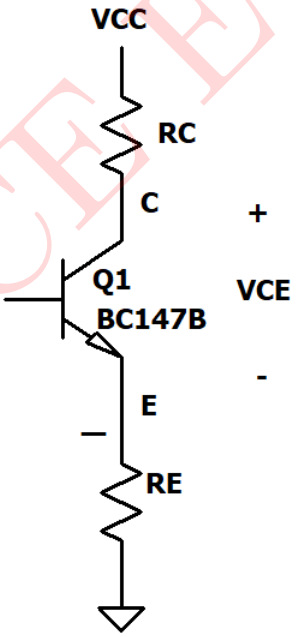

Figure 16: DC Equivalent Circuit for selection of Q point

Applying KVL to CE loop of BJT,

$V_{CC} - V_{RC} - V_{CEQ} - V_{RE} = 0$

$V_{RC} = V_{CC} - V_{CEQ} - V_{RE}$

$= 20 - 10 - 2$

$= \mathbf{8V}$

i.e $V_{RC} = I_{CQ}R_C = 8$

$I_{CQ} = \frac{V_{RC}}{R_C} = \frac{8}{1.8k\Omega} = \mathbf{4.44mA}$

5. Selection of $\mathbf{R_E}$:

$V_{RE} = 2V$

$I_{EQ}R_E = 2 \Longrightarrow R_E = \dfrac{2}{I_{CQ}}$ $[\because I_{CQ} \approx I_{EQ}]$

$R_E = 450.45\Omega$

Selecting a lower standard value,

Select $R_E = \mathbf{420\Omega}$, $\mathbf{\frac{1}{4}W}$

6. Selection of Biasing Resistors $\mathbf{R_1}$ & $\mathbf{R_2}$

S ≤ 10

Let S = 9, $\beta = 290$

$$S = \frac{1+\beta}{1+\beta\left[\dfrac{R_E}{R_E+R_B}\right]}$$

$$9 = \frac{1+290}{1+290\left[\dfrac{420}{420+R_B}\right]}$$

$R_B = 3.467k\Omega$

$$R_{TH} = R_B = R_1 \parallel R_2 = \frac{R_1R_2}{R_1+R_2} = 3.467k\Omega \quad .....(1$$

$$V_{TH} = V_B = \frac{R_2V_{CC}}{R_1+R_2} \quad .....(2)$$

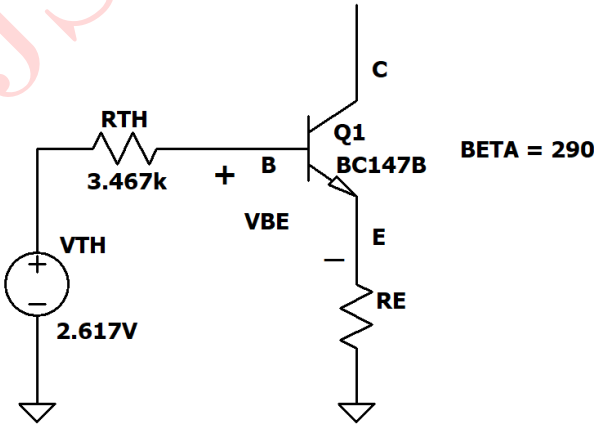

Figure 17: Thevenin's Equivalent Circuit

Applying KVL at B-E loop of BJT,

$V_{TH} - I_{BQ}R_{TH} - V_{BE} - I_{EQ}R_E = 0$

$$V_{TH} = \frac{I_{CQ}}{\beta}R_{TH} + V_{BE} + I_{CQ}R_E$$
$$= \frac{4.44mA}{290} \times (3.467k\Omega) + 0.7V + (4.44mA \times 420)$$
$$= \mathbf{2.617V}$$

From equation (2),

$$V_{TH} = 2.617 = \frac{R_2}{R_1 + R_2} \times 20V$$

$$\frac{R_2}{R_1 + R_2} = 0.13 \qquad \text{.....(3)}$$

Substituting equation (3) in equation (1),

$R_1 \times (0.13) = 3.467k\Omega$

$R_1 = 26.669k\Omega$

Select $R_1 = \mathbf{27k\Omega}$, $\mathbf{\frac{1}{4}W}$

From equation (3),

$$\frac{R_2}{27k\Omega + R_2} = 0.13$$
$R_2 = 4.034k\Omega$

Selecting a higher standard value,

Select $R_2 = \mathbf{4.2k\Omega}$, $\mathbf{\frac{1}{4}W}$

Design of 1st stage:

7. Selection of Q point ($\mathbf{I_{DQ}}$ & $\mathbf{V_{GSQ}}$)

Using mid point biasing,

$$I_{DQ} = \frac{I_{DSS}}{2} = \frac{7mA}{2} = \mathbf{3.5mA}$$

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$V_{GSQ} = V_p\left(1 - \sqrt{\frac{I_{DQ}}{I_{DSS}}}\right)$$
$$= -2.5\left(1 - \sqrt{\frac{3.5mA}{7mA}}\right)$$
$$= \mathbf{-0.732V}$$

$$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_p}\right)$$
$$= (5600 \times 10^{-6})\left(1 - \frac{(-0.732V)}{-2.5V}\right)$$
$$= \mathbf{3.96mA/V}$$

8. Selection of $\mathbf{R_D}$:

$$|A_{V_2}| = \frac{h_{fe(typ)\times R_C}}{h_{ie}} = \frac{330 \times 1.8k\Omega}{4.5k\Omega} = 132$$

$$|A_{V_1}| = \frac{A_V}{|A_{V_2}|} = \frac{480}{132} = 3.636$$

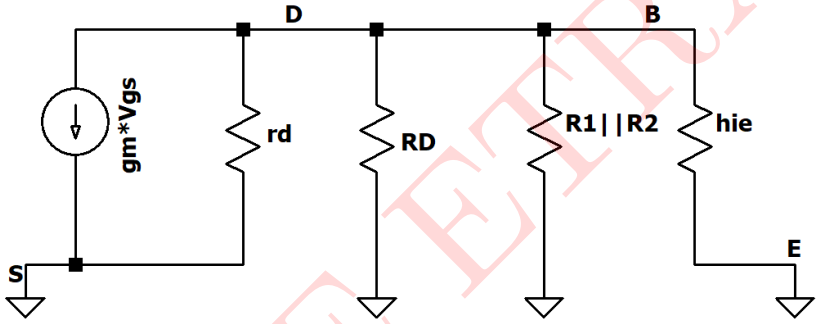

Figure 18: Small Signal Equivalent Circuit for selection of R_D

$$|Av_1| = g_m[R_D \parallel R_1 \parallel R_2 \parallel r_d \parallel h_{ie}]$$

$$R_{L_1} = r_d \parallel R_1 \parallel R_2 \parallel h_{ie}$$
$$= 50k\Omega \parallel 27k\Omega \parallel 4.2k\Omega \parallel 4.5k\Omega$$
$$= 17.532k\Omega \parallel 2.172k\Omega$$
$$= 1.932k\Omega$$

$$|Av_1| = g_m[R_D \parallel 1.932k\Omega]$$
$$3.636 = (3.96mA/V)\left[\frac{R_D \times 1.932k\Omega}{R_D + 1.932k\Omega}\right]$$
$$918.181 = \frac{R_D \times 1.932k\Omega}{R_D + 1.932k\Omega}$$
$$R_D = \mathbf{1.749k\Omega}$$

Select a higher standard value,

Select $R_D = \mathbf{2.2k\Omega}$, $\mathbf{\frac{1}{4}W}$

9. Selection of $\mathbf{R_S}$

$V_{GSQ} = -I_{DQ}R_S$

$-0.732 = -3.5mA \times R_S$

$R_S = 209.14\Omega$

Selecting a lower standard value,

Select $R_S = \mathbf{180\Omega}$, $\mathbf{\frac{1}{4}W}$

10. Selection of $\mathbf{R_G}$

Let $R_G = 1.2M\Omega, \frac{1}{4}W$ [Since $R_i = 1M\Omega$ to prevent loading we take $R_G \geq 1M\Omega$]

11. Selection of Coupling capacitors:

Since f_L is not given we consider audio frequency $f_L = 20Hz$

a. $\mathbf{C_{C_1}}$

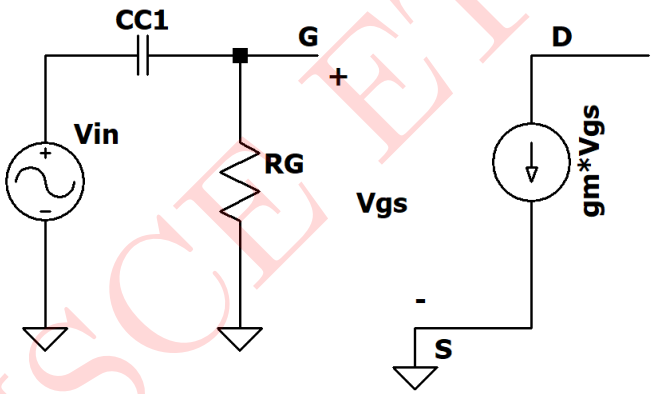

Figure 19: Small Signal Equivalent Circuit for C_{C_1}

$$C_{C_1} = \frac{1}{2\pi R_G f_L}$$
$$= \frac{1}{2\pi \times 1.2 \times 10^6 \times 20}$$
$$= 6.63nF$$

Selecting a higher standard value

Select $C_{C_1} = \mathbf{6.8nF/50V}$

b. $\mathbf{C_{C_2}}$

$$C_{C_2} = \frac{1}{2\pi \times R_{eq} \times f_L}$$

$$R_{eq} = (r_d \parallel R_D) + R_1 \parallel R_2 \parallel h_{ie}$$
$$= 50k\Omega \parallel 2.2k\Omega + 27k\Omega \parallel 4.2k\Omega \parallel 4.5k\Omega$$
$$= 2.107k\Omega + 2.010k\Omega$$
$$= 4.117k\Omega$$

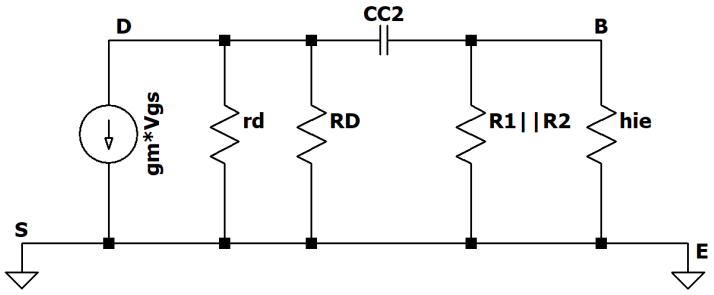

Figure 20: Small Signal Equivalent Circuit for C_{C_2}

$$C_{C_2} = \frac{1}{2\pi \times 4.117k\Omega \times 20Hz} = 1.932\mu F$$

Selecting a higher standard value,

Select $C_{C_2} = \mathbf{2.2\mu F/50V}$

c. $\mathbf{C_{C_3}}$

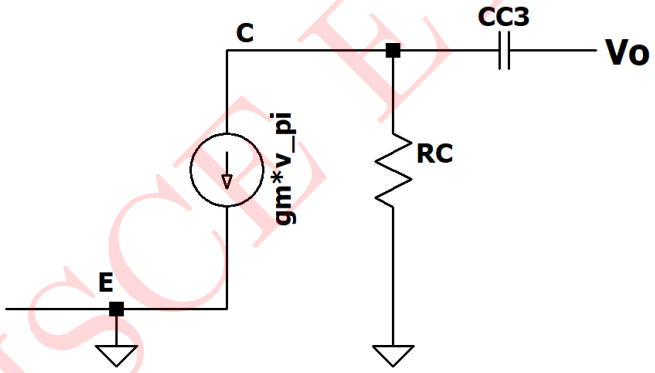

Figure 21: Small Signal Equivalent Circuit for C_{C_3}

$$C_{C_3} = \frac{1}{2\pi \times R_{eq} \times f_L}$$

$$R_{eq} = R_C = 1.8k\Omega$$

$$C_{C_3} = \frac{1}{2\pi \times 1.8k\Omega \times 20} = 4.42\mu F$$

Selecting a higher standard value,

Select $C_{C_3} = \mathbf{4.7\mu F/50V}$

12. Selection of Bypass Capacitors:

a. $\mathbf{C_S}$:

$$C_S = \frac{1}{2\pi \times R_{eq} \times f_L}$$

$$R_{eq} = \left(\frac{1}{g_m} \parallel R_S\right)$$
$$= \left(\frac{1}{3.96 \times 10^{-3}} \parallel 180\right)$$
$$= 252.52 \parallel 180$$
$$= \mathbf{105.09\Omega}$$

$$C_S = \frac{1}{2\pi \times 105.09 \times 20} = 75.72\mu F$$

Selecting a higher standard value,

Select $C_S = \mathbf{82\mu F/50V}$

a. C_E:

$X_{CE} = 0.1R_E$ [Ensures complete bypass of R_E]

i.e $\frac{1}{2\pi f_L C_E} = 0.1R_E$

$$C_E = \frac{1}{2\pi f_L 0.1R_E} = \frac{1}{2\pi \times 20 \times 0.1 \times 420}$$

Selecting a higher standard value

Select $C_E = \mathbf{220\mu F/50V}$

13. Complete Designed Circuit:

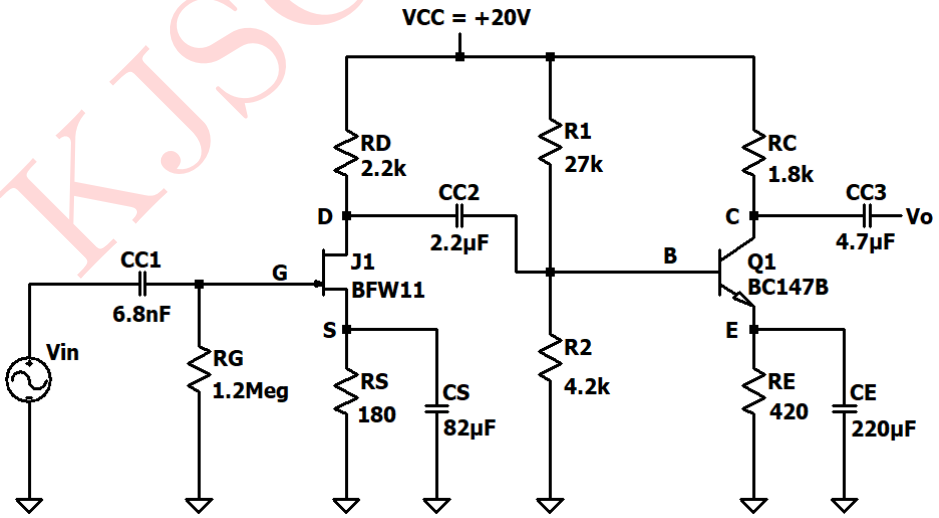

Figure 22: Designed Circuit

DC Analysis:

For 1st stage:

Applying KVL at G-S loop,

$V_{GS} - I_D R_S = 0$

$V_G S = I_D R_S$

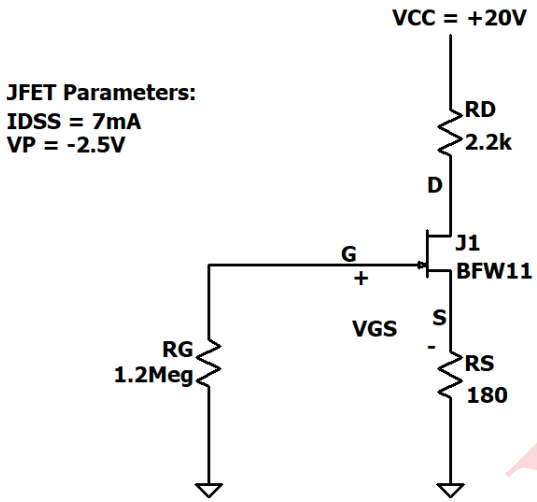

Figure 23: DC Equivalent Circuit for 1^{st} stage

$V_G - V_S = I_D R_S$

$V_G = 0$, since $I_G = 0$, $\therefore V_{GS} = -V_S$

$V_{GS} = -I_D R_S$ .....(1)

Now, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

$I_D = (7mA)\left(1 + \frac{V_{GS}}{2.5}\right)^2$ .....(2)

Substituting equation(2) in equation(1),

$$I_{GS} = -(7mA \times 180\Omega)\left(1 + \frac{V_{GS}}{2.5}\right)^2$$

$$= -1.26\left(1 + \frac{V_{GS}}{2.5}\right)^2$$

$$= -1.26\left(1 + \frac{V_{GS}^2}{6.25} + \frac{2V_{GS}}{2.5}\right)$$

$$= -1.26 - 0.2016V_{GS}^2 - 1.008V_{GS}$$

$0.2016V_{GS}^2 + 2.008V_{GS} + 1.26 = 0$

$V_{GS} = -0.67V \quad \text{or} \quad V_{GS} = -9.28V$

$\because V_{GS} > V_p, \therefore V_{GSQ} = \mathbf{-0.67V}$

From equation (1),

$V_{GS} = -I_D R_S$

$-0.67V = -I_D(180\Omega)$

$I_{DQ} = \mathbf{3.722mA}$

For 2nd stage:

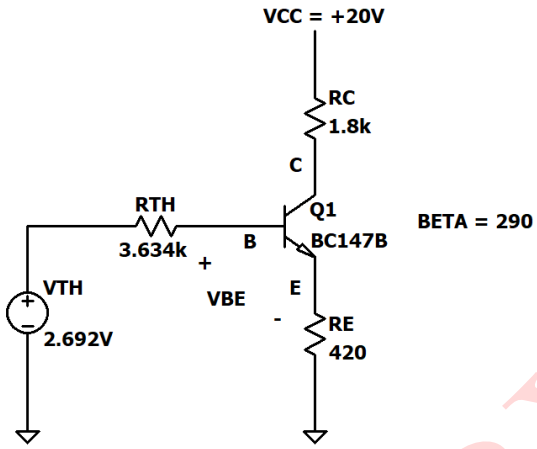

Figure 24: DC Equivalent Circuit for 2^{nd} stage

$R_{TH} = R_1 \parallel R_2 = 27k\Omega \parallel 4.2k\Omega = \mathbf{3.634k\Omega}$

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{CC} = 2.692V$$

Applying KVL at B-E loop,

$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$

$V_{TH} - I_B R_{TH} - V_{BE} - (1+\beta) I_B R_E = 0$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)R_E}$$
$$= \frac{2.692 - 0.7}{3.634k\Omega + (291 \times 420)}$$
$$= \mathbf{15.827\mu A}$$

$I_C = \beta I_B = 290 \times 15.827\mu A = \mathbf{4.589mA}$

$I_E = I_B + I_C = 4.589mA + 15.827\mu A = \mathbf{4.6mA}$

$V_E = I_E R_E = 4.6mA \times 420\Omega = \mathbf{1.932V}$

$V_{BE} = 0.7V = V_B - V_E$

$V_B = V_{BE} + V_E = \mathbf{2.632V}$

Small Signal Parameters:

For 1st stage:

$$g_m = \frac{2I_{DSS}}{|V_p|}\left(1 - \frac{V_{GS}}{V_p}\right) = \frac{2 \times 7mA}{2.5V}\left(1 - \frac{0.67}{2.5}\right) = 4.09mA/V$$

$r_d = 50k\Omega$ [Given]

$$r_d = \frac{1}{\lambda I_{DQ}}$$

$$\lambda = \frac{1}{r_d \times I_{DQ}} = \frac{1}{50k\Omega \times 3.722mA} = 5.373mV^{-1}$$

For 2nd stage:

$$g_m = \frac{I_C}{V_T} = \frac{4.589mA}{0.026V} = 176.5mA/V$$

$$r_\pi = \frac{\beta V_T}{I_C} = \frac{290 \times 26mV}{4.589mA} = 1.643k\Omega$$

Mid Frequency AC Equivalent Circuit:

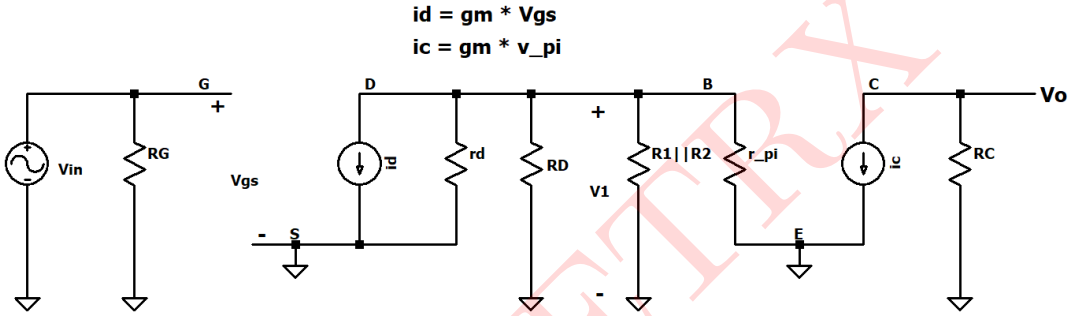

Figure 25: Small Signal Equivalent Circuit

Volatge gain of 1^{st} stage: $Av_1 = \frac{V_1}{V_{in}}$

$$Av_1 = \frac{V_1}{V_{in}} = \frac{-g_m V_{gs}(r_d \parallel R_D \parallel R_1 \parallel R_2 \parallel r_\pi)}{V_{gs}}$$

$$Av_1 = -g_{m_1}(r_d \parallel R_D \parallel R_1 \parallel R_2 \parallel r_\pi)$$

$$= -(4.09mA/V)(50k\Omega \parallel 2.2k\Omega \parallel 27k\Omega \parallel 4.2k\Omega \parallel 1.643k\Omega)$$
$$= -(4.09mA/V)(2.107k\Omega \parallel 3.634k\Omega \parallel 1.643k\Omega)$$
$$= -(4.09mA/V)(736.1439\Omega)$$
$$= \mathbf{-3.01}$$

Voltage gain of 2^{nd} stage: $Av_2 = \frac{V_o}{V_1}$

$$Av_2 = \frac{-g_m V_\pi R_C}{V_\pi}$$
$$= -g_m R_C$$
$$= -(176.5mA/V)(1.8k\Omega)$$
$$= \mathbf{-317.7}$$

Overall Voltage Gain: $A_{V_T} = \frac{V_o}{V_{in}}$

$$Av_T = Av_1 \times Av_2$$
$$= (-3.01) \times (-317.7)$$
$$= \mathbf{956.277}$$

Av_T in dB $= 20\log_{10}(Av_T) = 20\log_{10} 965.277 =$ **59.611**dB

Input Impedance of 1st stage: Z_i

$Z_i = R_G =$ **1.2MΩ**

Output Impedance of 2nd stage: Z_o

$Z_o = R_C$

$Z_o =$ **1.8kΩ**

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

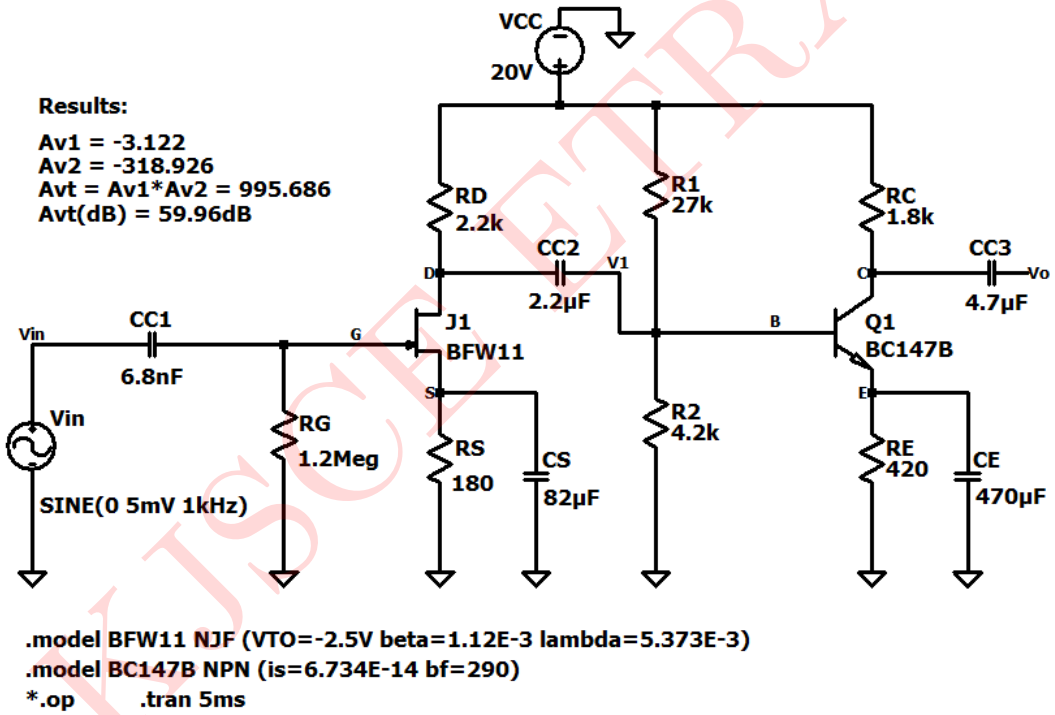

Figure 26: Circuit Schematic

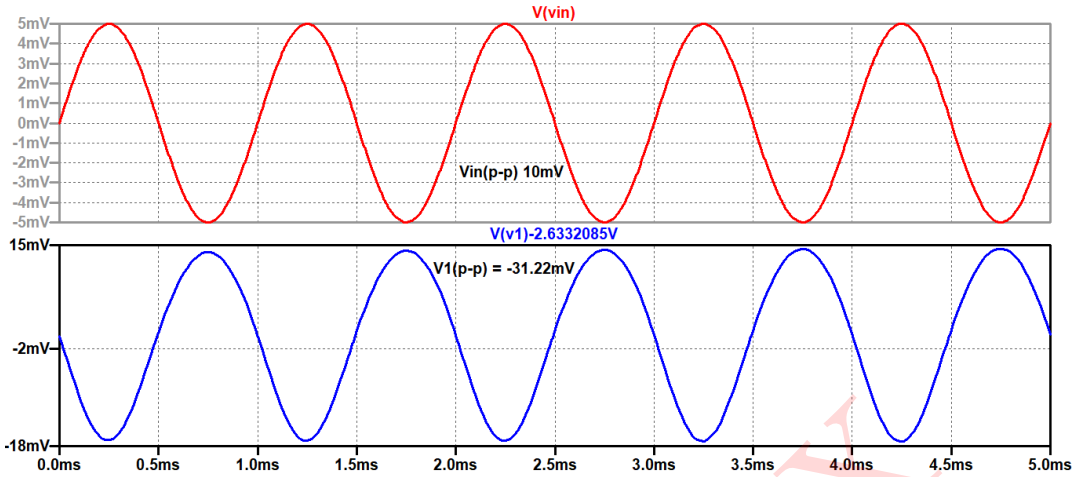

Figure 27: Input Output waveform of 1^{st} stage

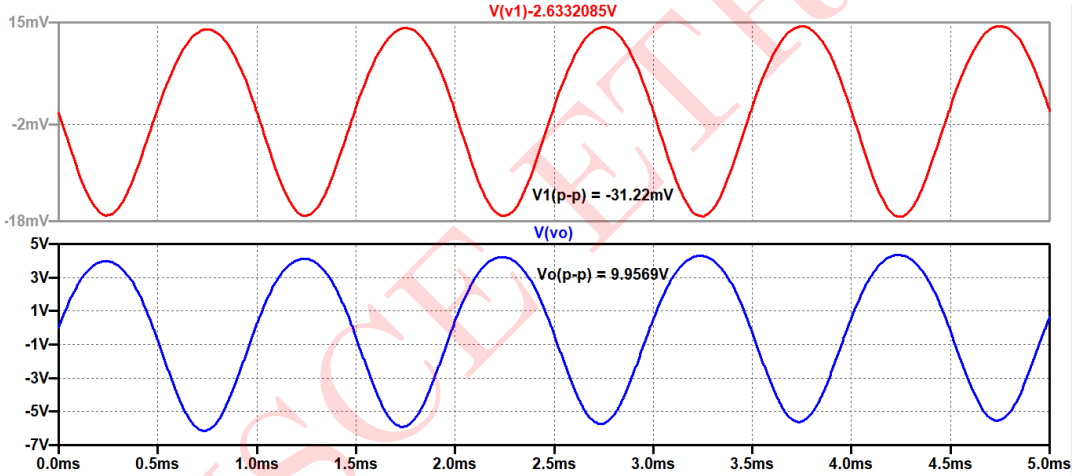

Figure 28: Input Output waveform of 2^{nd} stage

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
I_{DQ}, V_{GSQ}	$3.722mA$, $-0.67V$	$3.86mA$, $-0.694V$
I_B	$15.827\mu A$	$16.26\mu A$
I_C	$4.589mA$	$4.715mA$
V_E	$1.932V$	$1.987V$
V_B	$2.632V$	$2.633V$
Voltage gain of 1^{st} stage: Av_1	-3.01	-3.122
Voltage gain of 2^{nd} stage: Av_2	-317.7	-318.926
Overall Voltage gain: A_{V_T} in dB	59.611dB	59.96dB
Input Impedance of 1^{st} stage: Z_i	$1.2M\Omega$	–
Output Impedance of 2^{nd} stage: Z_o	$1.8k\Omega$	–

Table 2: Numerical 2

****