K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
DIODE APPLICATIONS

Numerical 1

For the clipper circuit shown in figure 1. Plot

a) Input $V_{in}(t)$ & Output $V_{out}(t)$ waveforms.

b) VTC Curve

Given: $V_{in}(t) = 10V_{p-p}$ sinusoidal signal with frequency of $5000Hz$.
Use constant voltage model i.e. $V_{D_{ON}} = 0.7V$, $V_B = 1V$ & $R_1 = 1k\Omega$

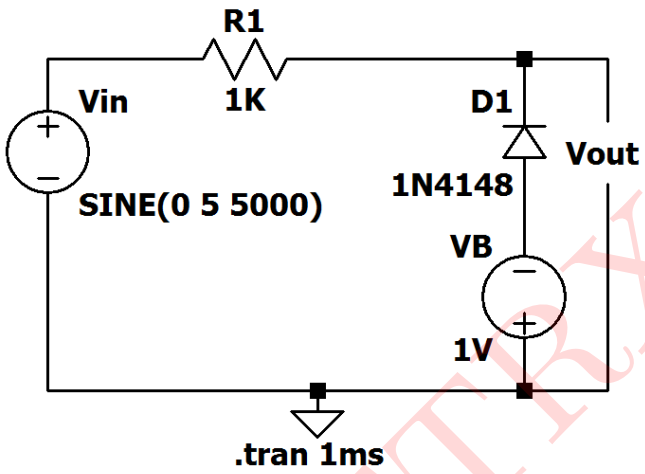

Figure 1: Circuit For Numerical 1

Solution:
Assuming constant voltage model for the diode D_1, bias voltage V_B reverse biases the diode D_1.

There are two cases considering V_{in}:

Case 1: If $V_{in} < (-V_{D_{ON}} - V_B)$

In this case diode D_1 is ON (i.e. Diode becomes short circuit).

The reduced circuit is shown in figure 2

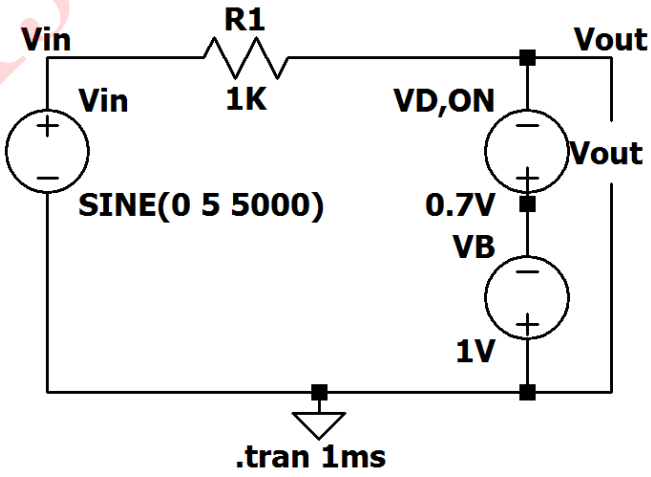

Figure 2: When diode is ON

i.e. $V_{out} = -V_{D_{ON}} - V_B$

$V_{out} = -0.7V - 1V$ $\quad (\because V_{D_{ON}} = 0.7V \ \& \ V_B = 1V\ )$

$\therefore \mathbf{V_{out} = -1.7V}$

Case 2: If $V_{in} > (-V_{D_{ON}} - V_B)$

In this case diode D_1 is OFF (i.e. Diode becomes open circuit).
The reduced circuit is shown in figure 3

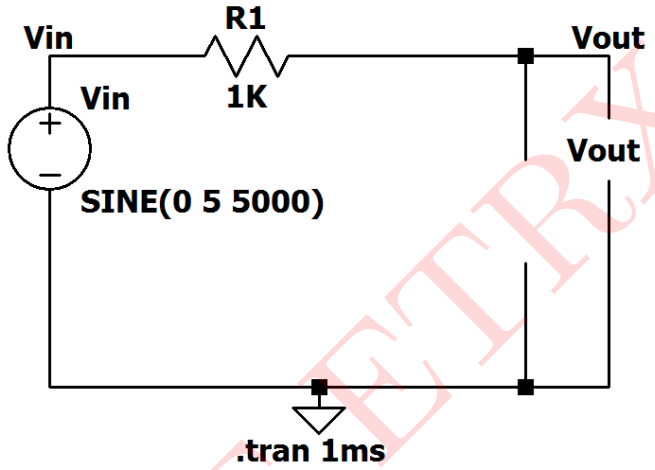

Figure 3: When diode is OFF

i.e. $V_{out} = V_{in}$

Here, output follows input but with shift

$(-V_{D_{ON}} - V_B) = (-0.7V - 1V) = -1.7V$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

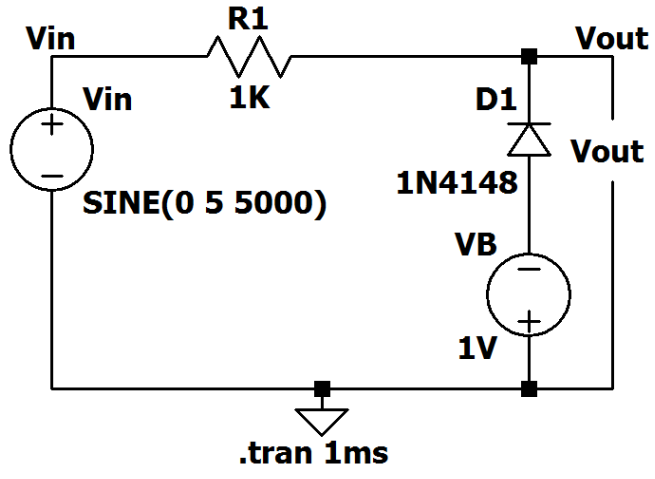

Figure 4: Circuit Schematic

The input and ouput waveforms are shown in figure 5

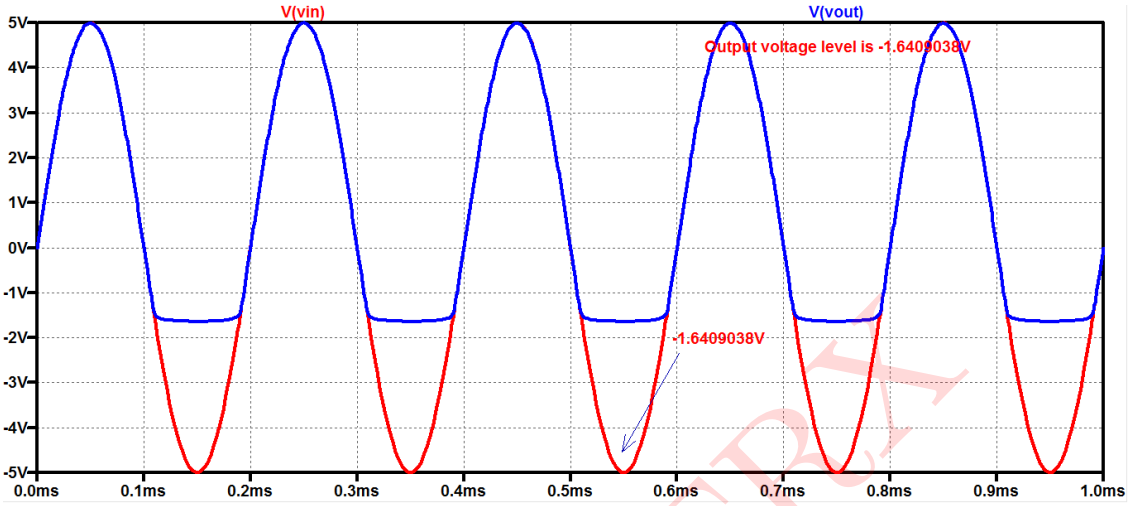

Figure 5: Input & Output waveforms

The VTC curve for the following circuit is given below in figure 6

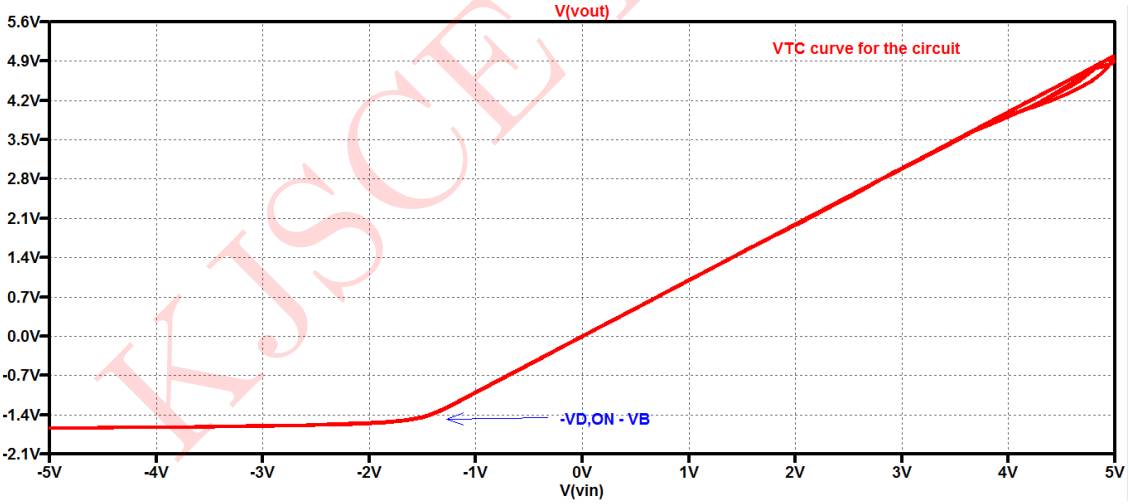

Figure 6: VTC Curve

Comparison between theoretical and simulated values is given below:

Parameters	Simulated Values	Theoretical Values
Level of clipped voltages	-1.64V	-1.7V

Table 1: Numerical 1

Numerical 2

For the clipper circuit shown in figure 7, plot the input & output waveforms.
Given: $V_{in}(t) = 16V_{p-p}$ sinusoidal signal with frequency of $1000Hz$.

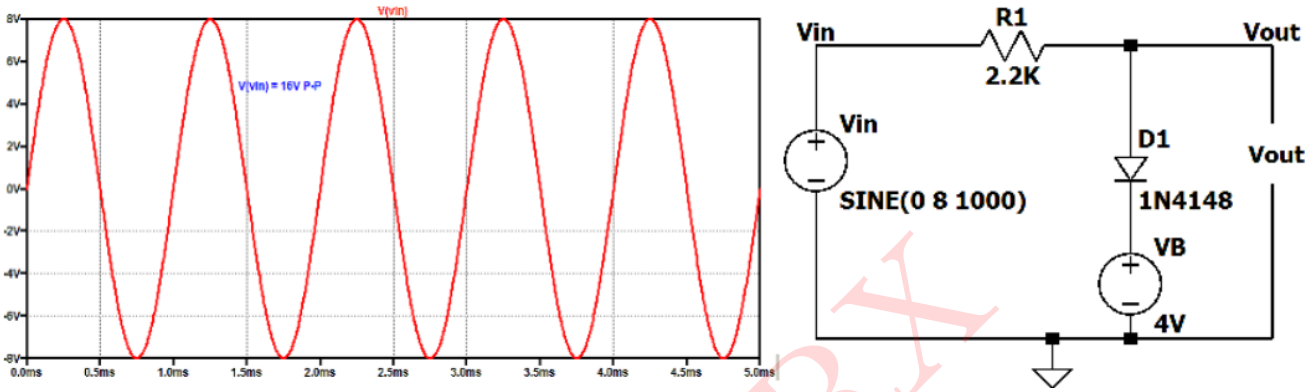

Figure 7: Circuit for Numerical 2

Solution:

Assuming constant voltage model for the diode D_1

There are two cases considering V_{in}:

Case 1: If $V_{in} < (V_{D_{ON}} + V_B)$

In this case diode D_1 is OFF. The reduced circuit is shown in figure 9.

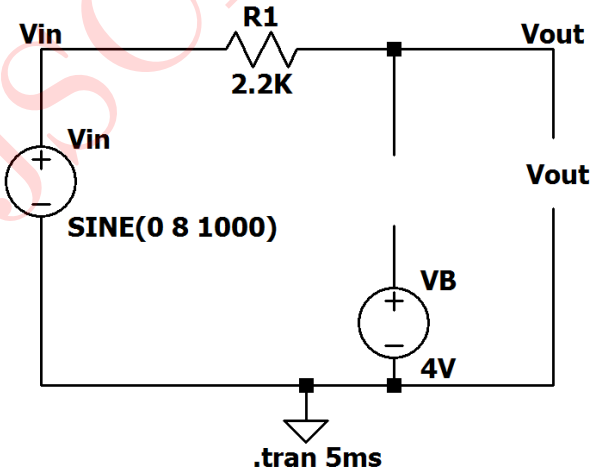

Figure 8: When diode is OFF

Here output follows input by the shift of $V_{D_{ON}} + V_B = 0.7V + 4V = 4.7V$

The circuit becomes open circuit because the cathode voltage is greater than anode voltage.

Case 2: If $V_{in} > (V_{D_{ON}} + V_B)$

In this case diode D_1 is ON. The reduced circuit is shown in figure 4.

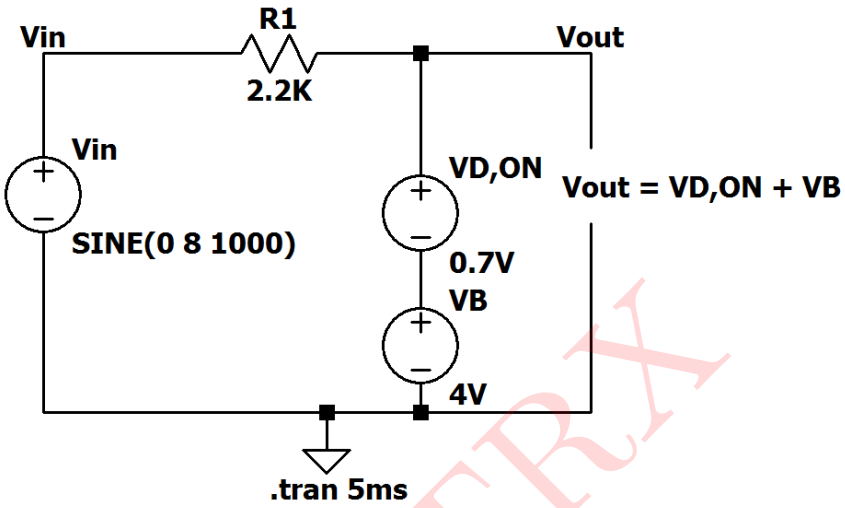

Figure 9: When diode is ON

$V_{out} = V_{D_{ON}} + V_B = (0.7V + 4V) = 4.7V \qquad (\because V_{D_{ON}} = 0.7V \ \& \ V_B = 4V)$

D_1 begins to turn ON at $V_{D_{ON}} + V_B = 4.7V$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

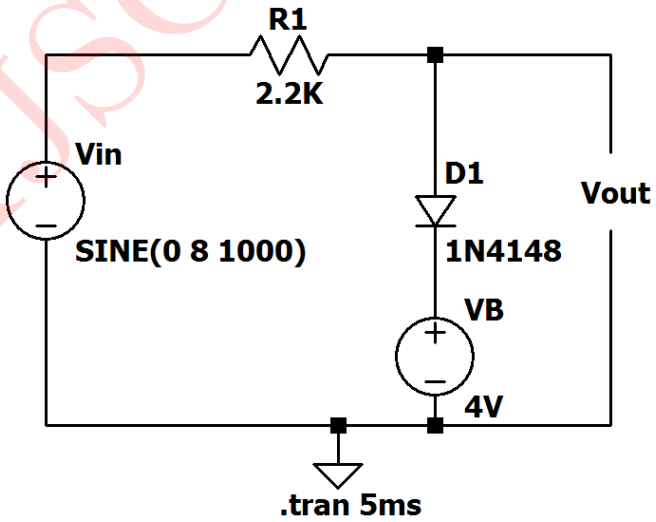

Figure 10: Circuit Schematic

The circuit given in the question is biased parallel positive clipper.

The input & output waveforms are shown below in figure 11.

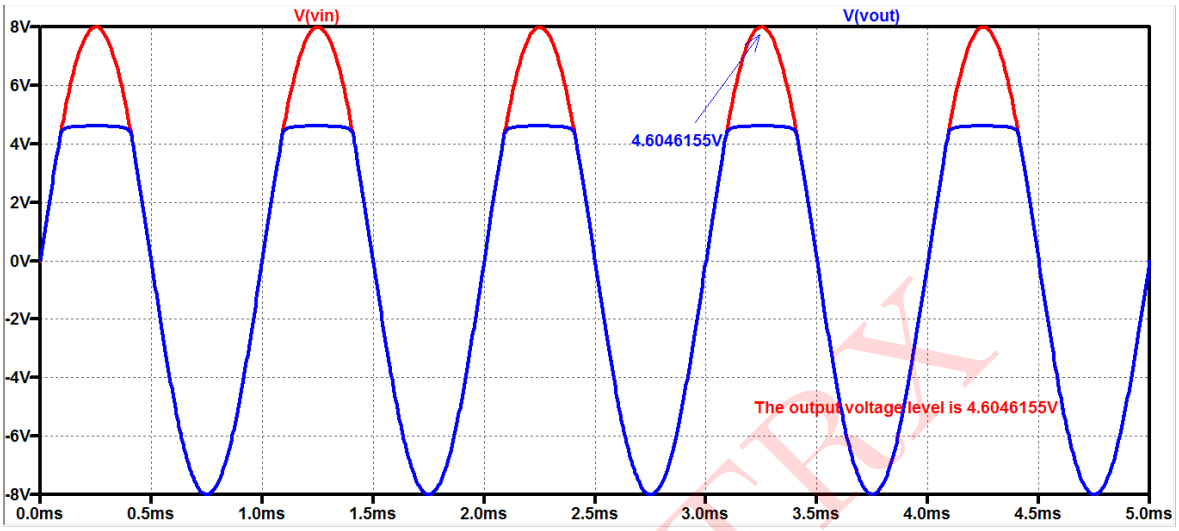

Figure 11: Input & Output Waveforms

Comparison between theoretical and simulated values is given below:

Parameters	Simulated Values	Theoretical Values
Level of clipped voltages	4.604V	4.7V

Table 2: Numerical 2

Numerical 3

For the clamper circuit shown in figure 12, plot the input $V_{in}(t)$ & output $V_{out}(t)$ waveforms. Given: $V_{in}(t) = 10V_{p-p}$ square wave with frequency of $1000Hz$, $C_1 = 10\mu F$, $R_1 = 10k\Omega$ & diode D_1 is Si diode i.e. $V_{D_{ON}} = 0.7V$

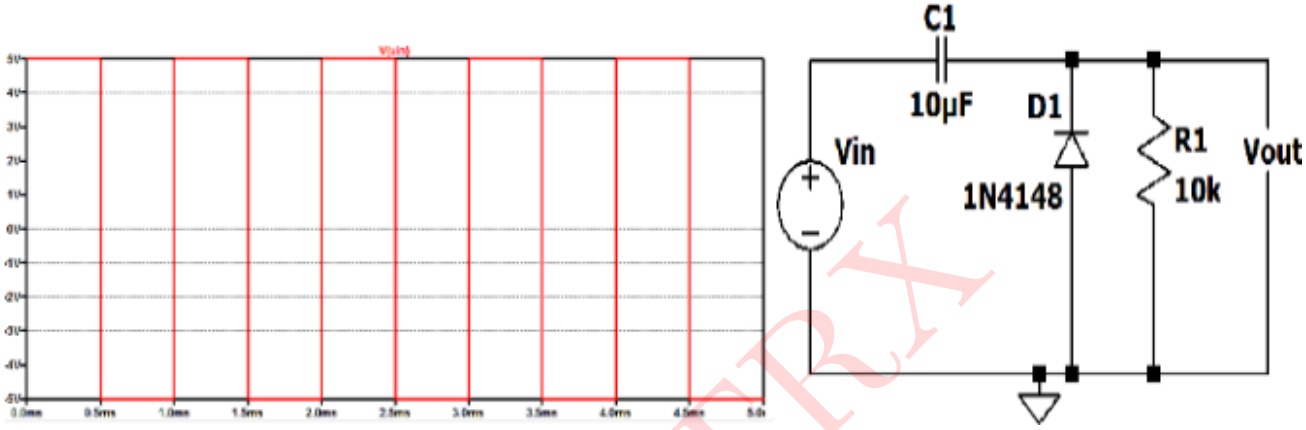

Figure 12: Circuit for Numerical 3

Solution:

Given: $V_{in} = 10V_{p-p}$ i.e. $V_m = 5V$.

Since the diode is Si, we will prefer constant voltage model.

Assumption: RC time constant is large enough to ensure that voltage across capacitor does not discharge significantly during the period the diode is ON.

Case 1: During negative half cycle, D_1 is ON $\quad (\because V_{in} < -V_{D_{ON}})$

The reduced circuit is shown in figure 13.

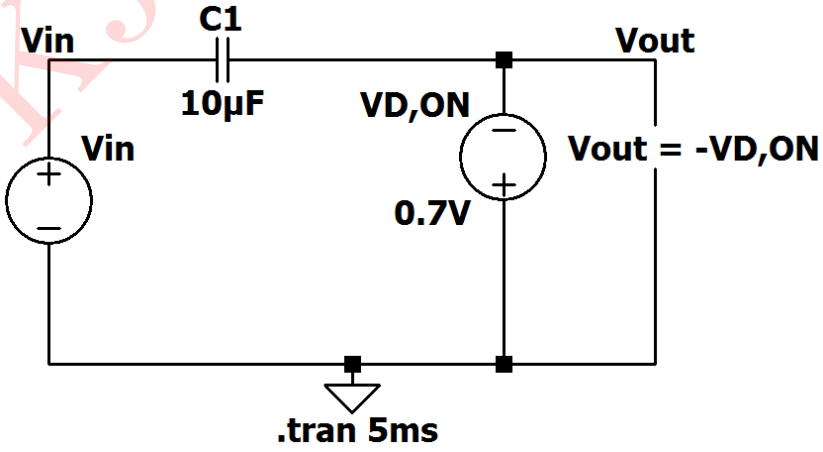

Figure 13: When diode is ON

During negative half cycle of input i.e. $V_{out} = -V_{D_{ON}} = -0.7V$

At the same time C_1 charges, the voltage across capacitor is V_C

By applying KVL to the circuit we get,

$V_{in} + V_C + V_{D_{ON}} = 0$

$V_C = -V_{in} - V_{D_{ON}} = -(-V_m) - 0.7$ (During negative half cycle $V_{in} = -V_m$)

$\mathbf{V_C = 4.3V}$

Case 2: During positive half cycle, D_1 is OFF

The reduced circuit is shown in figure 14.

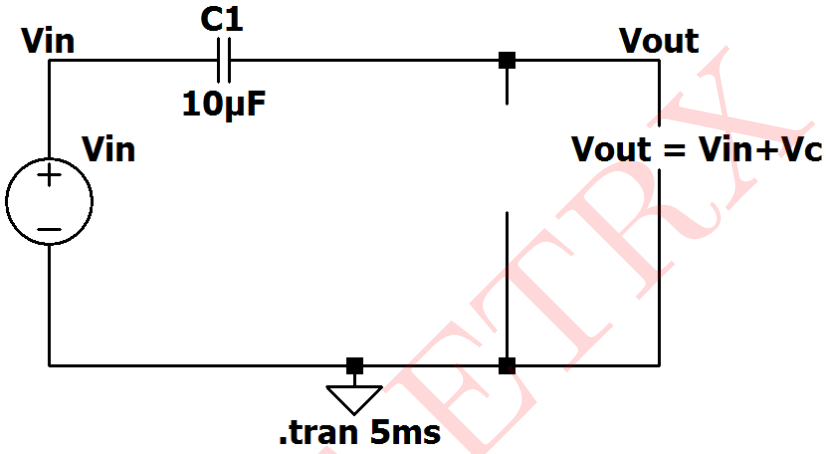

Figure 14: When diode is OFF

Applying KVL to the circuit we get

$V_{in} + V_C - V_{out} = 0$

$V_{out} = V_{in} + V_C = V_m + V_C = 5 + 4.3$

$\therefore \mathbf{V_{out}} = \mathbf{9.3}V$

SIMULATED RESULTS:

Above circuit is simulated in LTspice and results are as follows:

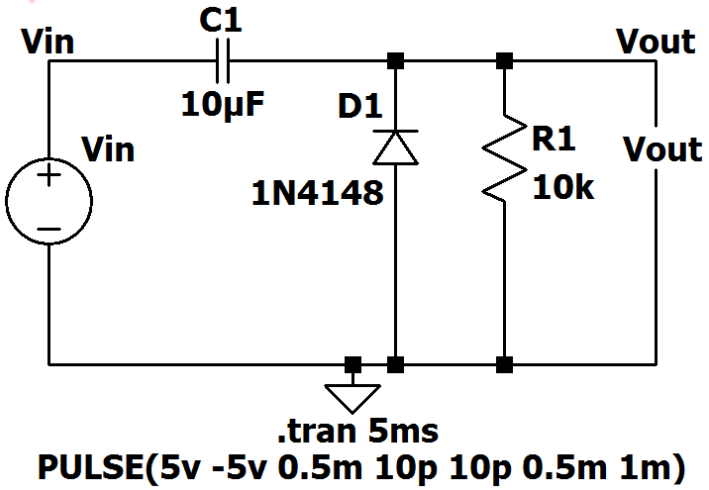

Figure 15: Circuit Schematic

The input & output waveforms are shown below in figure 16.

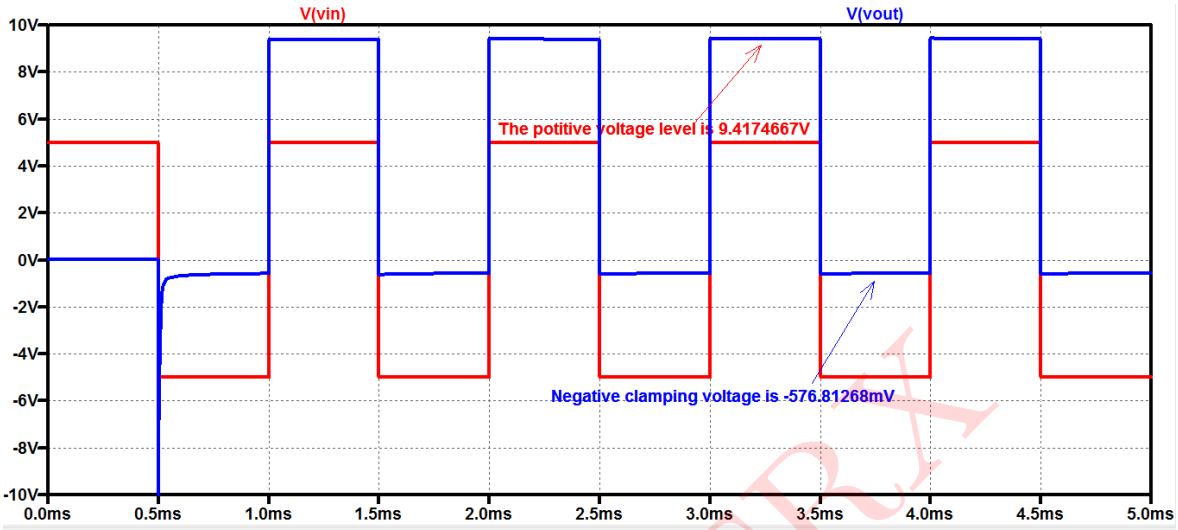

Figure 16: Input & Output Waveforms

Comparison between theoretical and simulated values is given below:

Parameters	Simulated Values	Theoretical Values
Positive voltage level	9.417V	9.3V

Table 3: Numerical 3

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