K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Multi-transistor circuits

Q1. Find the complete frequency respones of the circuit shown in figure 1
Given: $R_1 = R_3 = 25k\Omega$, $R_2 = 4.7k\Omega$, $R_4 = 4.7k\Omega$, $R_L = 1k\Omega$, $R_{sig} = 500\Omega$, $V_A = 100V$, $C_{C1} = C_{C2} = 4.7\mu F$, $C_{E1} = C_{E2} = 100\mu F$, $V_{CC} = 20V$, $\beta 1 = \beta 2 = 180$

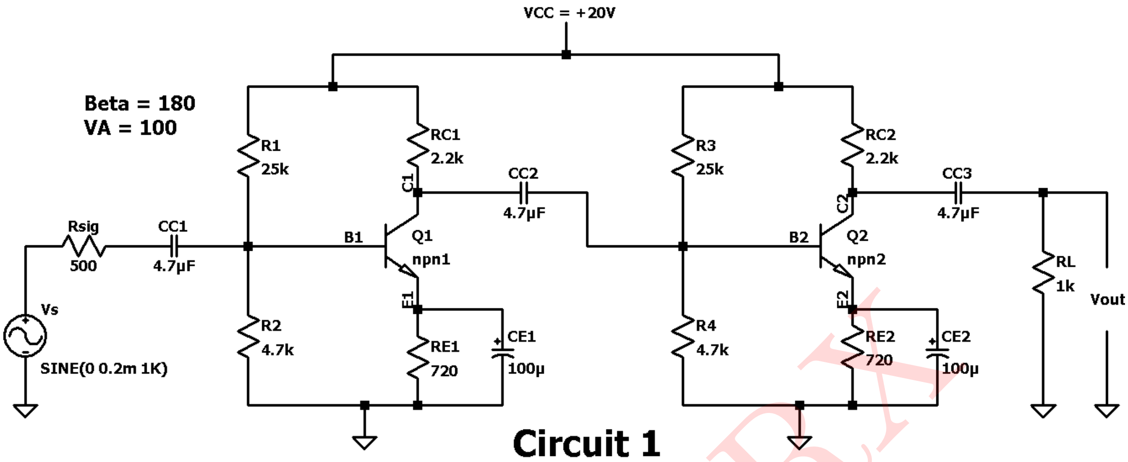

Figure 1: Circuit 1

Solution:

Above network is a CE - CE cascade RC coupled 2 stage amplifier

DC Analysis:

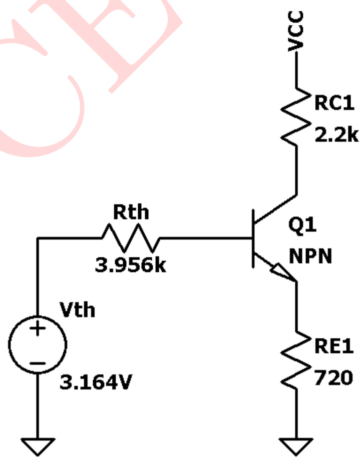

Figure 2: Thevenins equivalent circuit

Due to RC coupling, both the stages Q point are isolated Since both stages are symmetric in parameters and resistor values, DC analysis will be same of both the stages

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right) \times V_{CC}$$

$$V_{TH} = \frac{4.7 \times 10^3}{25 \times 10^3 + 4.7 \times 10^3}$$

$$V_{TH} = \mathbf{3.164V}$$

Applying KVL to the input loop

$R_{TH} = R_1 \mid\mid R_2$

$R_{TH} = 25k \mid\mid 4.7k$

$R_{TH} = \mathbf{3.956k}\Omega$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)R_E}$$

$$I_B = \frac{3.164 - 0.7}{3.956k + 181 \times 720}$$

$I_B = \mathbf{18.350}\mu\mathbf{A}$

$I_C = \beta I_B$

$I_C = \mathbf{3.303mA}$

Applying KVL to output loop

$V_{ECQ} = V_{CC} - I_{EQ}R_{EQ} - I_{CQ}R_{CQ}$

$I_E = I_B + I_C$

$I_C = \beta I_B$

$I_E = (1+\beta)I_B$

$V_{CEQ} = V_{CC} - (1+\beta)I_B R_{EQ} - I_{CQ}R_{CQ}$

$V_{CEQ} = 20 - (3.303 \times 2.2) - (181 \times 18.350 \times 10^{-6} \times 720)$

$V_{CEQ} = \mathbf{10.342V}$

Q point $= (V_{CEQ}, I_{CQ})$

Q point $=$ **(3.303mA , 10.342)**

Small signal parameters:

$$r_o = \frac{V_A}{I_{CQ}} = \frac{100}{3.303mA} = 30.275k\Omega \quad r_\pi = \frac{V_T}{I_{BQ}} = \frac{26 \times 10^{-3}}{18.350 \times 10^{-6}} = \mathbf{1.416}\ \Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{3.303 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{127.038\ mA/V}$$

AC mid frequency equivalent circuit:-

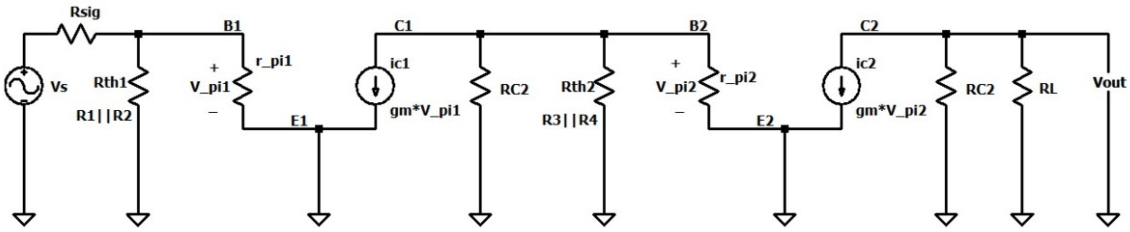

Figure 3: AC mid frequency equivalent circuit

$Z_i = R_1 \mid\mid R_2 \mid\mid r_\pi$

$Z_i = 25k \mid\mid 4.7k \mid\mid 1.416k$

$Z_i = \mathbf{1.0427k\Omega}$

$Z_o = r_o \mid\mid R_L \mid\mid R_C$

$Z_o = 30.275k \mid\mid 2.2k \mid\mid 1k$

$Z_o = \mathbf{672.131\Omega}$

$Z_{in} = Z_i + R_{sig}$

$Z_{in} = 1.0427 + 500$

$Z_{in} = \mathbf{1542.7\Omega}$

A_{V_1} is the gain of first stage

$A_{V_1} = \dfrac{V_1}{V_i}$

$V_1 = -g_m V_{\pi 1}(r_o \mid\mid R_C \mid\mid R_3 \mid\mid R_4 \mid\mid r_{\pi 2})$

$V_i = V_{\pi 1}$

$A_{V_1} = -g_m(r_o \mid\mid R_C \mid\mid R_3 \mid\mid R_4 \mid\mid r_{\pi 2})$

$A_{V_1} = -127.038(30.275k \mid\mid 2.2k \mid\mid 25k \mid\mid 2.7k \mid\mid 1.416k)$

$A_{V_1} = -127.038(30.275k \mid\mid 2.2k \mid\mid 25k \mid\mid 2.7k \mid\mid 1.416k)$

$A_{V_1} = -127.038(2.050k \mid\mid 3.956k \mid\mid 1.516k)$

$A_{V_1} = \mathbf{-87.796}$

A_{V_2} is the gain of second stage

$A_{V_2} = \dfrac{V_o}{V_1}$

$A_{V_2} = -g_m(r_{o2} \mid\mid R_{C2} \mid\mid R_L)$

$A_{V_2} = -127.038(30.275k \mid\mid 2.2k \mid\mid 1k)$

$A_{V_2} = -127.038(672.131)$

$A_{V_2} = \mathbf{-83.386}$

Overall MidBand Voltage Gain:

$A_{V_T} = A_{V_1} \times A_{V_2}$

$A_{V_T} = -87.796 \times -83.386$

$A_{V_T} = \mathbf{7496.549}$

A_{V_T} with $R_{sig} = \dfrac{Z_i}{Z_i \times R_{sig}} \times A_{V_T}$

A_{V_T} with $R_{sig} = \dfrac{1.0427k}{1.0427k \times 500} \times 7496.549$

A_{V_T} with $R_{sig} = \mathbf{5066.964}$

A_{V_T} with R_{sig} in dB $= 20\log(5066.864)$

A_{V_T} with R_{sig} in dB $= \mathbf{74.094dB}$

SIMULATED RESULTS:
Above circuit was simulated in LTSpice and results are presented below:

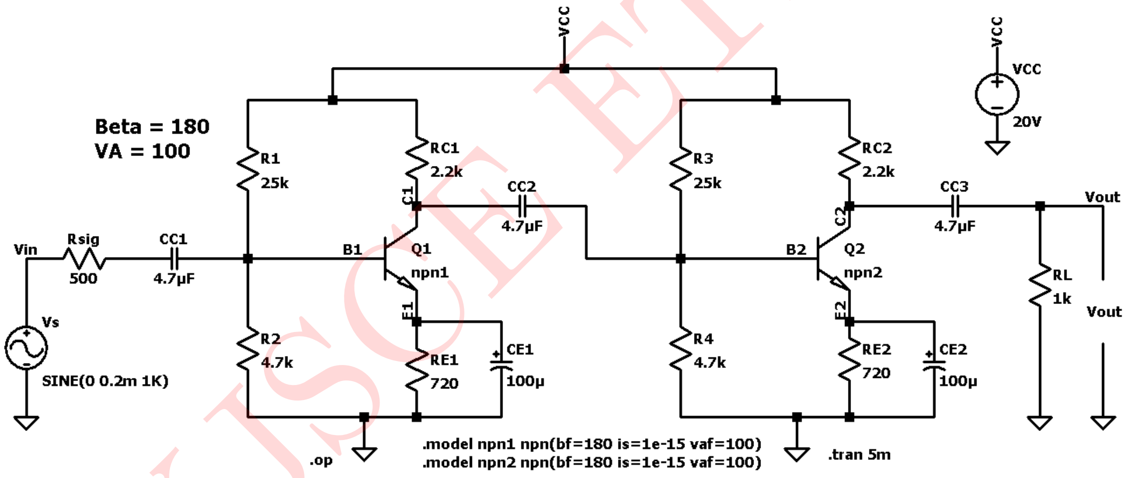

Figure 4: Circuit Schematic

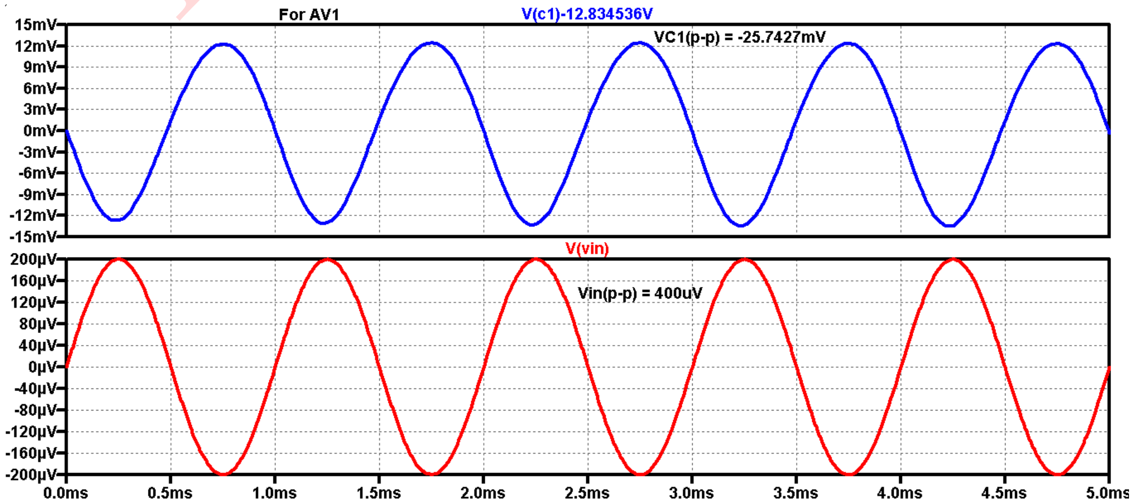

Figure 5: Input output waveforms for Voltage gain A_{V_1}

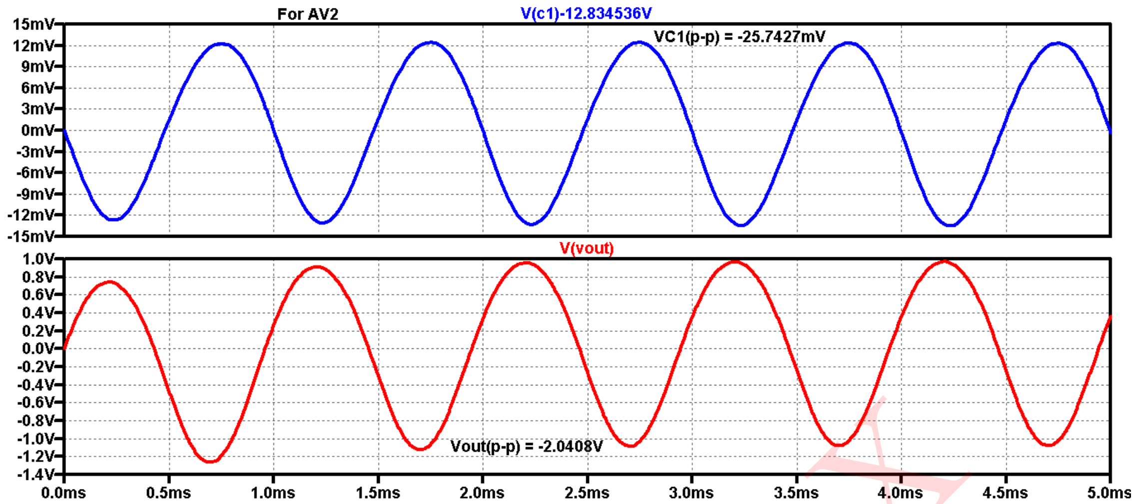

Figure 6: Input output waveforms for Voltage gain A_{V_2}

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
A_{V_1}: 1^{st} Stage	-64.353	-87.736
A_{V_1}: 1^{st} Stage in dB	36.171	38.869
A_{V_2}: 2^{nd} Stage	-79.281	-85.386
A_{V_2}: 2^{nd} Stage in dB	37.983	38.627
Q point: 1^{st} Stage	(3.257mA,10.478V)	(3.303mA,10.342V)
Q point: 2^{nd} Stage	(3.257mA,10.478V)	(3.303mA,10.342V)
Overall Voltage gain A_{V_T}	74.1547	74.094
Input impedence of 1^{st} Stage	-	1.0427kΩ
Output impedence of 2^{nd} Stage	-	672.131Ω

Table 1: Numerical 1

Q2. For the the circuit shown in figure 7, Find:

1. Determine Qpoint for both stages.
2. Draw mid frequency equivalent circuit
3. Calculate A_{V_1}, A_{V_2}, A_{V_T}
4. Calculate Z_i and Z_o

Given: $R_1 = R_3 = 22M\Omega$, $R_2 = 18M\Omega$, $R_4 = 18M\Omega$, $R_L = 10k\Omega$, $R_{sig} = 100\Omega$, $V_A = 100V$, $C_{C1} = C_{C2} = C_{C3} = 4.7\mu F$, $C_{S1} = C_{S2} = 47\mu F$, $V_{DD} = 24V$

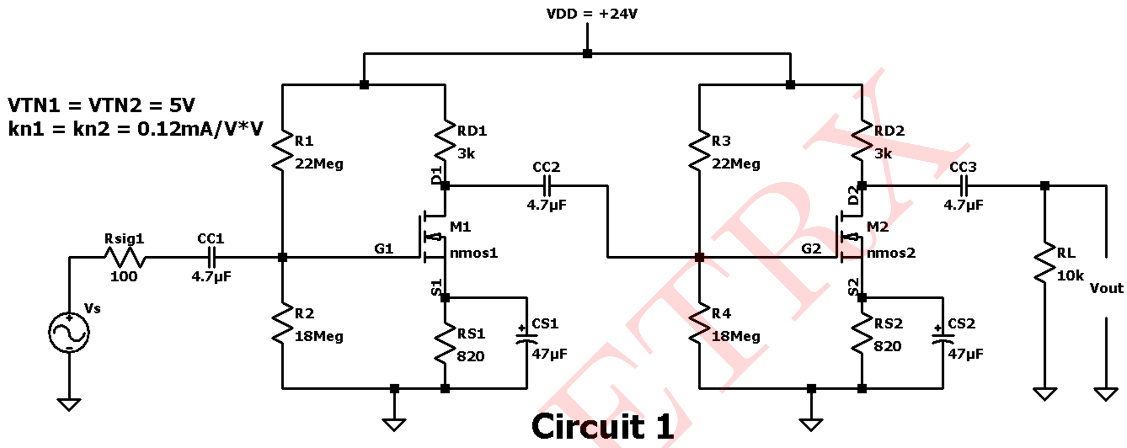

Figure 7: Circuit 1

Solution:

Above network is a CS - Cs cascade RC coupled 2 stage amplifier

DC Analysis:

Due to RC coupling, both the stages Q point are isolated
Since both stages are symmetric in parameters and resistor values, DC analysis will be same of both the stages

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) \times V_{DD}$$

$$V_{TH} = \frac{18M}{18M + 22M} \times 24$$

$$V_{TH} = \mathbf{10.8V}$$

$$V_{GS} = V_G - V_S$$

$$V_{GS} = 1.82 - I_D R_S$$

$$V_{GS} = 10.8 - (820)I_D \text{ ——— (1)}$$

$$I_D = k_n \left(V_{GS} - V_{TN}\right)^2$$

$$I_D = 0.12 \times 10^{-3} \left(V_{GS} - 5\right)^2 \text{ ——— (2)}$$

Solving equations (1) and (2)

$V_{GS} = 10.8 - 820 \times 0.12 \times 10^{-3}(V_{GS}^2 - 10V_{GS} + 25)$

$V_{GS} = 10.8 - 0.0984V_{GS}^2 + 0.0984V_{GS} - 2.46$

$0.0984V_{GS}^2 + 0.016_{GS} - 8.34 = 0$

$V_{GS} = -9.287V or 9.125V$

$V_{GS} = \mathbf{9.125V} \qquad \because (V_{GS} > VP)$

$I_D = 0.12 \times 10^{-3}\,(9.125 - 5)^2\ I_{DQ} = \mathbf{2.0418\ mA}$

Q point =(9.125V, 2.0418mA)

Small signal parameters:

$g_m = 2k_n\,(V_{GS} - V_{TN}) = 2 \times 0.12 \times 10^{-3}(9.125 - 5) =$**0.99 mA/V**

AC mid frequency equivalent circuit:-

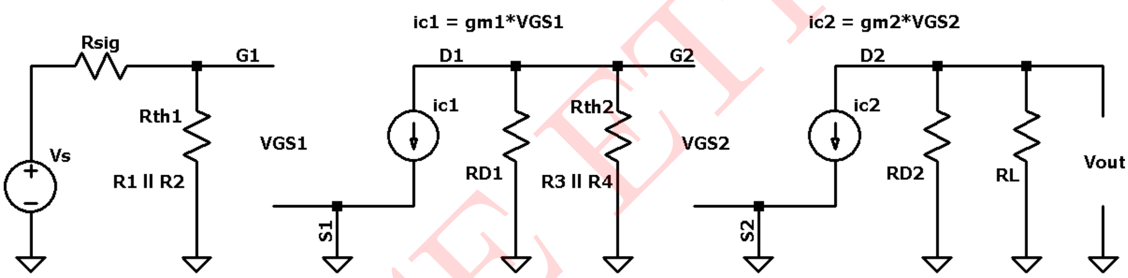

Figure 8: AC mid frequency equivalent circuit

$$A_{V_{mid}} = \frac{V_{out}}{V_S} = \frac{V_{out}}{V_1} \times \frac{V_1}{V_in} \times \frac{V_in}{V_S}$$

Gain of second stage $A_{V_2} = \dfrac{V_{out}}{V_1}$

$$\frac{V_{out}}{V_1} = \frac{g_{m2}V_{gs2}(R_D||R_L)}{V_{gs2}}$$

$$\frac{V_{out}}{V_1} = g_{m2}(R_D||R_L)$$

$A_{V_2} = -0.99m(3k||10K)$

$A_{V_2} = -2.2839$

A_{V_2} in dB =$20\log(2.2839) =$ **7.1735dB**

Gain of first stage $A_{V_1} = \dfrac{V_1}{V_{in}}$

$$\frac{V_1}{V_{in}} = \frac{g_{m1}V_{gs1}(R_D||R_3||R_4)}{V_{gs1}}$$

$$\frac{V_1}{V_{in}} = g_{m2}(R_D||R_3||R_4)$$

$A_{V_2} = -0.99(3k||22M||18M)$

$A_{V_2} = -2.9690$

A_{V_2} in dB $= 20\log(2.9690) = 9.4522dB$

$$\frac{V_{in}}{V_S} = \frac{R_1||R_2}{R_1||R_2 + R_{sig}} = \frac{22M||18M}{(22M||18M) + 100} = 0.999$$

$$\frac{V_{in}}{V_S} = \mathbf{0.999 \approx 1}$$

$$A_{V_{mid}} = \frac{V_{out}}{V_S} = \frac{V_{out}}{V_1} \times \frac{V_1}{V_in} \times \frac{V_{in}}{V_S}$$

$$A_{V_{mid}} = (-2.2830) \times (-2.9690) \times 1$$

$$A_{V_{mid}} = \mathbf{6.78089}$$

$A_{V_{mid}}$ in dB $= 20\log(6.78089) =$16.6257dB

Now, $V_{out} = 6.78089 \times 20mV$

$$V_{out} = \mathbf{135.6178mV}$$

Input Impedence:

$$Z_i = R_1||R_2 = 22M||18M = 9.9M\Omega$$

$$Z_{is} = R_{sig} + Z_i = 9.9001M\Omega$$

$$Z_o = R_D||R_L = 3k||10k$$

$$Z_o = \mathbf{2.307\ k\Omega}$$

SIMULATED RESULTS:
Above circuit was simulated in LTSpice and results are presented below:

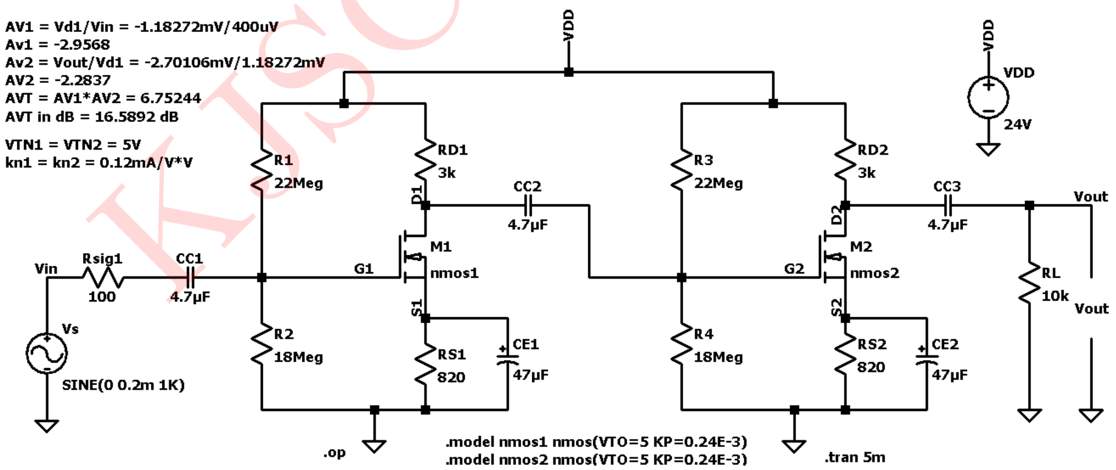

Figure 9: Circuit Schematic

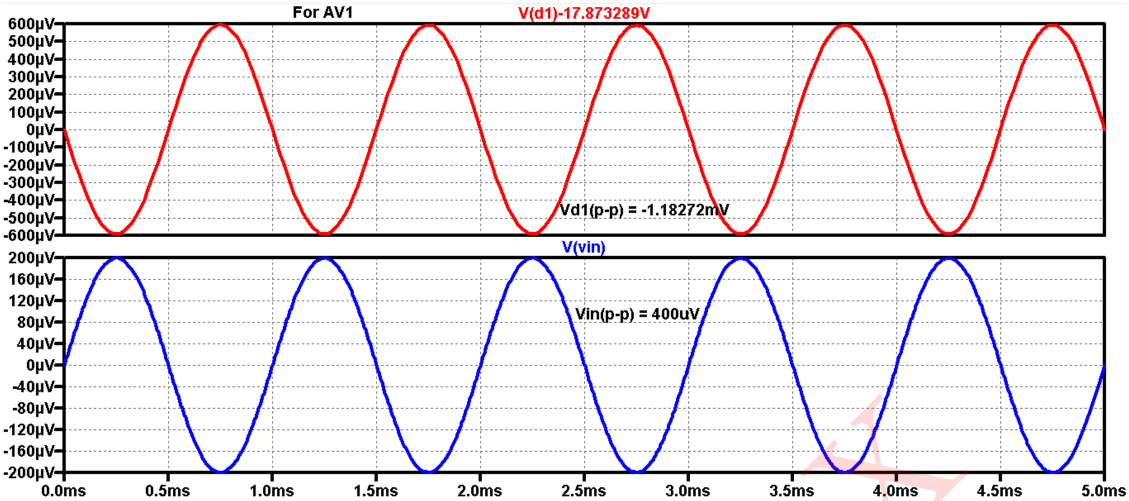

Figure 10: Input output waveforms for Voltage gain A_{V_1}

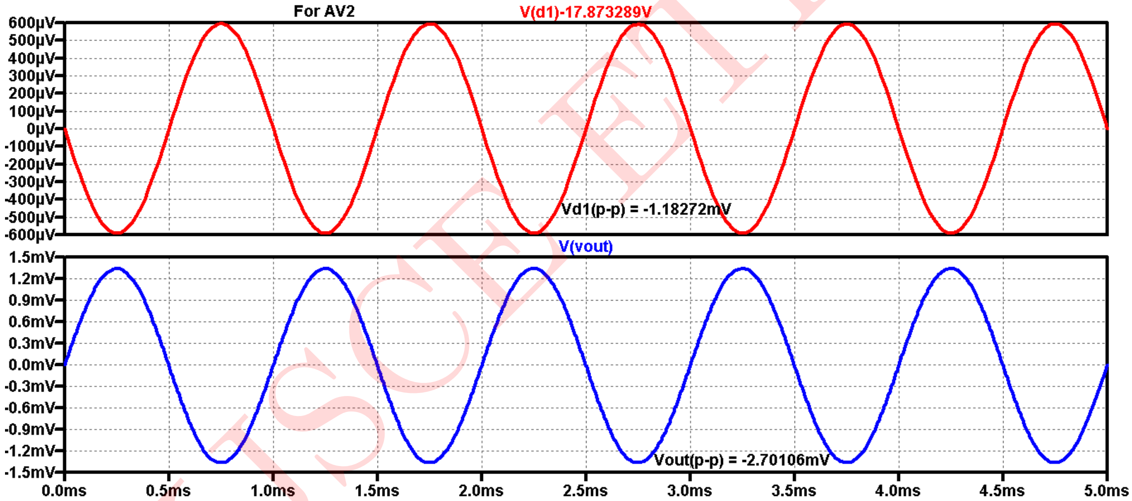

Figure 11: Input output waveforms for Voltage gain A_{V_2}

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
A_{V_1}: 1^{st} Stage	-2.9568	-2.9690
A_{V_1}: 1^{st} Stage in dB	9.4146	9.4522
A_{V_2}: 2^{nd} Stage	-2.2837	-2.2839
A_{V_2}: 2^{nd} Stage in dB	7.1727	7.1735
Q point: 1^{st} Stage	(2.042mA, 9.1254V)	(2.0418mA, 9.125V)
Q point: 2^{nd} Stage	(2.042mA, 9.1254V)	(2.0418mA, 9.125V)
Overall Voltage gain A_{V_T}	16.5892	9.4522
Input impedence of 1^{st} Stage	–	9.9MΩ
Output impedence of 2^{nd} Stage	–	2.307KΩ

Table 2: Numerical 2

Q3. Calculate DC voltages at each mode and DC currents in the give circuit.

Given: $R_1 = 100K\Omega$, $R_2 = 50K\Omega$, $R_{C1} = 5K\Omega$, $R_{C2} = 1.5k\Omega$, $R_{E1} = R_{E2} = 2k\Omega$, $V_{CC} = 5V$

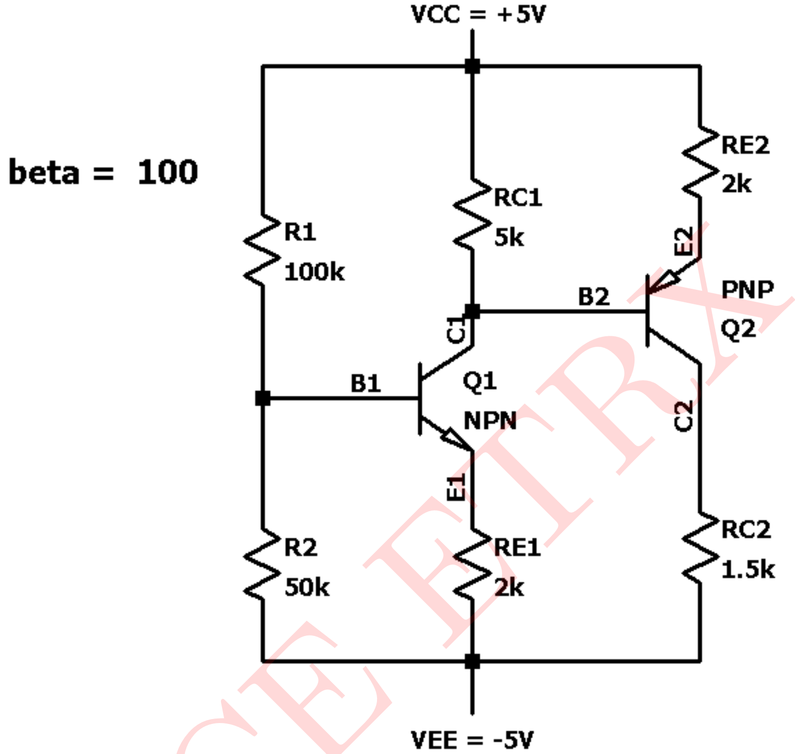

Figure 12: Circuit 1

Solution:

Considering the thevenins equivalent of base circuit transistor Q1

$R_{TH} = R1 \,||\, R2 = 100k \,||\, 50k = 33.3\text{K}\Omega$

$V_{TH} = \left(\left(\frac{R_2}{R_1 + R_2}\right) \times (5 - (-5))\right) - 5 = \left(\frac{50k}{150k}\right) \times 10 - 5 = -1.67\text{V}$

Applying KVL to the BE loop of Q1

$V_{TH} = I_{B1}R_{TH} + V_{BE(on)} + I_{E1}R_{E1} - 5$

$I_{E1} = I_{B1} + \beta I_{B1}$

$I_{B1} = \frac{V_{TH} - V_{BE(on)} + 5}{R_{TH} + (1 + \beta)R_{E1}}$

$I_{B1} = \frac{-1.67 - 0.7 + 5}{33.3k + 101(2k)} = \mathbf{11.177\mu A}$

$I_{C1} = \beta I_{B1} = \mathbf{1.11mA}$

$I_{E1} = I_{B1} + I_{C1} = 11.117\mu\text{A} + 1.1177\text{mA} = \mathbf{1.1288mA}$

Summing currents at collector of Q1

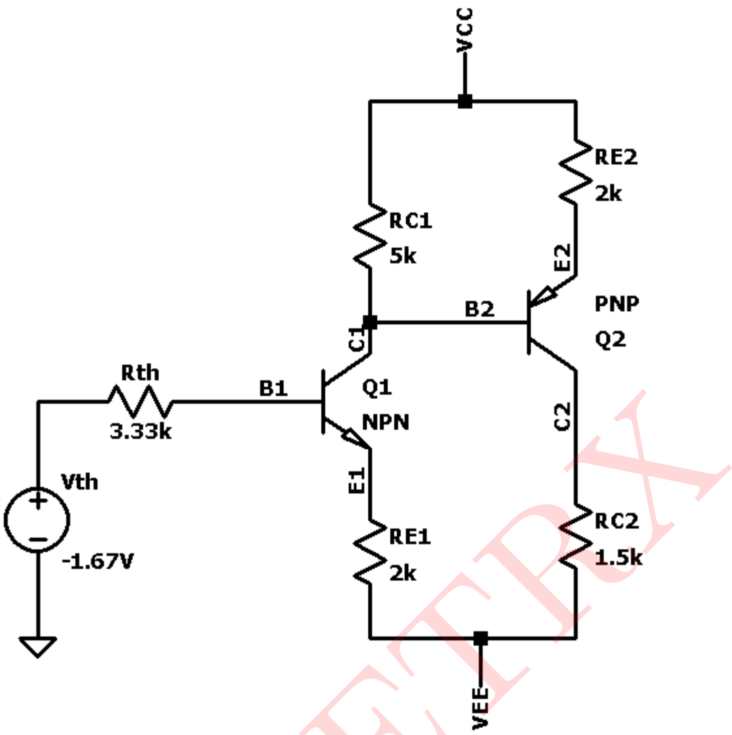

Figure 13: Thevenins equivalent of base circuit transistor Q1

$$I_{R1} + I_{B2} = I_{C1}$$

$$I_{R1} = \frac{5 - V_{C1}}{R_{C1}}$$

$$\frac{5 - V_{C1}}{R_{C1}} + I_{B2} = I_{C1} \text{ ——— } (\ 1\ )$$

Also, I_{B2} can be written as

$$I_{B2} = \frac{5 - (V_{C1} + 0.7)}{(1 + \beta)R_{E2}} \text{ ——— } (\ 2\ )$$

Put (2) in (1)

$$\frac{5 - V_{C1}}{R_{C1}} + \frac{5 - (V_{C1} + 0.7)}{(1 + \beta)R_{E2}} = I_{C1}$$

$$\frac{5 - V_{C1}}{5k} + \frac{5 - (V_{C1} + 0.7)}{(101)2k} = 1.1177mA$$

$$(101)(5 - V_{C1}) + 5(5 - 0.7 - V_{C1}) = (5 \times 101)(1.117)$$

$$505 - 101V_{C1} + 21.5 - 5V_{C1} = 564.4385$$

Solving Equation

$$V_{C1} = \mathbf{-0.482V}$$

$$I_{R1} = \frac{5 - V_{C1}}{R_{C1}} = \frac{5 - (-0.482)}{5k} = \mathbf{1.096mA}$$

$$V_{E2} = V_{B2} + V_{EB(on)}$$

$$V_{E2} = V_{C1} + V_{EB(on)} = -0.482 + 0.7 = \mathbf{0.218}$$

$$I_{E2} = \frac{V_{CC} - V_{E2}}{R_{E2}} = \frac{5 - 0.218}{2k} = \mathbf{2.391mA}$$

$$I_{C2} = \left(\frac{\beta}{1+\beta}\right) I_{E2} = \frac{100}{101} \times 2.391mA = \mathbf{2.367mA}$$

$I_{B2} = I_{E2}/(1+\beta) = 2.391mA/101 = \mathbf{23.673\mu A}$

Now, $V_{E1} = I_{E1}R_{E1} - V_{EE} = 1.1288 \times 2 - 5 = -\mathbf{2.742V}$

$V_{C2} = I_{C2}R_{C2} - V_{EE} = 2.3671 \times 1.5 - 5 = -\mathbf{1.449V}$

$V_{B1} = V_{BE(on)} + V_{E1} = 0.7 + (-2.742) = -\mathbf{2.042V}$

$V_{CE1} = V_{C1} - V_{E1} = -0482 - (-2.742) = \mathbf{2.25V}$

$V_{EC2} = V_{E2} - V_{C2} = 0.218 - (-1.449) = \mathbf{1.667V}$

SIMULATED RESULTS:

Above circuit was simulated in LTSpice and results are presented below:

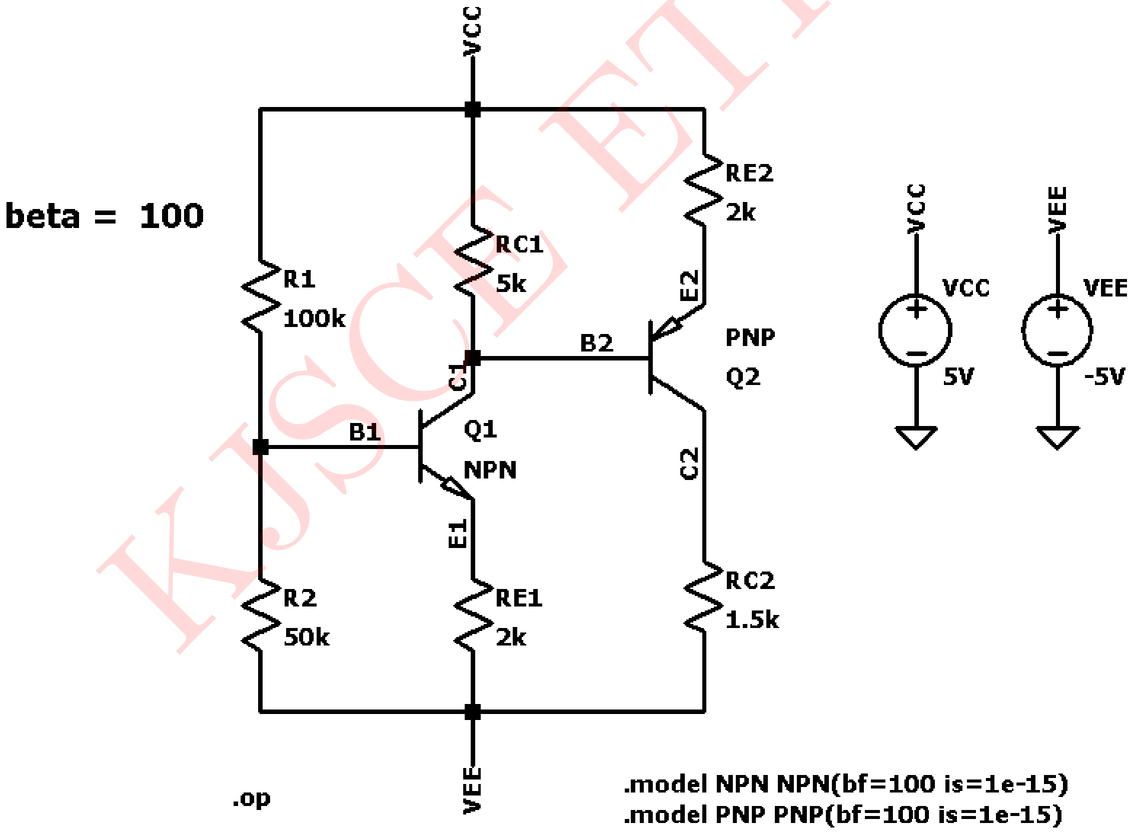

Figure 14: Circuit Schematic

Comparison of Theoretical and Simulated Values:

Parameters	Theoretical	Simulated
I_{B1}	11.115μA	11.177μA
I_{C1}, I_{E1}	1.115mA, 1.2227mA	1.1177mA, 1.1288mA
I_{B2}	23.2916μA	23.673μA
I_{C2}, I_{E2}	2.3291mA,2.352mA	2.367mA, 2.391mA
V_{C1}	-0.441V	-0.482V
V_{C2}	-1.5062	-1.449V
V_{E1}	-2.7546	-2.742V
V_{E2}	-0.295V	0.218V
V_{B1}	-2.0371V	-2.042V
V_{B2}	-0.441V	-0.482V
V_{CE1}	2.3132V	2.27V
V_{CE2}	1.8012V	1.667V

Table 3: Numerical 3

****