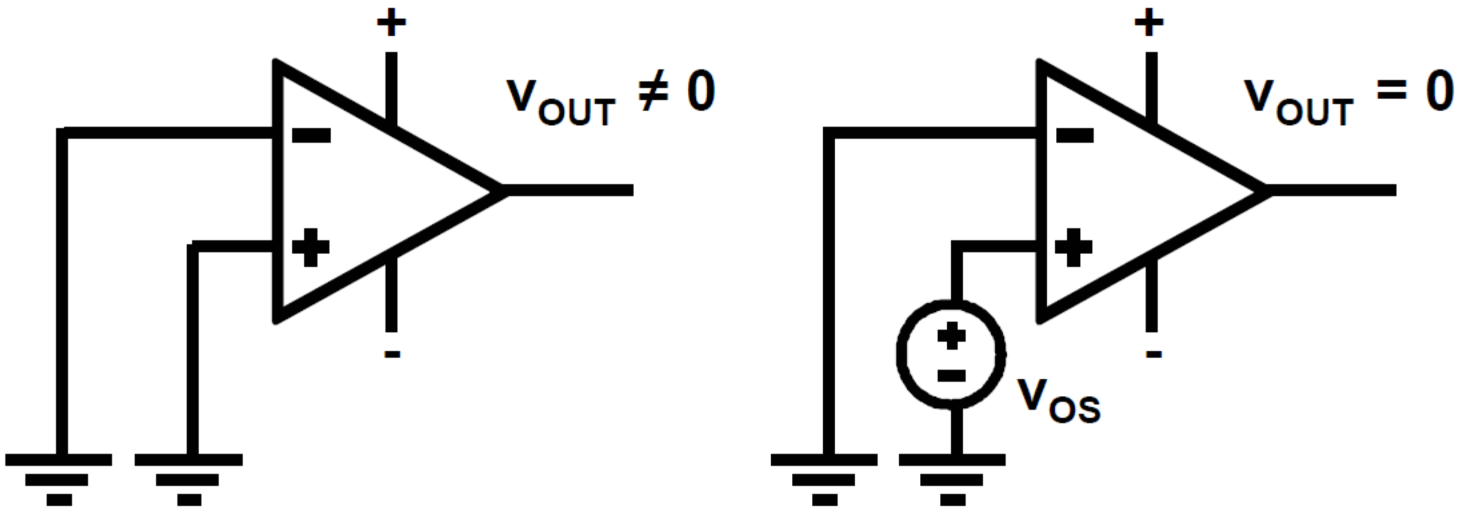
北京航空航天大学 BEIHANG UNIVERSITY | 微电子学院

CMOS模拟集成电路设计

第四章：失调与CMRR

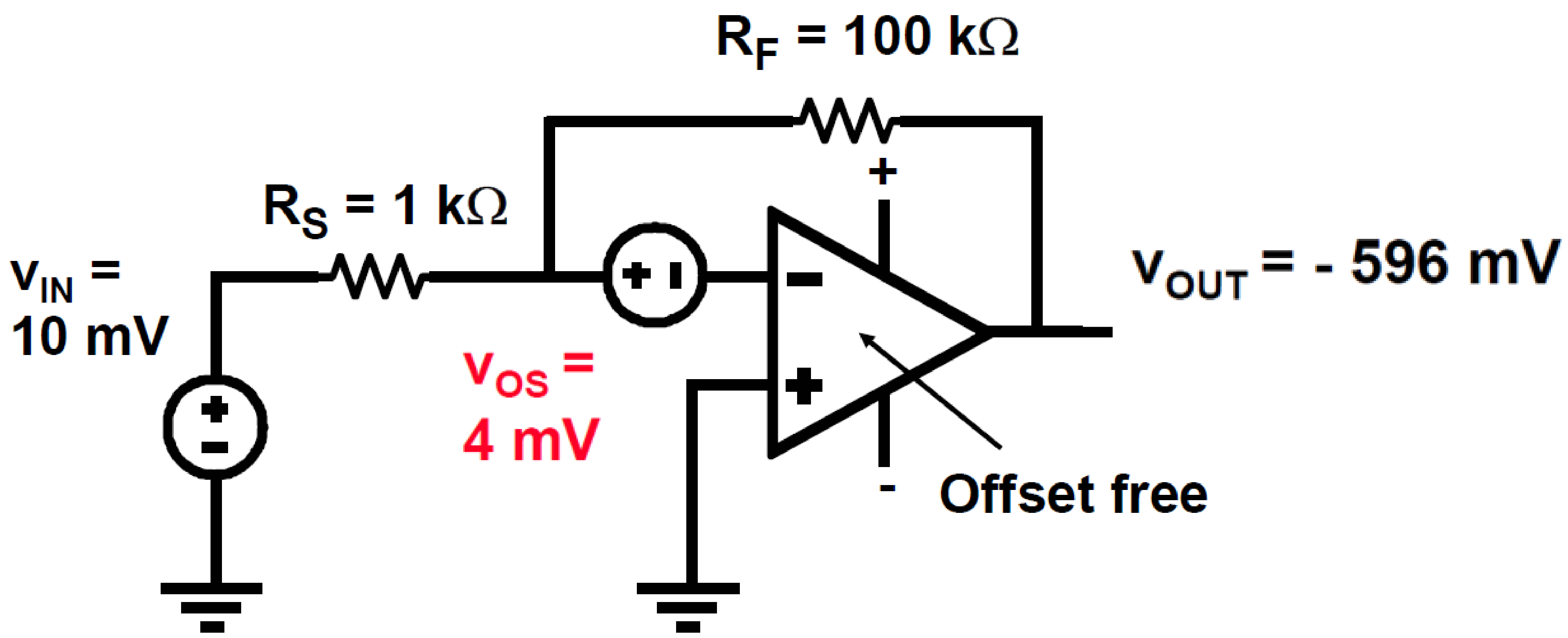
胡远奇

失调(Offset)的定义

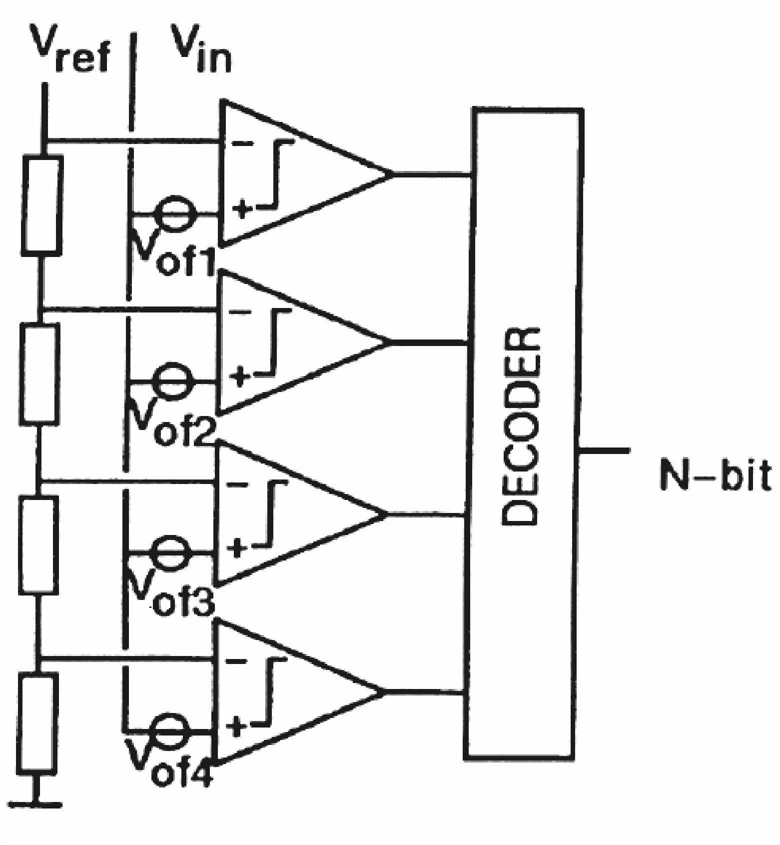


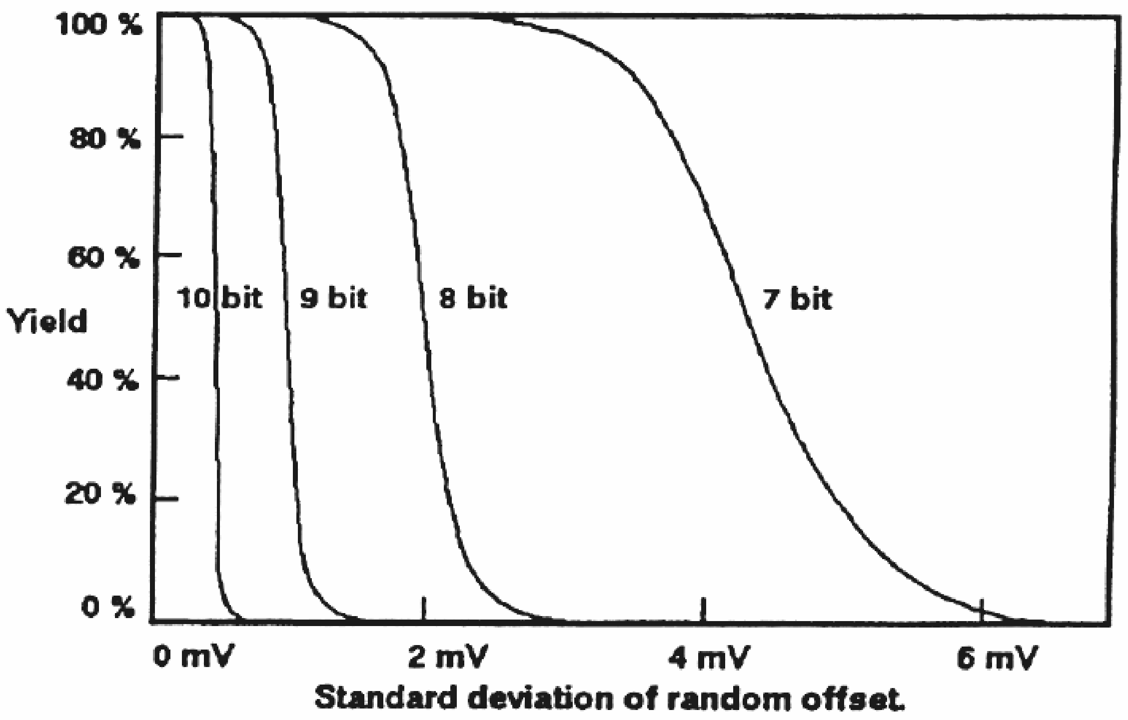
- 失调电压V_{OS}：使输出电压为零时的两端输入电压之差
  - 可以加在任意一端

失调(Offset)的影响



失调(Offset)的影响





n-bit Flash-ADC with offset

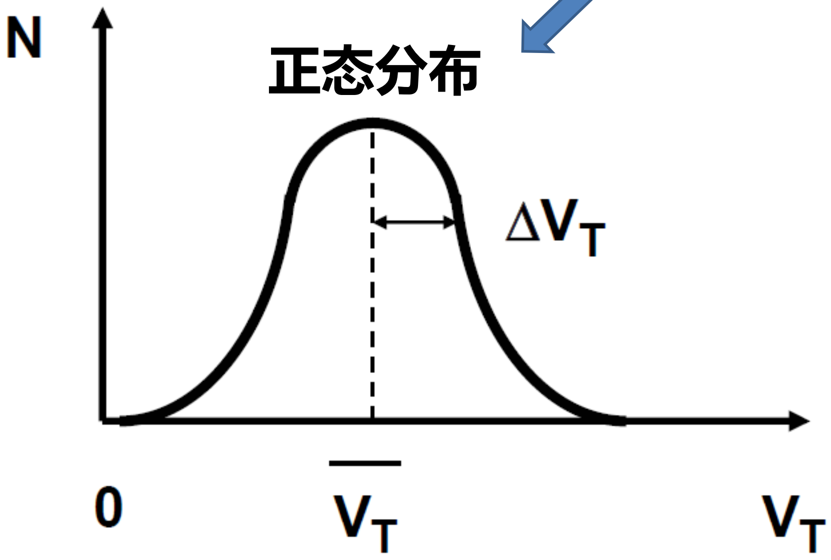
Ref: Pelgrom, IEDM 1998, pp.789.

失调与CMRR

- **随机性失调和$CMRR_R$**
- 系统性失调和$CMRR_S$
- 设计守则

随机失调：阈值电压的失配

$$I_{DS} = K' \, W/L (V_{GS} - V_T)^2$$



$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}}$$

$$A_{VT} \sim t_{ox} \sqrt[4]{N_B}$$

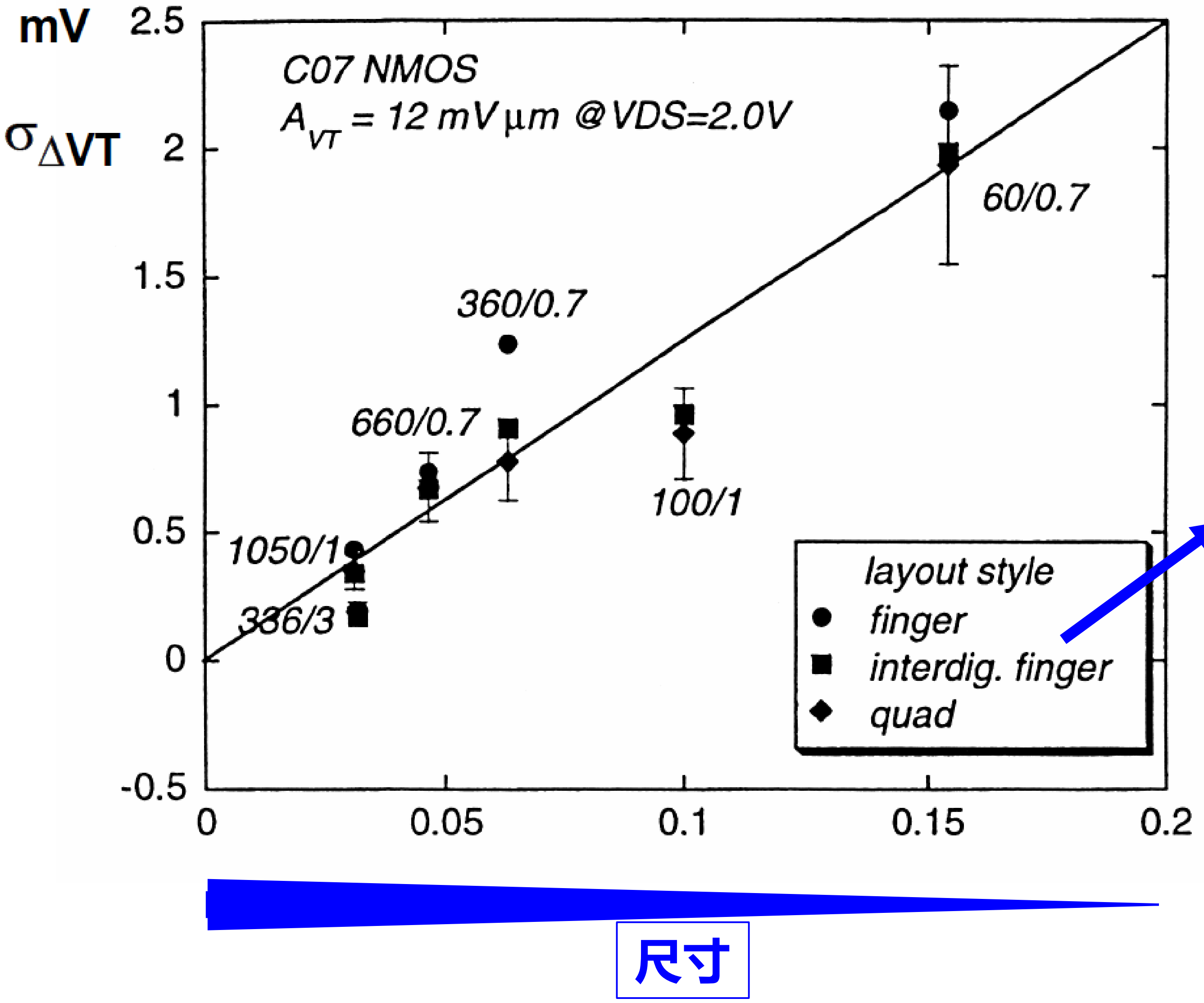
氧化层厚度 & 衬底参杂浓度

$A_{VT} \approx$ 5 mV um
for 0.25 um nMOST

+50 % for pMOST

❑估算0.25um工艺下、尺寸为16um/1um的PMOS差分对由阈值电压失配造成的最大失调电压？（要求99.5%良率）

阈值电压失配的标准差



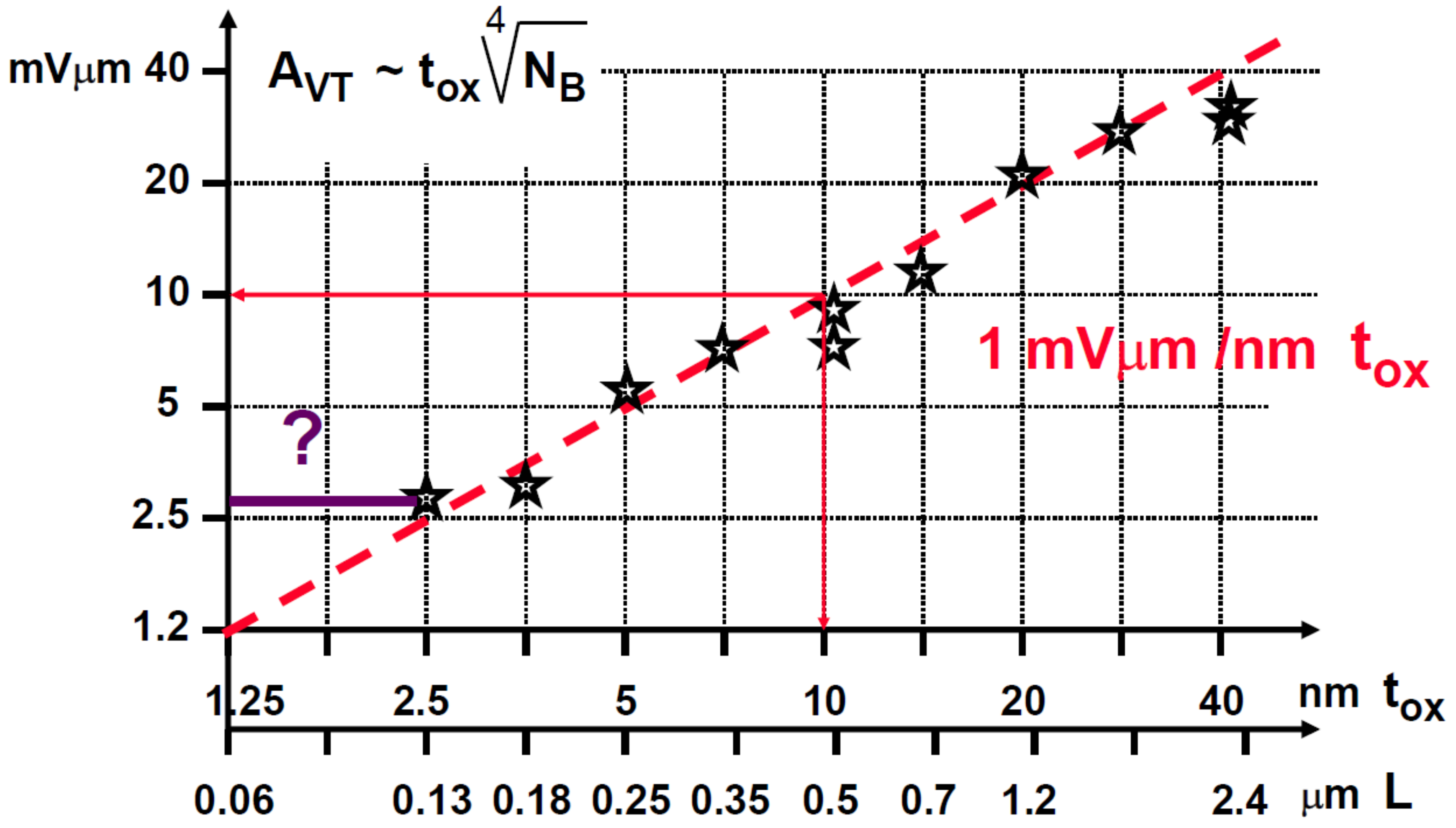
$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}}$$

版图方式有一定的作用，但是尺寸才是决定性的

$1/\sqrt{WL}$

$1/\mu m$

阈值电压失配的系数A_{VT}



- 某工厂55nm工艺的A_{VT}=2.05e-9

随机失调：工艺与尺寸的失配

$$I_{DS} = K' \, W/L(V_{GS} - V_T)^2$$

$$\frac{\Delta K'}{\overline{K'}} = \frac{A_{K'}}{\sqrt{WL}}$$

$$A_{K'} \approx 0.0056 \text{ um}$$

+50 % for pMOST

$$\frac{\Delta W/L}{\overline{W/L}} = A_{WL}\sqrt{\frac{1}{W^2}+\frac{1}{L^2}}$$

$$A_{WL} \approx 0.02 \text{ mV um}$$

+50 % for pMOST

- 参数K’ 造成的变化相对较小
- A_{WL}与工艺的相关性不强

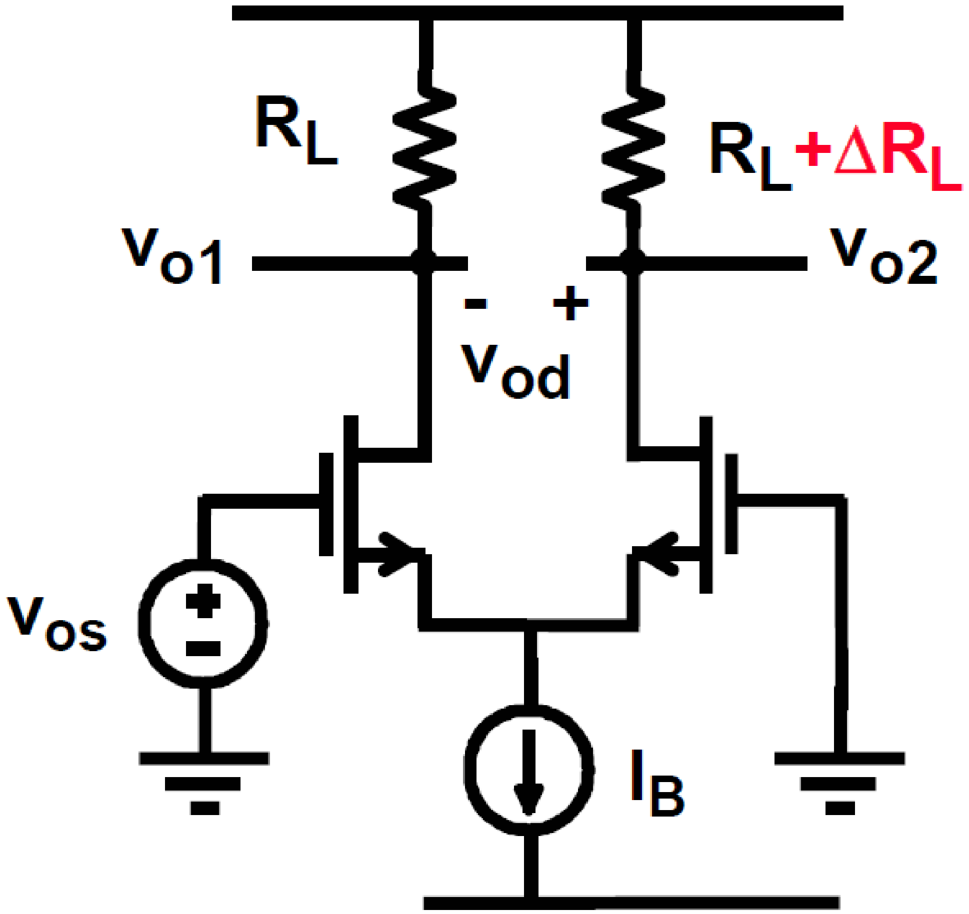
NMOS的失配参数

Techno L (μm) / t_{ox} (nm)	2.5 / 50	1.2 / 25	0.7 / 15	0.5 / 11	0.35 / 8	0.25 / 6
A_{VT} (mV μm)	30	21	13	7.1	6	⇨ 3
A_{WL} (% μm)	2.5	1.8	2.5	1.3	2	⇨ 1.8

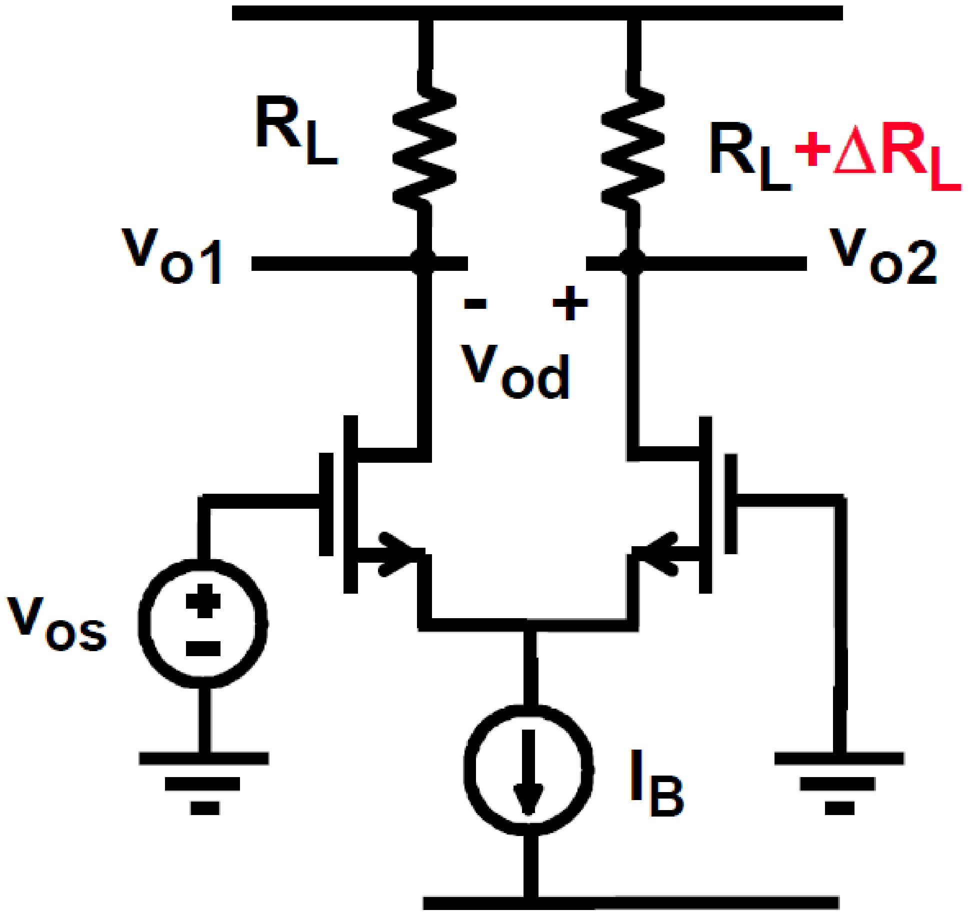
A_{WL}的单位是**um**，可以听过设计**尺寸**或**偏置电压**减小其影响

A_{VT}的单位是**mV*um**，只能通过设计**尺寸**减小其影响

差分对中的随机失调



差分对中的随机失调



$$v_{od} = \Delta R_L \frac{I_B}{2}$$

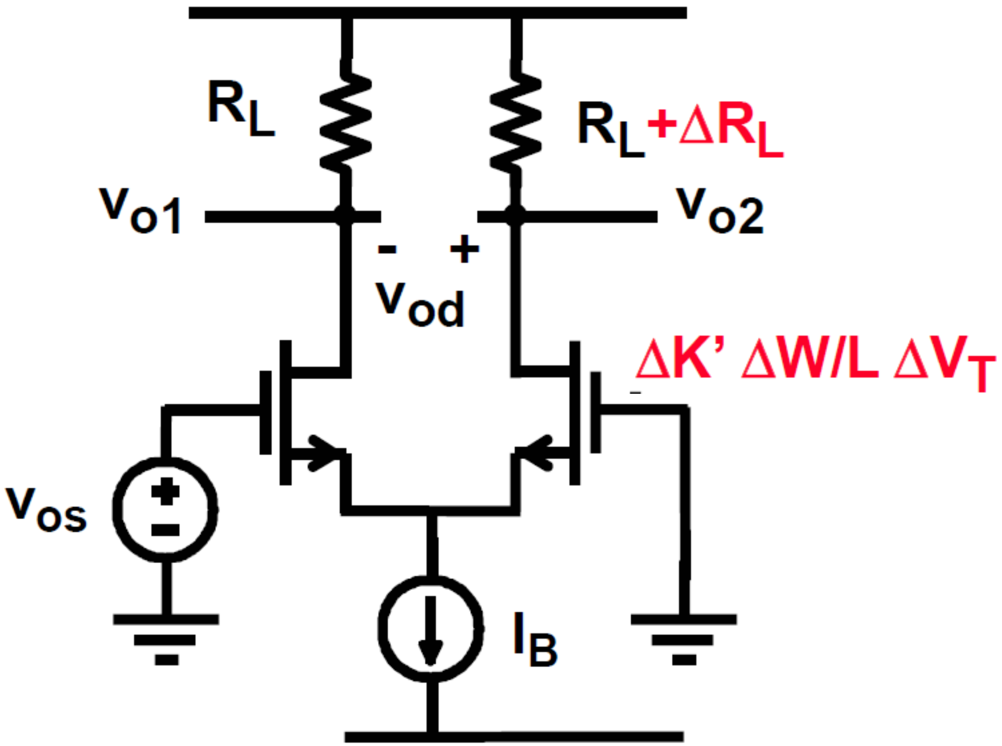
$$v_{os} = \frac{v_{od}}{g_m R_L}$$

$$v_{os} = \frac{\Delta R_L}{R_L} \frac{I_B}{2g_m}$$

- 需要减小 $V_{GS}-V_T$

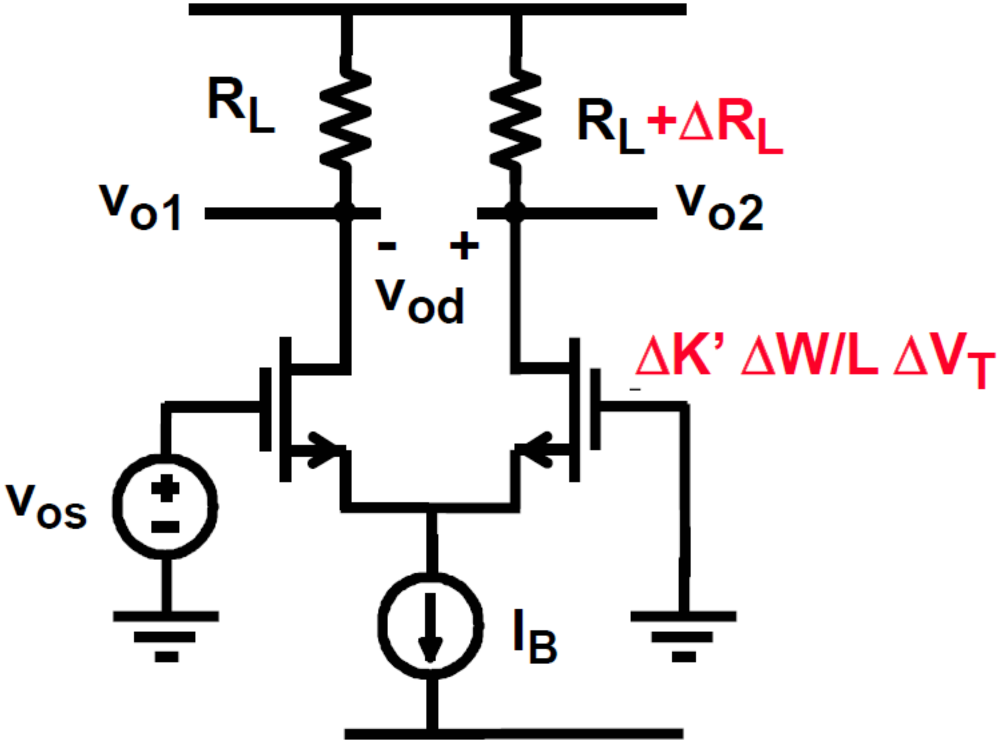
$$v_{os} = \frac{\Delta R_L}{R_L} \frac{V_{GS} - V_T}{2}$$

差分对中的随机失调



$$I_{DS} = K'\ W/L(V_{GS} - V_T)^2$$

差分对中的随机失调



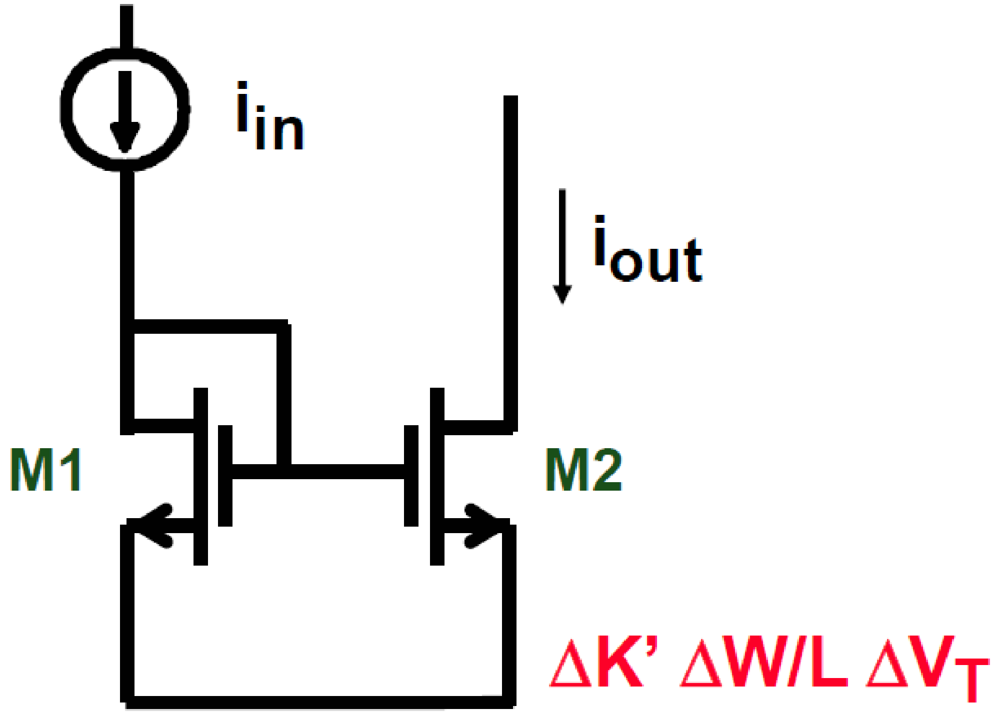
$$I_{DS} = K'\ W/L(V_{GS} - V_T)^2$$

差分对应尽可能的

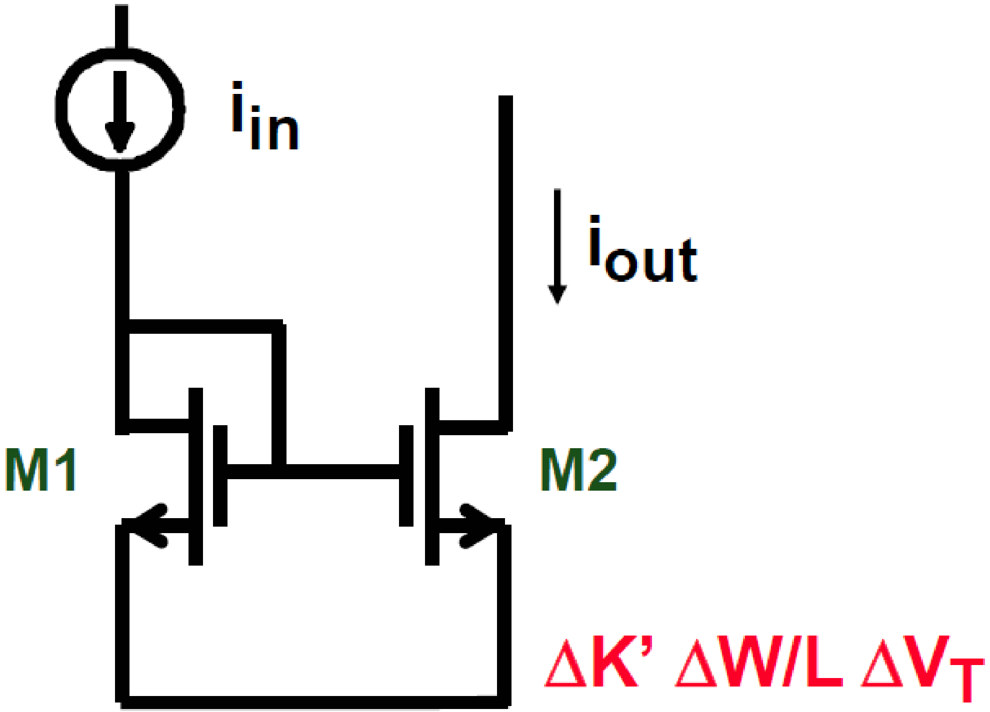
$$\boxed{V_{GS}-V_T \downarrow}$$

$$v_{OS} = \Delta V_T + \frac{V_{GS} - V_T}{2}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L}\right)$$

电流镜中的随机失调



电流镜中的随机失调



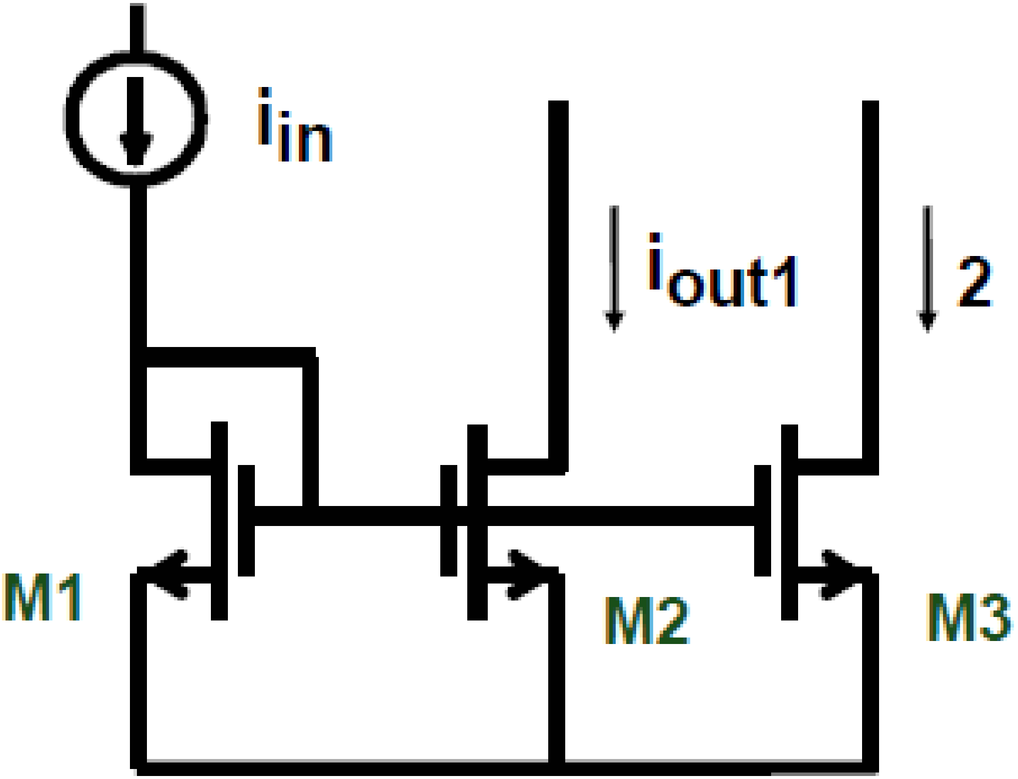
$$\frac{\Delta I_{out}}{I_{out}} = \frac{\Delta V_T}{(V_{GS} - V_T)/2} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L}$$

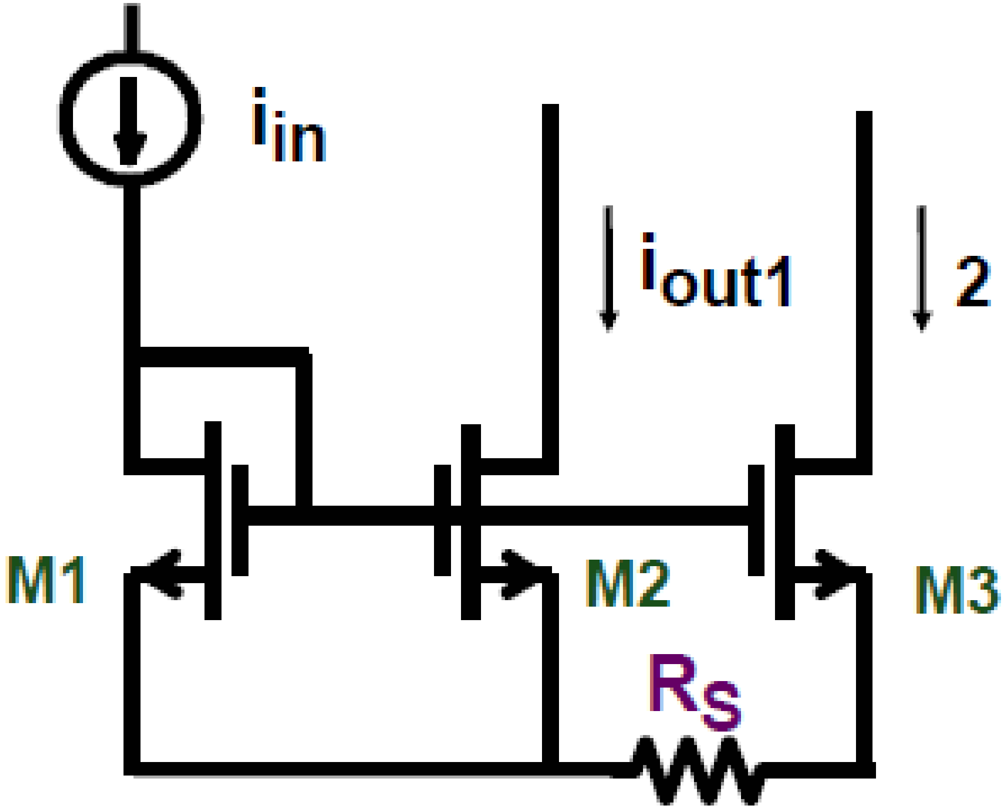
- A_{WL}是主要失配源

电流镜应尽可能的

$\boxed{V_{GS}-V_T \uparrow}$

电流镜中的其他失调因素





$\Delta K'$ $\Delta W/L$ ΔV_T

$\Delta K'$ $\Delta W/L$ ΔV_T R_S

输出电流的失配

$$I_{DS} = K' W/L(V_{GS} - V_T)^2$$

$$\Downarrow$$

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_T)^2$$

定义：总的电流失配由 β 失配和 V_T 失配造成

$$\frac{\Delta I_{DS}}{I_{DS}} =$$

$$\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) =$$

输出电流的失配

$$I_{DS} = K' W/L(V_{GS} - V_T)^2$$

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_T)^2$$

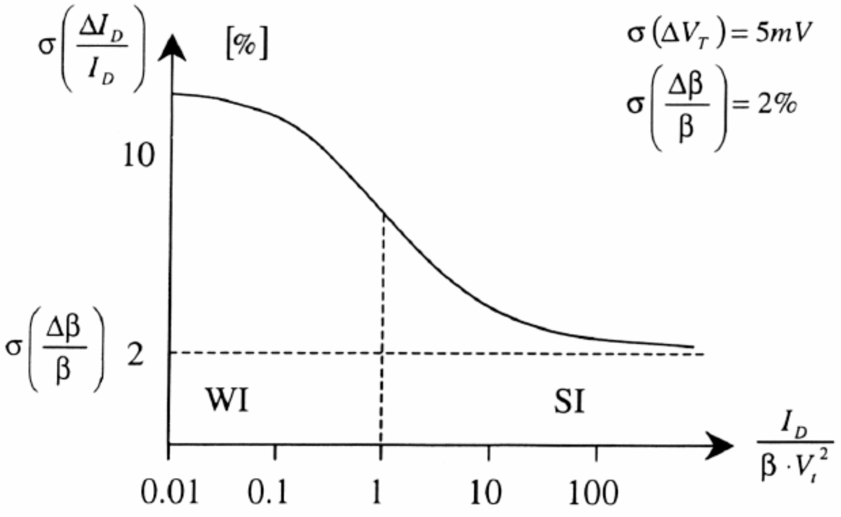
定义：总的电流失配由 β 失配和 V_T 失配造成

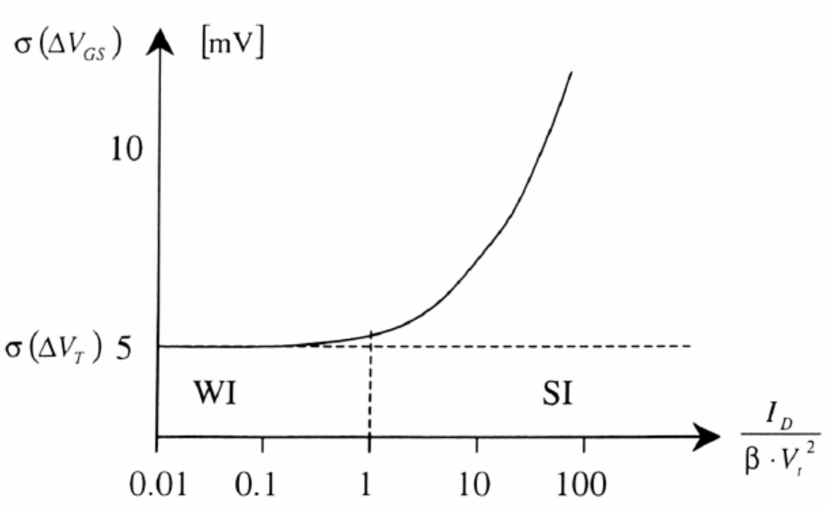
$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta\beta}{\beta} - \Delta V_T \frac{2}{V_{GS} - V_T}$$

$$\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \sigma^2(\Delta V_T)\frac{4}{(V_{GS} - V_T)^2}$$

输出电流的失配

$$\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \sigma^2(\Delta V_T)\ \underbrace{\frac{4}{(V_{GS}-V_T)^2}}_{\text{in si}}\ \text{or}\ \underbrace{\frac{1}{(nkT/q)^2}}_{\text{in wi}}$$

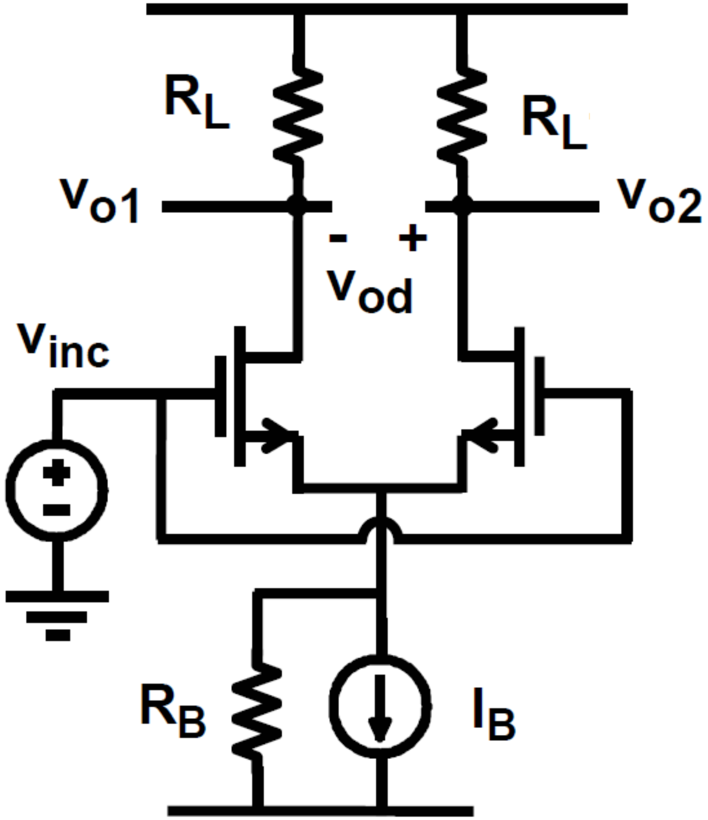




- 弱反型区中, V_T 失配占主要因素；强反型区中, β 失配占主要因素，其中主要又是W/L的失配为主

共模抑制比

- 差分对的另一随机指标：共模抑制比（Common Mode Rejection Ration）



共模增益：

差模输出V_{od} /共模输入V_{inc}

$$A_{dc} = \left.\frac{v_{od}}{v_{ic}}\right|_{v_{id}=0} \approx 0$$

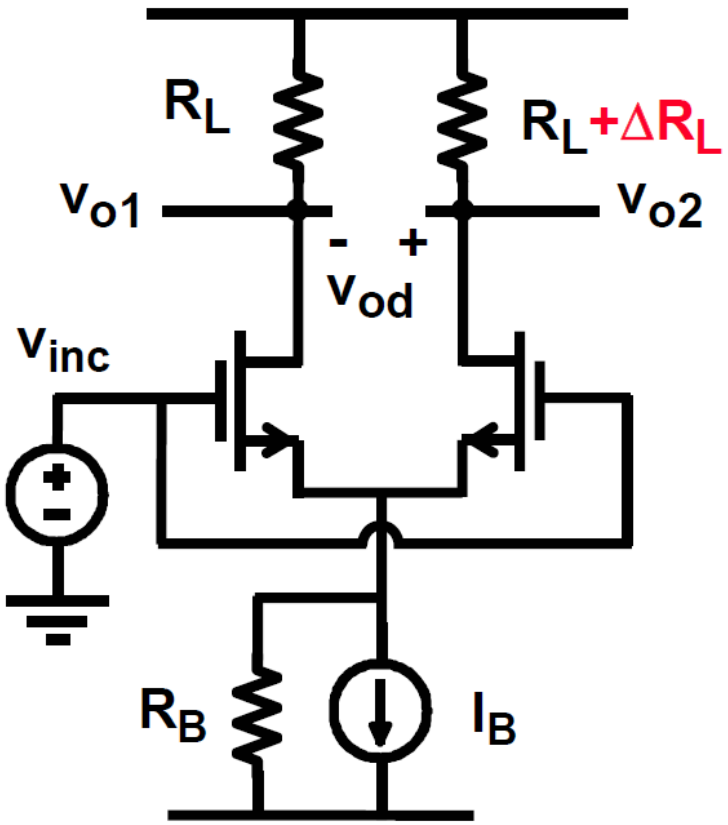
共模抑制比：

差模增益/共模增益

$$CMRR = \frac{A_{dd}}{A_{dc}} \approx \infty$$

共模抑制比

- 差分对的另一随机指标：共模抑制比（Common Mode Rejection Ration）

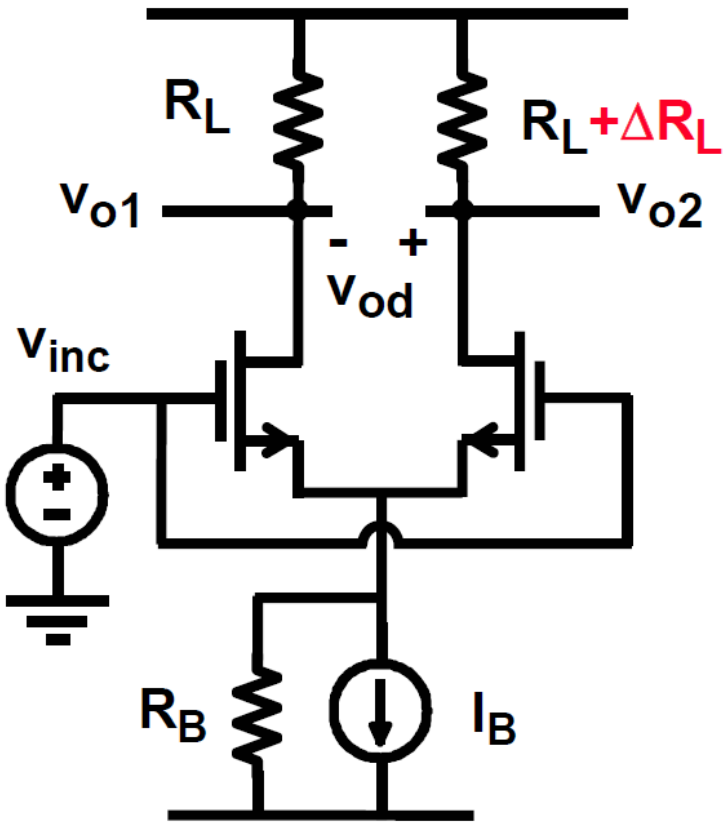


- **负载不对称**

$$A_{dc} = \left.\frac{V_{od}}{V_{ic}}\right|_{V_{id}=0} \neq 0$$

共模抑制比

- 差分对的另一随机指标：共模抑制比（Common Mode Rejection Ration）



- **负载不对称**

$$\Rightarrow \quad A_{dc} = \left.\frac{v_{od}}{v_{ic}}\right|_{v_{id}=0} \neq 0$$

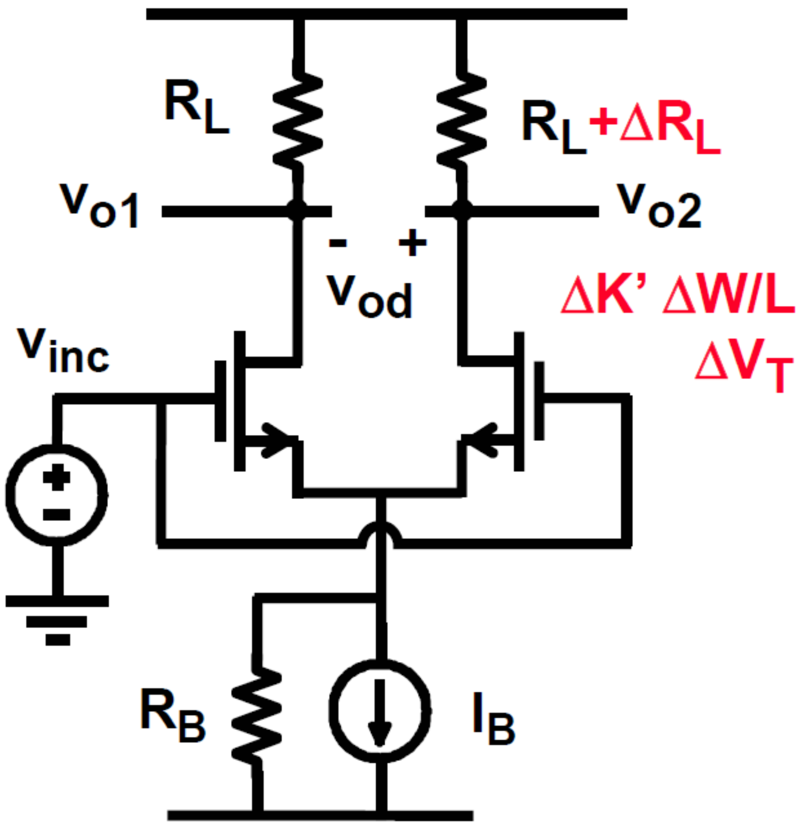
共模偏置电流： $I_B=V_{INC}/R_B$

差模输出： $V_{od}=\Delta R_L \cdot I_B/2$

$$A_{dc} = \frac{\Delta R_L}{2R_B} \qquad \boxed{CMRR = \frac{2g_m R_B}{\Delta R_L/R_L}}$$

共模抑制比

- 差分对的另一随机指标：共模抑制比（Common Mode Rejection Ration）



- **负载不对称**
- **差分对失调**

$$CMRR = \frac{2g_m R_B}{\frac{\Delta R_L}{R_L}}$$

$$CMRR = \frac{2g_m R_B}{\frac{\Delta R_L}{R_L} + \frac{2V_{OS}}{V_{GS}-V_T}}$$

随机失调与CMRR的关系

$$CMRR = \frac{2g_m R_B}{\frac{\Delta R_L}{R_L} + \frac{2V_{OS}}{V_{GS} - V_T}}$$

$$\Rightarrow \quad V_{OS} \cdot CMRR = V_{OS} \cdot \frac{2g_m R_B}{\frac{\Delta R_L}{R_L} + \frac{2V_{OS}}{V_{GS} - V_T}}$$

$$\Rightarrow \quad V_{OS} \cdot CMRR \approx (V_{GS} - V_T) g_m R_B$$

$$\Rightarrow \quad V_{OS} \cdot CMRR \approx V_E L_B$$

减小失调就是提高CMRR

随机失调与CMRR的关系

$v_{OSr}\, CMRR_r \approx V_E L_B \approx 10\ V \quad (\sim L_B)$

10 mV 60 dB ≈ 10 V as for MOSTs

1 mV 80 dB ≈ 10 V as for Bipolar transistors

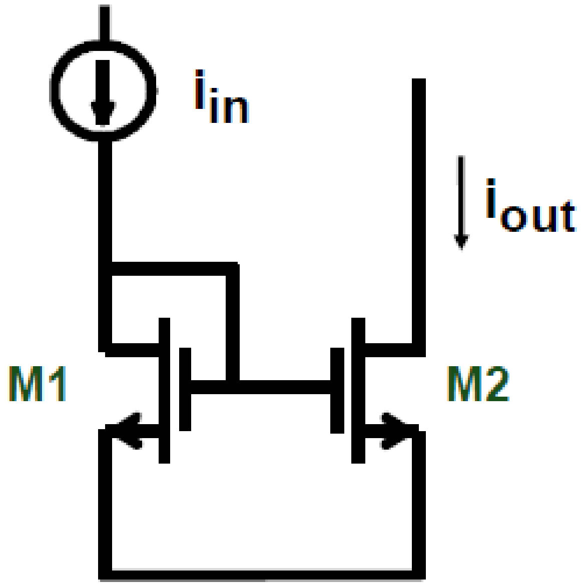
10 μV 120 dB ≈ 10 V with trimming : with laser
with Zener zap
with fusible links

Low offset = High CMRR

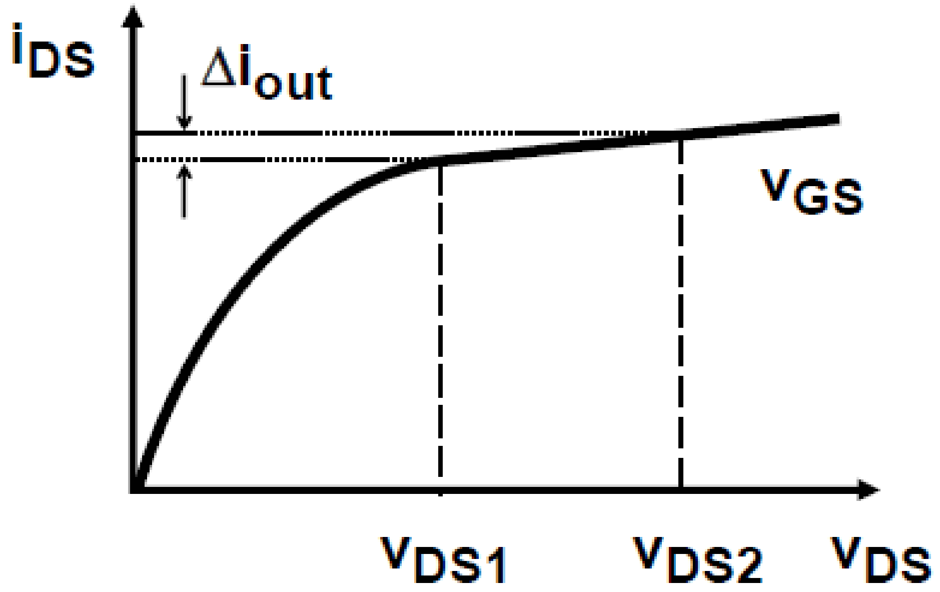
失调与CMRR

- 随机性失调和$CMRR_R$
- **系统性失调和$CMRR_S$**
- 设计守则

电流镜中的系统失调



$\cancel{\Delta K' \ \Delta W/L \ \Delta V_T}$

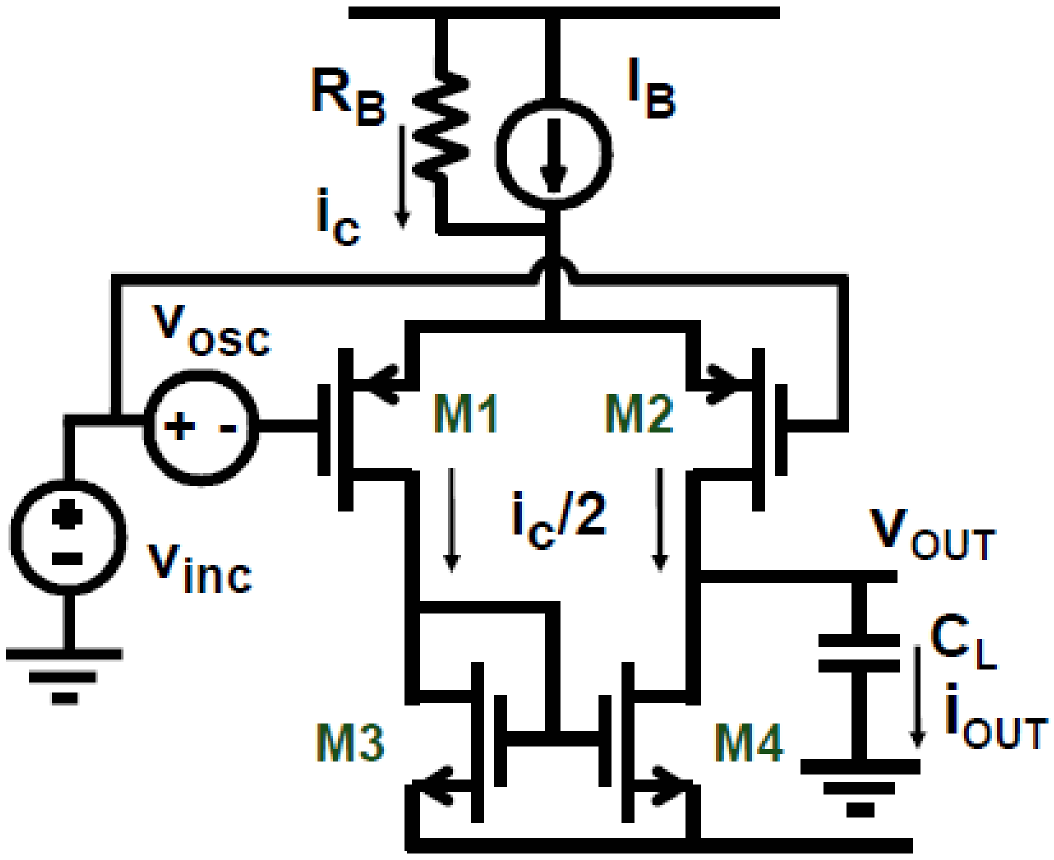


$$I_{out} \overset{?}{=} I_{in}$$

$$\frac{\Delta i_{out}}{i_{out}} = \frac{v_{DS2} - v_{DS1}}{V_E L_2}$$

差分运放中的系统性CMRR

- **不考虑任何随机性失调的情况下：**



$$V_{OUT} = V_{GS3}$$

$$\Delta V_{GS3} = \frac{1}{2}\Delta I_B / g_{m3}$$

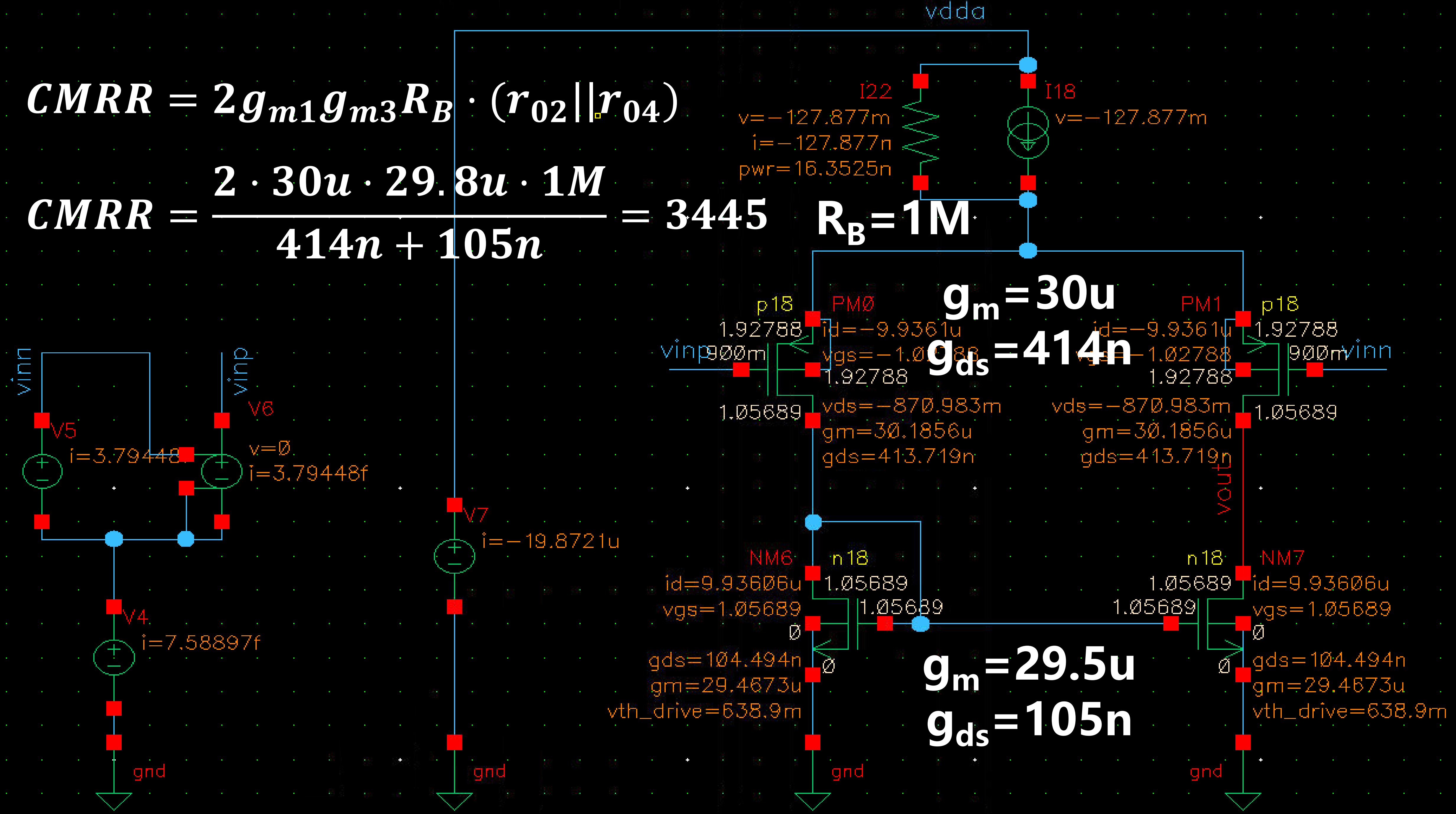
$$A_{dc} = \frac{1}{2g_{m3}R_B}$$

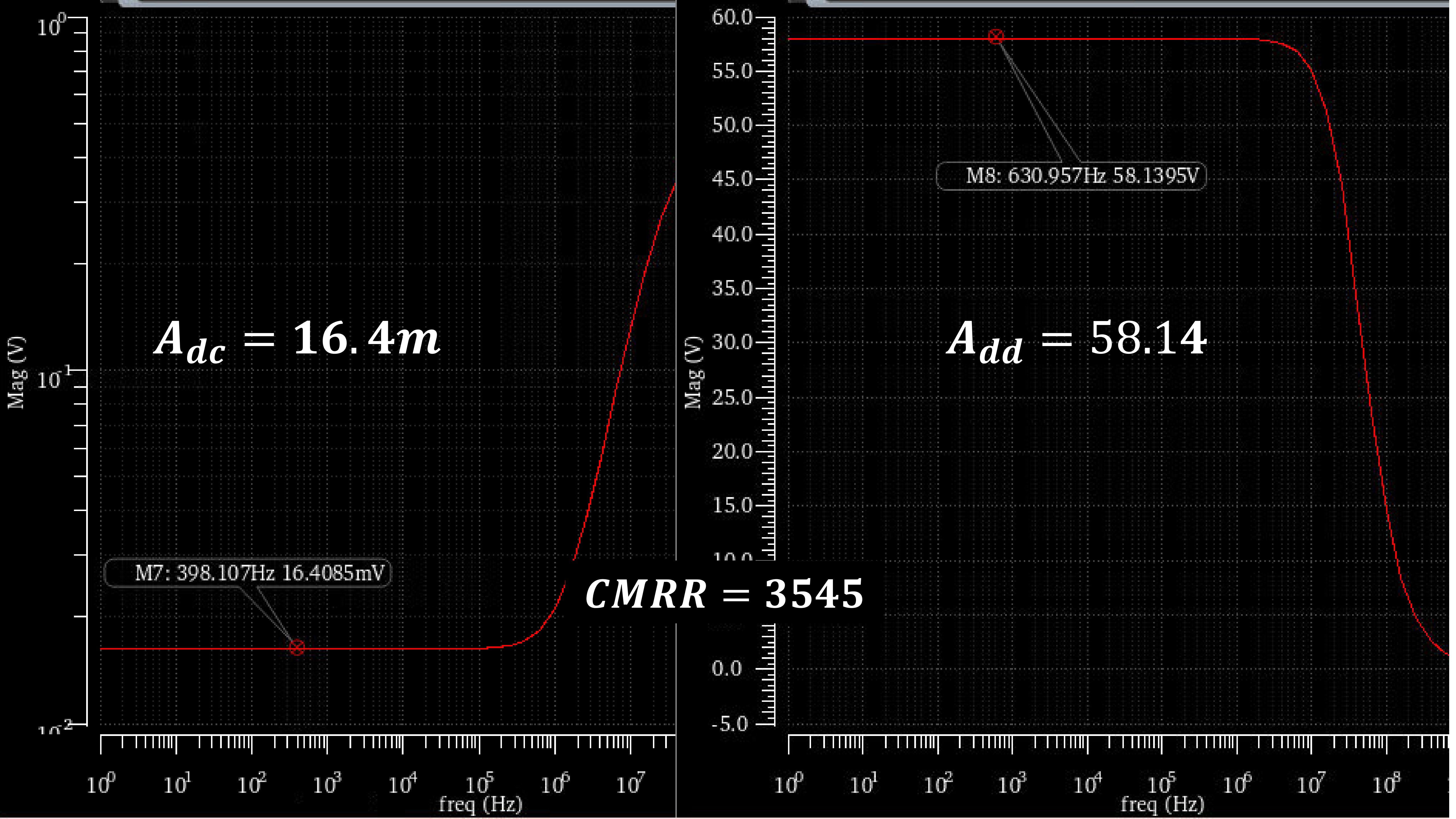
$$A_{dd} = g_{m1}\cdot(r_{02}||r_{04})$$

$$CMRR = 2g_{m1}g_{m3}R_B\cdot(r_{02}||r_{04})$$

$$CMRR = 2g_{m1}g_{m3}R_B \cdot (r_{02}||r_{04})$$

$$CMRR = \frac{2 \cdot 30u \cdot 29.8u \cdot 1M}{414n + 105n} = 3445$$

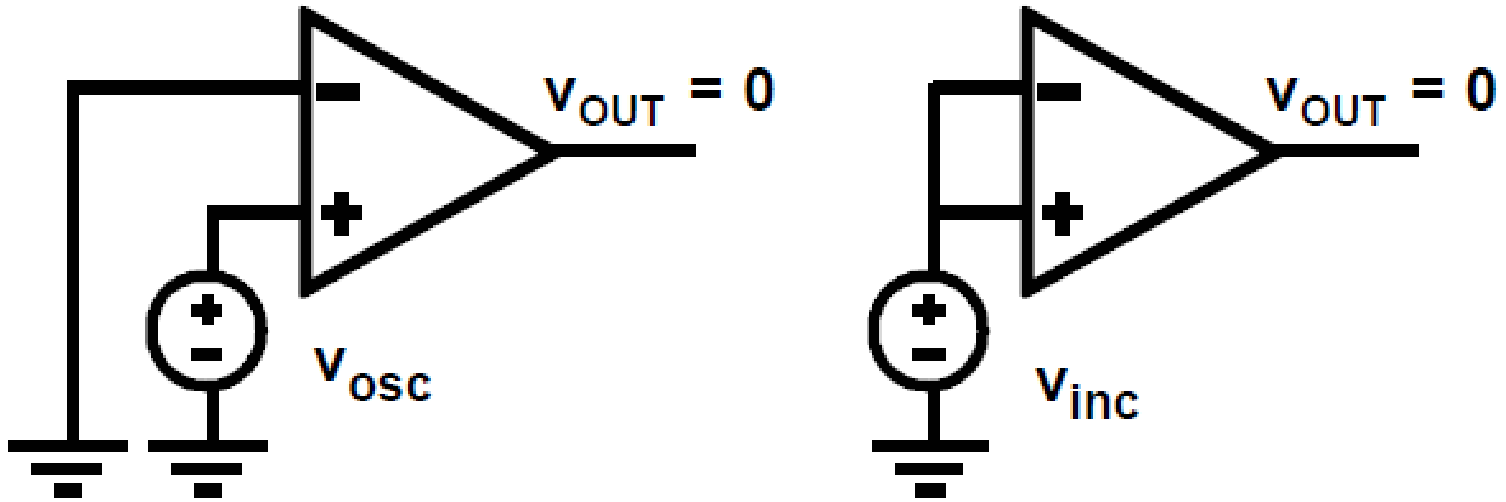




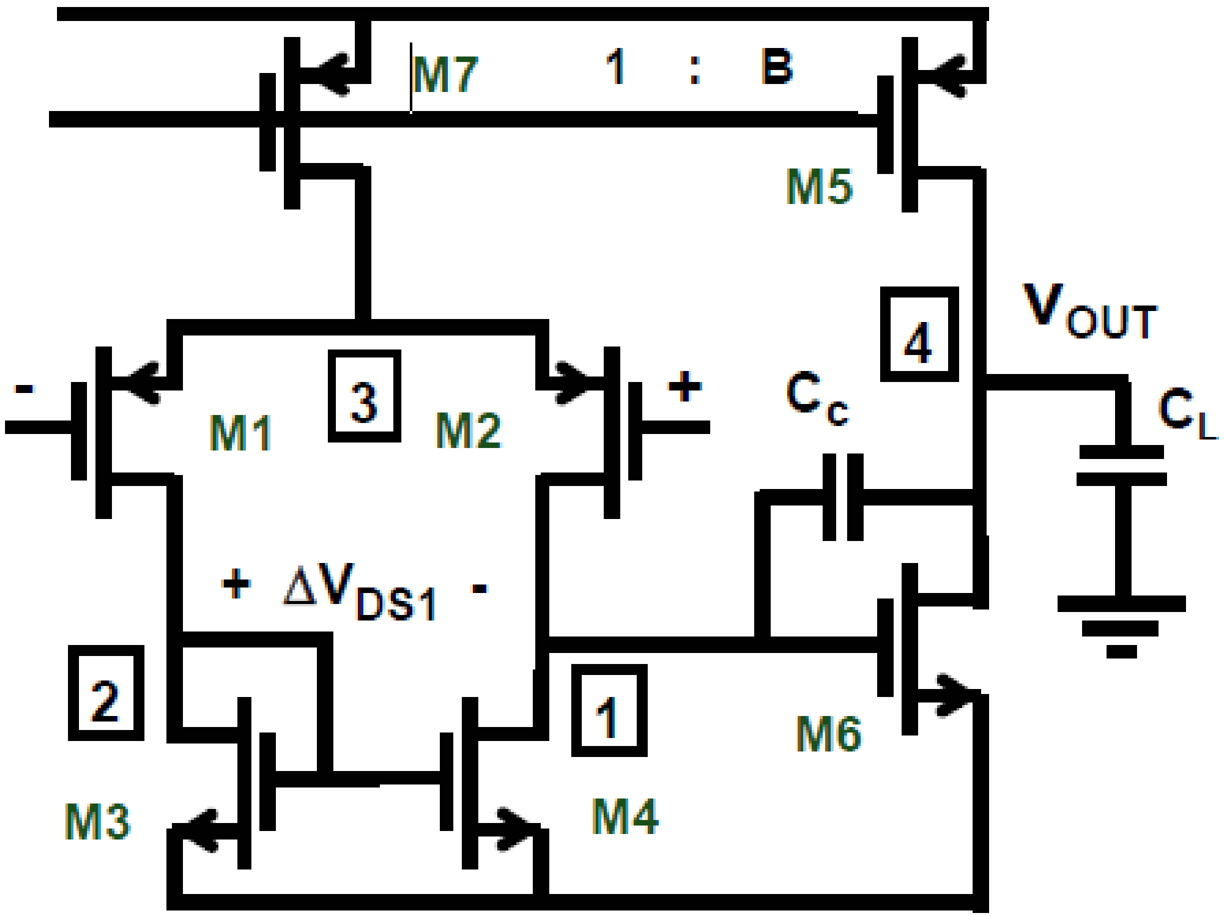
M7: 398.107Hz 16.4085mV
$A_{dc} = 16.4m$
Mag (V)
freq (Hz)
M8: 630.957Hz 58.1395V
$A_{dd} = 58.14$
Mag (V)
freq (Hz)
$CMRR = 3545$

差分运放中的总CMRR

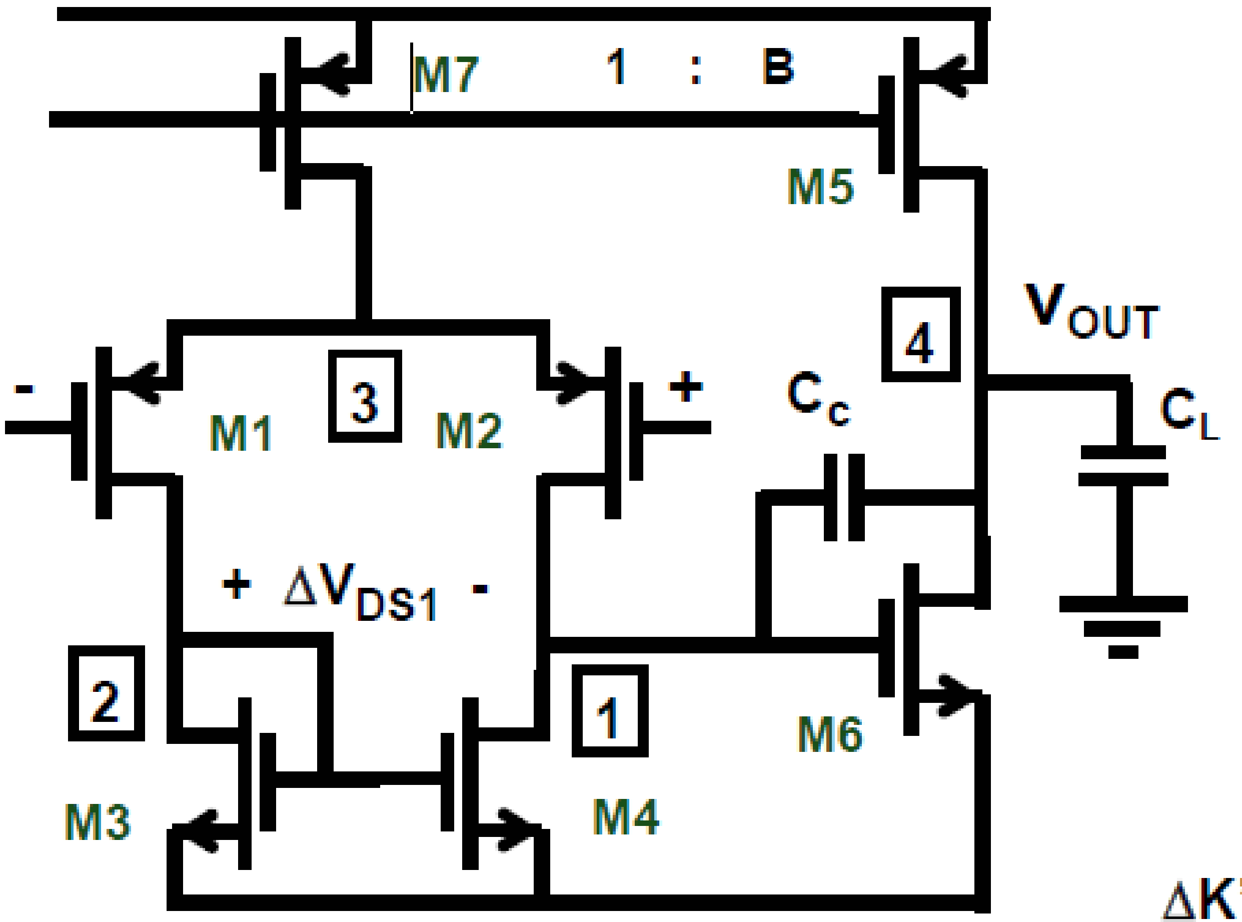
$$\frac{1}{CMRR} = \frac{1}{CMRR_r} + \frac{1}{CMRR_s}$$



两级运放中的失调现象



两级运放中的失调现象

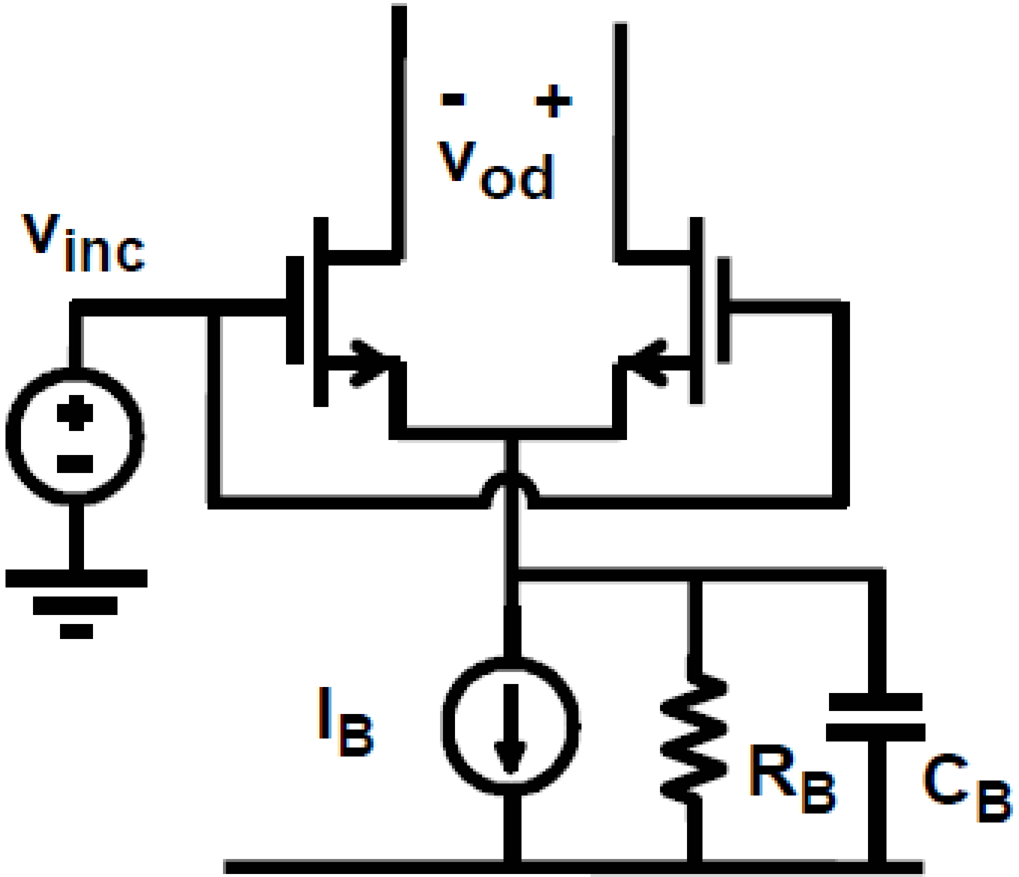


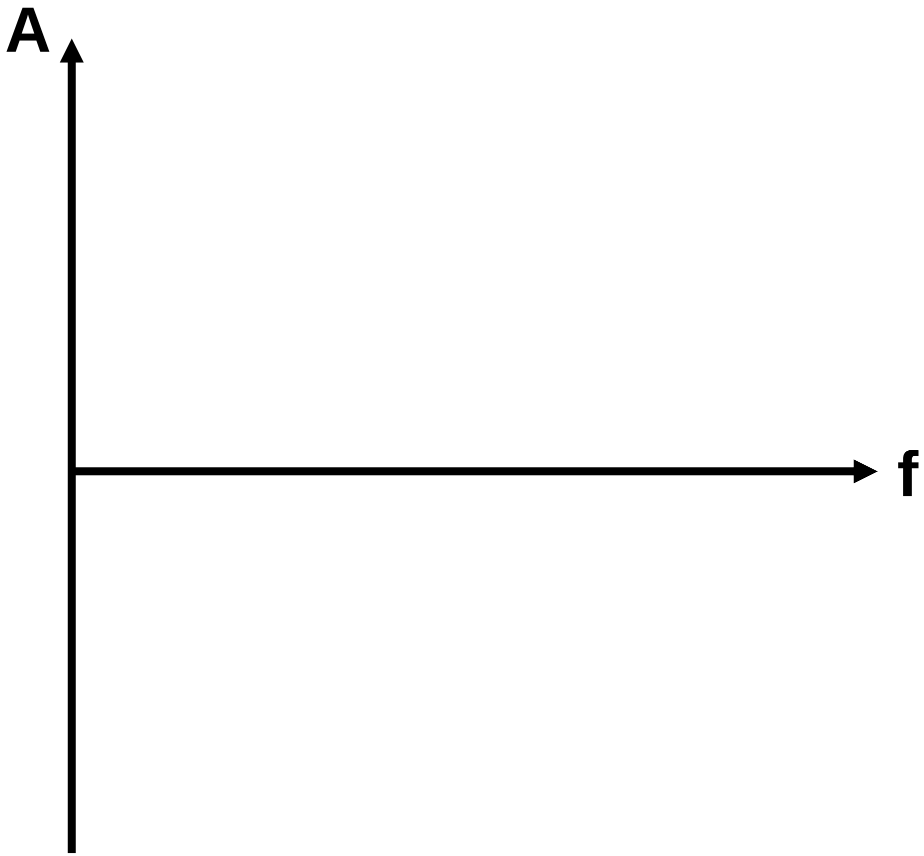
$$A_{v1} = g_{m1}\, r_{02} // r_{04}$$

$$v_{OS} = \frac{\Delta V_{DS1}}{A_{v1}} + \Delta V_{T1} + \frac{g_{m3}}{g_{m1}} \Delta V_{T3}^{*} + \frac{V_{GS1} - V_T}{2} S$$

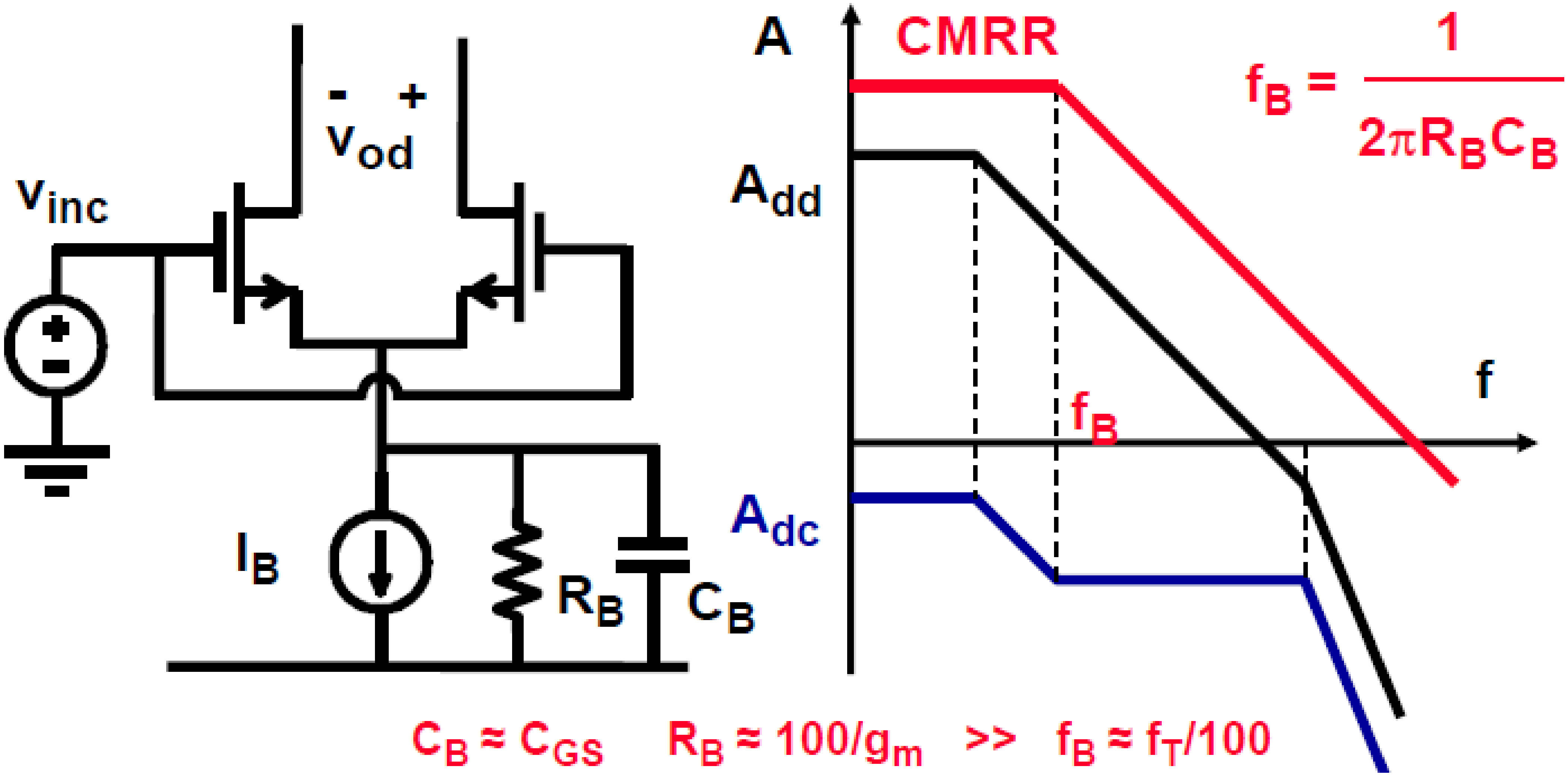
$$S = \frac{\Delta K'_n}{K'_n} + \frac{\Delta K'_p}{K'_p} + \frac{\Delta W/L_1}{W/L_1} + \frac{\Delta W/L_3}{W/L_3}$$

CMRR的频率特性





CMRR的频率特性



$C_B \approx C_{GS}$ $R_B \approx 100/g_m$ >> $f_B \approx f_T/100$

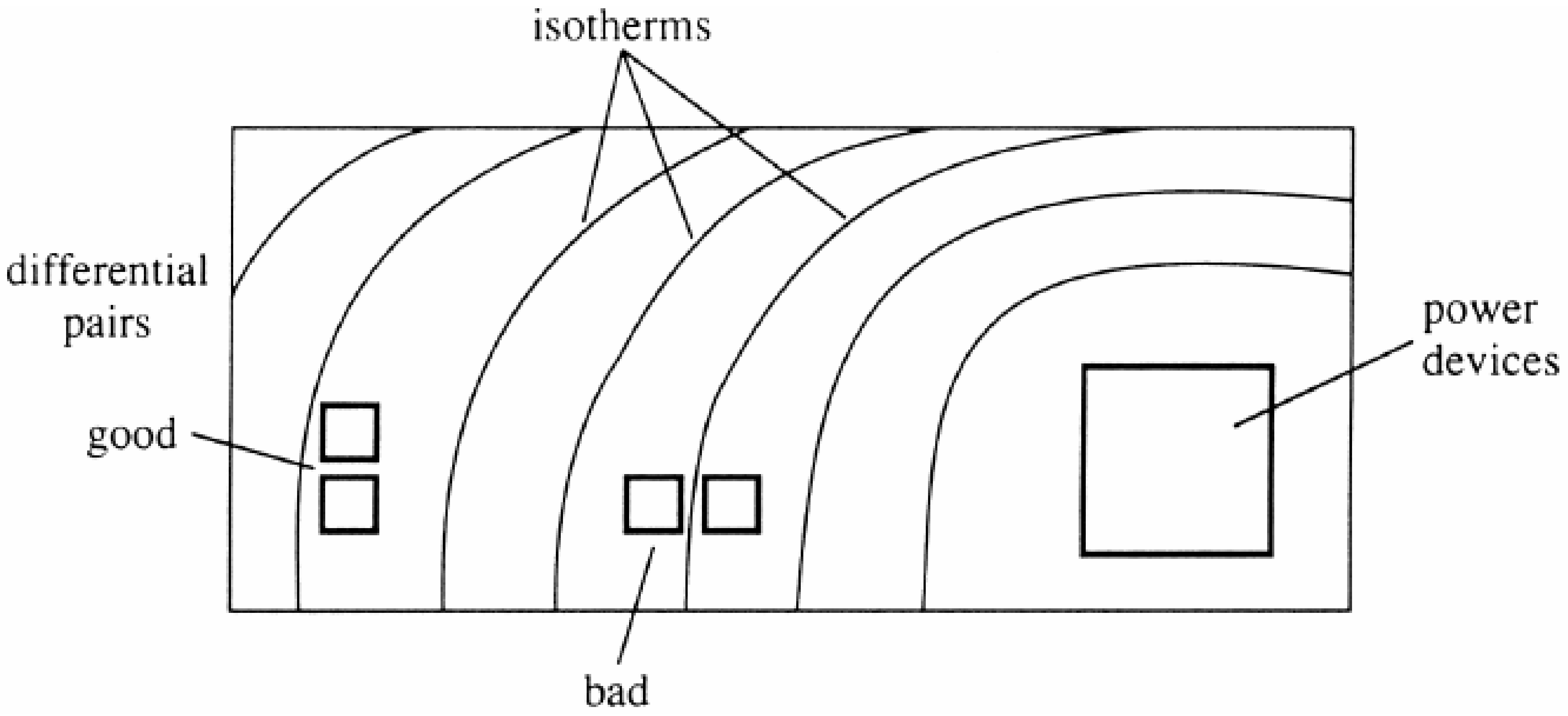
失调与CMRR

- 随机性失调和$CMRR_R$
- 系统性失调和$CMRR_S$
- **设计守则**

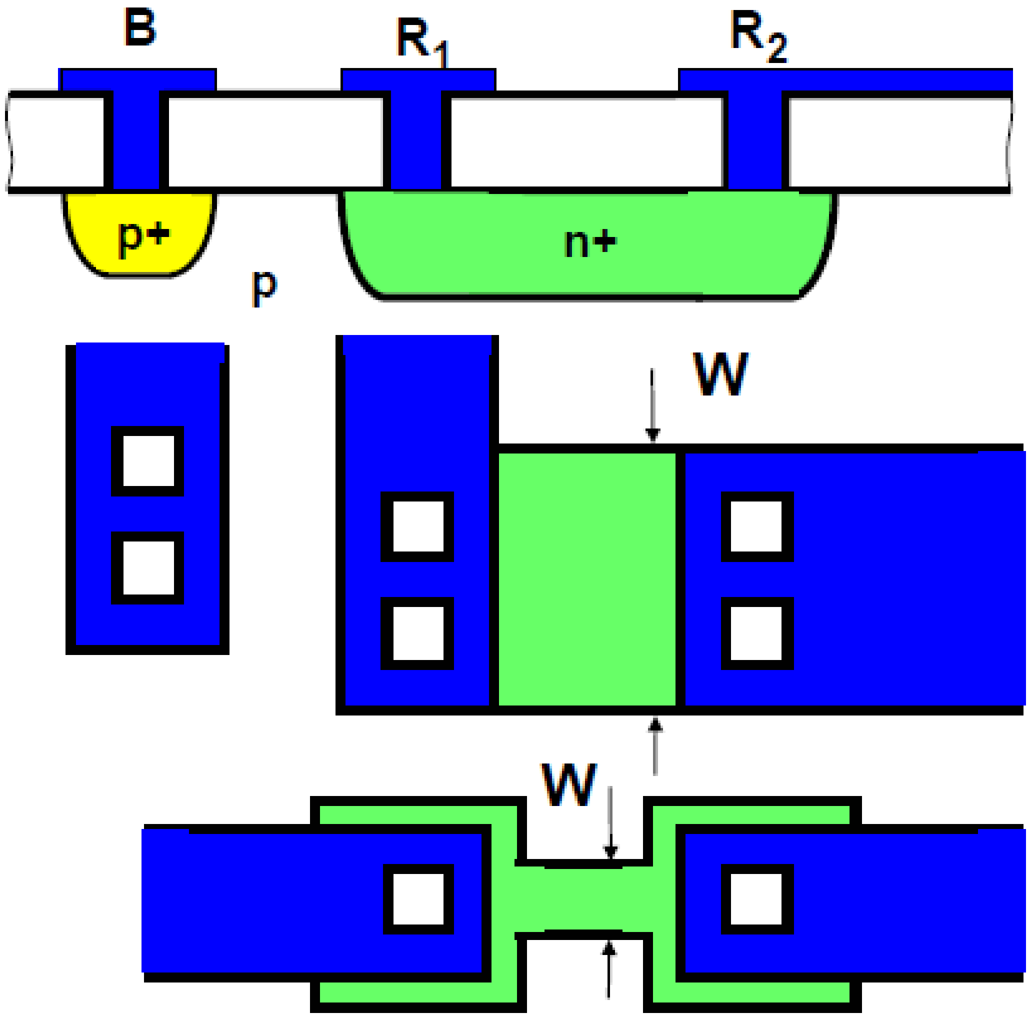
设计守则

- 相同的特性
- 相同的温度
- 增大尺寸
- 减小间距
- 同样的方向
- 同样的长宽比
- 中心对称
- Dummy

相同的温度



电阻的版图



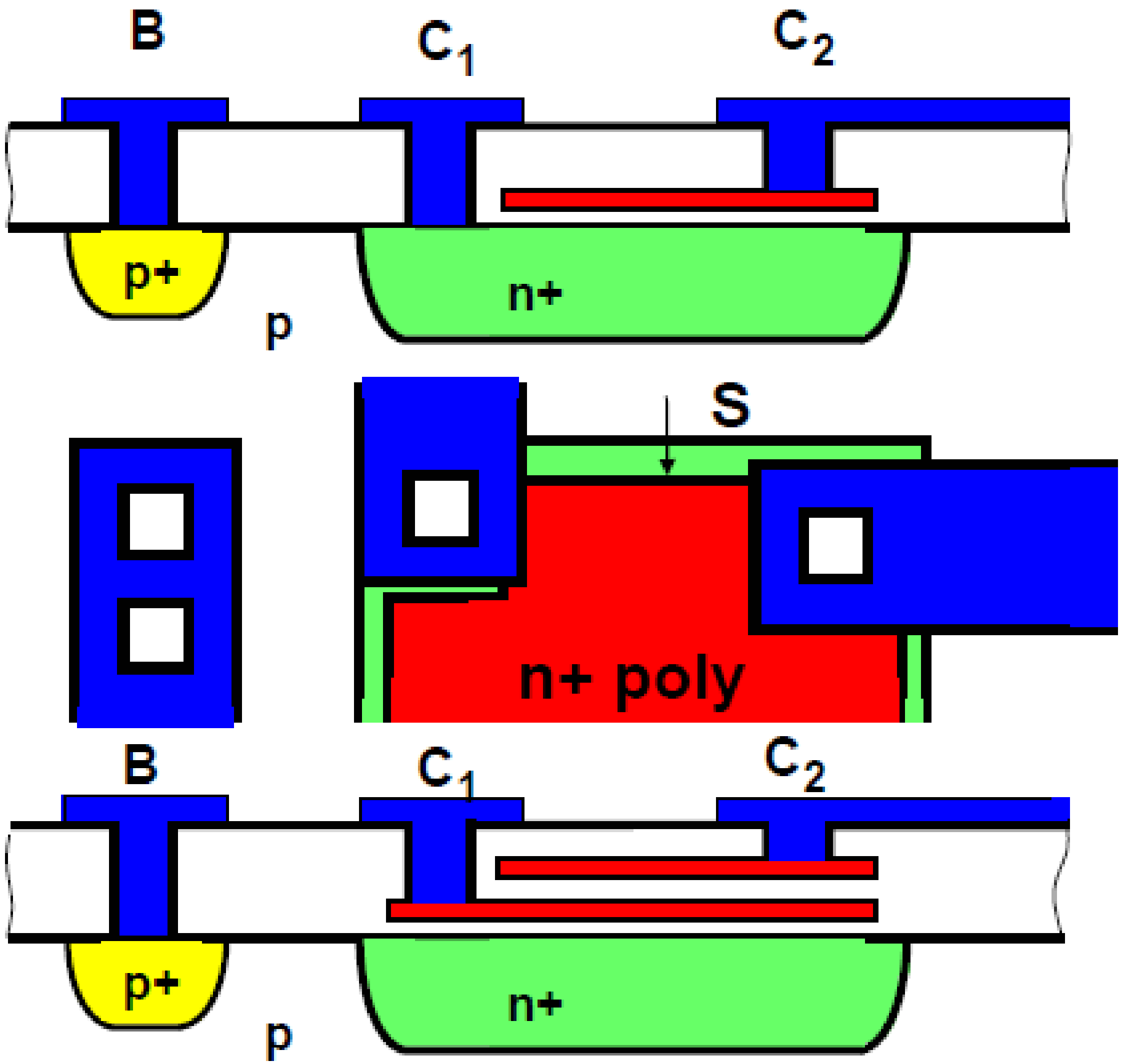
Source/drain diffusion resistor in CMOS

Ref.: Laker, Sansen : Design of analog …, MacGrawHill 1994 Table 2-6

电阻的实现方式及对比

Process	Type	ρ□ Ω/□	absolute accuracy percent	temperature coefficient percent/°C	voltage coefficient percent/V	breakdown voltage V
CMOS	S/D diffusion	20-50	20	0.2	0.5	20
	well	2.5k	10	0.3	1	20
	poly gate	50	20	0.2	0.05	40
	poly resistance	1.5k	**1**	0.05	0.02	20
	aluminum	50m	20	0.01	0.02	90

电容的版图



Poly to S/D capacitor

Poly to poly capacitor

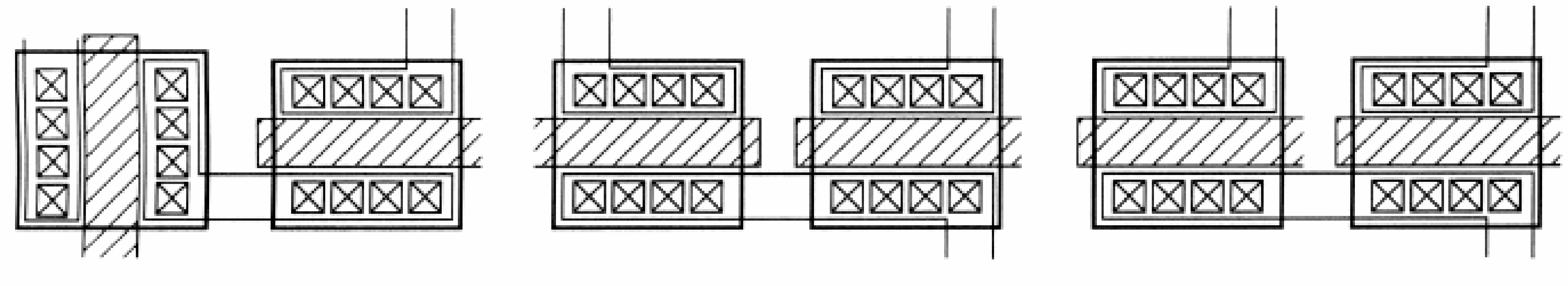
$$C_{par} \approx \frac{1}{6 \ldots 15} C_{pp}$$

电容的实现方式及对比

Process	Type	C Nf/cm^2	absolute accuracy percent	temperature coefficient percent/^{o}C	voltage coefficient percent/V	breakdown voltage V
CMOS	C_{ox}(50nm)	70	5	0.002	0.005	40
	$C_{m,poly}$	12	10	0.002	0.005	40
	$C_{poly,poly}$	56	**2**	0.002	0.005	40
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20
	$C_{m,substrate}$	5.2	10	0.01	0.05	20
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20

Ref.:Laker,Sanse:
Design of analog…,
MacGrawHill 1994
Table 2-7

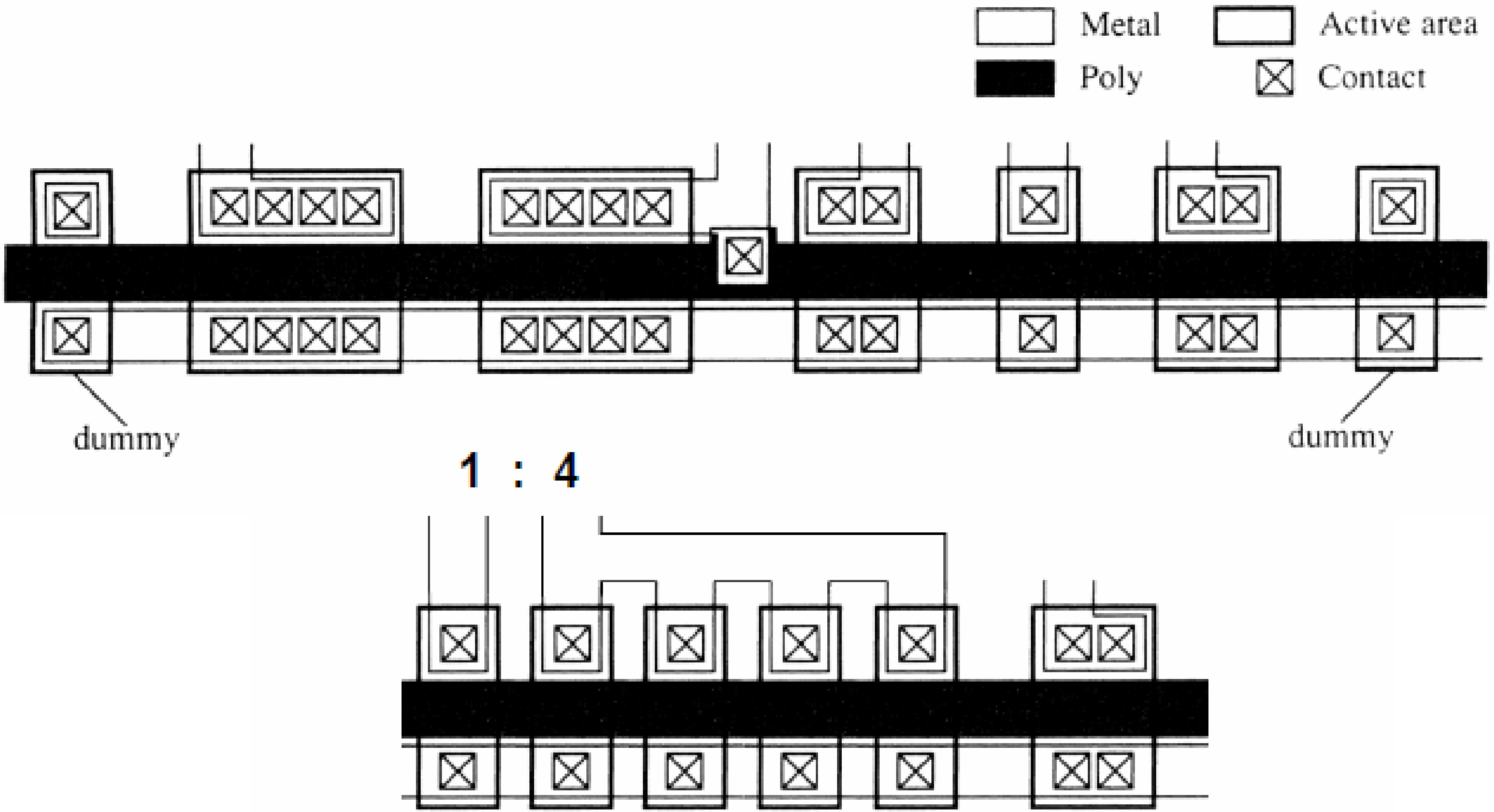
差分对的匹配



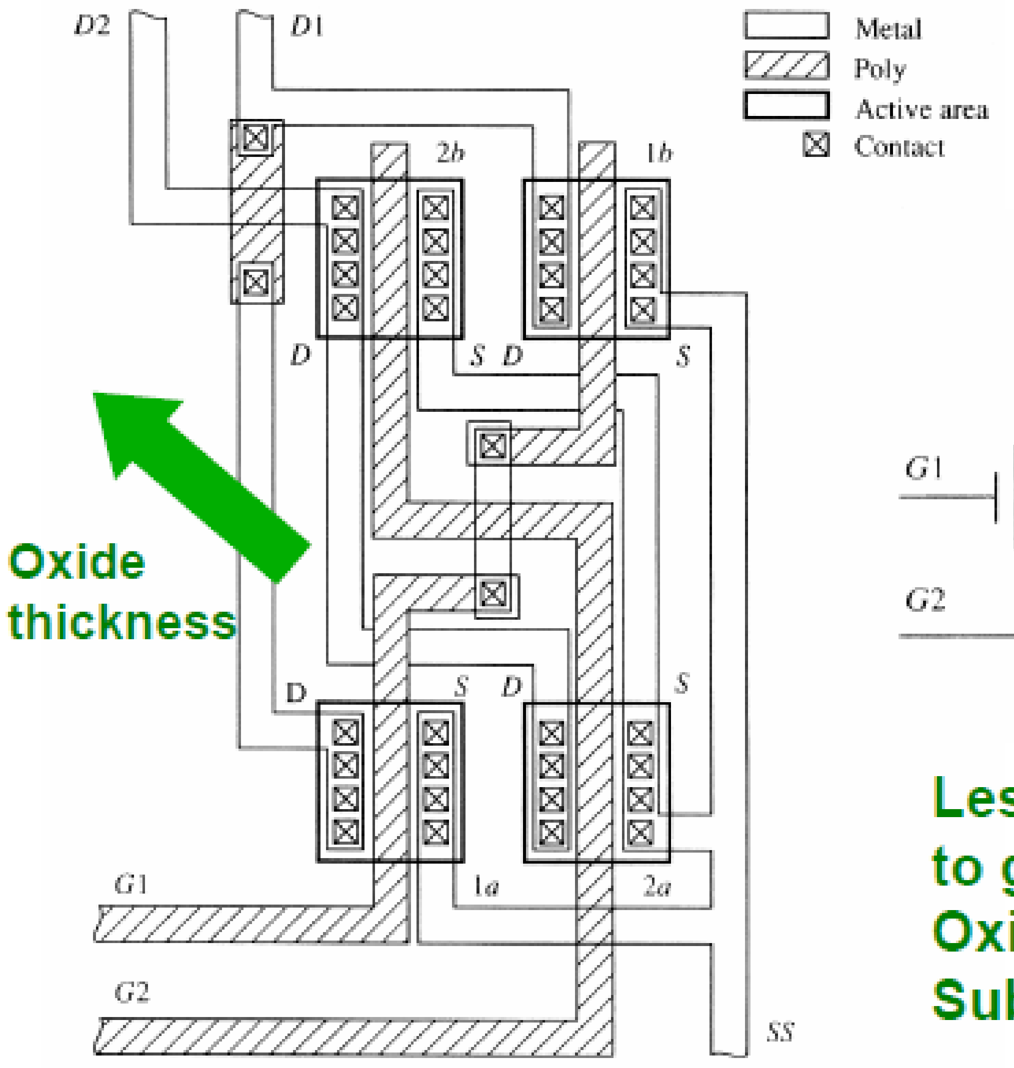
Bad　　　　Better　　　　Better

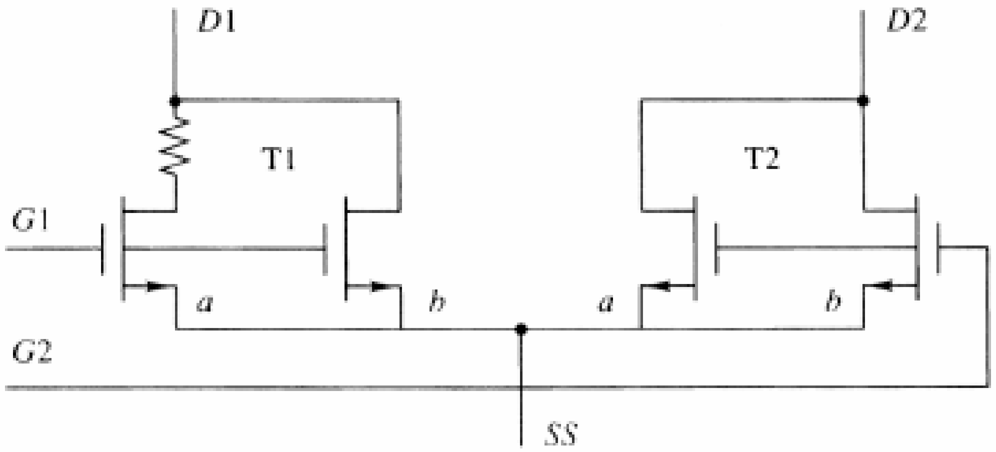
同样的长宽比

Current mirror 4:4:2:1:2 with end dummies.



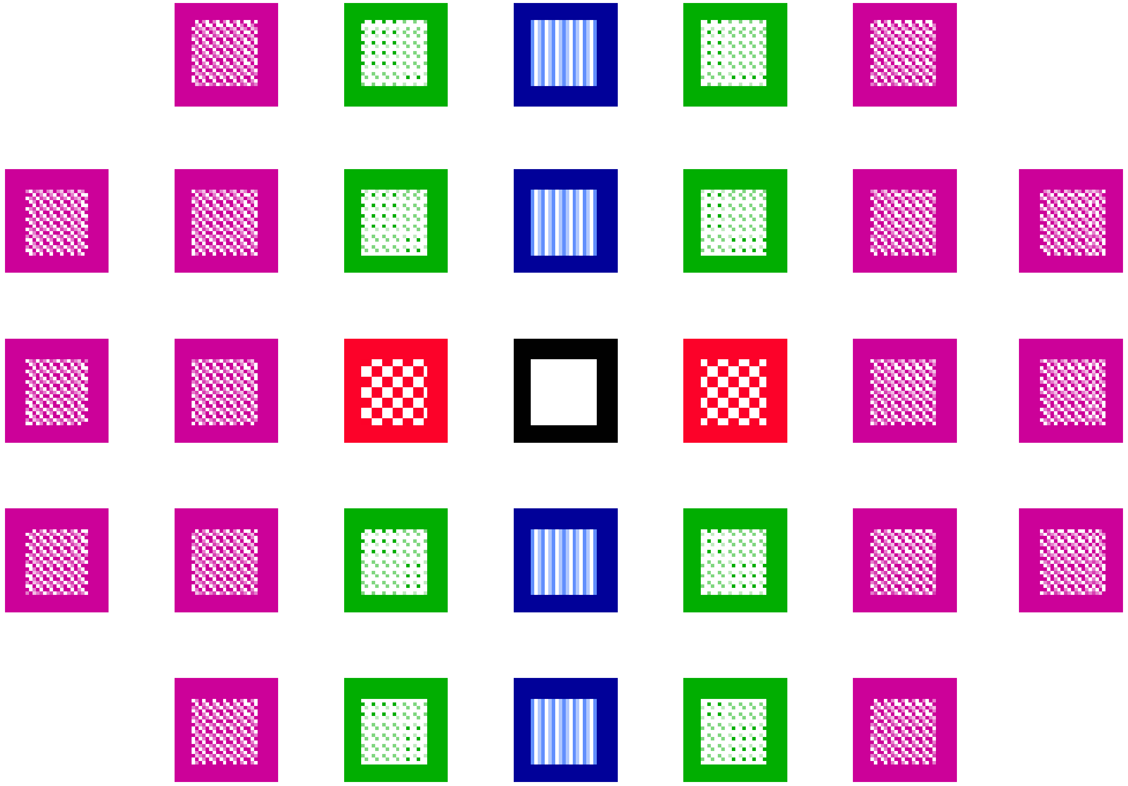
中心对称的版图





Less sensitive
to global variations :
Oxide thickness
Substrate doping level
....

中心对称的版图



Ratio:

1

2

4

8

16

设计思路总结

1. 与噪声的设计一样，差分对需要V_{GST}尽量小，而电流镜则需要V_{GST}尽量大
2. 失调的优化与CMRR的优化相同，超高的CMRR往往需要后期的Calibration.
3. 在版图中选择合适的被动器件，以及优秀的版图技巧都能改善失调的现象。

课后作业

- 对一偏置电流为100uA的五管OTA，共模电压为0.9V，设计晶体管的尺寸，
  1. 使其在单位增益负反馈时系统性失调小于**0.1mV**；
  2. 使其随机性失调的标准差（std）小于**1mV**；
  3. 使其共模抑制比大于 **50dB**。