Low-power Sigma-Delta AD Converters

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Ref. Norsworthy, Delta-Sigma Converters, Wiley 1996
Ref. Op ‘t Eynde, Peluso, Geerts, Marquez, Geerts, Yao, Kluwer/Springer

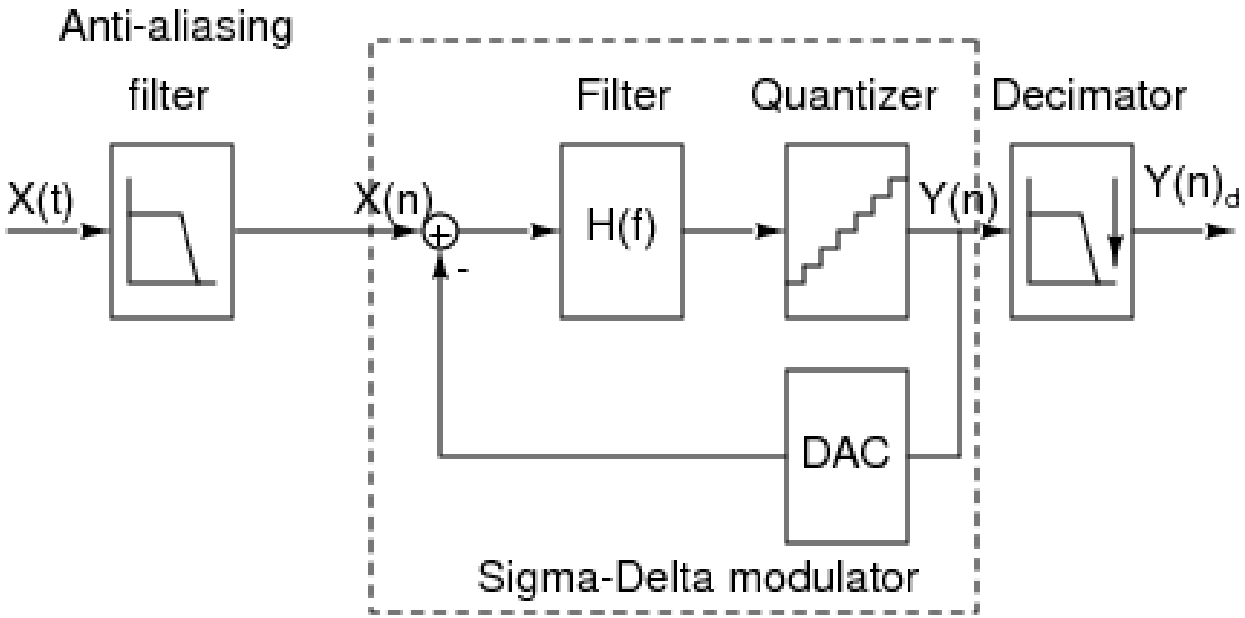
Sigma-Delta ADC

Sigma-Delta ADC exchanges resolution with speed

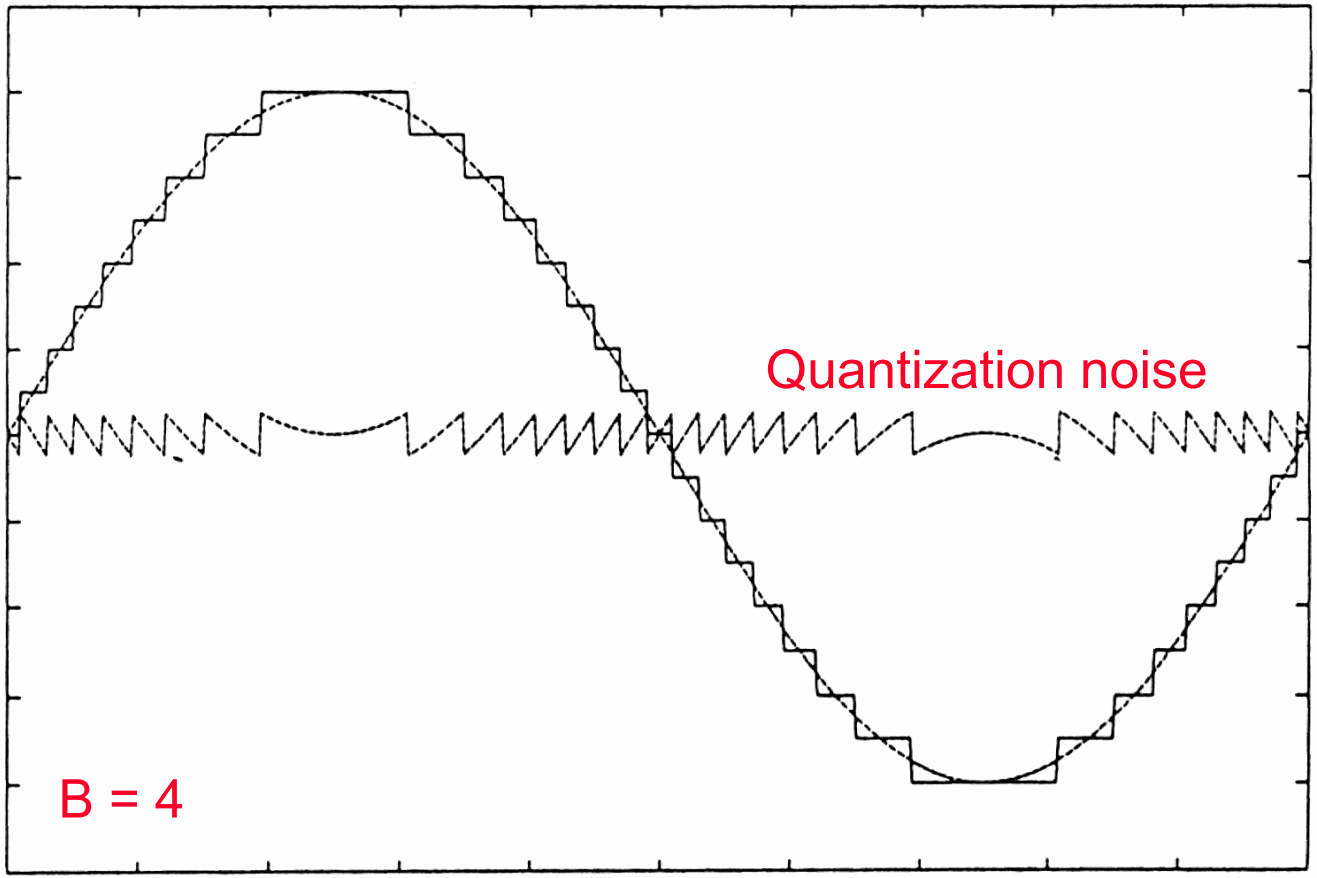
by means of :

Oversampling

Noise shaping



Quantization noise (4 bit)



Number bits ↑

Quant. noise ↓

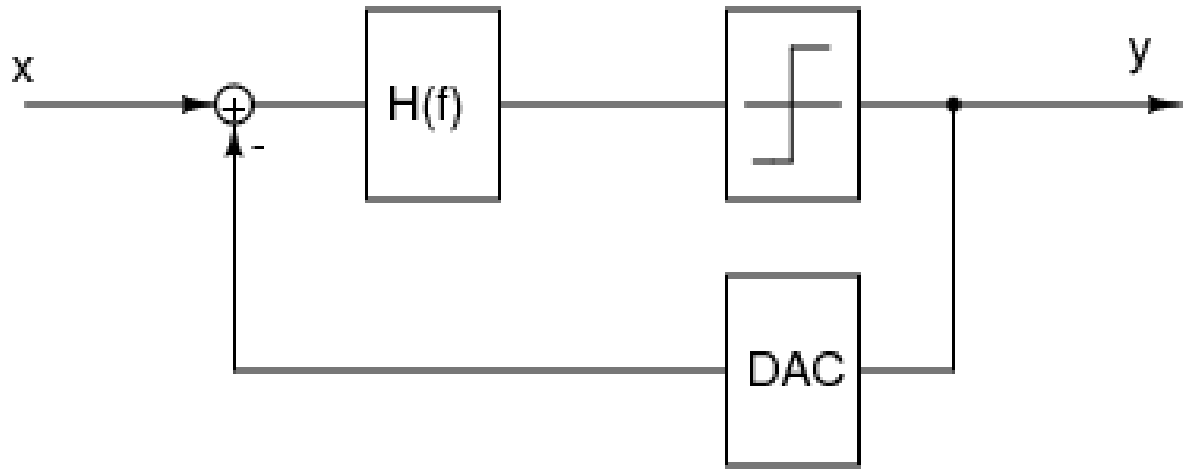
Step = $\frac{V_{ref}}{2^B}$

B = 8 bits
SNR = 50 dB

B =16 bits
SNR = 98 dB

SNR ≈ 2 + 6B

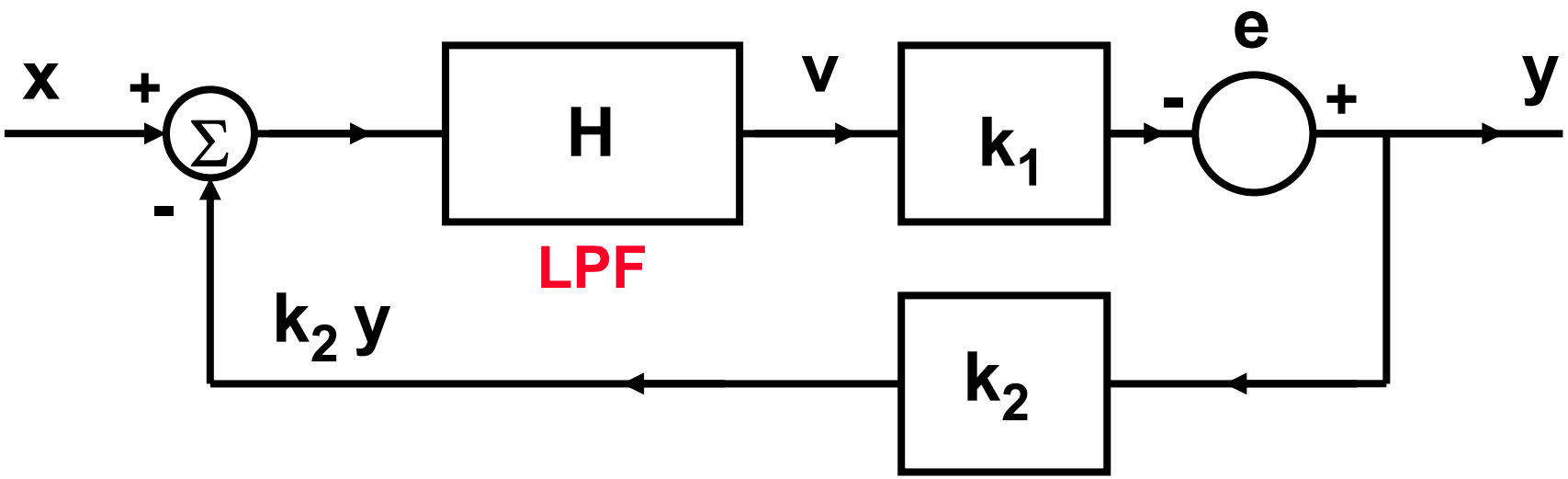
Sigma-Delta modulator



Signal transfer function: $$H_x(z) = \frac{H(z)}{1+H(z)}$$

Noise transfer function: $$H_e(z) = \frac{1}{1+H(z)}$$

Noise filtering



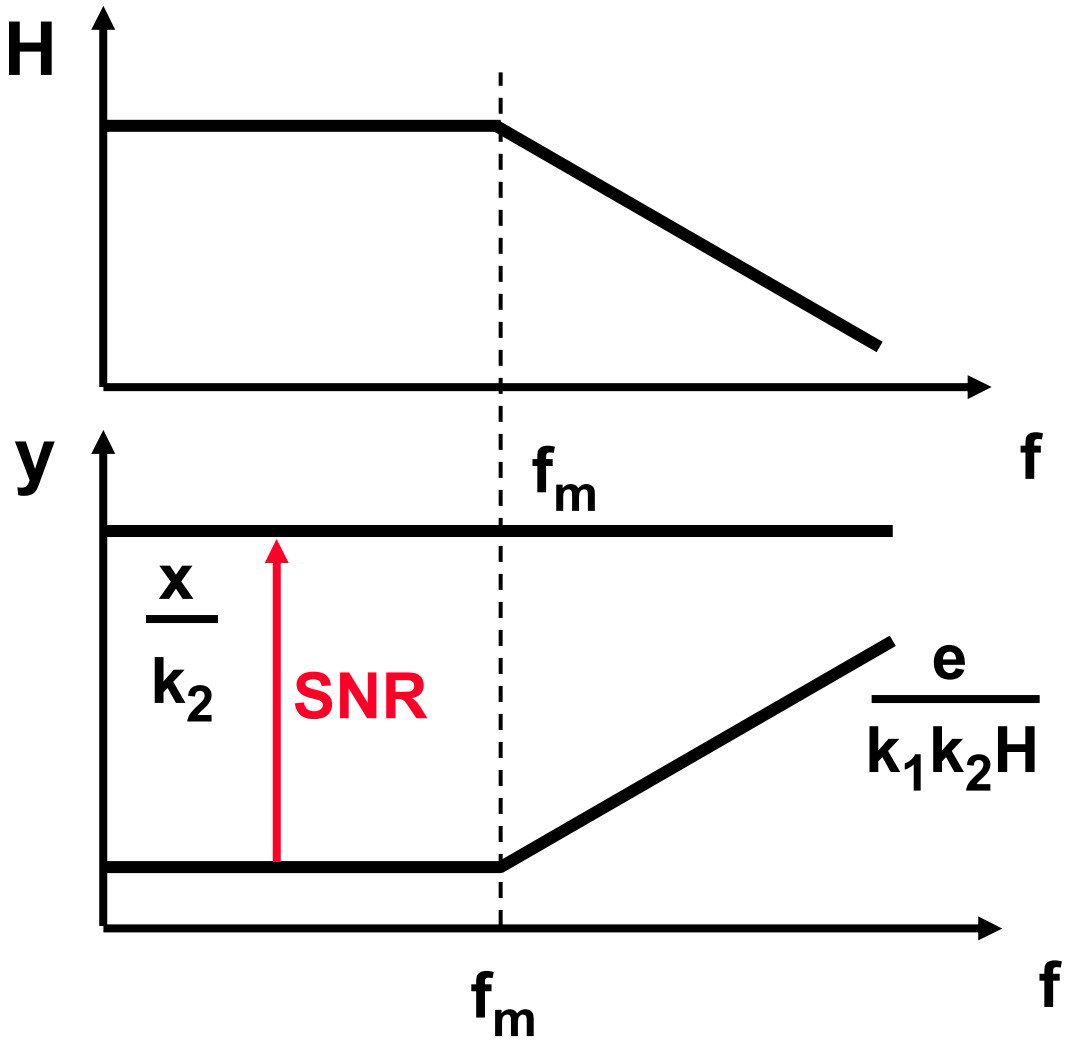
$$v = H\,(x - k_2\,y)$$

$$y = k_1\,v + e$$

Noise shaping

$$y = \frac{k_1 H}{1 + k_1 k_2 H}\,x + \frac{1}{1 + k_1 k_2 H}\,e \approx \frac{1}{k_2}\,x + \frac{1}{k_1 k_2 H}\,e$$

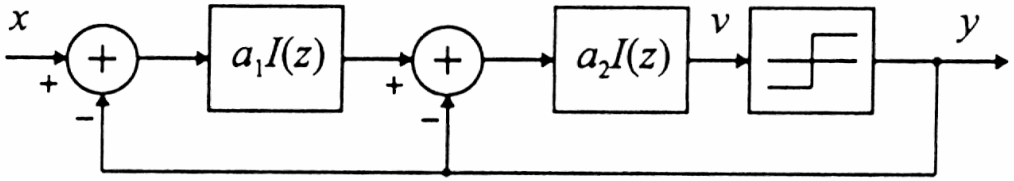
Feedback loop with low-pass filter



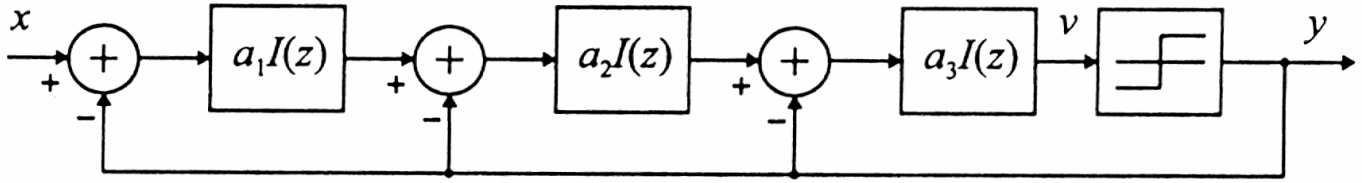
$$y \approx \frac{1}{k_2} x + \frac{1}{k_1 k_2 H} e$$

Noise shaping

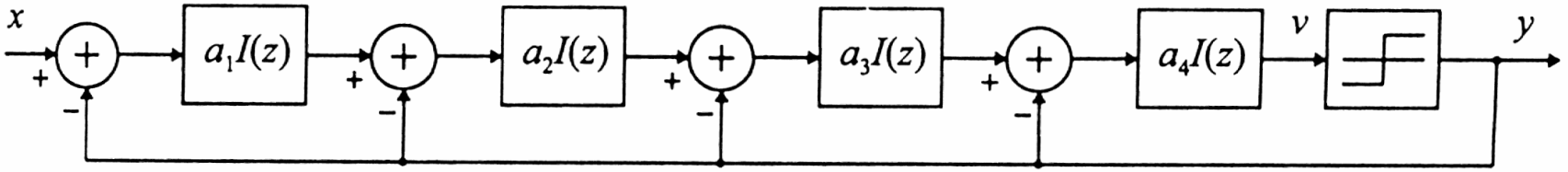
Higher-order Sigma-delta converters



(a) Second order structure

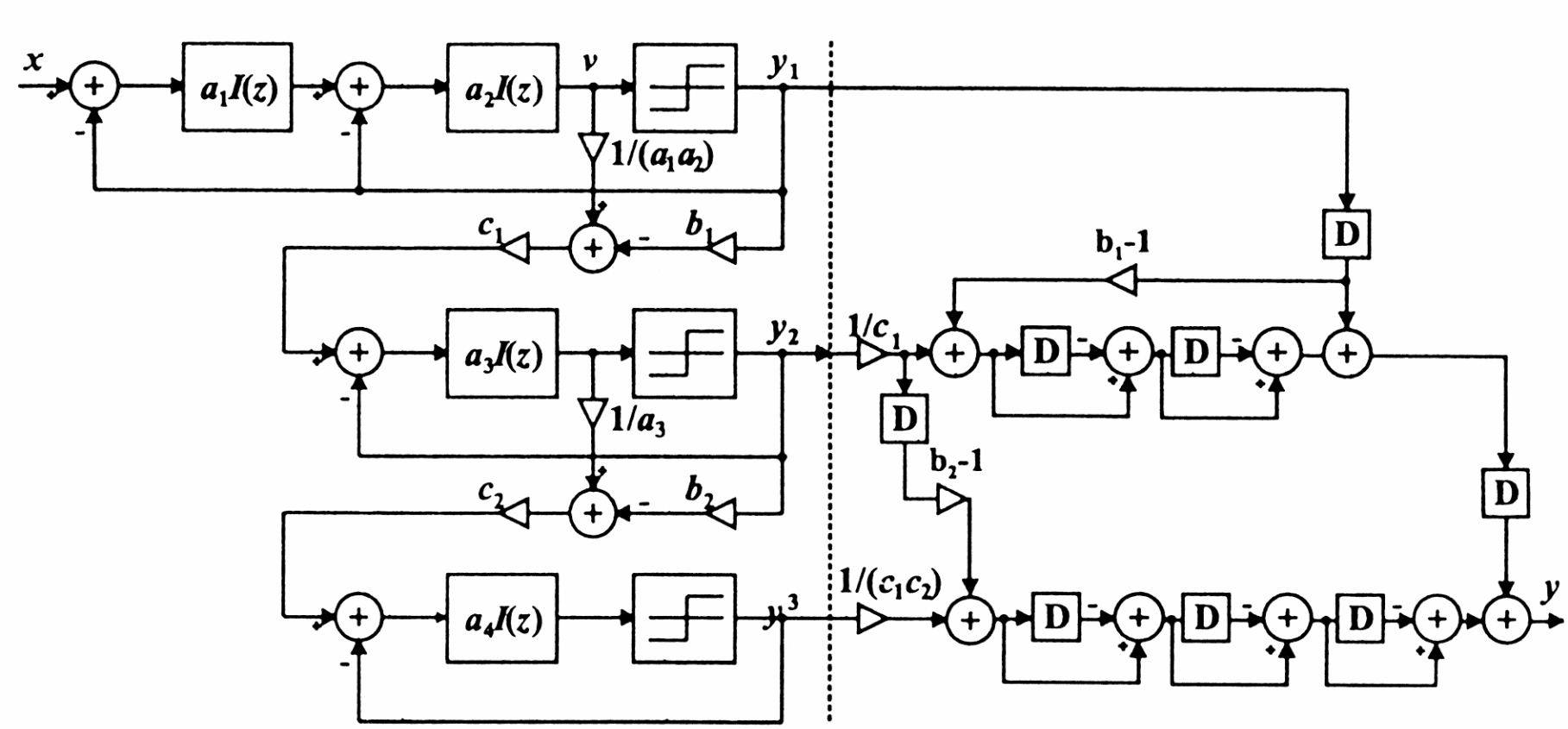


(b) Third order structure

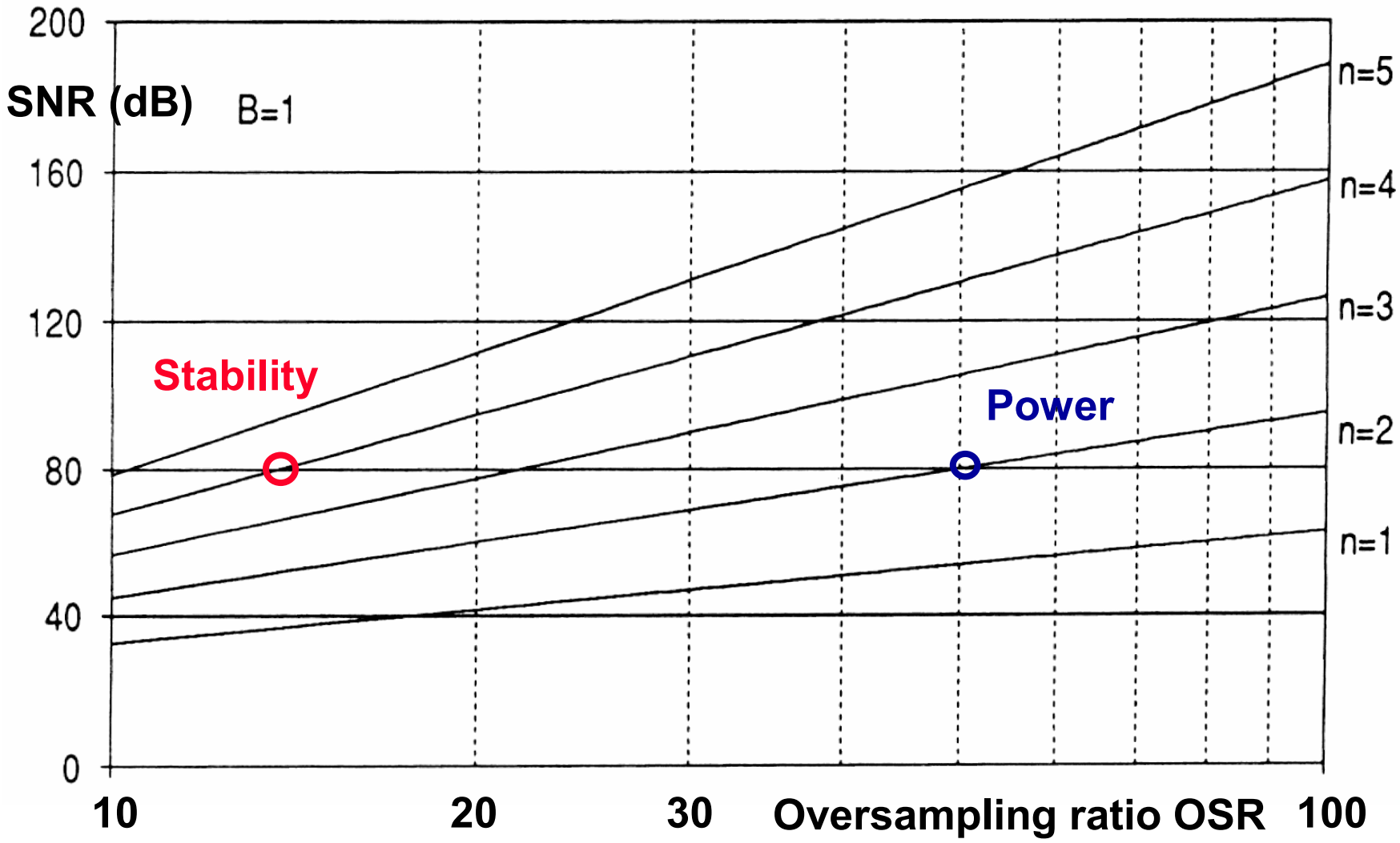


(c) Fourth order structure

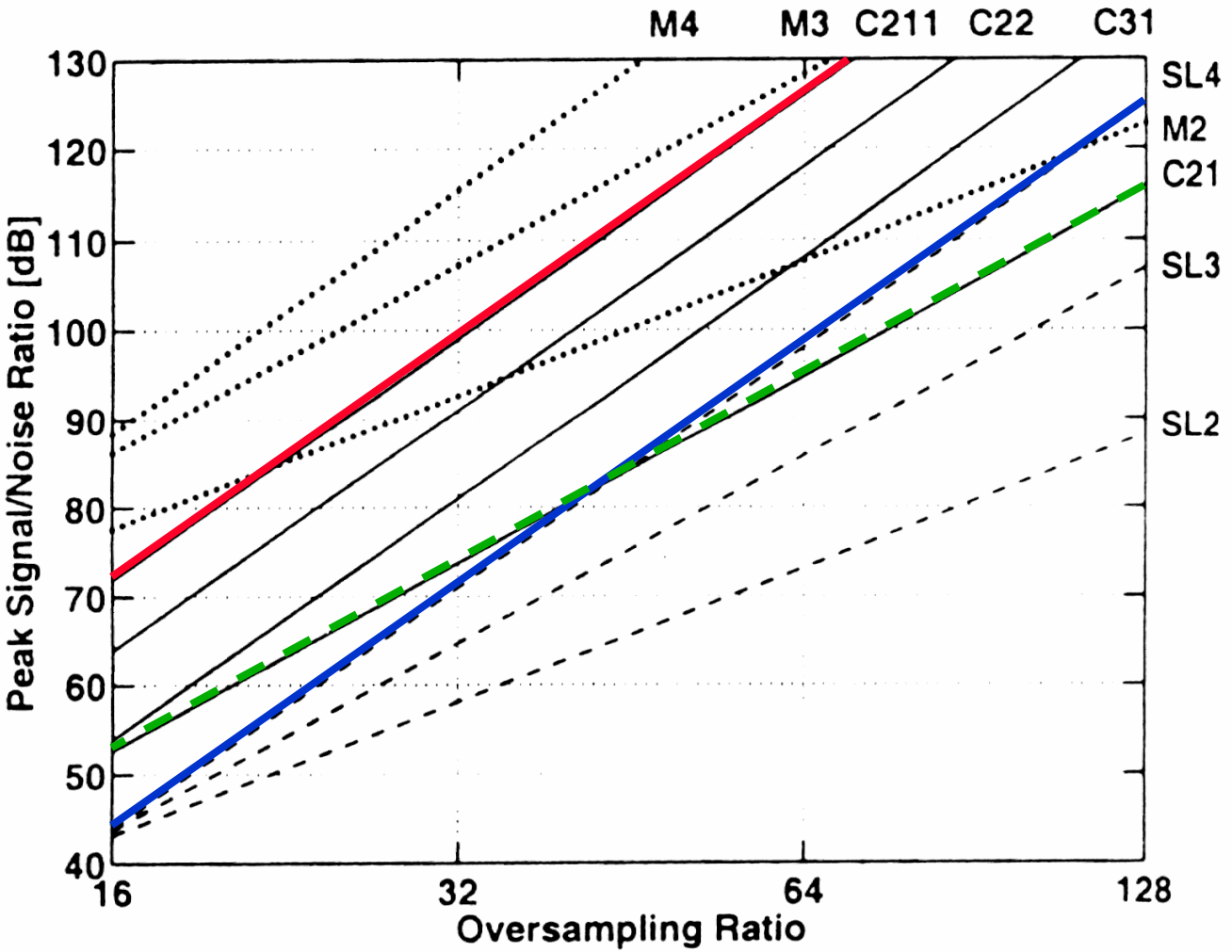
Mash Sigma-delta topologies (2-1-1)



SNR vs OSR for single-bit ΣΔ



Multibit versus Single-bit



Cascaded 2-1-1

Single loop 4th

Cascaded 2-1

Multibit (4 bit)

Ref. Marquez
CAS Sept 98,
1232-1241

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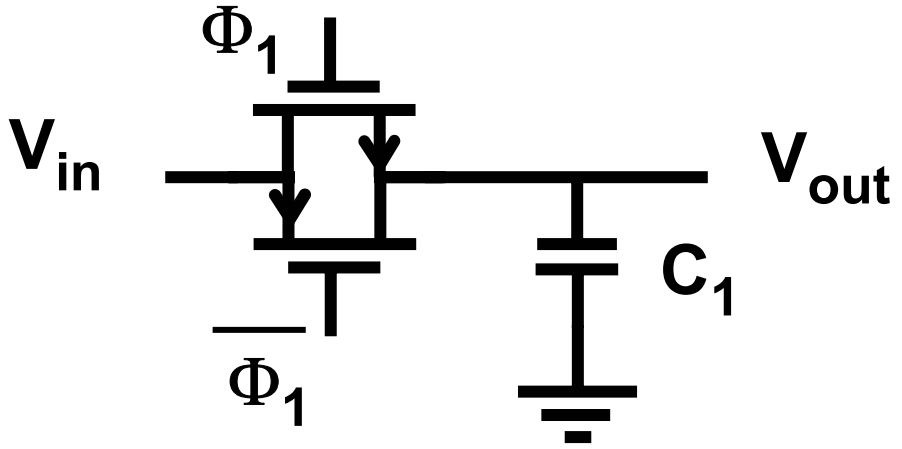
Low Voltage SC: problem

Switch:



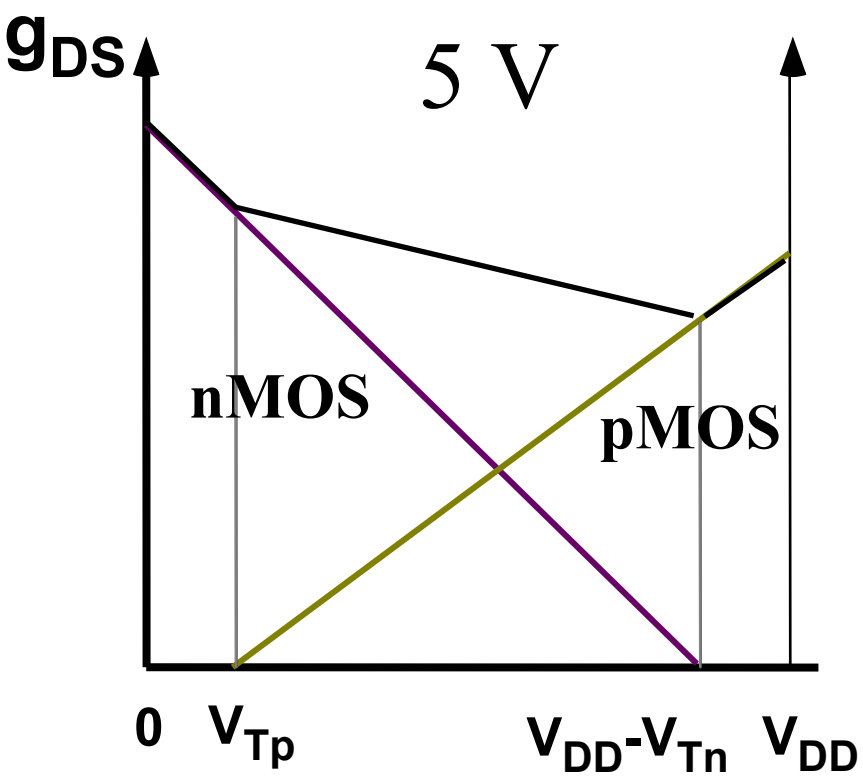
nMOS: $V_{in} < V_{DD} - V_{GSn} \approx V_{DD} - 0.8\ V$

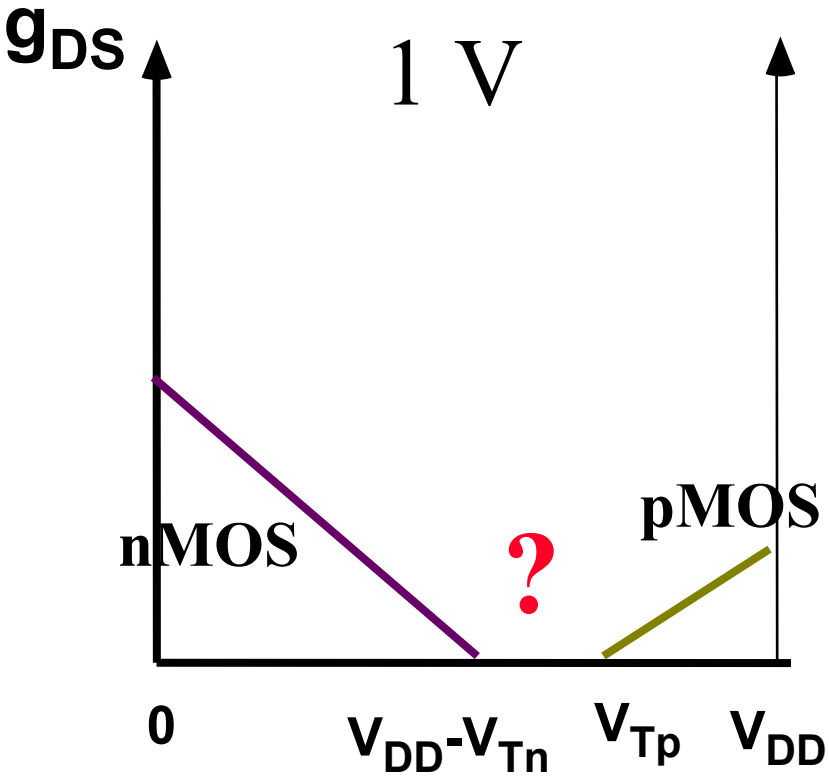
pMOS: $V_{in} > V_{GSp} \approx 0.8\ V$

Limit : $V_{DD} - V_{GSn} = V_{GSp}$

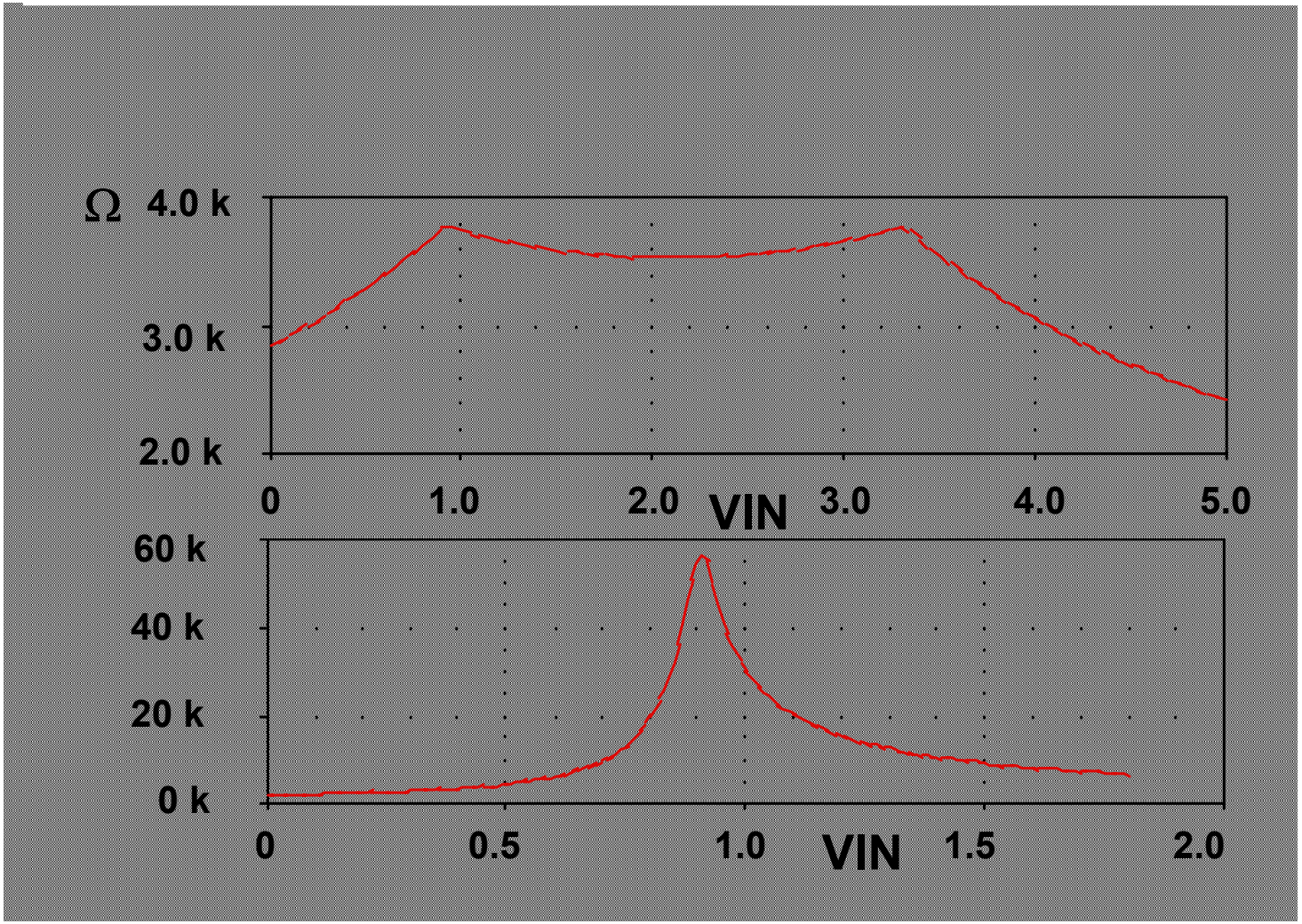
➡ $V_{DDmin} > 1.6\ V$

Low Voltage switch : g_{DS} versus input voltage





Low Voltage switch : ON- resistance



V_{DD} = 5 V

V_{DD} = 1.8 V

Low Voltage SC: solutions

- Low V_T techology
  - special technology : cost
  - switch-off leakage
- On-Chip voltage multipliers
  - poor power efficiency
  - applicability in submicron technologies ?
- Switched Opamp Ref.Crols, ESSCIRC 93, JSSC Aug.94

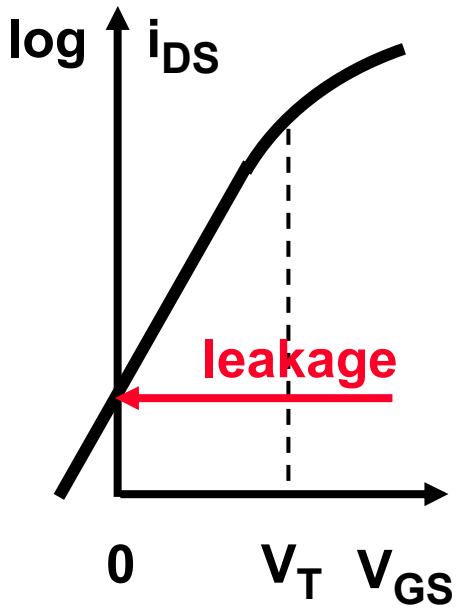
Smaller V_{DD} require smaller V_T

Smaller V_T is not possible because

1. **Leakage : wi curve crosses axis !**
   Minimum value : 0.3 V

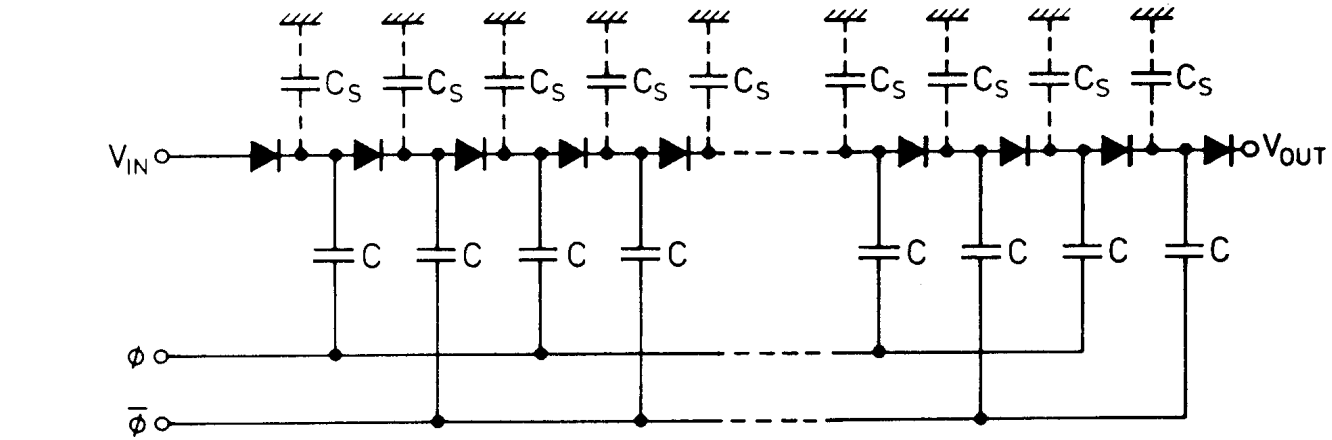
2. **Temperature variations : + 0.2 V**

3. **Mismatch : + 0.1 V**

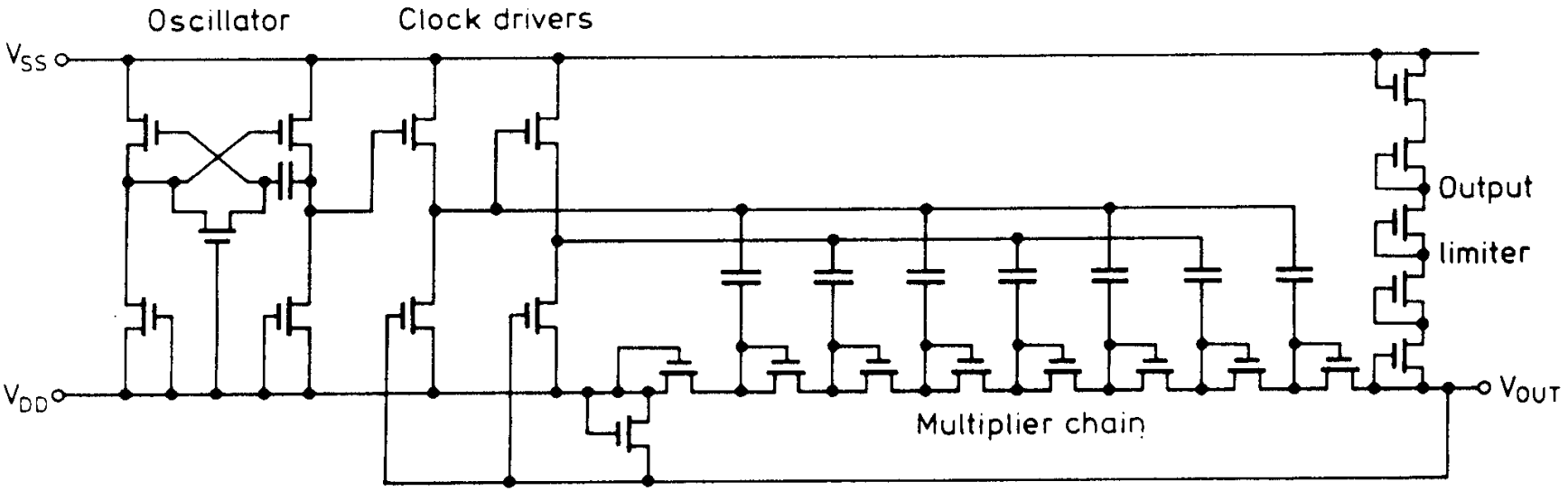


>>> V_T cannot be smaller than 0.3 … 0.4 V

On-chip voltage multipliers



Dickson, ..,
JSSC June 76,
pp.374-378



Voltage multipliers : power efficiency

$$P_{loss} \approx R_{eq} I_{out}^2$$

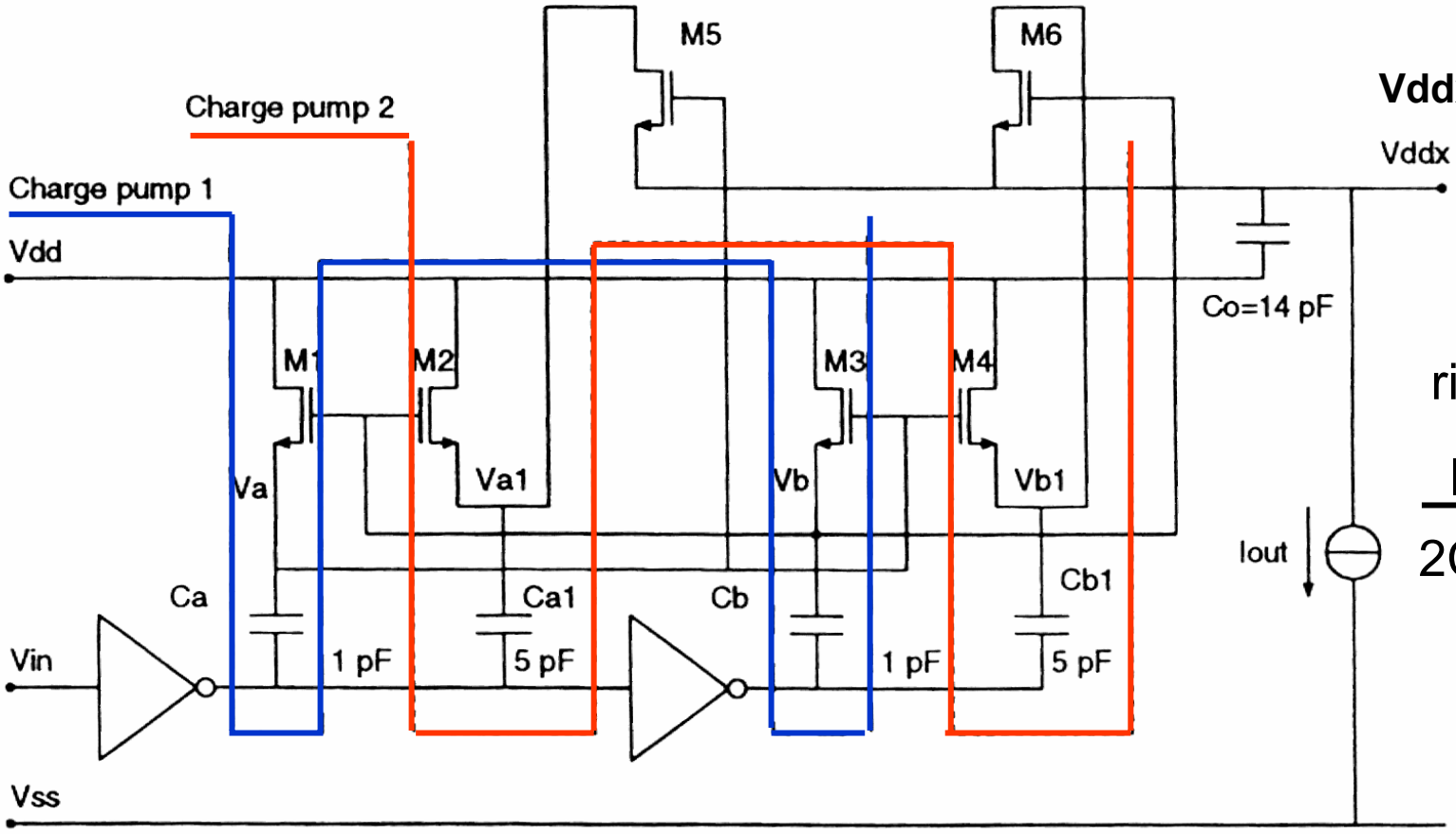
$$P_{VDD} \approx I_{out} V_{DD} \qquad \eta \approx 1 - \frac{R_{eq} I_{out}}{V_{DD}} \approx 50\ \%$$

$$R_{eq} \approx \frac{n}{fC} \frac{1}{\tan (2f R_{on,sw} C)}$$

Drawbacks of voltage multipliers

- High voltage technology:
  - In deep submicron : V_{DD} < 1.8 V in 0.18 μm CMOS
  - Oxide cannot take more !! 800 V/μm or 0.8 V/nm
- Requires high-speed clock drivers
- Injection in substrate : coupling to Analog
- Low power-efficiency

Voltage multiplier for rail-to-rail opamp



Vddx - Vdd ≈ 1 V

60 μA
10 MHz

ripple ≈

$$\frac{I_{out}}{2C_o f_c}\,\frac{1}{g_{m5} r_{o5}}$$

≈ 5 mV

Duisters, .., JSSC July 98,pp.947-955

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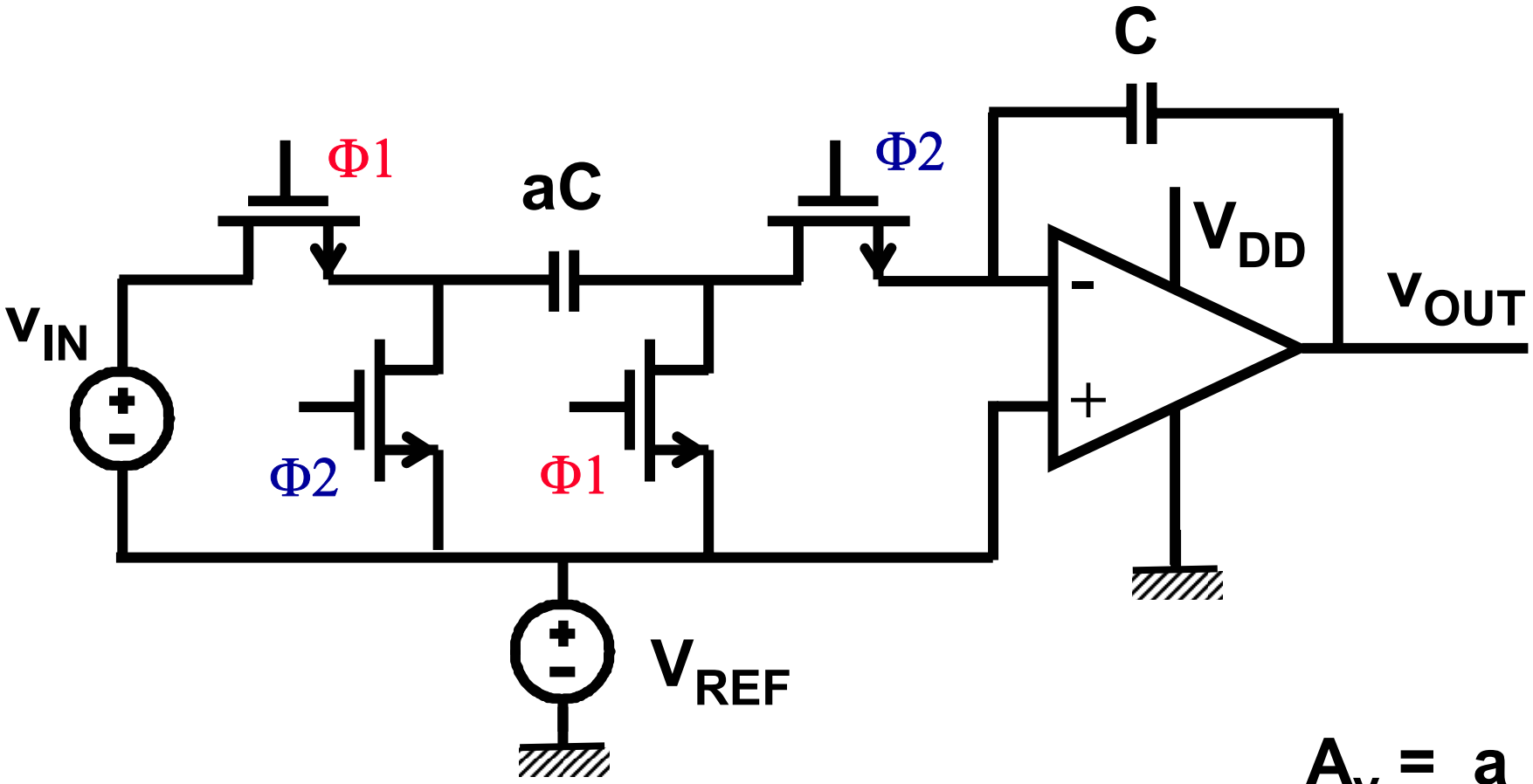
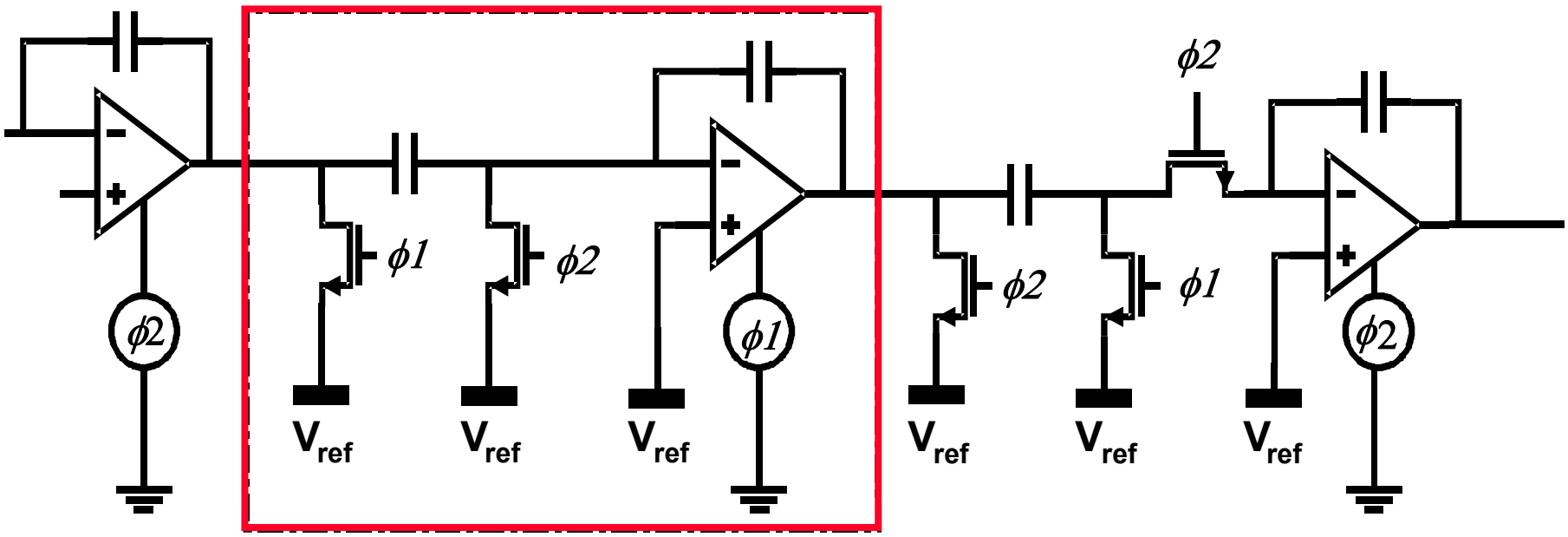
Conventional SC Integrator



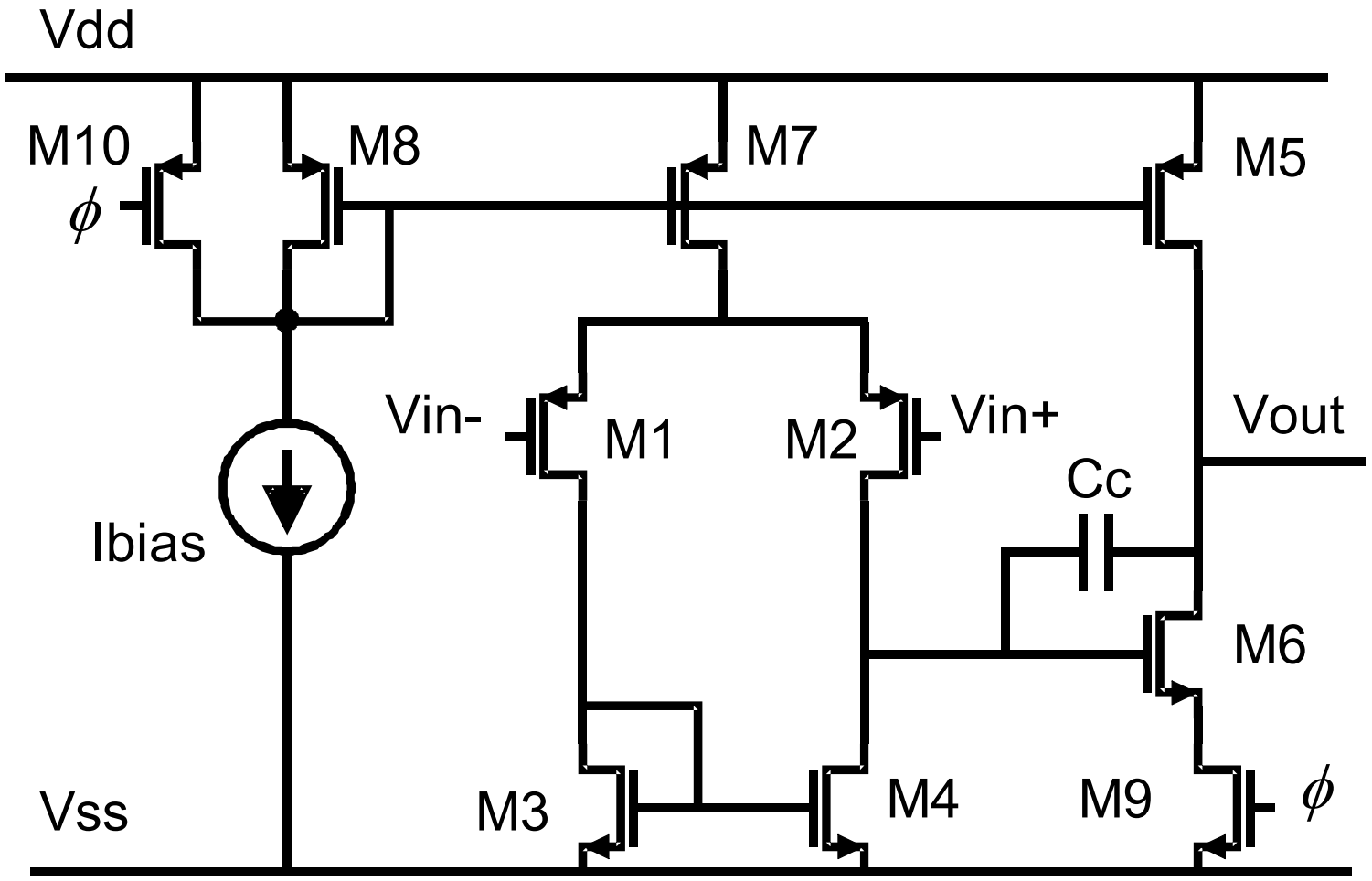
Switched Opamp

Critical input switch
is replaced by a switched opamp



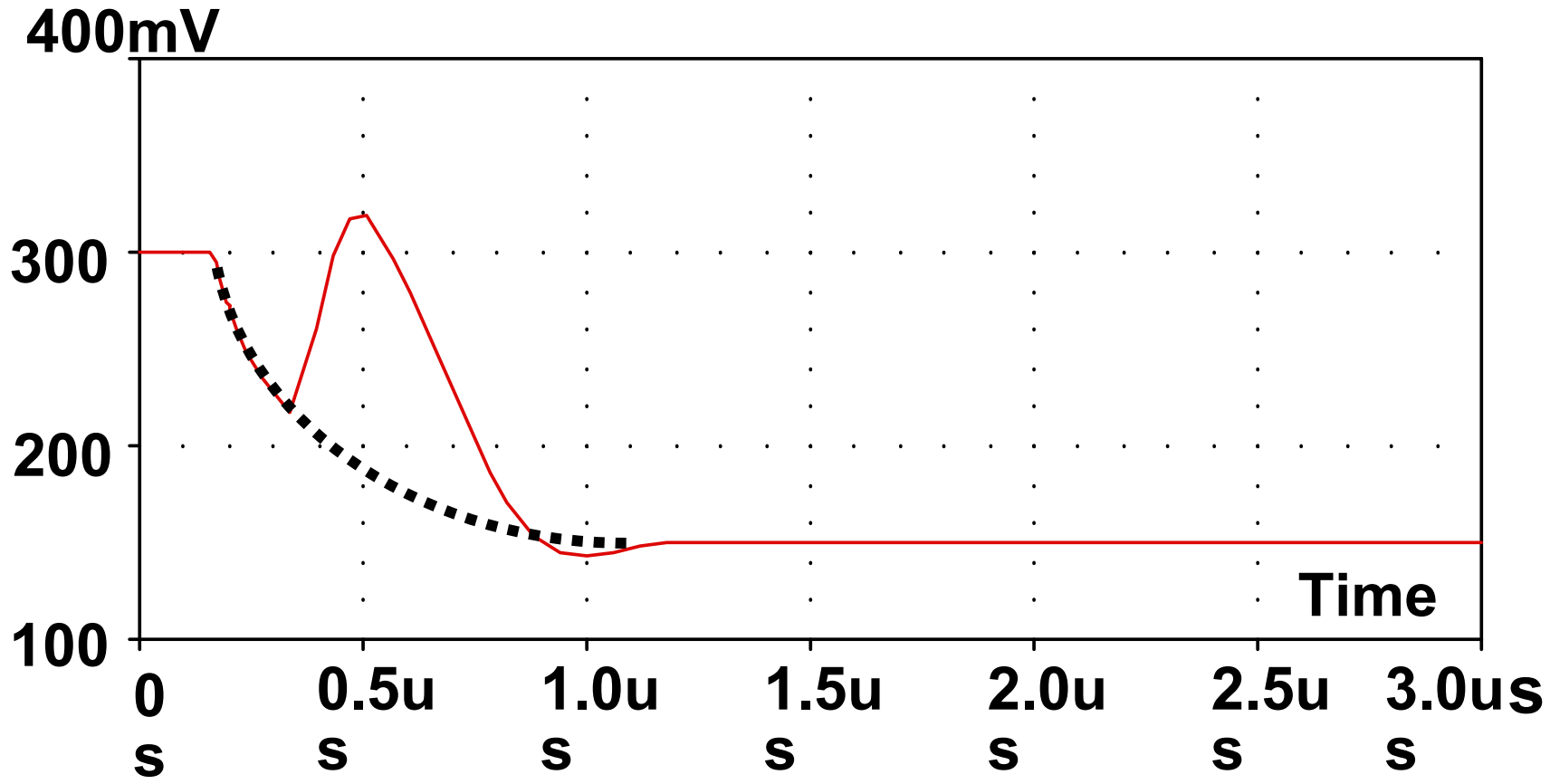
Crols, .., JSSC Aug.94, 936-942

Switched-opamp schematic

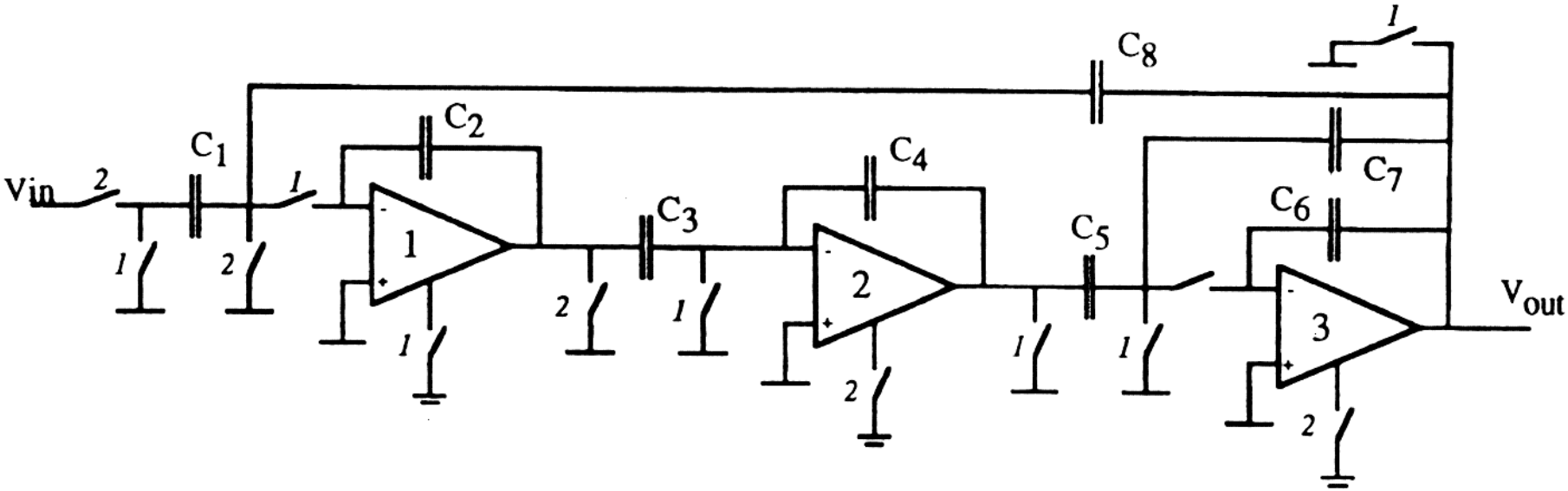


Crols, .., JSSC Aug.94, 936-942

Switched-Opamp response



Switched-opamp low-pass biquad



One extra opamp per biquad

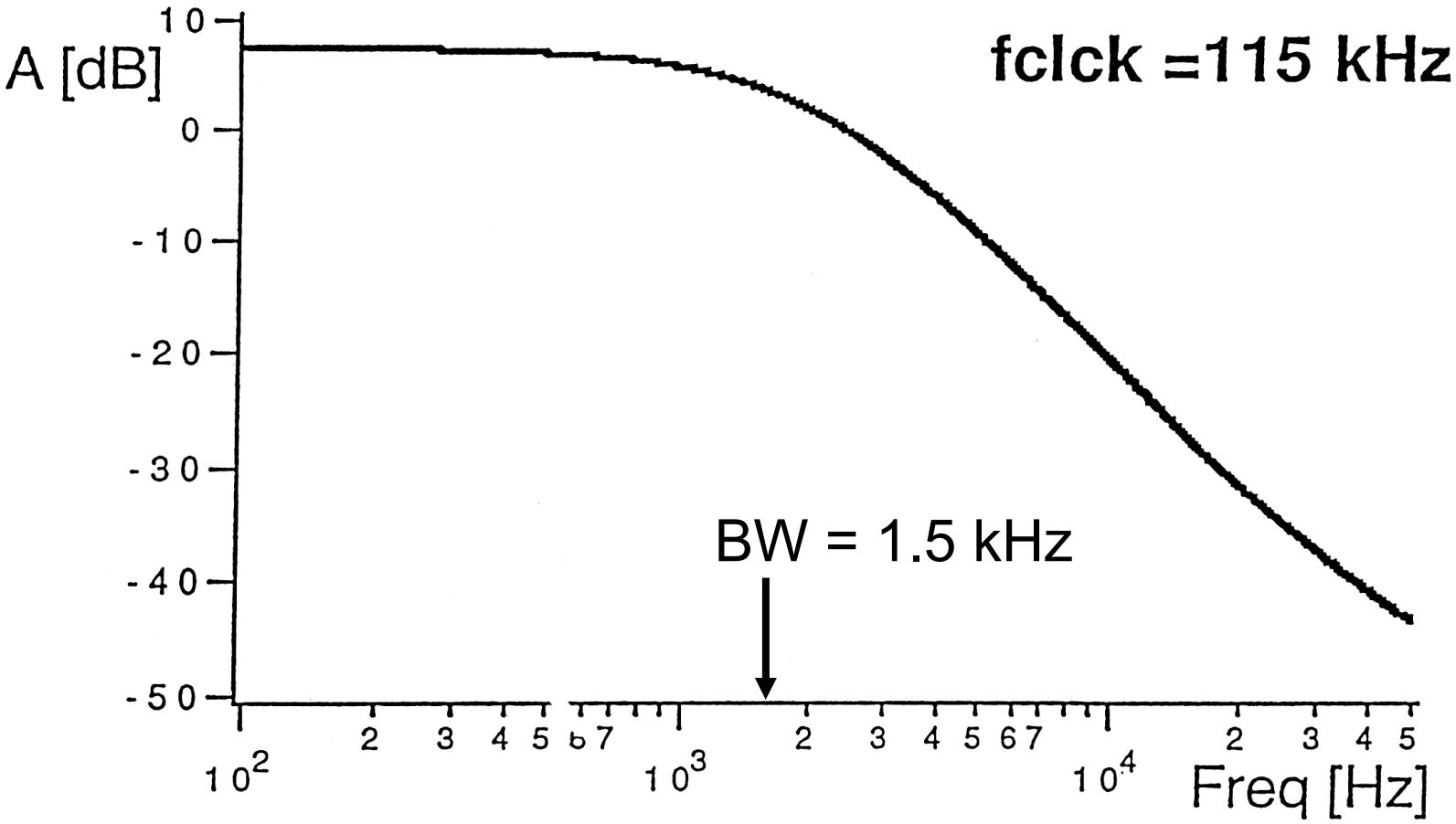
$V_{DD} > V_{GS} + V_{signal}$

$1.2\ V + 0.3\ V = 1.5\ V \quad (0.6\ V_{ptp})$

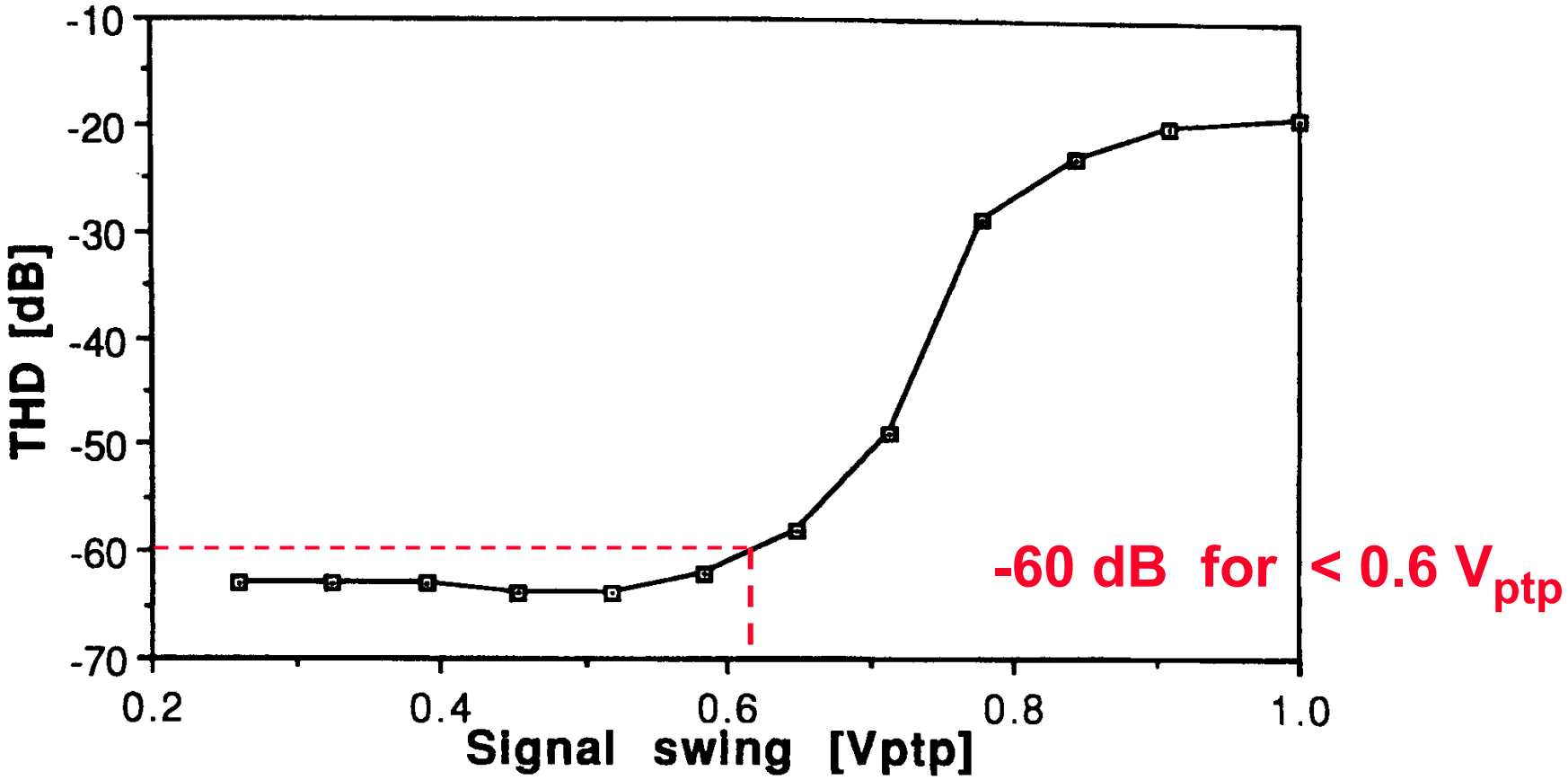
Standard 2.4 μm CMOS ($V_{Tn} \approx V_{Tp} \approx 0.9\ V$)

Crols, .., JSSC
Aug.94, 936-942

Measured transfer characteristic



THD versus input signal swing



Input noise 140 μV_{RMS} : DR > 70 dB

Crols, .., JSSC
Aug.94, 936-942

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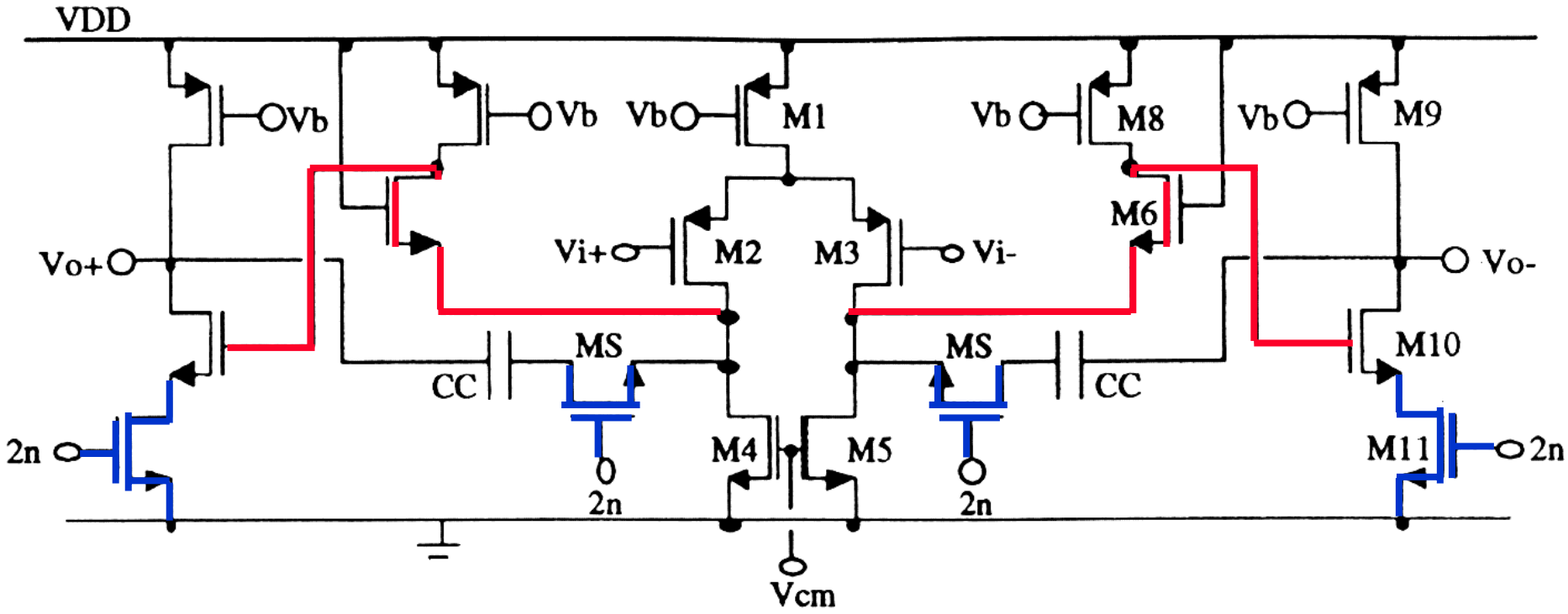
1 Volt OTA



1 V (min: V_T+2V_{DSsat})

Fully differential : 75 dB

30 MHz 1 pF 80 μA

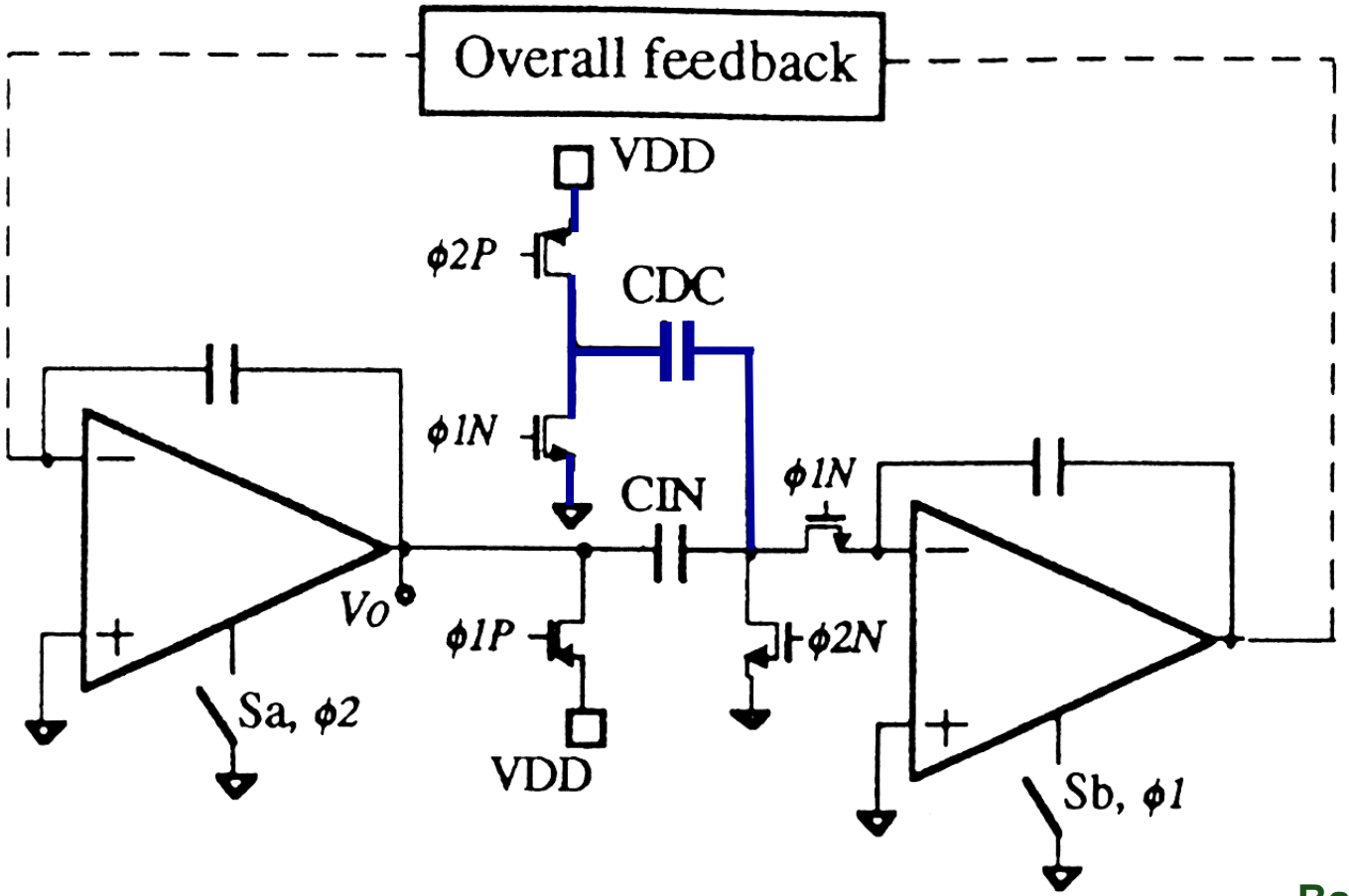
< 100 ns

4 Switches 2n :

Only 2nd stage switched off !

Baschirotto, .. JSSC Dec.97,pp.1979-1986

SO SC integrator

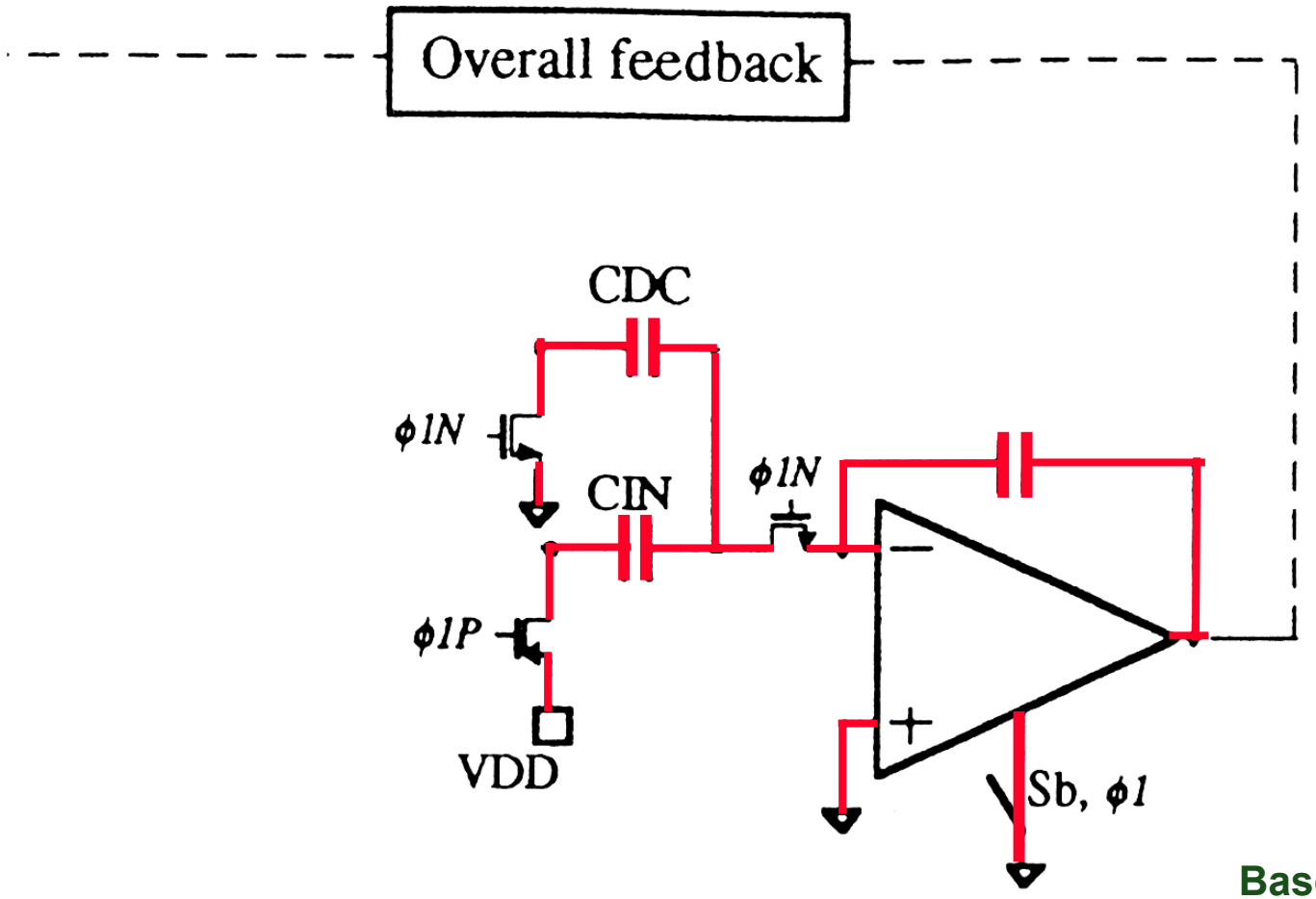


CDC for level shift : CDC= CIN

$V_{O,DC} = V_{DD}/2$

Baschirotto, .. JSSC Dec.97, pp.1979-1986

SO SC integrator : Φ1 closed



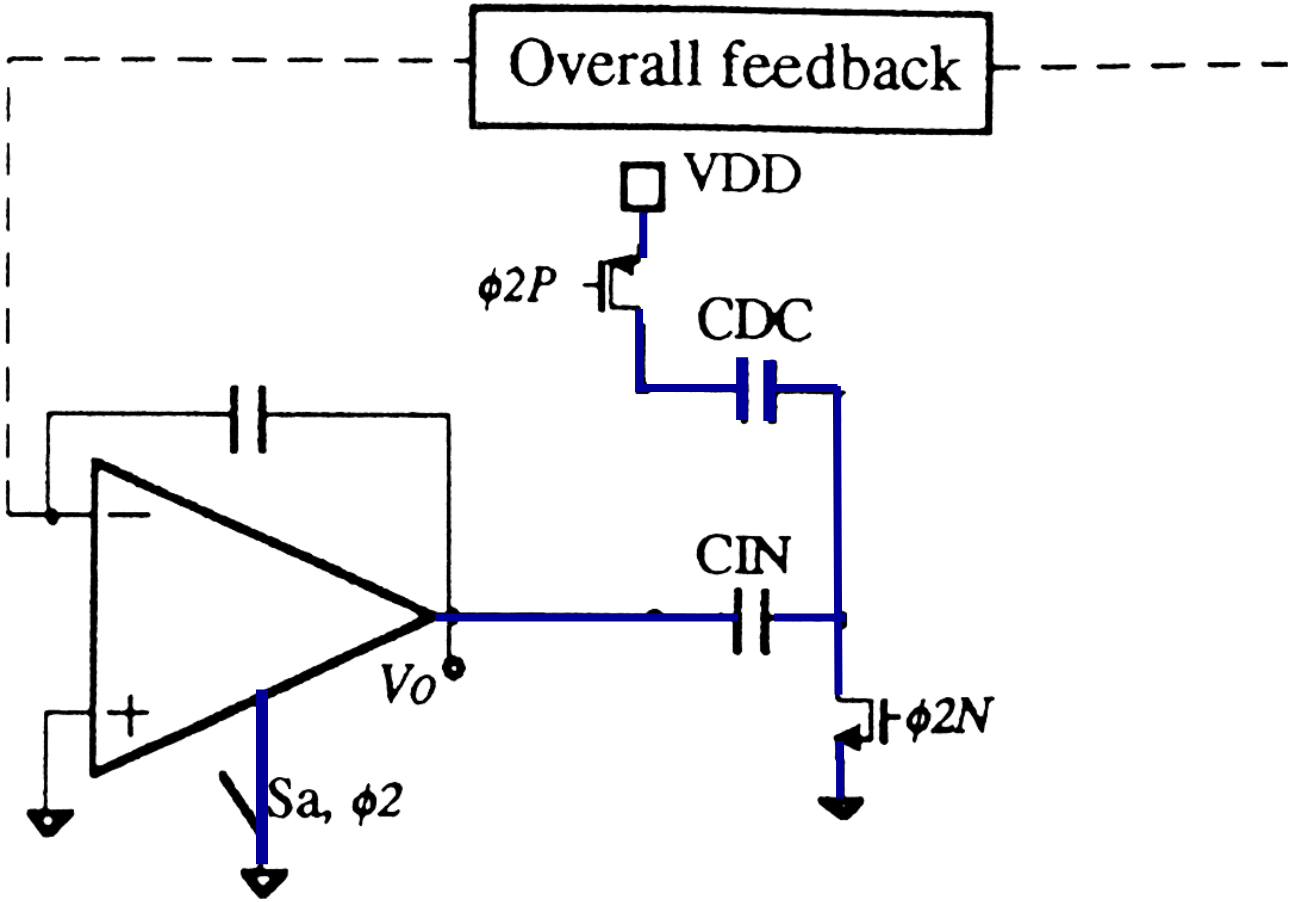
CDC for level shift : CDC= CIN

$V_{O,DC} = V_{DD}/2$

$Q_{TOT} = V_{DD}C_{IN}$

Baschirotto, .. JSSC Dec.97,pp.1979-1986

SO SC integrator : Φ2 closed



CDC for level shift : CDC= CIN

$V_{O,DC} = V_{DD}/2$

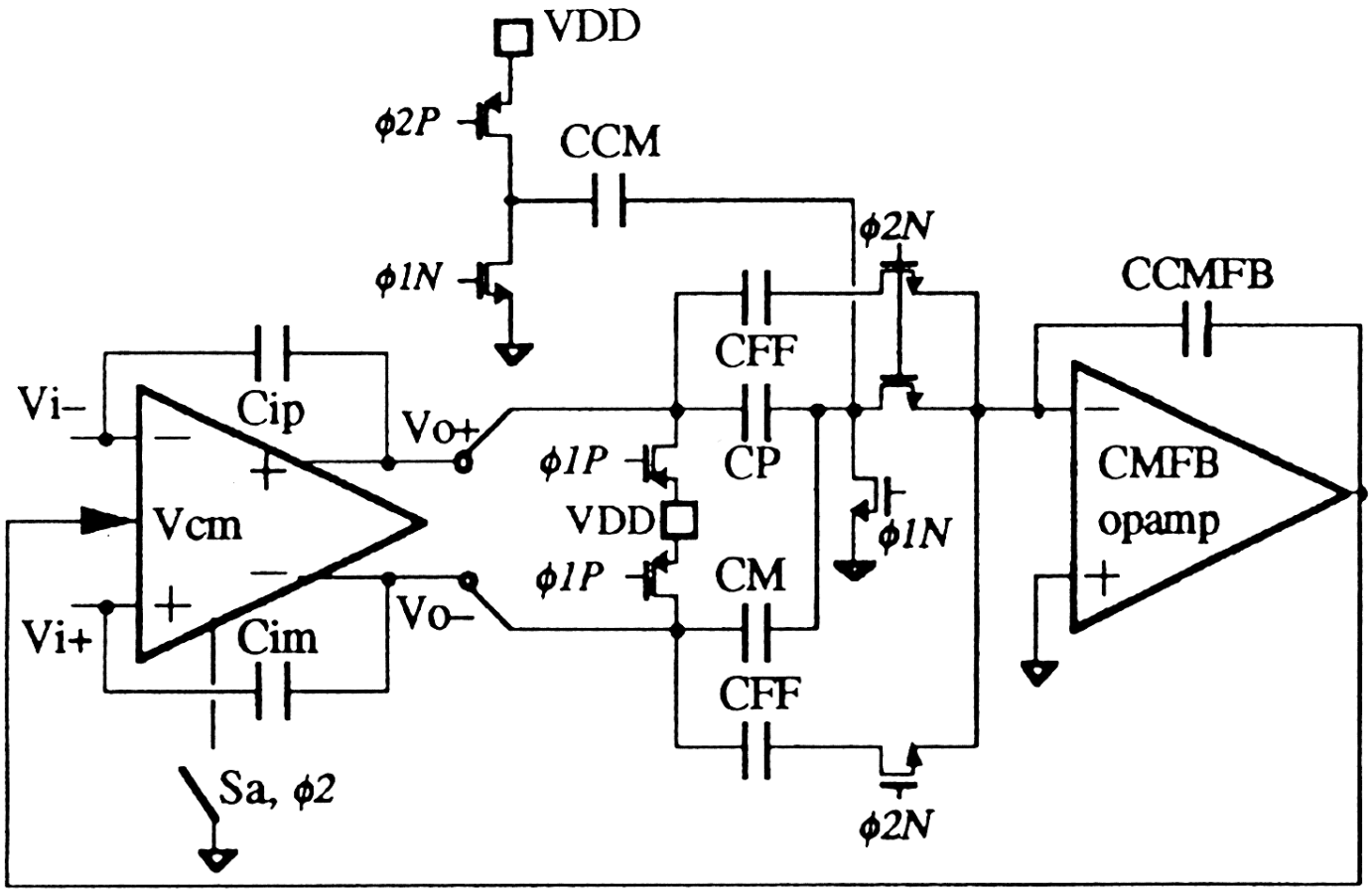
$Q_{TOT} = V_{DD}C_{DC} + V_OC_{IN}$

if $C_{DC} = C_{IN}$

$V_{DD}/2 = V_O$

Baschirotto, .. JSSC Dec.97,pp.1979-1986

CMFB with level shifting



$C_M = C_P = 0.1$ pF

$C_{CM} = 0.1$ pF

$C_{CMFB} = 2$ pF

$C_{FF} = 0.1$ pF

provides zero

$V_{OUT,DC} = V_{DD}/2$

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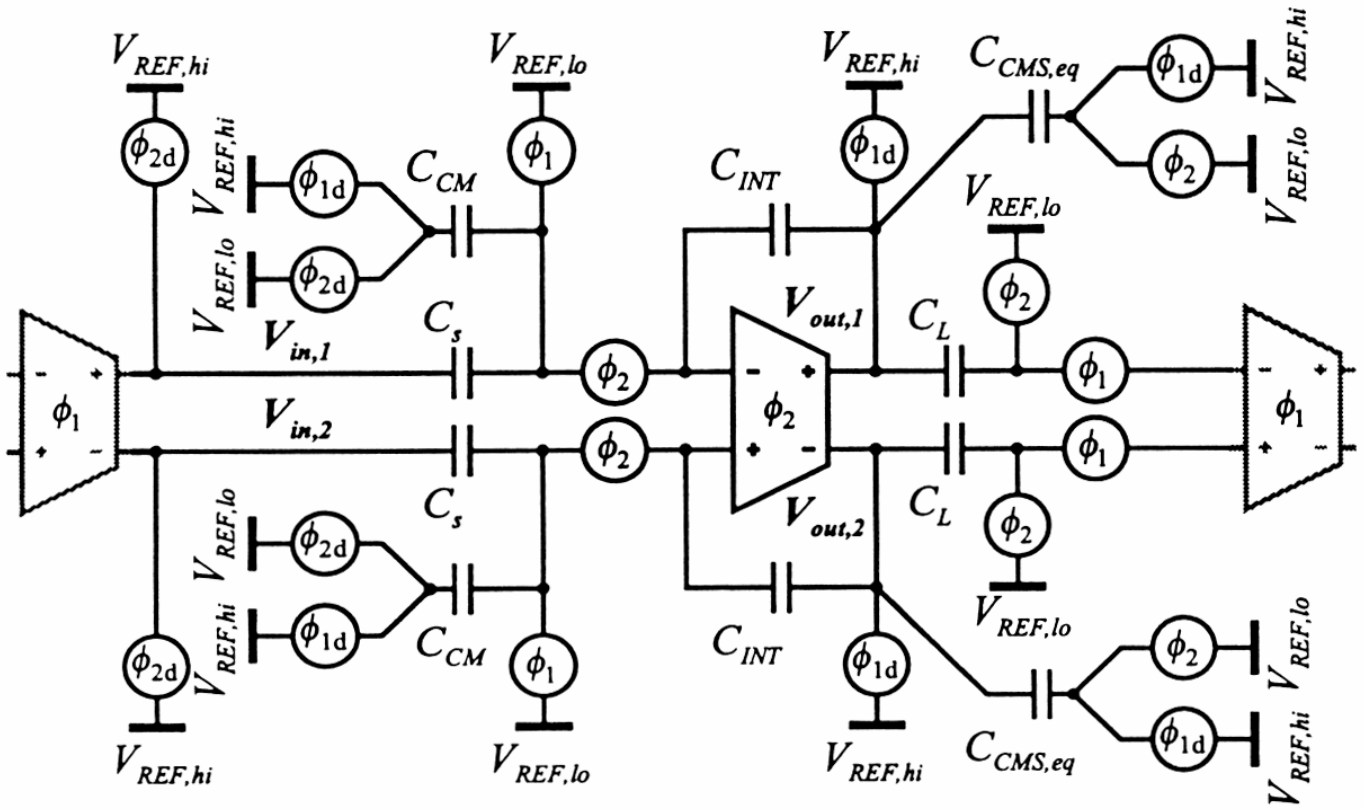
Differential SO integrator



C_S Sampling

C_{INT} Integrat.

C_L Load

C_{CM} Level shift

$C_{CMS,eq}$ CMFB

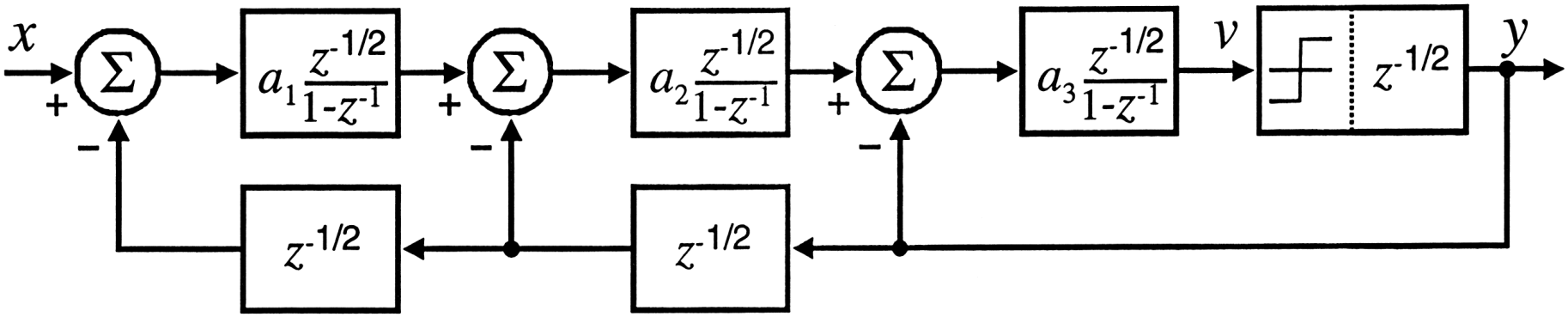
$V_{REF,hl} = V_{DD}$

$V_{REF,lo} = 0$

Peluso, ..., JSSC, Dec.98, 1887-1896

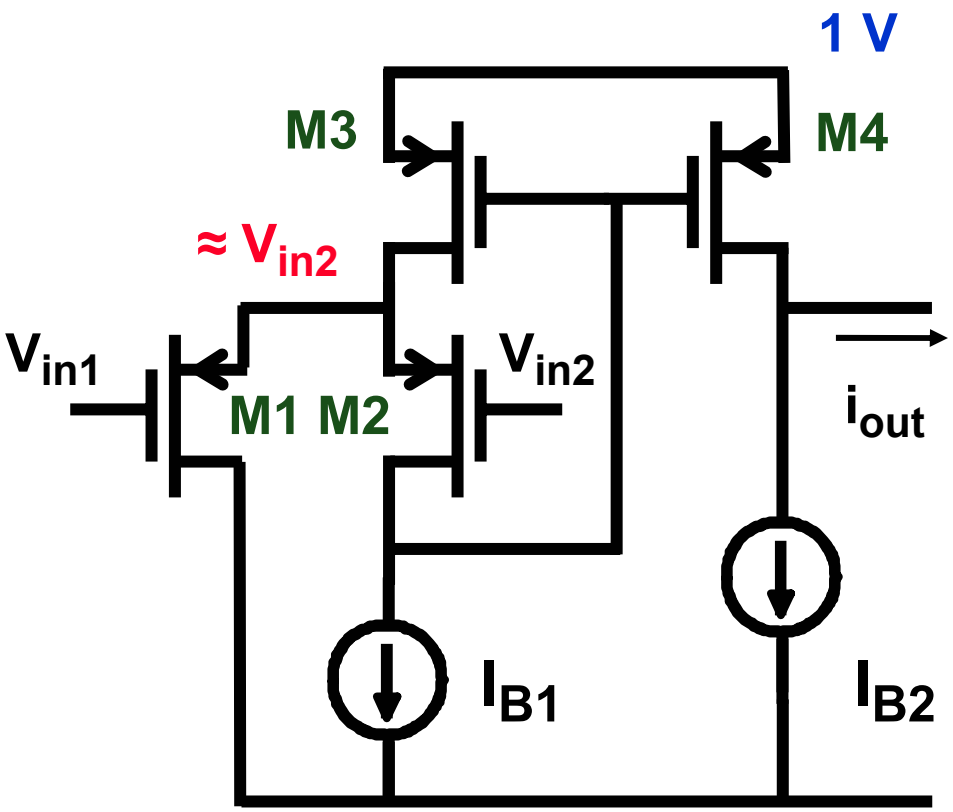
Peluso etal “Design of low-voltage low-power CMOS Delta-Sigma ADC’s”, Kluwer 1999

ΣΔ topology with half-delay integrators



- 3rd order single-loop implementation
- coefficients $a_1 = 0.2$; $a_2 = 0.5$; $a_3 = 0.5$
- 1/2 phase delays in feedback path

Class AB differential Voltage amplifier



$V_T = 0.6$ V

$V_{GS} - V_T = 0.2$ V

$V_{GS} = 0.8$ V

$V_{DSsat} = 0.2$ V

M2 is source follower

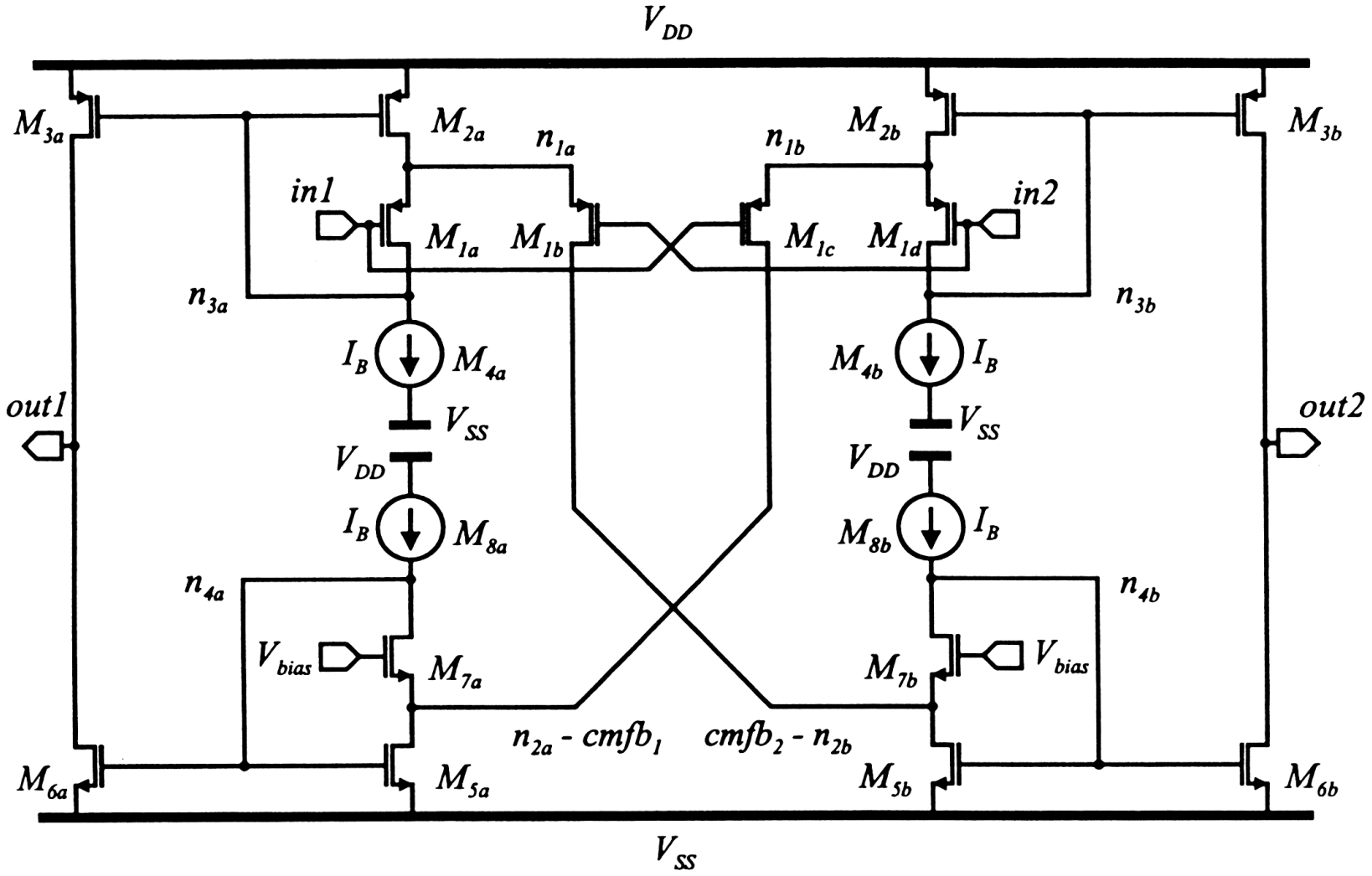
$V_{GS1} = V_{in1} - V_{in2}$

$i_{out} \sim (V_{in1} - V_{in2})^2$

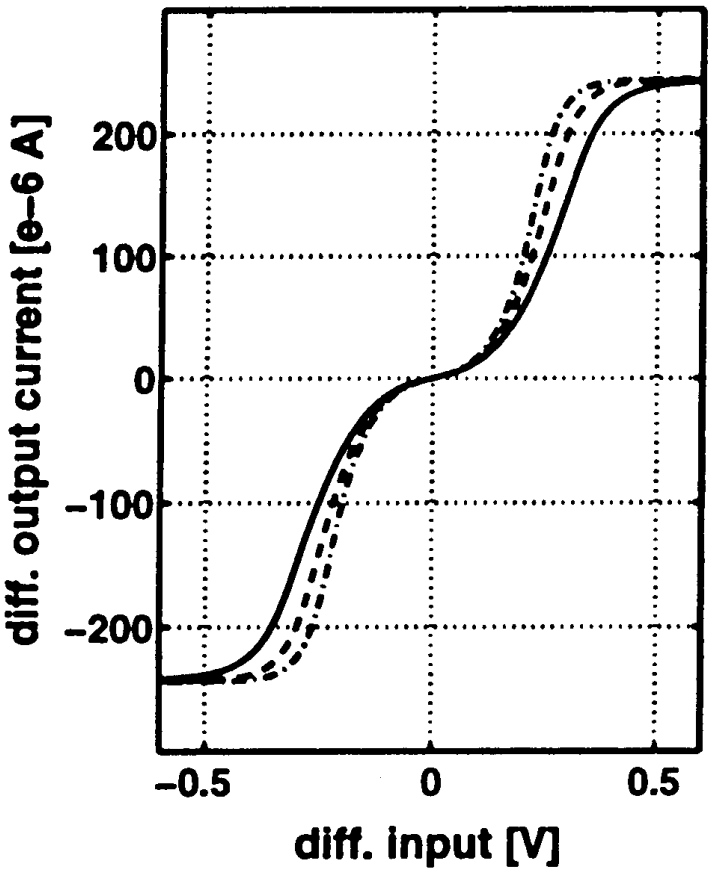
>>> Class AB

Peluso, ..., JSSC, Dec.98,pp.1887-1896

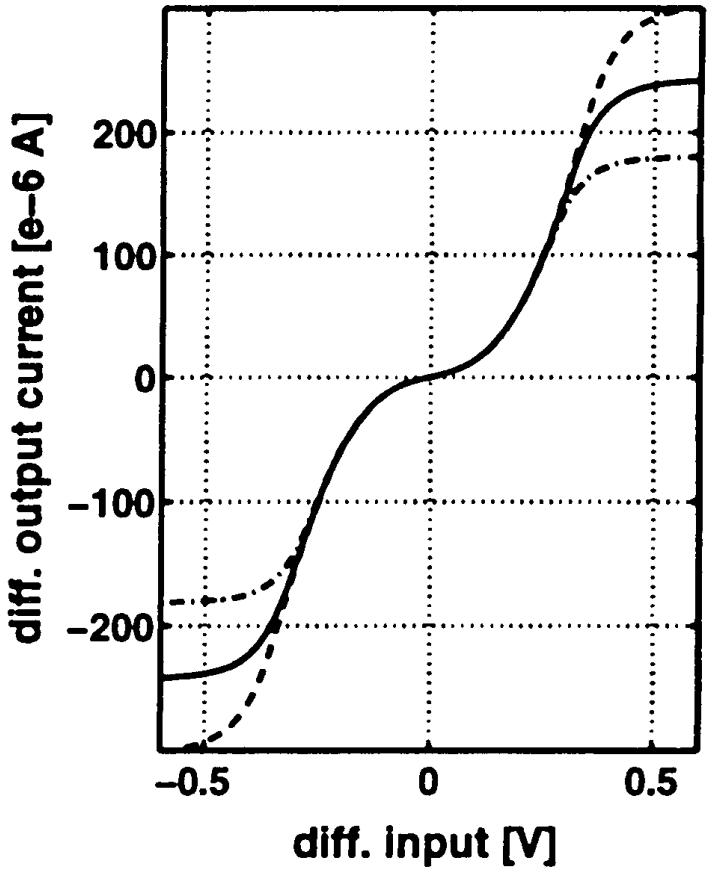
Differential class AB OTA



Class AB characteristic

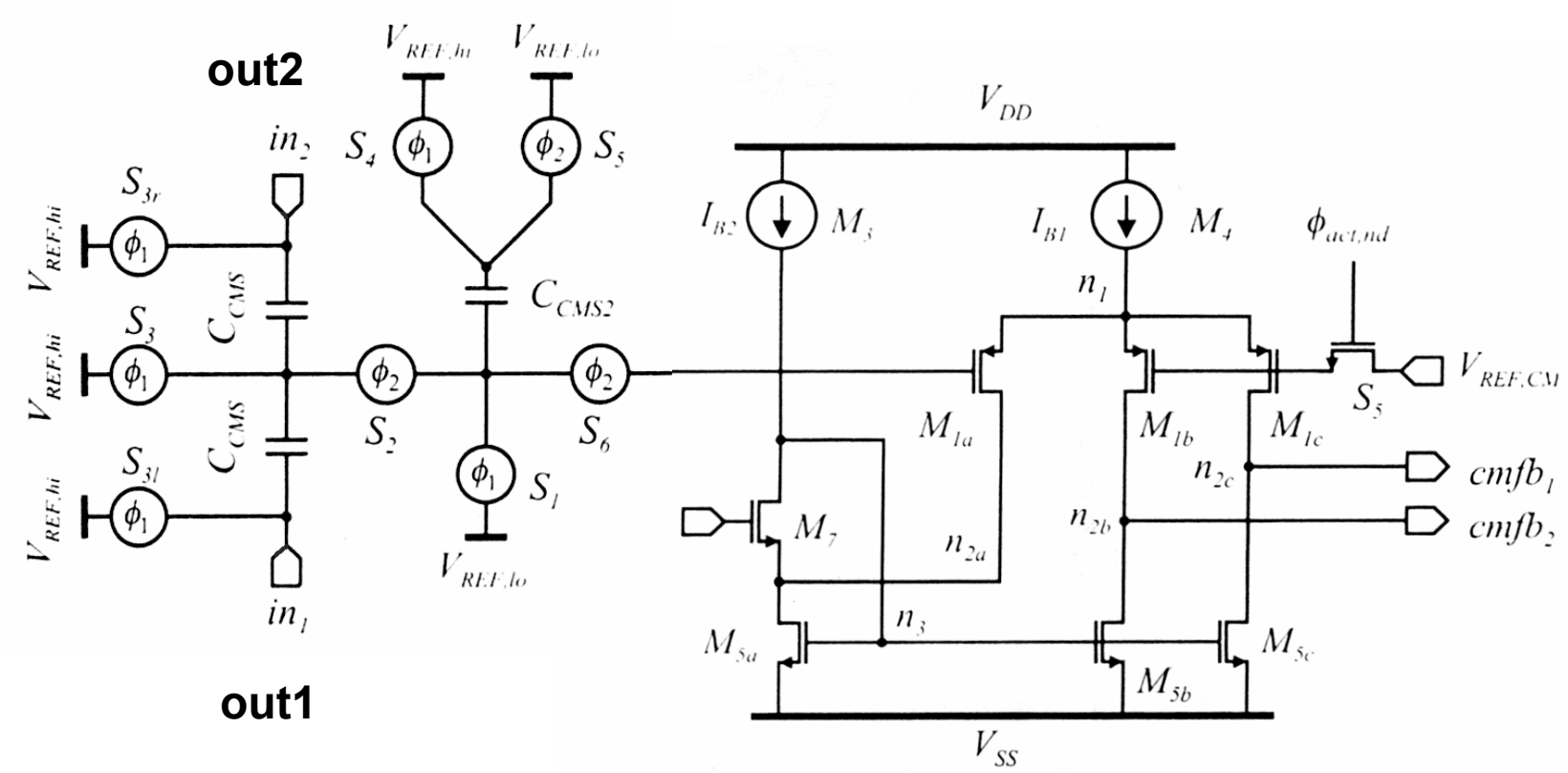


Larger input W/L

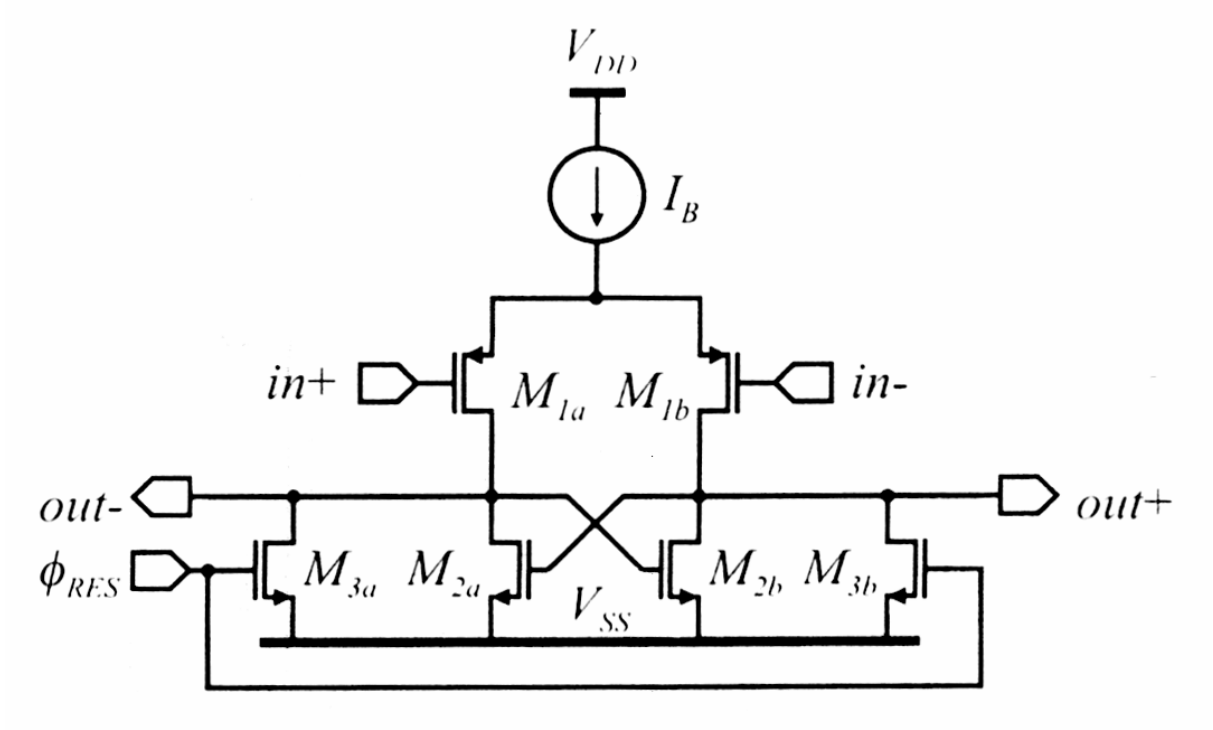


Larger current source W/L

CMFB and level-shift



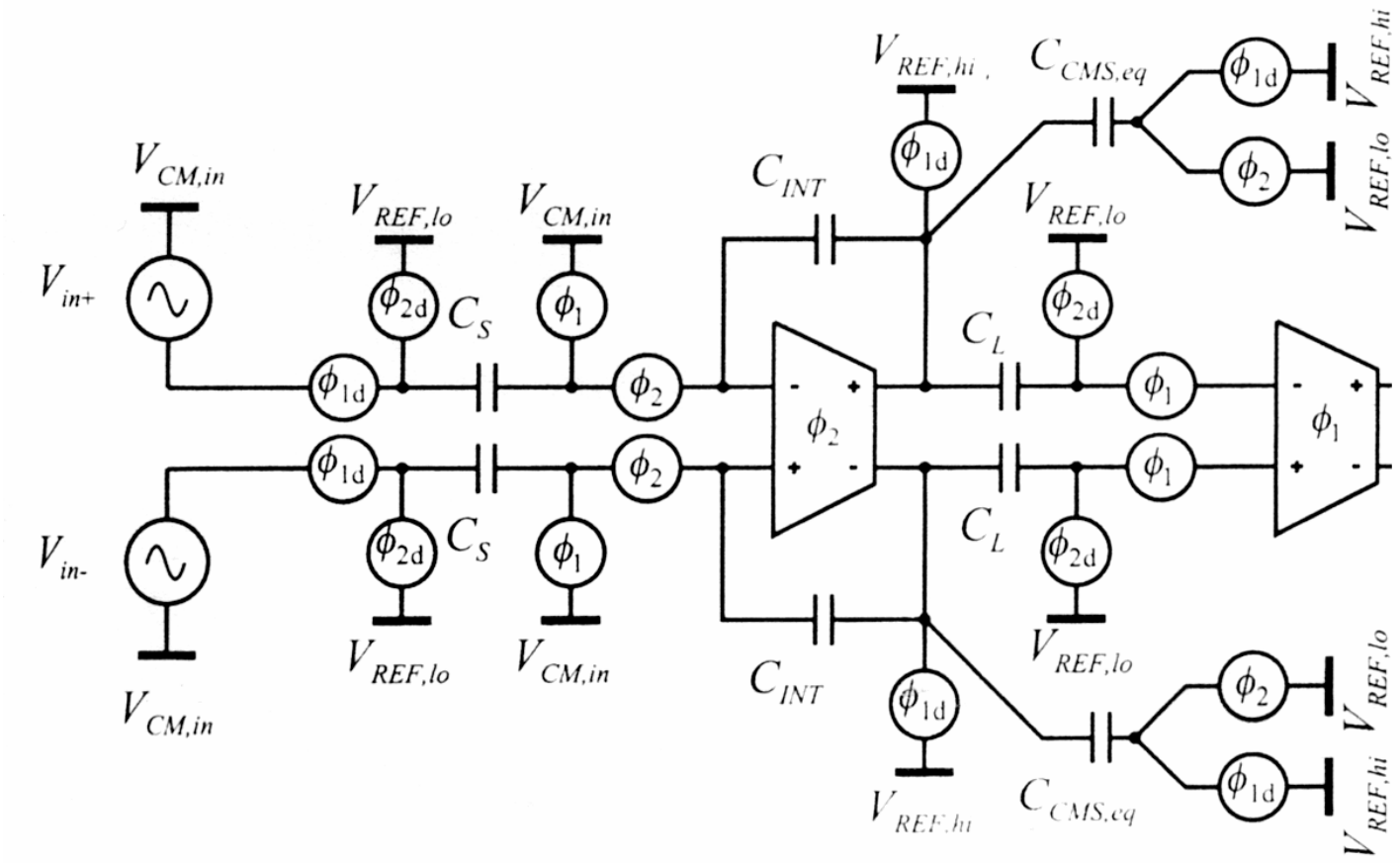
Low voltage comparator (level shift omitted)



Two switches

Input at V_{SS}

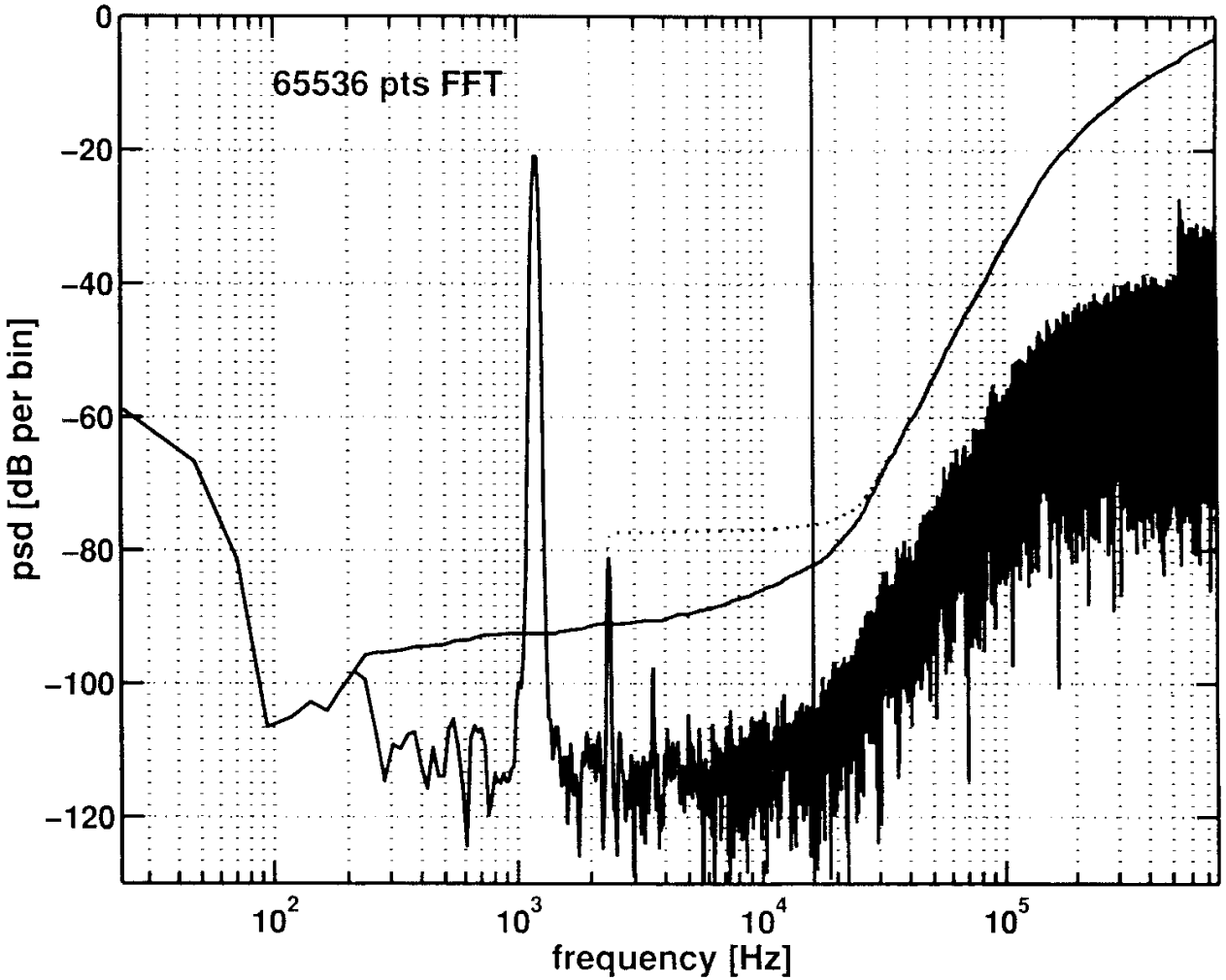
The input integrator



$V_{REF,hi} = V_{DD}$

$V_{REF,lo} = 0$

Spectrum for maximum input signal (470 mV_{ptp})



BW 16 kHz

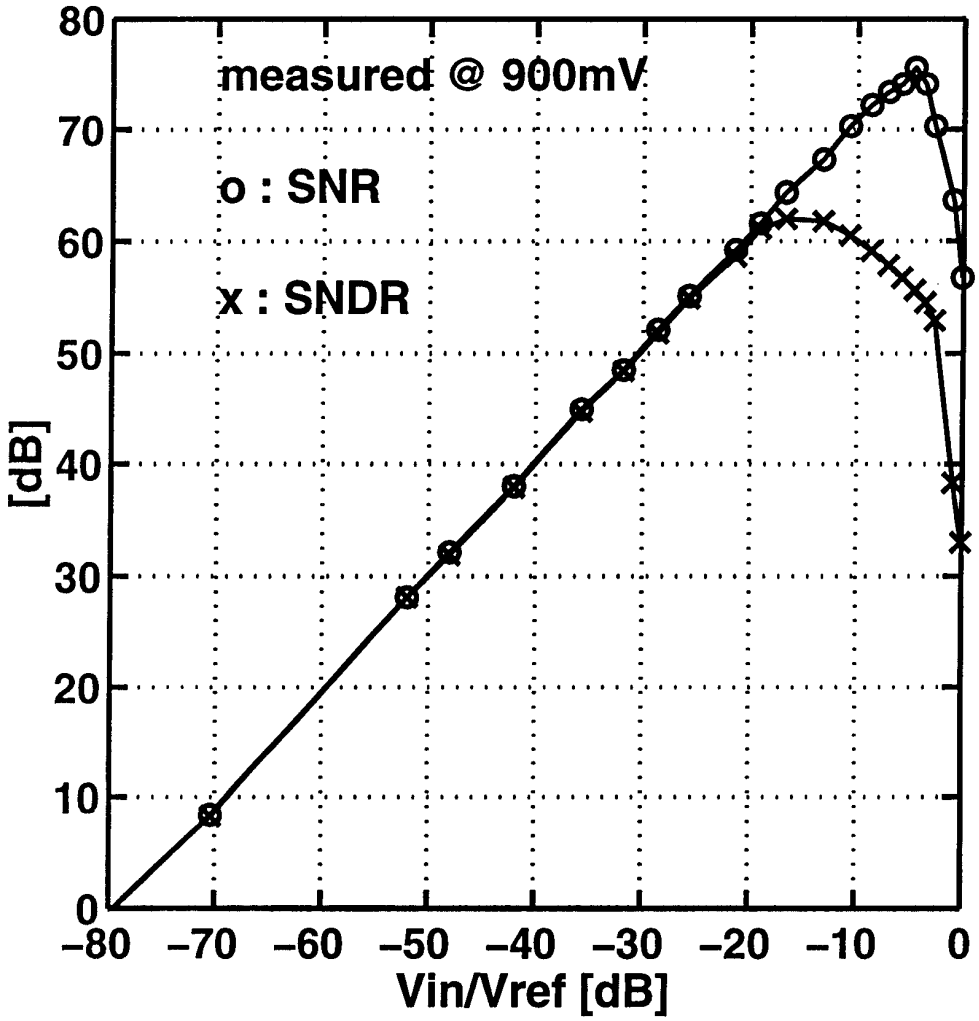
Clock freq. 1.5 MHz

Peak SNR 76 dB

Peak SNDR 62 dB

Peluso, ..., JSSC
Dec.98,pp.1887-1896

SNDR versus input signal level

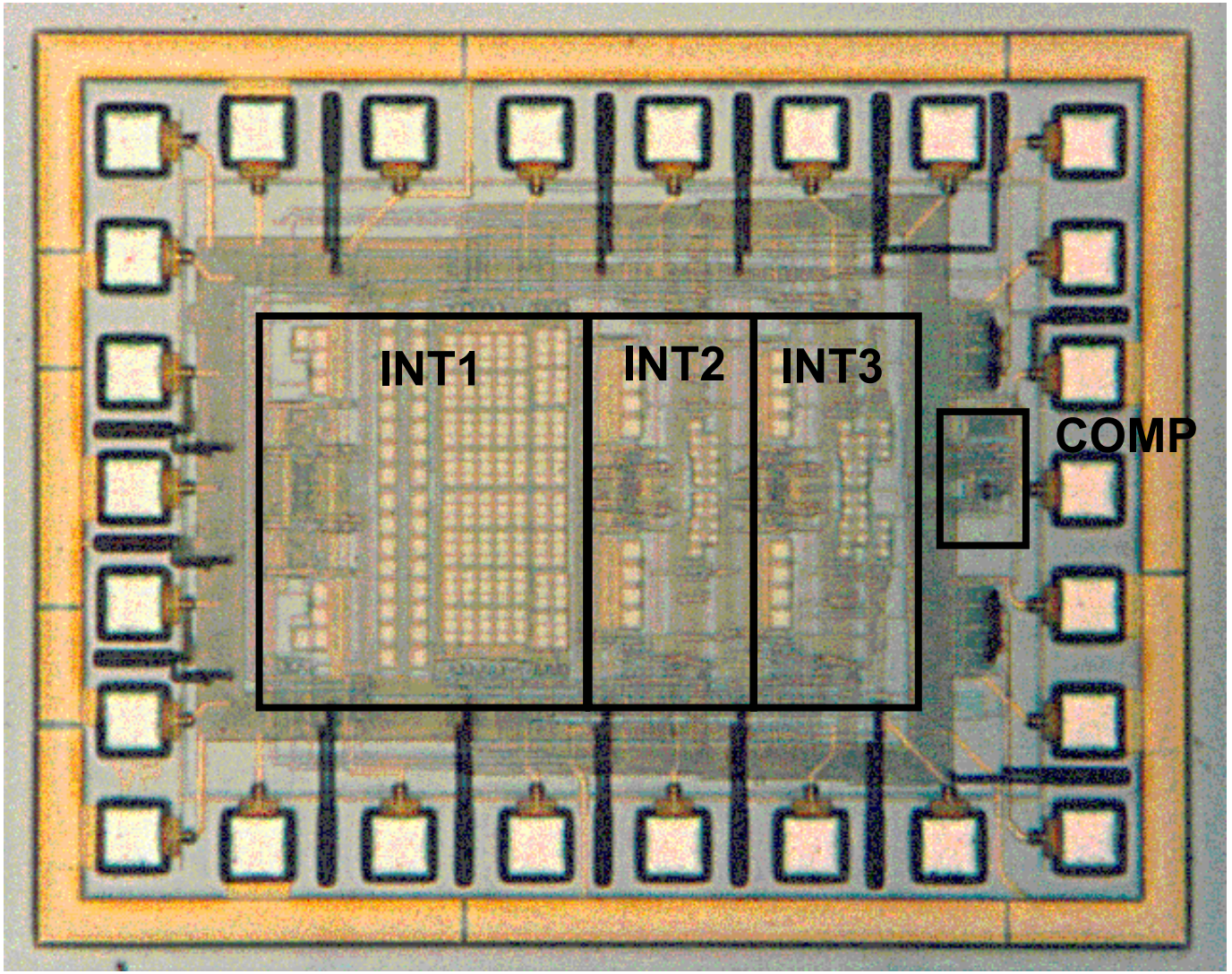


Peak SNR = 76 dB

DR = 77 dB

SNDR = 62 dB

SO 12 bit 0.9 V 40 μW CMOS ΣΔ



0.5 μm CMOS

V_{Tn} = 0.62 V

V_{Tp} = 0.55 V

V_{DD} = 0.9 V

40 μW

Peluso, ...
JSSC Dec.98,
pp.1887-1896

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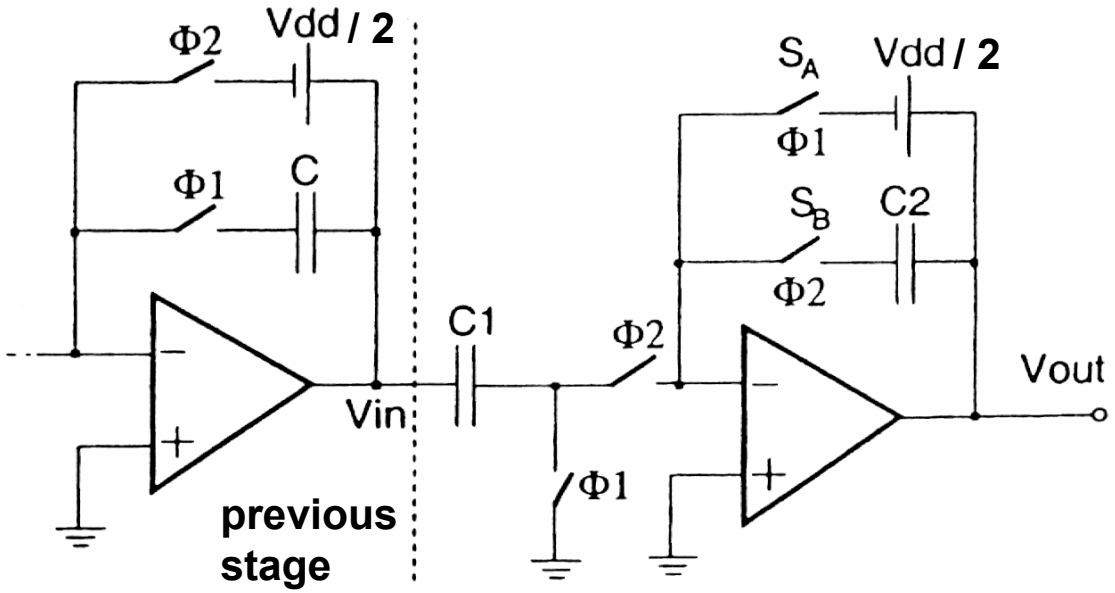
Reset-opamp integrator



V_{out} = 0 … 1 V

$V_{out,av} \approx 0.5$ V

$V_{in} \approx 0$ V

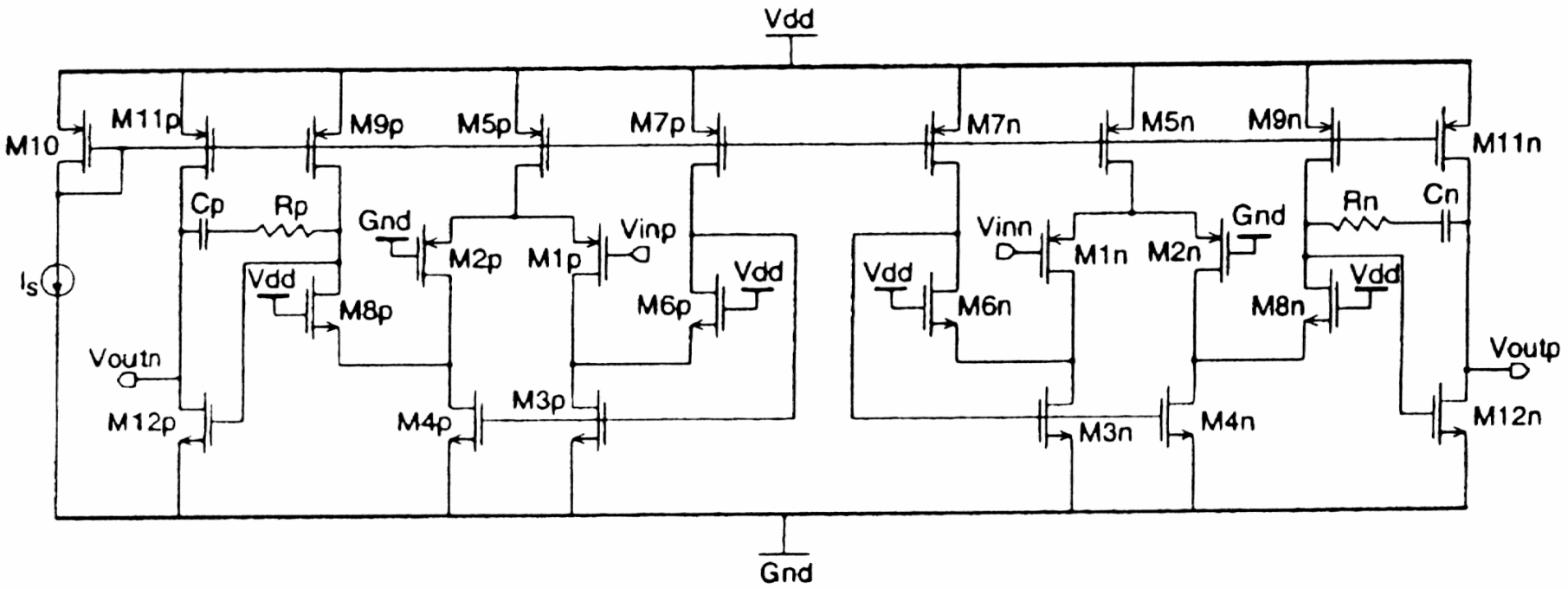
$V_{dd}/2 \approx 0.5$ V

On Φ_1 :	$Q_1 = C_1 V_{in}$	Q_2	$V_{out} = 0$
On Φ_2 :	$Q_1 = 0$	$Q_2 + C_1 V_{in}$	V_{out}

Level shift needed to avoid forward biased junctions !

Keskin, .., JSSC July 02, 817-824

Pseudo-differential opamp

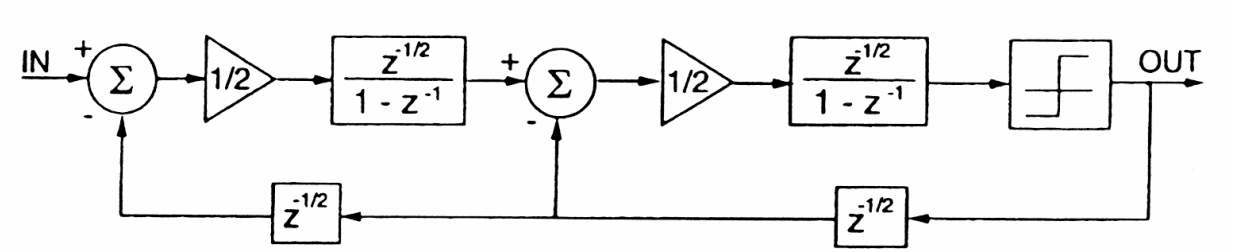


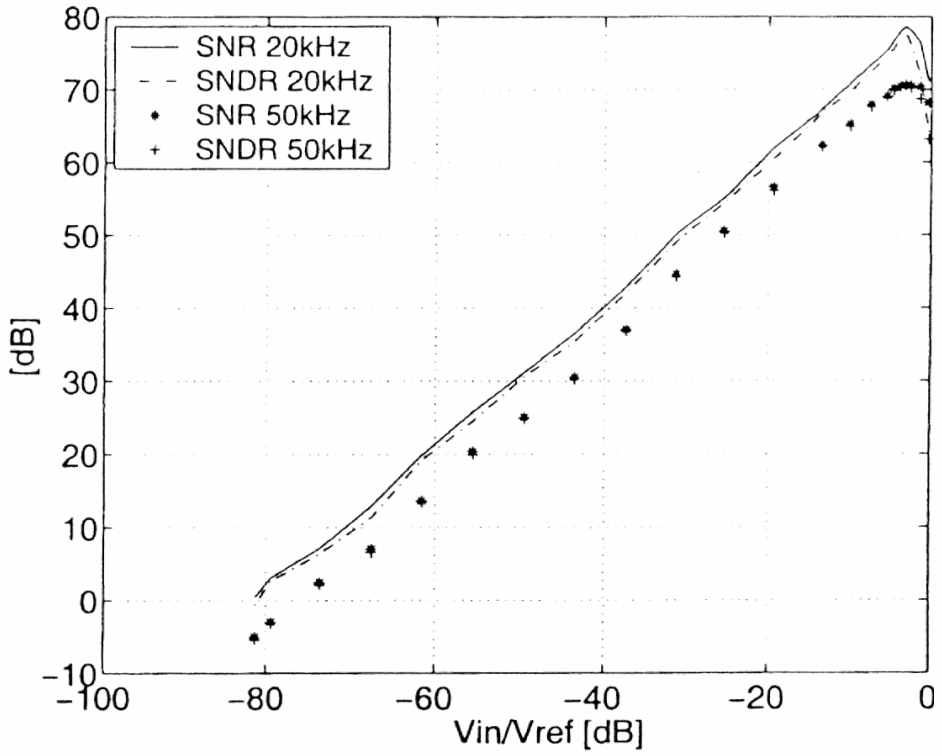
170 MHz 100 V/μs 3.5 pF 1 V 200 μA

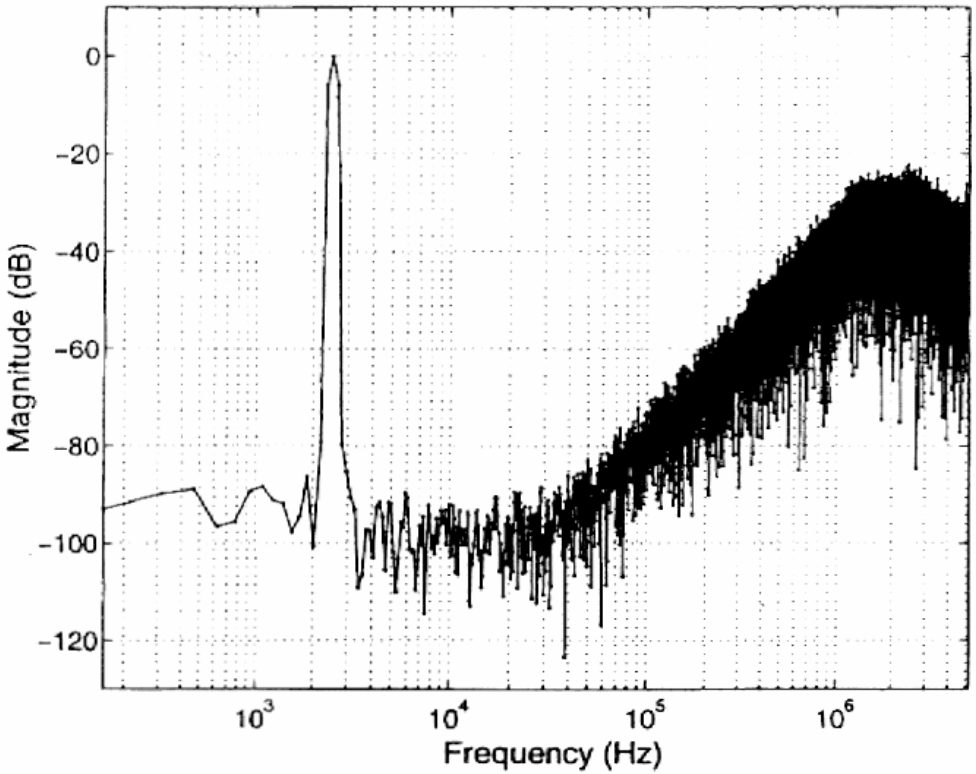
0.35 μm CMOS $V_{Tn} \approx 0.52$ V $V_{Tp} \approx 0.45$ V

Ref.Keskin, JSSC July 2002, 817-824

1-Volt 2nd-order 13 -bit ΣΔ modulator







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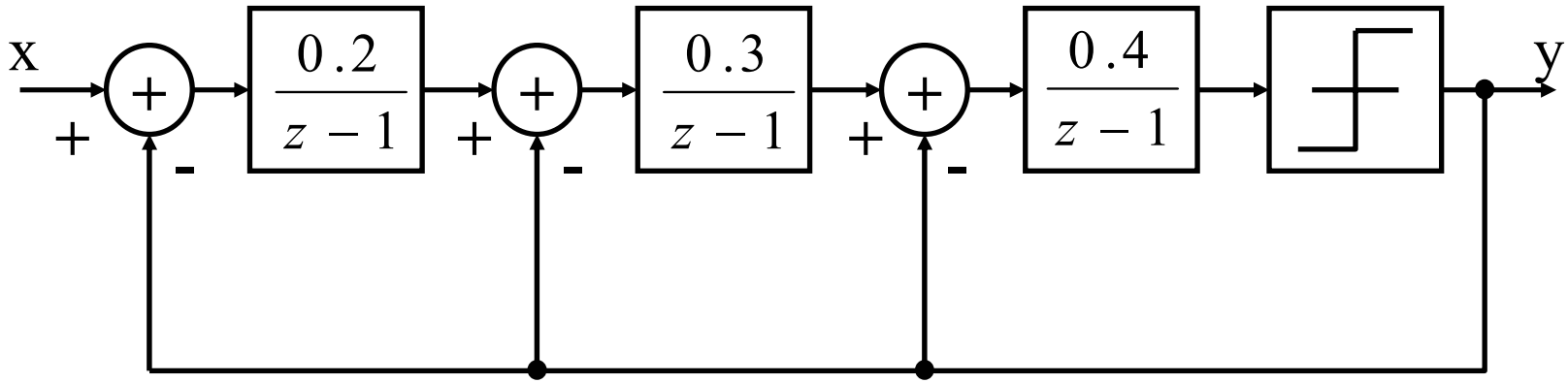
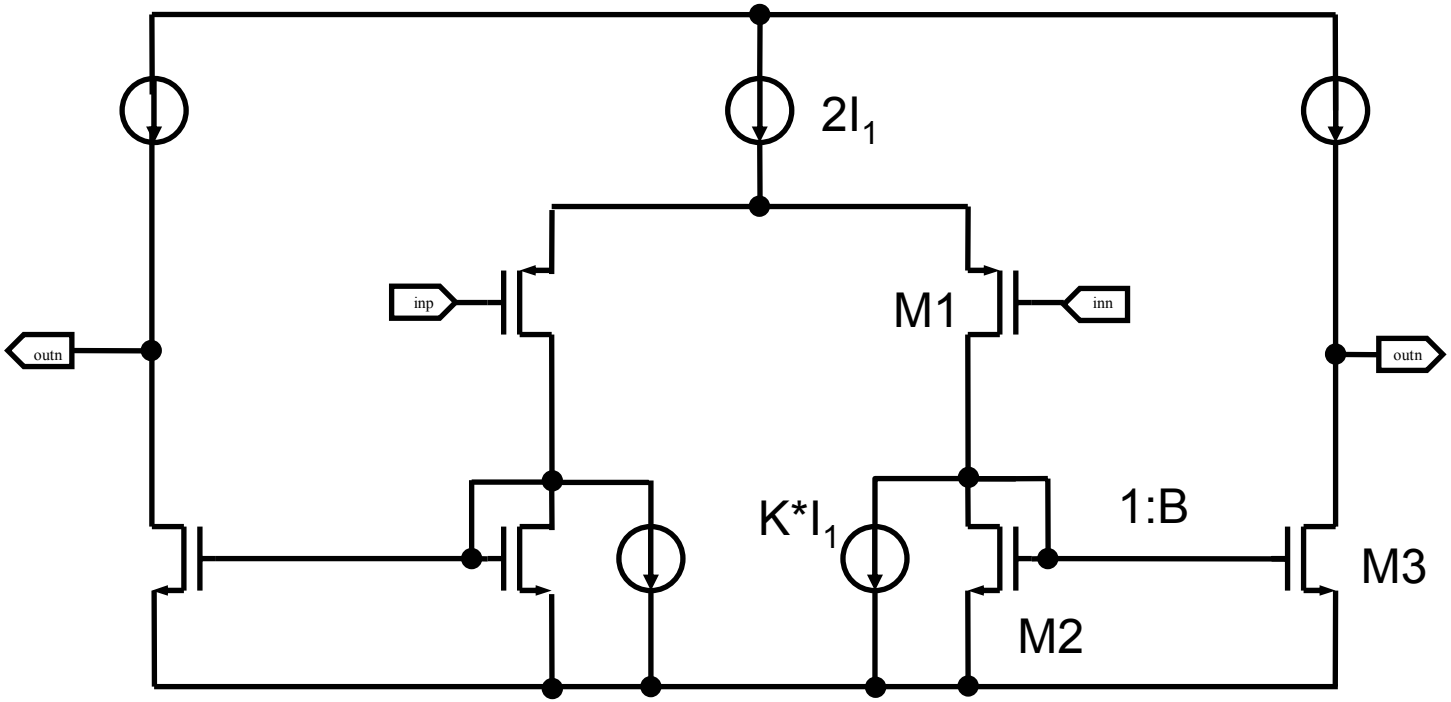
ΣΔ Modulator on 1 Volt in 90 nm CMOS



- **Single-loop third-order single-bit topology**
  - **Simple and robust**
  - **Tolerance to building block non-idealities**
- **Coefficients selected not sensitive to capacitance mismatches**

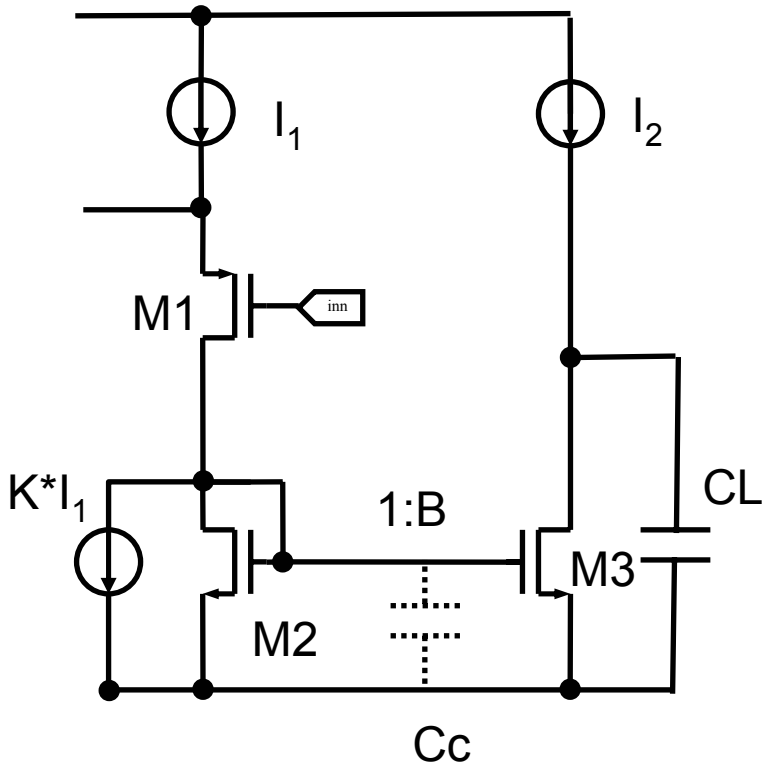
Yao, ..., JSSC Nov.04, 1809-1818
Yao. etal. "Low-Power Low-Voltage ΣΔ modulators in Nanometer CMOS", Springer '06

Gain enhancement



$$A = \frac{2}{(1-k)(V_{GS} - V_T)_1 \cdot \lambda_3} = \frac{A_0}{1-k}$$

Stability



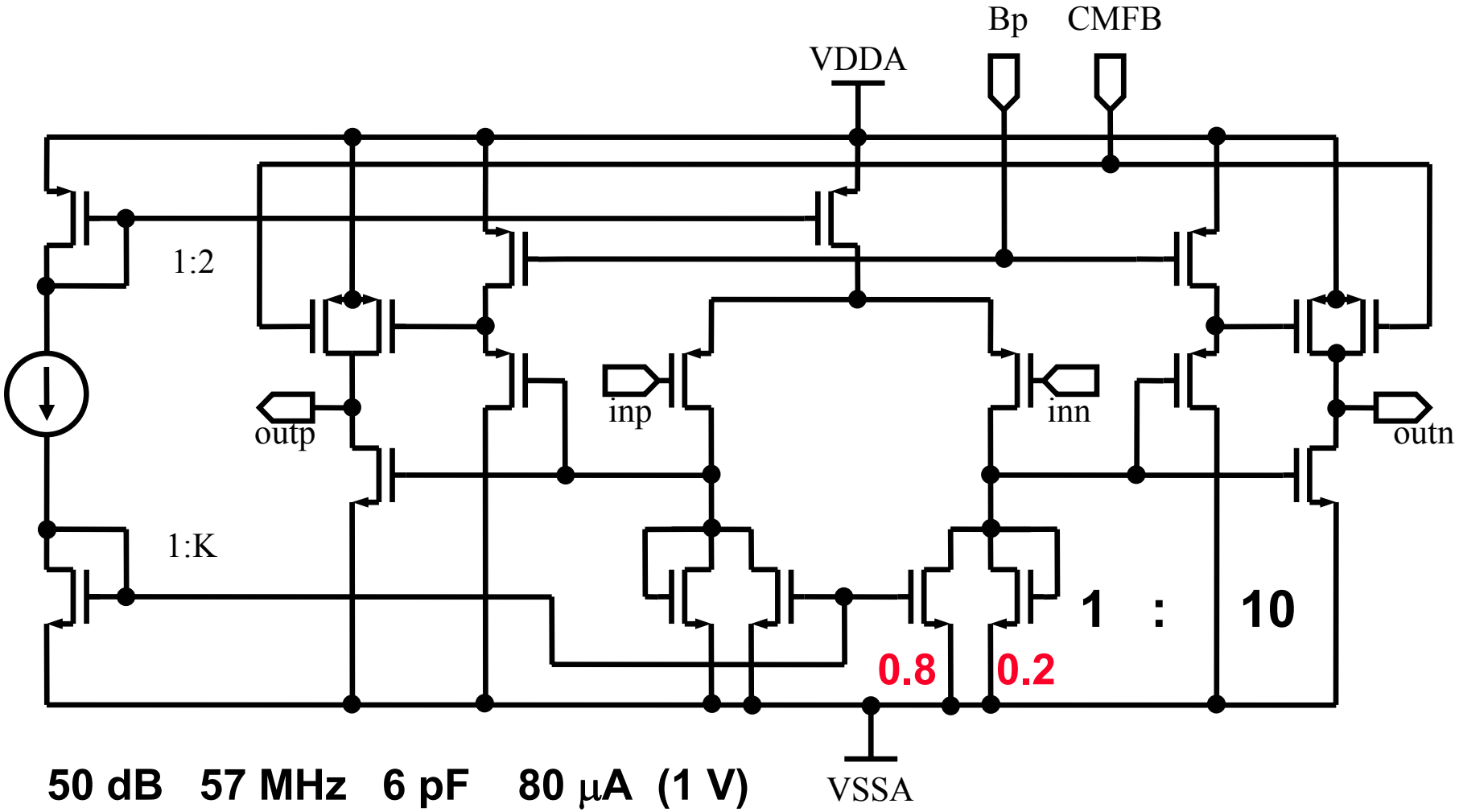
The non-dominate pole
must be > 3GBW
for sufficient phase margin

$$P_{nd} = \frac{gm_2}{2\pi \cdot C_c} = \frac{2(1-k)I_1}{2\pi \cdot C_c \cdot (V_{GS} - V_T)_2}$$

$$GBW = \frac{B \cdot gm_1}{2\pi \cdot C_L} = \frac{2B \cdot I_1}{2\pi \cdot C_L \cdot (V_{GS} - V_T)_1}$$

$$P_{nd} > 3GBW \Rightarrow k < 1 - 3B\frac{C_c}{C_L}$$

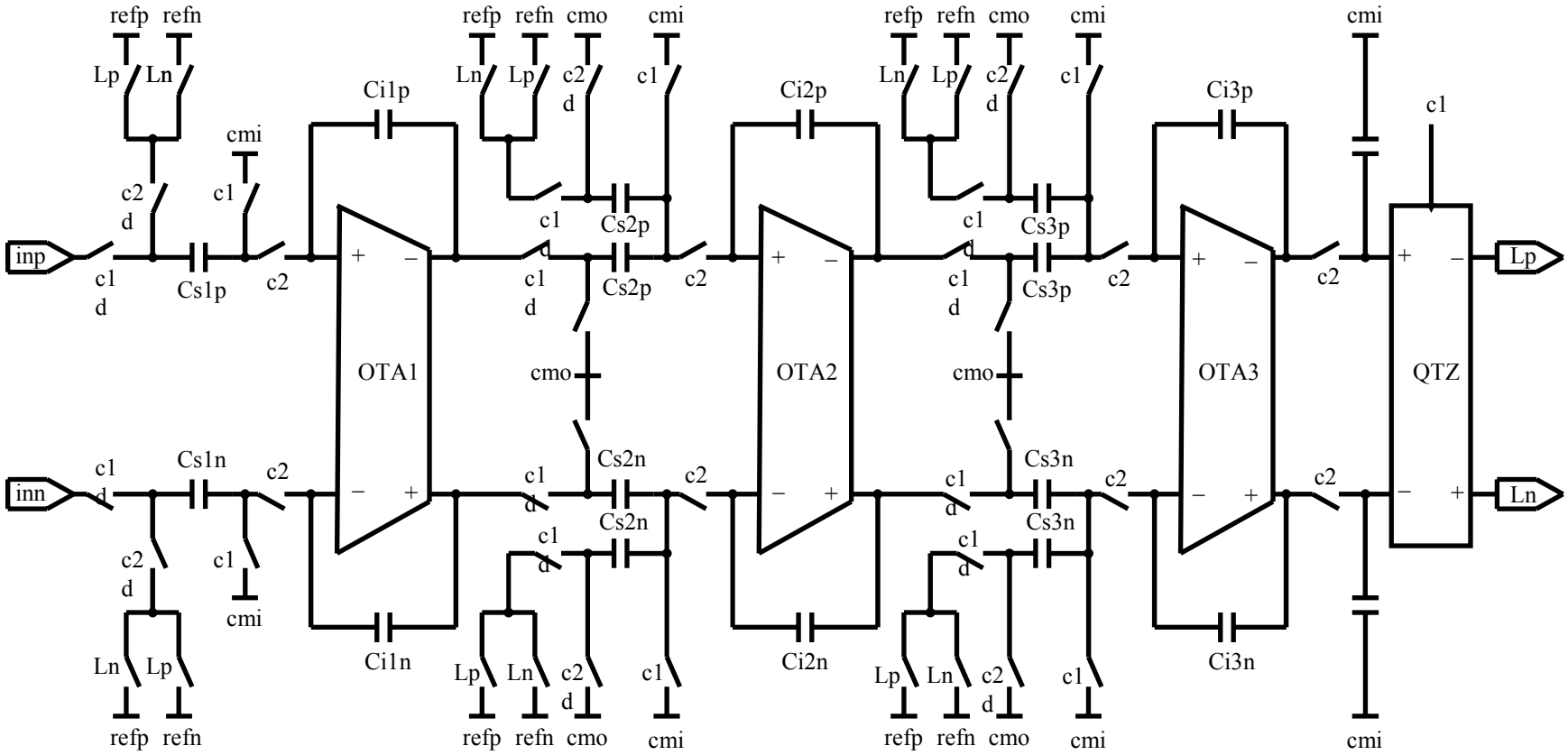
Full OTA circuit



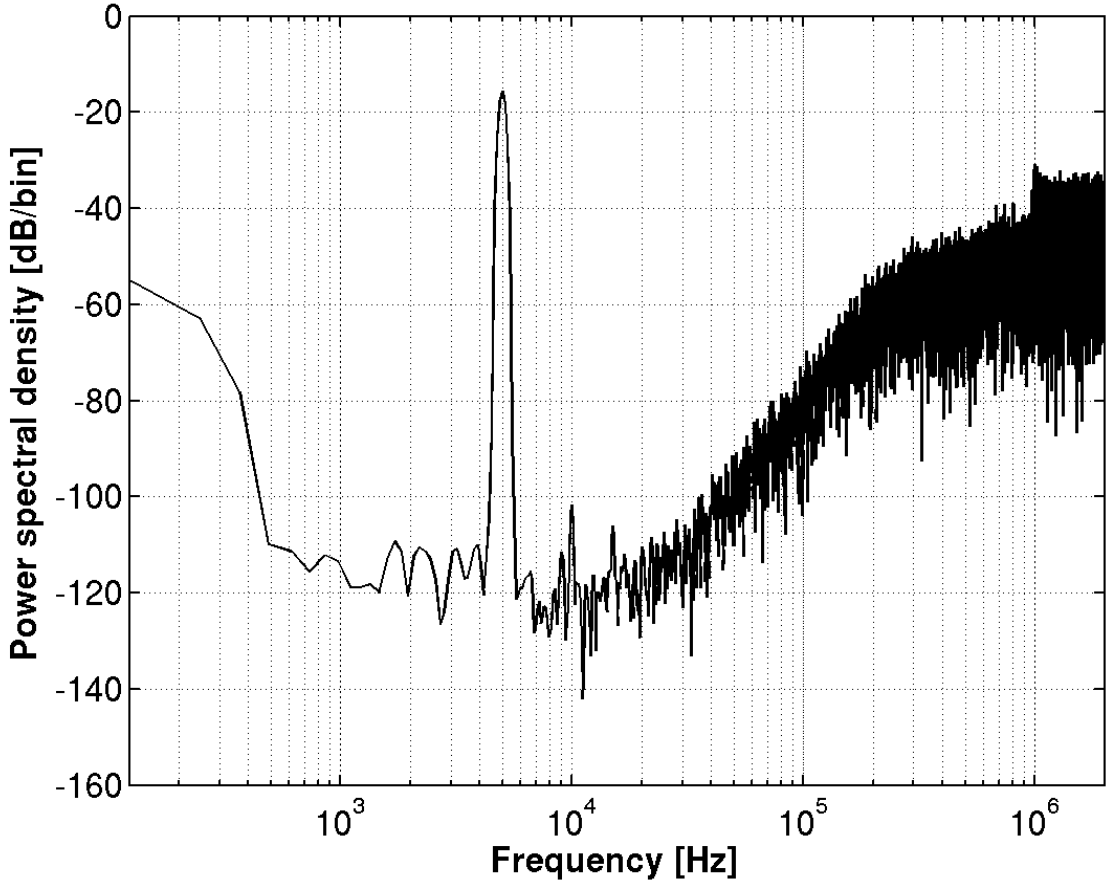
50 dB 57 MHz 6 pF 80 μA (1 V)

Yao, ..., JSSC Nov.04, 1809-1818

Full modulator circuits

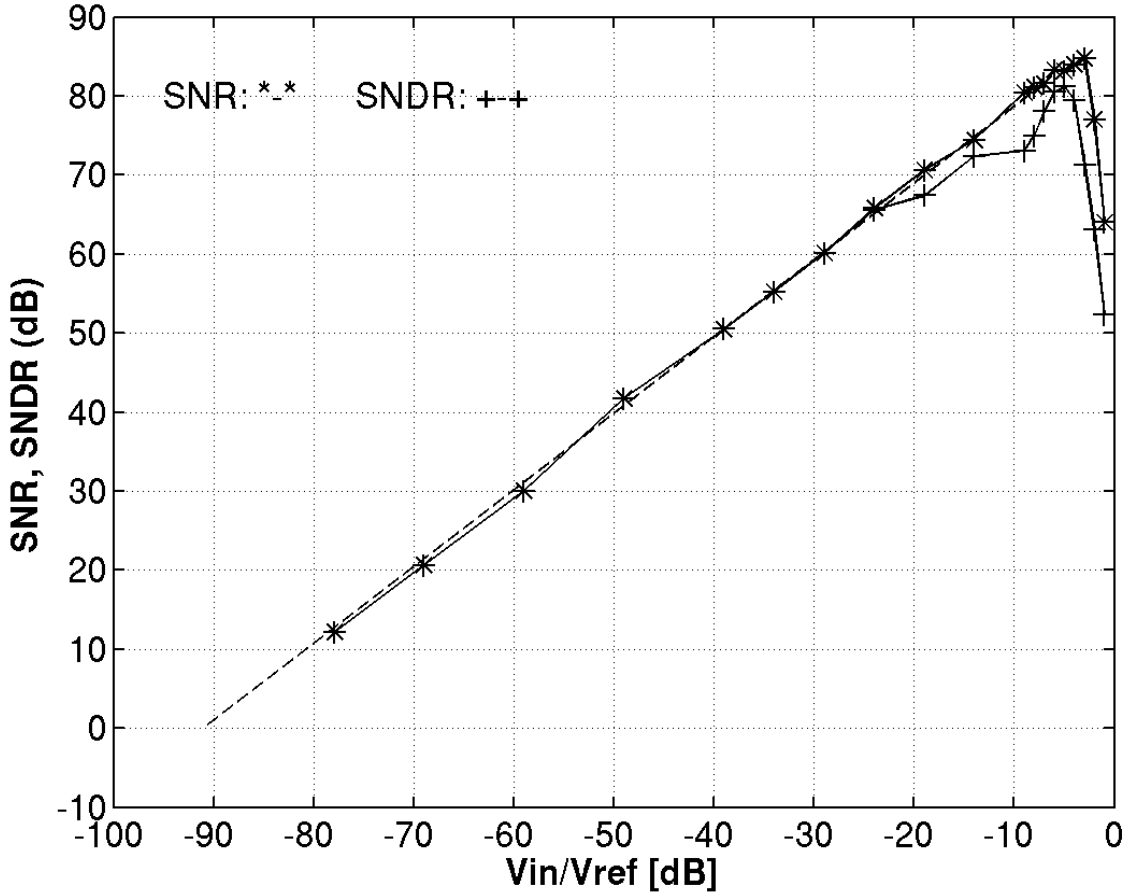


Measurement Output spectrum



Output spectrum of a 5 kHz input signal

Measured SNR and SNDR vs input amplitude



Yao, ..., JSSC Nov.04, 1809-1818

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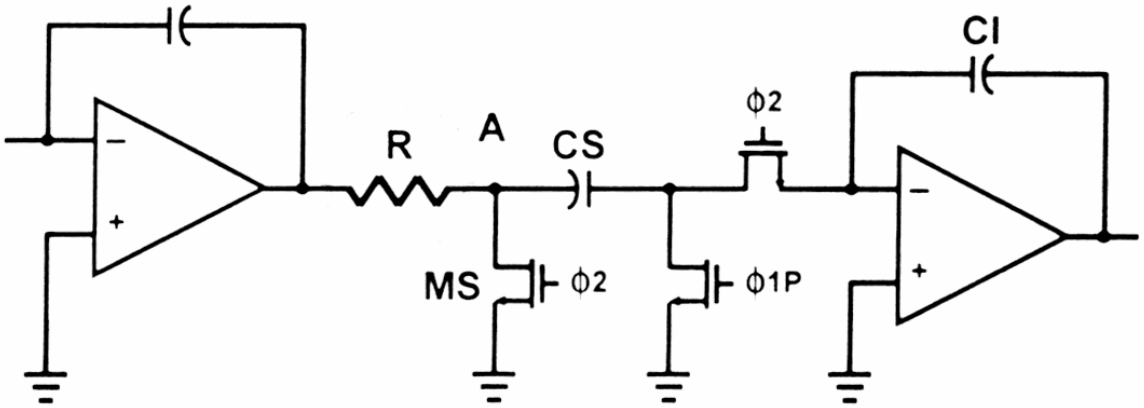
Switched-resistor integrator

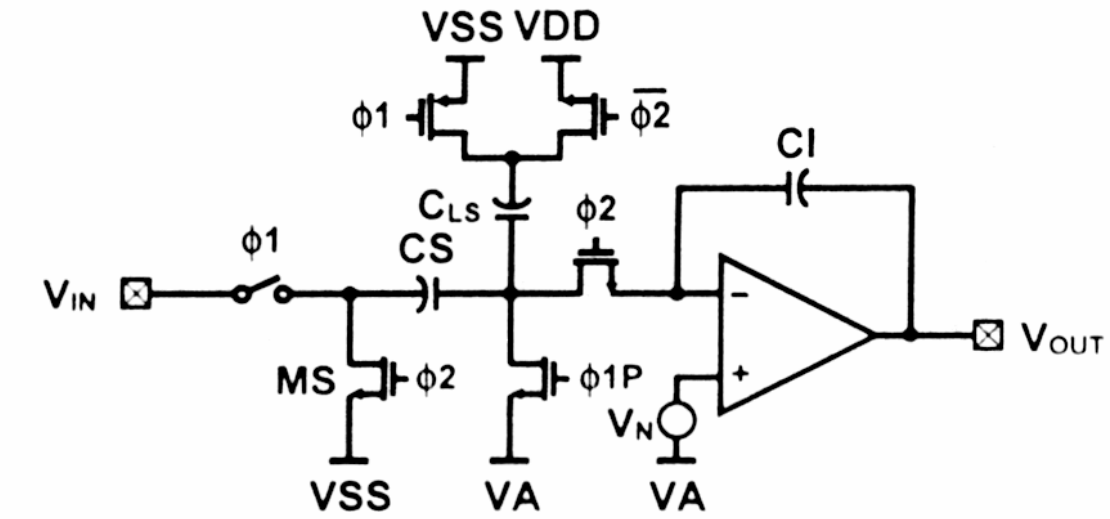


Input switch
replaced by resistor R

Larger resistor for better linearity
Smaller resistor for higher speed

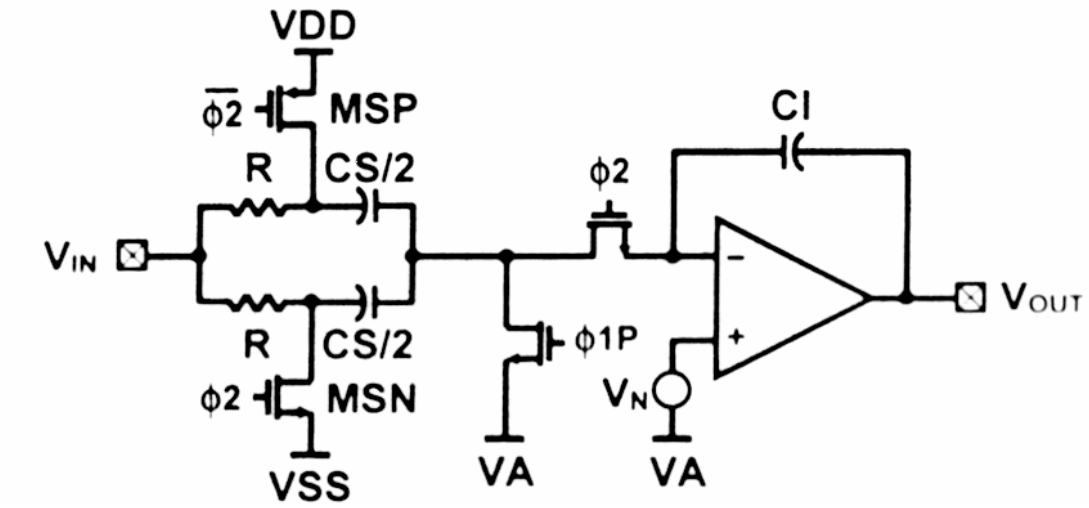
Ahn, .. ISSCC 05, 166-167

Input sampling : maintain constant V_{INCM}



C_{Ls} added

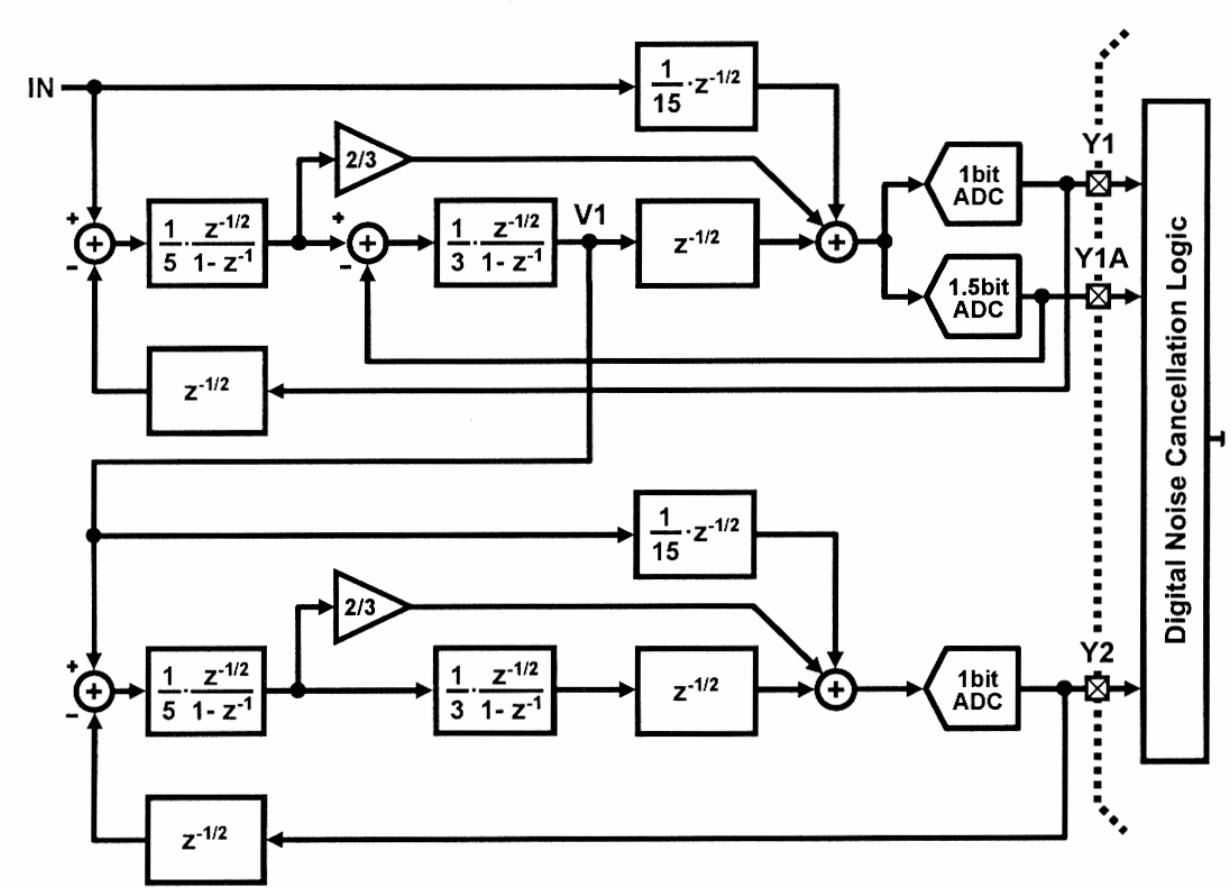
Baschirotto, JSSC
Dec.1997, 1979-1986



R & C_S doubled

Ahn, .. ISSCC 05, 166-167

Mash 2-2 ΣΔ Audio ADC



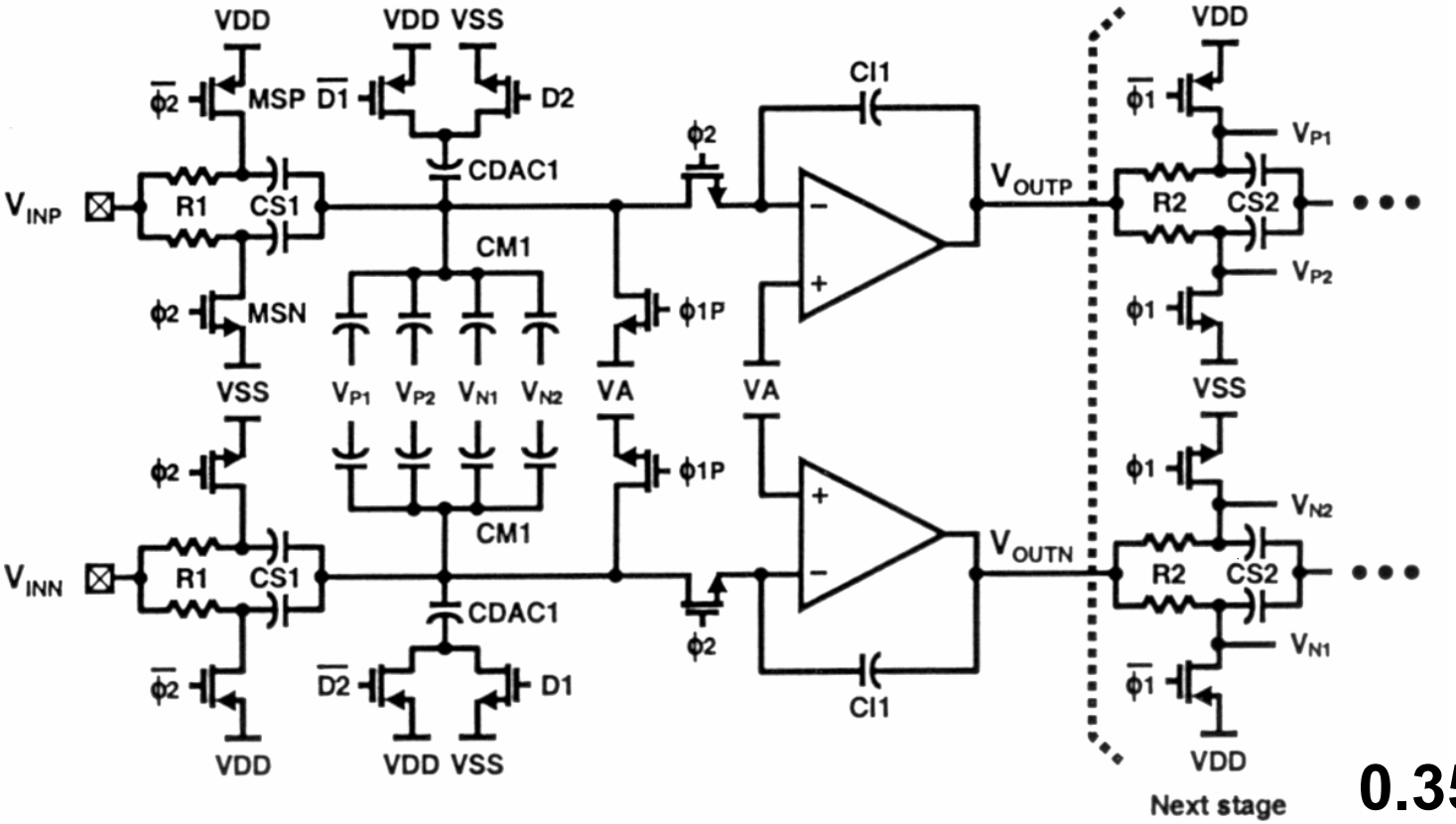
Low-distortion :
- **switched resistor**
- **loop filter processes only quantization error**

OSR = 64
25 kHz
3 MHz clock
SNDR = 78 dB

0.35 μm CMOS
0.6 V
1 mW

Ahn, .. ISSCC 05, 166-167
Silva, Electronic Letters, June 01, 737-738

4-th order ΣΔ converter with switched-resistors

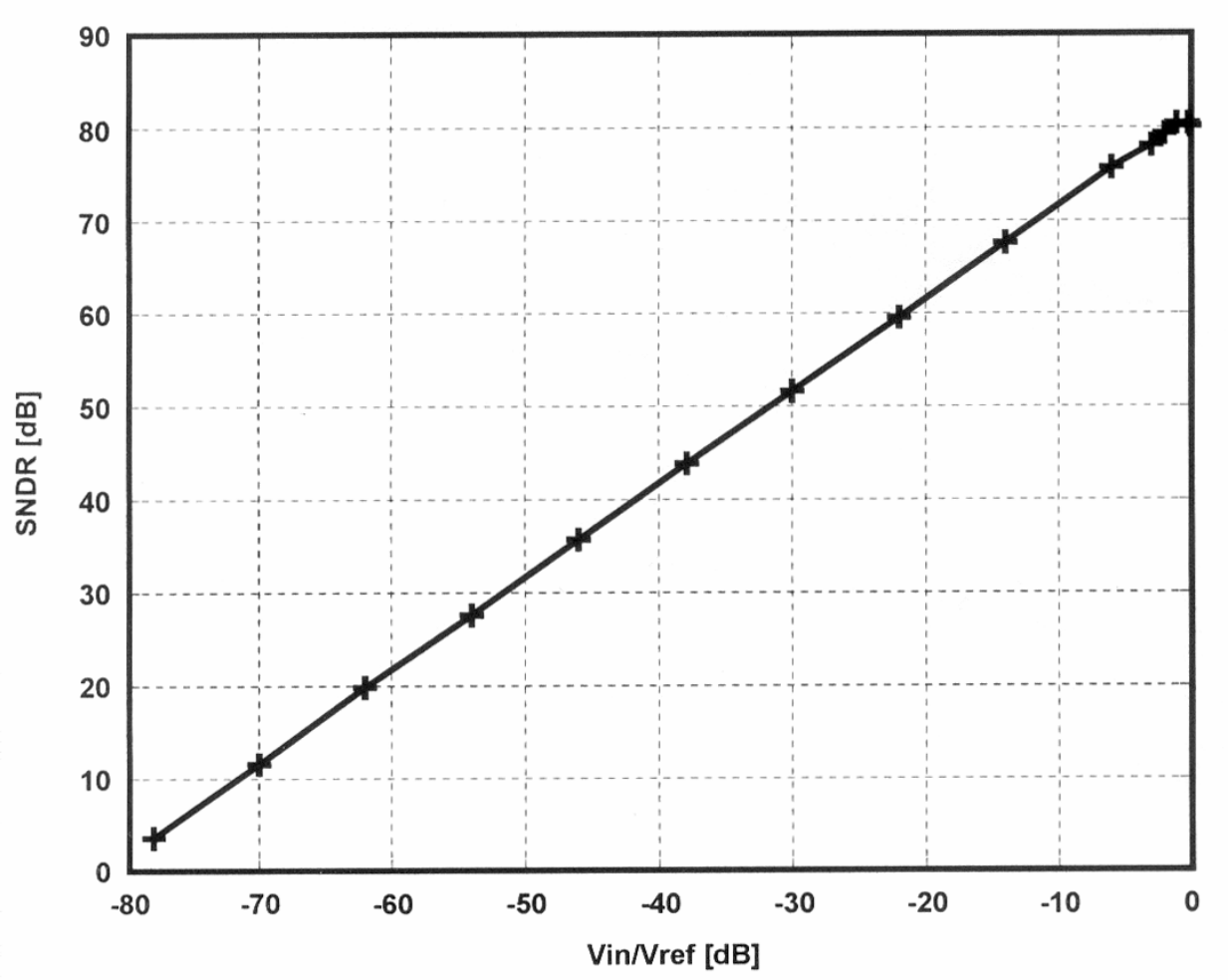


0.35 μm CMOS

Mash 2-2 Two-stage opamp with folded cascode

OSR = 64 0.6 V 1 mW 24 kHz BW

Measured SNDR



Low-distortion :
Vref = 0.6 V

SNR ≈ SNDR
= 78 dB
at 1 kHz

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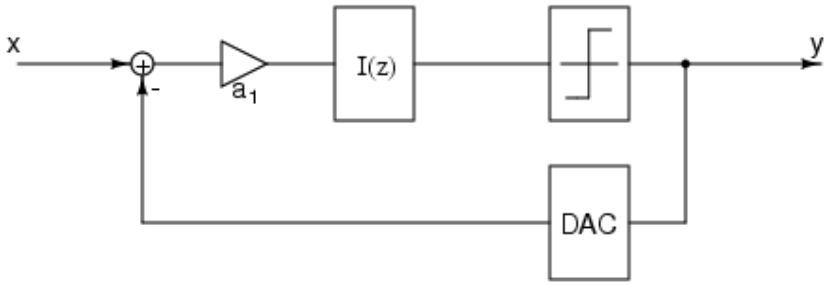
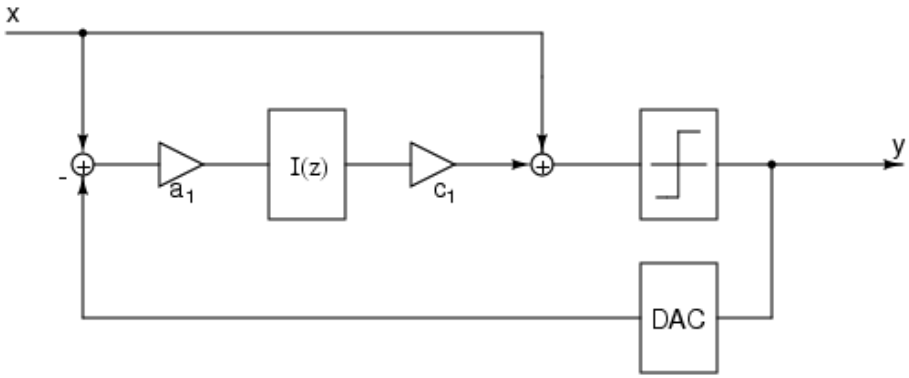
Full Feedforward Topology





Convent. Sigma-Delta topology

$$H_x(z) = \frac{a_1 I}{1 + a_1 I}$$

$$H_e(z) = \frac{1}{1 + a_1 I}$$

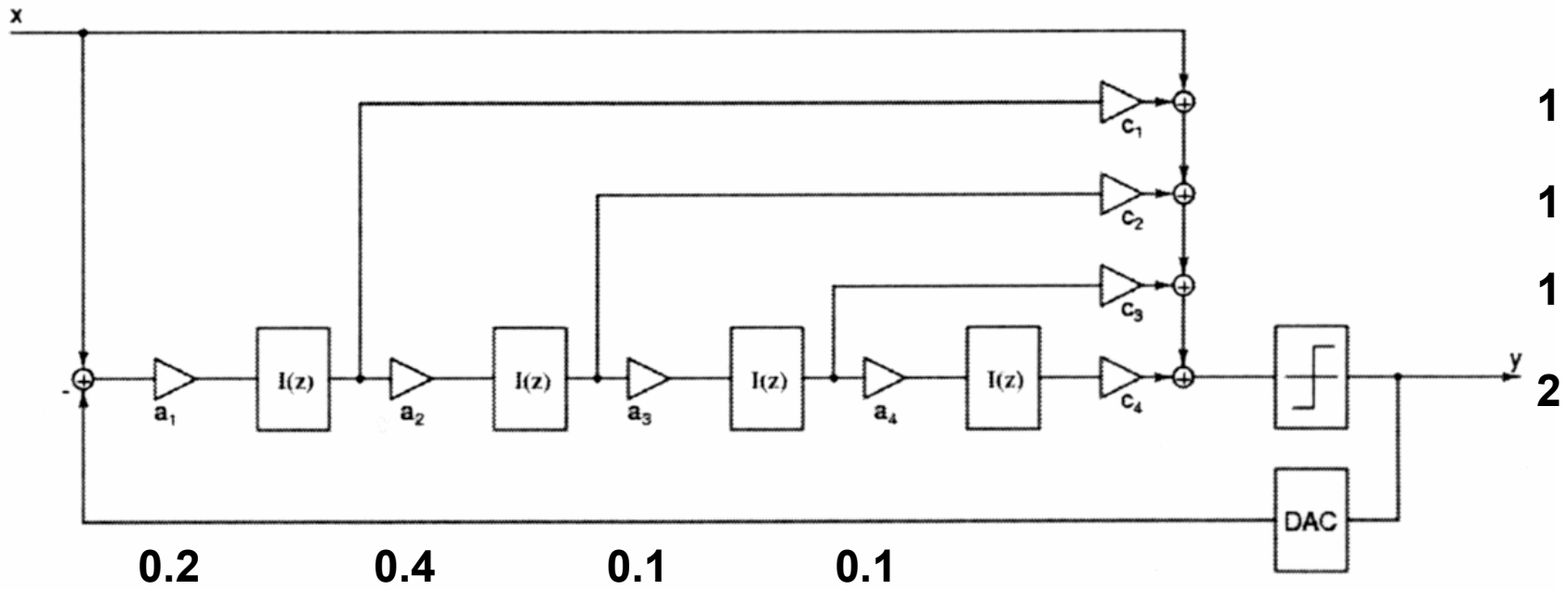
Full feedforward topology

$$H_x(z) = 1$$

$$H_e(z) = \frac{1}{1 + a_1 c_1 I}$$

Silva, Electronic Letters, June 01, 737-738

4th-Order single-bit 1 Ms/s ΣΔ modulator



Single feedback loop : processes quantization noise only

Full feedforward : unity-gain transfer

4th order - single bit

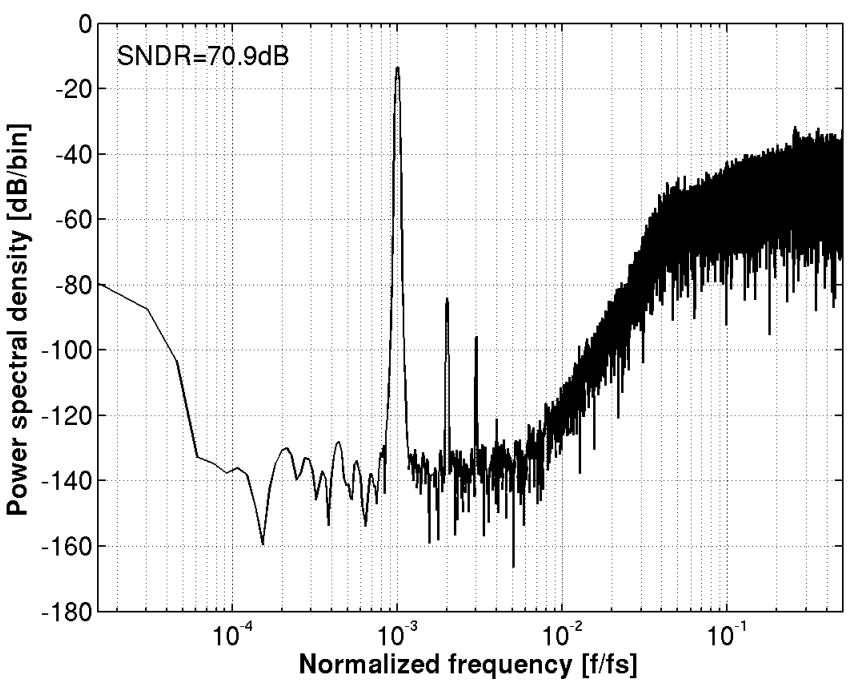
Optimization coefficients or equal swing

Yao, .., VLSI Circuits '05
Yao. etal. "Low-Power Low-Voltage ΣΔ modulators in Nanometer CMOS", Springer '06

Performance comparison

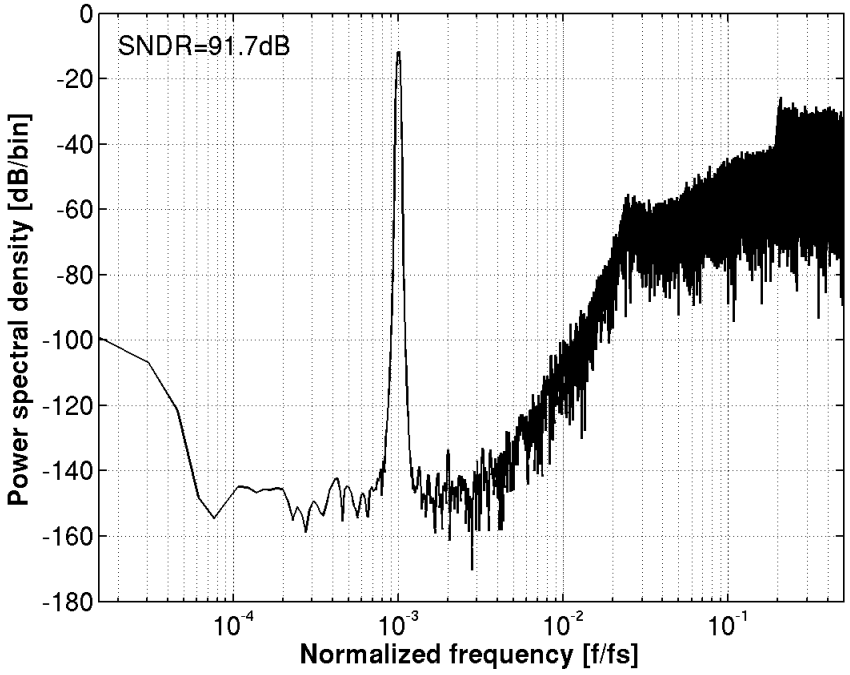
- 4th-order conventional topology
- Behavioral simulation with:

  a_1=-0.1, a_2=-0.1, A_0=40 dB

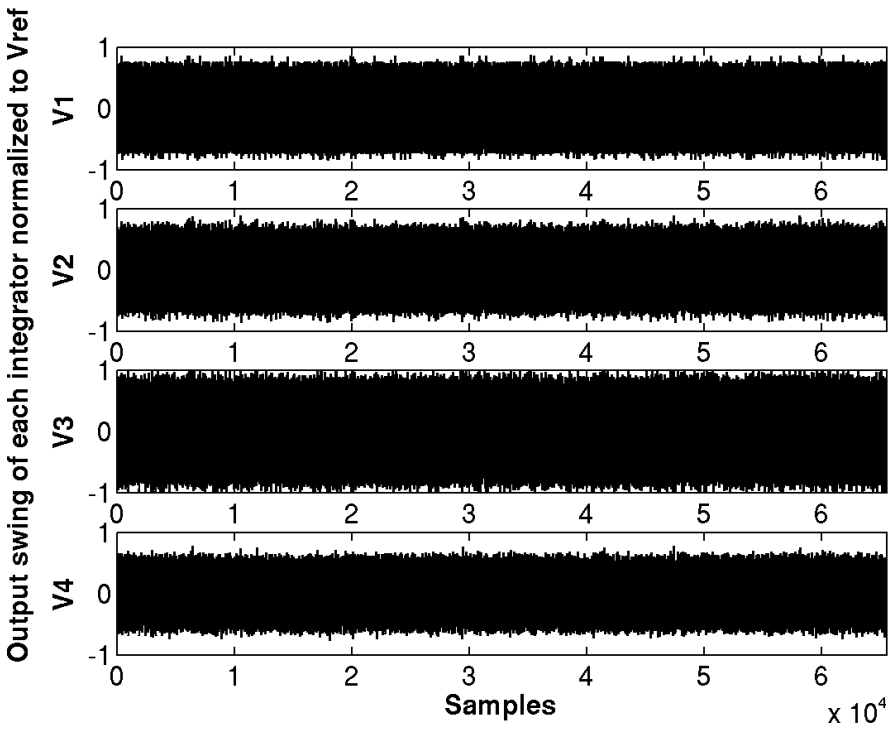


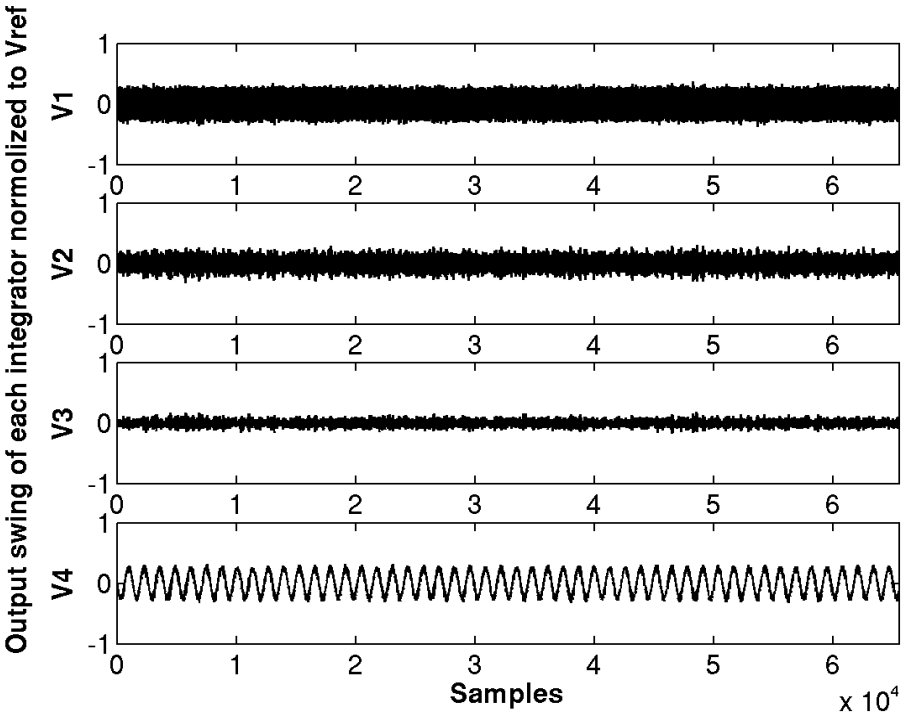
- 4th-order full feedforward topology
- Behavioral simulation with:

  a_1=-0.1, a_2=-0.1, A_0=40 dB



Output swing of integrators

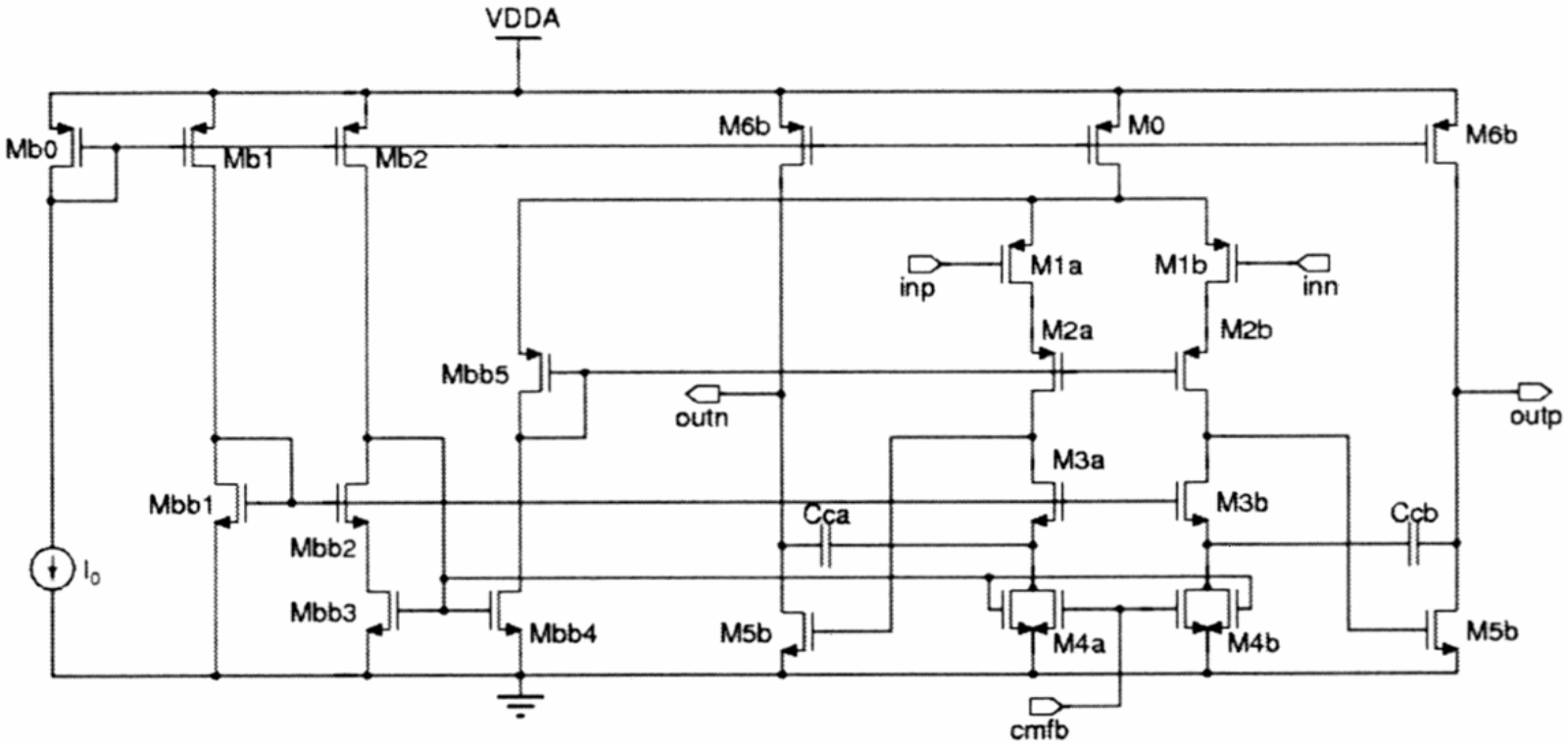




Output swings of each integrator in the conventional topology

Output swings of each integrator in the full-feedforward topology

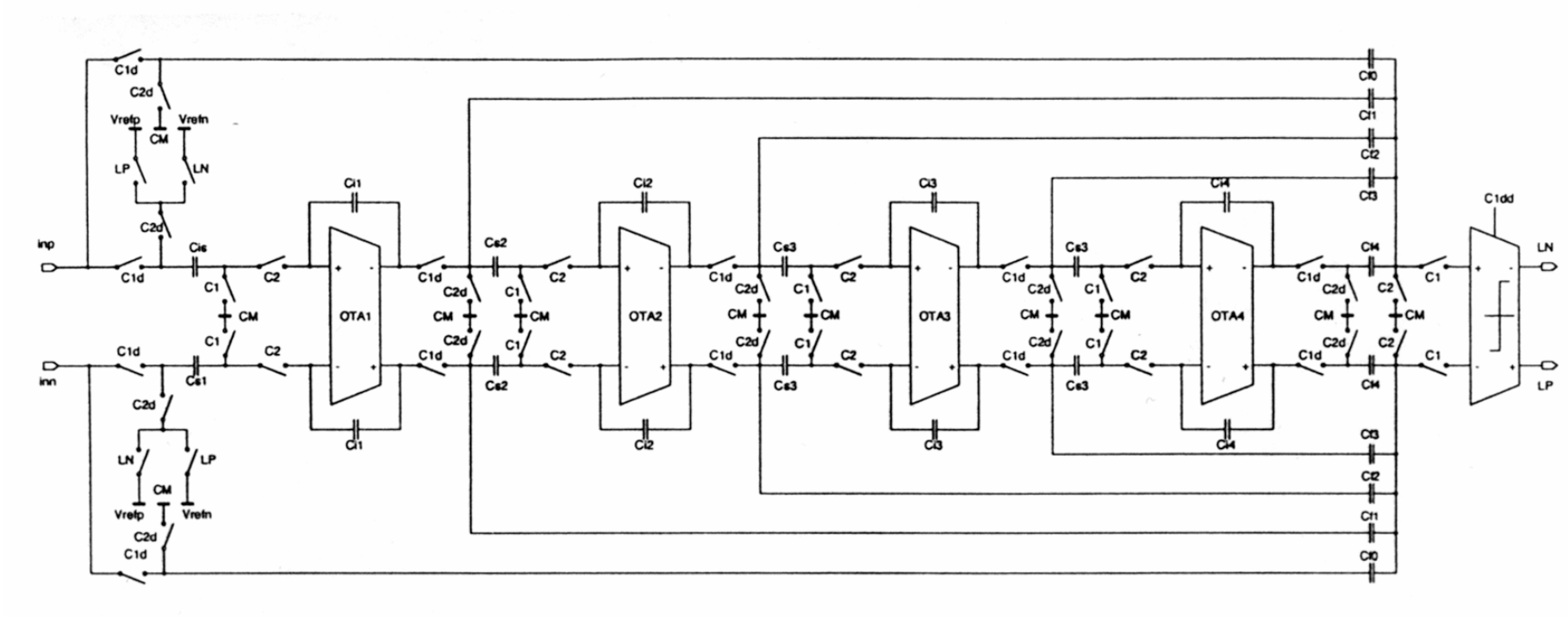
Single-stage OTA for fast settling (0.13 μm)



Yao, .., VLSI Circ.05

Yao. etal. "Low-Power Low-Voltage ΣΔ modulators in Nanometer CMOS", Springer '06

Circuit Realization



OSR = 64

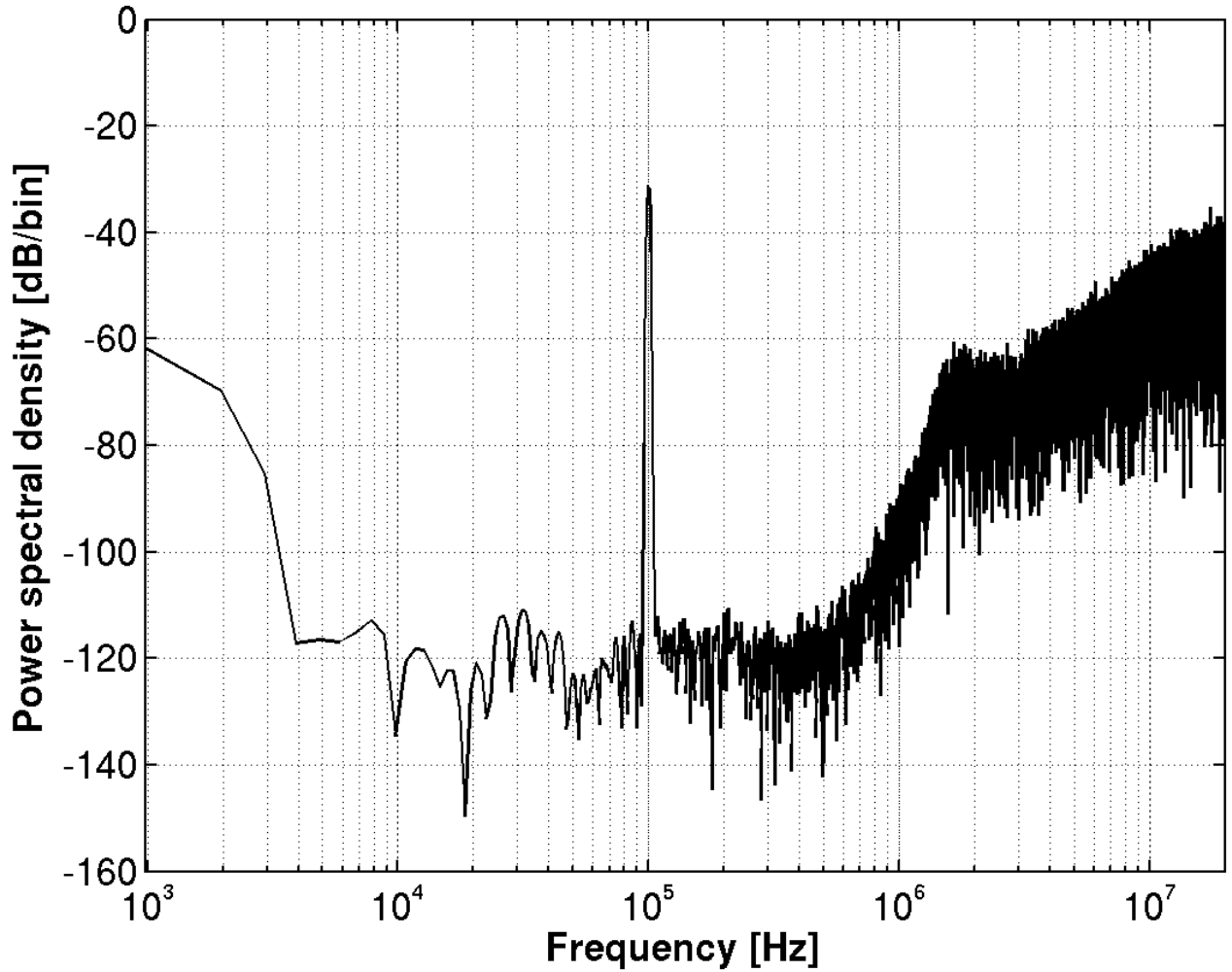
Clock of 64 MHz

1 V 6.1 mA + 1.3 mA

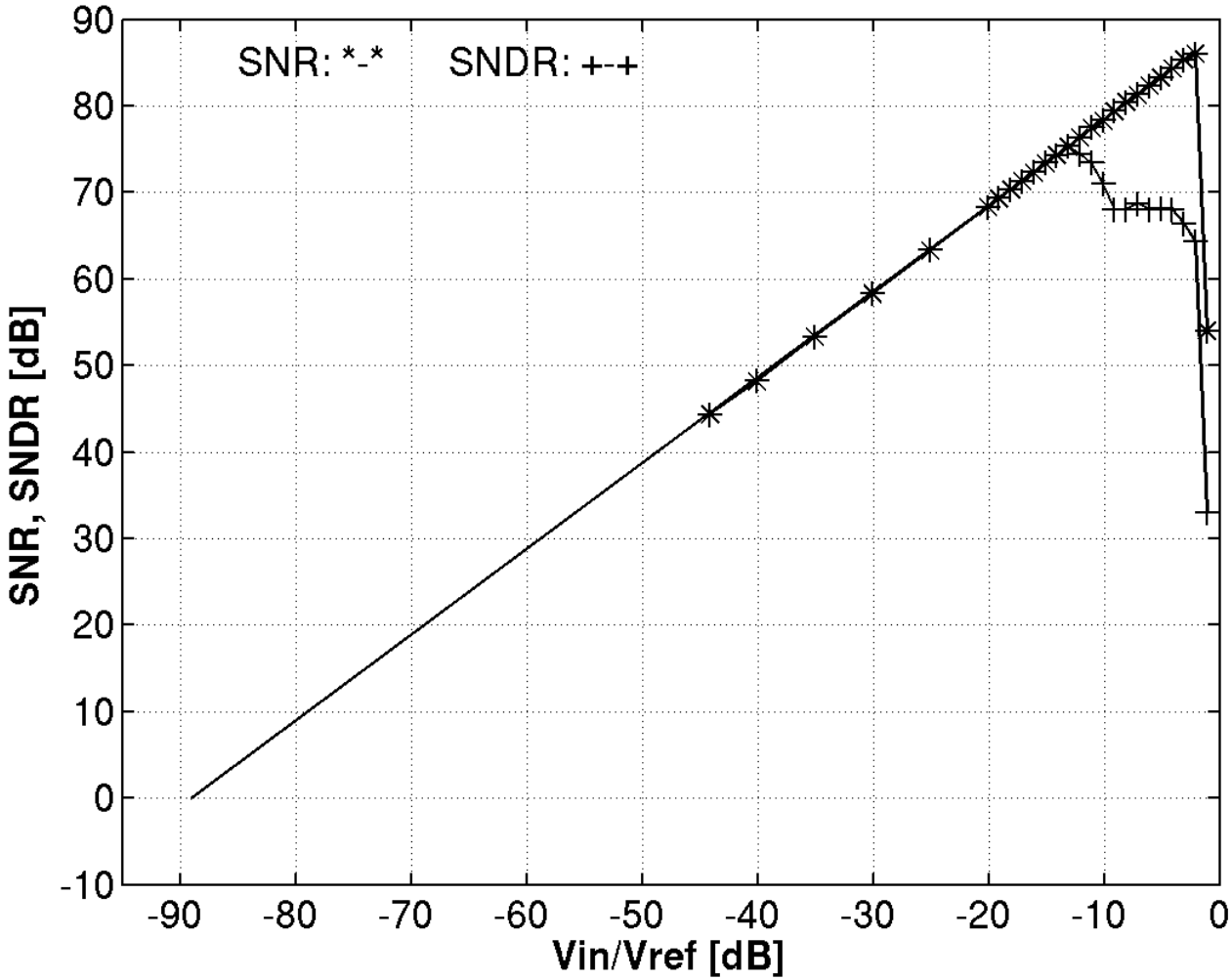
Yao, .., VLSI Circuits, '05

Yao. etal. "Low-Power Low-Voltage ΣΔ modulators in Nanometer CMOS", Springer '06

Measured output spectrum



Measured SNR versus Input voltage

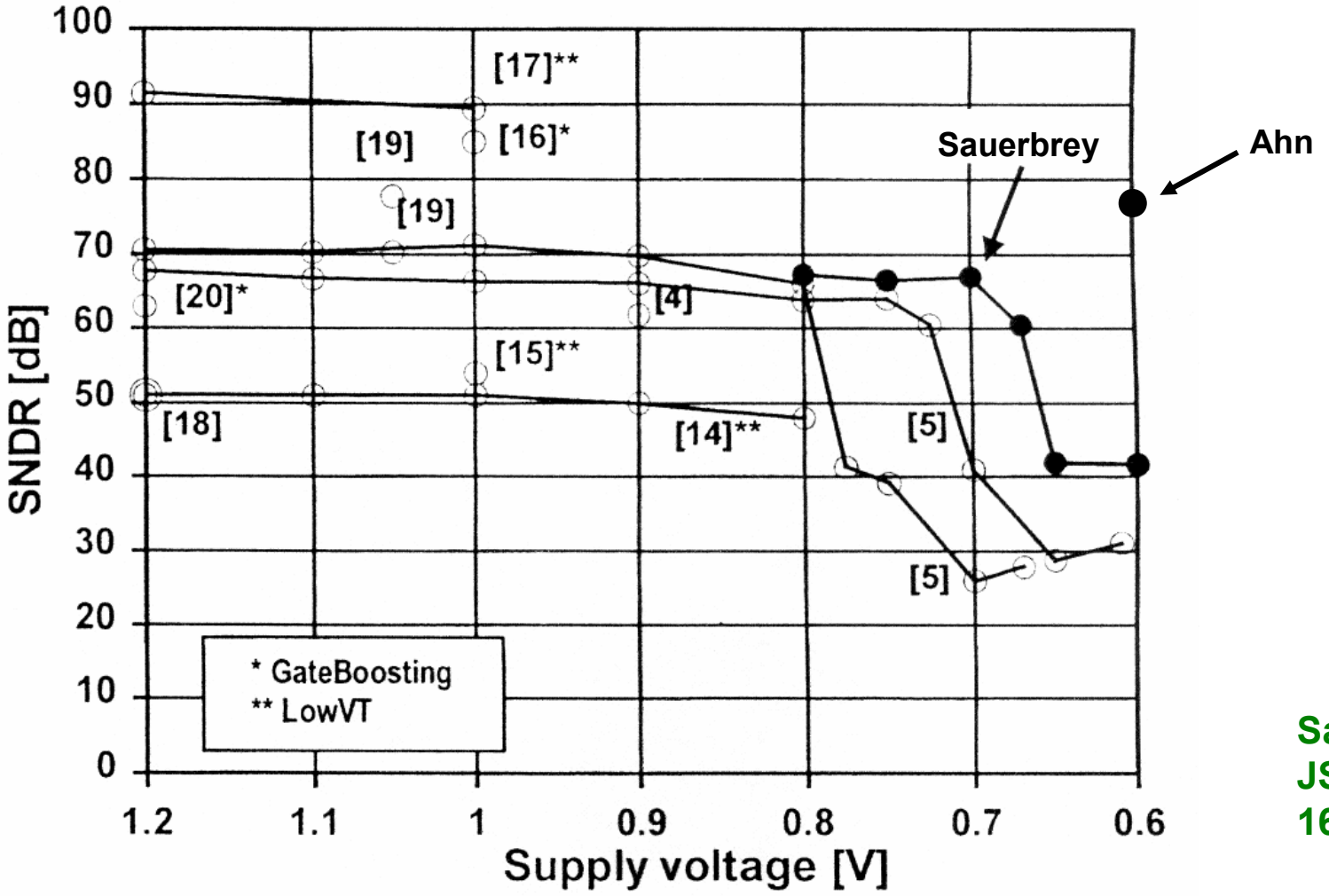


Comparison of Low-power ΣΔ converters

Ref.	Type	V_{DD} V	DR dB	BW kHz	P μW	FOM x 10^{-6}
Ahn 05	SwR	0.6	78	24	1000	20
Sauerbrey 02	SO,LV	0.7	75	8	80	53
Peluso 98	SO	0.9	77	16	40	330
Dessouky 01	LV	1	88	25	950	275
Keskin 02	ResetOp.	1	74	20	5600	6
Yao 04	LV	1	88	20	140	1490
Rabii 96	SC, VM	1.8	92	25	5400	121
Yin 94	211	5	97	750	180k	346
Geerts 00	211	5	92	1100	200k	144
Vleugels 01	221	2.5	95	2000	150k	700
Gaggl 04	4	1.5	88	300	8k	400
Yao 05	4	1	88	500	7.4k	706
Doerrer 05	Track	1.5	74	2000	3k	280
Hezar 05	5	1.3	86	600	5.4k	737

FOM = 4kT DR BW / P

Low-voltage low-VT comparison



Sauerbrey, .., JSSC Dec.02 1662-1669

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