Rail-to-rail input and output amplifiers

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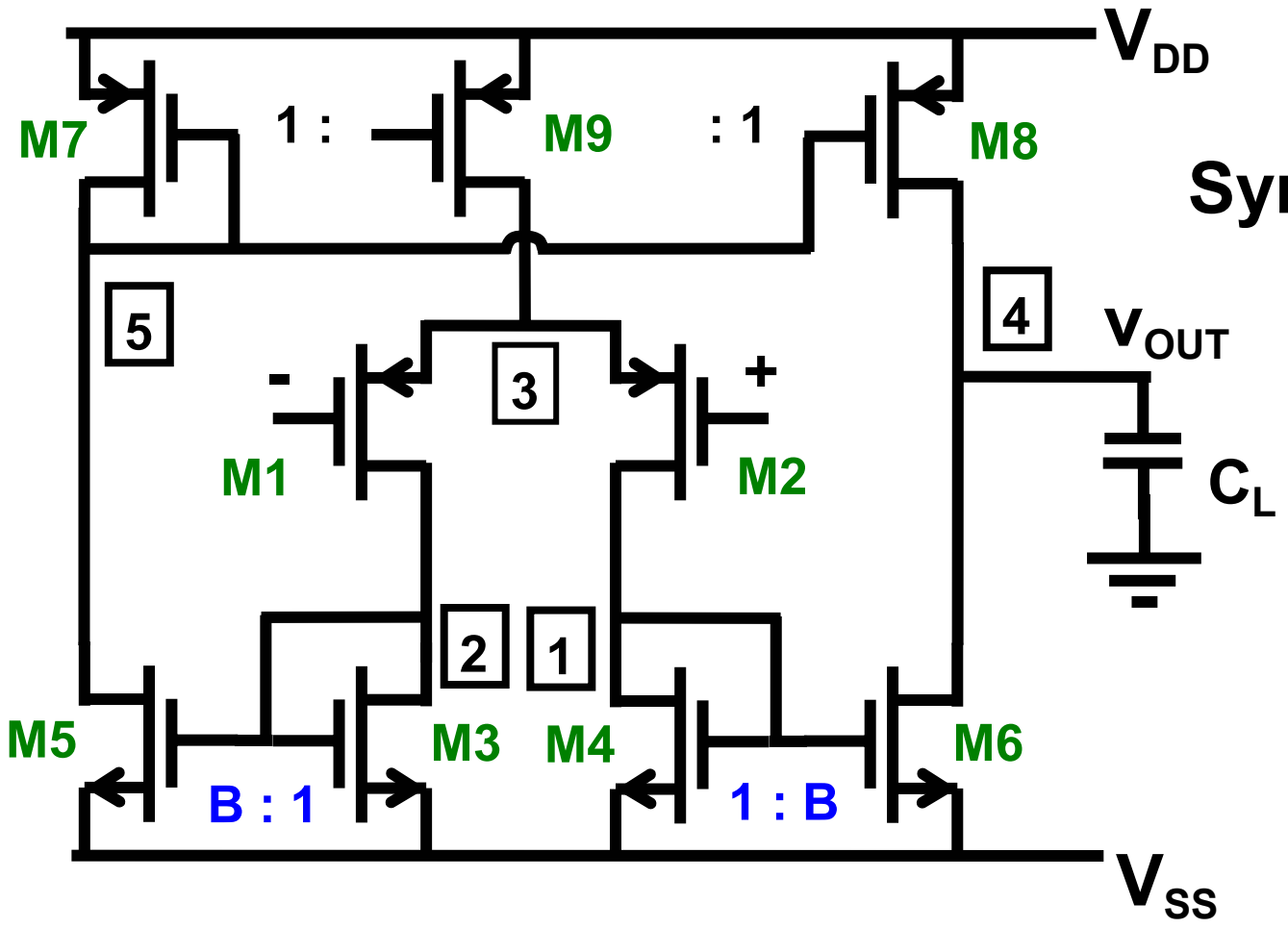
Table of contents

Why rail-to-rail amplifiers ?

- For low supply voltages : use full range for maximum dynamic range
- Fully differential signal processing
- Rail-to-rail output is always required
- But not necessarily rail-to-rail-input !

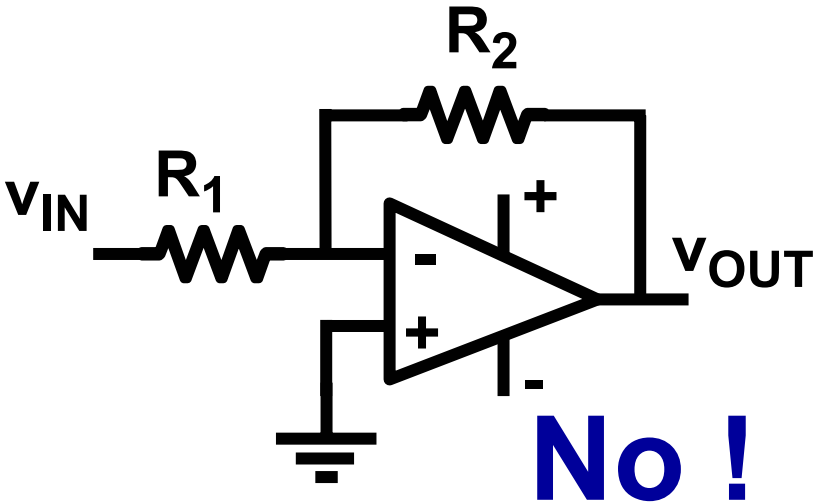
Symmetrical CMOS OTA

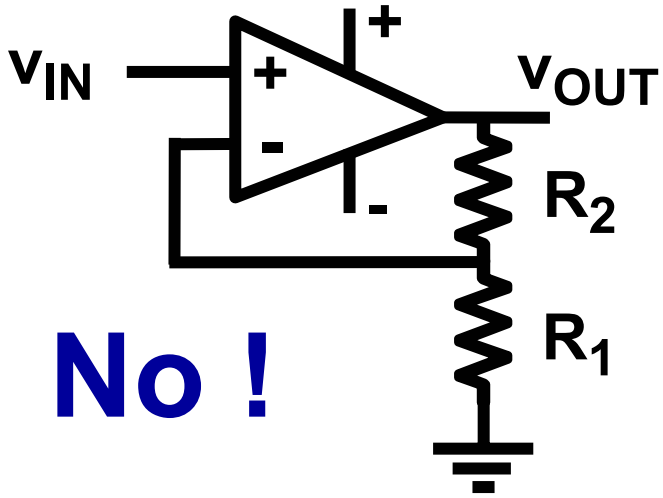


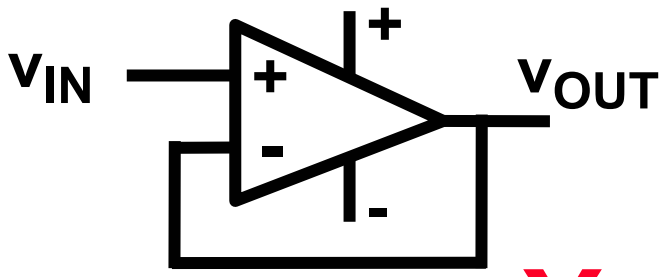
Symmetrical OTA

Rail-to-rail output swing !

When rail-to-rail input ?

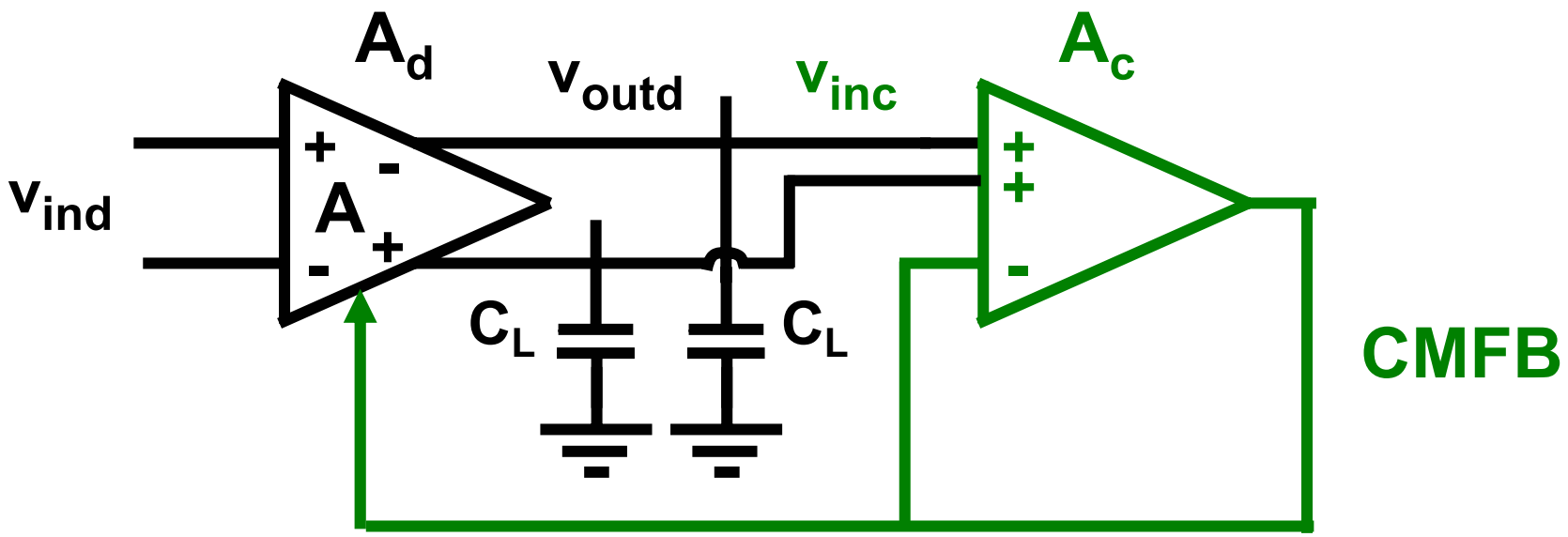






Yes !

Rail-to-rail input for CMFB

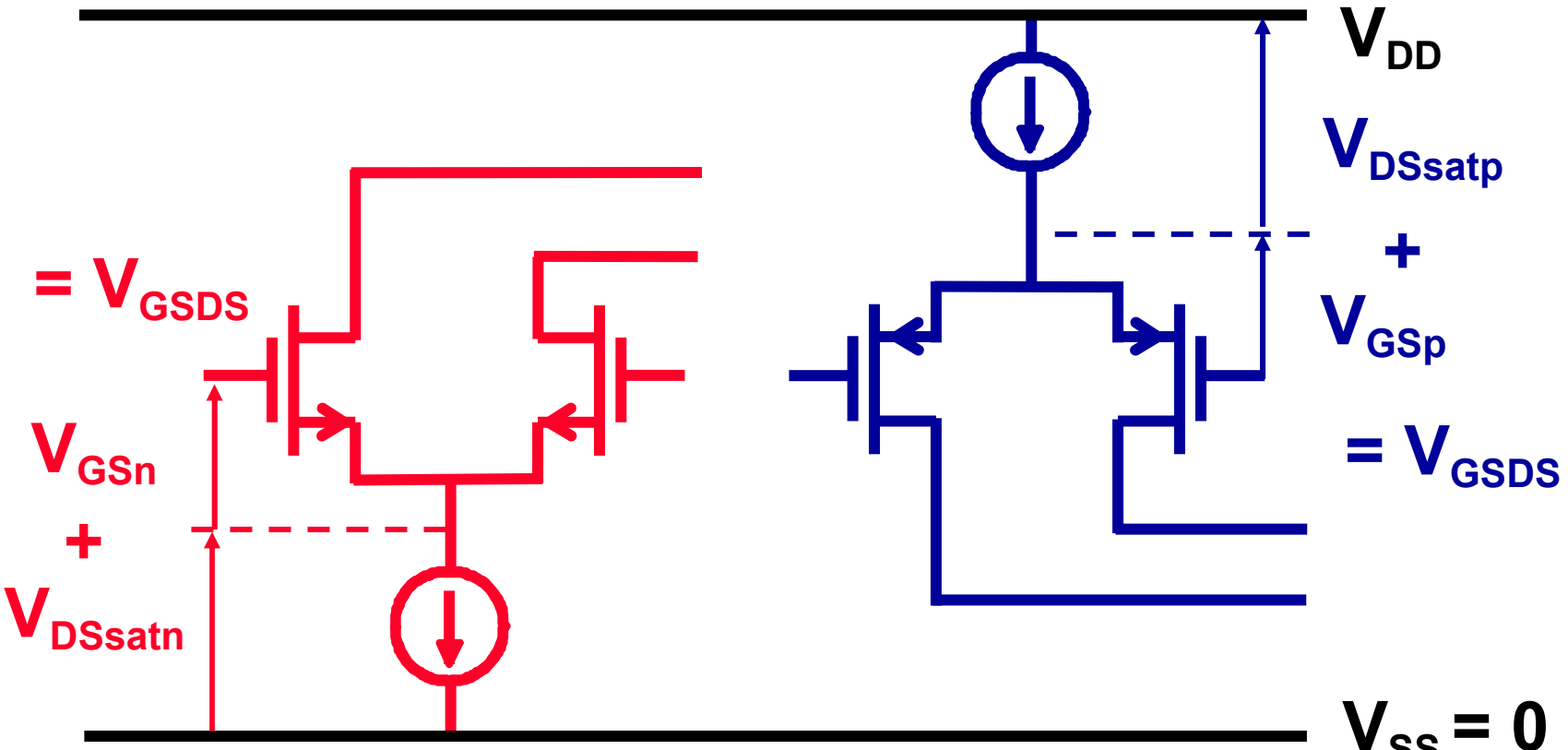


For a rail-to-rail output swing in fully-differential amplifiers
A CMFB amplifier is required
With rail-to-rail input capability !

Table of contents

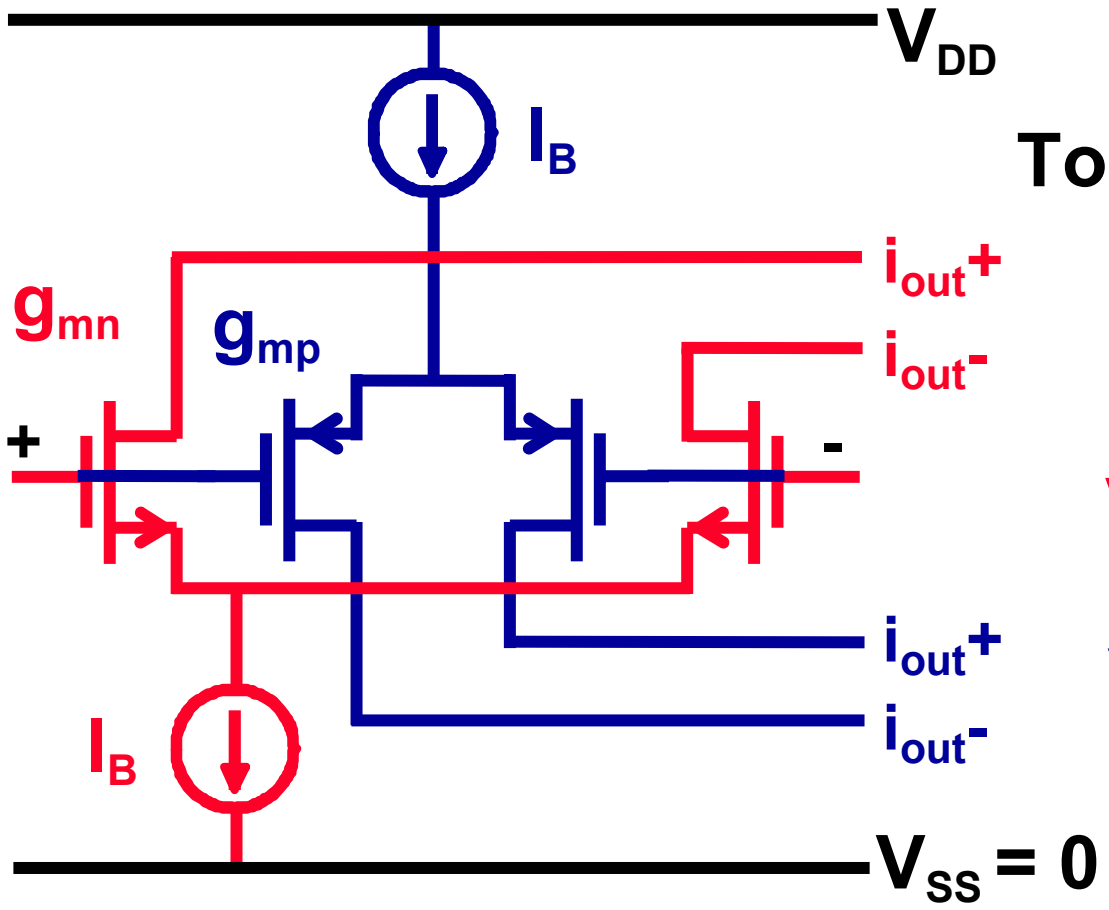
Problem ?

$V_{GS} \approx 0.9\ V$ & $V_{DSsat} \approx 0.2\ V$ >>> $V_{GSDS} = 1.1\ V$



$V_{INCM} > 1.1\ V$ $V_{INCM} < V_{DD} - 1.1\ V$

Problem : limited input CM range



To be operational :

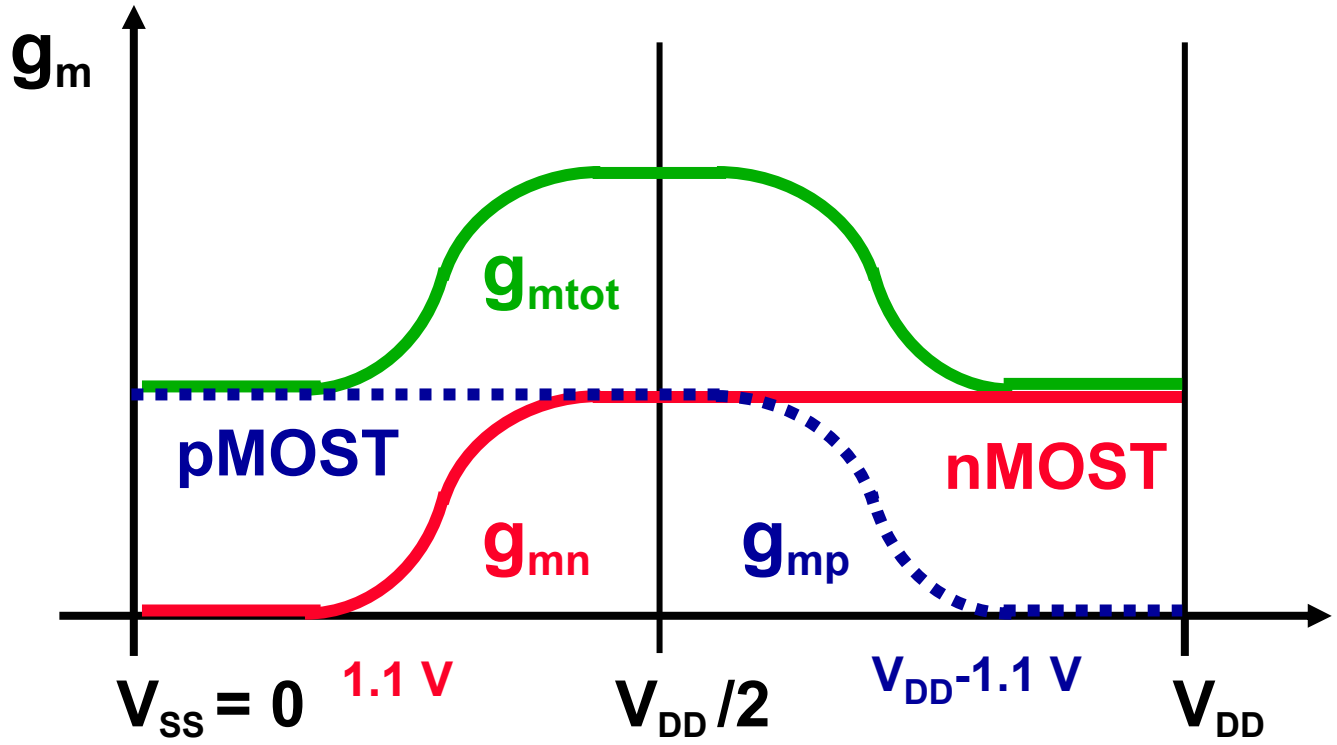
$V_{INCM} > 1.1\ V$

$V_{INCM} < V_{DD} - 1.1\ V$

$V_{DDmin} = 2.2\ V$

□

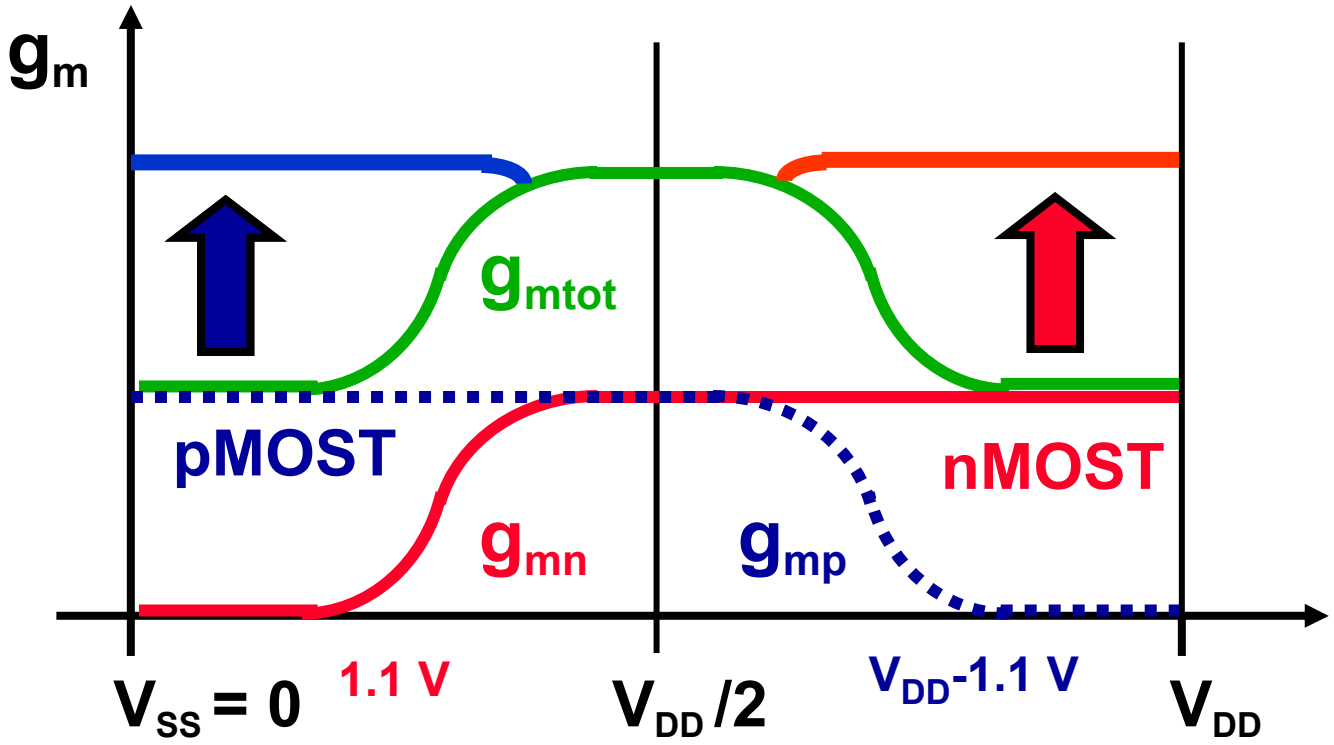
Problem: unequal g_{mtot}



nMOST on : $V_{INCM} > 1.1$ V

pMOST on : $V_{INCM} < V_{DD} - 1.1$ V

Solution : g_m equalization



nMOST on : $V_{INCM} > 1.1$ V

pMOST on : $V_{INCM} < V_{DD} - 1.1$ V

Increase g_m:

$g_{mn} + g_{mp} = ct$

Equalize g_{mtot} in strong inversion

$$g_{mn} + g_{mp} = ct1$$

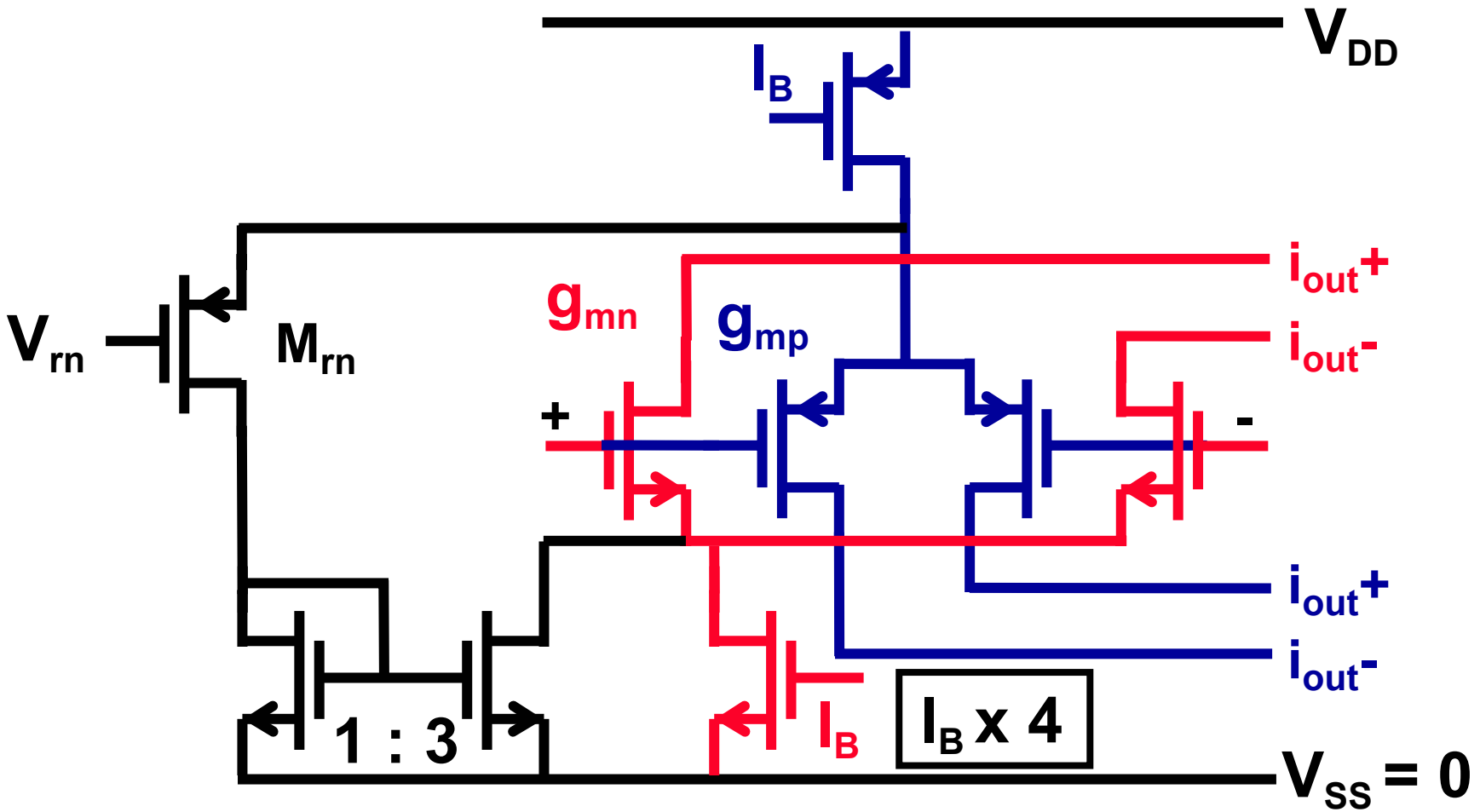
$$\sqrt{2\,K'_n \frac{W_n}{L_n} I_{Bn}} + \sqrt{2\,K'_p \frac{W_p}{L_p} I_{Bp}} = ct1$$

$$\sqrt{K'_n\, I_{Bn}} + \sqrt{K'_p\, I_{Bp}} = ct2$$

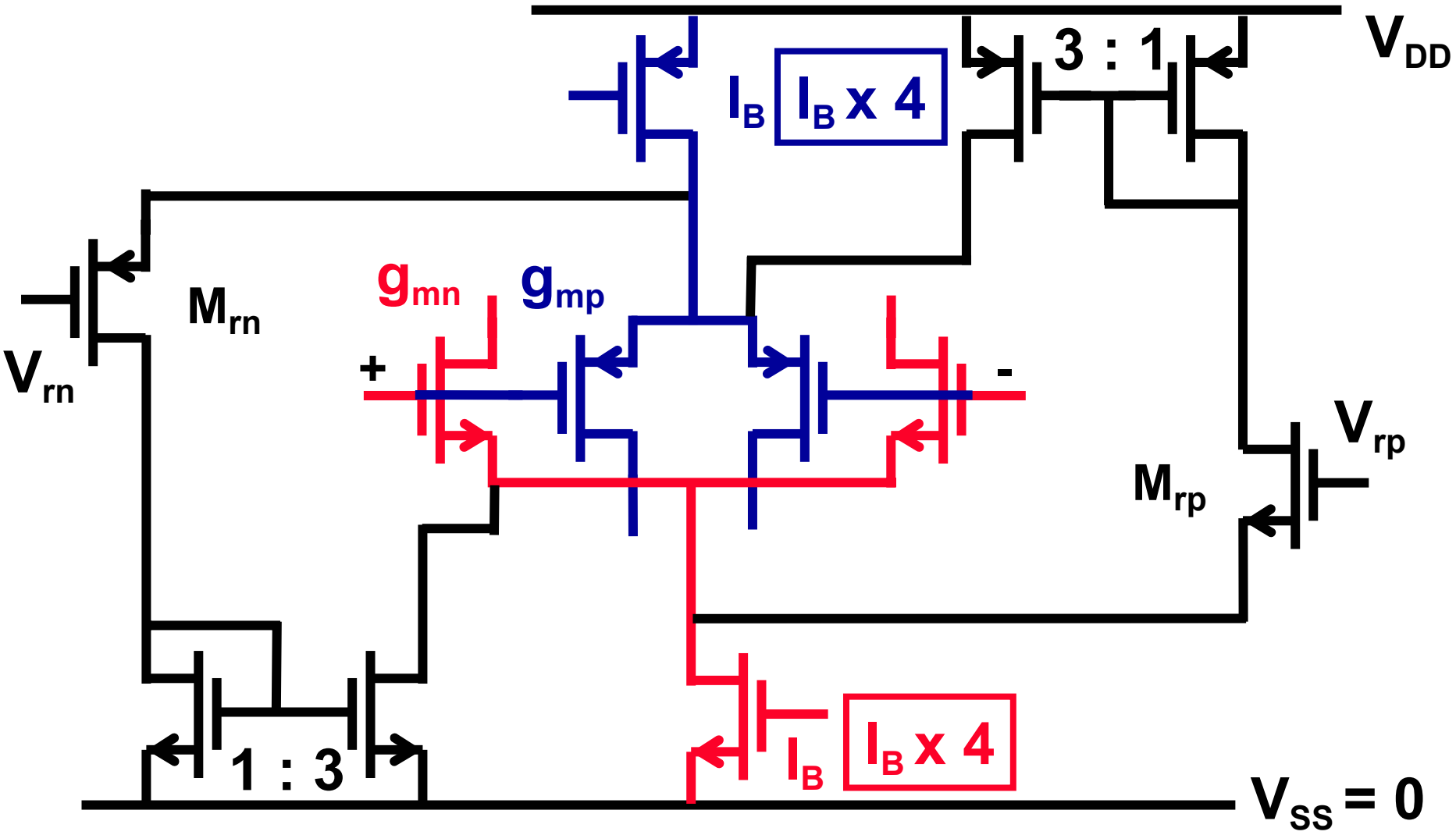
$$\sqrt{I_{Bn}} + \sqrt{I_{Bp}} = ct3$$

3 x Current mirror : $\sqrt{1} + \sqrt{1} = \sqrt{0} + \sqrt{4}$ > 4 - 1 = 3

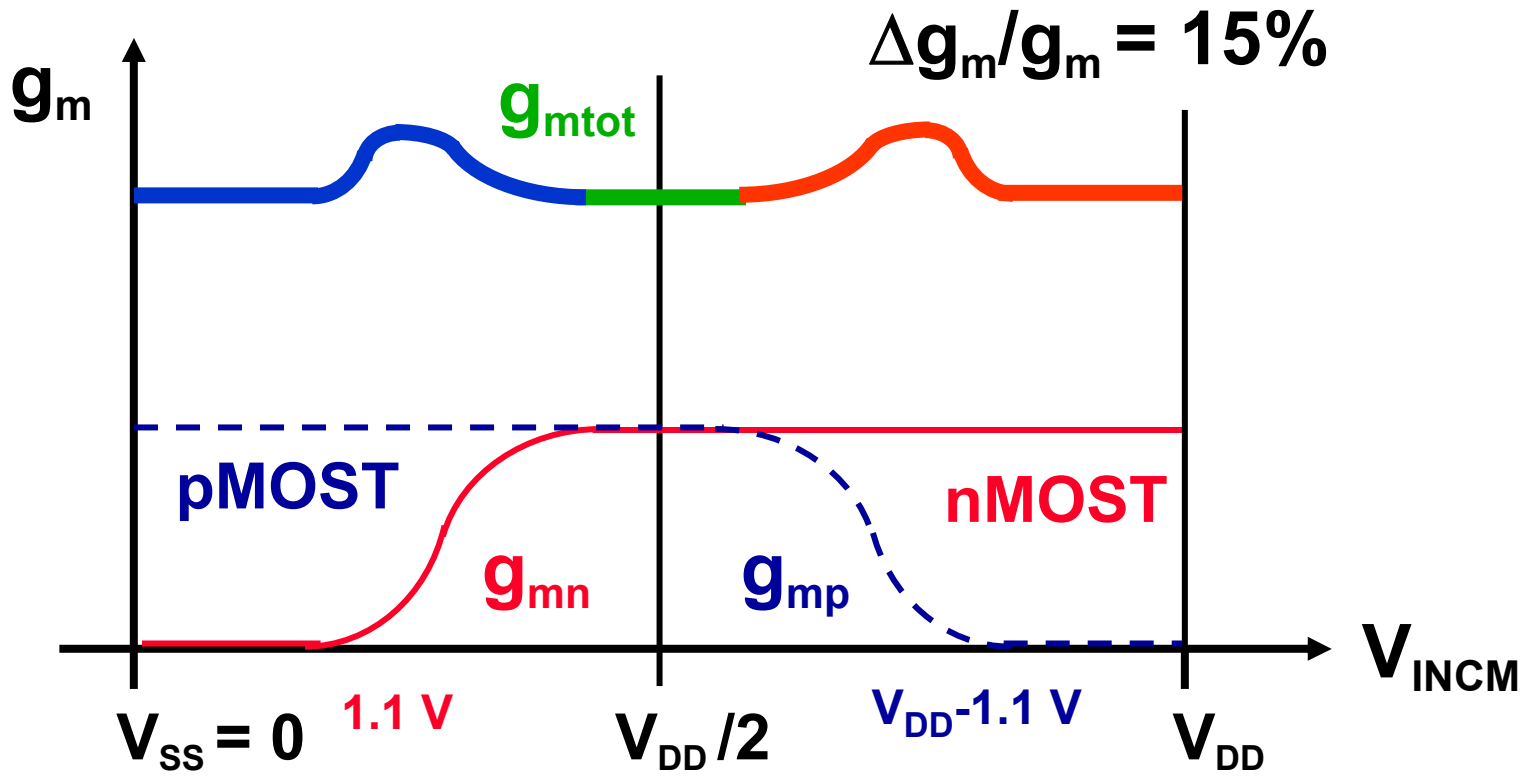
3x Current mirror for nMOSTs



3x Current mirror for all MOSTs

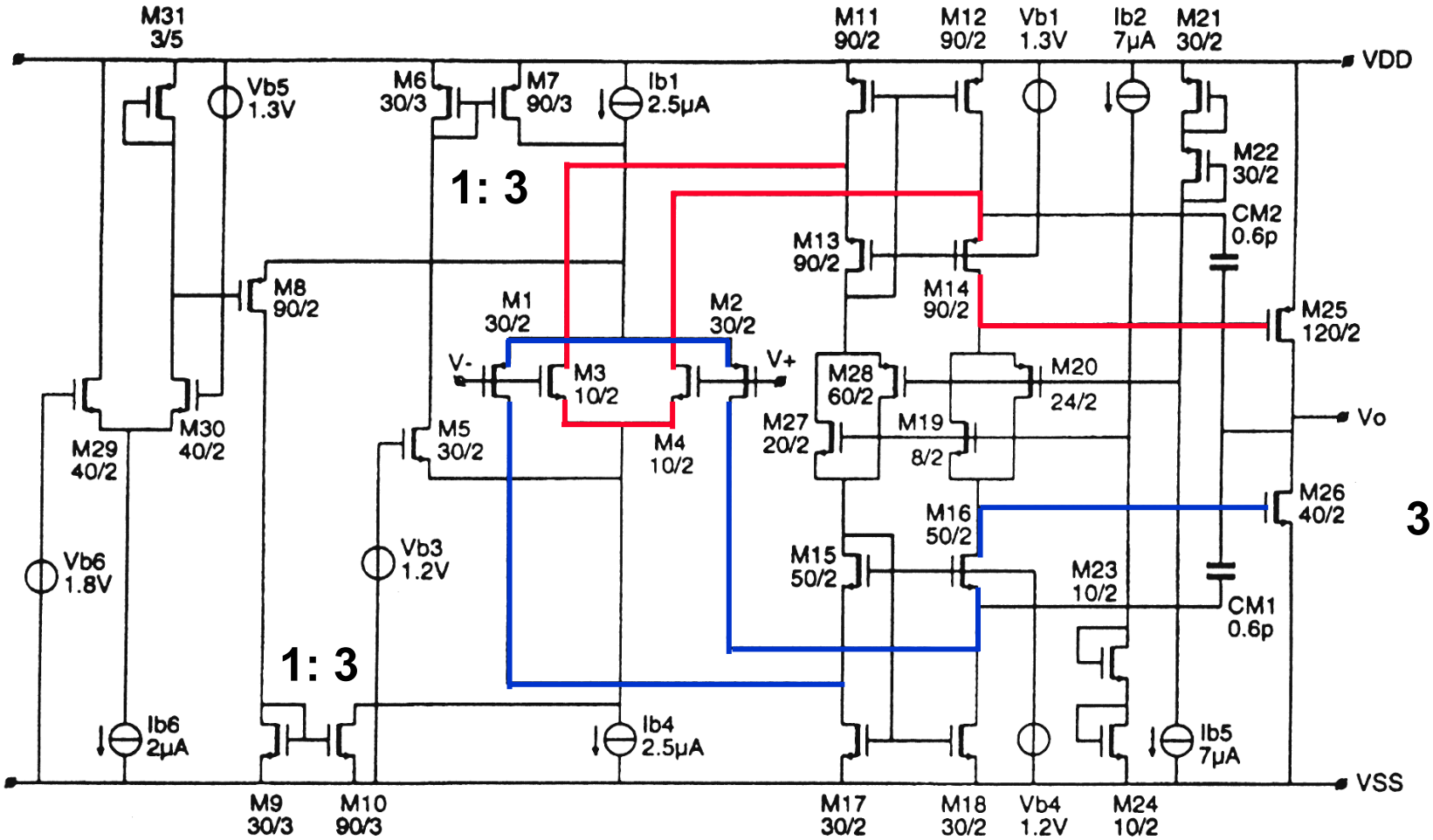


3x Current mirror : performance



$$g_{mtot} \sim \sqrt{(4 - 3x)\, I_B} + \sqrt{x\, I_B} \qquad \Delta g_m/g_m = 15\% \quad (x=1/3)$$

Rail-to-rail opamp



6.4 MHz
/ 10 pF

6.4 V/µs

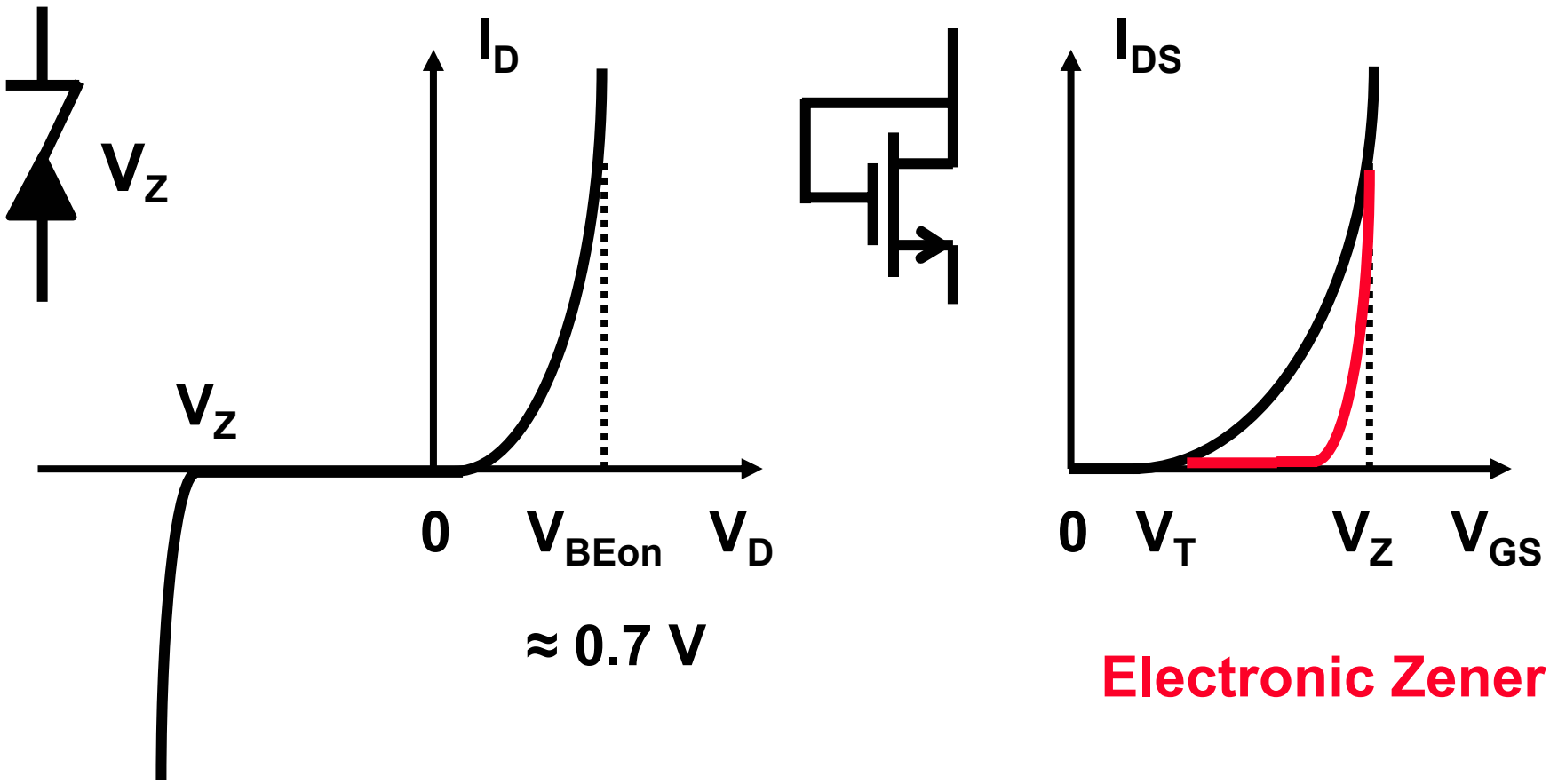
31 nV/√ Hz

3.3 V
0.18 mA
3 mApk

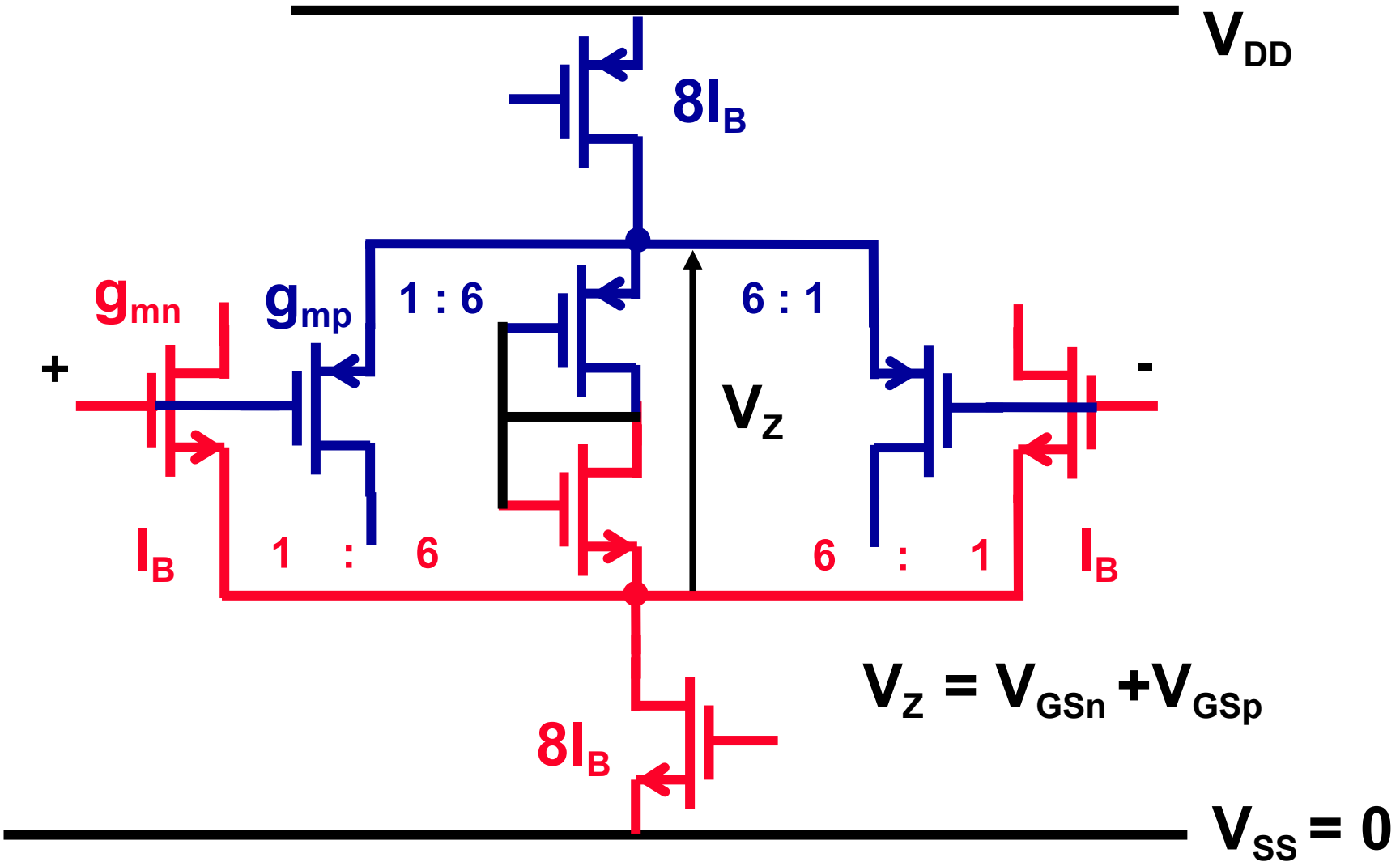
Ref.Hogervorst, JSSC Dec.1994, 1505-1512

Table of contents

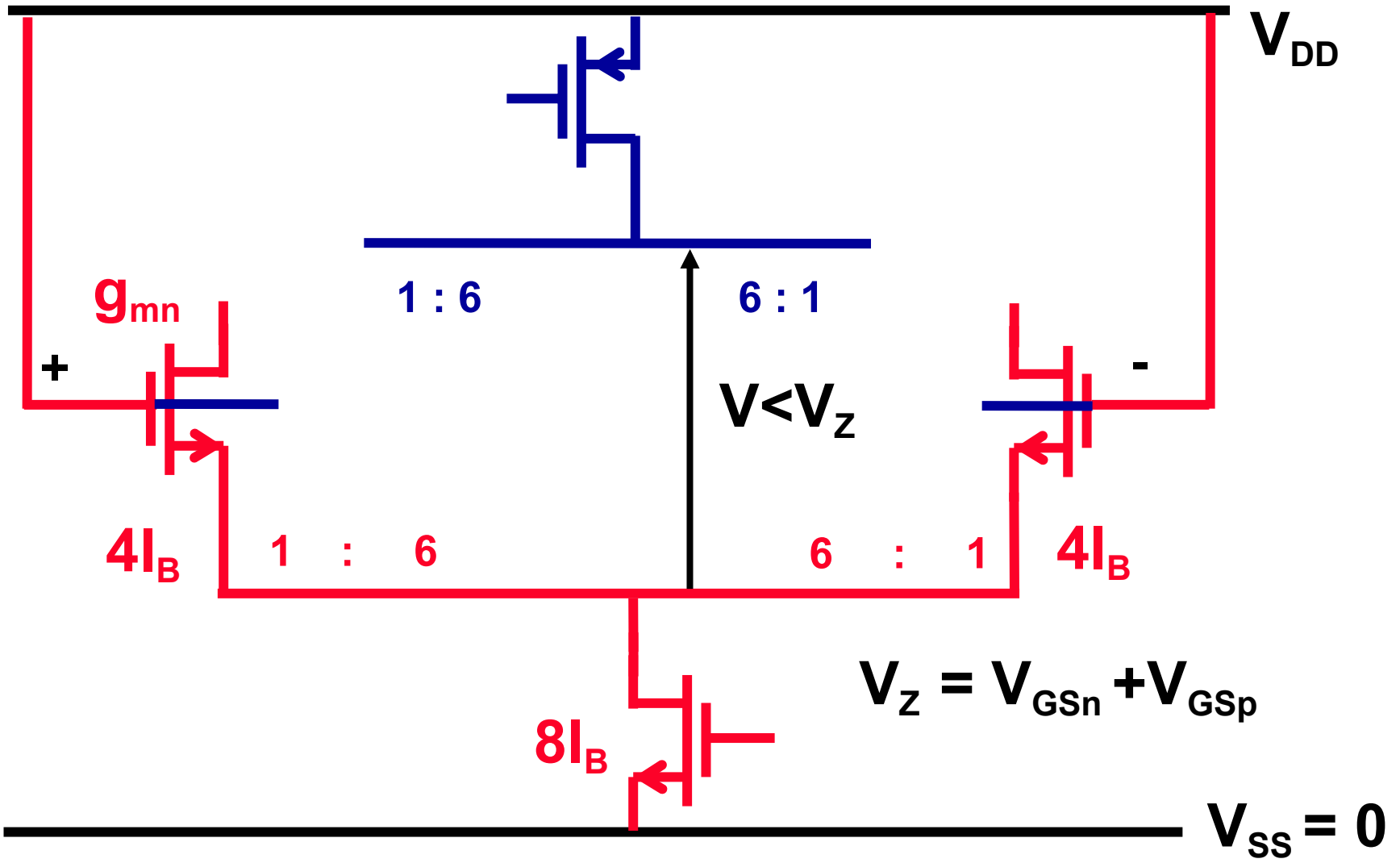
Zener diodes



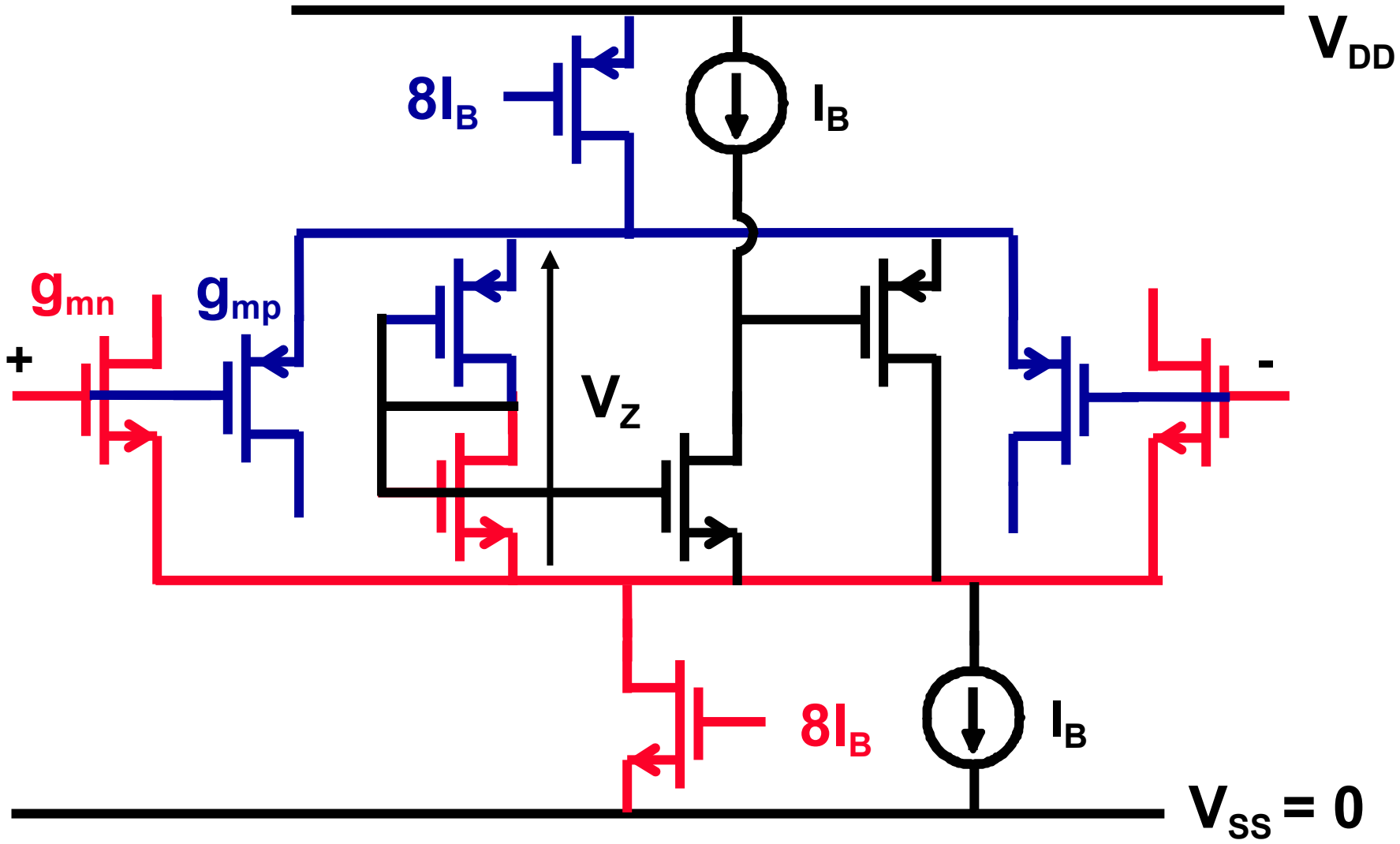
Rail-to-rail amplifier with Zener diode



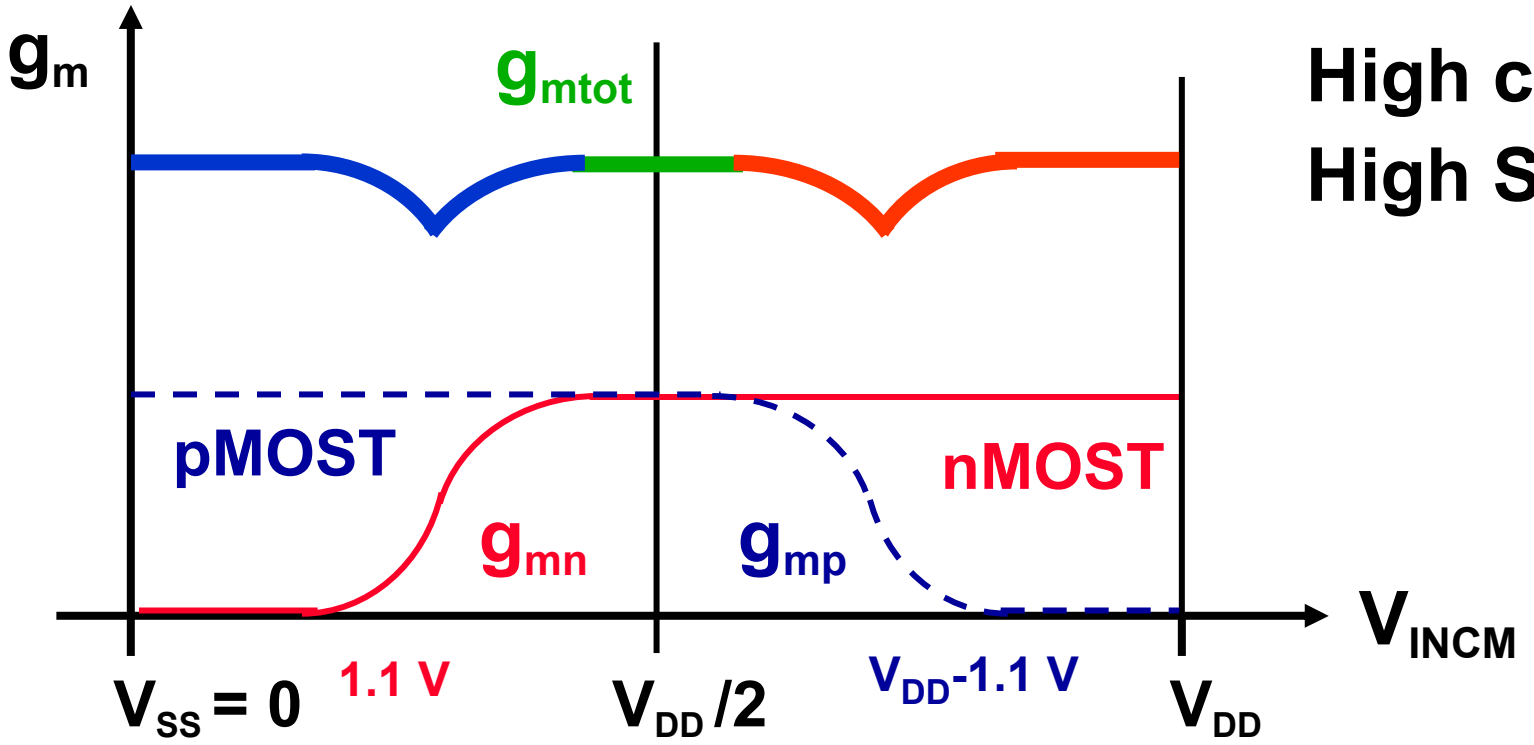
Rail-to-rail amplifier with Zener diode



Rtr amp. with electronic Zener



Rail-to-rail amp. with Zener : performance



High current
High SR !

Zener: $\Delta g_m/g_m = 25\%$ Electronic Zener: $\Delta g_m/g_m = 6\%$

Ref.Hogervorst, JSSC July 1996, 1035-1040

Table of contents

Equalize g_{mtot} in weak inversion

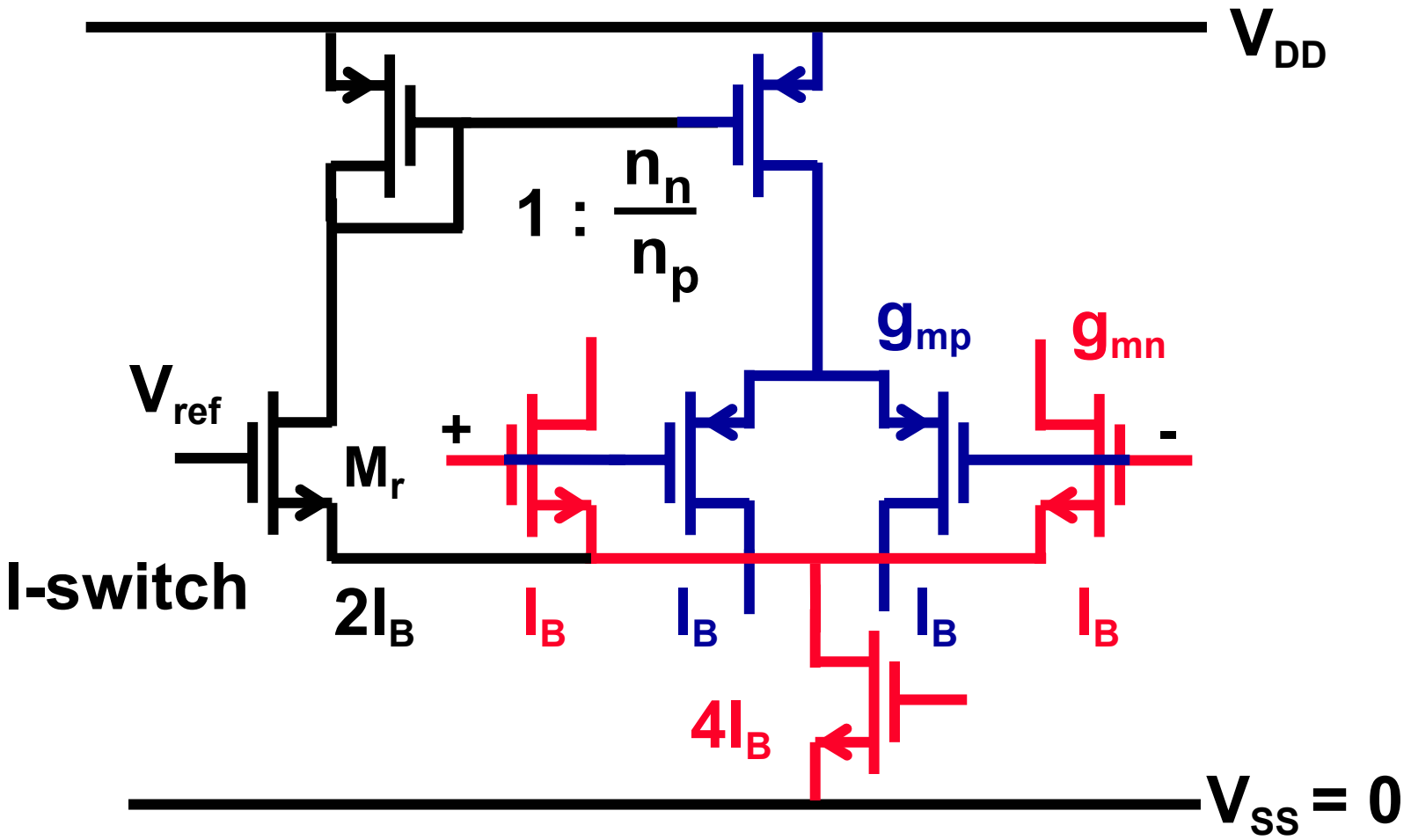
$$g_{mn} + g_{mp} = ct$$

$$\frac{I_{Bn}}{2\, n_n\ kT/q} + \frac{I_{Bp}}{2\, n_p\, kT/q} = ct$$

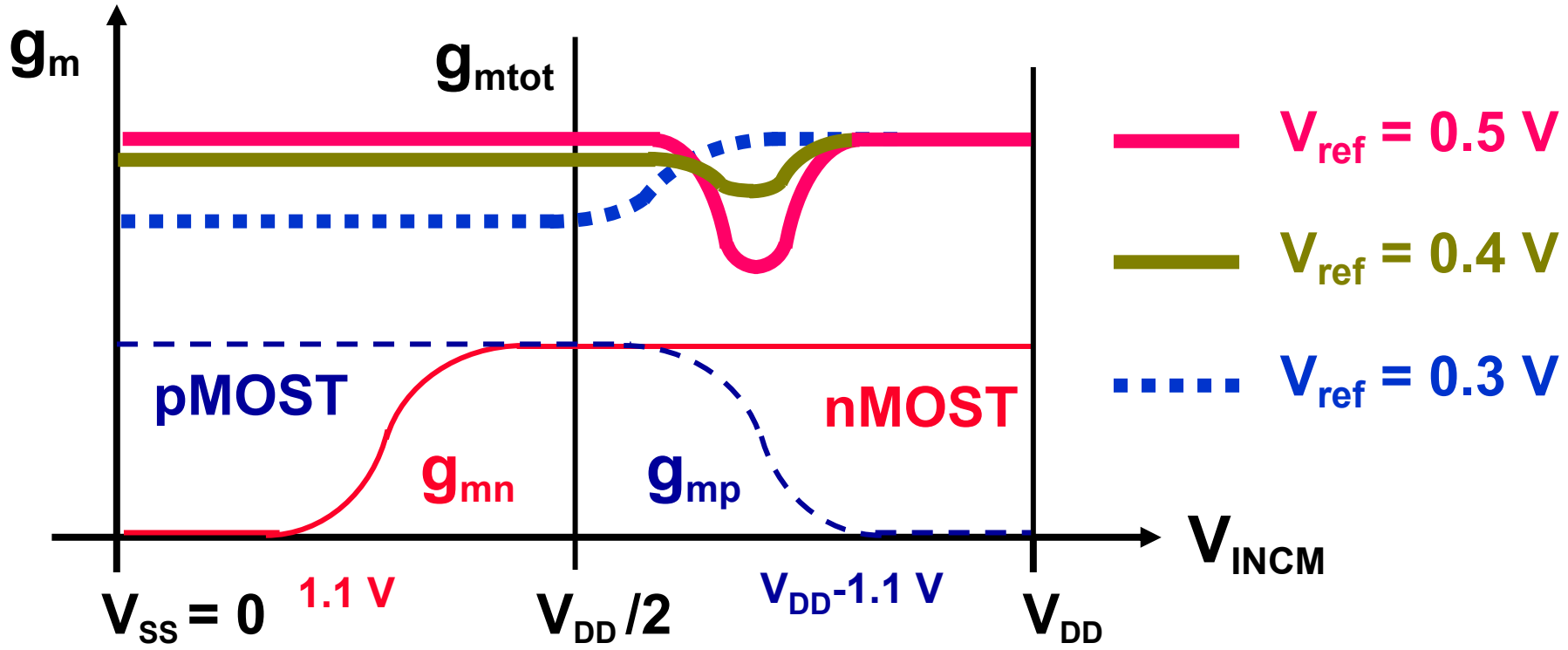
$$I_{Bn} + \frac{n_n}{n_p} I_{Bp} = ct$$

$$n = 1 + \frac{C_D\,(V_{BS})}{C_{ox}}$$

Rail-to-rail amplifier with current switch

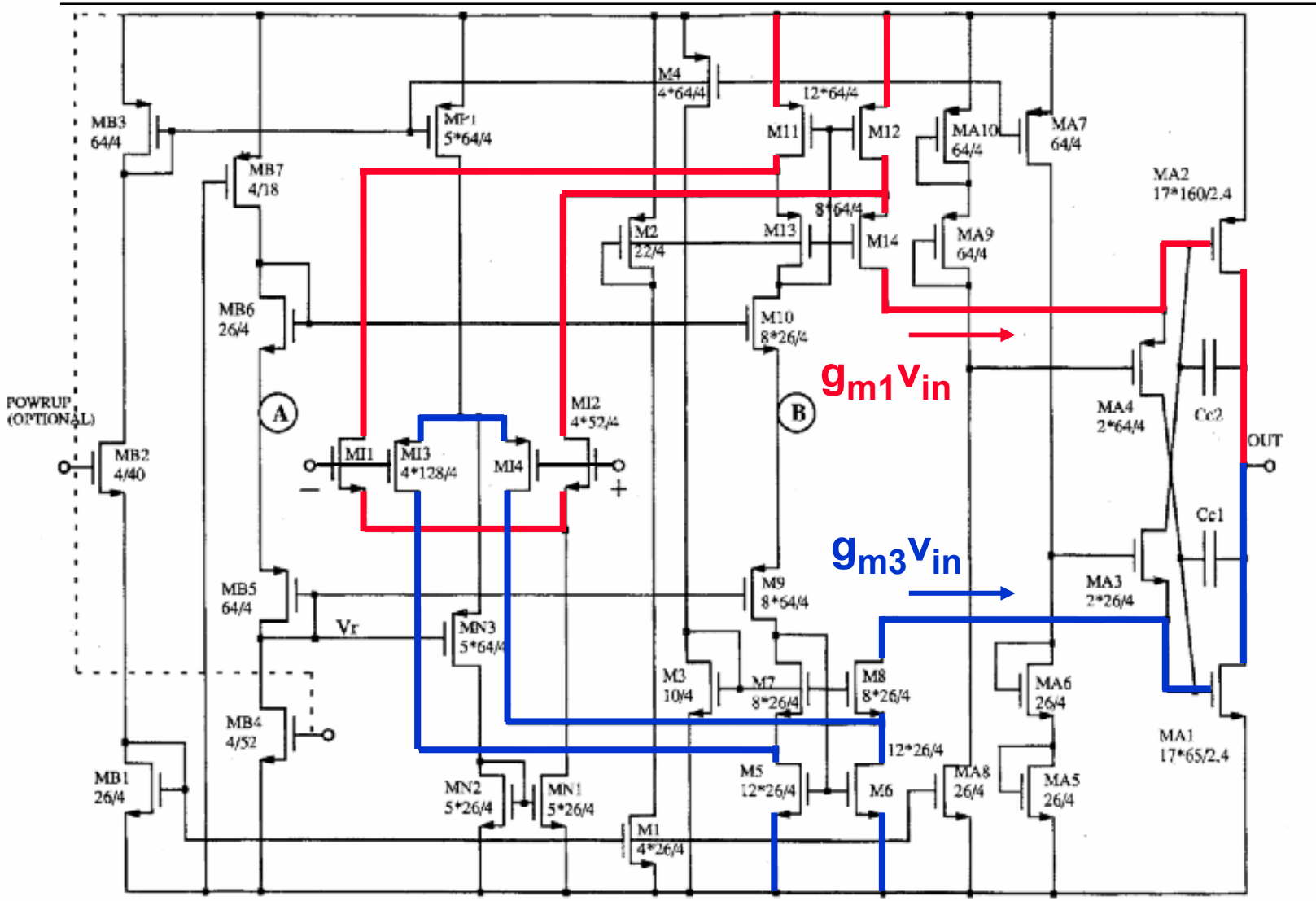


Rtr amp. with I-switch : performance



Current switch : V_{ref} very critical !

Ref. : Wu etal, JSSC Jan.1994, pp.63-66



14 MHz / 11pF

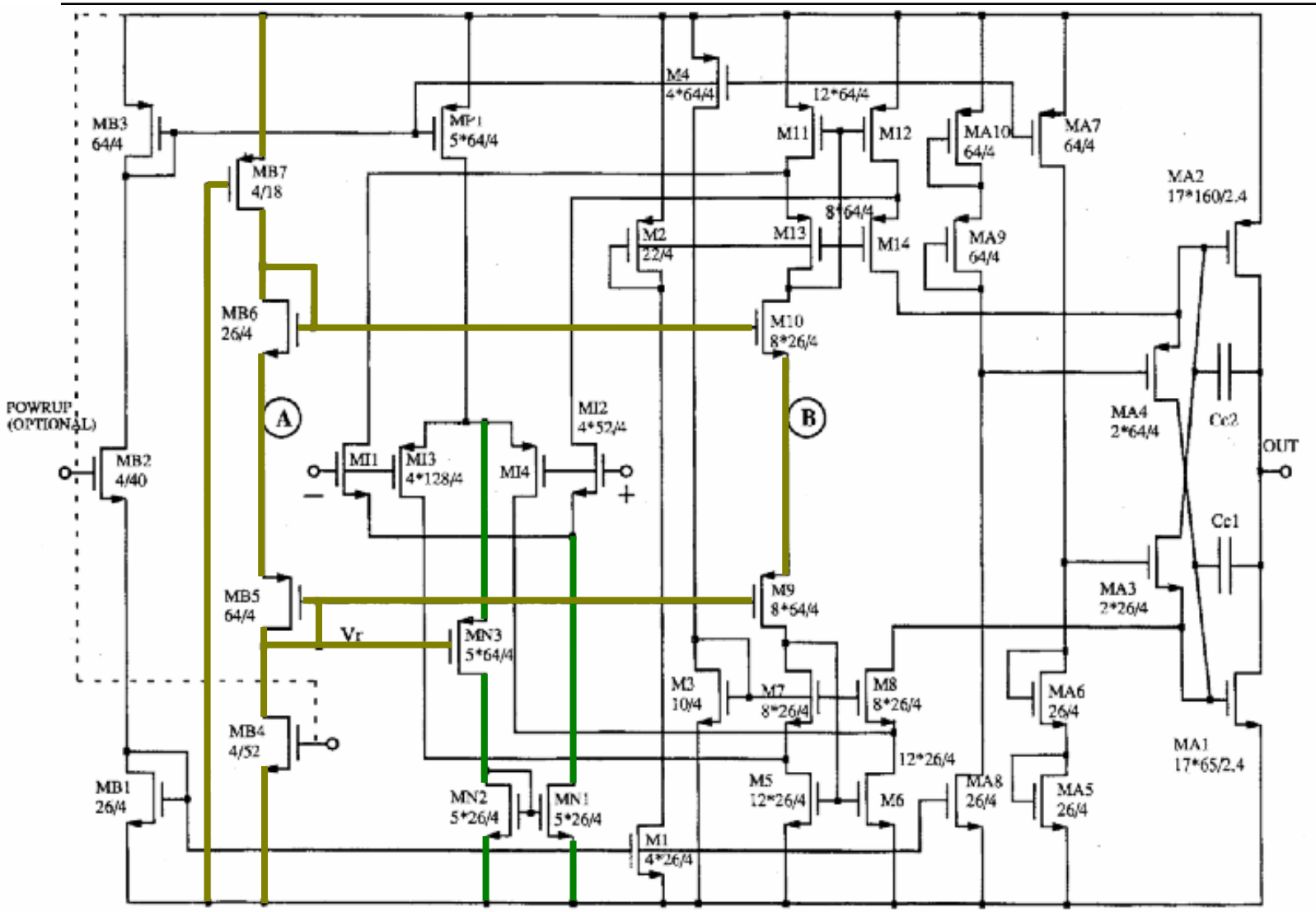
5.6 MHz / 100pF

4 V/μs

36 nV/√ Hz

5 V
0.4 mA

Ref. : Wu etal, JSSC Jan.1994, pp.63-66

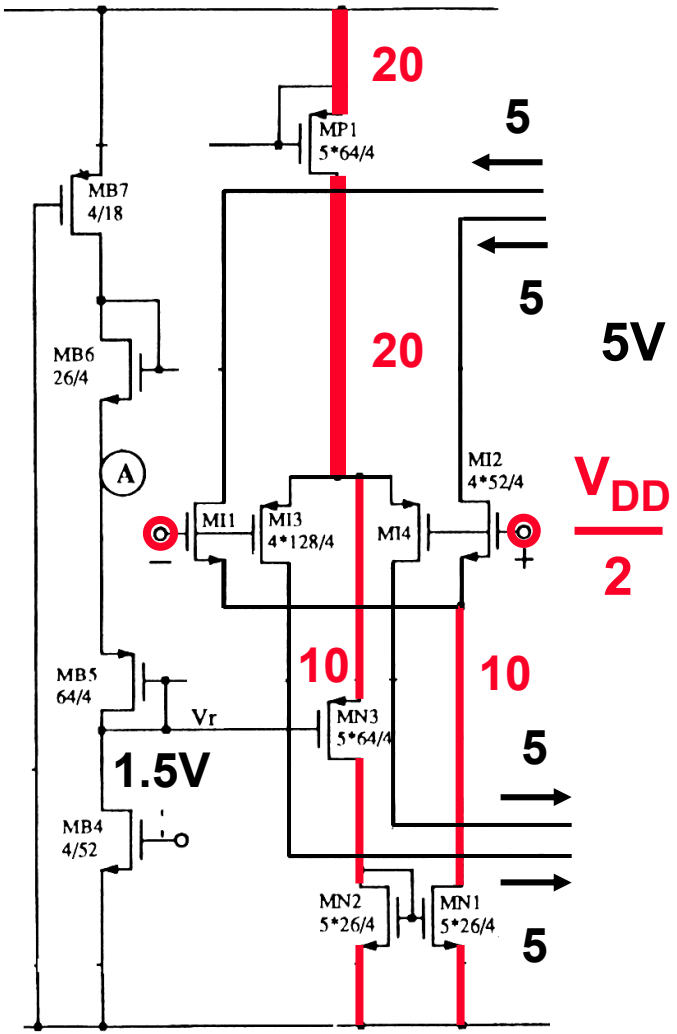


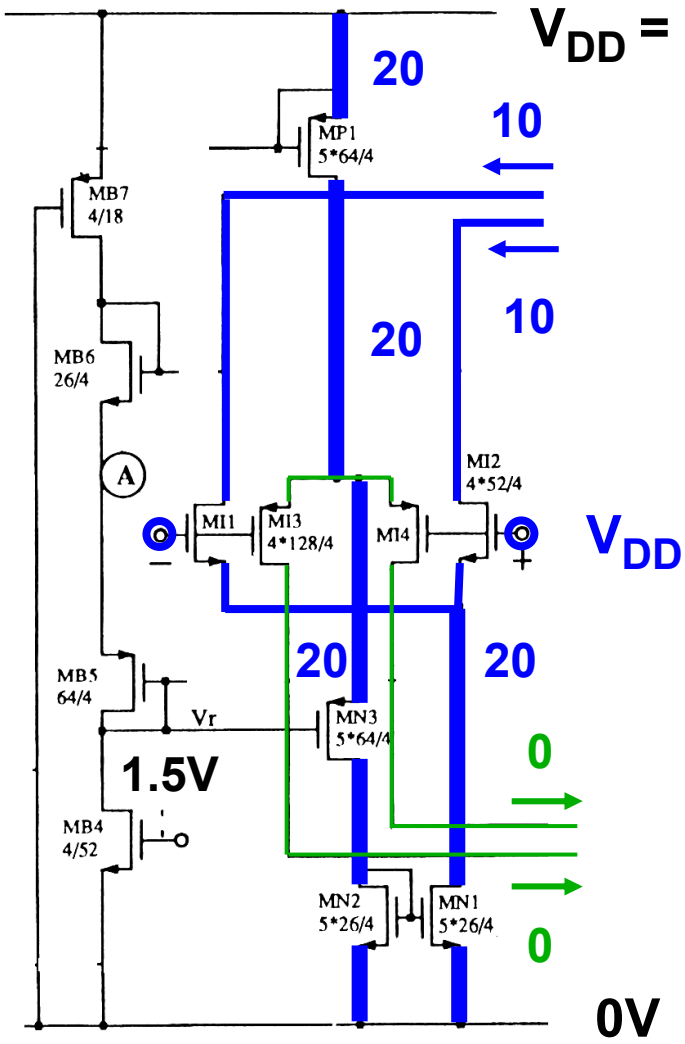
Biasing :

I_{DS} x 2

g_m x 2

Input rail-to-rail stage





V_{+-} high :

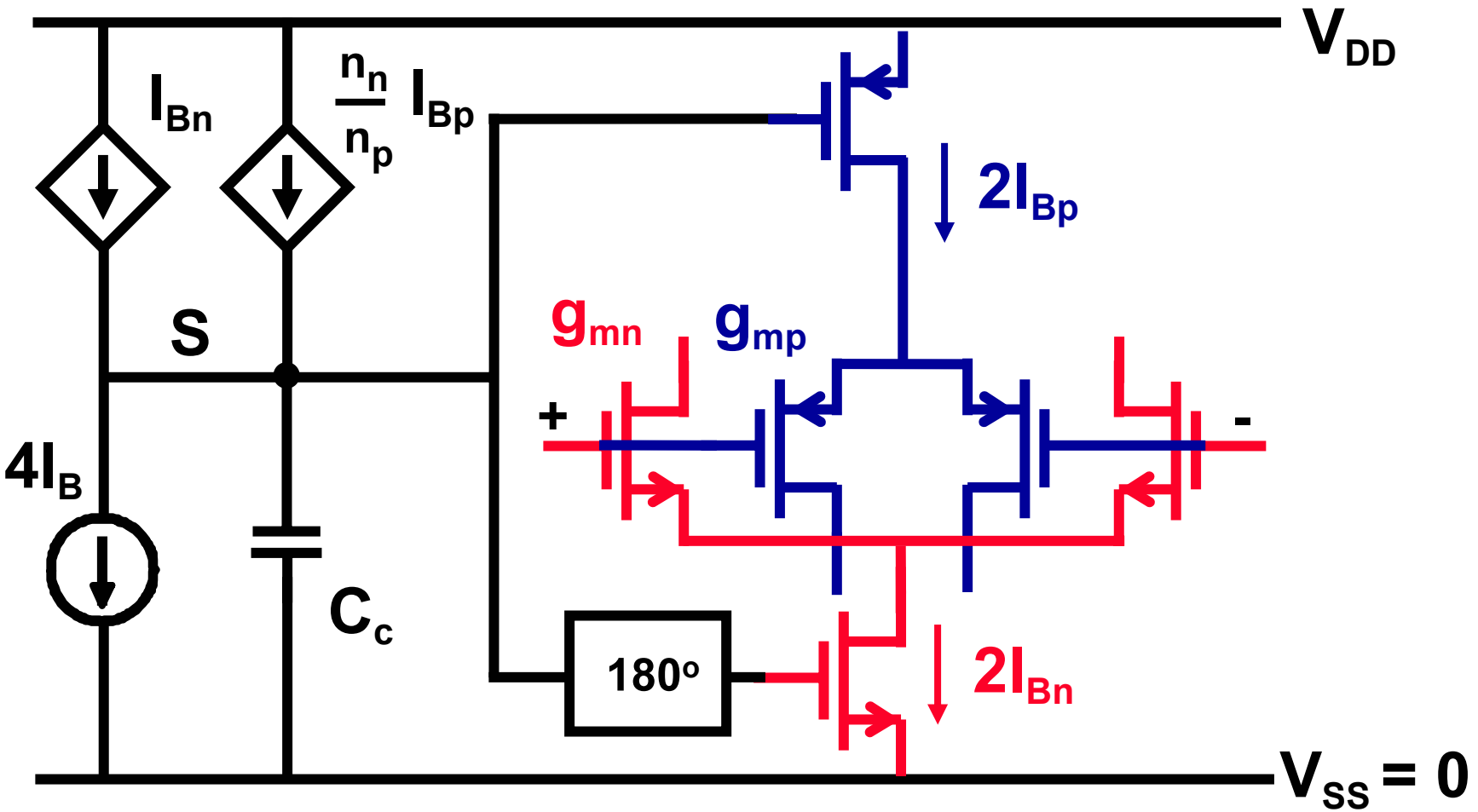
pMOSTs off !

nMOSTs :

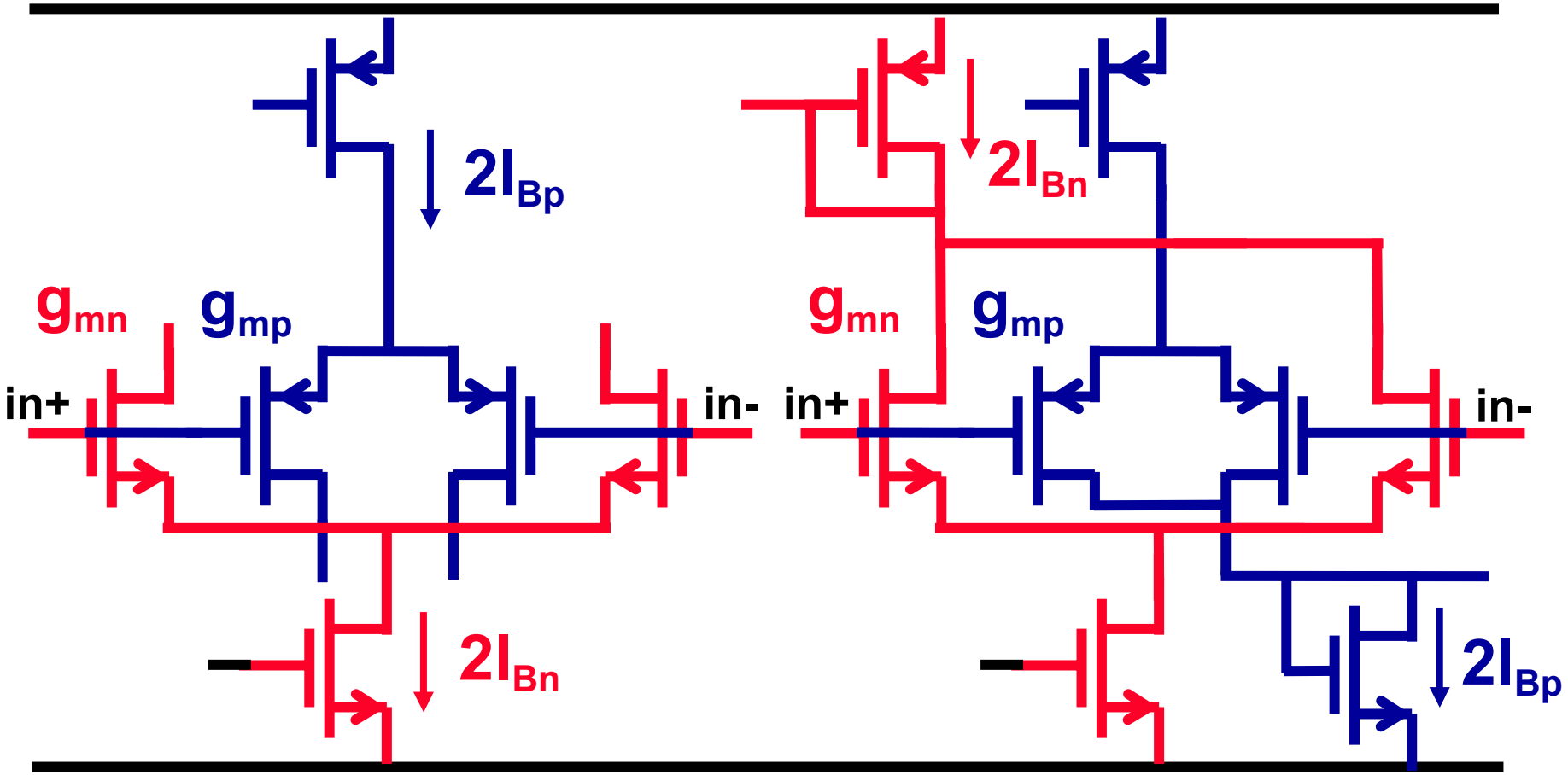
I_{DS1} x 2

g_{m1} x 2

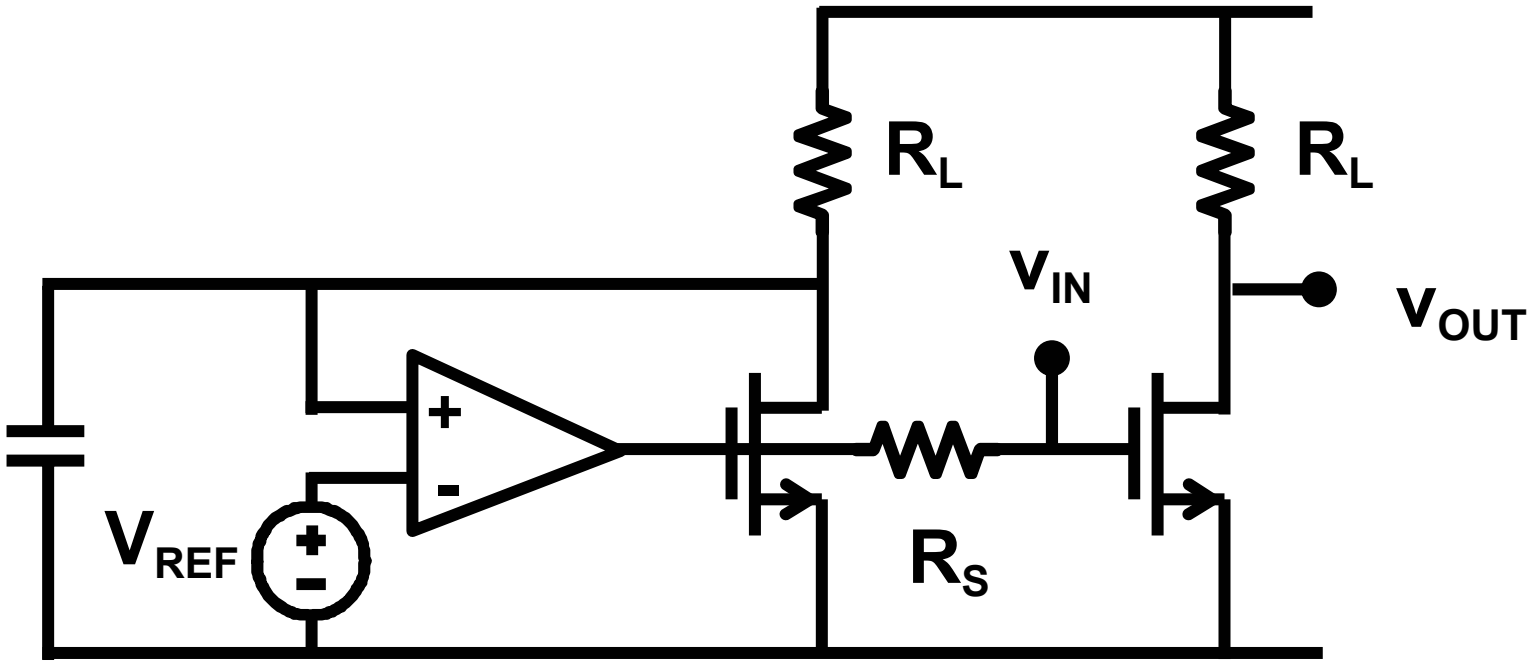
Current regulator FB loop



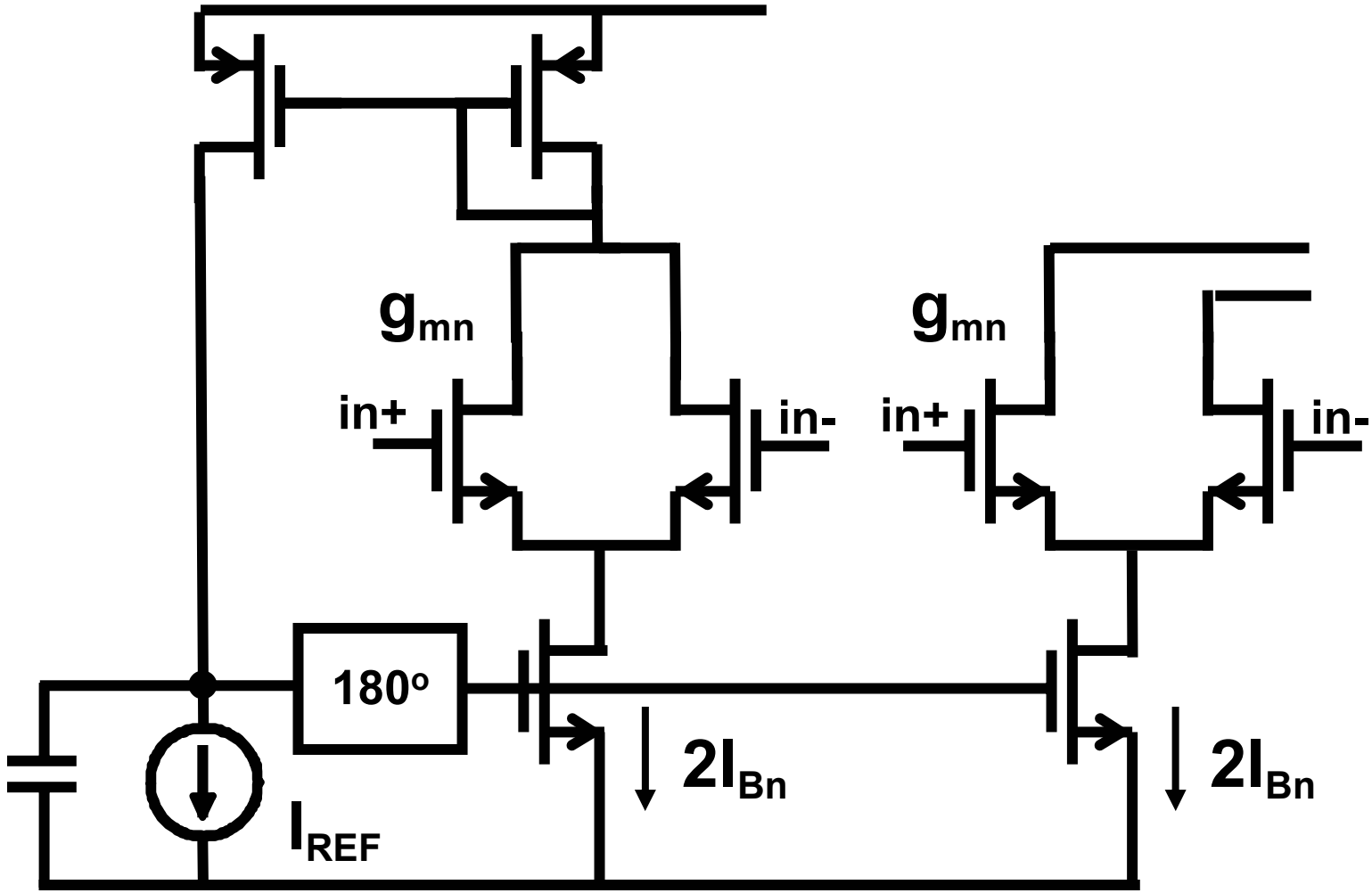
Current regulator FB loop : replica biasing



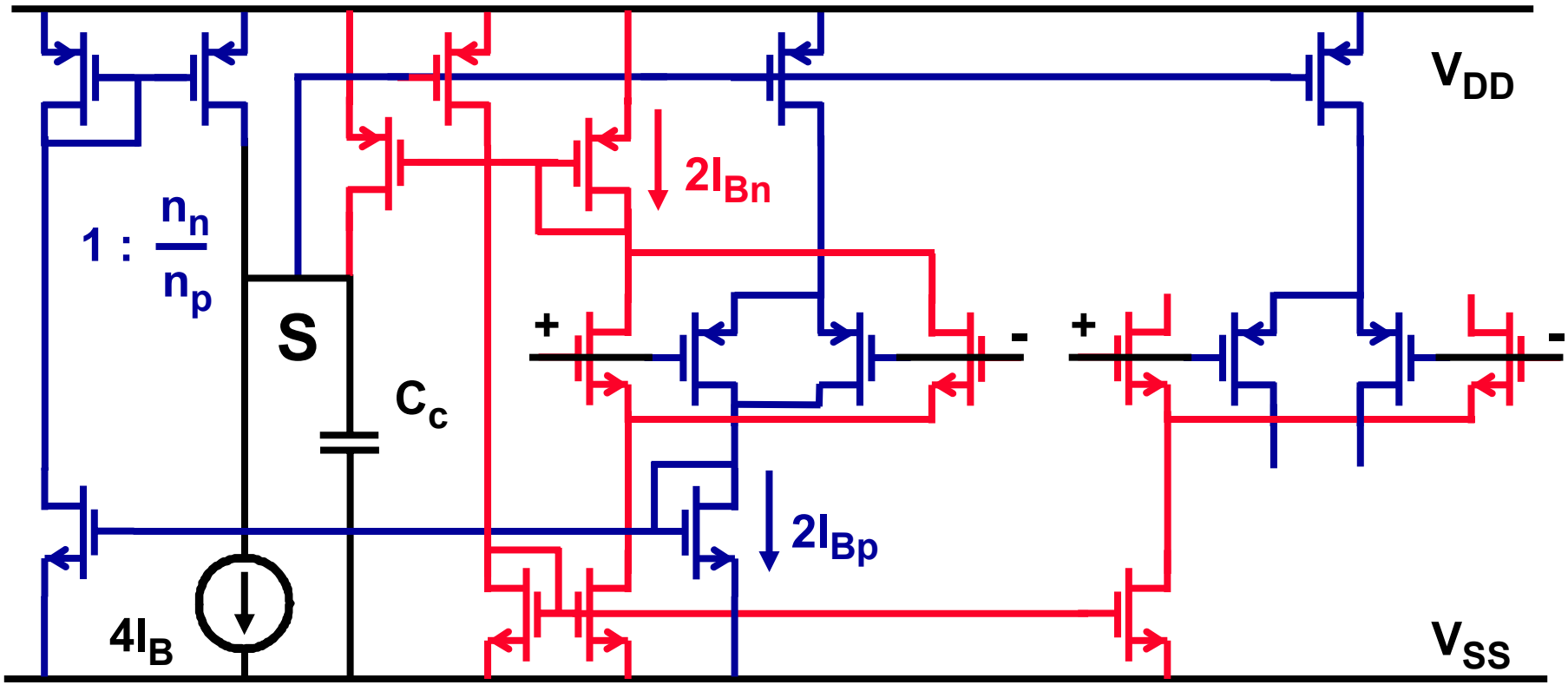
Replica biasing with one transistor



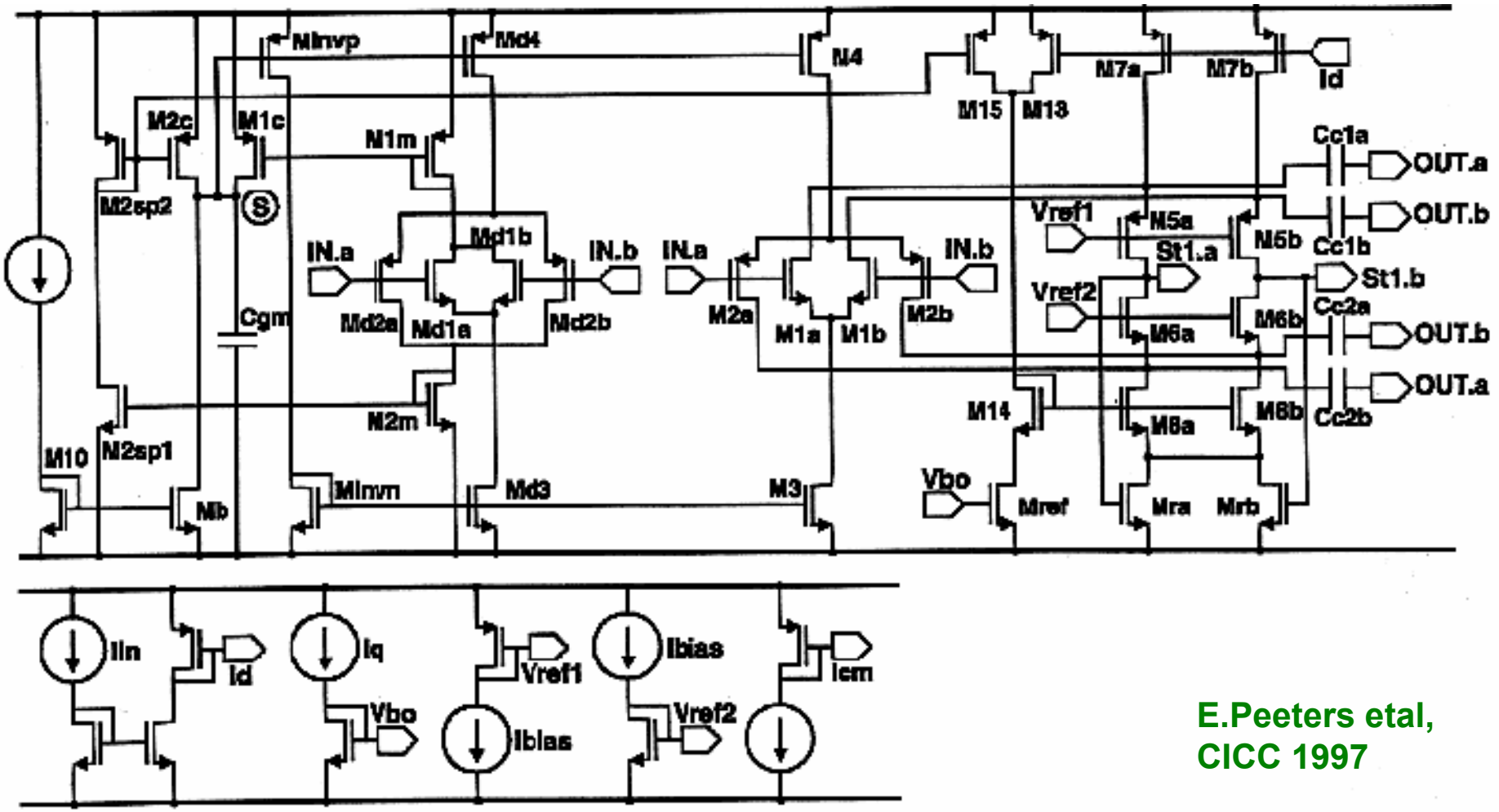
Replica biasing with differential pair



Current regulator rail-to-rail amplifier

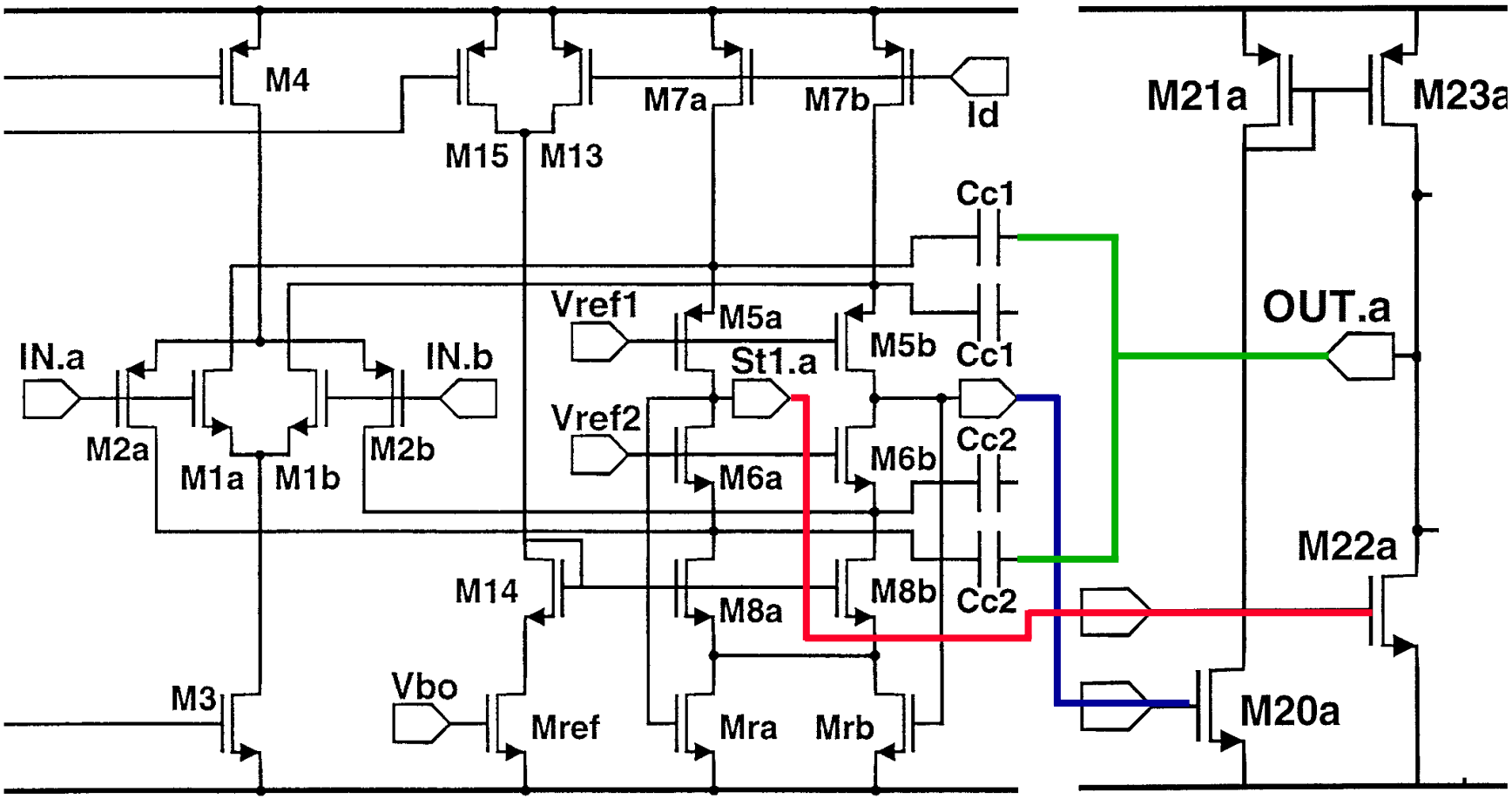


I-regulator rtr amplifier



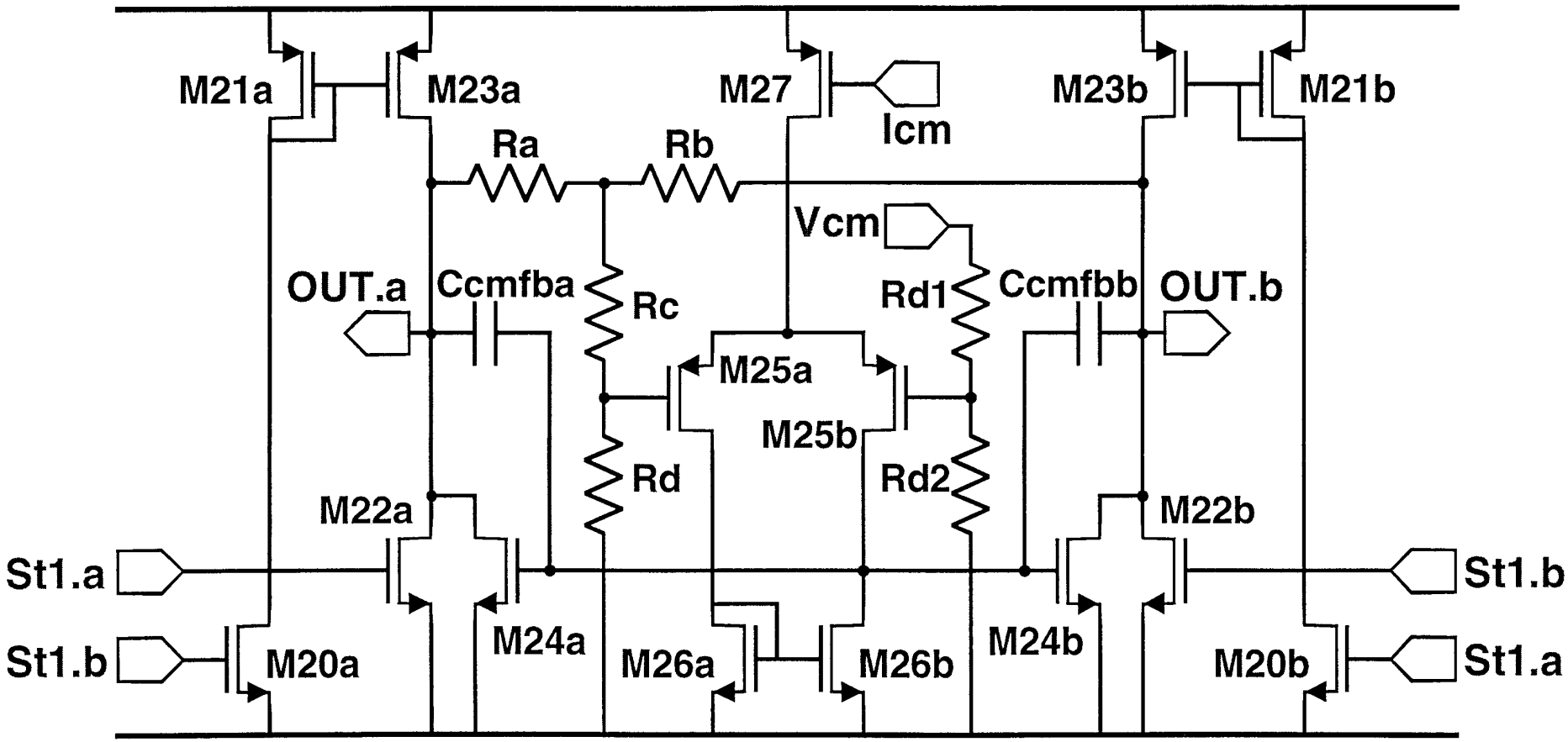
E.Peeters etal,
CICC 1997

Total amplifier schematic

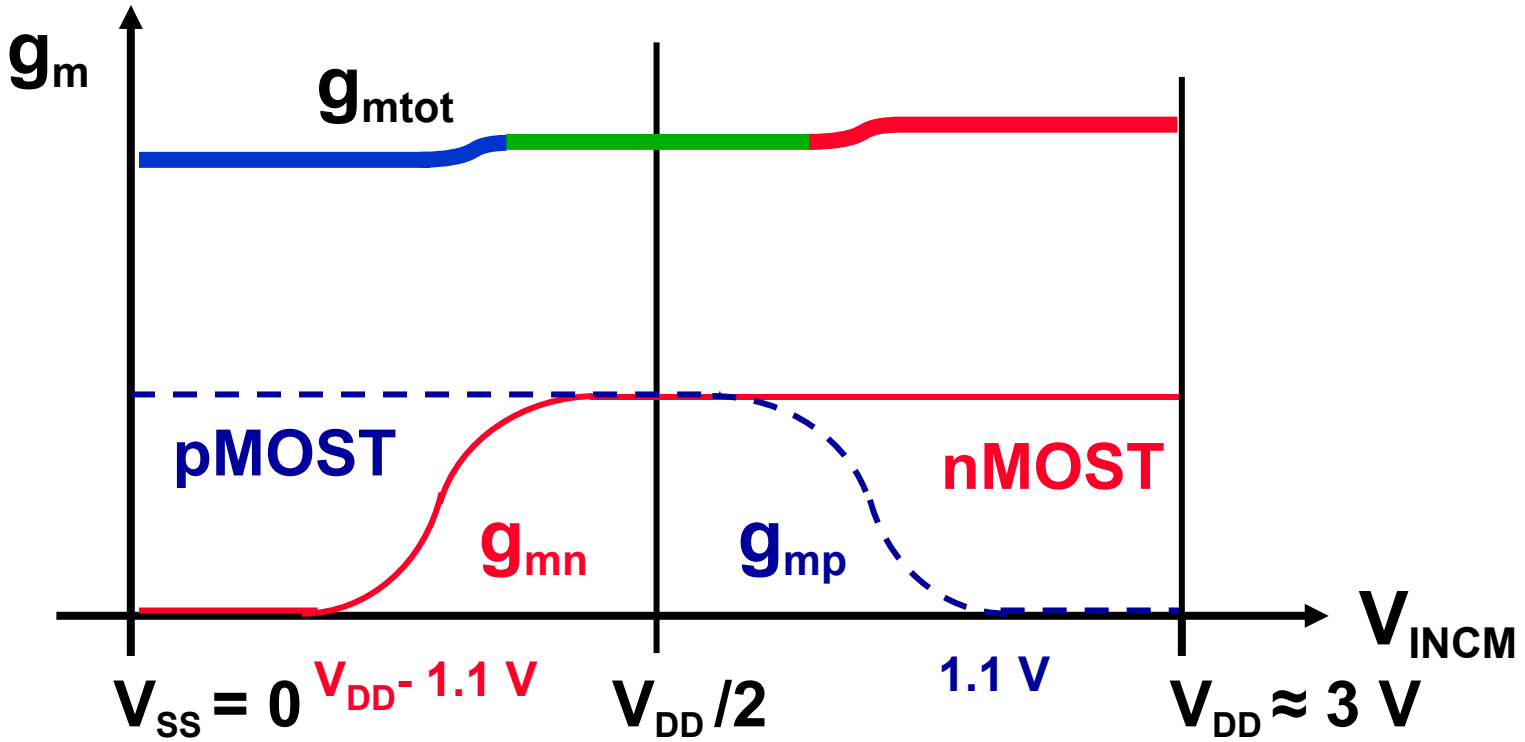


E.Peeters etal, CICC 1997

Output stage

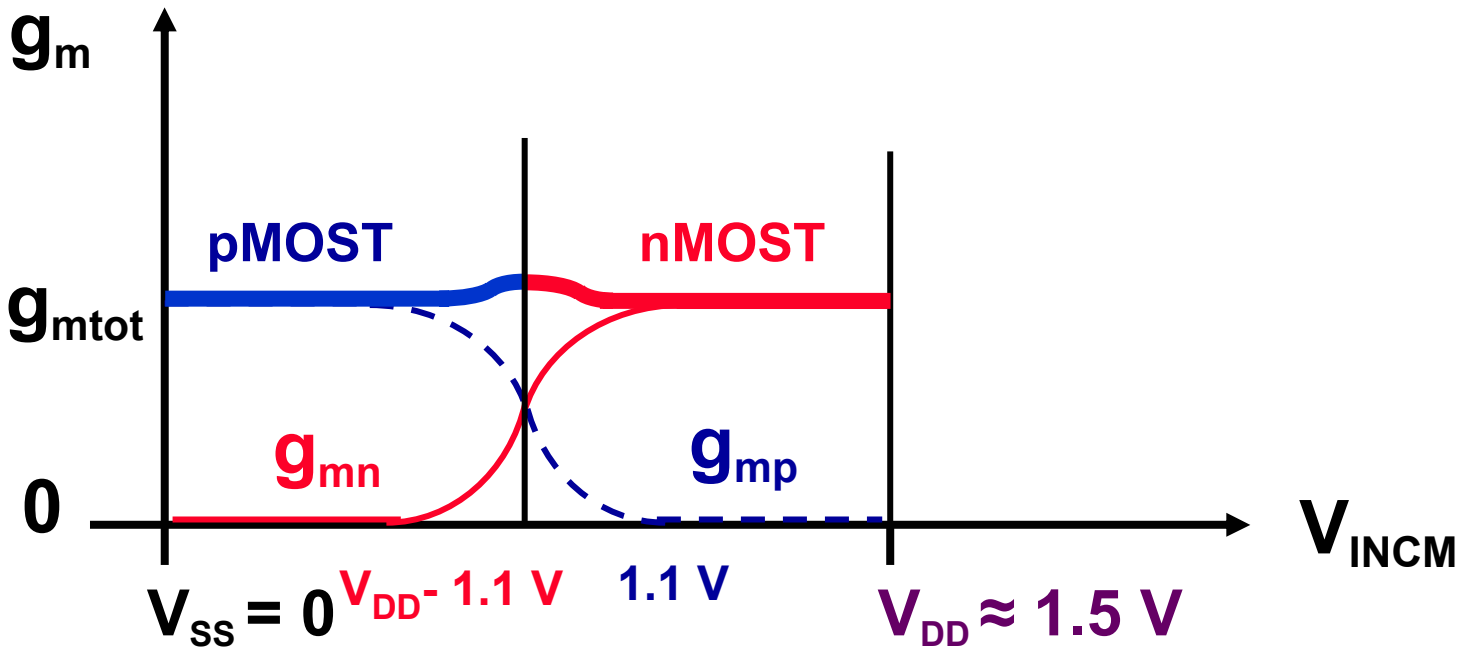


Current-regulator rtr amp. : performance



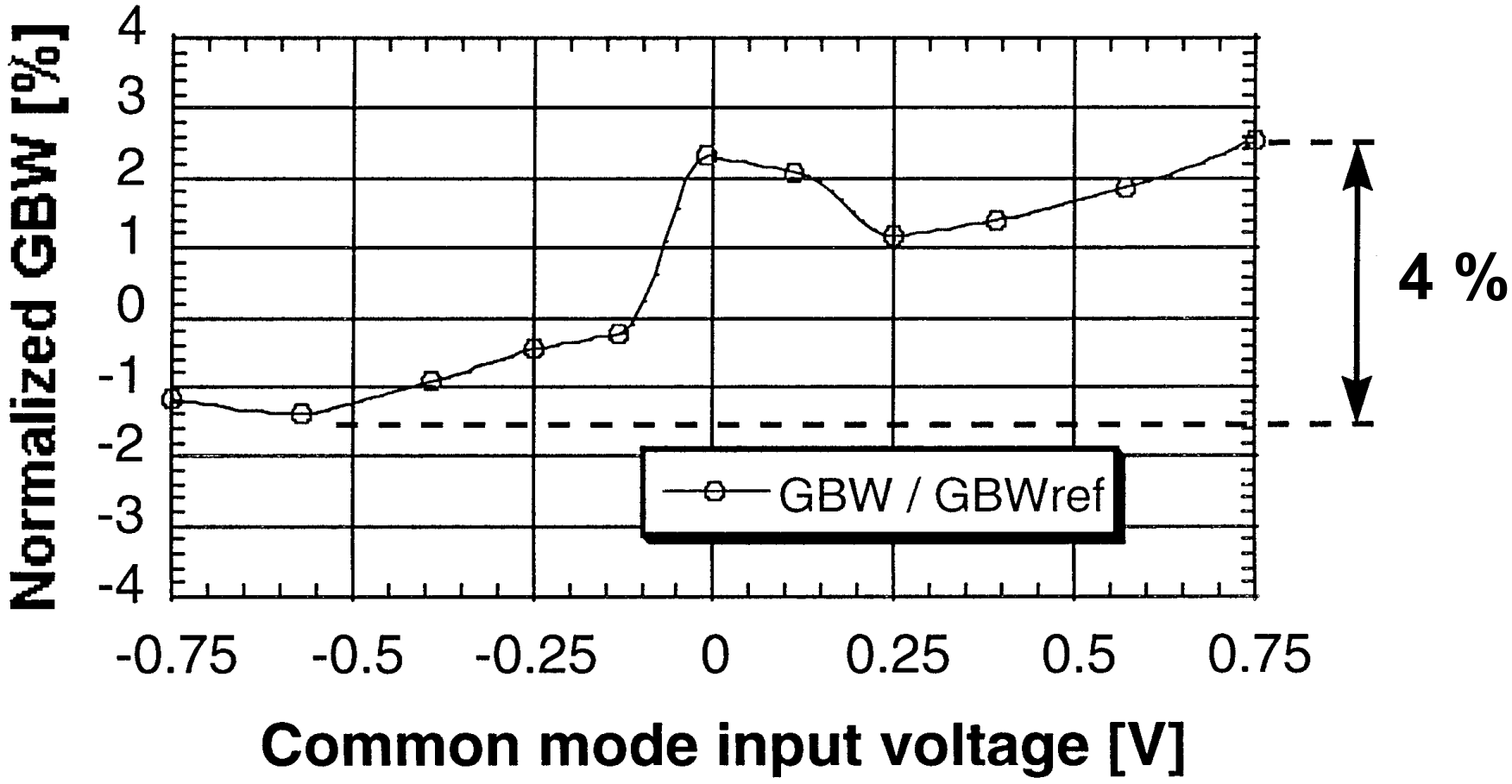
n - mismatch : $\Delta g_m/g_m \approx 4\%$

Current-regulator rtr amp. : towards 1.5 V

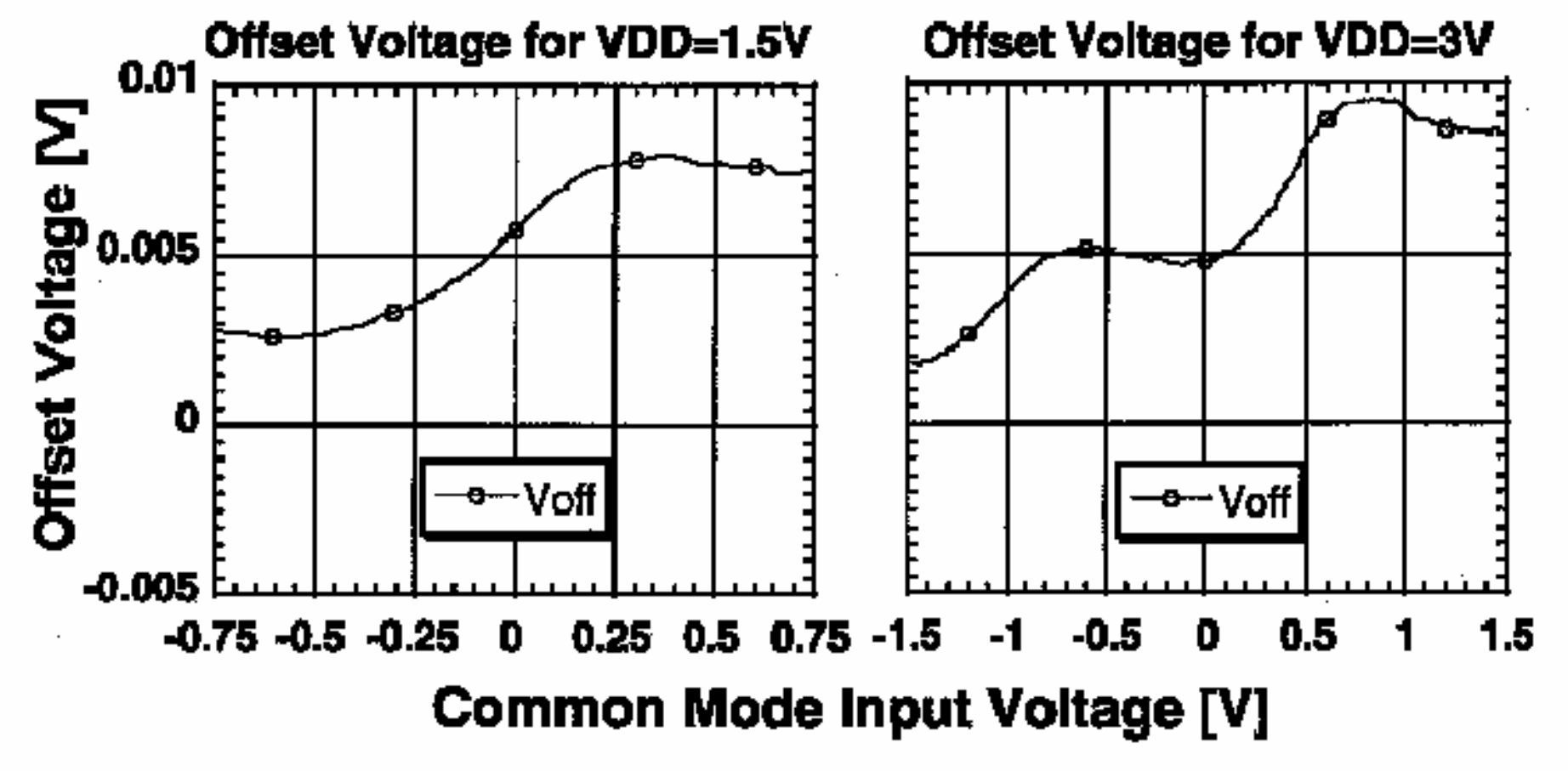


n - mismatch : $\Delta g_m/g_m \approx 4\%$

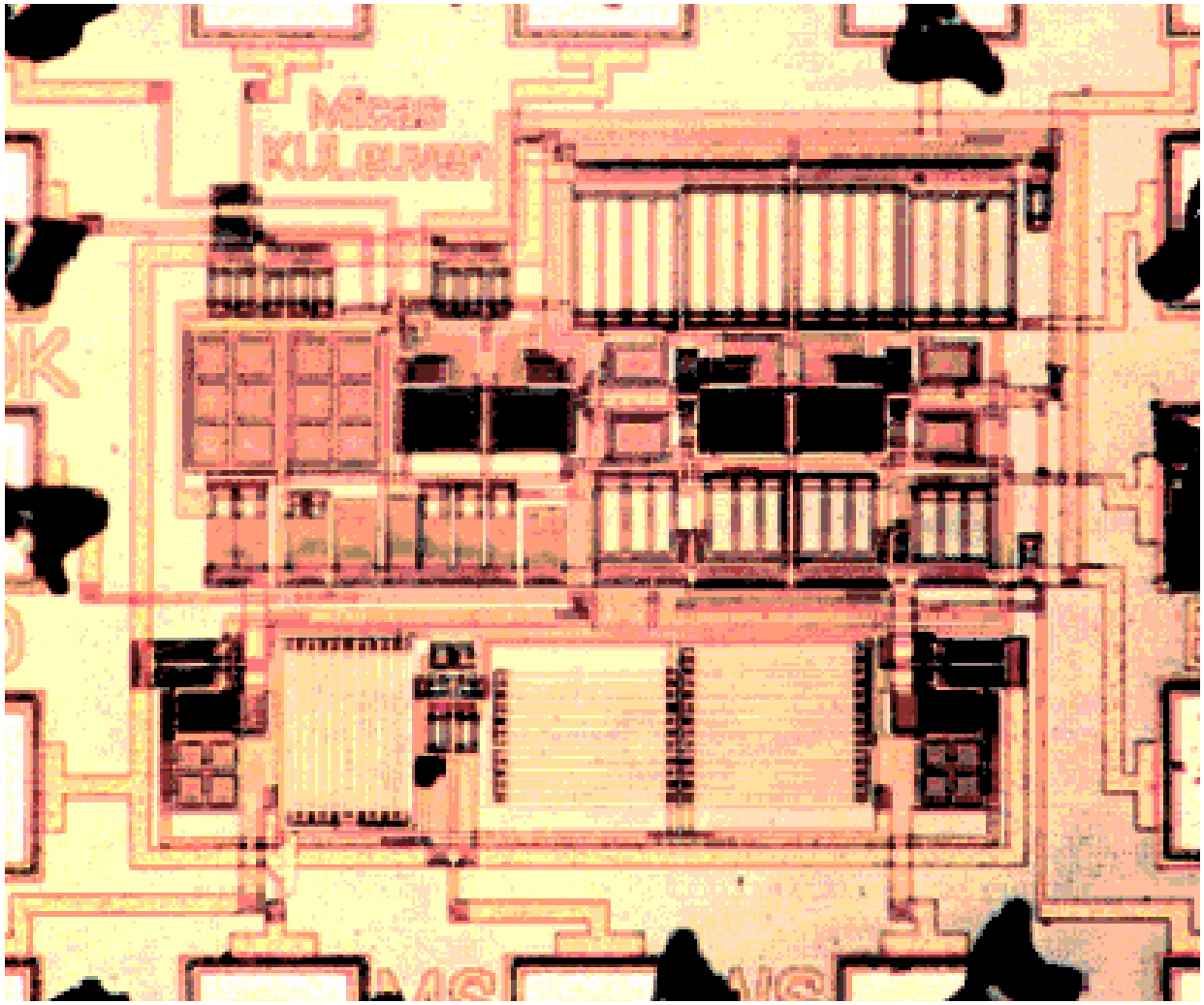
GBW error


Normalized GBW [%]
4
3
2
1
0
-1
-2
-3
-4
-0.75
-0.5
-0.25
0
0.25
0.5
0.75
Common mode input voltage [V]
GBW / GBWref
4 %

Input offset voltage



Rail-to-rail Opamp with Current regulator



V_{DD} = 1.5 V

I_{TOT} = 0.2 mA

$\Delta g_m/g_m$ = 4 %

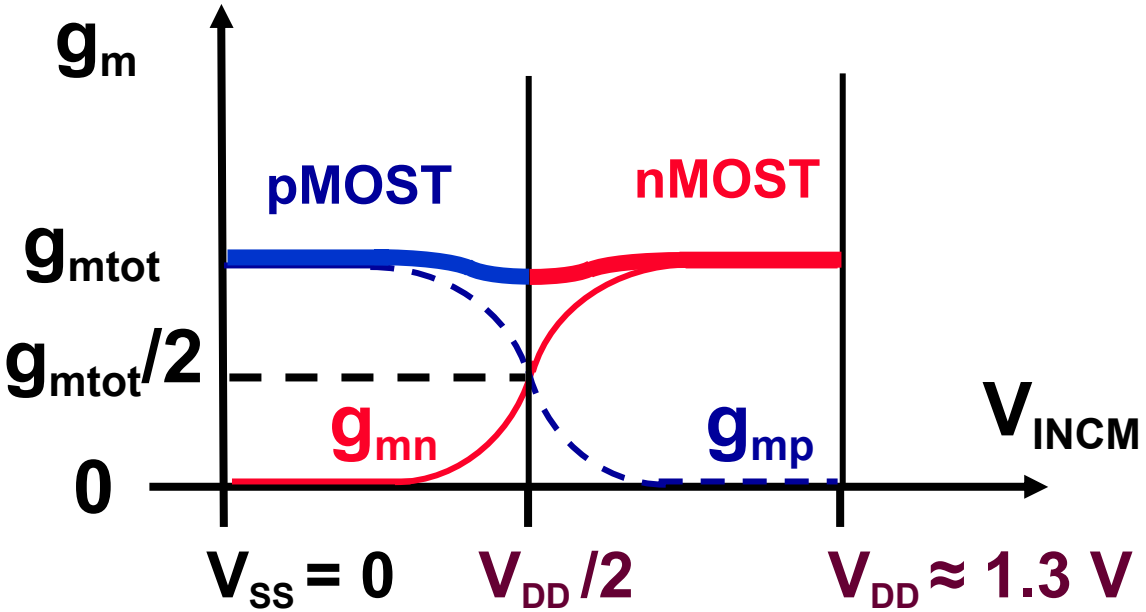
GBW = 4.3 MHz

C_L = 15 pF

E.Peeters etal, CICC 1997

Table of contents

Internal V_{DD} Regulator



Weak inversion :

$$I_{Bn} + \frac{n_n}{n_p} I_{Bp} = ct$$

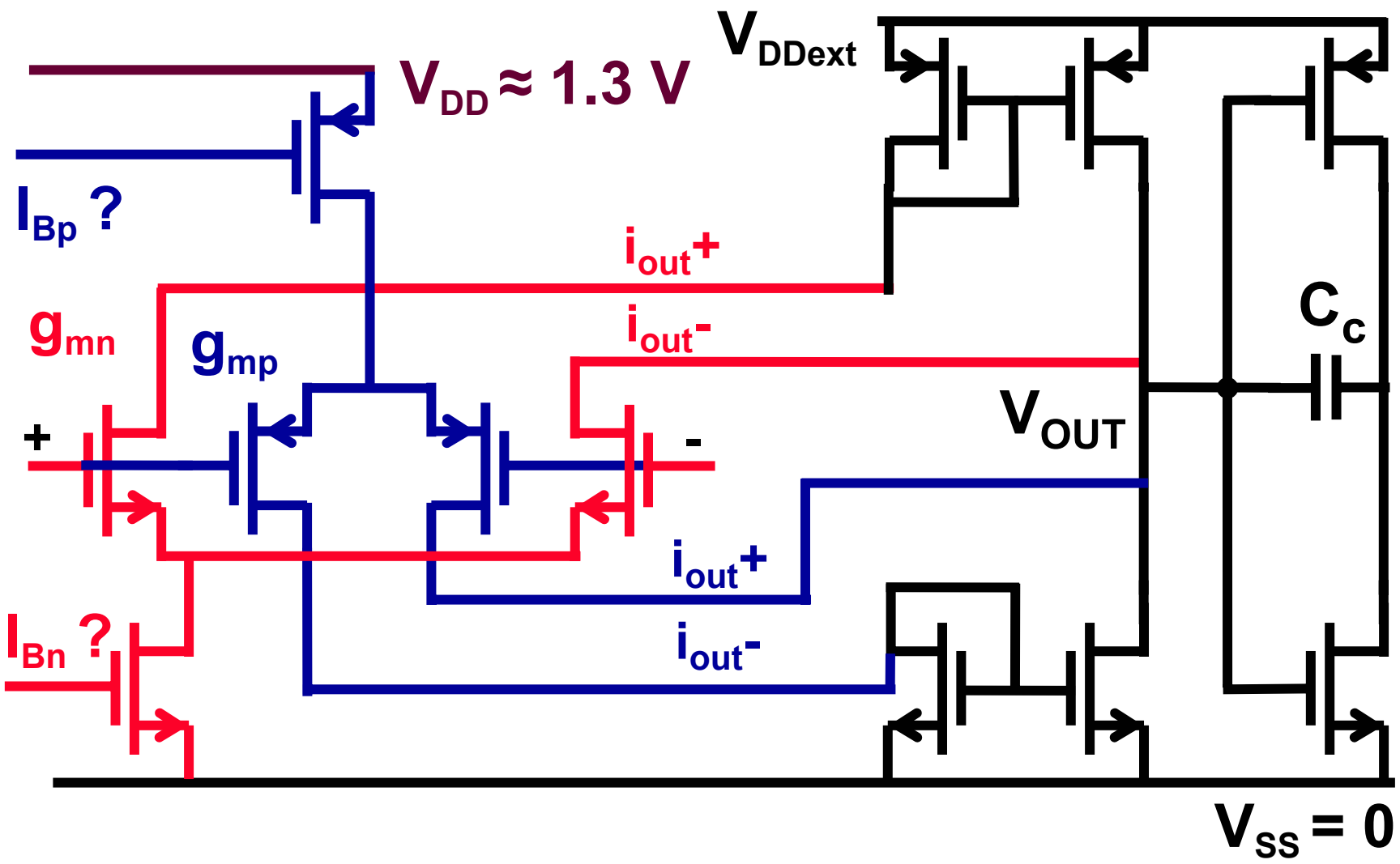
Minimum V_{DD} ?

Minimum $V_{GS}+V_{DSsat}$?

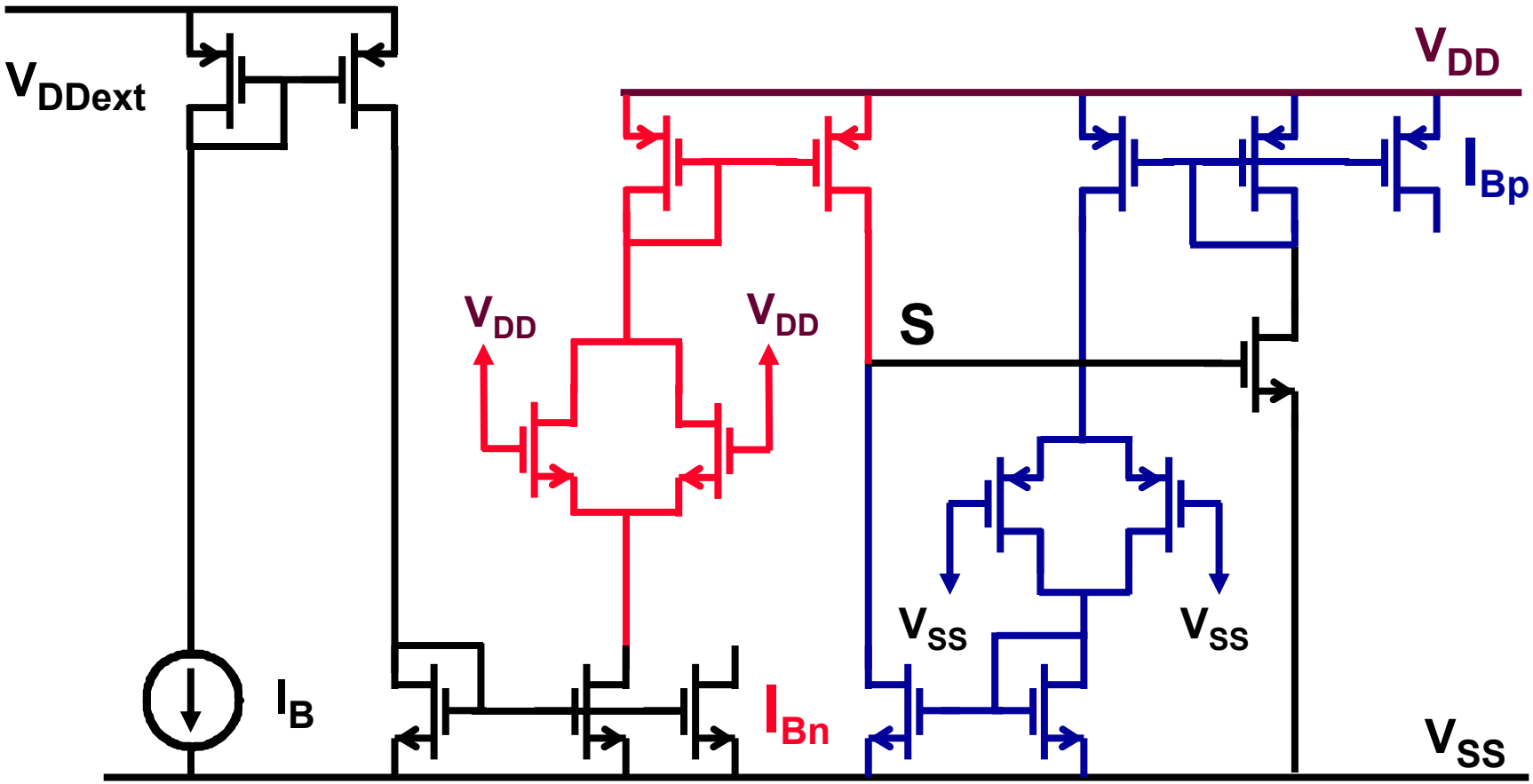
Independent of ΔV_T's !

n - mismatch and g_{mtot} dip : $\Delta g_m/g_m \approx 15\ \%$

Regulating V_{DD} : total schematic

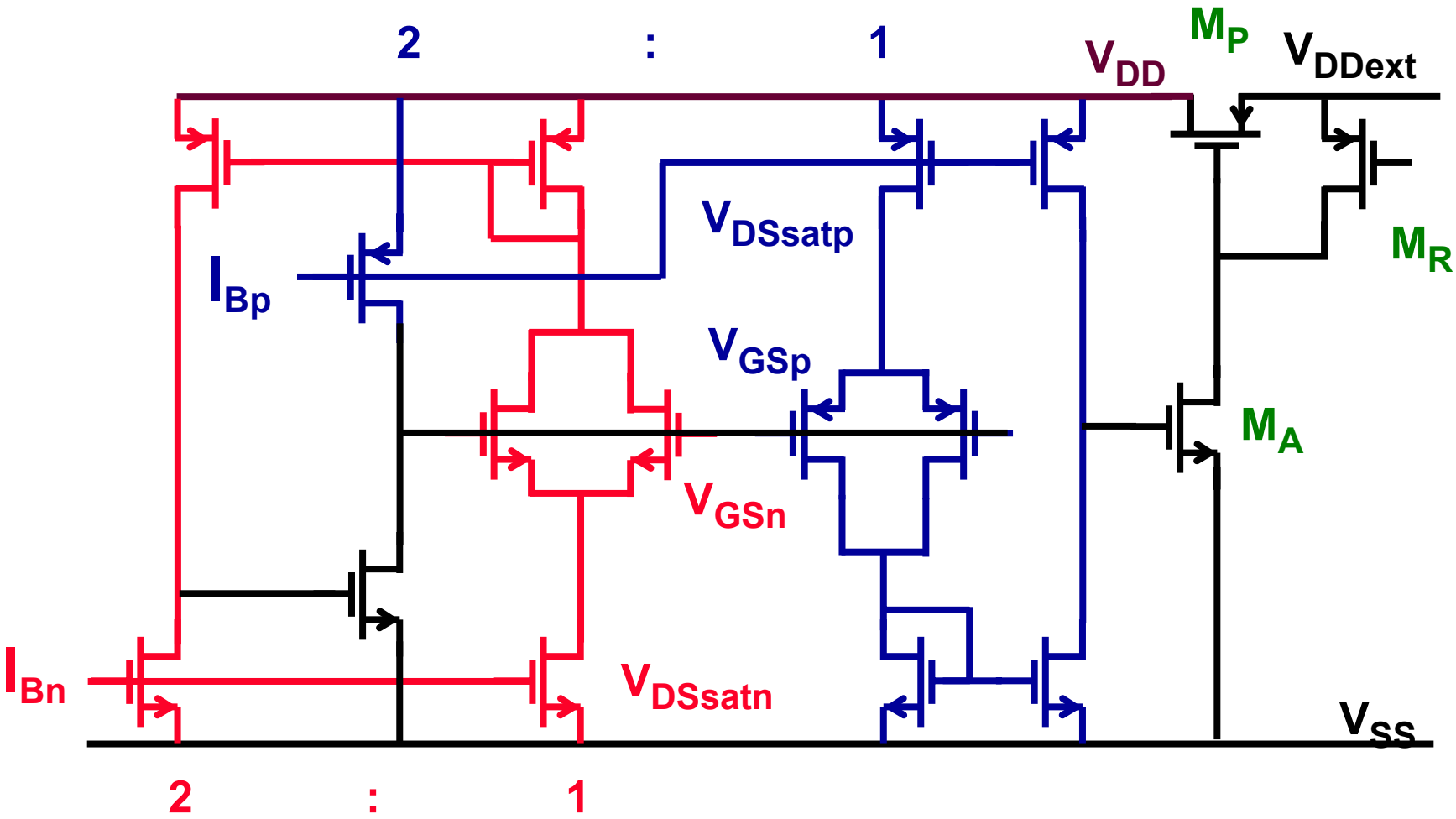


Replica biasing block

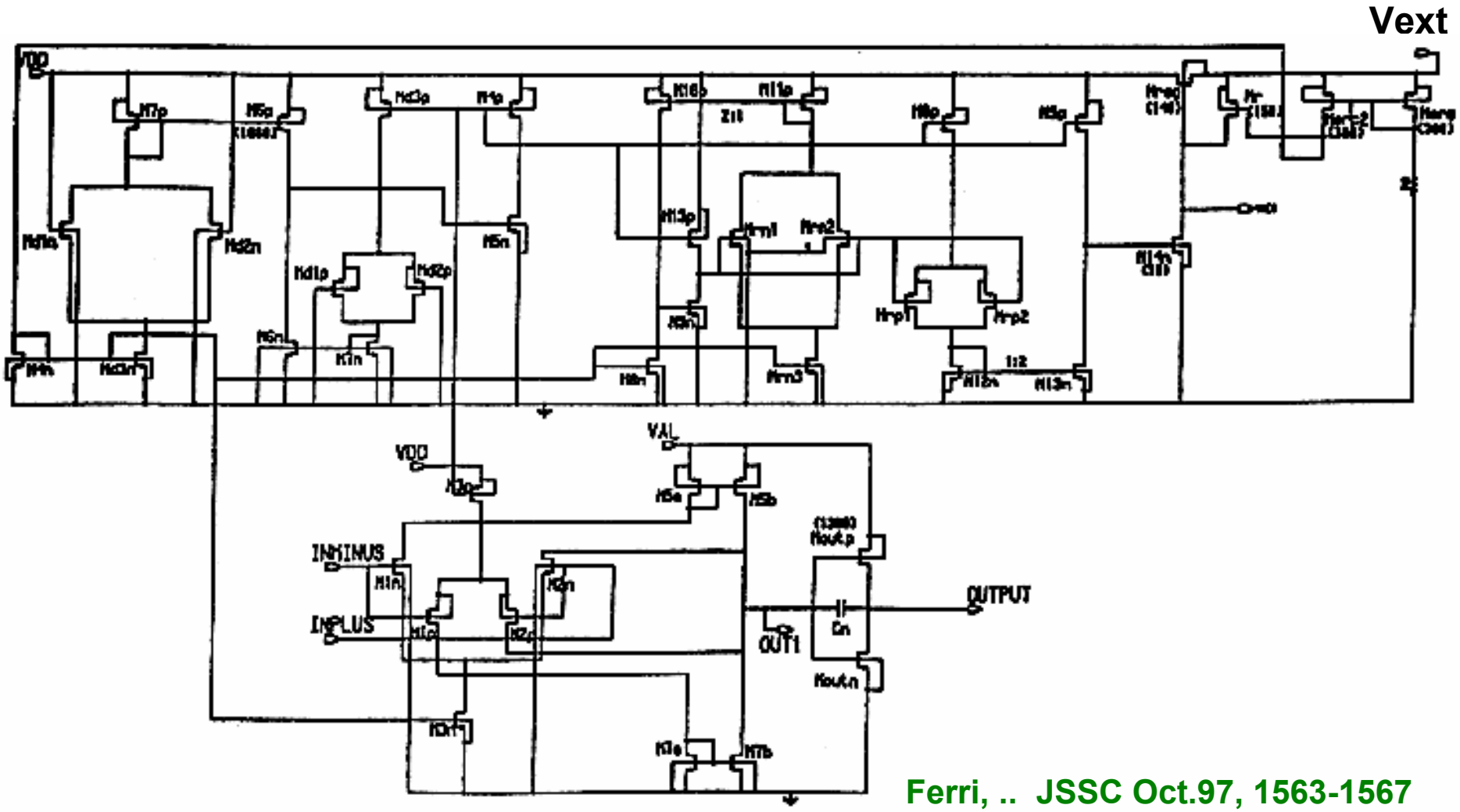


Ferri, .. JSSC Oct.97, 1563-1567

Internal V_{DD} regulator

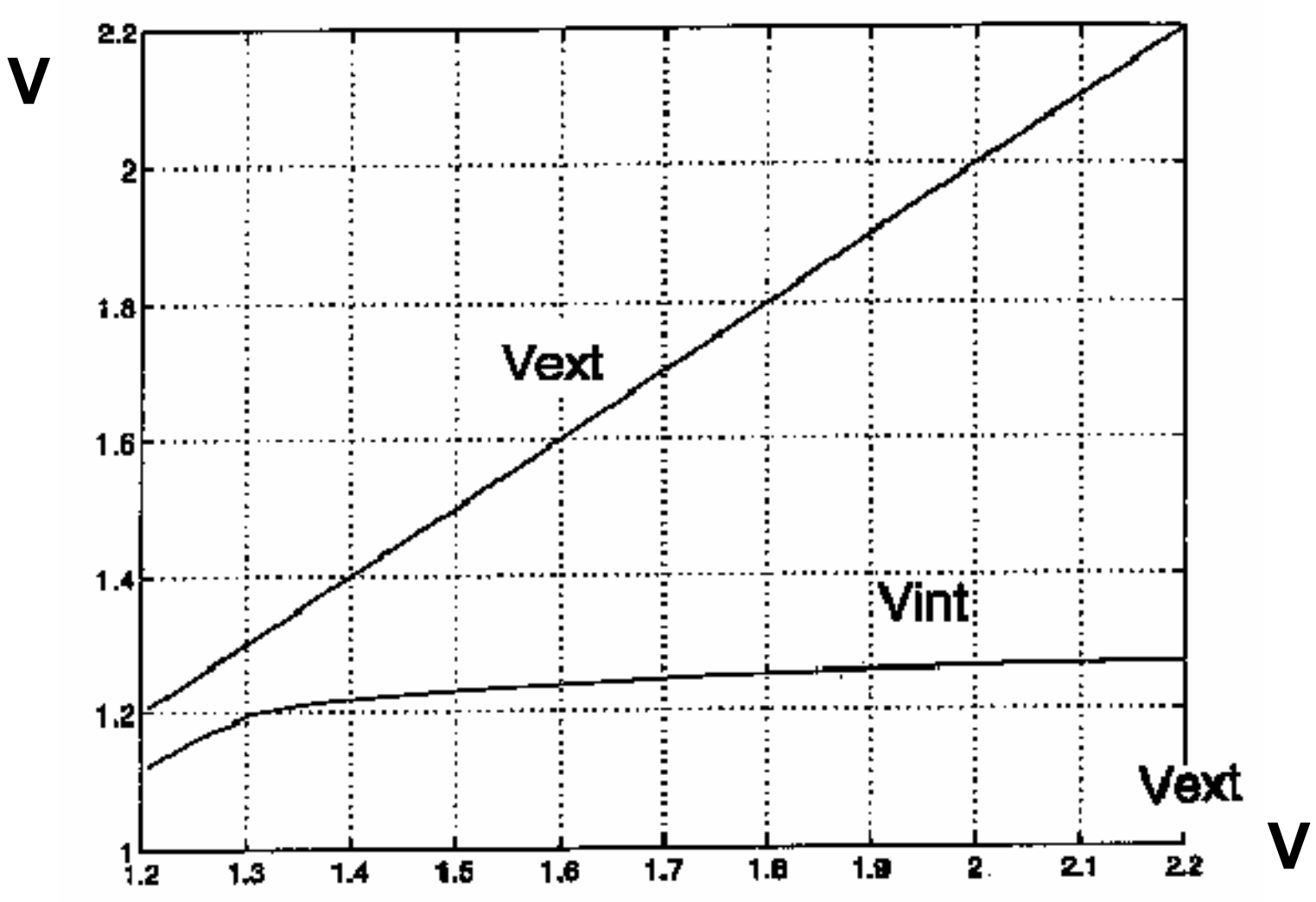


Total amplifier schematic

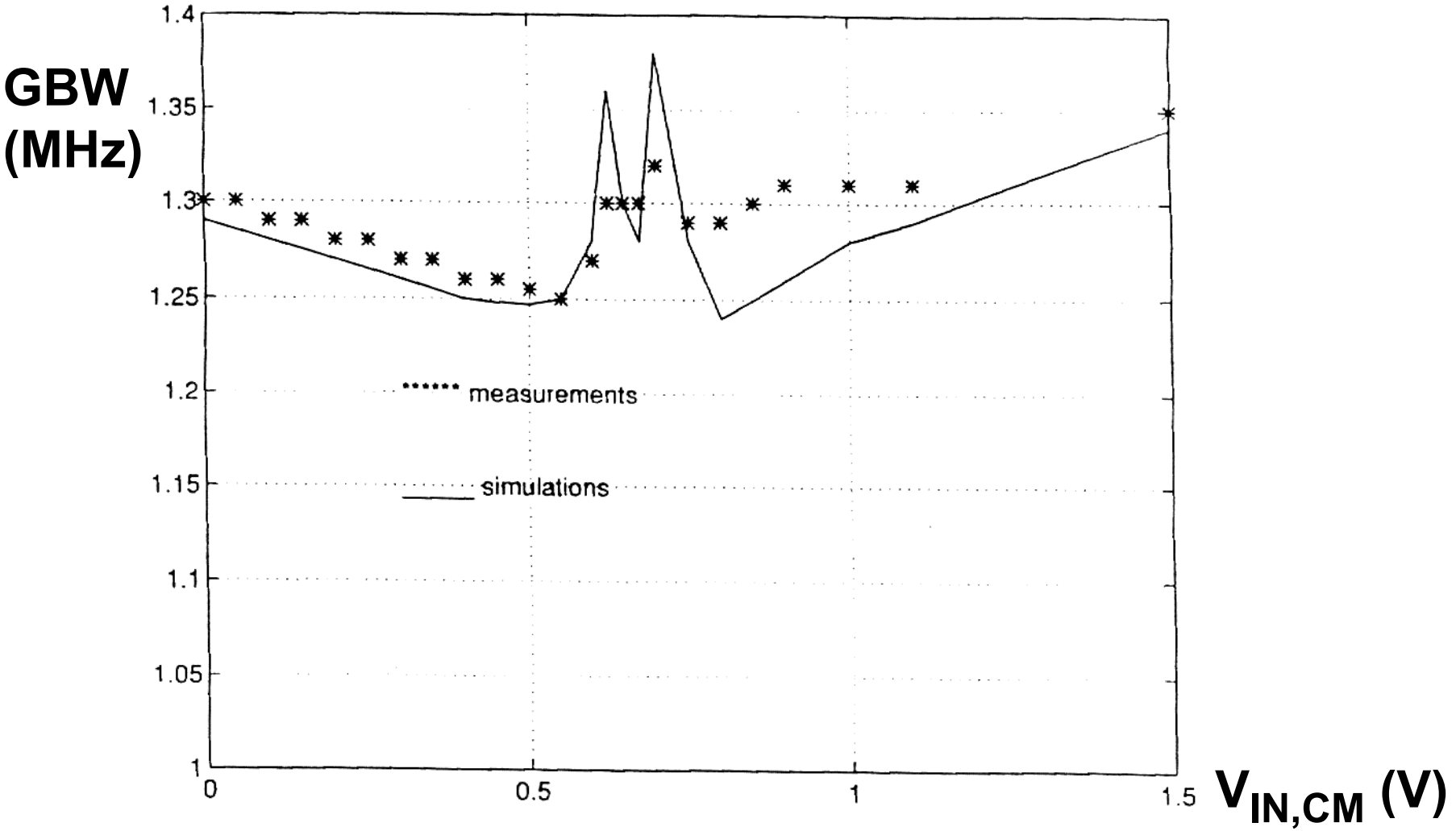


Ferri, .. JSSC Oct.97, 1563-1567

Internal supply voltage



GBW error


GBW (MHz)
1.4
1.35
1.3
1.25
1.2
1.15
1.1
1.05
1
0
0.5
1
1.5
measurements
simulations
$V_{IN,CM}$ (V)

Rail-to-rail amp. with V_{DD} regulator : Specs

V_{DDmin} = 1.3 V

GBW = 1.3 MHz in C_L = 15 pF

g_{m1} = 200 μS

I_{DSn1} = 10 μA

W/L_{in} = 830

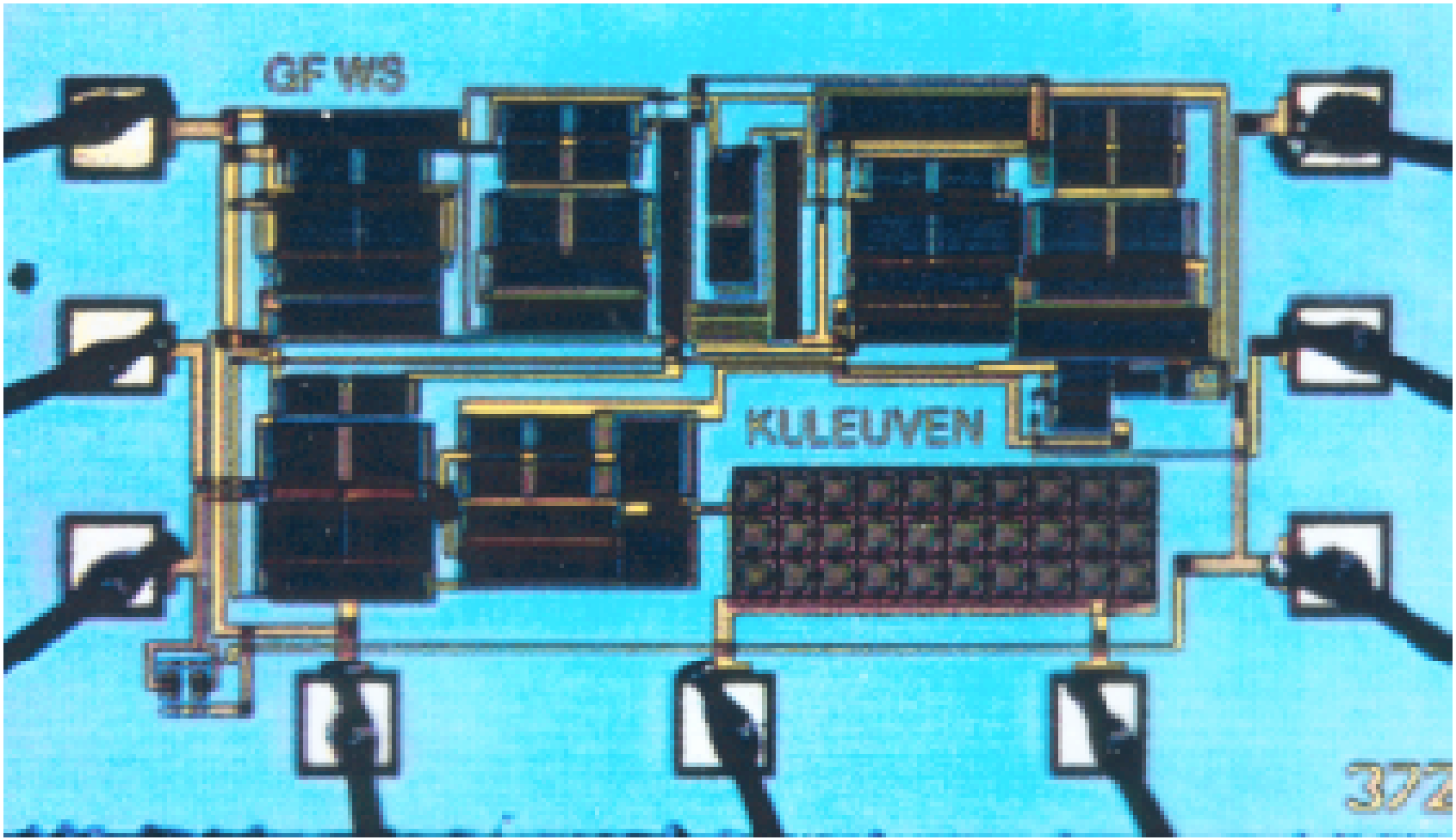
I_{TOT} = 354 μA

$V_{in,eq}$ = 25 $nV_{RMS}/\sqrt{Hz}$

$V_{in,offset}$ = 0.8 mV (3σ = 0.2 mV)

Ferri, .. JSSC Oct.97, 1563-1567

Rtr Opamp with V_{DD}-regulator



Rail-to-rail with V_{DD} regulator : min V_{DD}

$$V_{DDmin} = 2 (V_{GS} + V_{DSsat})$$

$$= 2 (V_{GS} - V_T + V_T + V_{GS} - V_T)$$

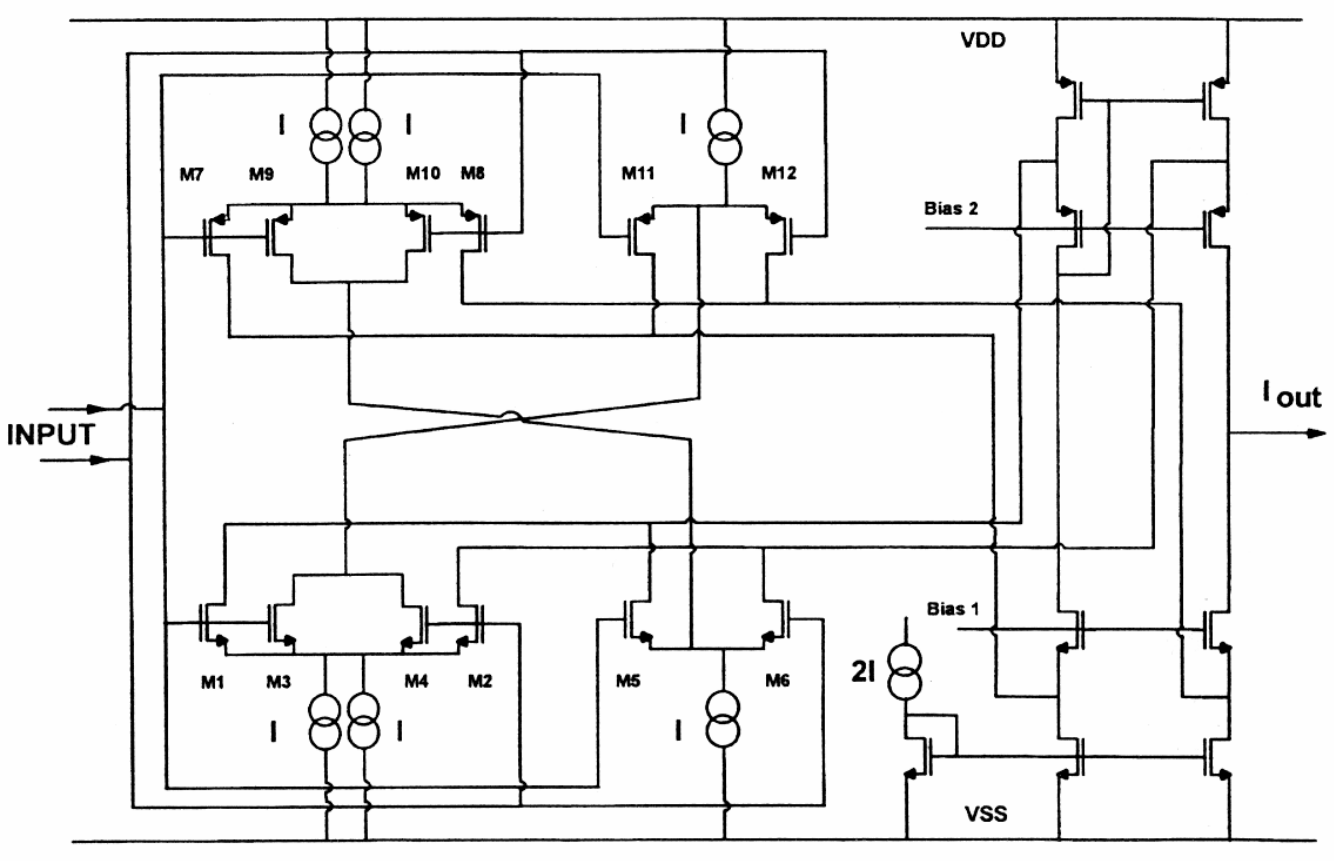
$$= 2 [V_T + 2(V_{GS} - V_T)]$$

$$= 2 [0.6 + 2(0.15)] = 1.8 \text{ V}$$

$$= 2 [0.3 + 2(0.10)] = 1.0 \text{ V} \quad !!!!$$

Table of contents

Rail-to-rail opamp with current summation



3.3 V

2.3 mW

(2.2 V min.)

Gm ± 10%

THD :

-55 dB

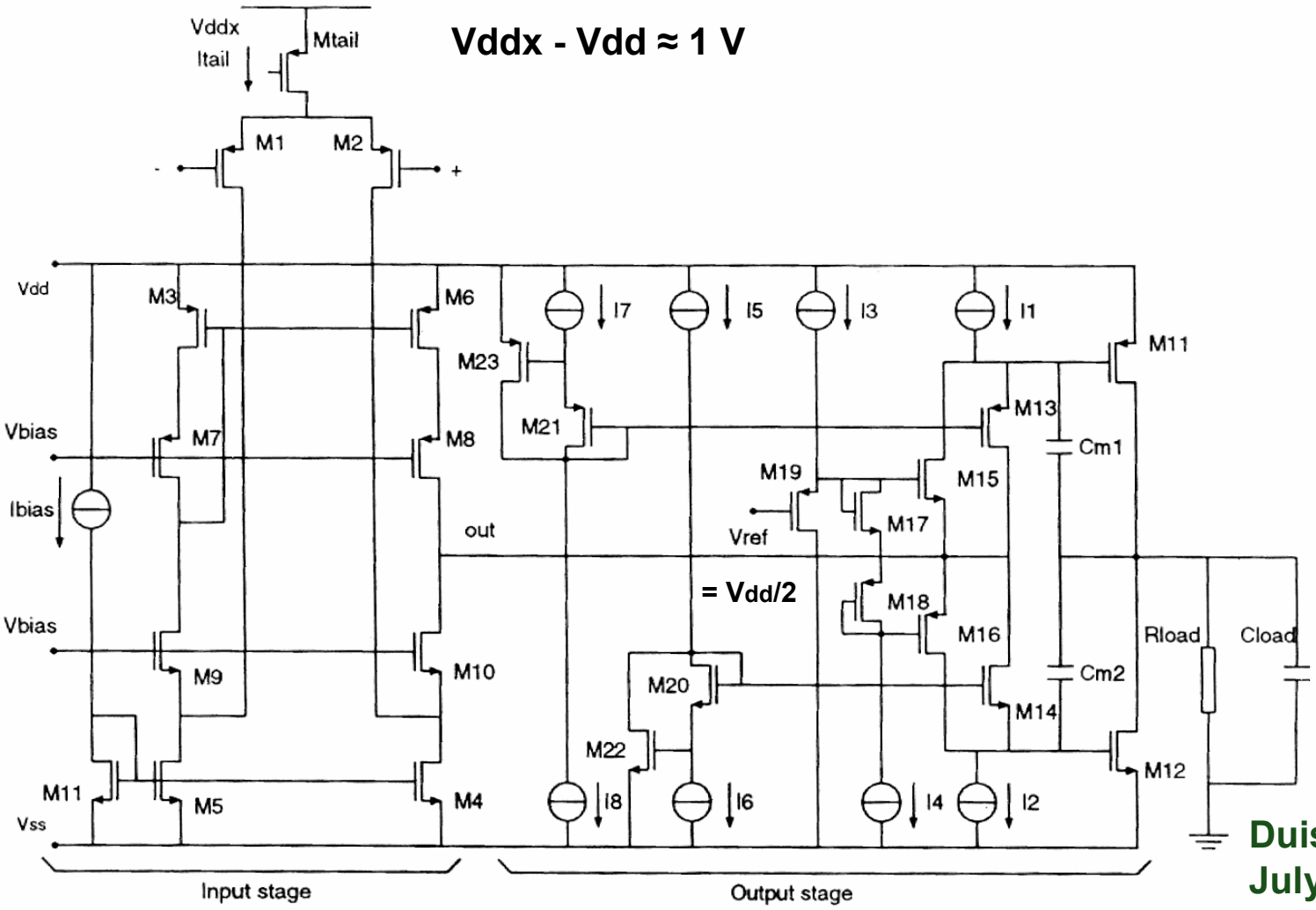
40 MHz

9 mW

0.5 μm CMOS

Redman-White, JSSC May 97, 701-712

Opamp with voltage multiplier



Vddx - Vdd ≈ 1 V

1.8 - 3.3 V

0.75 mA

6.5 MHz

On 3 V :

2.8 V_{ptpt}

THD :

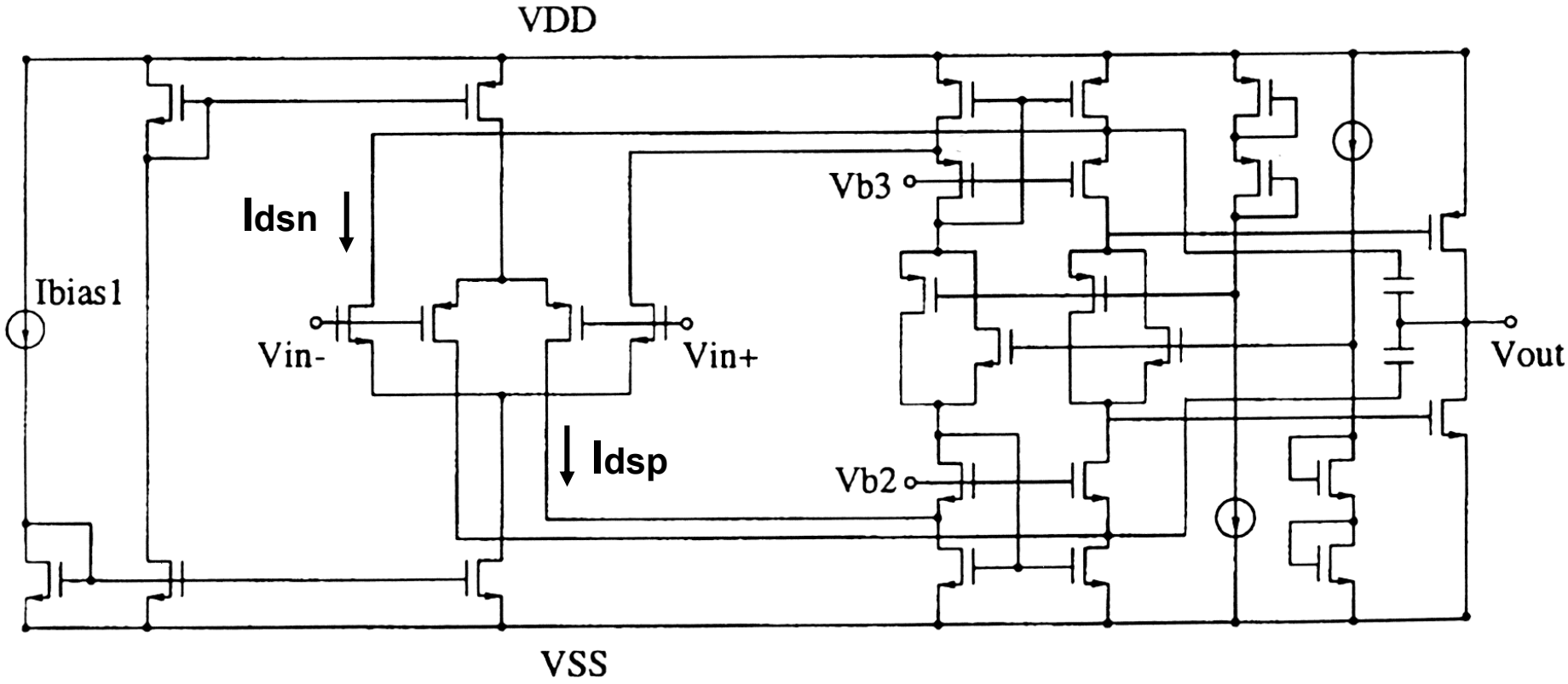
-90 dB /10kΩ

-81 dB/32 Ω

0.5 μm CMOS

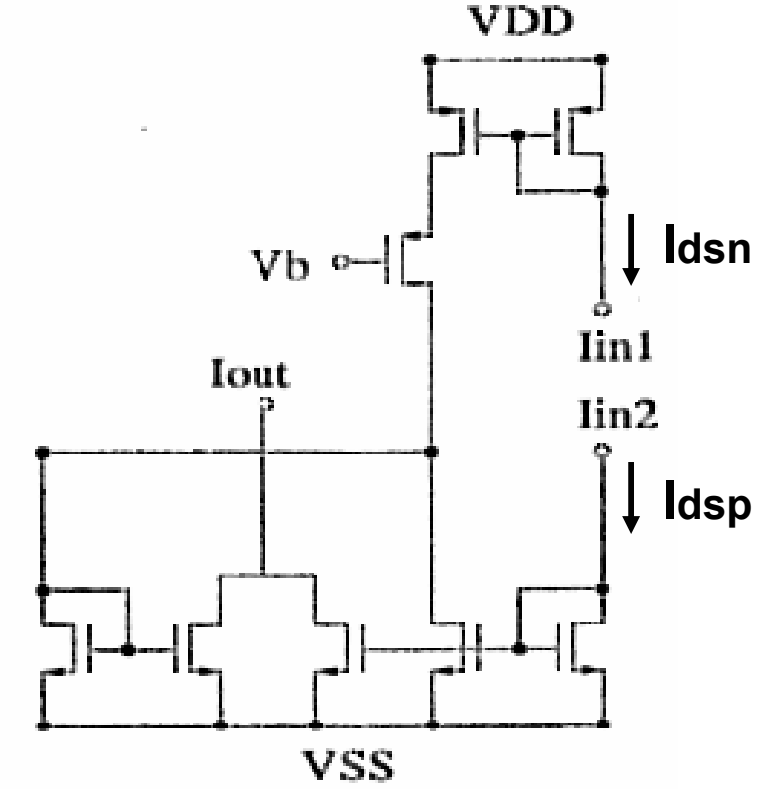
Duisters, .., JSSC July 98,pp.947-955

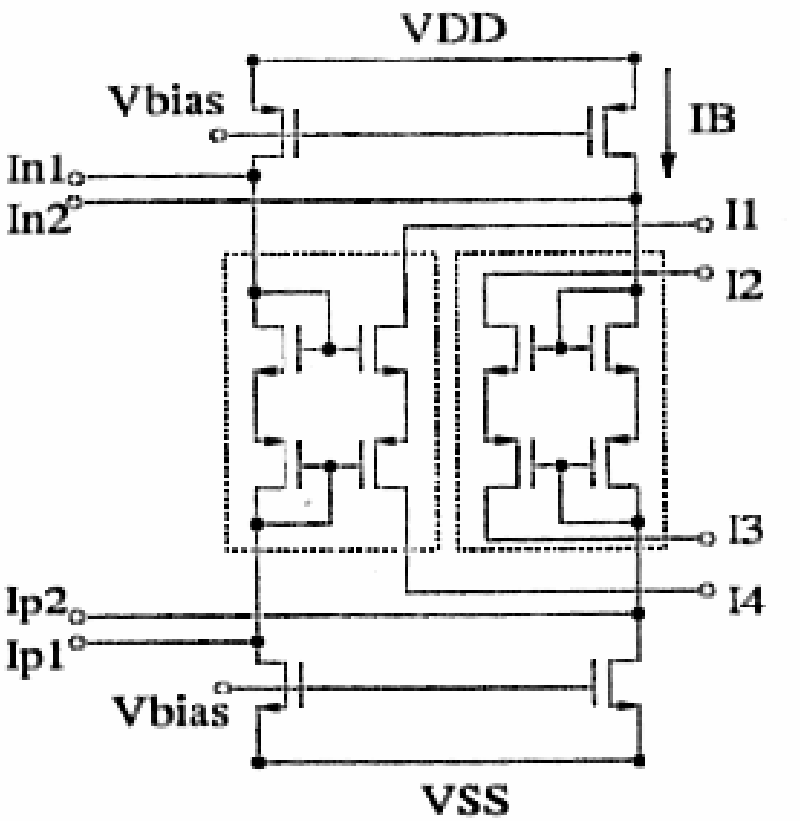
Rail-to-rail opamp with differential signal proc.



Ref.Lin, AICSP 1999, 153-162

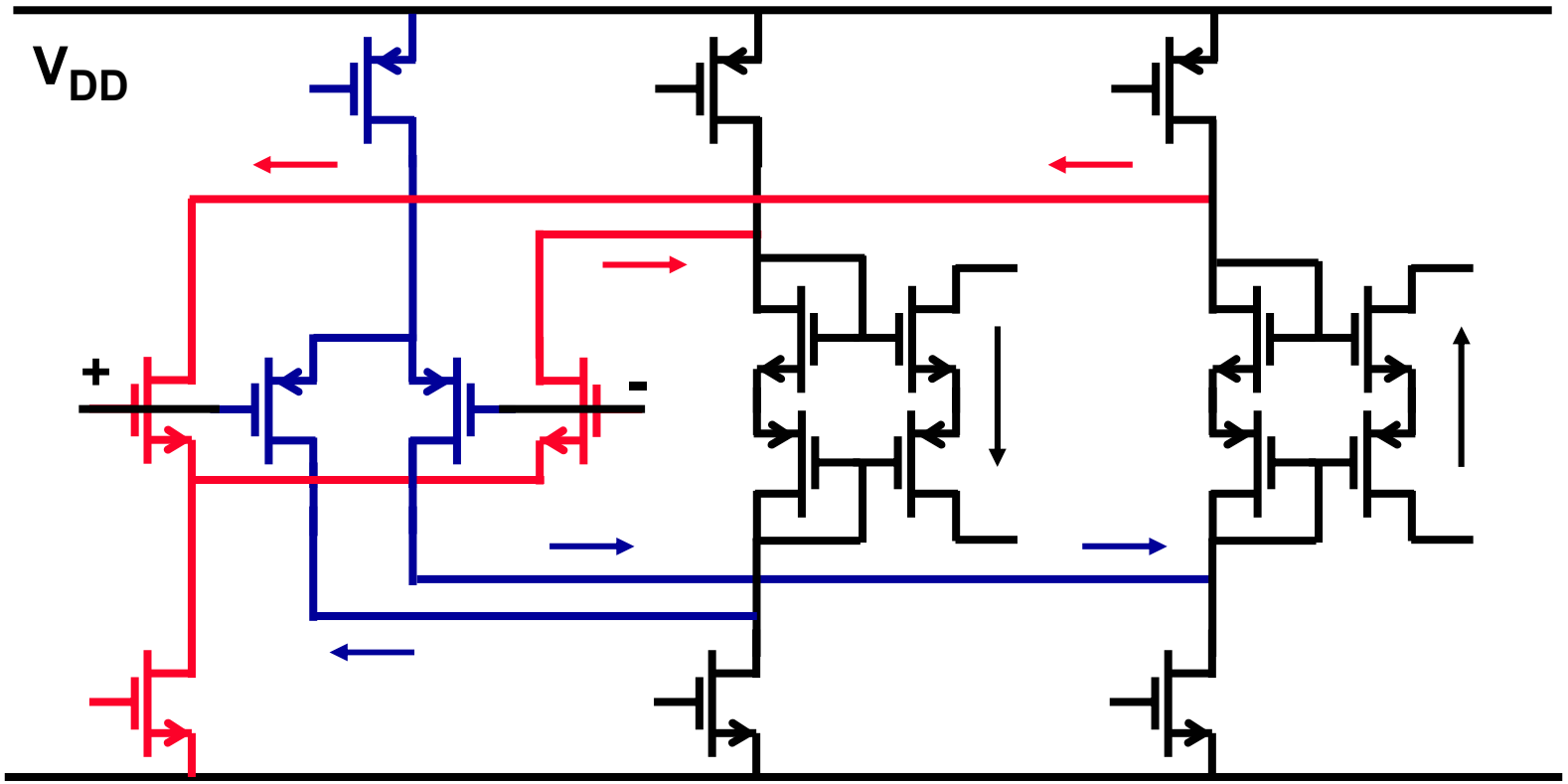
Maximum-current selecting circuits



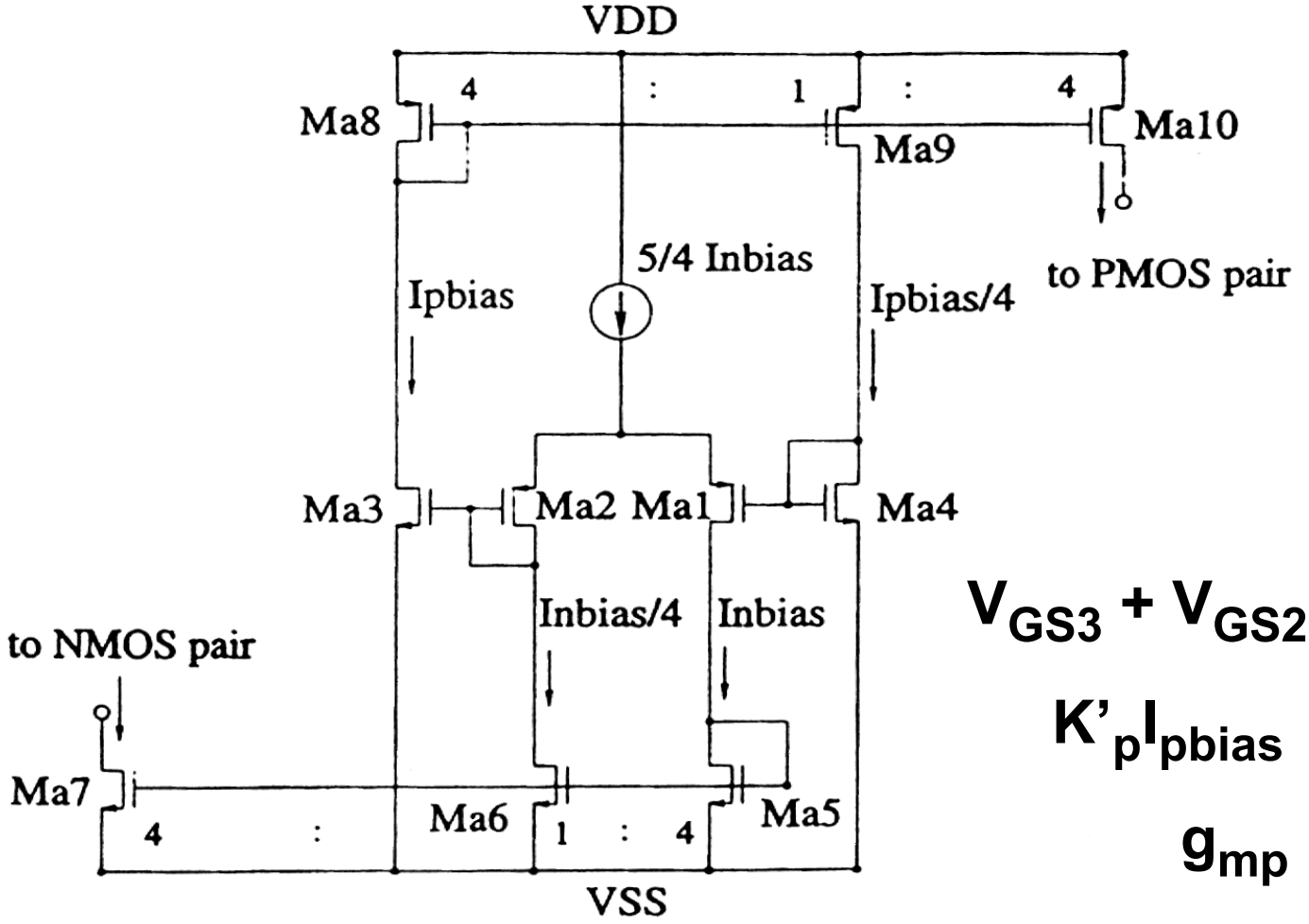


Ref.Lin, AICSP 1999, 153-162

Maximum-current selecting circuit



Transconductance equalizer circuit



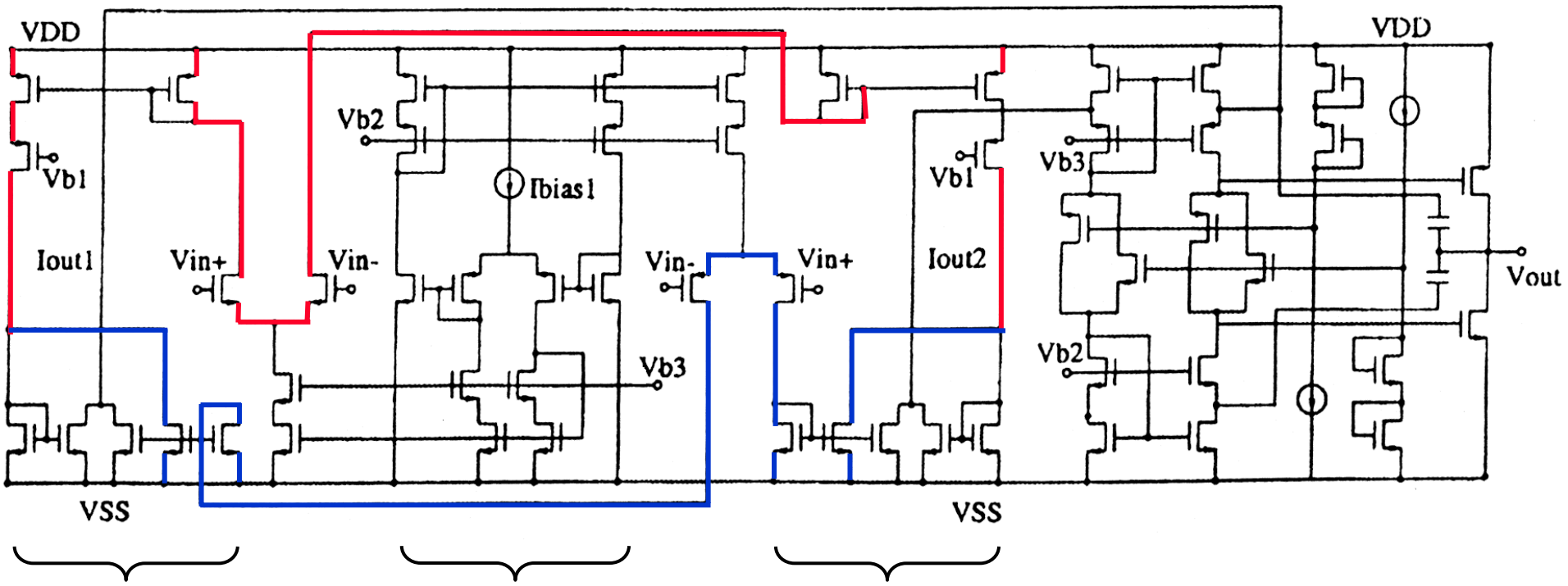
$$V_{GS3} + V_{GS2} = V_{GS1} + V_{GS4}$$

$$K'_p I_{pbias} = K'_n I_{nbias}$$

$$g_{mp} = g_{mn}$$

Ref.Lin, AICSP 1999, 153-162

Rail-to-rail opamp with max.-current selector

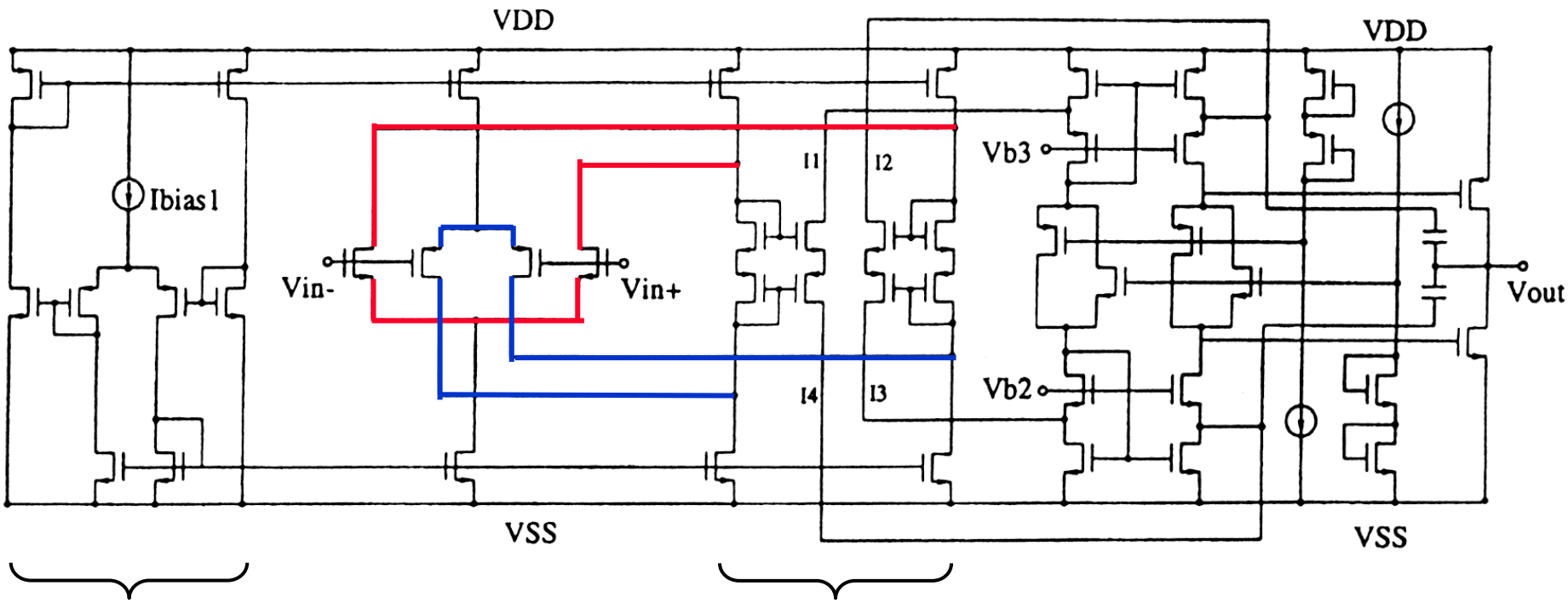


max.curr.selector g_m equalizer max.curr.selector

1.9 MHz 20 pF
3 V/ 0.26 mA

Ref.Lin, AICSP 1999, 153-162

Rail-to-rail opamp with max.-current selector



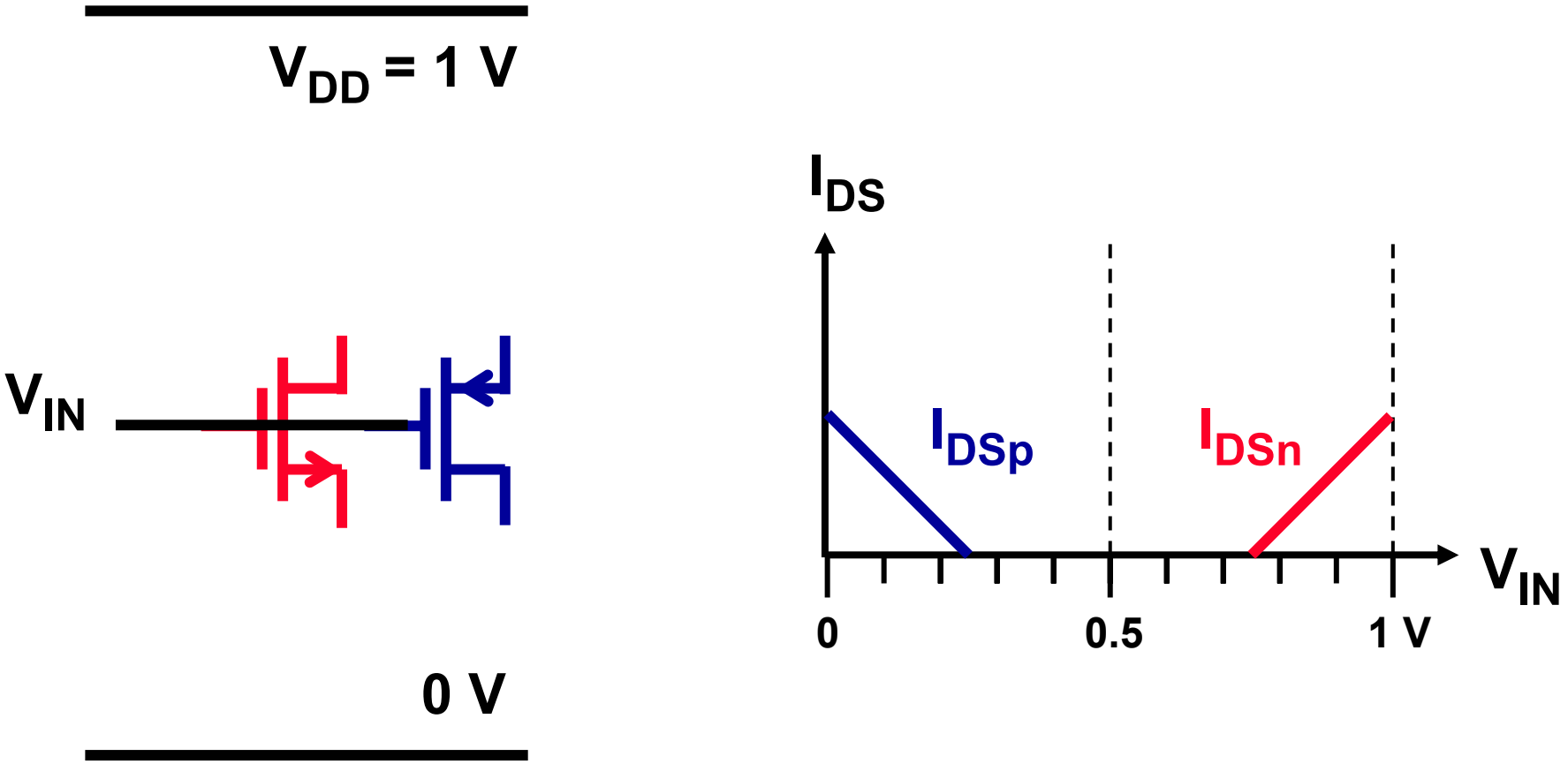
g_m equalizer

max.curr.selector

1.9 MHz 20 pF
3 V/ 0.26 mA

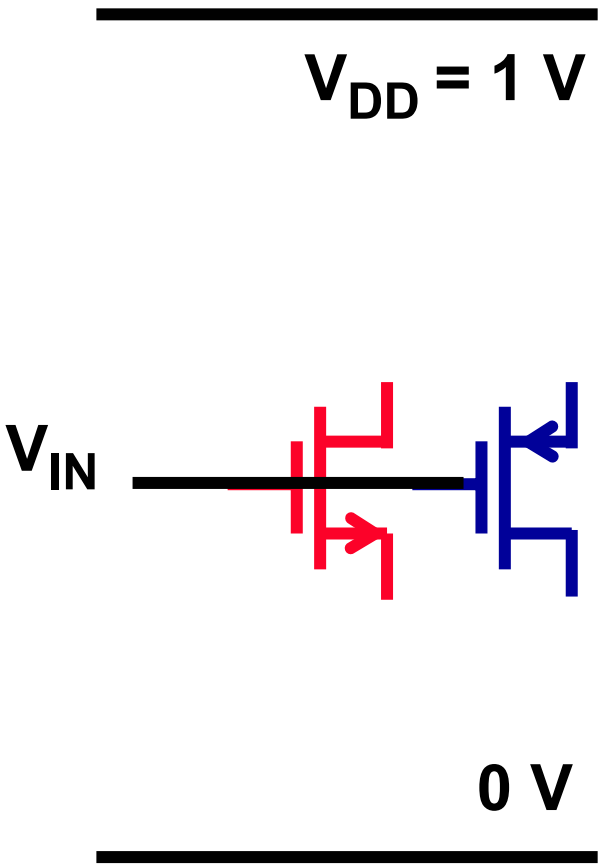
Ref.Lin, AICSP 1999, 153-162

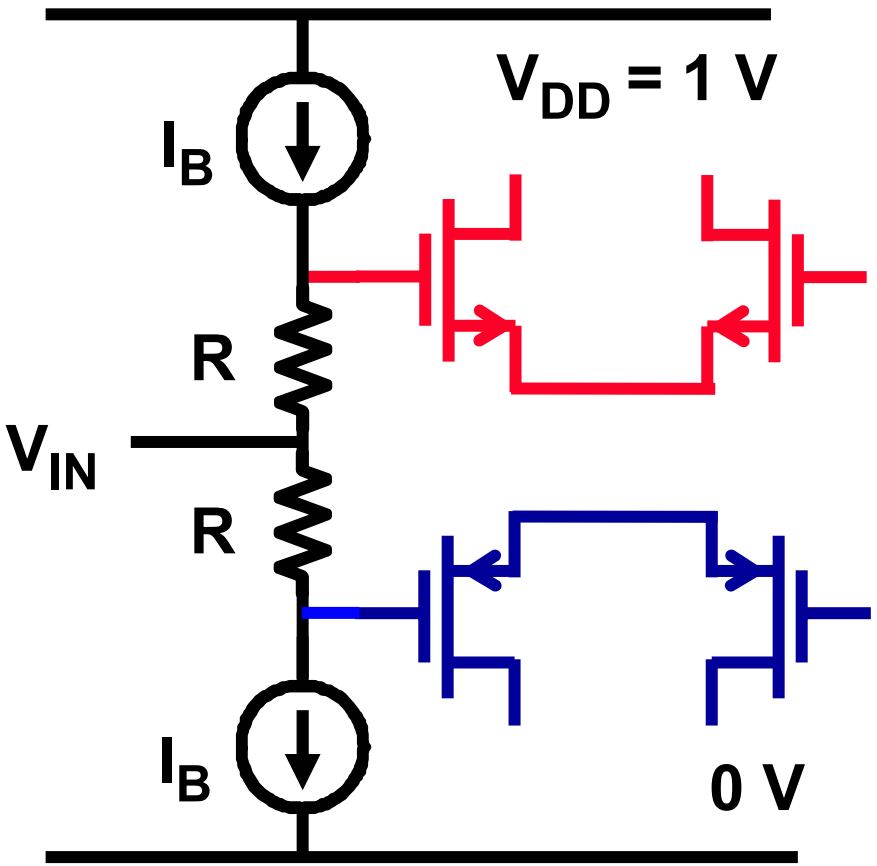
Rail-to-rail opamp on 1 Volt Supply



Ref.Duque-Carrillo, JSSC Jan.2000, 33-43

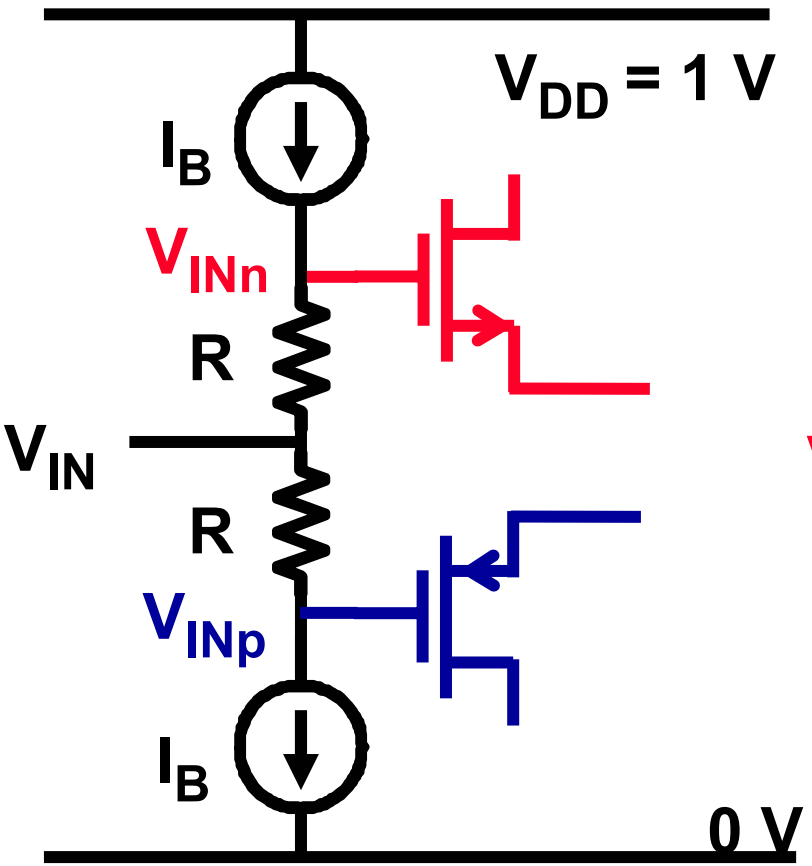
Rail-to-rail opamp on 1 Volt

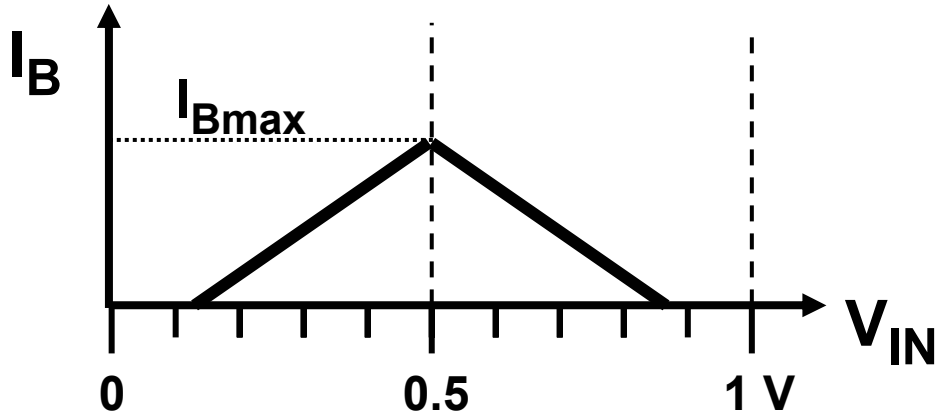


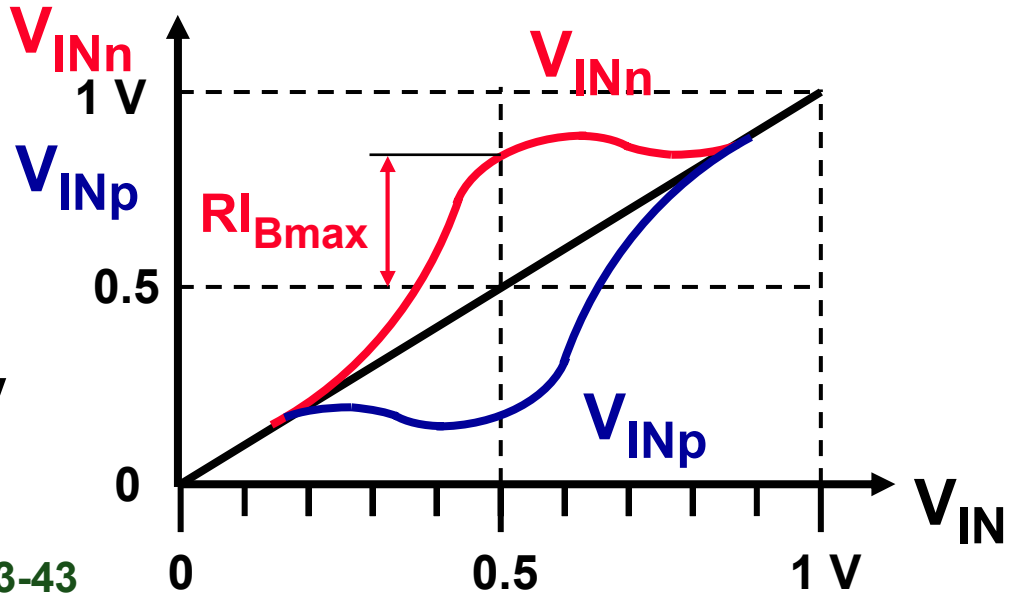


Ref.Duque-Carrillo, JSSC Jan.2000, 33-43

Rail-to-Rail opamp on 1 Volt

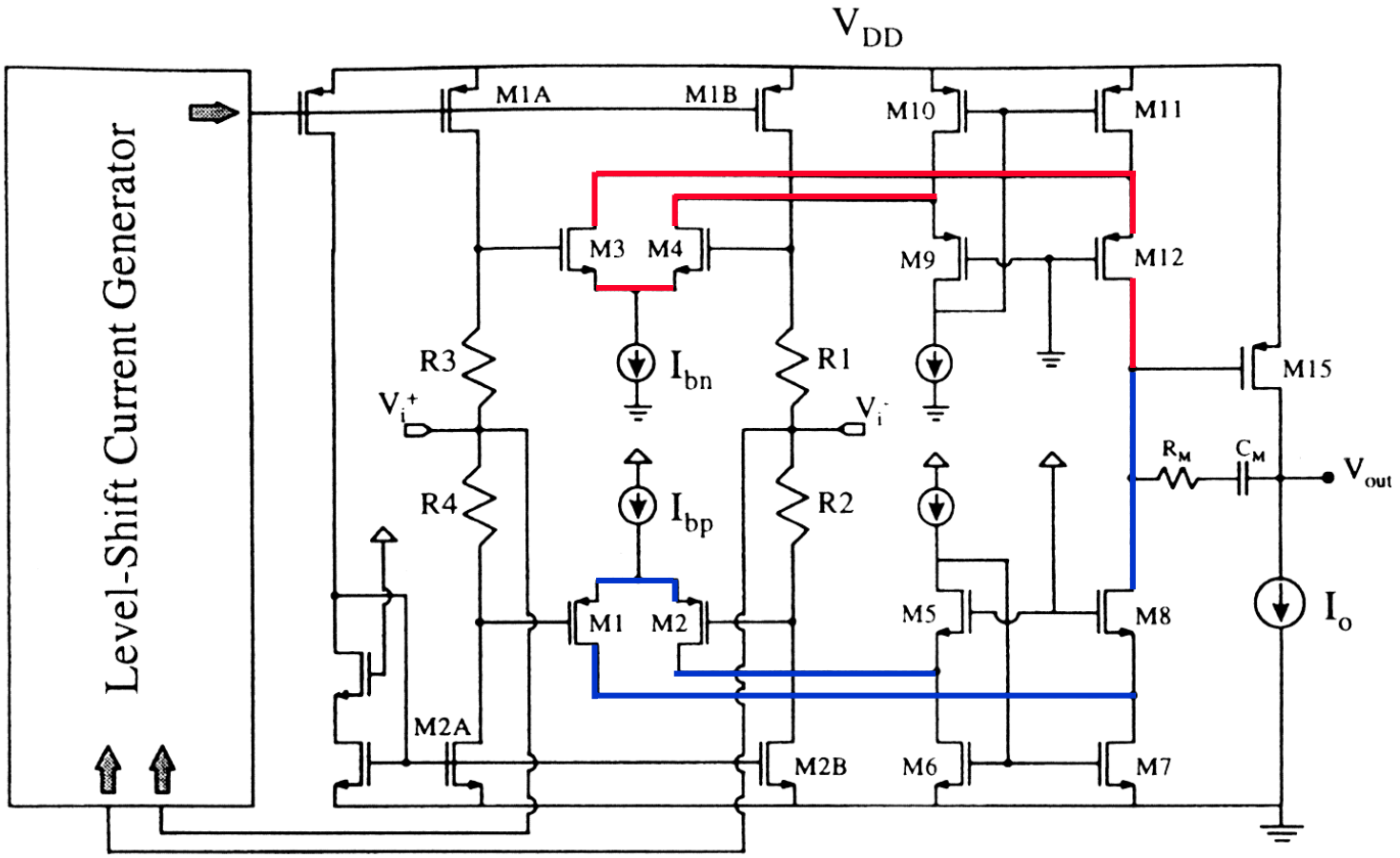






Ref.Duque-Carrillo, JSSC Jan.2000, 33-43

RtR opamp : full opamp schematic



2 MHz
15 pF

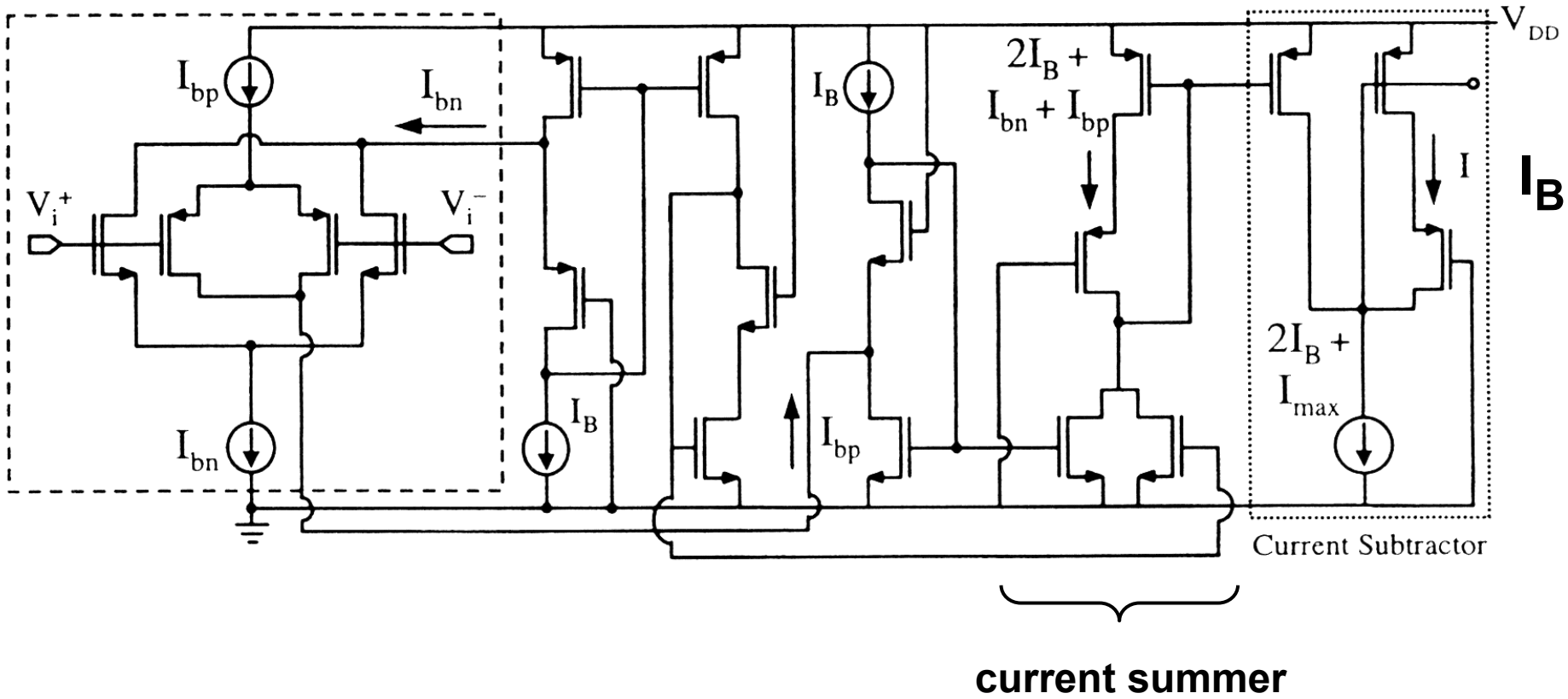
1 V
0.4 mA

I_{offset}
< 1 µA

Ref.Duque-Carrillo, JSSC Jan.2000, 33-43

R ↑ I_{offset} ↓ noise ↑

RtR opamp : current generator



Ref.Duque-Carrillo, JSSC Jan.2000, 33-43

Comparison rail-to-rail input amplifiers

Type	Ref.	$\Delta g_m/g_m$ %	GBW MHzpF/mW	I_{TOT} µA	V_{DDmin} V
3x Curr.mirr.	JSSC-12-94	15	110	150	3
Electr. Zener	JSSC-7-96	6	70	215	2.7
Curr.switch	AICSP-5-94	8	1.1	500	3.3
Curr.regulat.	CICC 97	4	210	200	1.5
Regulat. VDD	JSSC-10-97	6	43	350	1.3
MOST translin.	AICSP-6-94	8	4.2	800	2.5
Improv.CMRR	JSSC-2-95	9	3	1400	5
Max. current	AICSP-1-99	10	77	260	3
Resistive input	JSSC-1-00	x	75	400	1

Table of contents

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G.Ferri, W.Sansen, ”A rail-to-rail constant-gm low-voltage CMOS operational transconductance amplifier", IEEE Journal Solid-State Circuits, Vol. SC-32, pp. 1563-1567, Oct.1997.

R. Hogervorst, etal, "A compact power-efficient 3V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries", IEEE Journal Solid-State Circuits, Vol. SC-29, pp. 1504-1512, Dec.1994.

R. Hogervorst, etal, ”Compact CMOS constant-gm rail-to-rail input stage with gm-control by an electronic Zener diode", IEEE Journal Solid-State Circuits, Vol. SC-31, pp. 1035-1040, July 1996.

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