

CMOS 模拟集成电路设计

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Je reviendrai et je serai des millions. ——«Spartacus»

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第一部分

课件

第1章 MOSFET



北京航空航天大學
BEIHANG UNIVERSITY

| 微电子学院

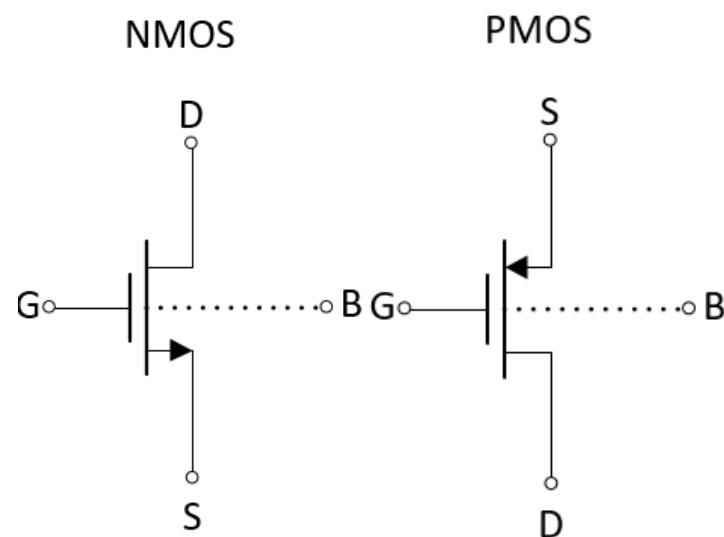
CMOS模拟集成电路设计

第一章：MOSFET

胡远奇

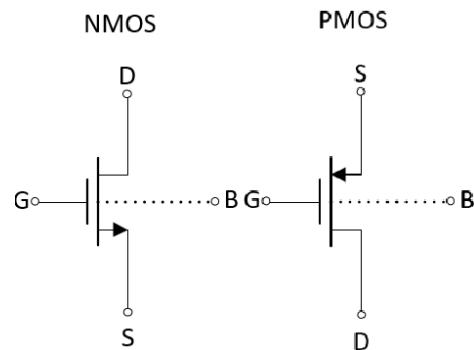
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»» MOSFET



Id=?

》》 MOSFET



线性区

vs

饱和区



如何选择?

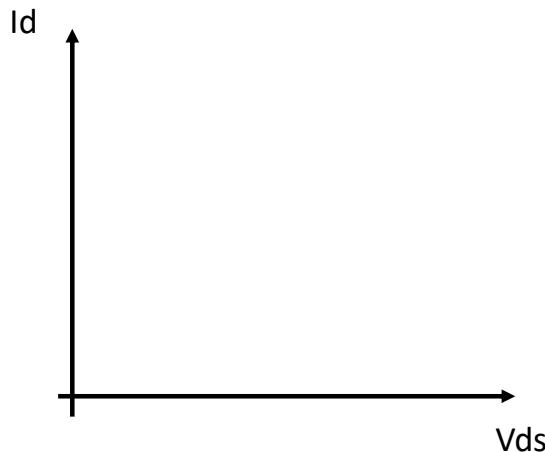
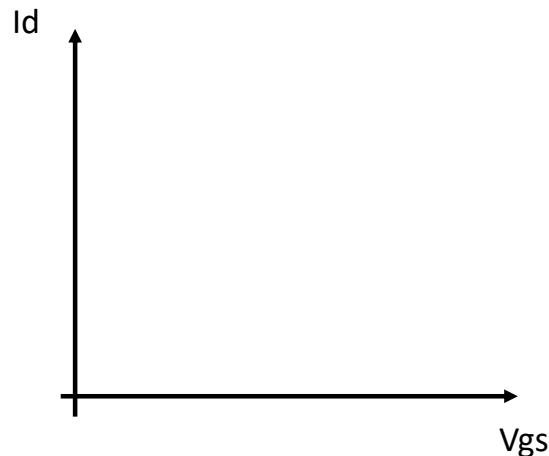
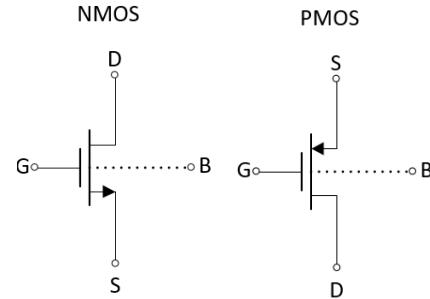


开关、电阻

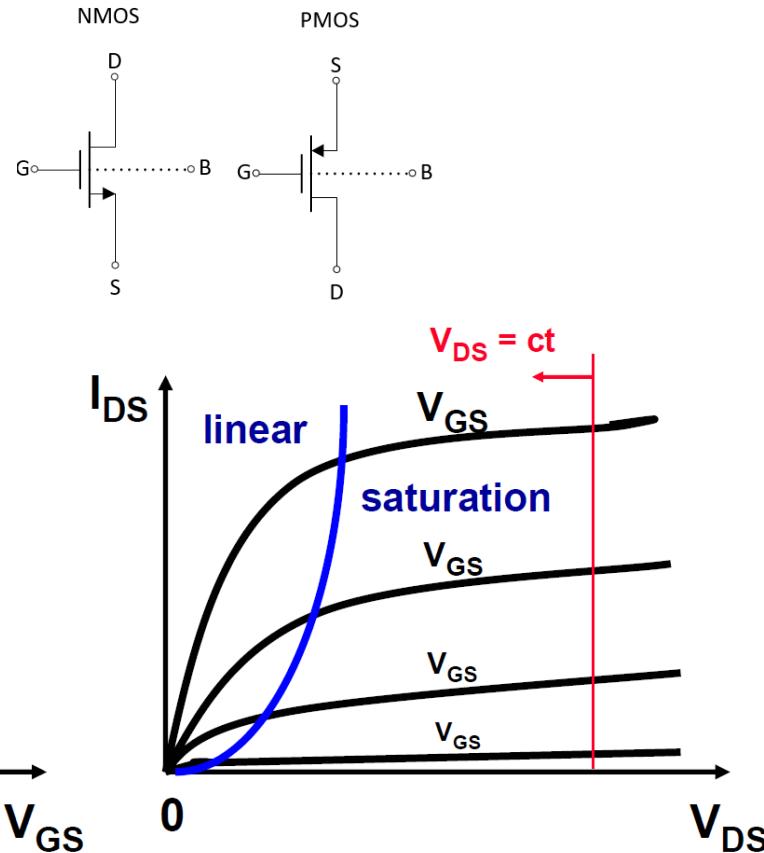
放大器



MOSFET的I-V关系



»» MOSFET的I-V关系





MOSFET

- 晶体管工作在线性区：电阻
- 晶体管工作在饱和区：放大器
- 亚反型区/弱翻转区 (Weak Inversion)
- 速度饱和区 (Velocity Saturation)
- 特征频率

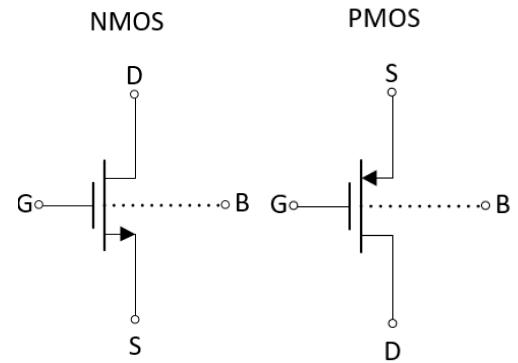
»» MOSFET当作开关

线性区: $V_{DS} < V_{GS} - V_{TH}$

$$I_D =$$

- 小信号导通电阻:

$$R =$$



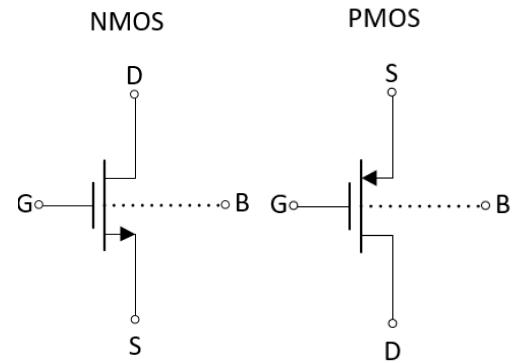
》》 MOSFET当作开关

线性区: $V_{DS} < V_{GS} - V_{TH}$

$$I_D = \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}$$

- 小信号导通电阻:

$$R \approx \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \quad \text{for } V_{GS} - V_{TH} \gg V_{DS}$$



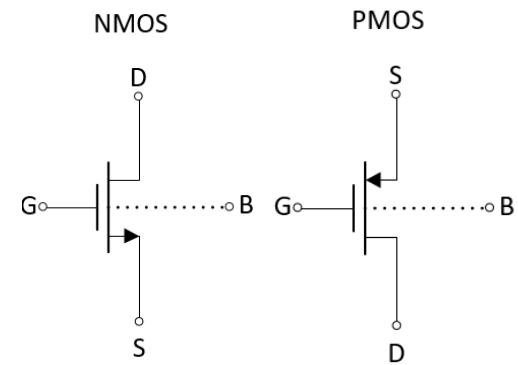
»» MOSFET参数

$$R \approx \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

- 电子迁移率 μ : $\mu_p \approx 250 \text{ cm}^2/\text{Vs}$

$$\mu_n \approx 600 \text{ cm}^2/\text{Vs}$$

- 栅氧层电容 C_{ox} : $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

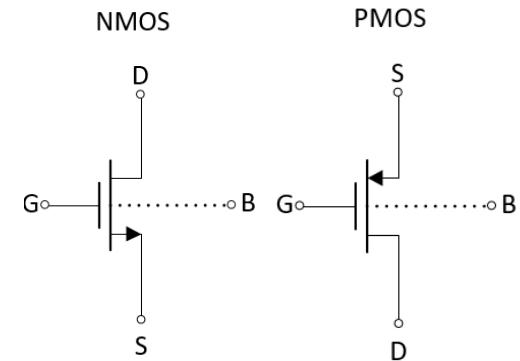


»» MOSFET参数

L_{min} = 0.35 μm

- 电子迁移率 μ : $\mu_p \approx 250 \text{ cm}^2/\text{Vs}$
 $\mu_n \approx 600 \text{ cm}^2/\text{Vs}$
- 棚氧层电容 C_{ox} : $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \approx 5 \cdot 10^{-7} \text{ F/cm}^2$

KP_n ≈ 300 μA/V²





MOSFET电阻快速估算

$$L_{min} = 0.35 \mu m \quad K_P n \approx 300 \mu A/V^2$$

$$R \approx \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

- 对于0.35um工艺方块NMOS晶体管，在 $V_{GS}-V_{TH}=1V$ 的驱动电压下，其电阻约为：

3.4KΩ



MOSFET电阻快速估算

已知0.35um工艺方块NMOS晶体管，在 $V_{GS}-V_{TH}=1V$ 的驱动电压下，其电阻约为3.4Kohm，请估算电阻值：

1. 0.35um工艺方块PMOS晶体管， $V_{GS}-V_{TH}=1V$ **8.16KΩ**

2. 0.18um工艺方块NMOS晶体管， $V_{GS}-V_{TH}=1V$ **1.75KΩ**

$$\mu_p \approx 250 \text{ cm}^2/\text{Vs}$$

$$\mu_n \approx 600 \text{ cm}^2/\text{Vs}$$

$$t_{ox} = \frac{L_{min}}{50}$$



MOSFET

- 晶体管工作在线性区：电阻
- **晶体管工作在饱和区：放大器**
- 亚反型区/弱翻转区 (Weak Inversion)
- 速度饱和区 (Velocity Saturation)
- 特征频率



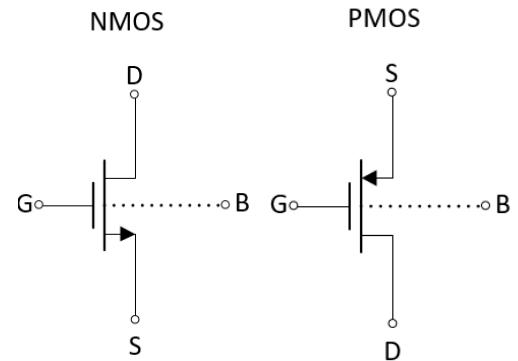
MOSFET当作放大器

饱和区： $V_{DS} > V_{GS} - V_{TH}$

$$I_D =$$

- 小信号跨导：

$$g_m \approx$$





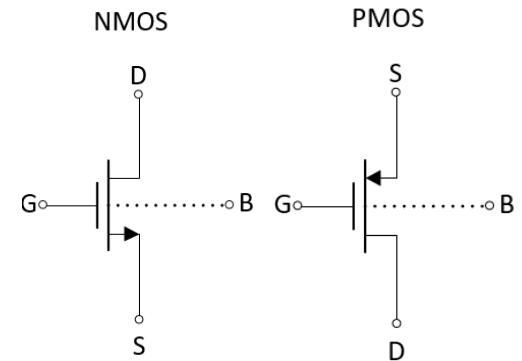
MOSFET当作放大器

饱和区: $V_{DS} > V_{GS} - V_{TH}$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

- 小信号跨导:

$$g_m \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DS}} = \frac{2I_{DS}}{V_{GS} - V_{TH}}$$



》》 晶体管跨导gm

$$g_m \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DS}} = \frac{2I_{DS}}{V_{GS} - V_{TH}}$$

问：小信号跨导 g_m 与 I_{DS} 的关系？

$$g_m \propto \sqrt{I_{DS}}$$



测试中尺寸固定

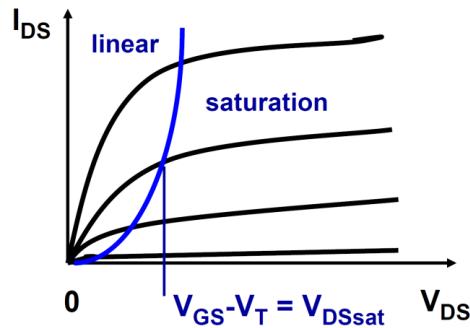
VS

$$g_m \propto I_{DS}$$



设计中偏置固定

》》 输出电阻 r_0

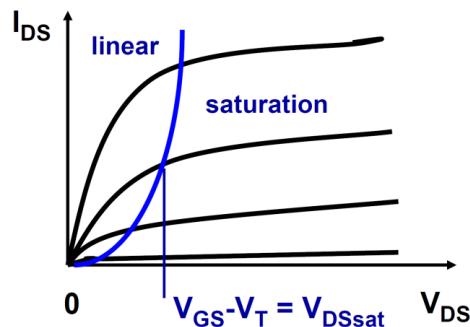


$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

- 输出电阻：

$$r_0 =$$

》》 输出电阻 r_0



$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

- 输出电阻：

$$r_0 \approx \frac{1}{\lambda I_{DS}} = \frac{V_E \cdot L}{I_{DS}}$$



$$V_{En} = 4 \text{ V}/\mu\text{mL}$$

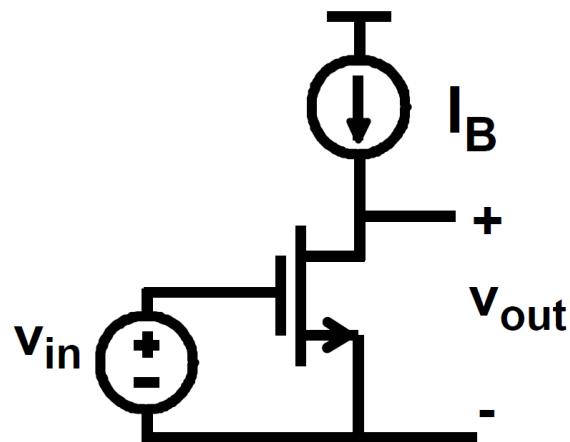
$$L = 1 \text{ } \mu\text{m}$$

$$I_{DS} = 100 \text{ } \mu\text{A}$$

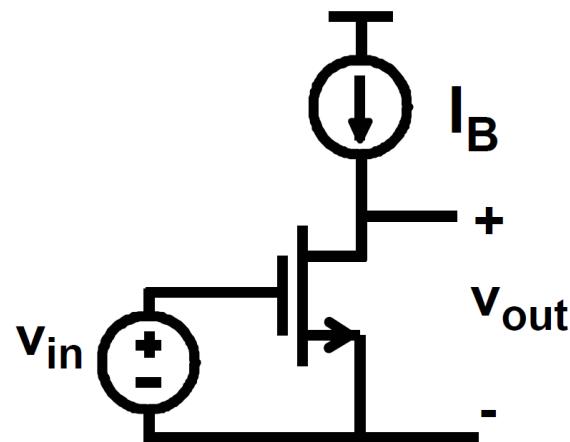
$$r_0 = 40 \text{ k}\Omega$$



单晶体管放大器



》》 单晶体管放大器



$$A_v = g_m r_{DS} = \frac{2 V_E L}{V_{GS} - V_T}$$

$$A_v \approx 100$$

If $V_E L \approx 10 \text{ V}$
and $V_{GS} - V_T \approx 0.2 \text{ V}$

》》运放设计Trade-off

$$g_m \approx \frac{2I_{DS}}{V_{GS} - V_{TH}}$$

$$A = \frac{2 \cdot V_E \cdot L}{V_{GS} - V_{TH}}$$

	高增益	高速
$V_{GS} - V_{TH}$		
L		

》》运放设计Trade-off

$$g_m \approx \frac{2I_{DS}}{V_{GS} - V_{TH}}$$

$$A = \frac{2 \cdot V_E \cdot L}{V_{GS} - V_{TH}}$$

	高增益	高速
$V_{GS} - V_{TH}$	↓	↑
L	↑	↓



MOSFET

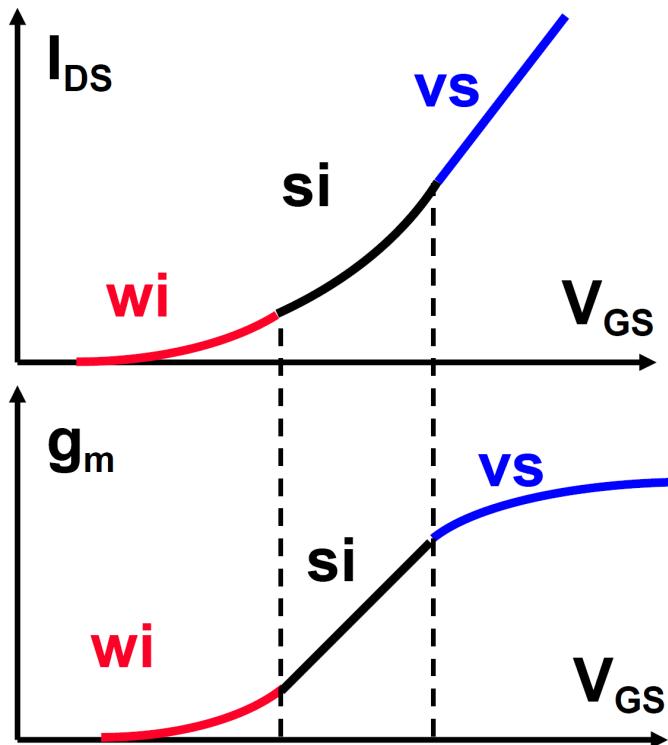
- 晶体管工作在线性区：电阻
- 晶体管工作在饱和区：放大器
- **亚反型区/弱翻转区 (Weak Inversion)**
- 速度饱和去 (Velocity Saturation)
- 特征频率

》》弱反型区和速度饱和区

- 假设晶体管始终工作在饱和区： $V_{DS} > V_{GS} - V_{TH}$



》》 弱反型区 (weak inversion)



- 弱反型区:

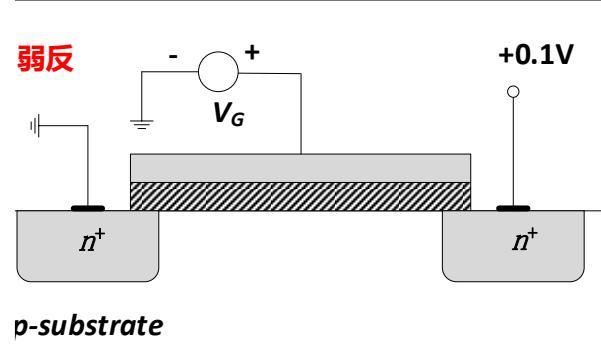
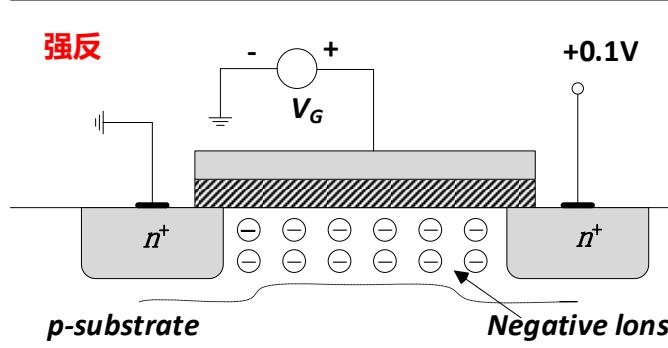
$$I_{D,wi} = I_{D0} \frac{W}{L} e^{\frac{V_{GS}}{nkT/q}}$$

$$g_{m,wi} = \frac{I_{D,wi}}{nkT/q}$$



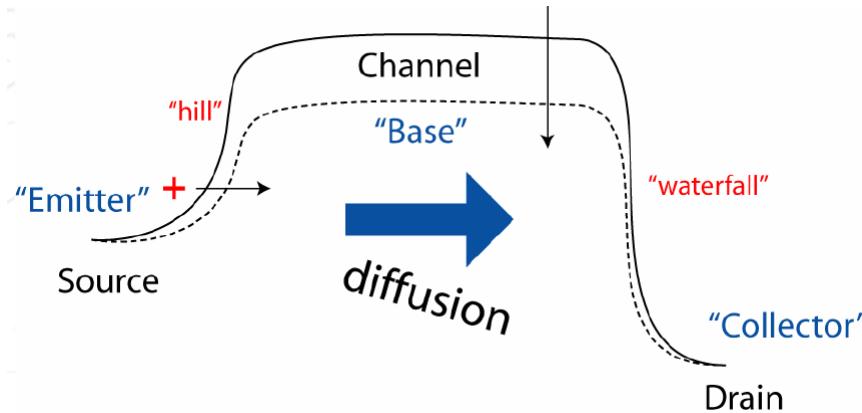
$n > 1$, 取决于偏置电压

》》弱反型区



- 场效应管实际是一个水平的BJT三极管
- 漏极的反向偏置形成二极管，增加栅极电压将线性降低二极管的电势壁垒 (Potential Barrier)
- 主要的电流是扩散电流(diffusion)而非漂移电流(drift)
- 通道中电势几乎不变，离子浓度线性变化

》》弱反型区



$$I_{D,wi} = I_{D0} \frac{W}{L} \exp\left(\frac{V_{GS}}{nU_T}\right) \cdot \left[1 - \exp\left(-\frac{V_{DS}}{U_T}\right) \right]$$

$$I_{D,wi} = I_{D0} \frac{W}{L} \exp\left(\frac{V_{GS}}{nU_T}\right) \quad \text{for } V_{DS} > 4U_T \text{ (饱和)}$$

》》弱反型与强反型

弱反型区 (Weak Inversion)

$$g_{m,wi} = \frac{I_{DS}}{nkT/q}$$



$$\frac{g_{m,wi}}{I_{DS}} = \frac{1}{nkT/q}$$

强反型区 (Strong Inversion)

$$g_{m,si} = \frac{2I_{DS}}{V_{GS} - V_{TH}}$$



$$\frac{g_{m,si}}{I_{DS}} = \frac{2}{V_{GS} - V_{TH}}$$

$$V_{GS} - V_{TH} = 2n \frac{kT}{q} \approx 70mV$$



弱-强反型区转换点

$$V_{GS} - V_{TH} = 2n \frac{kT}{q} \approx 70mV$$

- 强弱的转换点独立于工艺的尺寸
- 保证 $V_{GS} - V_{TH} = 0.2V$ 可以在不同工艺中均保证晶体管工作在强反型区
- 转换点电流: $I_{DSt} = K'_n \frac{W}{L} (V_{GS} - V_{TH})^2$

$$I_{DSt} = \frac{W}{L} \cdot \textcolor{red}{0.} \textcolor{red}{x} \mu A$$

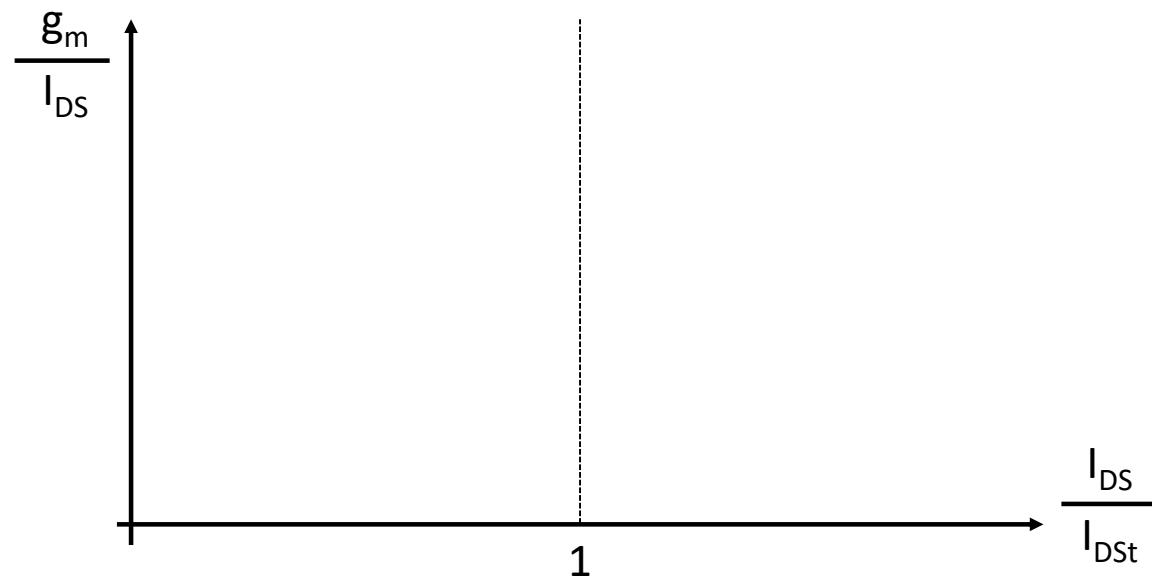
》》弱反型与强反型

弱反型区 (Weak Inversion)

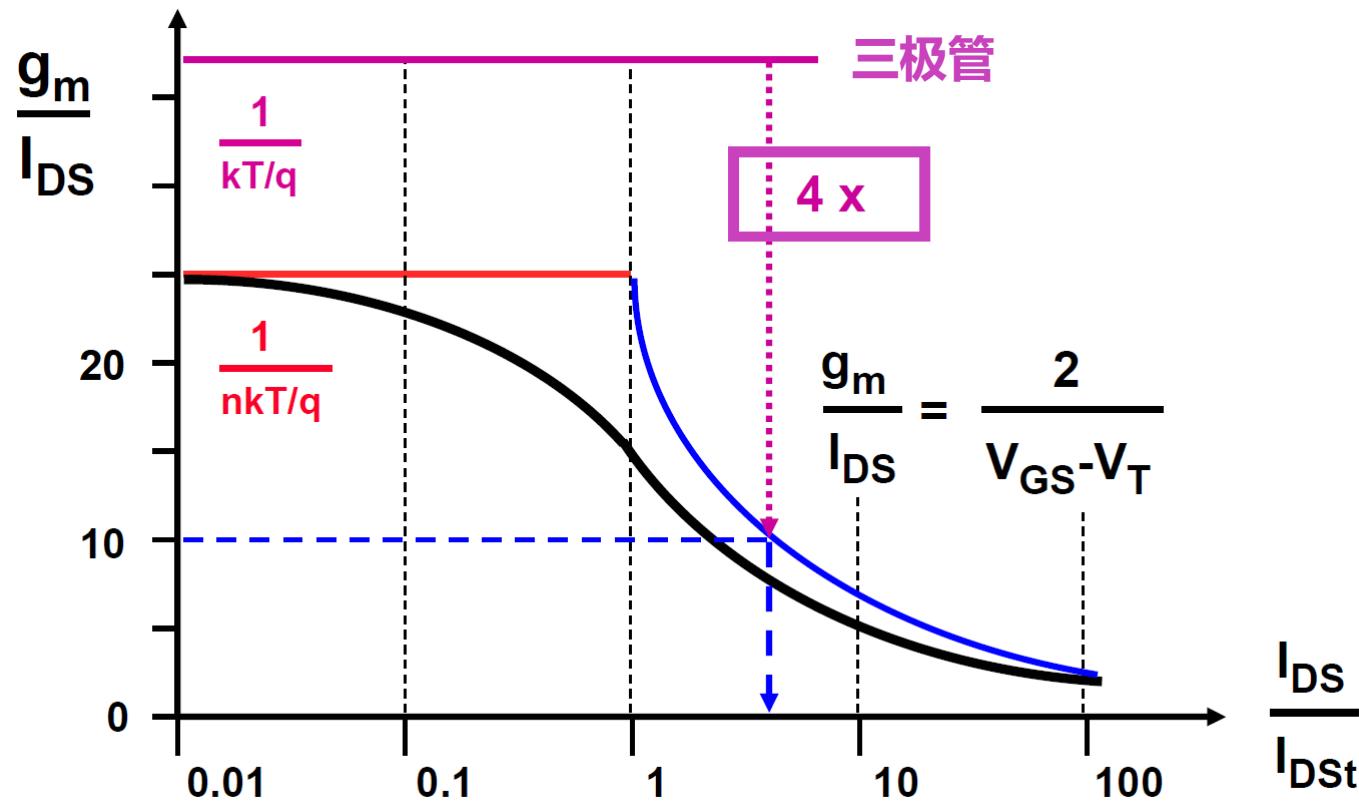
$$\frac{g_{m,wi}}{I_{DS}} = \frac{1}{nkT/q}$$

强反型区 (Strong Inversion)

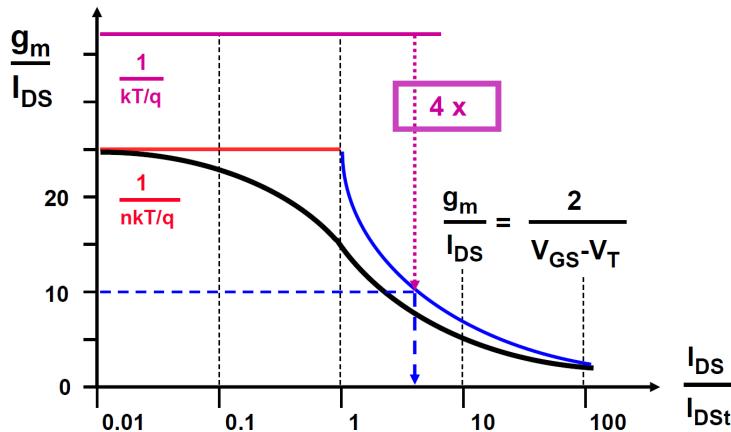
$$\frac{g_{m,si}}{I_{DS}} = \frac{2}{V_{GS} - V_{TH}}$$



》》弱反型与强反型



弱反型与强反型：EKV模型

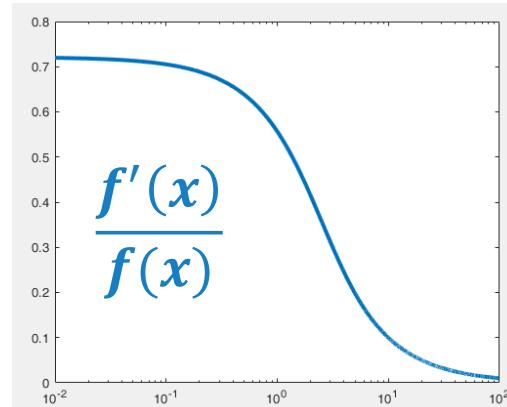


$$I_{DS} = K' \frac{W}{L} V_{GSTt}^2 \cdot \ln^2(1 + e^\nu)$$

$$\nu = \frac{V_{GST}}{V_{GSTt}}$$

- 能否通过一个公式同时表述两种反型区？

$$\ln^2(1 + e^\nu)$$



》》弱反型与强反型：EKV模型

$$I_{DS} = K' \frac{W}{L} V_{GSTt}^2 \cdot \ln^2(1 + e^\nu), \quad \nu = \frac{V_{GST}}{V_{GSTt}}, \quad V_{GSTt} = (V_{GS} - V_T)_t = 2n \frac{kT}{q}$$

- 弱反型区中:
- 强反型区中:

》》弱反型与强反型：EKV模型

$$I_{DS} = K' \frac{W}{L} V_{GSTt}^2 \cdot \ln^2(1 + e^\nu), \quad \nu = \frac{V_{GST}}{V_{GSTt}}, \quad V_{GSTt} = (V_{GS} - V_T)_t = 2n \frac{kT}{q}$$

- 弱反型区中: $\ln(1 + e^\nu) \approx e^\nu$

$$I_{DS} = K' \frac{W}{L} V_{GSTt}^2 \cdot e^{2\nu} = I_{DSt} \cdot \exp\left(\frac{V_{GS} - V_T}{nkT/q}\right)$$

- 强反型区中: $\ln(1 + e^\nu) \approx \nu$

$$I_{DS} = K' \frac{W}{L} V_{GSTt}^2 \cdot \nu^2 = K' \frac{W}{L} (V_{GS} - V_T)^2$$

》》弱反型与强反型：反型系数

$$I_{DS} = K' \frac{W}{L} V_{GSTt}^2 \cdot \ln^2(1 + e^\nu), \quad \nu = \frac{V_{GST}}{V_{GSTt}}, \quad V_{GSTt} = (V_{GS} - V_T)_t = 2n \frac{kT}{q}$$

反型系数 i : $i = \frac{I_{DS}}{I_{DSt}} = \ln^2(1 + e^\nu)$



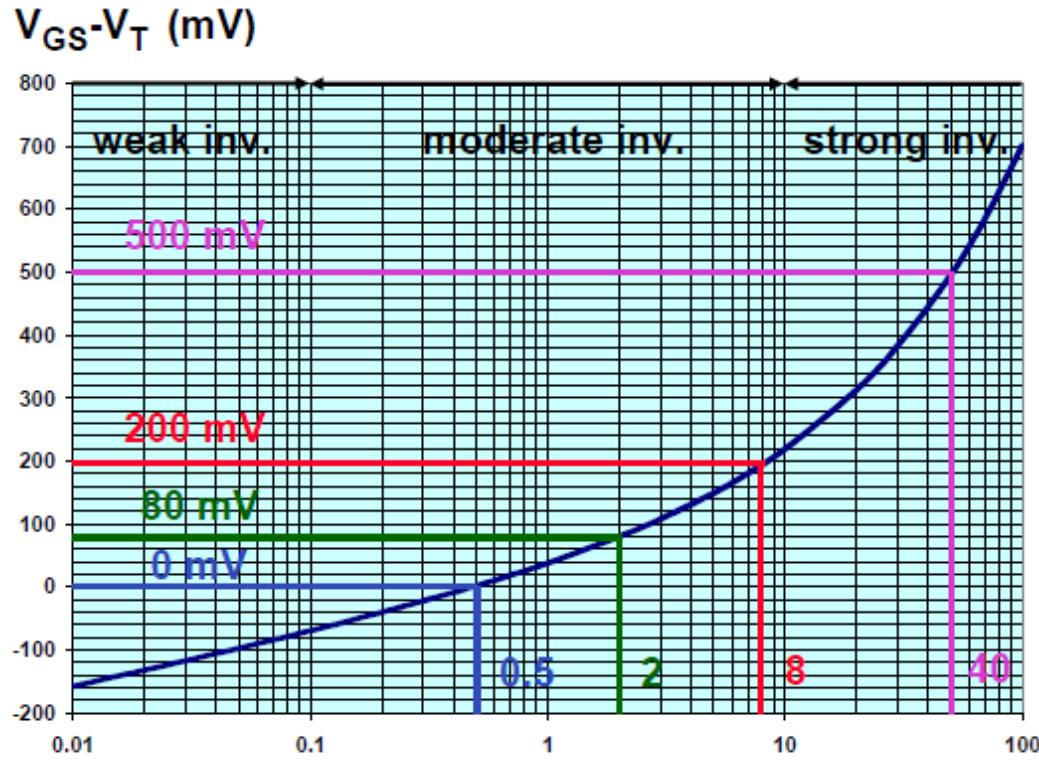
$$\nu = \ln(e^{\sqrt{i}} - 1)$$



$$V_{GST} = V_{GSTt} \cdot \ln(e^{\sqrt{i}} - 1)$$

$$V_{GSTt} = 2n \frac{kT}{q} \approx 70mV$$

》》弱反型与强反型：反型系数



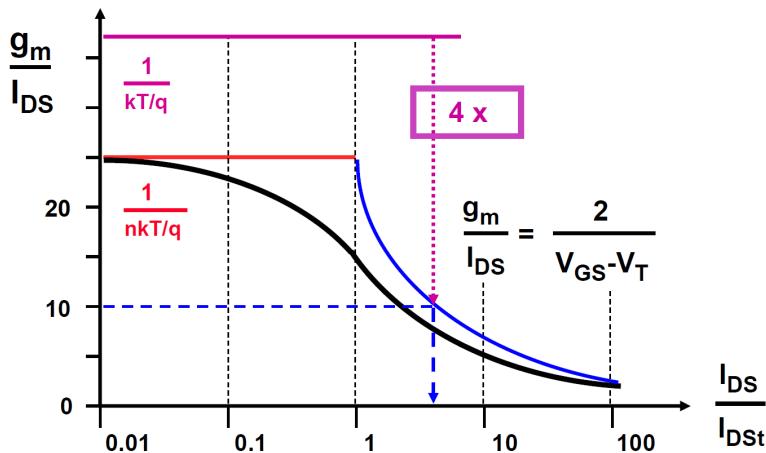
$$V_{GST} = V_{GSTt} \cdot \ln(e^{\sqrt{i}} - 1)$$

$$V_{GSTt} = 2n \frac{kT}{q} \approx 70mV$$

$$i = \frac{I_{DS}}{I_{DSt}}$$



弱反型与强反型：反型系数与 g_m/I_{DS}

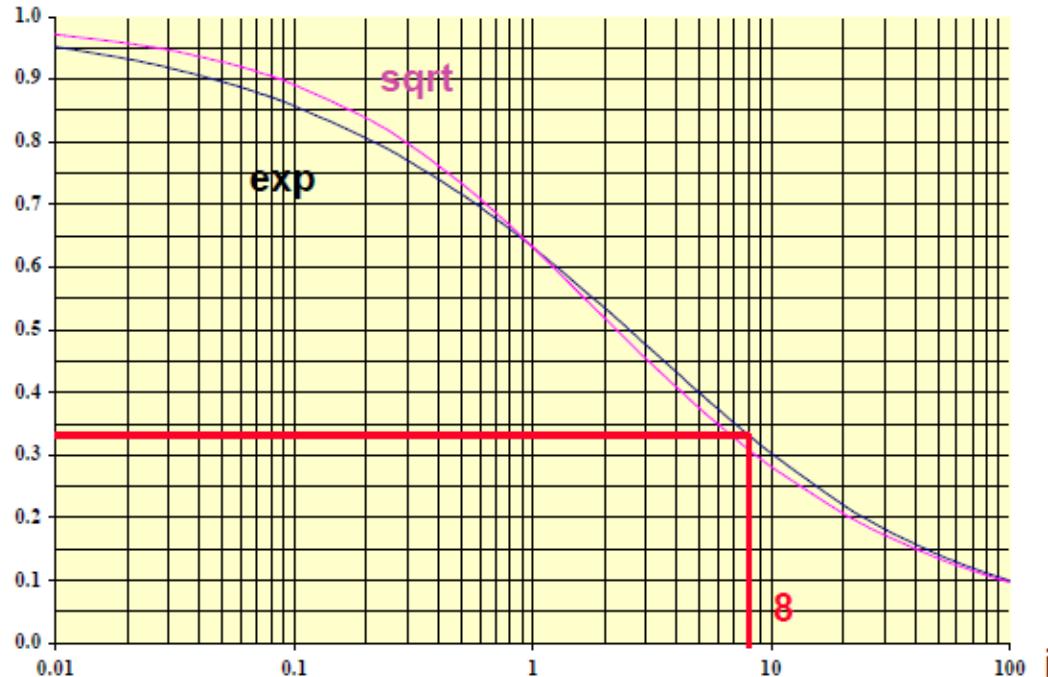


晶体管最大的 g_m/I_{DS} 出现在弱饱和区，且随着反型系数增加而下降

归一化效率 GM/ID: $GM/ID = \frac{g_m/I_{DS}}{(g_m/I_{DS})_{max}}$

→ $GM/ID = \frac{1 - e^{-\sqrt{i}}}{\sqrt{i}}$

弱反型与强反型：反型系数与 g_m/I_{DS}



$$GM/ID = \frac{1 - e^{-\sqrt{i}}}{\sqrt{i}}$$

- 反型系数为8，即 $V_{GS} - V_T = 200\text{mV}$ 时，晶体管在跨导值和跨导效率中取得一个较好的平衡。

» 弱反型与强反型

- 晶体管不会立即从弱反型区的指数行为切换为强反型区的二次项行为。在这两个极端之间有一个平滑的过渡，其中漂移和扩散均会产生电流。对该区域进行建模非常困难，通常将其行为理解为弱反型和强反型行为的混合体。

$$V_{GS} > V_T + 100\text{mV}$$

strong inversion

$$V_T + 100\text{mV} > V_{GS} > V_T - 100\text{mV}$$

moderate inversion

$$V_{GS} < V_T - 100\text{mV}$$

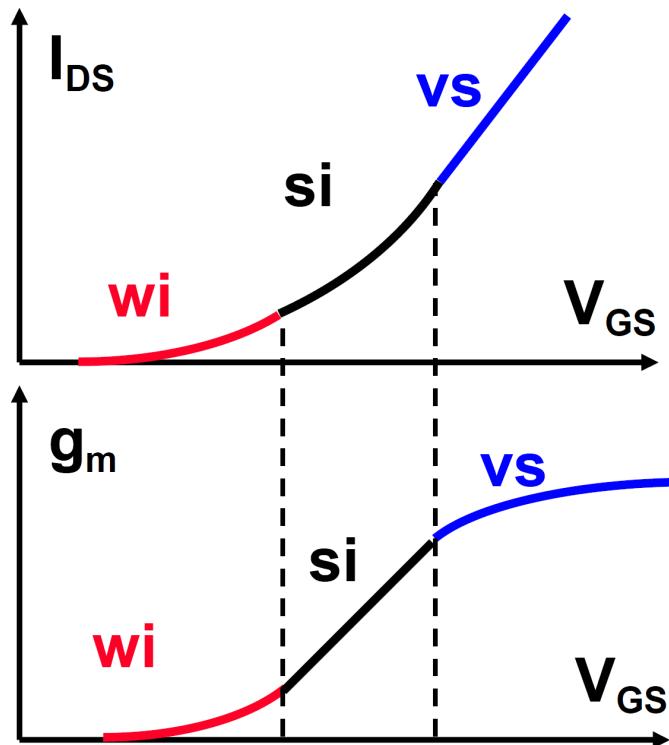
weak inversion



MOSFET

- 晶体管工作在线性区：电阻
- 晶体管工作在饱和区：放大器
- 亚反型区/弱翻转区 (Weak Inversion)
- **速度饱和区 (Velocity Saturation)**
- 特征频率

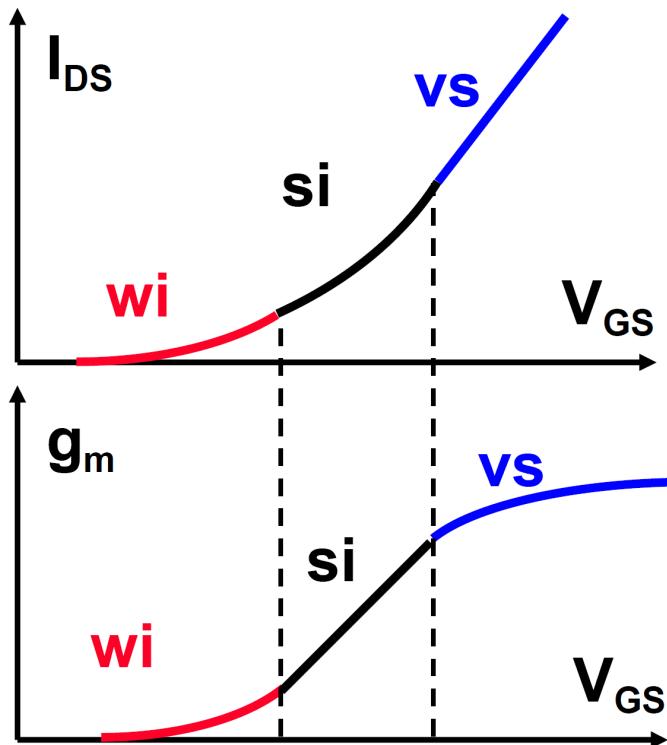
》》速度饱和区 (Velocity Saturation)



□ 如何理解饱和区电流中 V_{GS} 的平方项?

□ 如何理解饱和区跨导与 V_{GS} 的线性关系

》》速度饱和区 (Velocity Saturation)

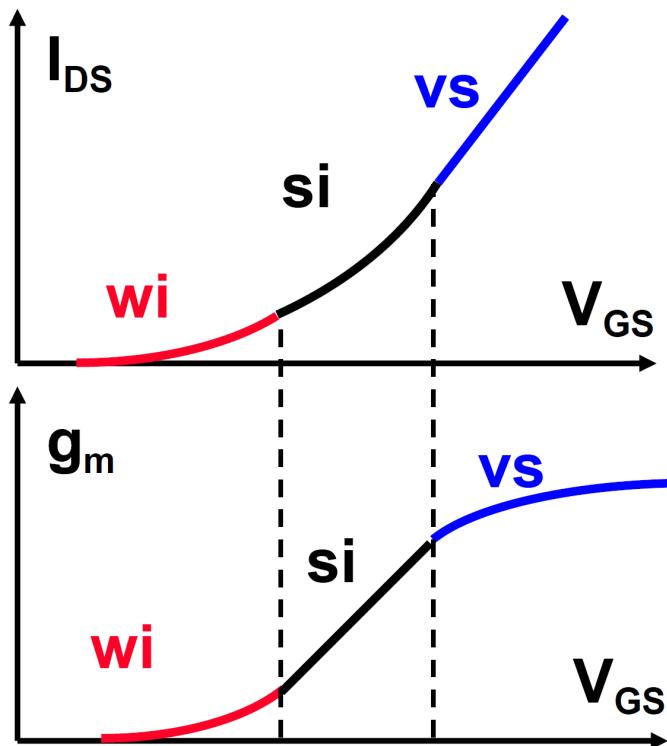


- **速度饱和区:**

- ✓ 电子以最大速度流过沟道
- ✓ 电流随着驱动电压线性增加

$$I_{DSvs} = ?$$

》》速度饱和区 (Velocity Saturation)



- 速度饱和区:

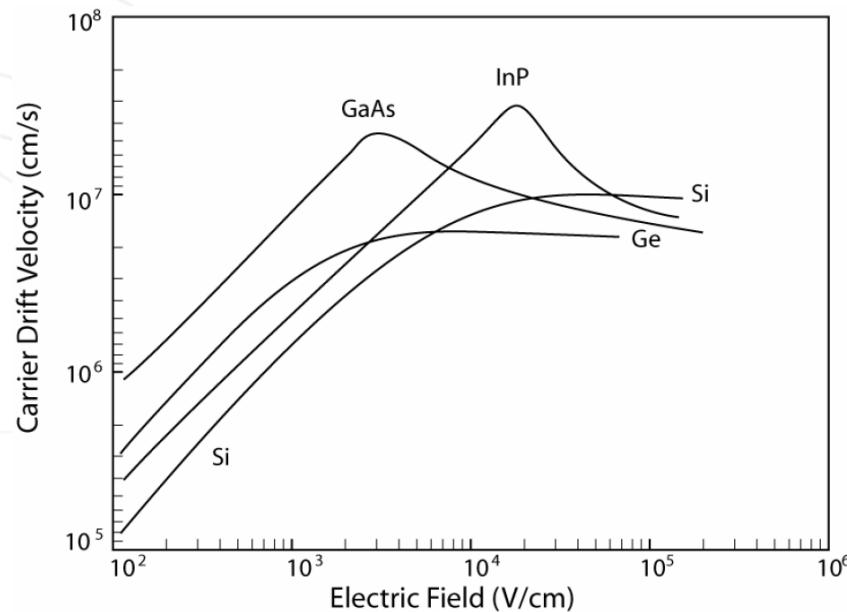
$$I_{DSvs} = WC_{ox}v_{sat} (V_{GS} - V_T)$$

$$v_{sat} \approx 10^7 \text{ cm/s}$$

$$g_{msat} = WC_{ox}v_{sat}$$

跨导到达最大值!

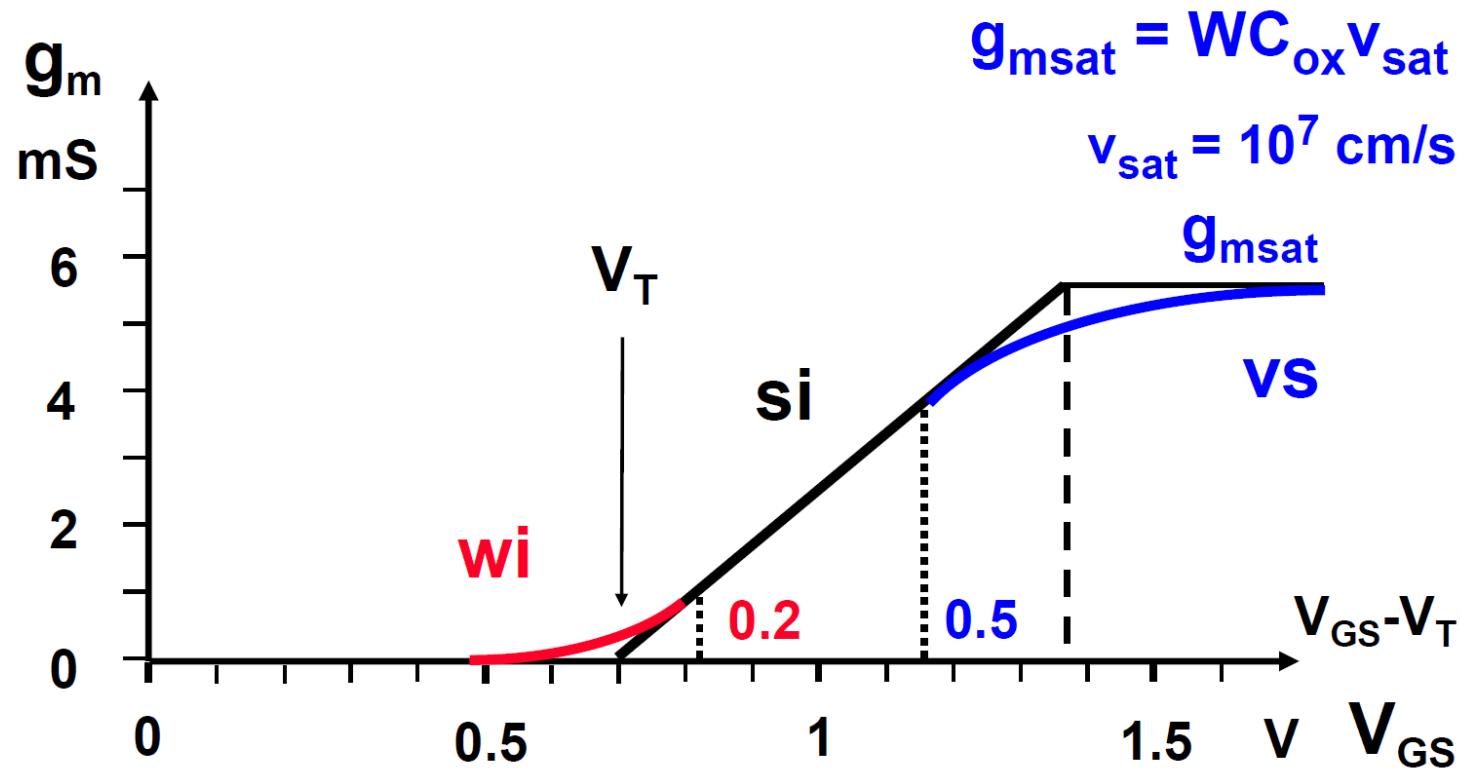
》》速度饱和区 (Velocity Saturation)



$$g_{msat} = WC_{ox}v_{sat}$$

- g_{msat}/W 只与工艺参数 C_{OX} 和物理参数 v_{sat} 有关
- 模拟电路中一般不使用该区域

》》速度饱和区



》》速度饱和区

强反型区(Strong Inversion)

$$g_{m,si} \approx \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

速度饱和区(Velocity Saturation)

$$g_{m,sat} = WC_{OX}v_{sat}$$



$$(V_{GS} - V_{TH})_{vs} = \frac{L \cdot v_{sat}}{\mu}$$

$$v_{sat} \approx 10^7 \text{ cm/s}$$

$$\mu_p \approx 250 \text{ cm}^2/\text{Vs}$$

$$\mu_n \approx 600 \text{ cm}^2/\text{Vs}$$



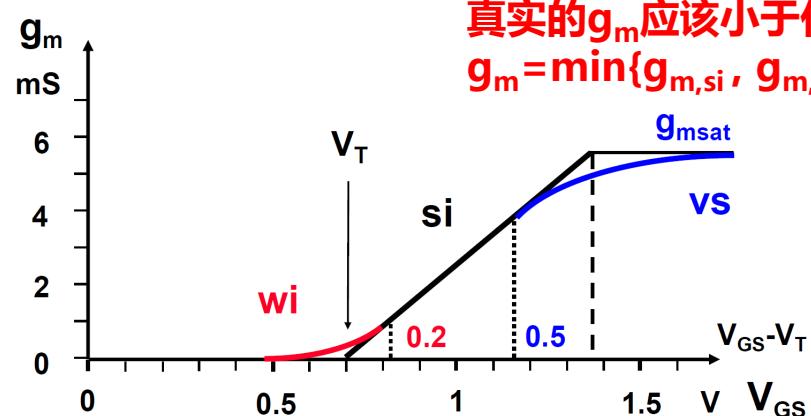
$$(V_{GS} - V_{TH})_{vs} = 0.58V$$

$$L_{min} = 0.35 \mu\text{m}$$

》》速度饱和区

强反型区(Strong Inversion)

$$g_{m,si} \approx \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$



速度饱和区(Velocity Saturation)

$$g_{m,sat} = W C_{OX} v_{sat}$$

真实的 g_m 应该小于任意一个表达式

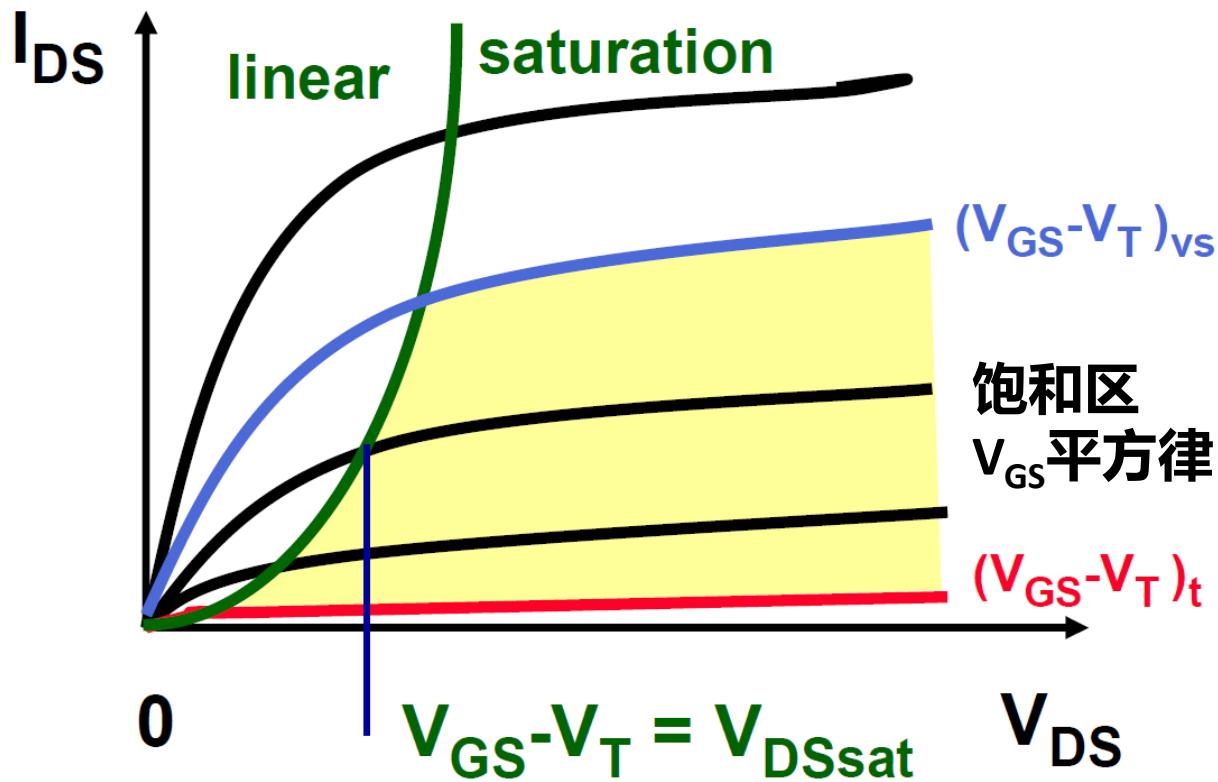
$$g_m = \min\{g_{m,si}, g_{m,sat}\}$$

$$\frac{1}{g_m} = \frac{1}{g_{m,si}} + \frac{1}{g_{m,sat}}$$

$$g_m \approx \frac{W}{L} \frac{17 \cdot 10^{-5}}{1 + 2.8 \cdot 10^4 L / V_{GST}}$$

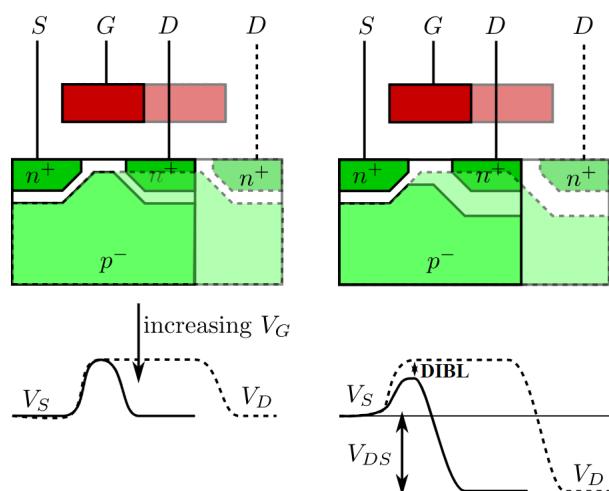
L
in cm

» 饱和区VS速度饱和区

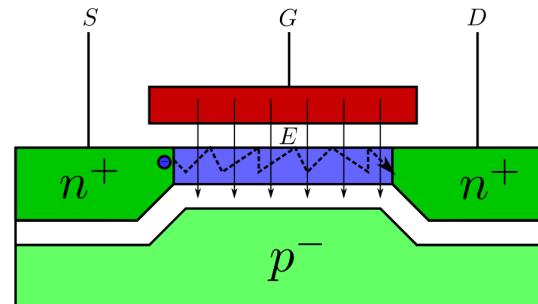


》》 其他因素

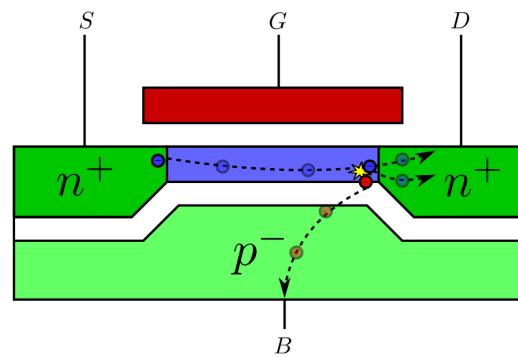
Drain-Induced Barrier Lowering (DIBL)



Surface Scattering



Impact ionization

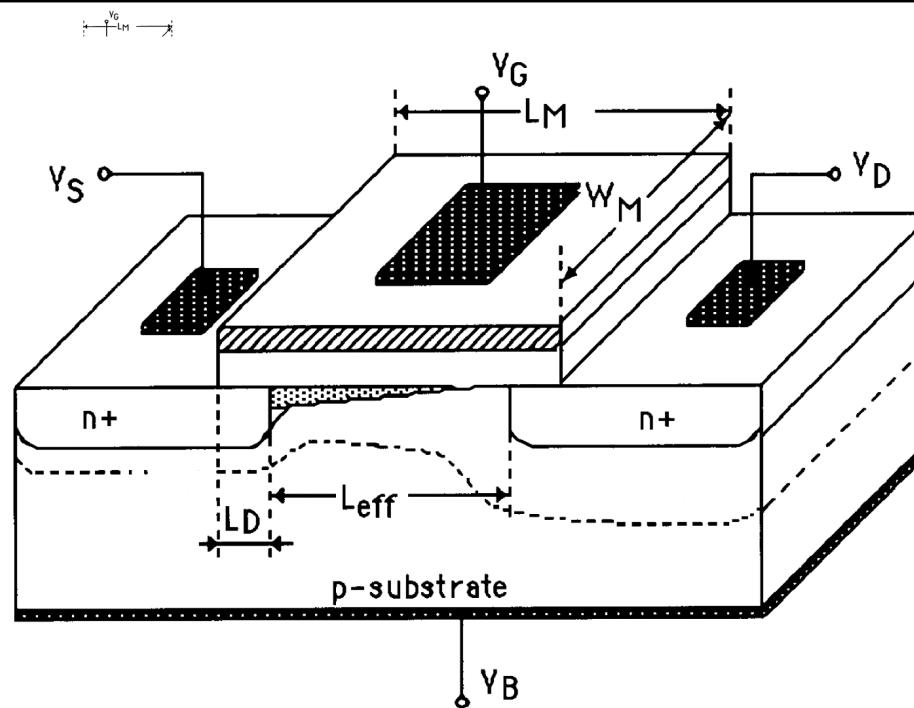




MOSFET

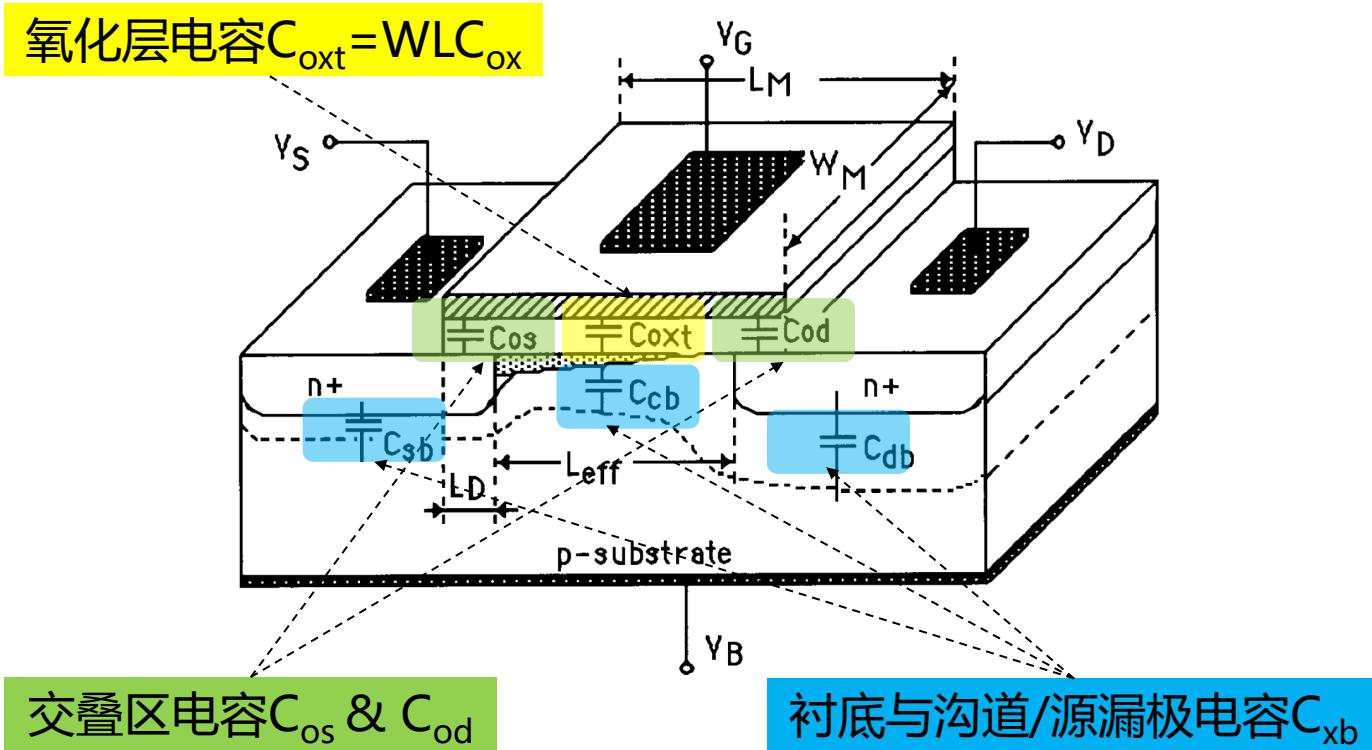
- 晶体管工作在线性区：电阻
- 晶体管工作在饱和区：放大器
- 亚反型区/弱翻转区 (Weak Inversion)
- 速度饱和区 (Velocity Saturation)
- **特征频率**

》》 特征频率 f_T

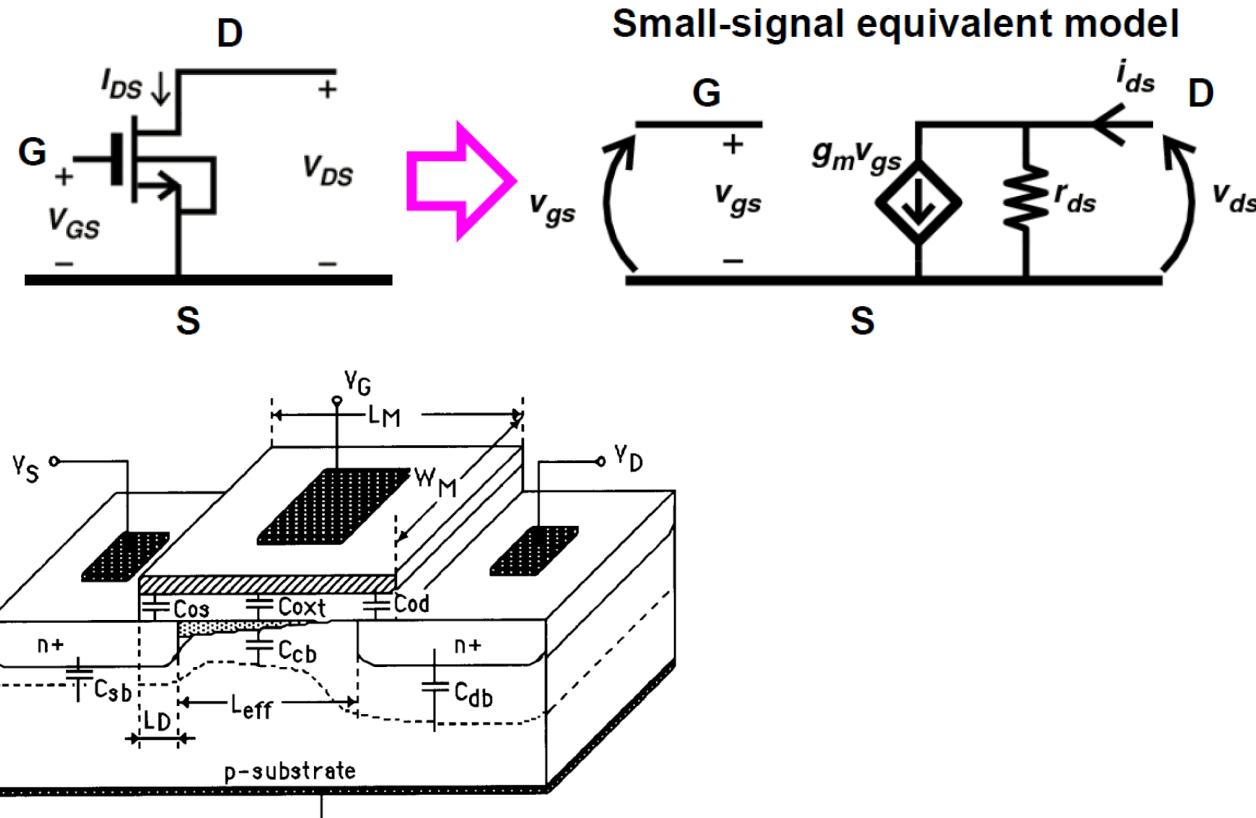


- 特征频率是表征晶体管在高频时放大能力的一个基本参量，主要由晶体管的**跨导**和**寄生电容**决定。

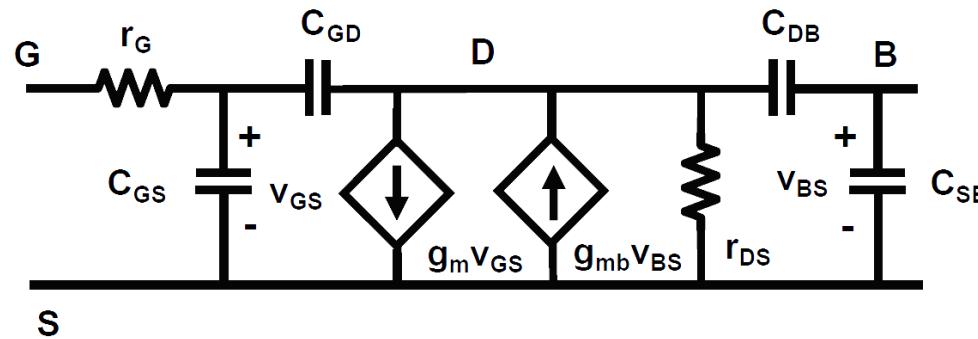
》》 特征频率 f_T



》》高频小信号模型



》》高频小信号模型

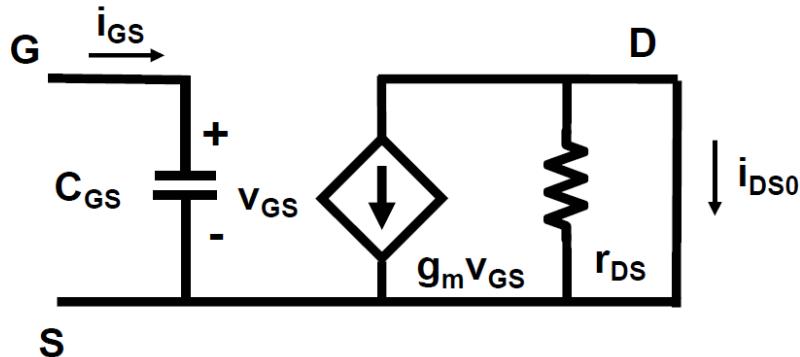


$$C_{GS} \approx \frac{2}{3} WLC_{ox} \approx 2W \text{ fF}/\mu\text{m for } L_{min}$$

$$L_{min} C_{ox} \approx L_{min} \frac{\epsilon_{ox}}{t_{ox}} \approx 50 \epsilon_{ox} \approx 2 \text{ fF}/\mu\text{m}$$

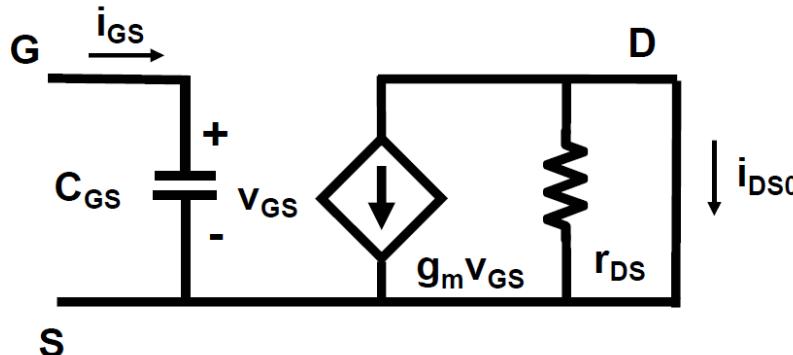
$$C_{GD} = W C_{gdo}$$

》》 特征频率 f_T , $i_{DS} = i_{GS}$



$$i_{GS} =$$
$$i_{DS0} =$$

》》 特征频率 f_T , $i_{DS} = i_{GS}$



$$i_{GS} = v_{GS} C_{GS} s$$

$$i_{DS} = g_m v_{GS}$$

$$C_{GS} = \frac{2}{3} WLC_{ox} \quad g_m = 2K' \frac{W}{L} (V_{GS} - V_T) \quad K' = \frac{\mu C_{ox}}{2n}$$

$$f_T = \frac{g_m}{2\pi C_{GS}} = \frac{1}{2\pi} \frac{3}{2n} \frac{\mu}{L^2} (V_{GS} - V_T)$$

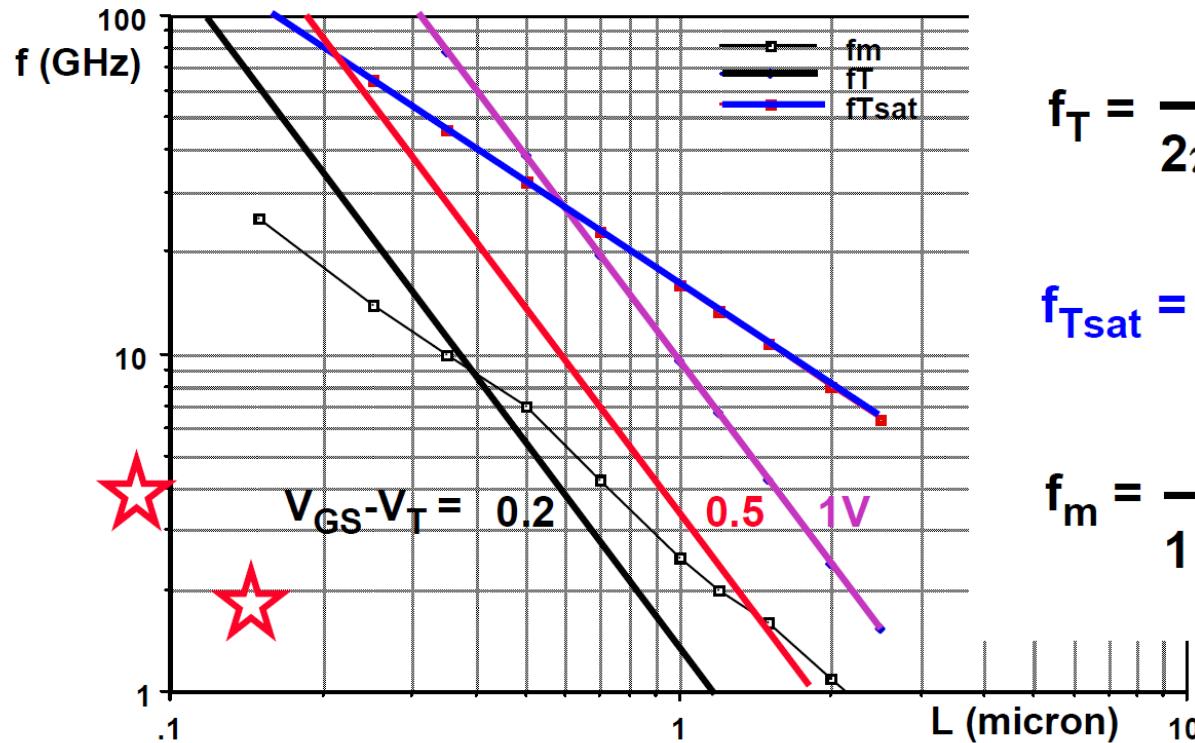
↑
反型区

or

$$\approx \frac{v_{sat}}{2\pi L}$$

↑
速度饱和区

》》 f_T与沟道长度L的关系



Processors

$$f_T = \frac{\mu}{2\pi L^2} \underbrace{(V_{GS} - V_T)}_{0.2 \dots 1 \text{ V}}$$

$$f_{Tsat} = \frac{v_{sat}}{2\pi L}$$

$$f_m = \frac{f_T}{1 + \alpha_{BD}}$$

$$\alpha_{BD} \approx \frac{C_{BD}}{C_{ox}}$$



f_T 与沟道长度L的关系

$$f_T = \frac{1}{L} \frac{13.5}{1 + 2.8 L / V_{GST}} \text{ GHz}$$

L in μm

If $V_{GST} = 0.2 \text{ V}$, v_{sat} takes over for $L < 65 \text{ nm}$

If $V_{GST} = 0.5 \text{ V}$ for $L < 0.15 \mu\text{m}$



f_T在强反型区和弱反型区中模型

$$\left\{ \begin{array}{l} GM/ID = \frac{g_m/I_{DS}}{(g_m/I_{DS})_{max}} = \frac{1 - e^{-\sqrt{i}}}{\sqrt{i}} \\ i = \frac{I_{DS}}{I_{DSt}} \end{array} \right.$$

$$f_T =$$

》》 f_T 在强反型区和弱反型区中模型

$$\left\{ \begin{array}{l} GM/ID = \frac{g_m/I_{DS}}{(g_m/I_{DS})_{max}} = \frac{1 - e^{-\sqrt{i}}}{\sqrt{i}} \\ i = \frac{I_{DS}}{I_{DSt}} \end{array} \right.$$

$$f_T = \frac{g_m}{2\pi C_{GS}} = \frac{1}{2\pi C_{GS}} \frac{I_{DSt}}{nkT/q} \sqrt{i}(1 - e^{\sqrt{i}})$$

$$= \frac{2\mu kT/q}{2\pi L^2} \cdot \sqrt{i}(1 - e^{\sqrt{i}})$$

尺寸设计 偏置设计



设计思路总结

1. 手工计算用来估算尺寸，精确设计依赖仿真结果。
2. 时刻牢记 g_m/I_D 的曲线及大致数值。
3. 低功耗电路取 $V_{GS} - V_{TH} < -0.1V$ ；高增益电路取 $V_{GS} - V_{TH} = 0.2V$ ；
高速电路取 $V_{GS} - V_{TH} = 0.5V$ 。
4. 通过 f_T 的公式来估算设计的特征频率。

》》 课程群（钉钉）



扫一扫二维码，加入班级

》》课后作业

1. 分别对于 $W/L=1\text{um}/1\text{um}$ 的NMOS和PMOS，在 $0-1.8\text{V}$ 的区域内，扫描 V_{GS} ，同时令 $V_{DS}=1.8\text{V}$ ，画出 I_{DS} , g_m 和 g_m/I_{DS} 的曲线。（提示：改变坐标的刻度表现形式，以得到更直观的展示）
2. 估算 $V_{GS}=0.5\text{V}$, 0.8V 和 1.1V 且 $V_{DS}=1.8\text{V}$ 时， $W/L=1\text{um}/0.18\text{um}$ 的NMOS的 g_m 和 r_0 。
3. 估算 $V_{GS}=0.5\text{V}$, 0.8V 和 1.1V 且 $V_{DS}=1.8\text{V}$ 时， $W/L=1\text{um}/0.18\text{um}$ 的NMOS的特征频率 f_T ，并通过AC仿真得到所求的特征频率。

第2章 模拟电路基本组成



北京航空航天大學
BEIHANG UNIVERSITY

| 微电子学院

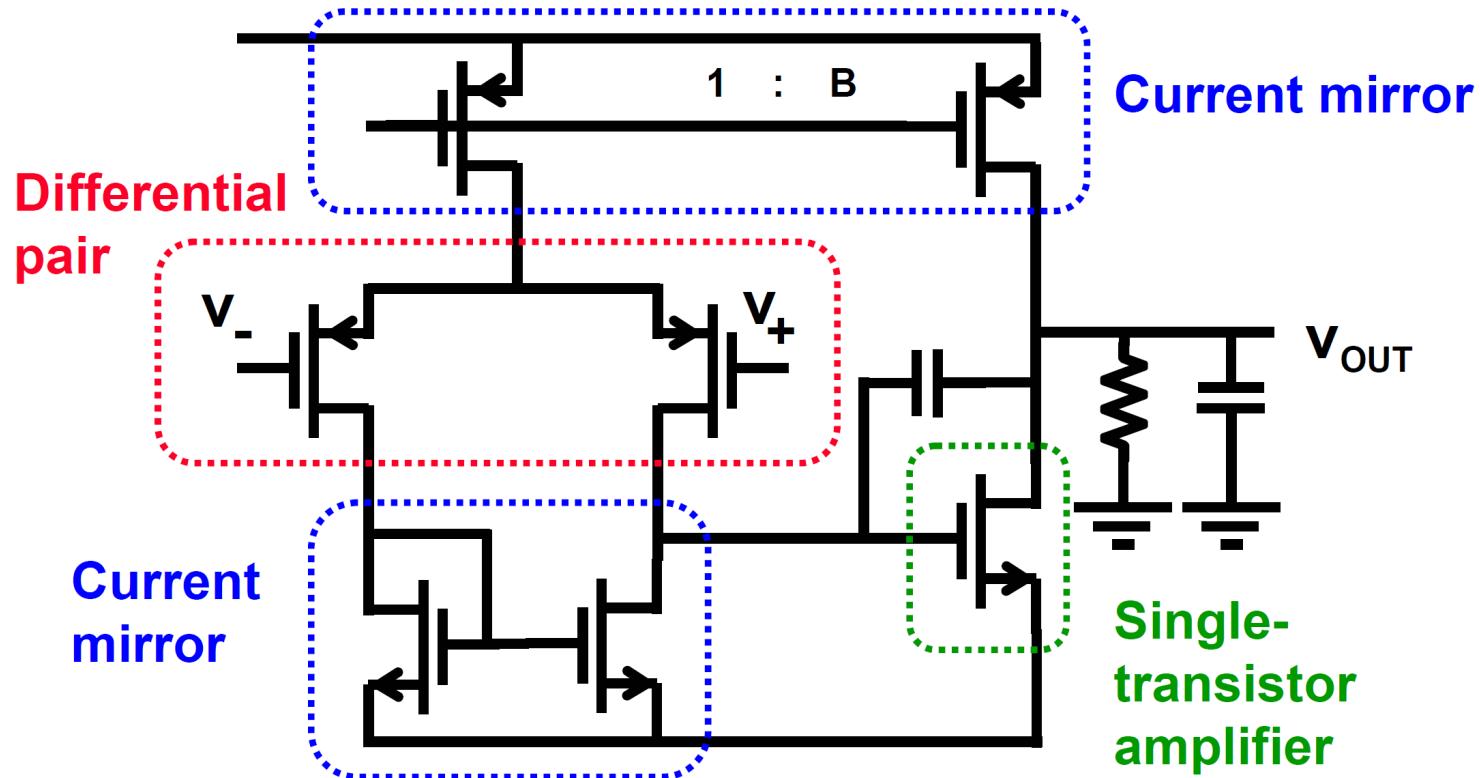
CMOS模拟集成电路设计

第二章：模拟电路的基本构成

胡远奇

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》》运算放大器

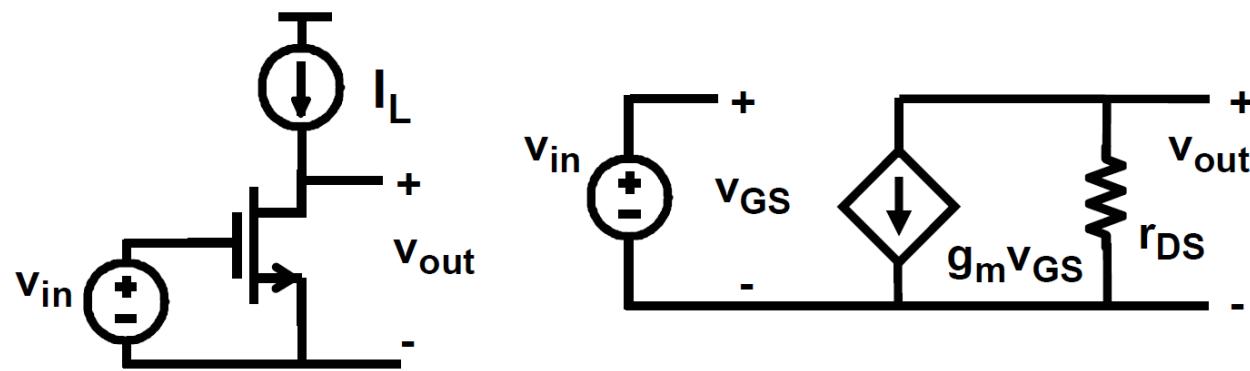




模拟电路的基本结构

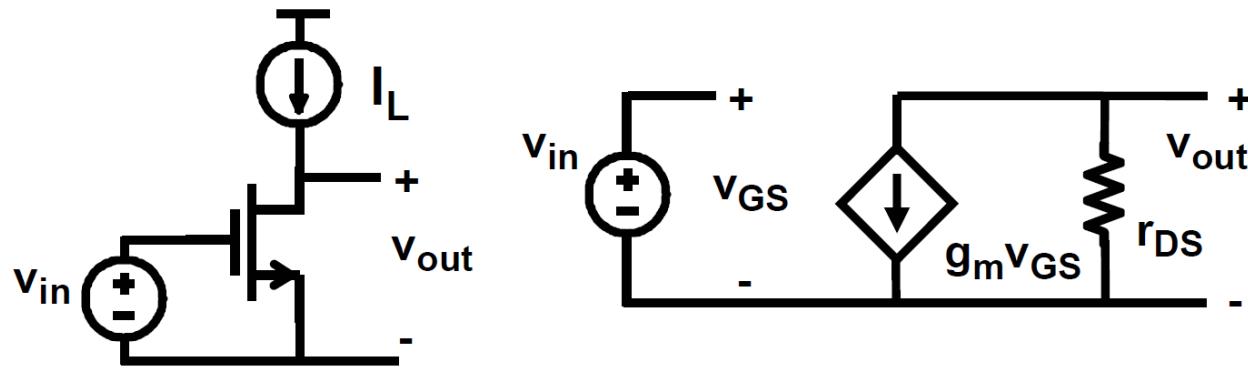
1. 单晶体管放大器
2. 源极跟随器
3. Cascode (共源共栅极)
4. 电流镜
5. 差分对

》》单晶体管放大器



$$A_v =$$

》》单晶体管放大器



$$A_v = g_m r_{DS} = \frac{2 I_{DS}}{V_{GS} - V_T} \frac{V_E L}{I_{DS}} = \frac{2 V_E L}{V_{GS} - V_T}$$

$$A_v \approx 100 \quad \text{if } V_E L \approx 10 \text{ V and } V_{GS} - V_T \approx 0.2 \text{ V}$$

》》单晶体管放大器

如何获得高增益?

降低 $V_{GS} - V_T$

增加L

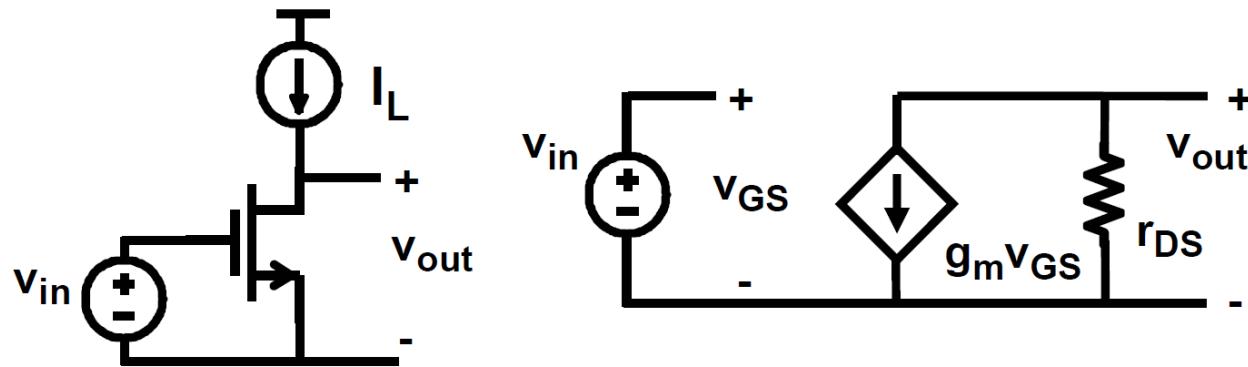
0.15-0.2V

4-5x minL

进一步减小会牺牲信噪
比SNR和跨导gm

进一步增大会牺牲速度
和面积

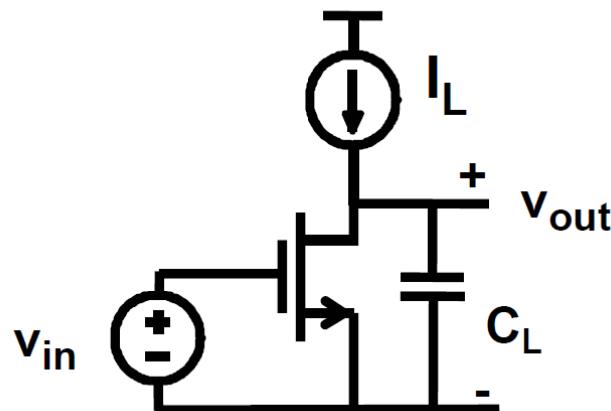
》》单晶体管放大器



□问：对于一个55nm工艺的单晶体管放大器，其典型的放大倍数是多少？($V_E=4V/\mu m$)

》》 单晶体管放大器的频率特性

- 如果只有大的负载电容



$$A_{v0} = g_m r_{DS}$$

$$BW = \frac{1}{2\pi r_{DS} C_L}$$

$$GBW = \frac{g_m}{2\pi C_L}$$

For all single-stage
Operational amplifiers



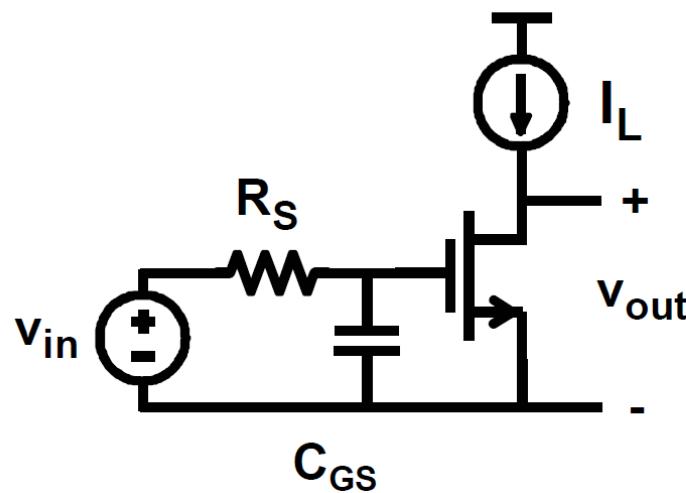
单晶体管放大器的频率特性

设计指标 $GBW = 100M$, 负载电容 $2pF$ 的NMOS单晶体放大器,
根据工艺指标计算相应的直流偏置电流和典型晶体管尺寸。

$$L_{min} = 0.35 \mu m \quad K_P_n \approx 300 \mu A/V^2$$

》》单晶体管放大器的频率特性

- 如果只有大的输入电容

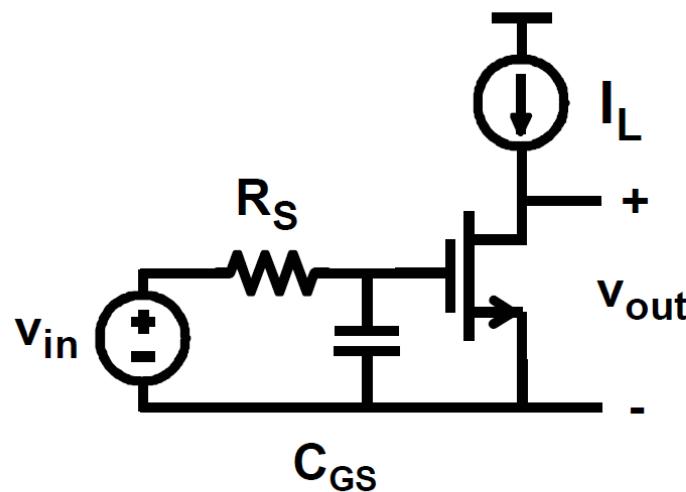


$$A_{v0} = g_m r_{DS}$$

$$BW = \frac{1}{2\pi R_s C_{GS}}$$

》》单晶体管放大器的频率特性

- 如果只有大的输入电容



$$A_{v0} = g_m r_{DS}$$

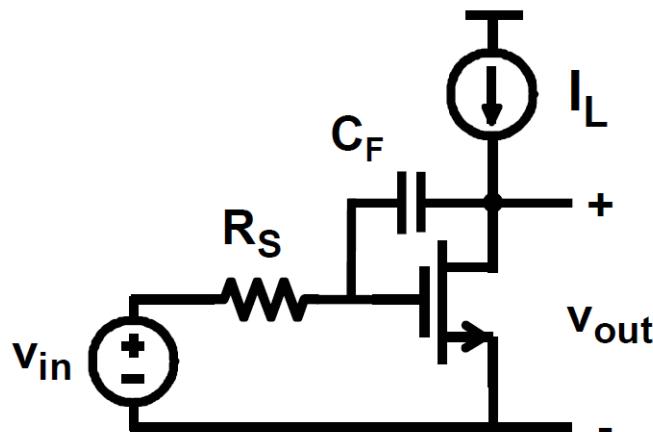
$$BW = \frac{1}{2\pi R_s C_{GS}}$$

GBW和长度L无关!

$$GBW = \frac{g_m}{2\pi C_{GS}} \frac{r_{DS}}{R_s} = f_T \frac{r_{DS}}{R_s} \sim \frac{1}{WC_{ox}} \frac{1}{V_{GS}-V_T}$$

》》单晶体管放大器的频率特性

- 如果只有大的反馈电容



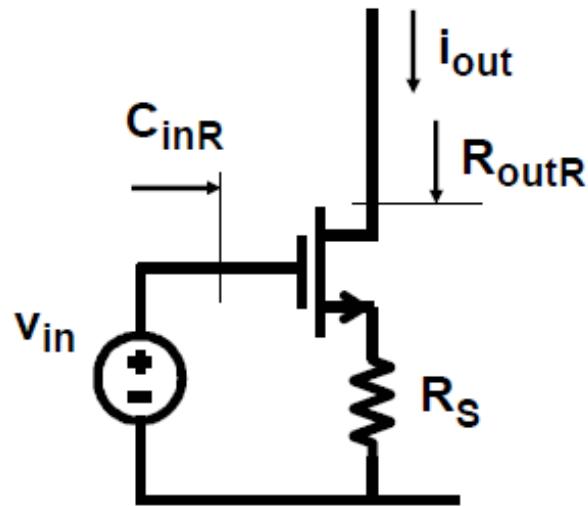
$$A_{v0} = g_m r_{DS}$$

$$BW = \frac{1}{2\pi R_S A_{v0} C_F}$$

$$GBW = \frac{1}{2\pi R_S C_F}$$

GBW和晶体管的参数无关!

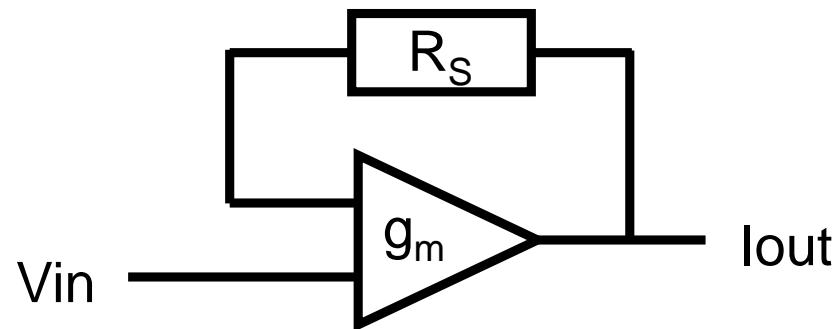
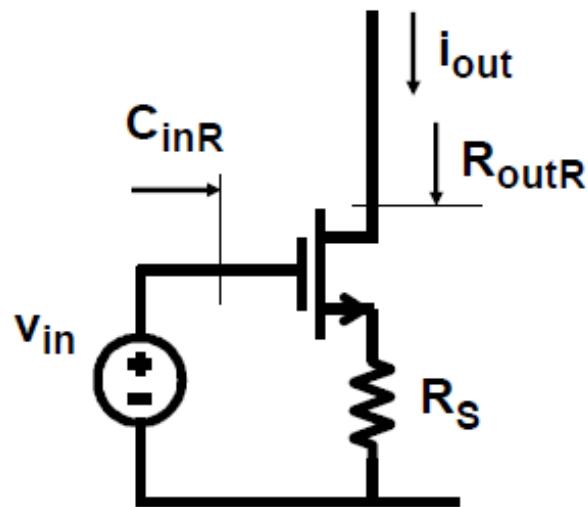
»» Source Degeneration



Source Degeneration

是一种**负反馈**形式

»» Source Degeneration

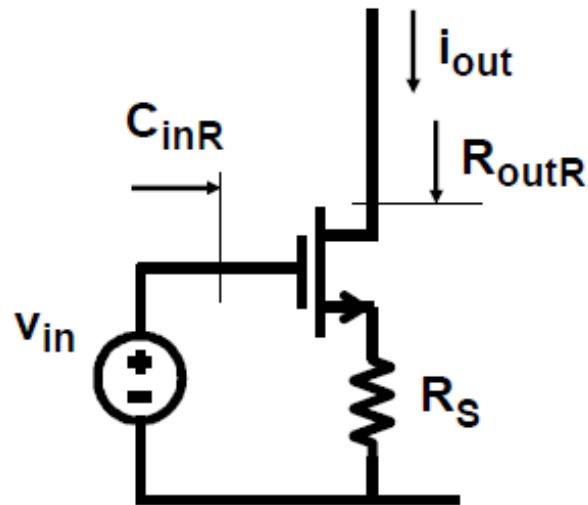


$$G_m = \frac{g_m}{1 + g_m R_s}$$

Source Degeneration
是一种**负反馈**形式

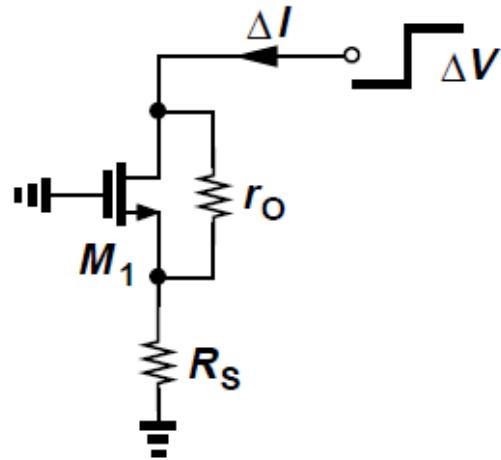
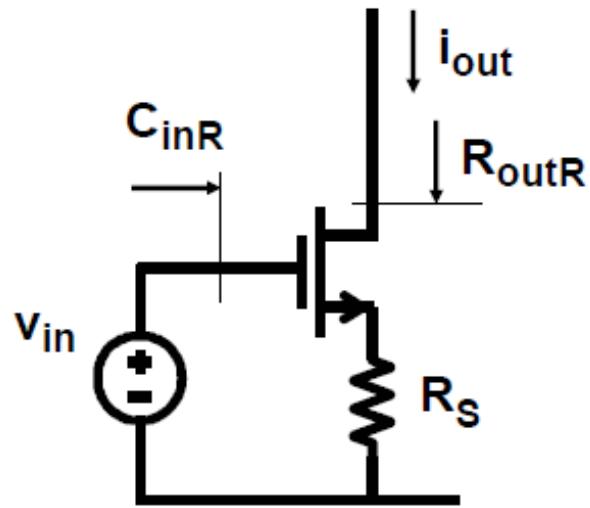
$$C_{inR} = \frac{C_{GS}}{1 + g_m R_s}$$

»» Source Degeneration



- 在输出端施加电压变化 ΔV 并测量输出电流的最终变化 ΔI

»» Source Degeneration



$$\bullet R_{outR} = r_{DS} (1 + g_m R_s) \approx (g_m r_{DS}) R_s$$

R_s 造成额外的噪声

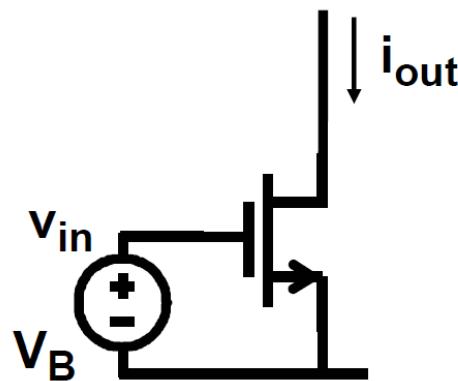


模拟电路的基本结构

1. 单晶体管放大器
2. 源极跟随器
3. Cascode (共源共栅极)
4. 电流镜
5. 差分对

》》 源极跟随器 (Source Follower)

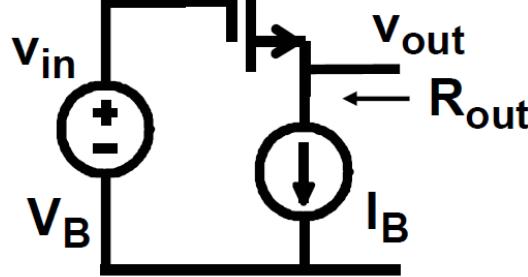
Common source



$$i_{out} = g_m v_{in}$$



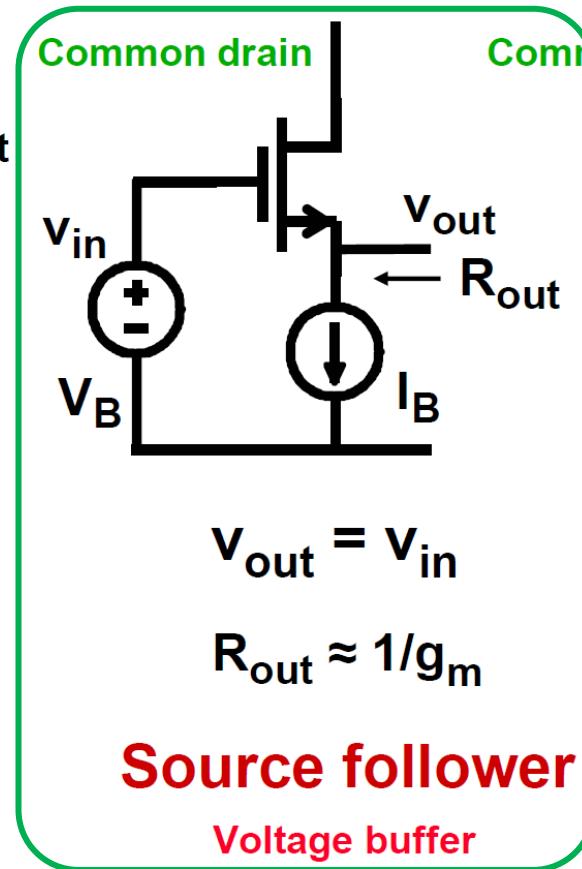
Common drain



$$v_{out} = v_{in}$$

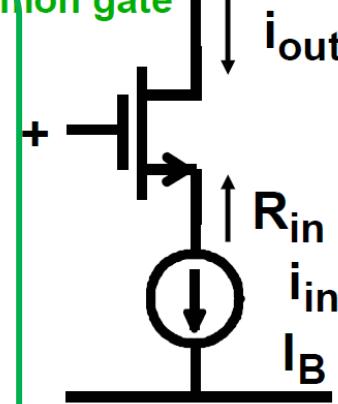
$$R_{out} \approx 1/g_m$$

Amplifier



Source follower
Voltage buffer

Common gate

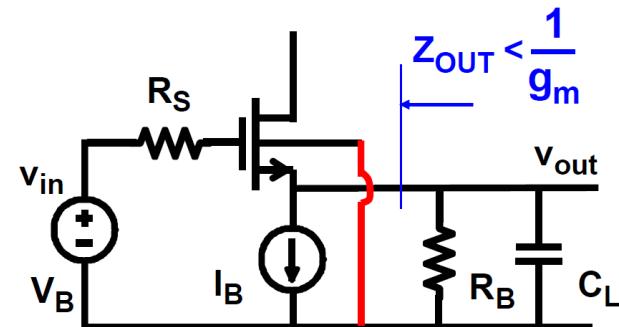
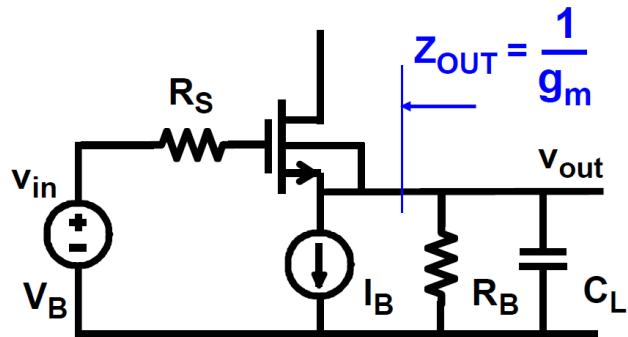


$$i_{out} = i_{in}$$

$$R_{in} \approx 1/g_m$$

Cascode
Current buffer

》》 源极跟随器 (Source Follower)



I_B 为常数
↓
 V_{GS} 为常数
↓
 $\Delta V_{OUT} = \Delta V_{IN}$
↓
 $A_V = 1$

V_{GS} 不为常数
↓
 $A_V = \frac{1}{n} < 1$

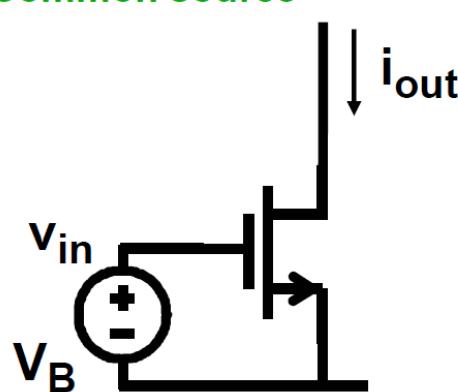


模拟电路的基本结构

1. 单晶体管放大器
2. 源极跟随器
3. **Cascode (共源共栅极)**
4. 电流镜
5. 差分对

»» Cascode

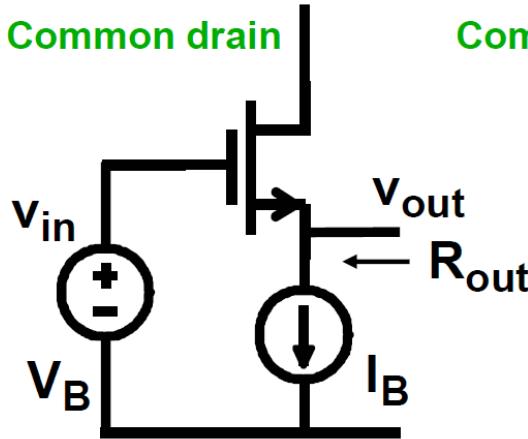
Common source



$$i_{out} = g_m v_{in}$$



Common drain

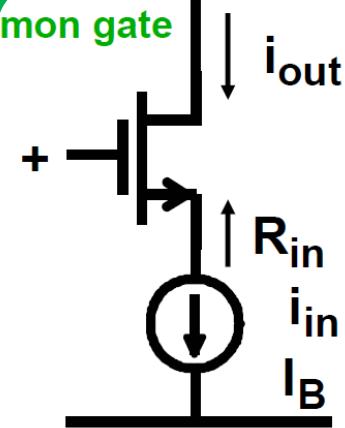


$$v_{out} = v_{in}$$

$$R_{out} \approx 1/g_m$$

Amplifier

Common gate



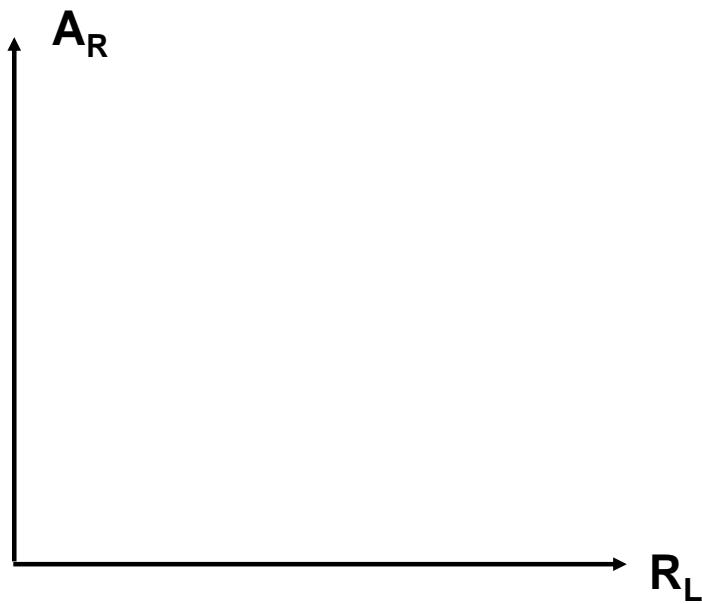
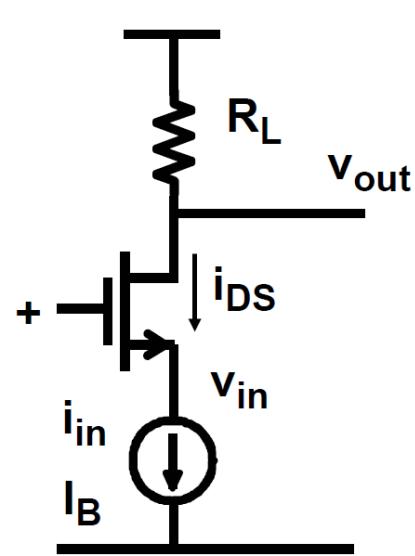
$$i_{out} = i_{in}$$

$$R_{in} \approx 1/g_m$$

Source follower
Voltage buffer

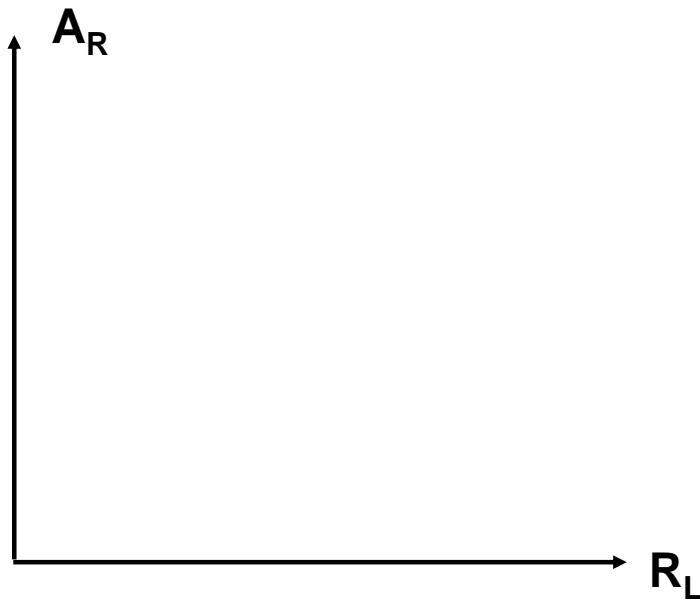
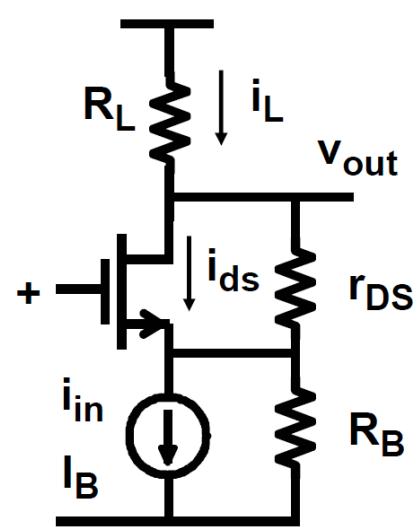
Cascode
Current buffer

»» Cascode



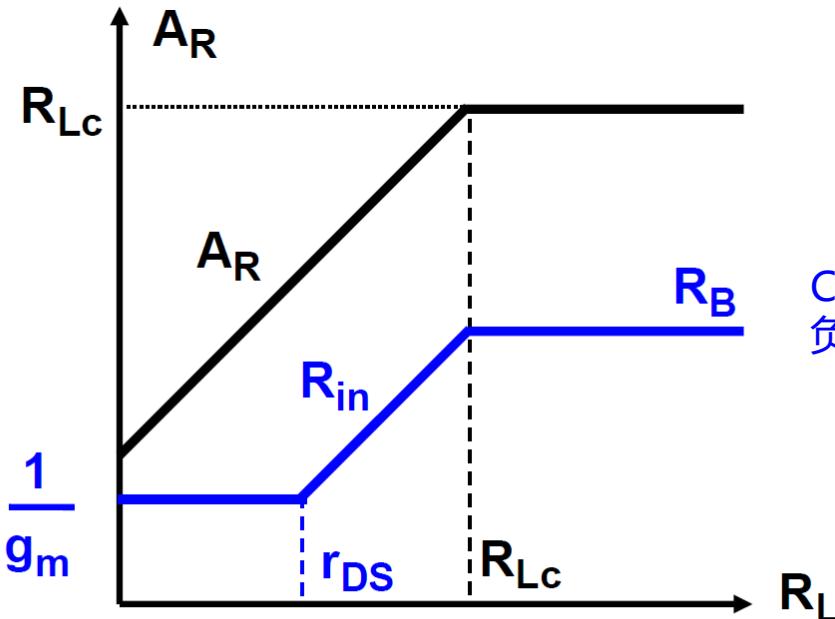
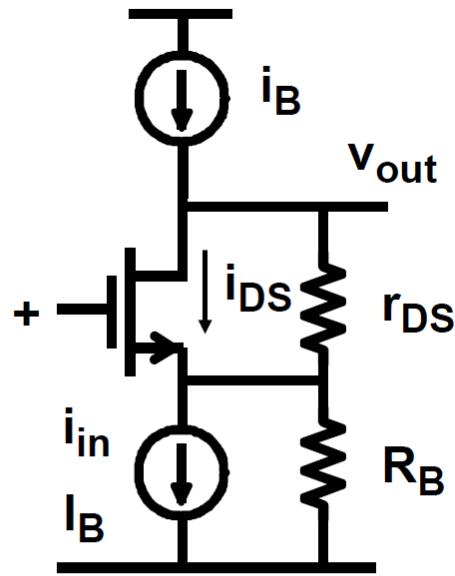
- 定义跨阻增益 $A_R = v_{out}/i_{in}$

»» Cascode



- 分析输入电阻 R_{in}

»» Cascode

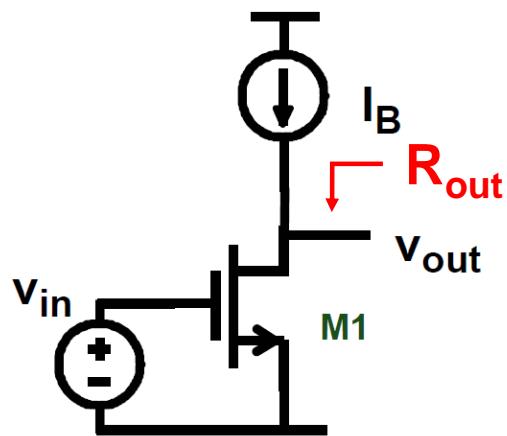


$$A_R = \frac{v_{out}}{i_{in}}$$

$$R_{in} = \frac{v_{in}}{i_{in}}$$

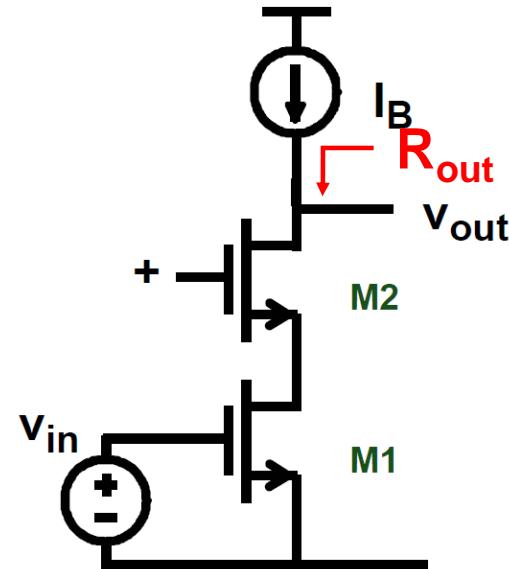
$$R_{in} = \frac{r_{DS} + R_L}{g_m r_{DS}} || R_B$$

»» Cascode vs 单晶体管



$$A_v = (g_m r_{DS})_1$$

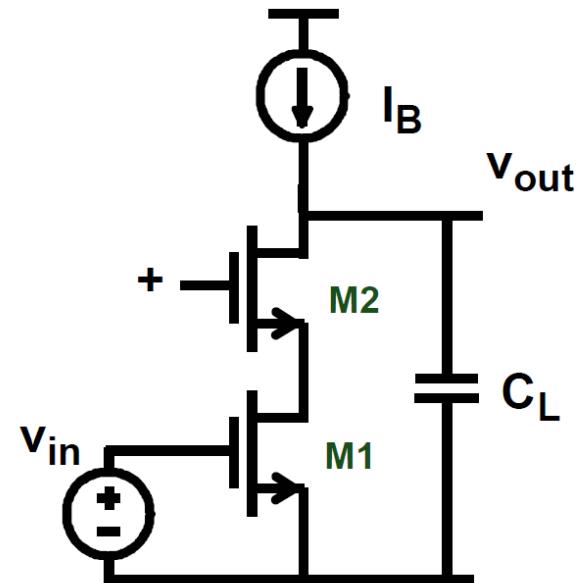
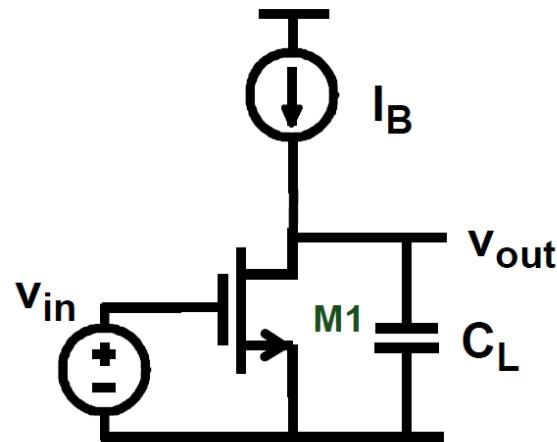
$$R_{out} = r_{DS1}$$



$$A_v = (g_m r_{DS})_1 (g_m r_{DS})_2$$

$$R_{out} = r_{DS1} (g_m r_{DS})_2$$

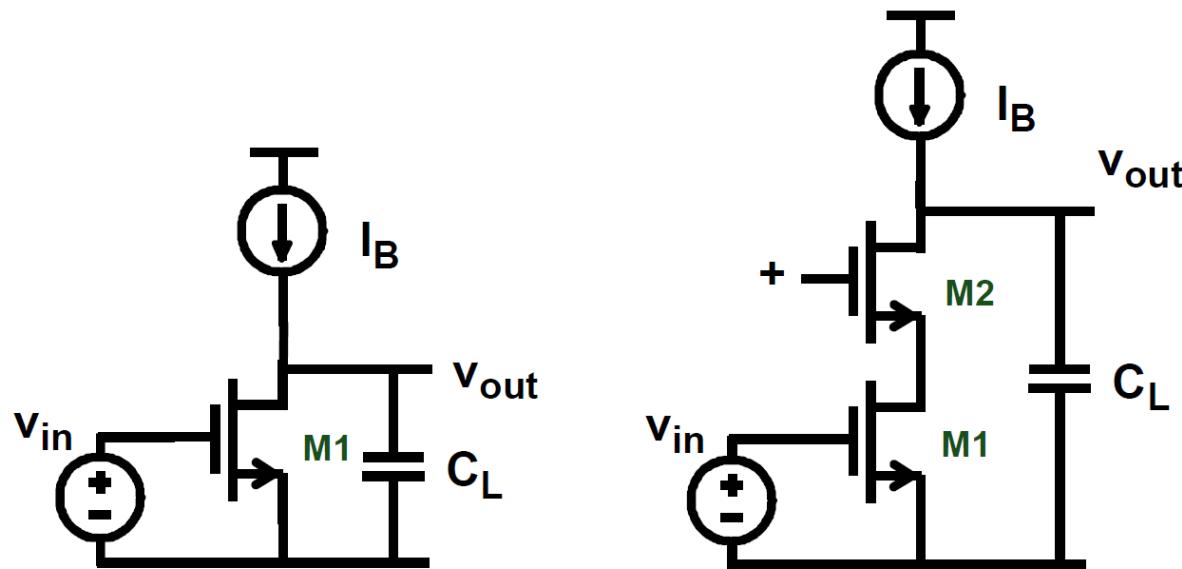
»» Cascode vs 单晶体管



BW =

GBW =

»» Cascode vs 单晶体管

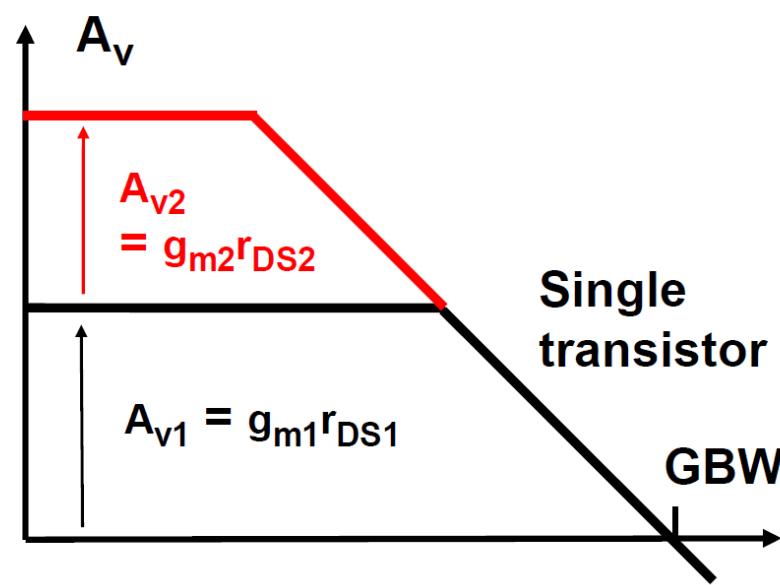
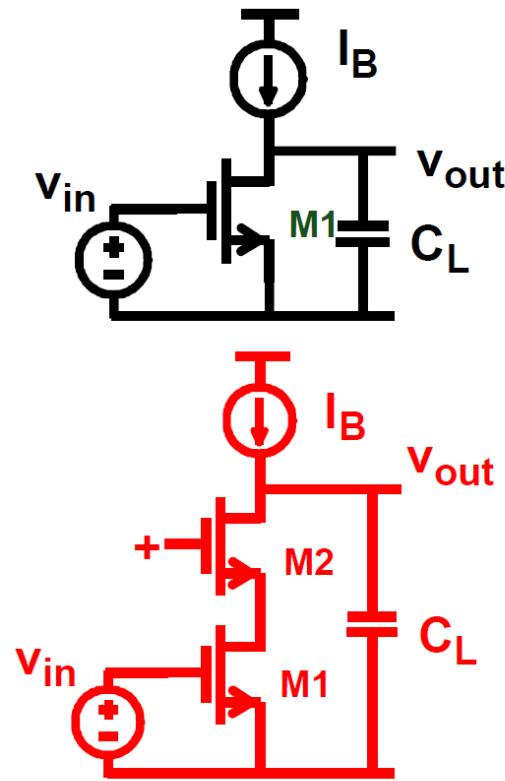


$$BW = \frac{1}{2\pi R_{out} C_L}$$

$$GBW = \frac{g_{m1}}{2\pi C_L} \quad \text{for both !}$$

- 增益带宽积不变！

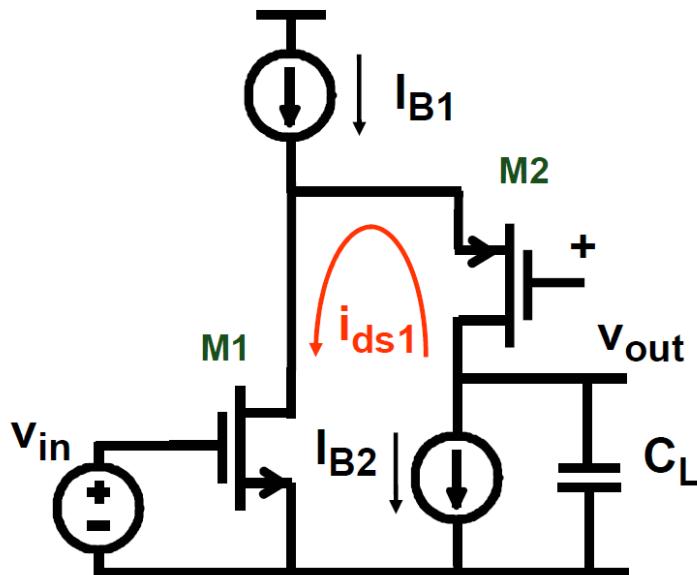
»» Cascode vs 单晶体管



在低频区域提供更高的增益，没有额外的电流消耗

$$GBW = \frac{g_m}{2\pi C_L}$$

》》 折叠式Cascode



$$I_{DS1} = I_{B1} - I_{B2} \approx I_{B1} / 2$$

$$A_v = g_{m1} R_{out}$$

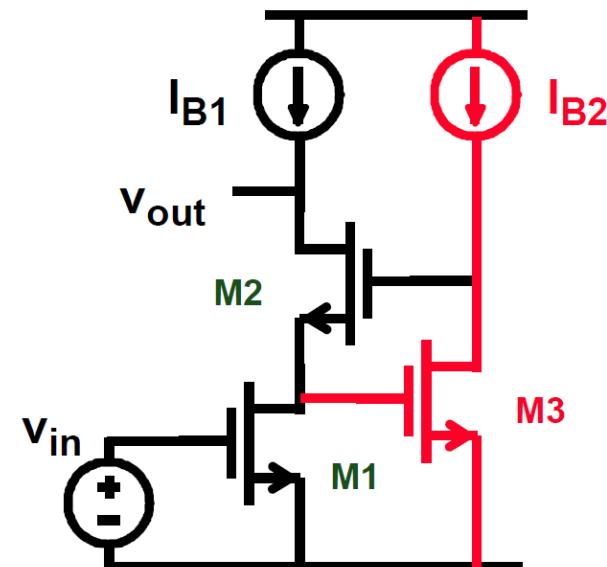
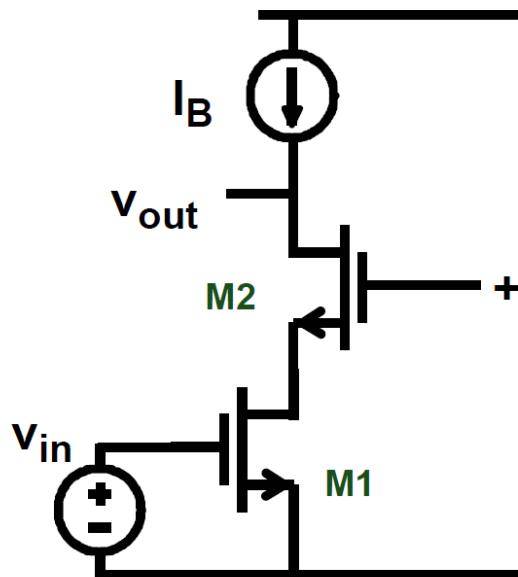
$$R_{out} = r_{DS1} g_{m2} r_{DS2}$$

$$BW = \frac{1}{2\pi R_{out} C_L}$$

$$GBW = \frac{g_{m1}}{2\pi C_L}$$

- 主要参数指标与套筒式一致，功耗是其两倍！

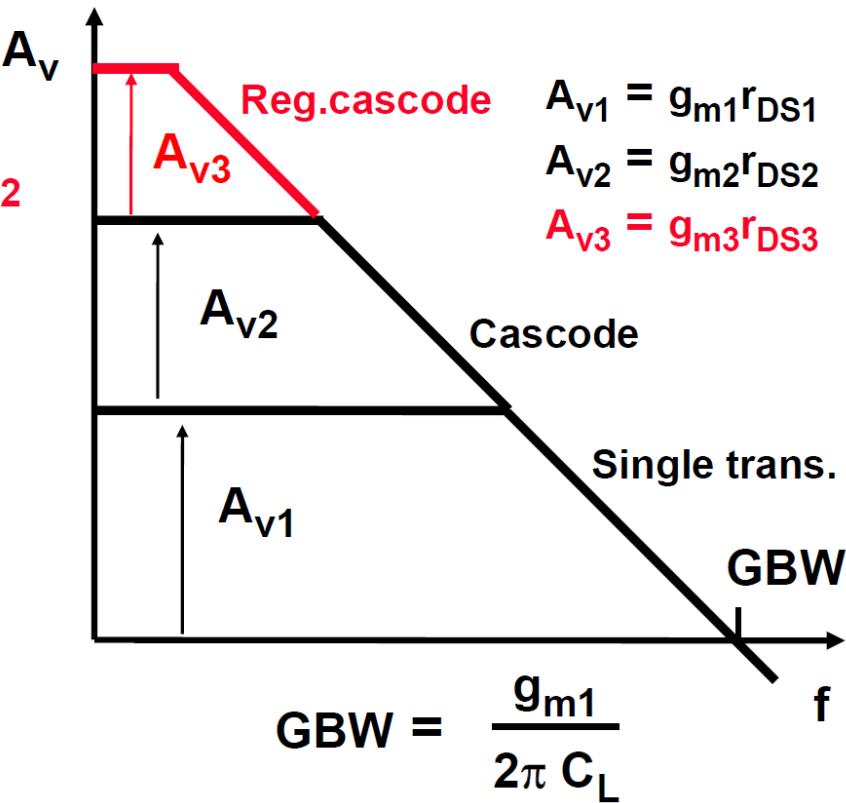
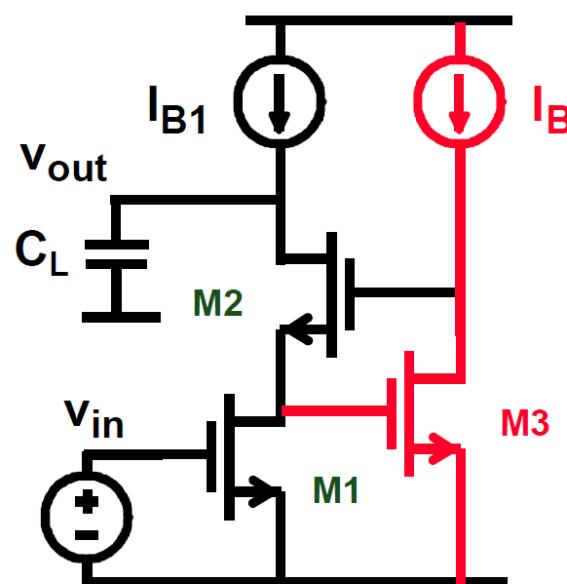
»» 调节式 (Regulated) Cascode



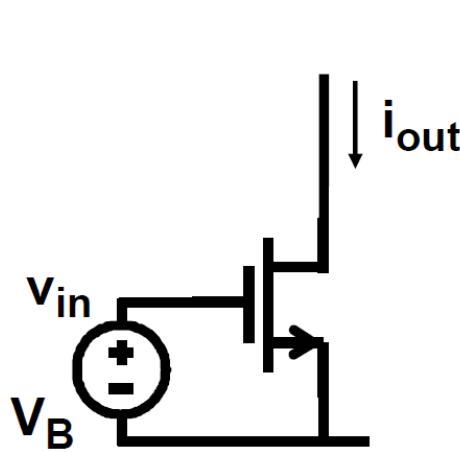
$$A_v = (g_m r_{DS})_1 (g_m r_{DS})_2$$

$$A_v = (g_m r_{DS})_1 (g_m r_{DS})_2 (g_m r_{DS})_3$$

》》 调节式 (Regulated) Cascode

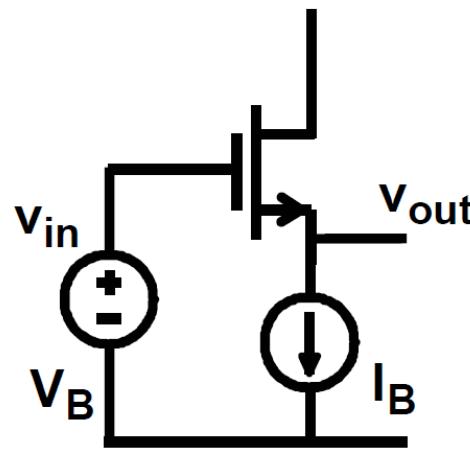


》》 单晶体管结构对比



$$i_{out} = g_m v_{in}$$

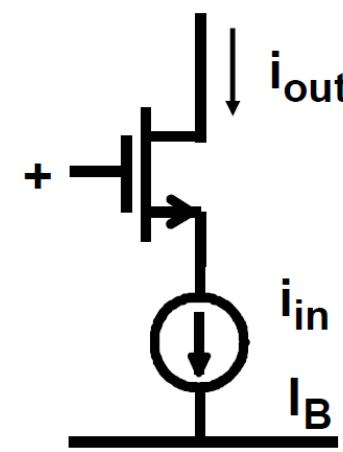
Amplifier



$$v_{out} = v_{in}$$

$$Z_{out} \approx 1/g_m$$

Source follower



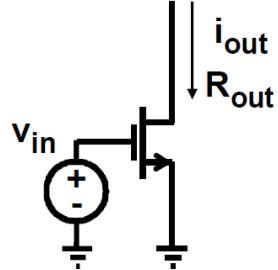
$$i_{out} = i_{in}$$

$$Z_{in} \approx 1/g_m$$

Cascode

》》低频特性对比

- 放大器

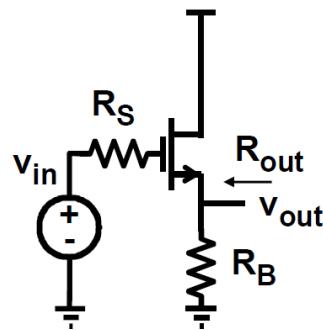


$$A_G \quad g_m$$

$$R_{in} \quad \infty$$

$$R_{out} \quad r_o$$

- 源极跟随器



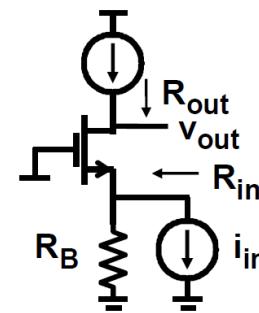
$$R_B > 1/g_m$$

$$A_V \quad 1$$

$$\infty$$

$$1/g_m$$

- Cascode



$$R_B > 1/g_m$$

$$A_R \quad g_m r_o R_B$$

$$R_B$$

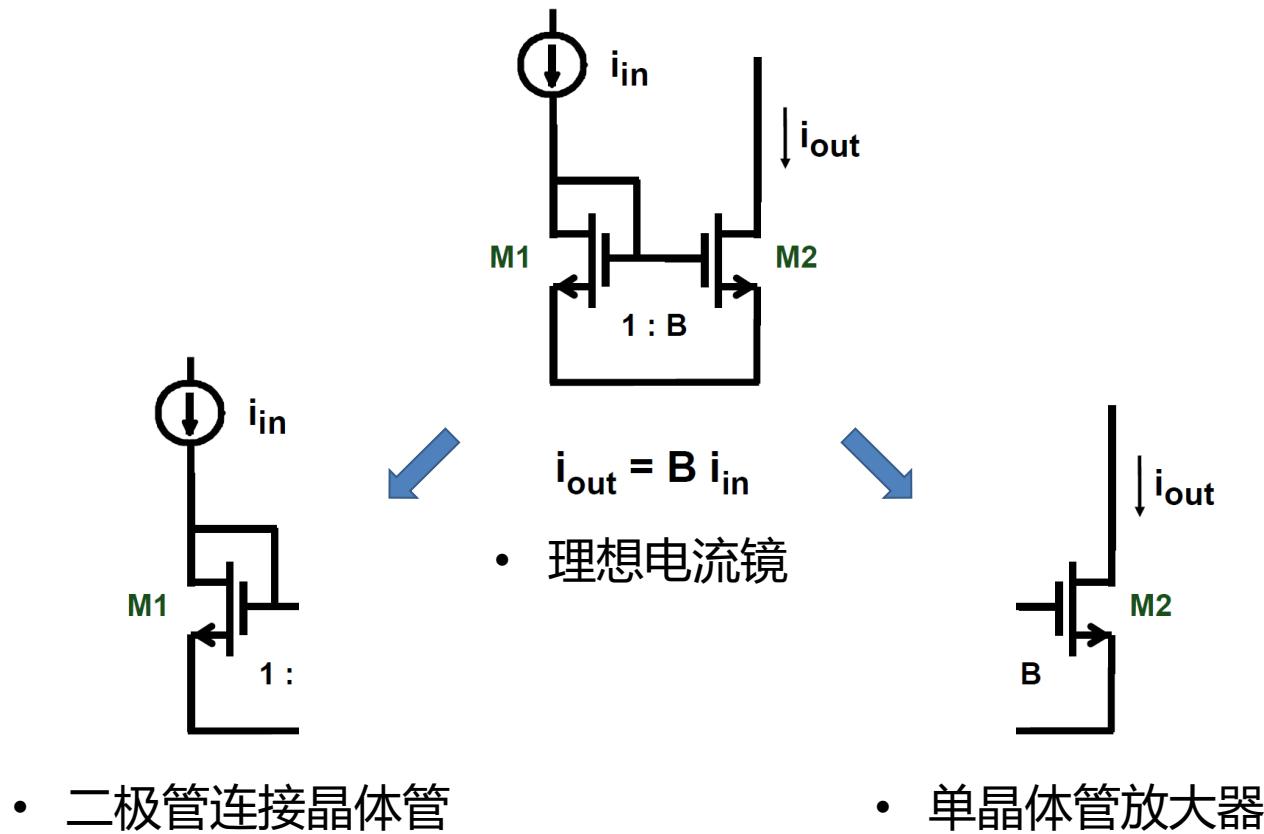
$$g_m r_o R_B$$



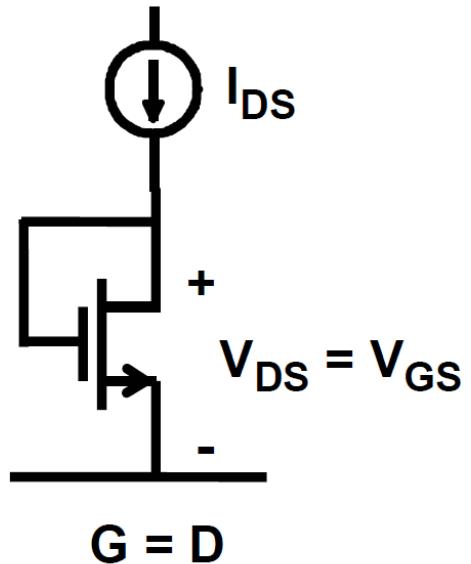
模拟电路的基本结构

1. 单晶体管放大器
2. 源极跟随器
3. Cascode (共源共栅极)
- 4. 电流镜**
5. 差分对

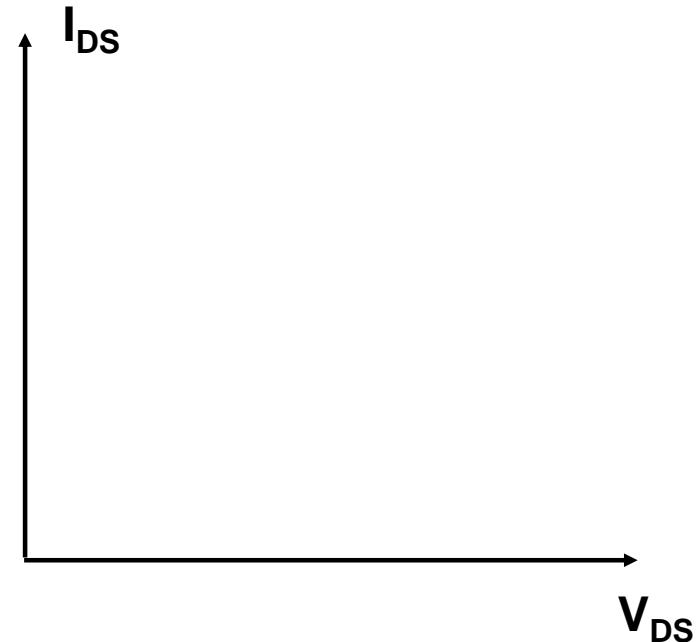
》》 电流镜 (Current Mirror)



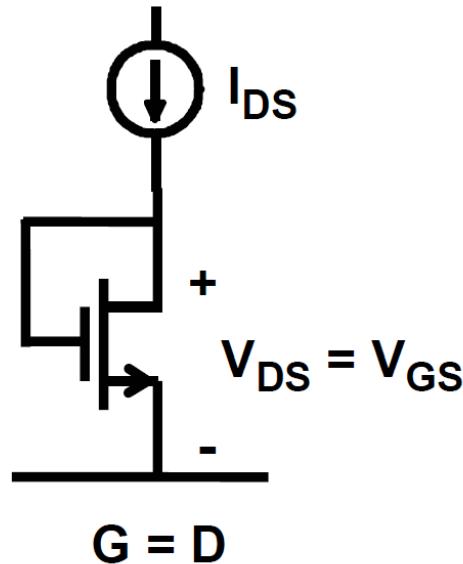
》》 二极管连接晶体管 (Diode-connected)



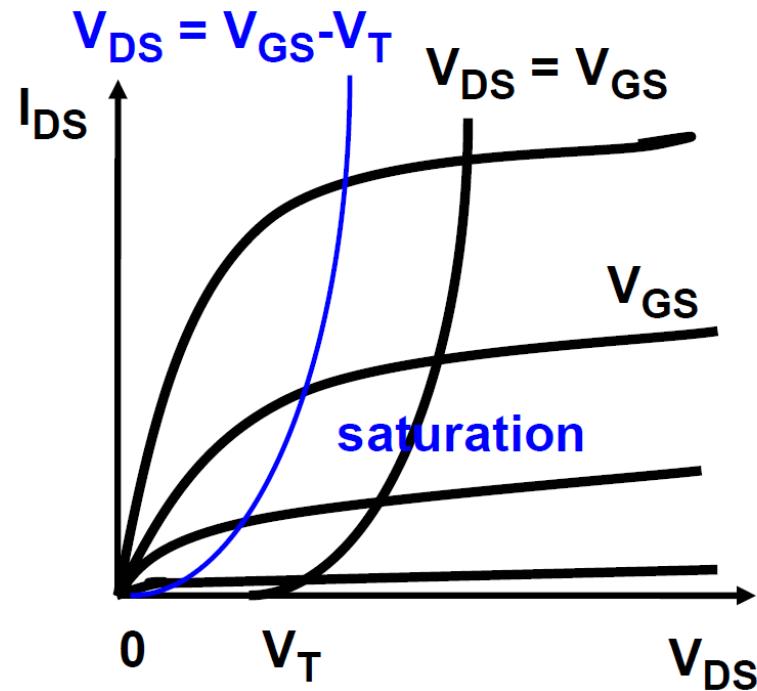
$$I_{DS} = K_n \frac{W}{L} (V_{DS} - V_T)^2$$



二极管连接晶体管 (Diode-connected)

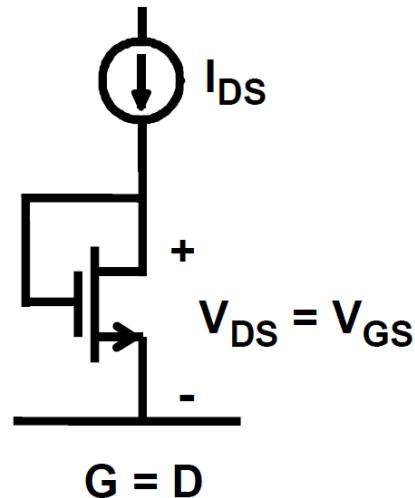


$$I_{DS} = K_n \frac{W}{L} (V_{DS} - V_T)^2$$

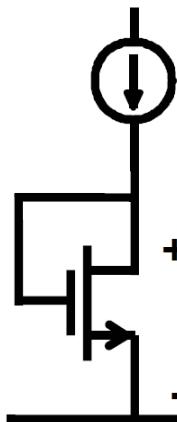


》》二极管连接的小信号模型

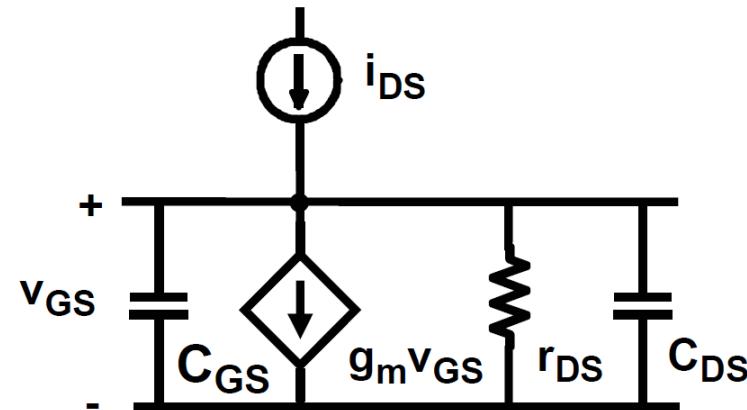
口求二极管连接方式的输入电阻和带宽?



二极管连接的小信号模型



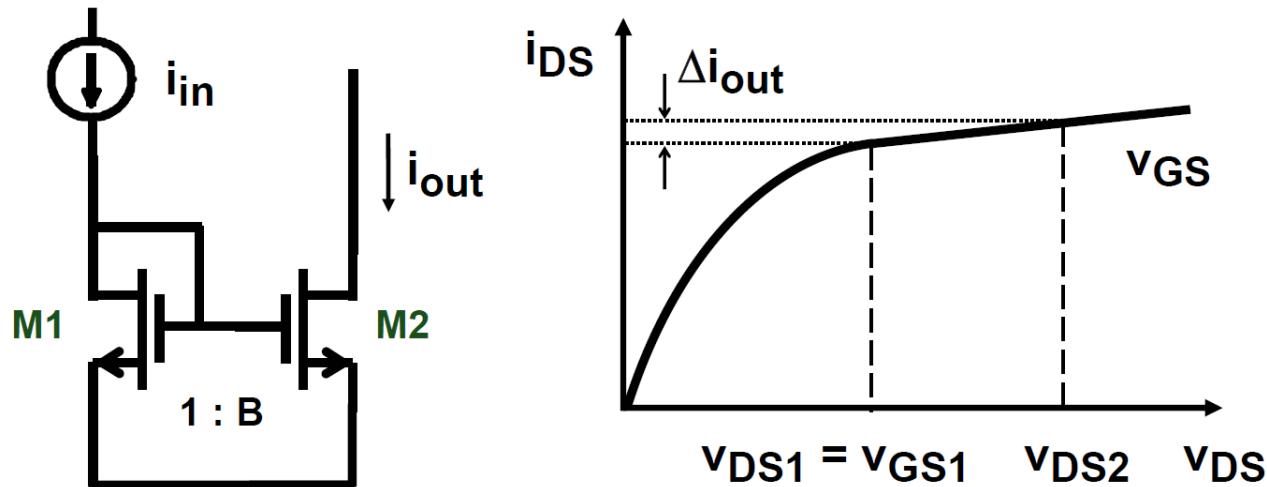
$$G = D$$



输入电阻 $r_{ds} = 1/g_m \parallel r_{DS} \approx \boxed{1/g_m}$

带宽 $BW = \frac{g_m}{2\pi(C_{GS}+C_{DS})} \approx \frac{f_T}{2}$

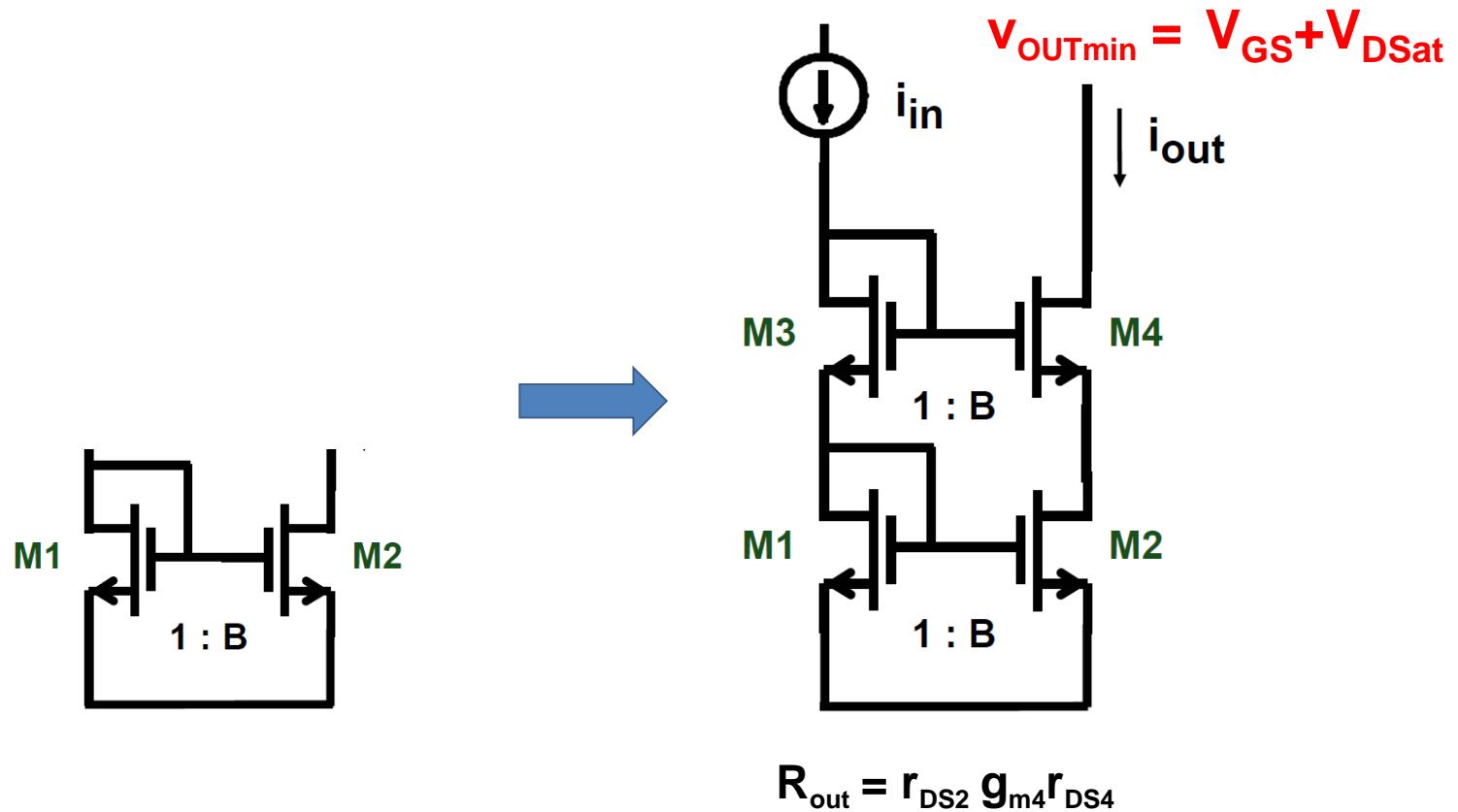
》》 电流镜的输出特性



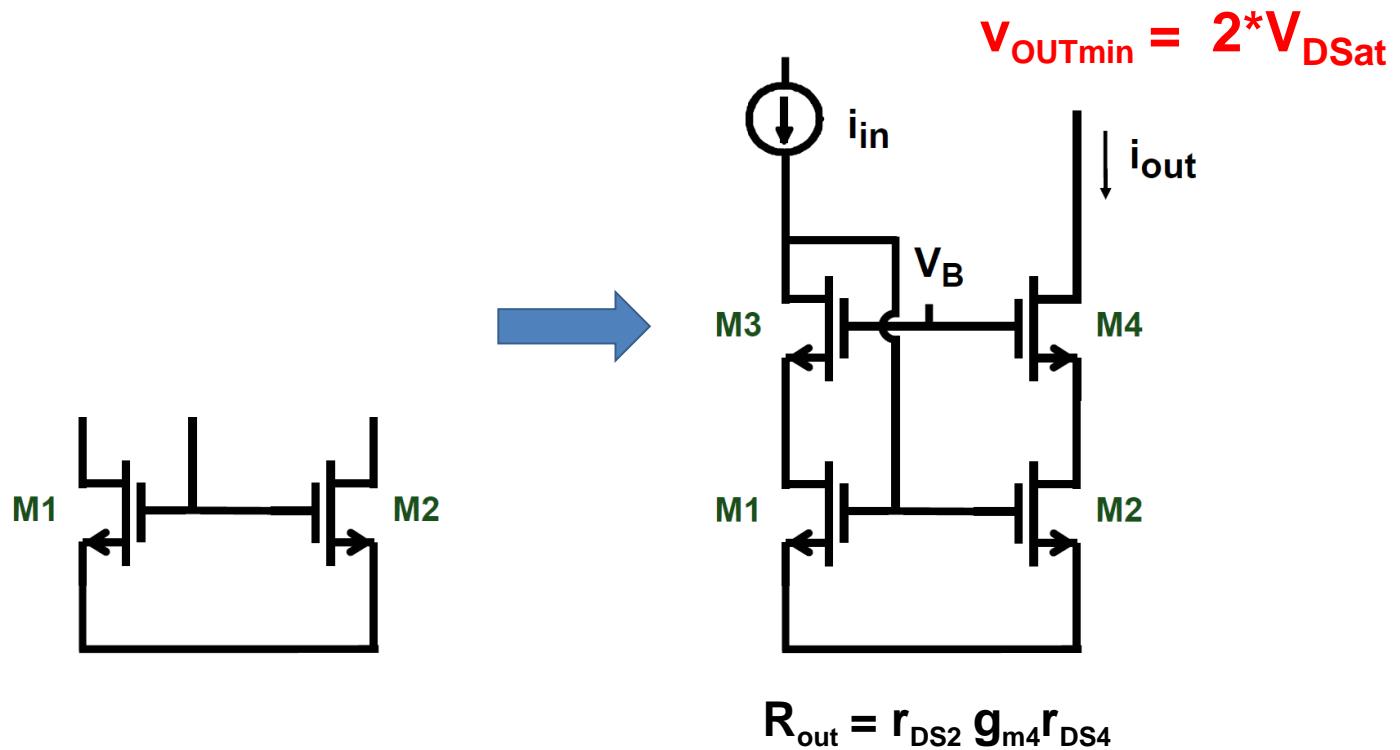
- 电流镜的输出阻抗即是单晶体管放大器的输出阻抗
- 电流镜的输出精度可以描述为

$$\frac{\Delta i_{out}}{i_{out}} =$$

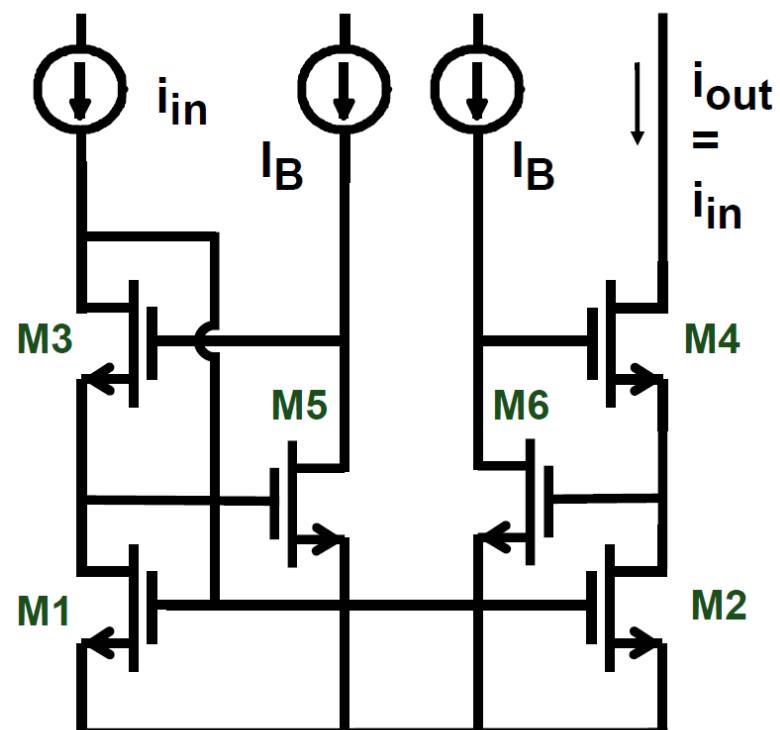
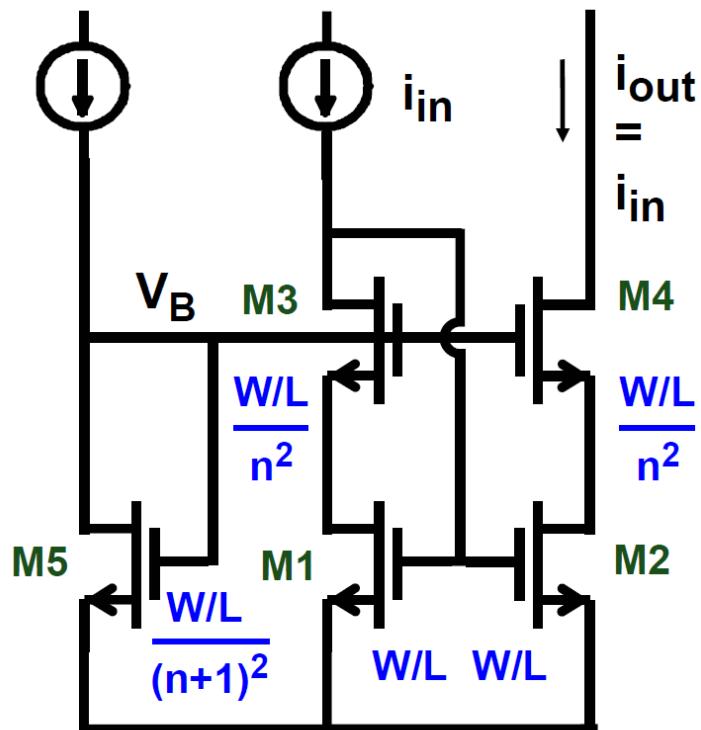
》》改进型的电流镜



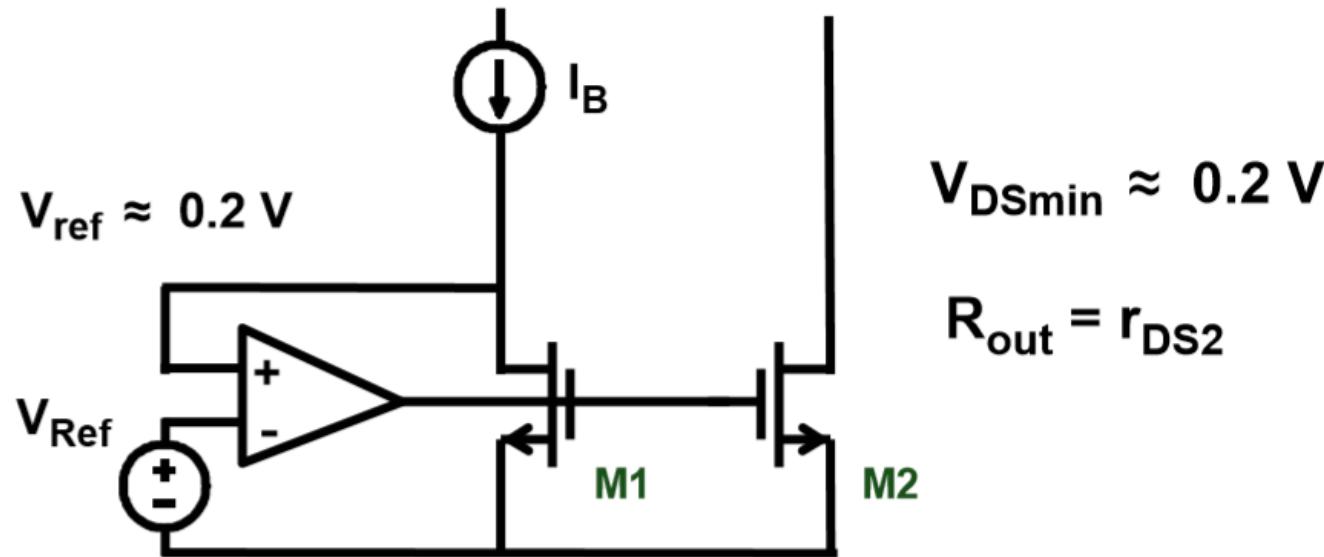
»» 改进型的电流镜



》》 电流镜案例



» 低电压电流镜

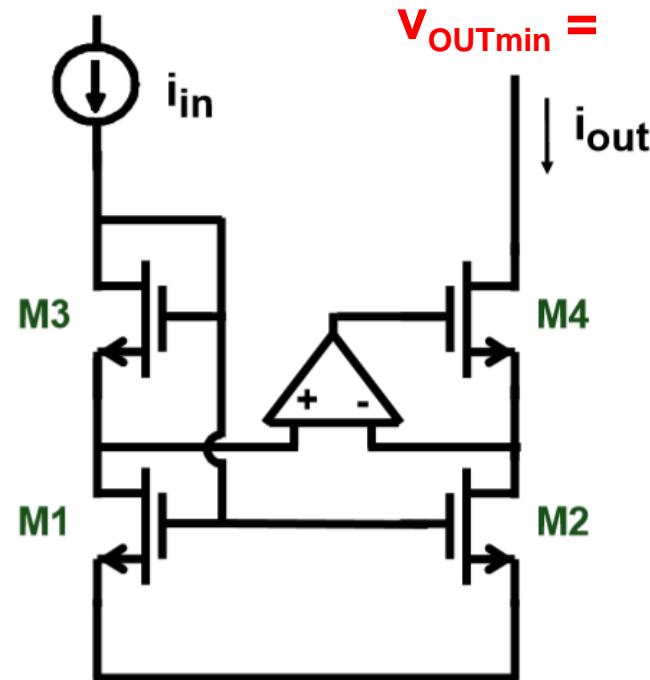
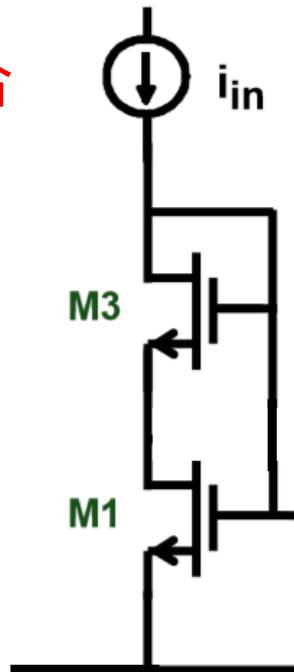


- 该电路**不能**改善输出电阻
- 该电路**可以**改善系统性失配问题

»» 超低电压电流镜

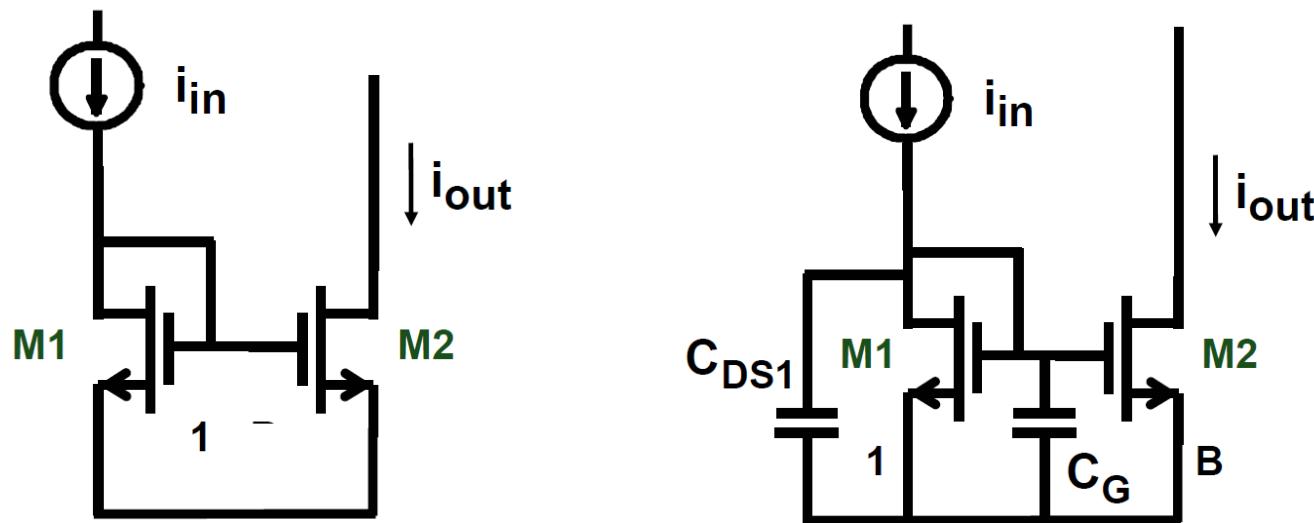
□此结构是否是合适的Cascode?

● 不是!



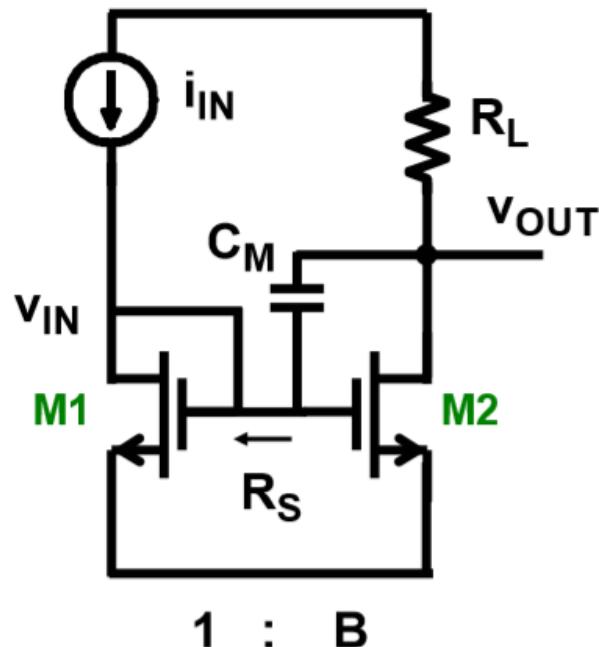
- 电流镜晶体管工作在线性区，通过运放锁定 V_{ds} ，使得两个晶体管工作电压完全一致！

》》 电流镜的高频特性



$$BW = \frac{g_m}{2\pi (C_G + C_{DS1})} \approx f_T \frac{1}{(2 + B)}$$

》》 电流镜中的密勒效应



Miller effect :

$$f_{-3dB} = \frac{1}{2\pi R_S A_{v2} C_M}$$

$$R_S = 1/g_{m1} \quad A_{v2} = g_{m2} R_L$$

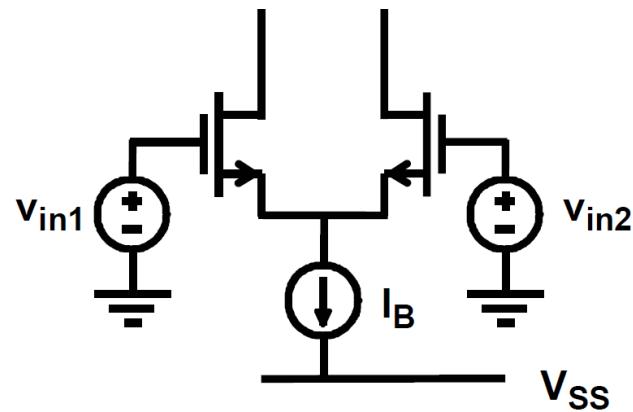
$$f_{-3dB} = \frac{1}{2\pi (1+B) C_M R_L}$$



模拟电路的基本结构

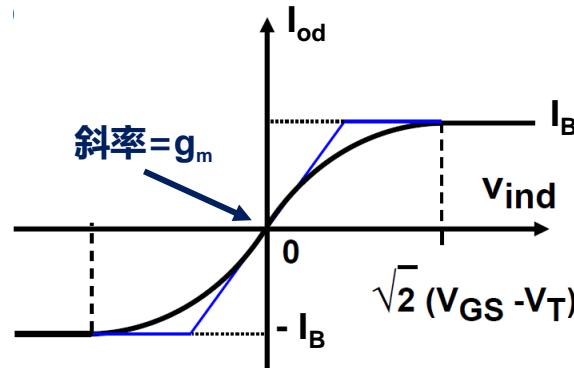
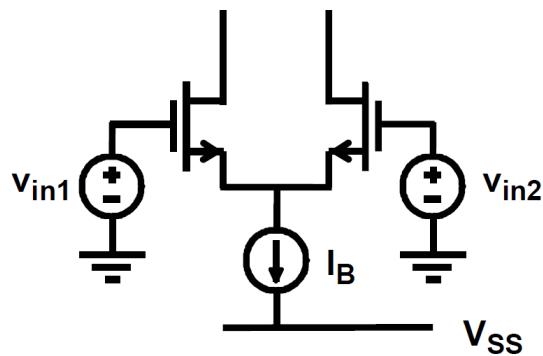
1. 单晶体管放大器
2. 源极跟随器
3. Cascode (共源共栅极)
4. 电流镜
5. 差分对

》》 差分对 (Differential Pair)



- 差分对的本质依旧是**电压输入电流输出**
- 差分对中的信号均以**差分**形式体现
- 差分对的能效是单晶体放大器的**一半**

》》 差分对 (Differential Pair)



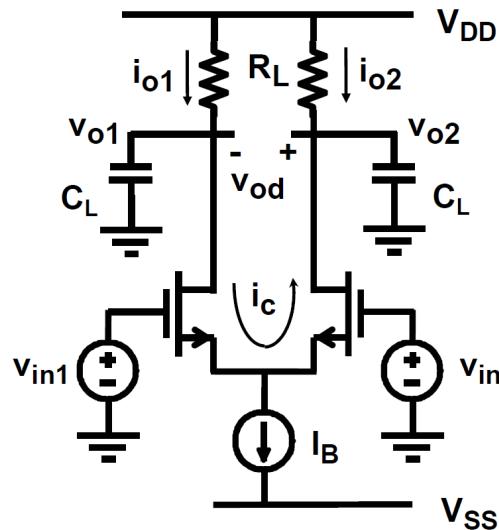
$$\frac{i_{Od}}{I_B} = \frac{v_{Id}}{(V_{GS}-V_T)} \sqrt{1 + \frac{1}{4} \left(\frac{v_{Id}}{V_{GS}-V_T} \right)^2}$$

- V_{Id} 为差分输入电压
- I_{Od} 为差分输出电流
- I_B 为差分对总偏置电流

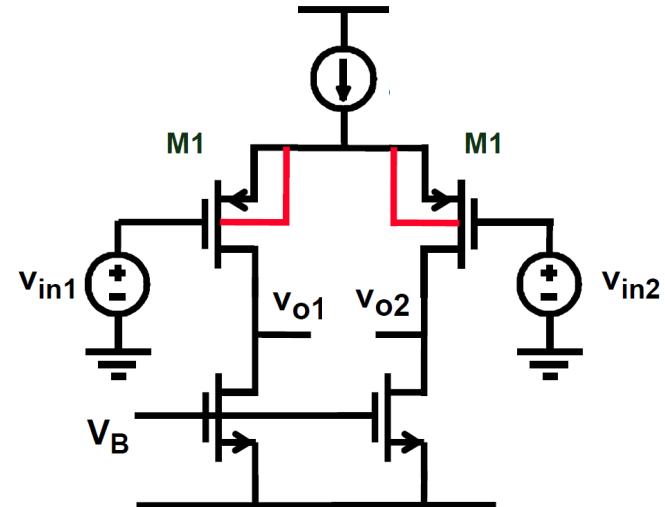
• $V_{GS}-V_T$ 决定 g_m 和 直流 范围

》》》 差分放大器

- 差分放大器 = 差分对 + 负载



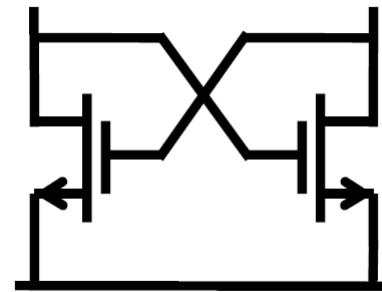
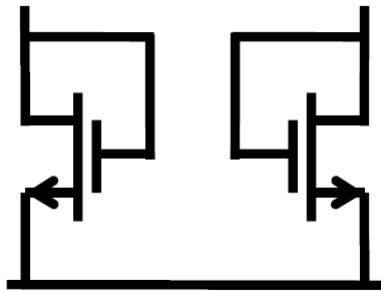
$$A_v = g_m R_L$$



$$A_v = g_{m1} (r_{DS1} // r_{DS2})$$

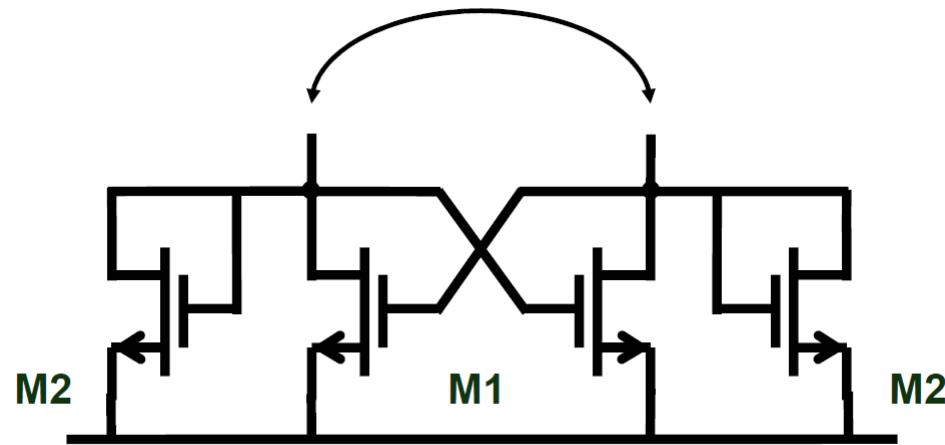
»» 特殊形态的负载-交叉耦合对

- 交叉耦合对 (Cross Coupled Pair)



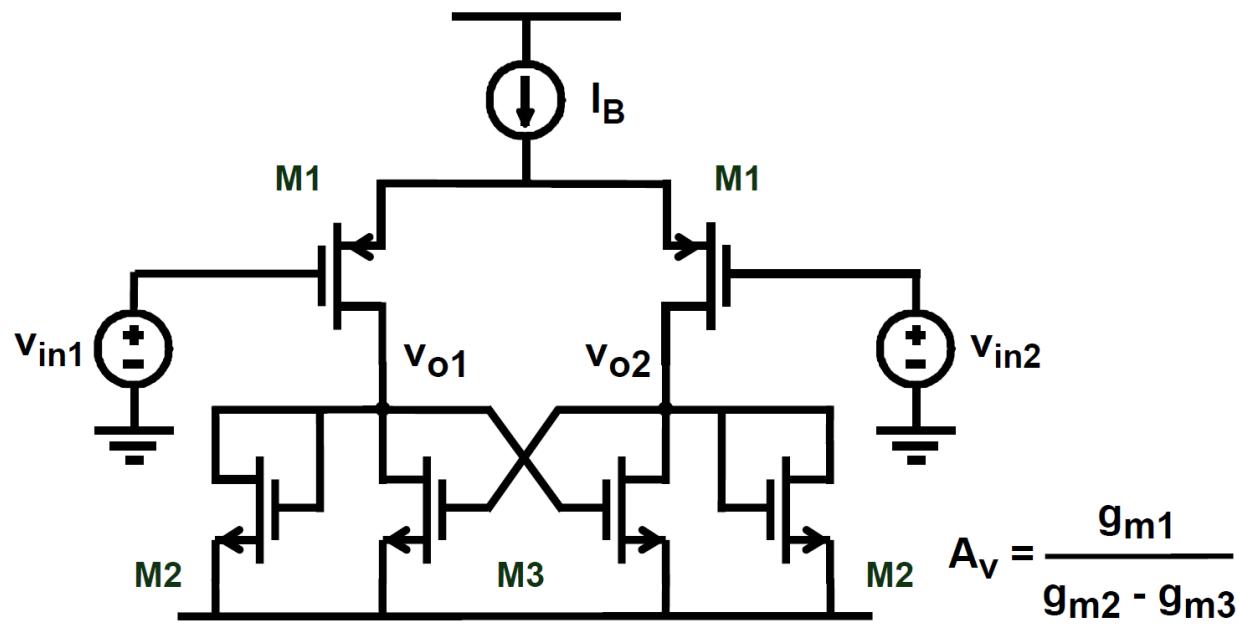
» 特殊形态的负载-交叉耦合对

差分输入电导: $g_{m2} - g_{m1}$



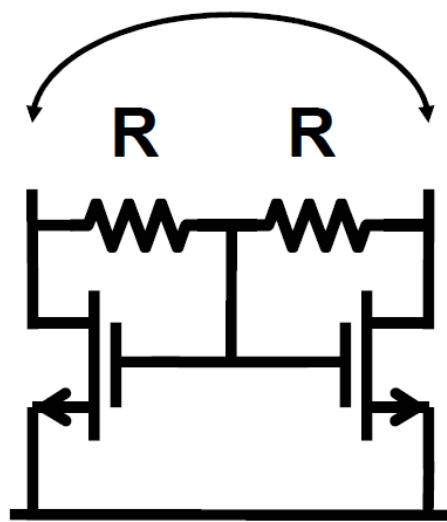
实际使用中受到匹配(matching)的限制

» 特殊形态的负载-交叉耦合对



实际使用中受到**匹配(matching)**的限制

»» 特殊形态的负载-共模反馈

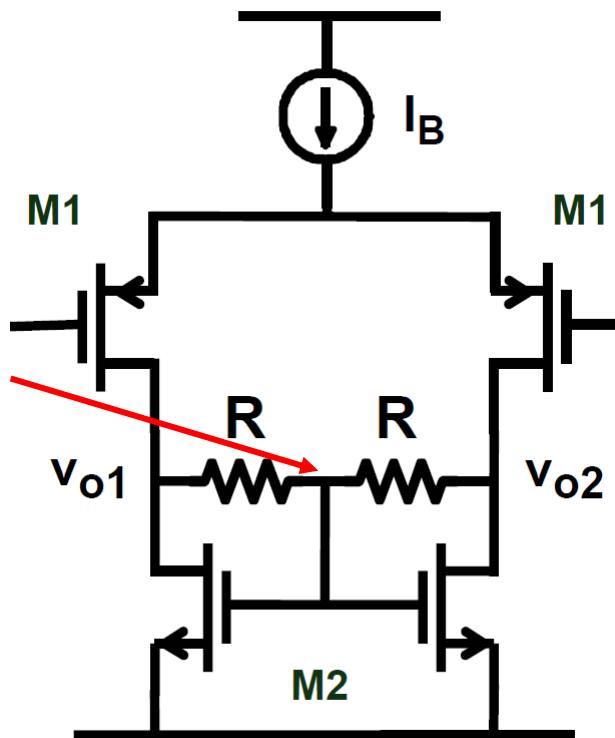


»» 特殊形态的负载

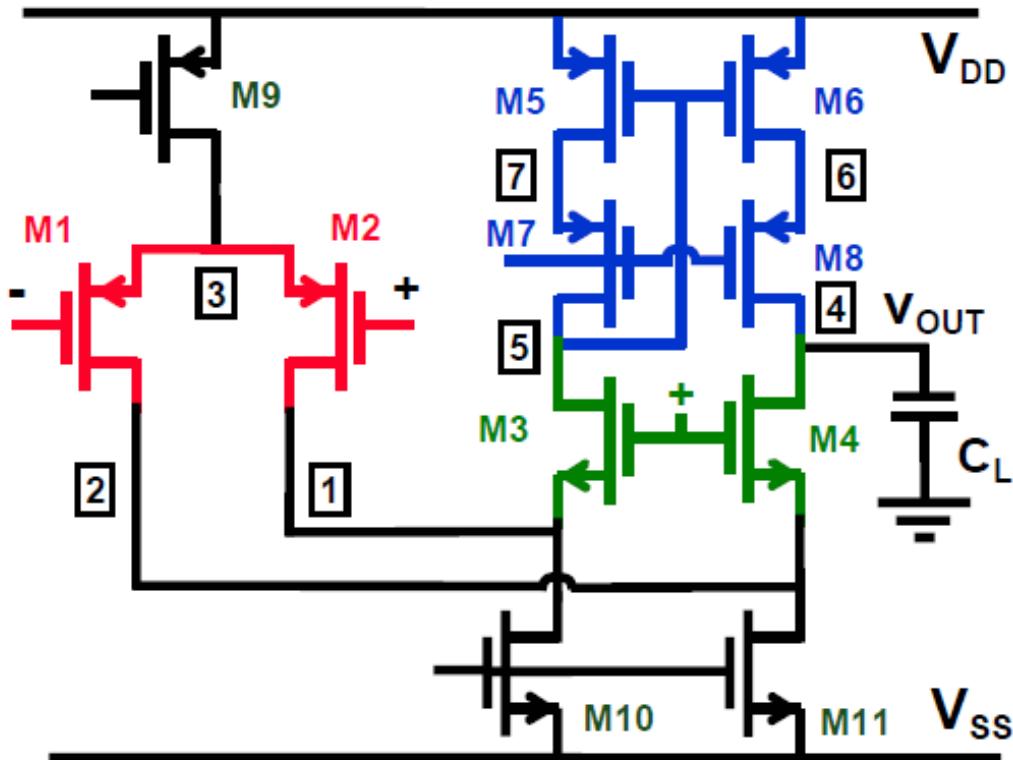
- 本质上是一种**共模反馈**形式

$$A_v = g_{m1} (R // r_o)$$

$$r_o = r_{o1} // r_{o2}$$



»» Cascode



求该折叠套筒型运放的第一和第二高阻点的阻值，用公式表示。

》》》 总结

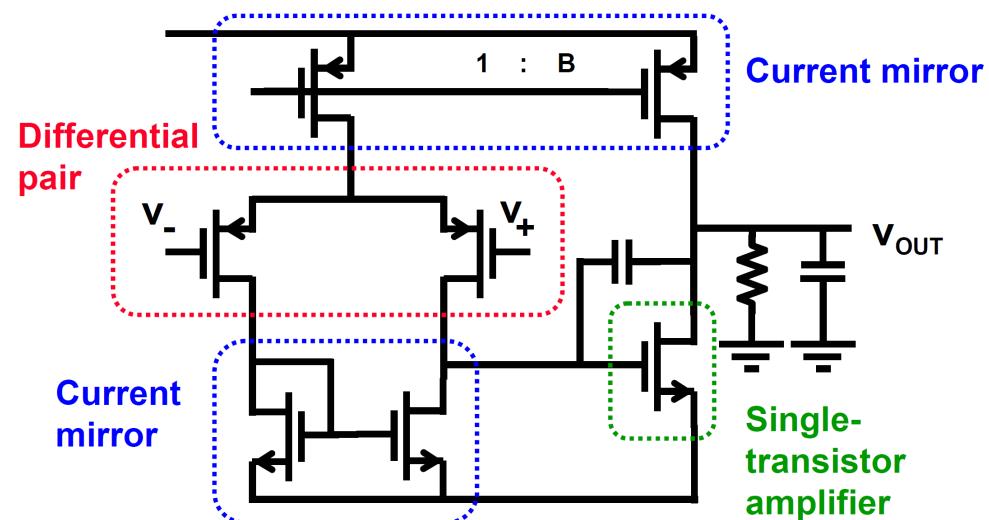
□ 模拟电路的基本构成单元：

1. 单晶体管

- 放大器
- 源极跟随器
- Cascode

2. 多晶体管

- 差分对
- 电流镜



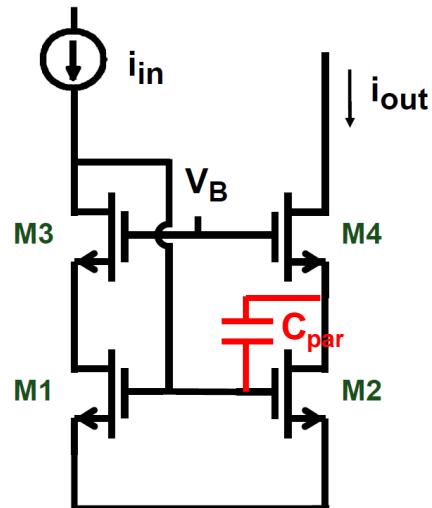


作业1

- 利用仿真结果，找到我们所使用工艺的 $u_{0p,n}$, C_{ox} , V_{THn} , V_{THp}

》》作业2

- 通过公式描述 V_B 的取值范围 (提示：晶体管M1-M4均需要工作在饱和区)
- 在Cascode电流镜中，假设有寄生电容 C_{par} ，利用公式估算并用仿真验证该电流镜的频率特性。 (可以自由设置偏置、晶体管的尺寸以及寄生电容)





作业3

- 假设差分对偏置电流为200uA， $W/L=20\mu m/1\mu m$ ，根据理论分析和仿真验证。
 - 计算 $g_m > 99\% * g_{m,max}$ 的区间。
 - 计算差分输出电流为198uA时的差分输入电压。
 - 如果需要把问题2中求得的电压扩大一倍，差分对的W需要如何修改？

第3章 噪声



北京航空航天大學
BEIHANG UNIVERSITY

| 微电子学院

CMOS模拟集成电路设计

第三章：噪声

胡远奇

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噪声 Noise

- **噪声的特点**
- 系统中的噪声
- 电阻的热噪声
- 晶体管的噪声源
- 等效噪声的换算



噪声

- 为什么它很重要?
- 信噪比 (Signal-to-Noise Ratio, SNR)
 - 信号功率 $P_{sig} \sim V_{DD}^2$
 - 噪声功率 $P_{noise} \sim kT/C$
 - $SNR = P_{sig} / P_{noise}$
- 工艺演进
 - V_{DD} 下降 -> SNR下降
 - 保持SNR -> 增加C -> 功耗提升
- 优秀的低功耗设计意味着对噪声的充分了解

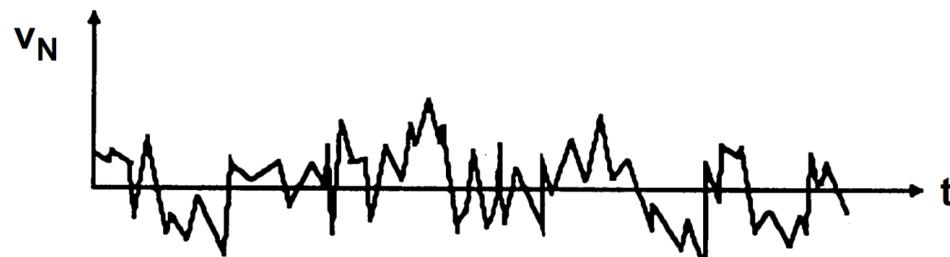


噪声的类型

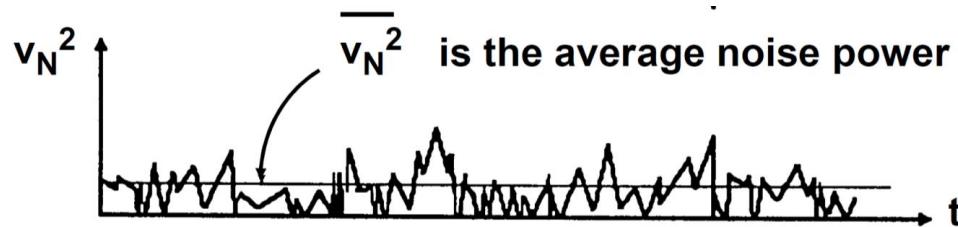
- 干扰（人为造成的）
 - 信号耦合
 - 电容
 - 电感
 - 基底
 - 键合线
 - 电源噪声
 - 解决方案：差分电路、版图技巧
- **器件噪声**
 - 由电荷的不连续性造成
 - 根本性的噪声

》》 噪声

- 时域上的表现形式：随机出现，通过**概率**表征

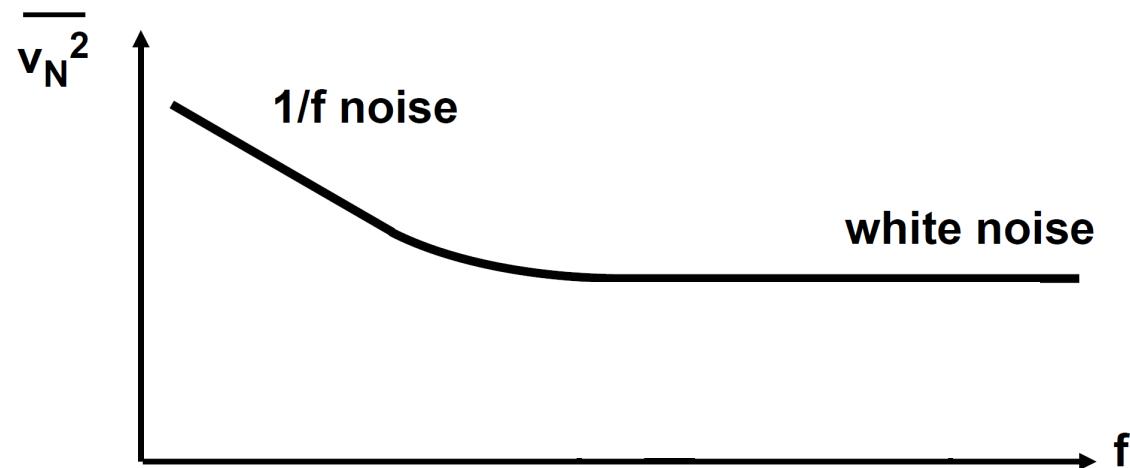


- 噪声的强度通过**平均功率**表达



》》 噪声

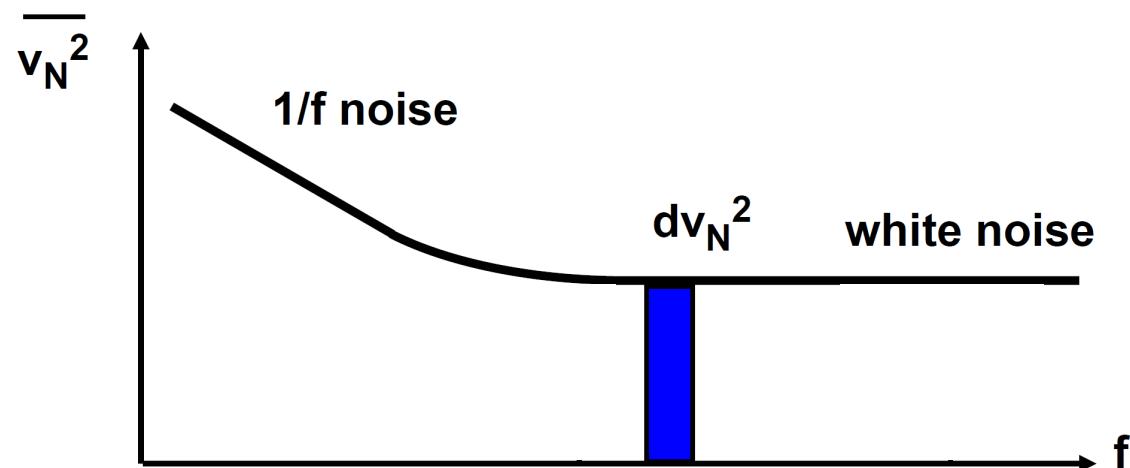
- 频域上的表现形式：



- 低频区域**闪烁噪声**
(Flicker Noise)
- 高频区域**白噪声**

》》 噪声

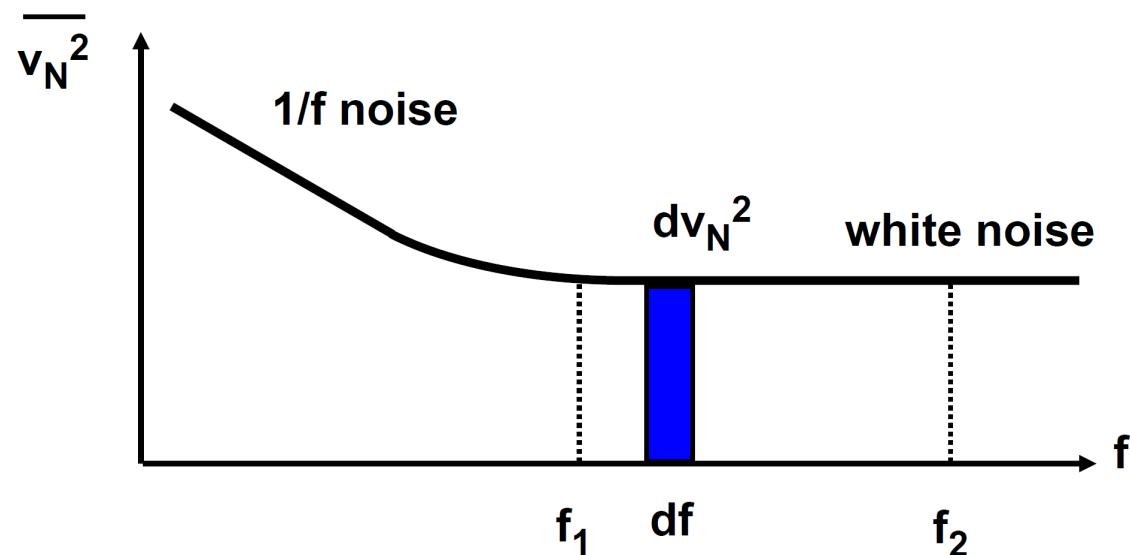
- 频域上的表现形式：



- 噪声的**功率谱密度**: V^2/Hz
 - 如何计算总噪声?

》》 噪声

- 频域上的表现形式：



- 积分噪声： $\overline{v_{N,int}^2} = \int_{f_1}^{f_2} d\overline{v_N^2} df = (f_2 - f_1) \overline{v_N^2}$



噪声

- 当我们描述一个噪声时，通常的形式是：
 - 特定频率下表述其功率谱密度（均方根）
 - 一定带宽内，表述其积分噪声总量



噪声 Noise

- 噪声的特点
- **系统中的噪声**
- 电阻的热噪声
- 晶体管的噪声源
- 等效噪声的换算



噪声因子(Noise Factor)

- 一个系统噪声性能的衡量指标：

$$\text{噪声因子 } F = \frac{\text{总的噪声输出功率}}{\text{输入噪声源引起的噪声功率}}$$

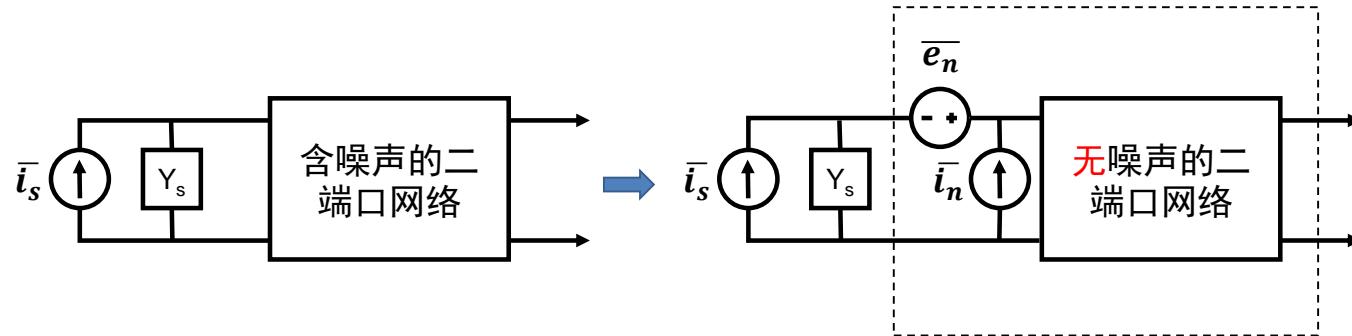


图：噪声源驱动一个含噪声的二端网络

》》 噪声因子(Noise Factor)

- 一个系统噪声性能的衡量指标：

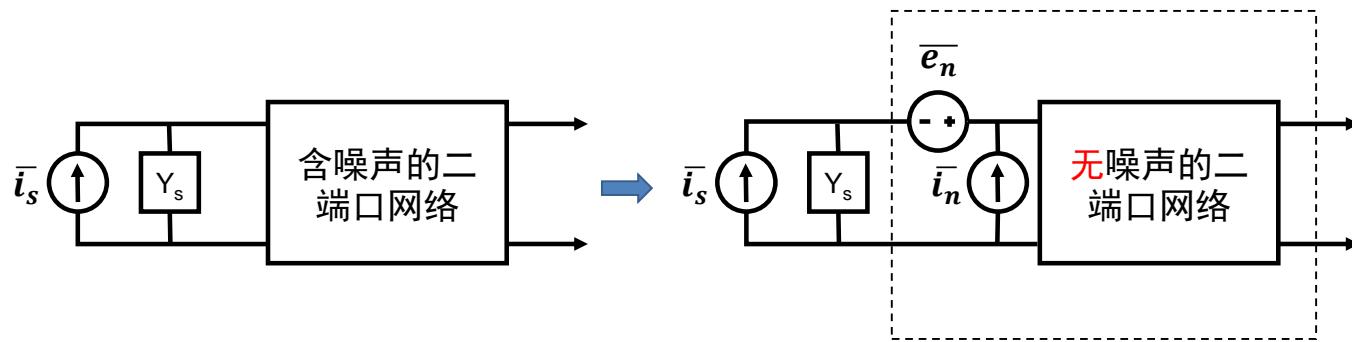
$$\text{噪声因子 } F = \frac{\text{总的噪声输出功率}}{\text{输入噪声源引起的噪声功率}}$$



- 通常我们更关注系统或电路的**输入参考噪声**(Input-Referred Noise)

》》 噪声因子(Noise Factor)

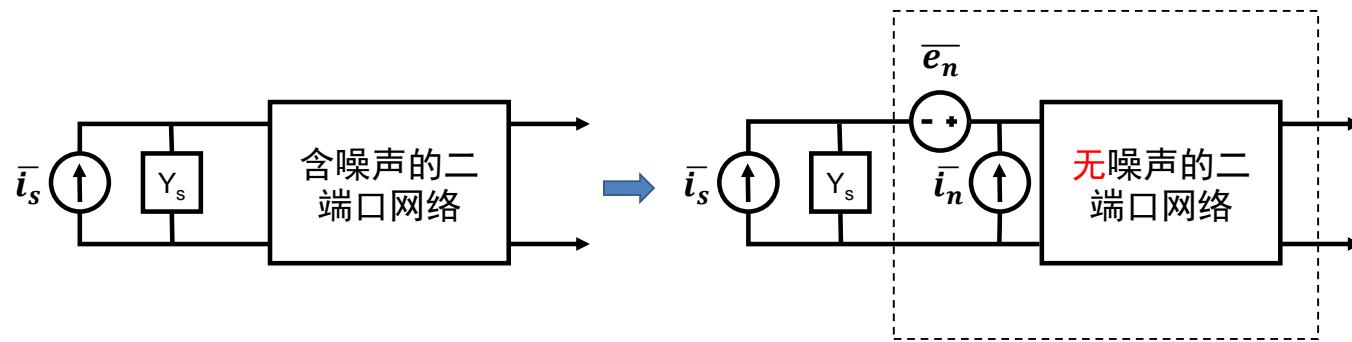
- 一个系统噪声性能的衡量指标：



噪声因子 $F =$

》》 噪声因子(Noise Factor)

- 一个系统噪声性能的衡量指标：

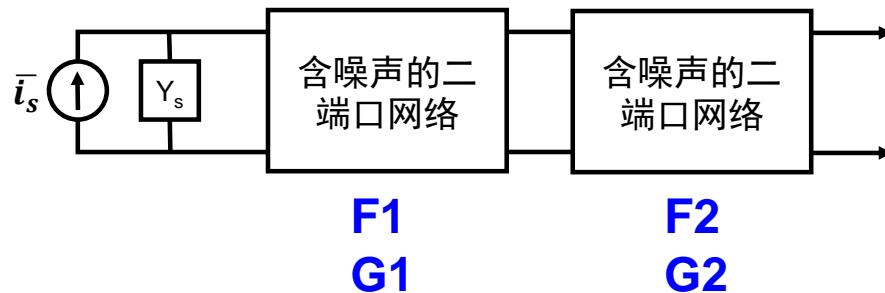


$$\text{噪声因子 } F = \frac{\bar{i}_s^2 + |\bar{i}_n + Y_s \bar{e}_n|^2}{\bar{i}_s^2} = \frac{SNR_{IN}}{SNR_{OUT}}$$

- 注意：输入参考噪声电压/电流 e_n 和 i_n 可能具有相关性

》》 噪声因子(Noise Factor)

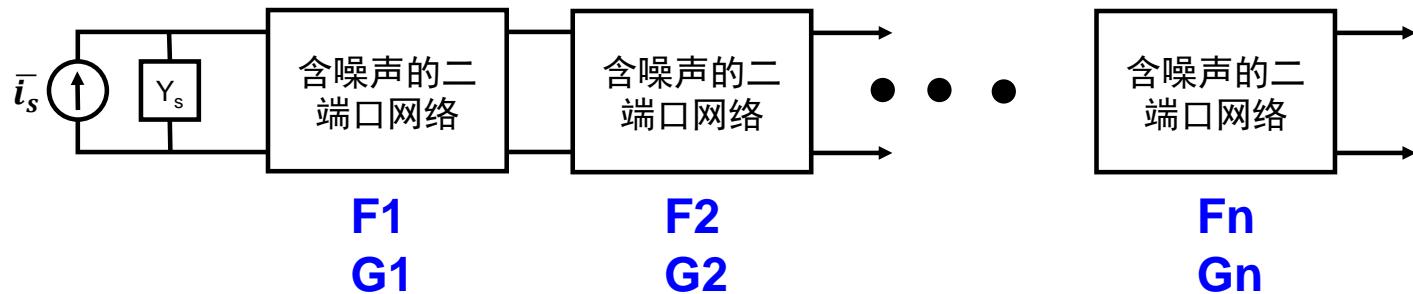
- 一个两级系统的噪声指标：



$$\text{总噪声因子 } F = F_1 + \frac{F_2 - 1}{G_1}$$

》》 噪声因子(Noise Factor)

□求一个n级系统的噪声指标?



$$\text{总噪声因子 } F = F_1 + \frac{F_2 - 1}{G_1} + \cdots + \frac{F_n - 1}{G_1 \cdot G_2 \cdot \cdots \cdot G_n}$$

噪声因子最低的系统在第一级!

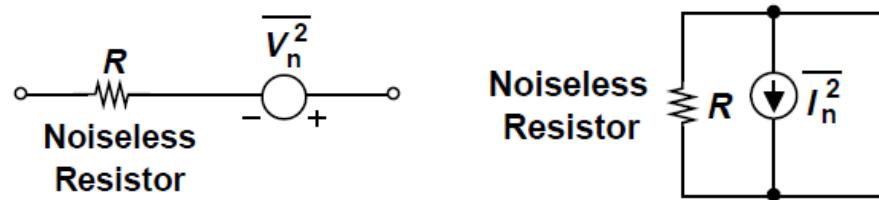


噪声 Noise

- 噪声的特点
- 系统中的噪声
- **电阻的热噪声**
- 晶体管的噪声源
- 等效噪声的换算

》》 电阻的热噪声

- 电阻的热噪声既可以用串联电压源表示，也可以用并联电流源来表示：

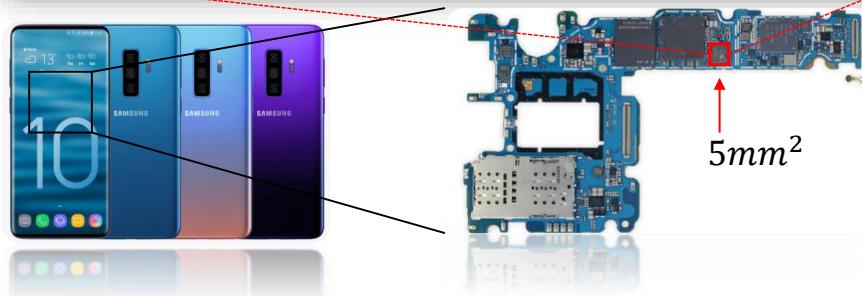
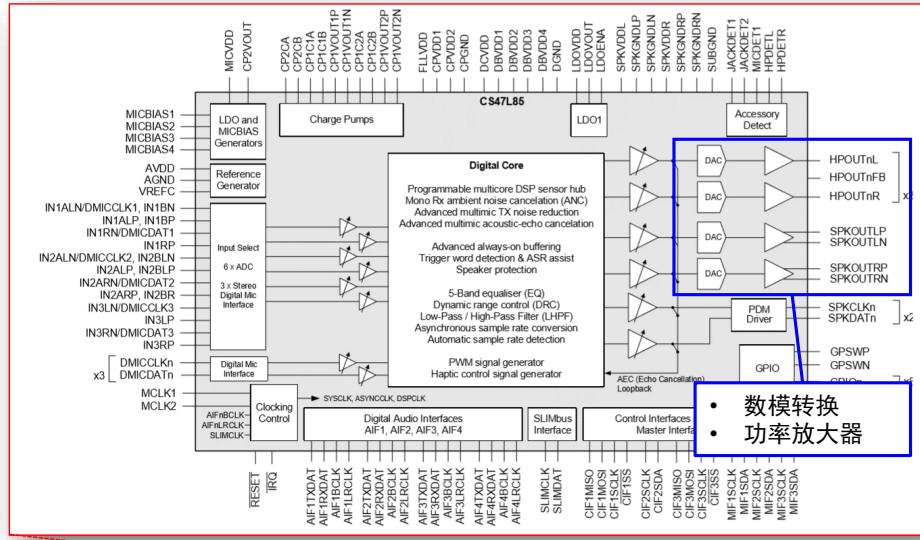


功率谱: $\overline{dV_n^2} = 4kTR$ $\overline{dI_n^2} = 4kT/R$

已知 $R=1\text{k}\Omega$, $T=300\text{K}$, $\sqrt{\overline{dV_n^2}} = 4\text{nV}_{\text{RMS}}/\sqrt{\text{Hz}}$



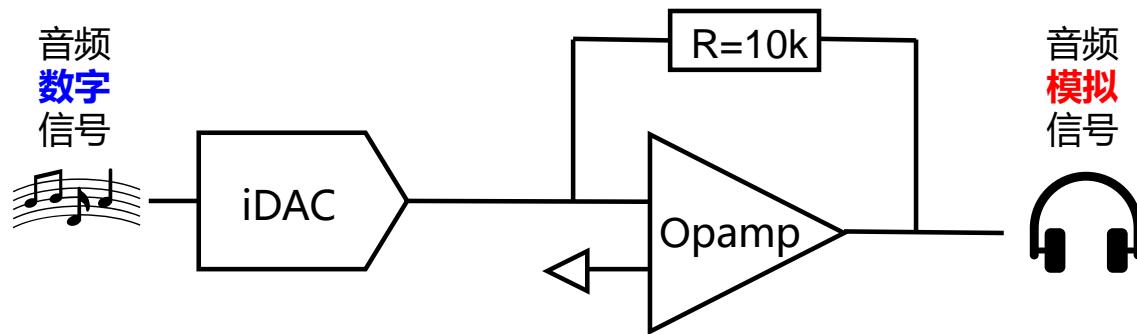
电阻的热噪声



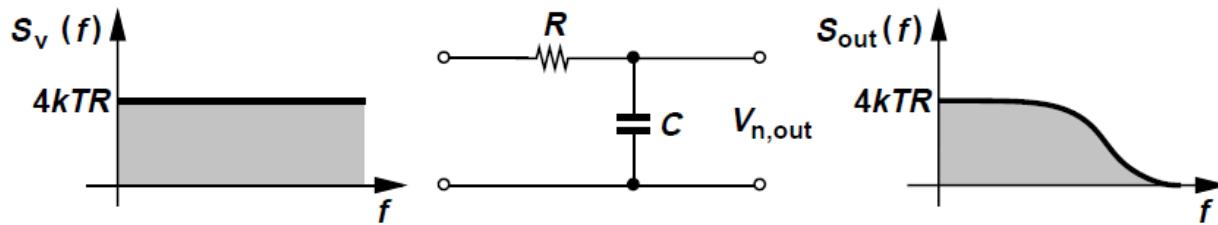
5mm²

》》 电阻的热噪声

有一音频功放系统，它的基本模块如下图所示，求该系统输出的理论最小噪声？ (20-20KHz)



》》 电阻的积分噪声



$$\overline{d\nu_n^2} = 4kTR$$

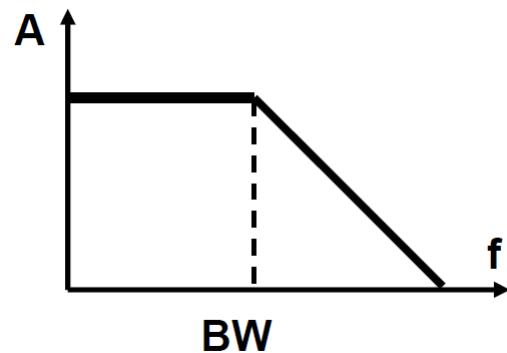
$$H(s) = \frac{1}{1 + s \cdot RC}$$



$$\overline{\nu_n^2} = \int_0^{\infty} 4kTR \cdot H^2(s) ds$$

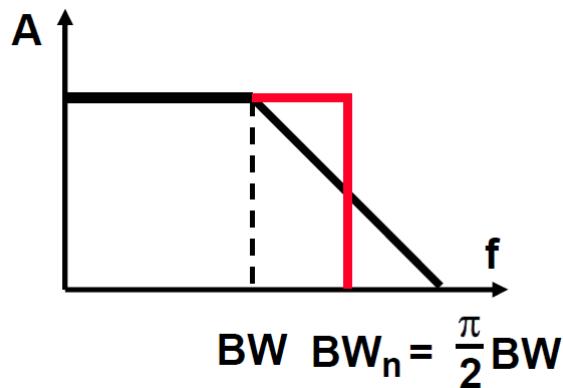


电阻的积分噪声



$$\int_0^{\infty} \frac{1}{1 + (\omega RC)^2} d\omega$$

》》 电阻的积分噪声



$$\int_0^{\infty} \frac{dx}{1+x^2} = \frac{\pi}{2}$$

$$BW_{nL} = \frac{\pi}{2} BW$$

$$\overline{v_n^2} = 4kTR \cdot \frac{1}{2\pi RC} \cdot \frac{\pi}{2} = \frac{kT}{C}$$

C_L = 1pF时
v_s = 65uV_{RMS}

- 所有**开关采样**电路的噪声极限由该公式表达

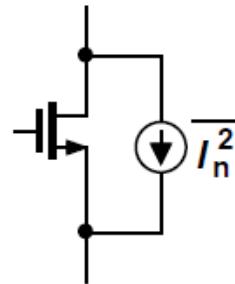


噪声 Noise

- 噪声的特点
- 系统中的噪声
- 电阻的热噪声
- **晶体管的噪声源**
- 等效噪声的换算

»» 晶体管的噪声

- 晶体管的**沟道电阻**和其他电阻一样，也会产生热噪声

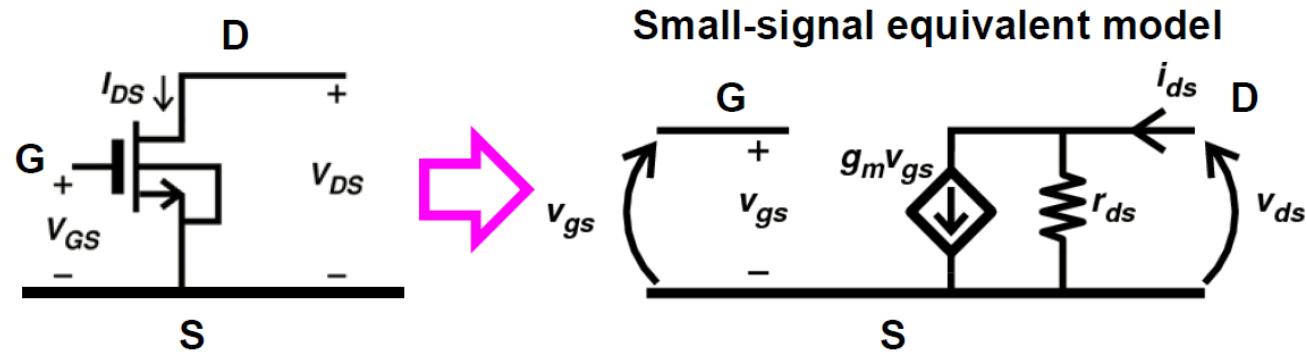


$$\overline{di_n^2} = 4kT/R = 4kT\gamma g_m$$

$$\gamma \approx \frac{2}{3} \text{ for } > 0.35\mu\text{m}; \approx 1 \text{ for } 0.18\mu\text{m}; \approx \frac{4}{3} \text{ for } 0.13\mu\text{m}$$

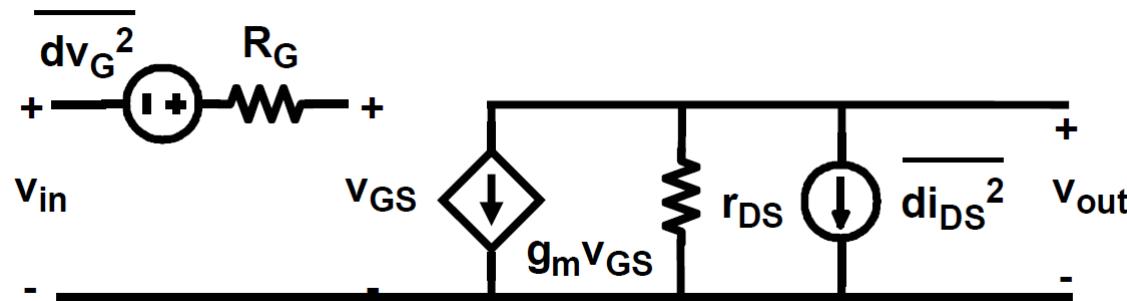
》》 晶体管的噪声

- 晶体管的**输入电阻**和其他电阻一样，也会产生热噪声
- 无噪声小信号模型：



》》 晶体管的噪声

- 含噪声小信号模型：

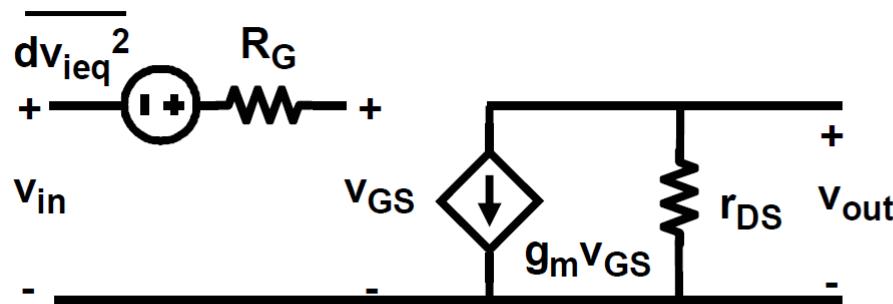


$$\overline{dv_G^2} = 4kT R_G df$$

$$\overline{di_{DS}^2} = \frac{4kT}{R_{CH}} df = 4kT \frac{2}{3} g_m df$$

》》 晶体管的噪声

- 输入等效噪声小信号模型：

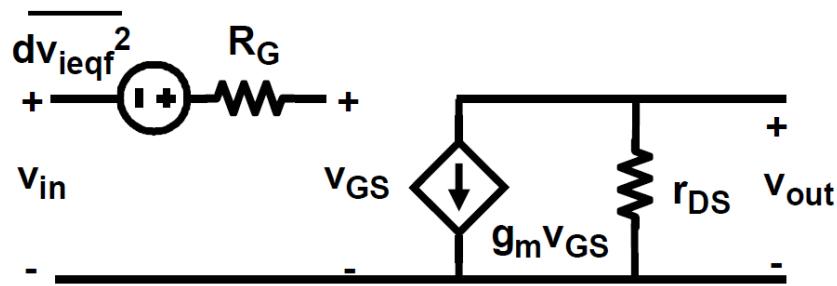


$$\overline{dv_{ieq}^2} = 4kT (R_{eff}) df \quad R_{eff} = \frac{2/3}{g_m} + R_G$$

- 高频时，**电流**可以通过 C_{GS} ，因此也需考虑，同时需注意与输入噪声电压**相关**

》》 晶体管的噪声

- 输入等效噪声小信号模型：**1/f 噪声**



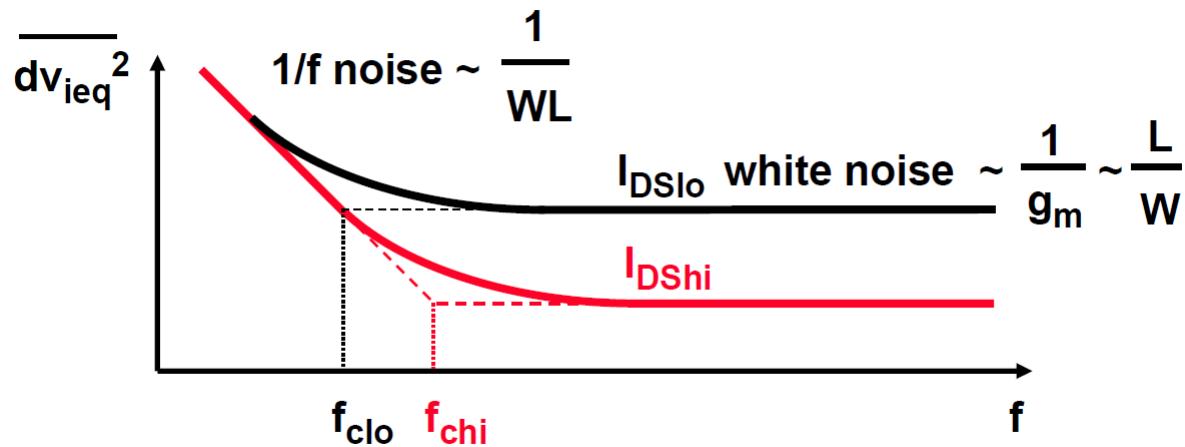
$$\overline{dv_{ieqf}^2} = \frac{KF_F}{WL C_{ox}^2} \frac{df}{f}$$

pMOS $KF_F \approx 10^{-32} \text{ C}^2/\text{cm}^2$
nMOS $KF_F \approx 4 \cdot 10^{-31} \text{ C}^2/\text{cm}^2$

$W \text{ & } L \text{ in cm; } C_{ox} \text{ in F/cm}^2$

- NMOS的闪烁噪声是PMOS的**40倍**！

》》 晶体管的噪声：转角频率



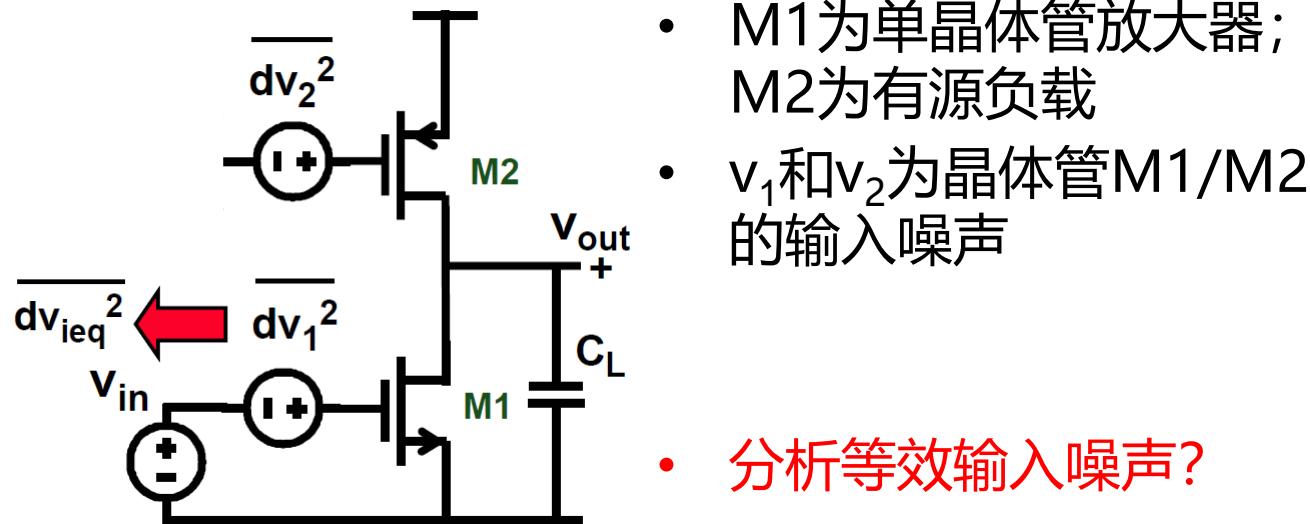
- 偏置电流越大，白噪声越低，拐角频率越大



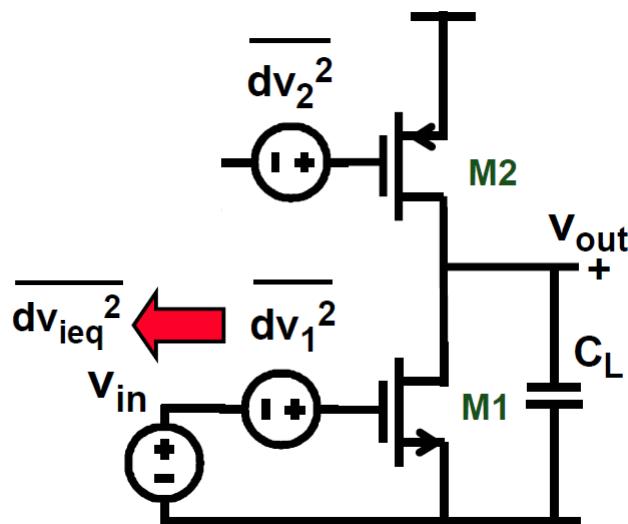
噪声 Noise

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- 电阻的热噪声
- 晶体管的噪声源
- **等效噪声的换算**

》》 放大器的噪声



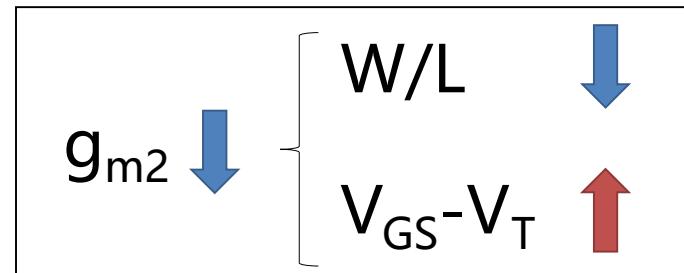
》》 放大器的噪声



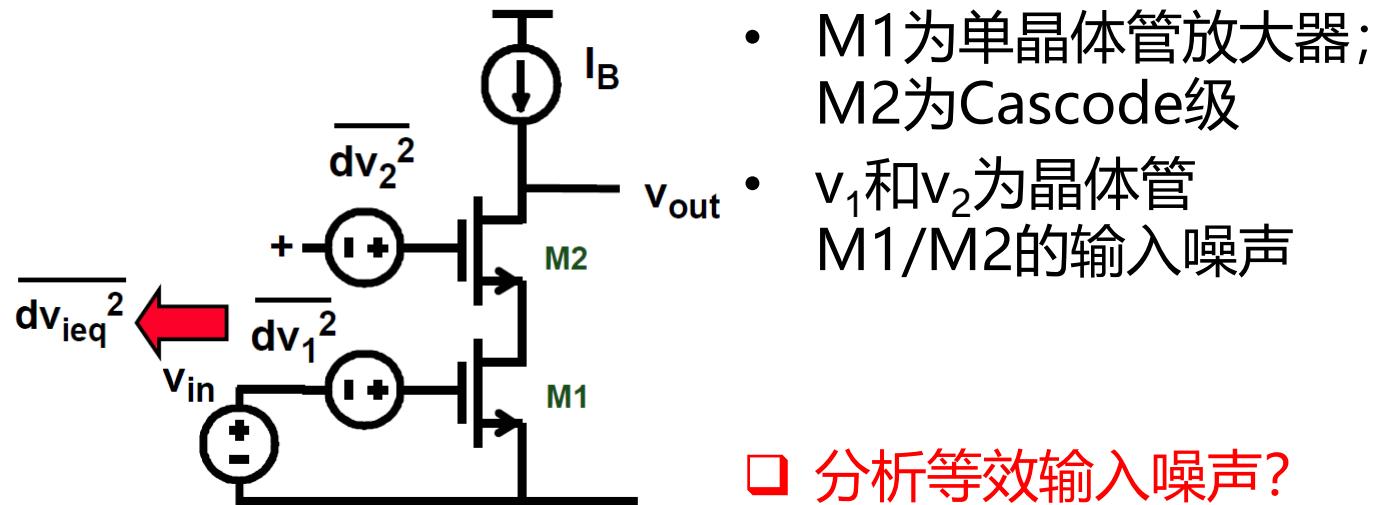
- M1为单晶体管放大器；
M2为有源负载
- v_1 和 v_2 为晶体管M1/M2
的输入噪声
- 分析等效输入噪声？

$$\overline{di_{out}^2} = g_{m1}^2 \overline{dv_1^2} + g_{m2}^2 \overline{dv_2^2}$$

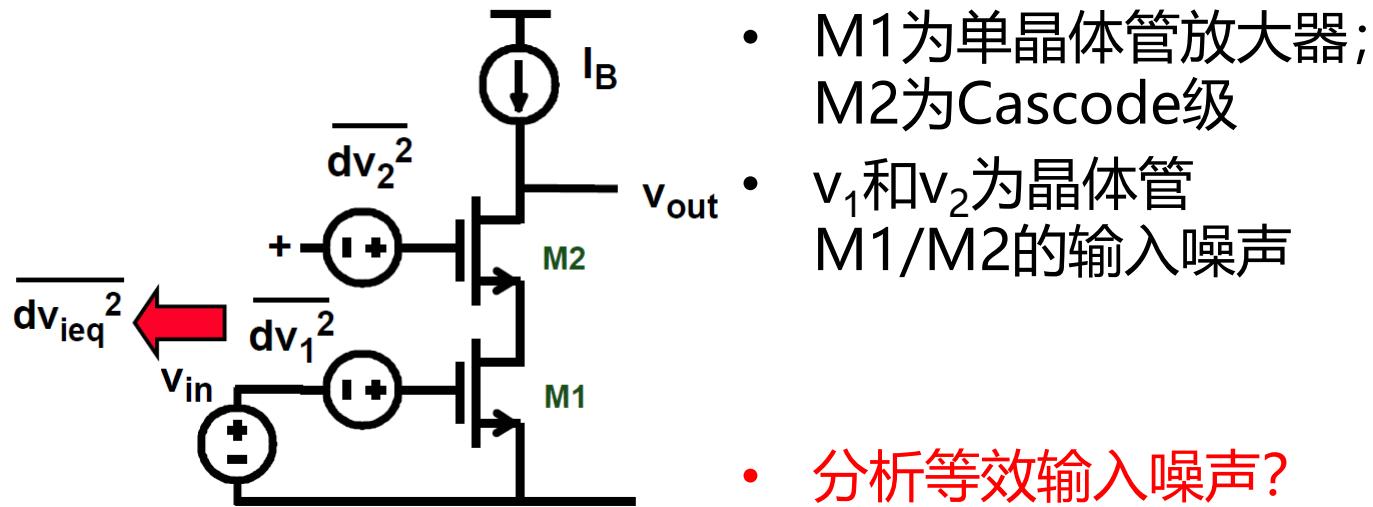
$$\overline{dv_{ieq}^2} = \overline{dv_1^2} \left(1 + \frac{g_{m2}}{g_{m1}} \right)$$



»» Cascode的噪声



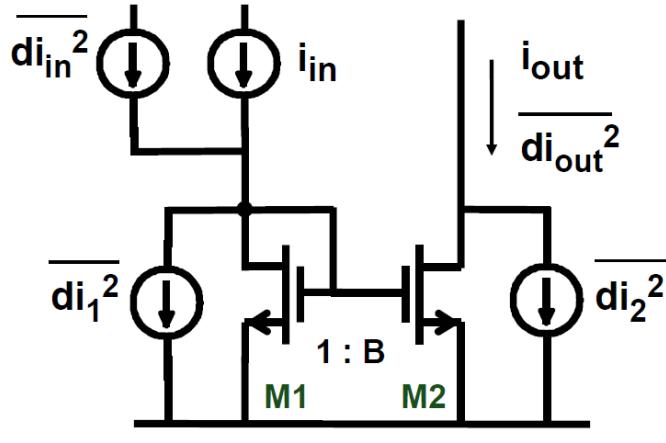
»» Cascode的噪声



$$\overline{dv_{ieq}^2} = \overline{dv_1^2} + \overline{dv_2^2} \quad \frac{1}{(g_{m1} r_{o1})^2} \approx \overline{dv_1^2}$$

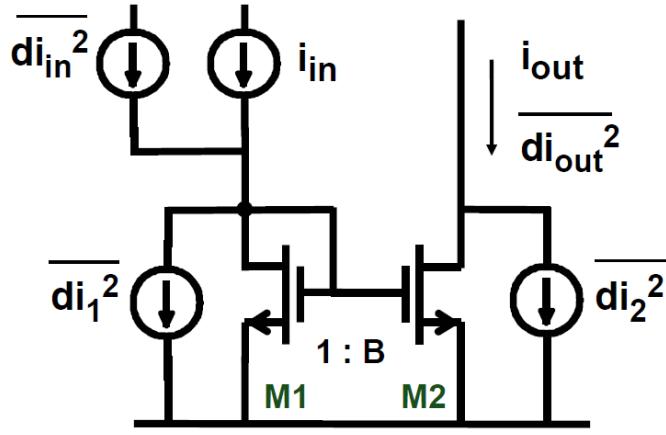
Cascode 晶体
管M2的噪声忽
略不计

》》 电流镜的噪声



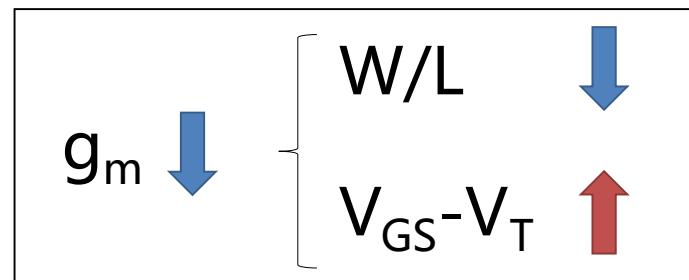
- M1/M2 为放大比例为B的电流镜
- i_1 和 i_2 为晶体管M1/M2的沟道噪声电流
- i_{in} 为输入噪声电流

》》 电流镜的噪声

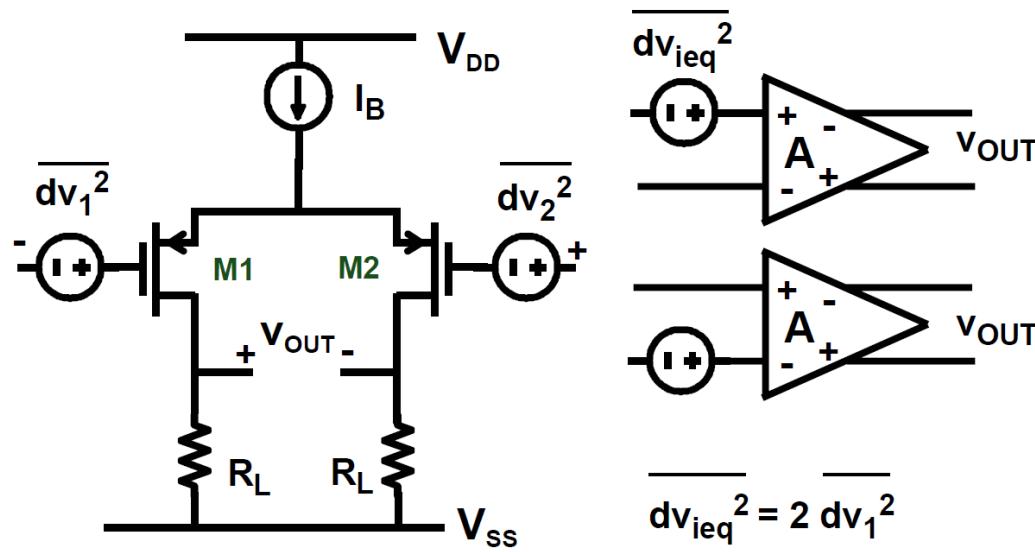


- M1/M2 为放大比例为B的电流镜
- i_1 和 i_2 为晶体管M1/M2的沟道噪声电流
- i_{in} 为输入噪声电流

$$\overline{di_{out}^2} = \overline{di_2^2} + B^2 (\overline{di_{in}^2} + \overline{di_1^2})$$

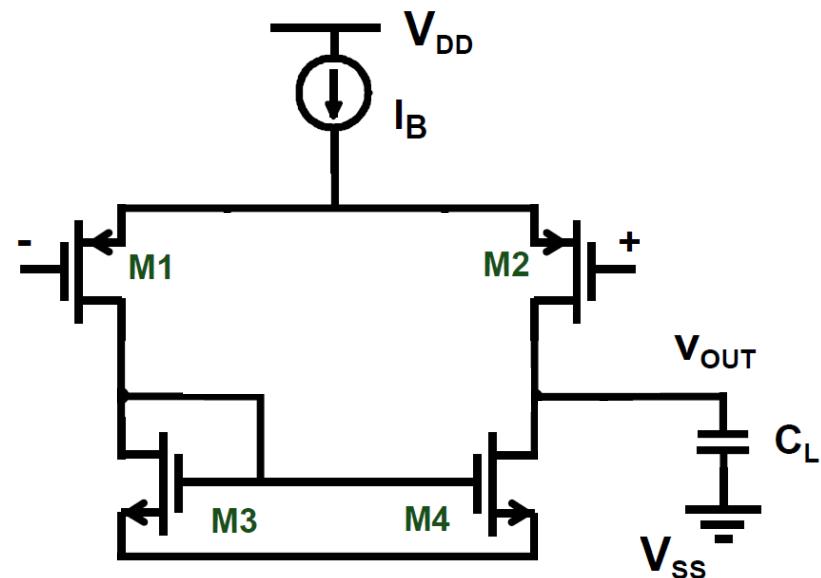


》》差分对的噪声

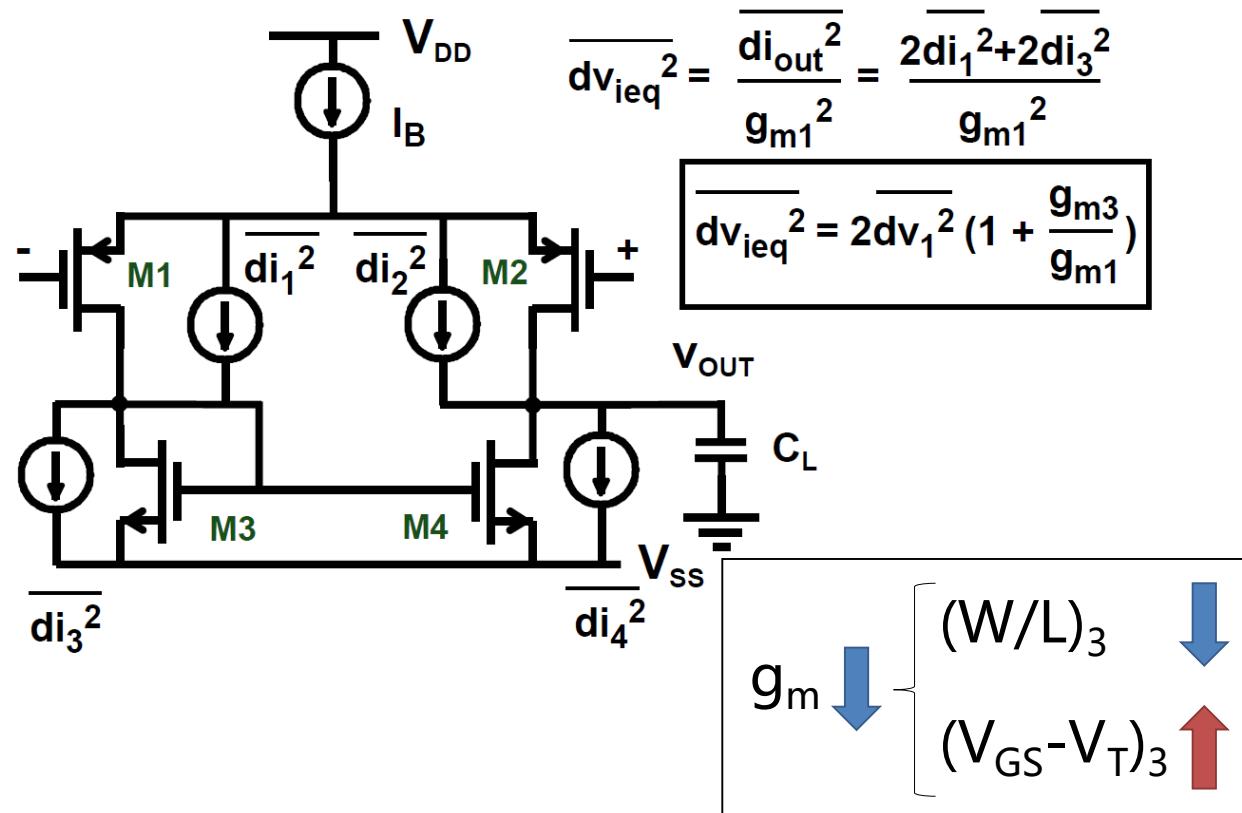


差分对的噪声即为两个输入晶体管噪声的和

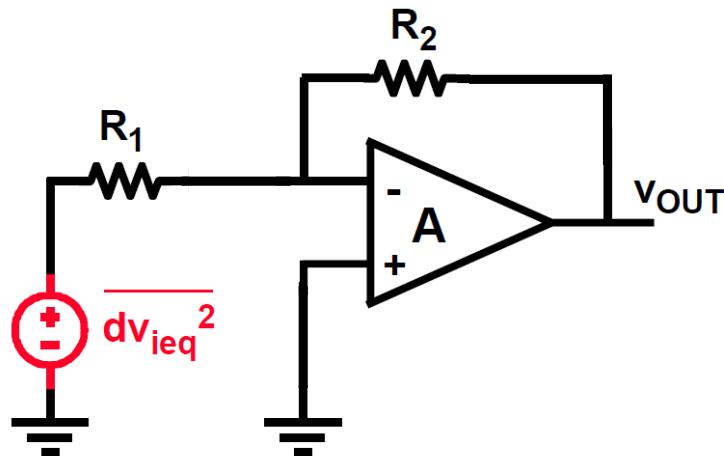
》》 典型运放的噪声



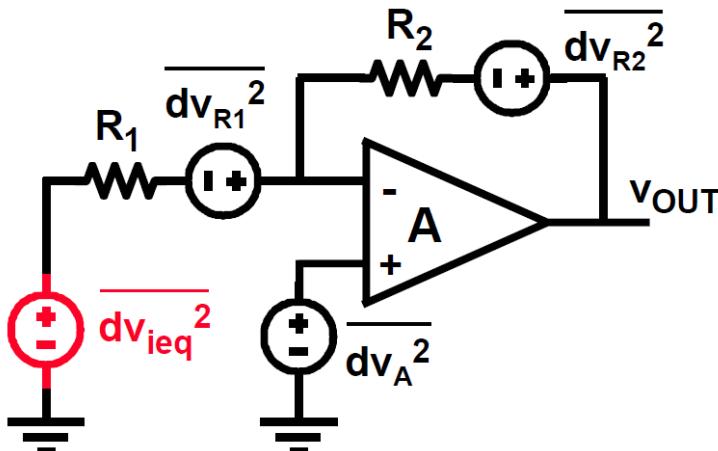
典型运放的噪声



》》 典型运放的噪声



典型运放的噪声



$$\overline{dv_{ieq}^2} = \sum \overline{dv_{out}^2} \left(\frac{R_1}{R_2} \right)^2$$

$$\overline{dv_{out}^2} = \overline{dv_{R1}^2} \left(\frac{R_2}{R_1} \right)^2$$

$$\overline{dv_{out}^2} = \overline{dv_{R2}^2}$$

$$\overline{dv_{out}^2} = \overline{dv_A^2} \left(1 + \frac{R_2}{R_1} \right)^2$$

$$\overline{dv_{ieq}^2} = \overline{dv_{R1}^2} + \overline{dv_{R2}^2} \left(\frac{R_1}{R_2} \right)^2 + \overline{dv_A^2} \left(1 + \frac{R_1}{R_2} \right)^2 \approx \overline{dv_{R1}^2} + \overline{dv_A^2}$$

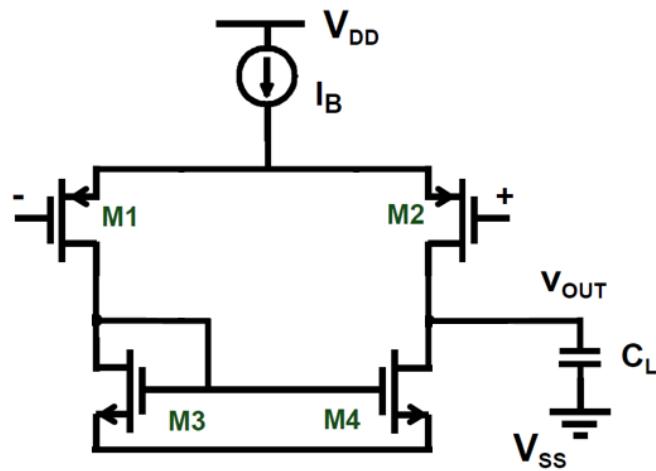


设计思路总结

1. 噪声通过功率表述
2. 注意噪声源之间的相关性
3. 对于系统噪声性能的分析需要转换成输入参考噪声
4. 输入参考的转换参考电路的跨导计算等

》》作业

1. 自由确定晶体管的尺寸，通过仿真寻找NMOS和PMOS的 $1/f$ 噪声系数KF，以及热噪声系数 γ
2. 对一偏置电流为100uA的五管OTA，通过晶体管的设计，使其等效输入噪声的80%来源于差分对M1和M2。



第4章 失配



北京航空航天大學
BEIHANG UNIVERSITY

| 微电子学院

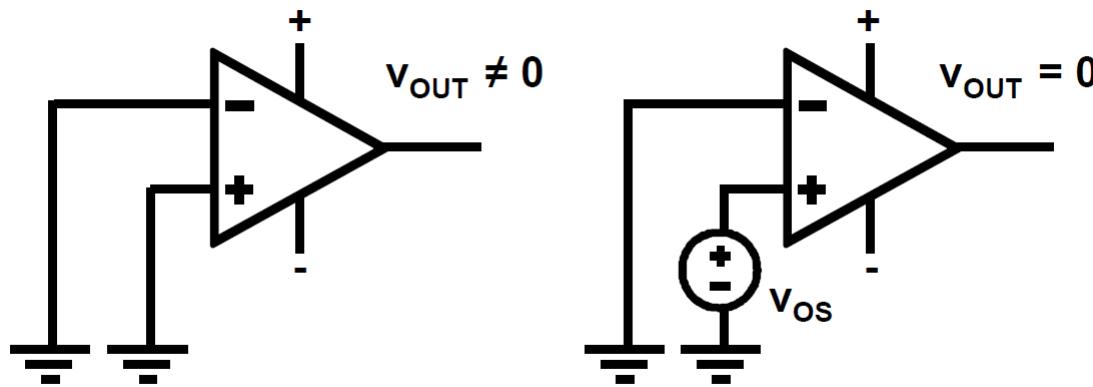
CMOS模拟集成电路设计

第四章：失调与CMRR

胡远奇

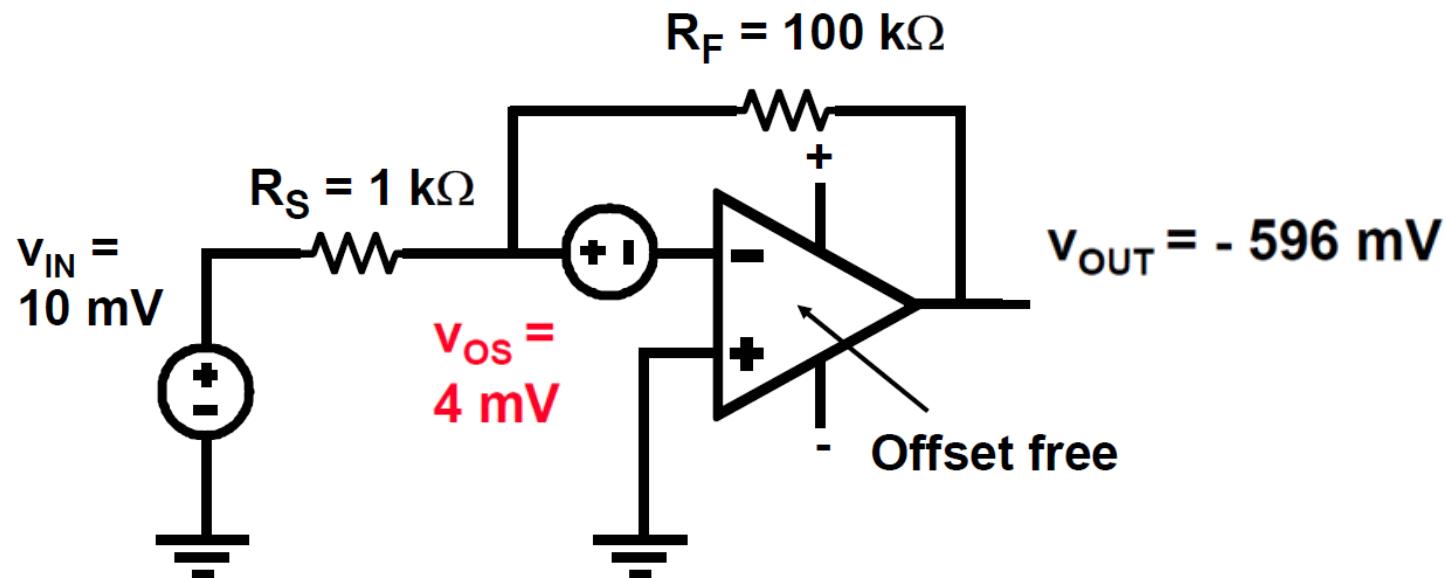
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》》失调(Offset)的定义

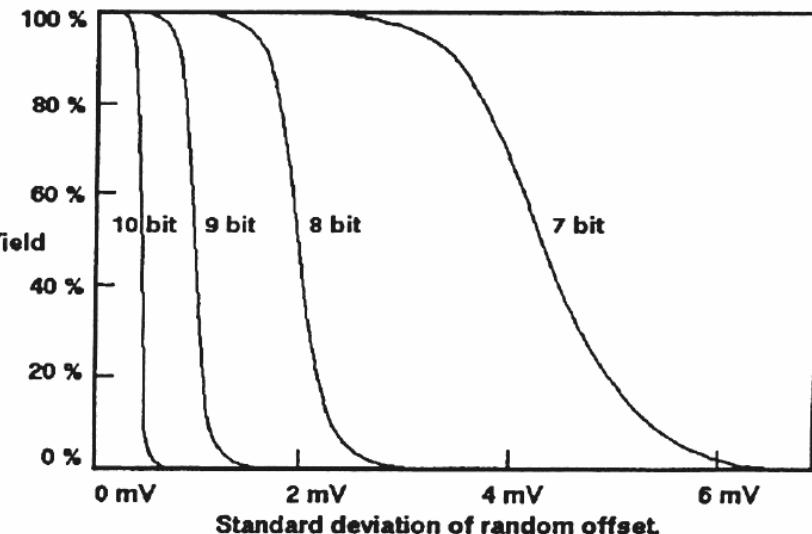
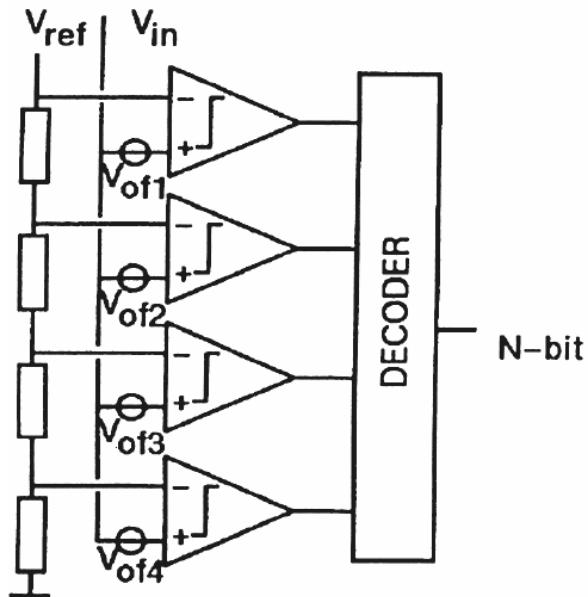


- 失调电压 V_{OS} : 使输出电压为零时的两端输入电压之差
 - 可以加在任意一端

》》失调(Offset)的影响



》》失调(Offset)的影响



n-bit Flash-ADC with offset

Ref: Pelgrom, IEDM 1998, pp.789.

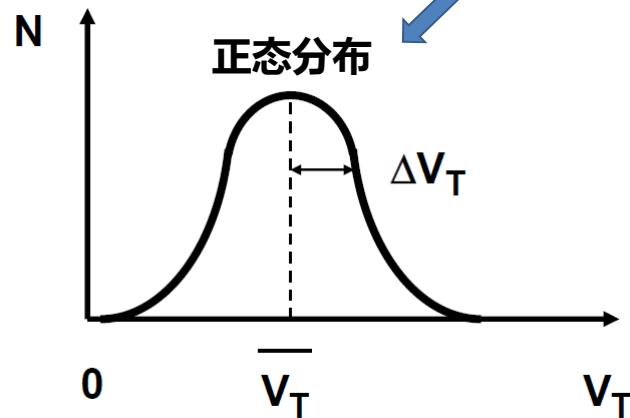


失调与CMRR

- 随机性失调和 $CMRR_R$
- 系统性失调和 $CMRR_S$
- 设计守则

» 随机失调：阈值电压的失配

$$I_{DS} = K' W/L (V_{GS} - V_T)^2$$



$$\sigma_{\Delta V_T} = \frac{A_{VT}}{\sqrt{WL}}$$

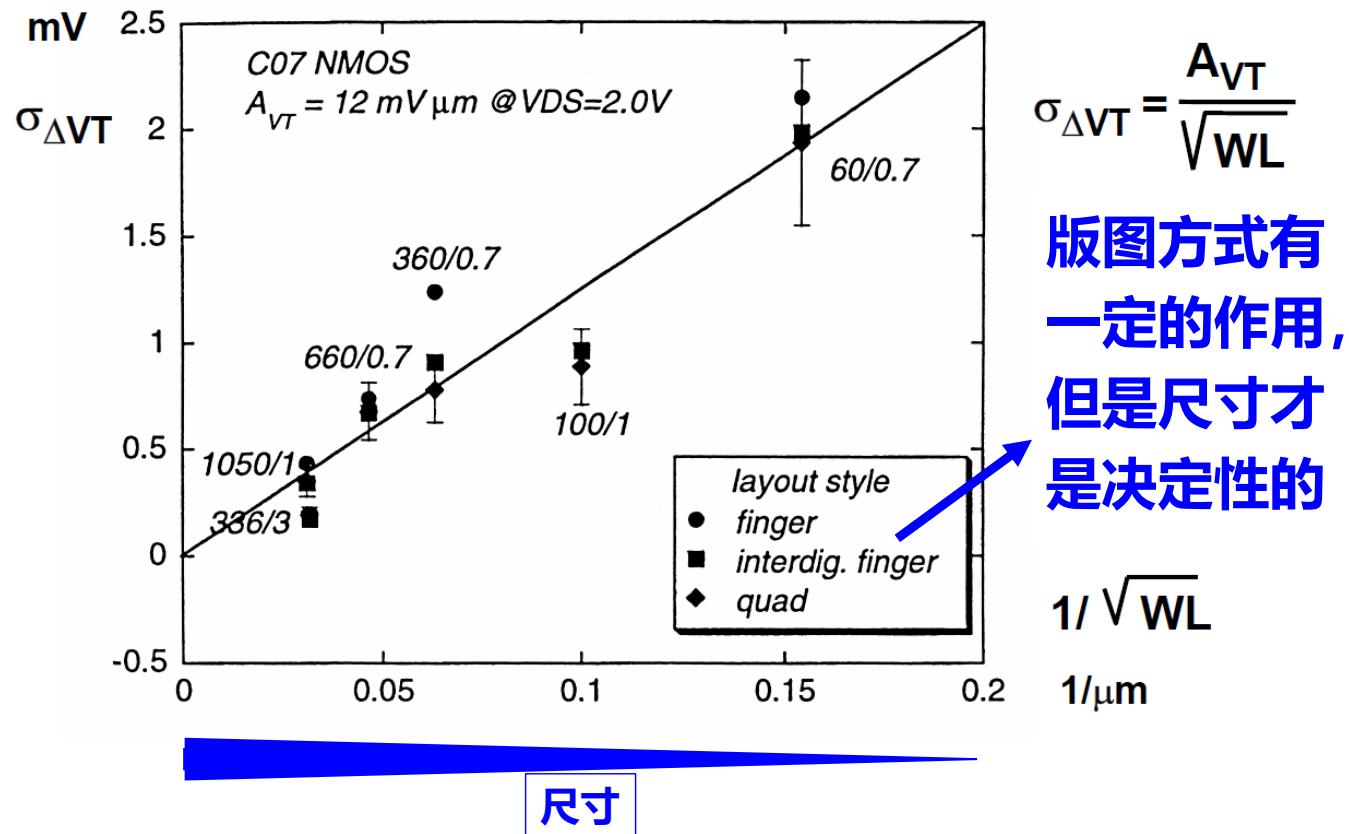
$$A_{VT} \sim t_{ox} \sqrt[4]{N_B}$$

氧化层厚度 & 衬底参杂浓度

$A_{VT} \approx 5 \text{ mV um}$
for 0.25 um nMOST
+50 % for pMOST

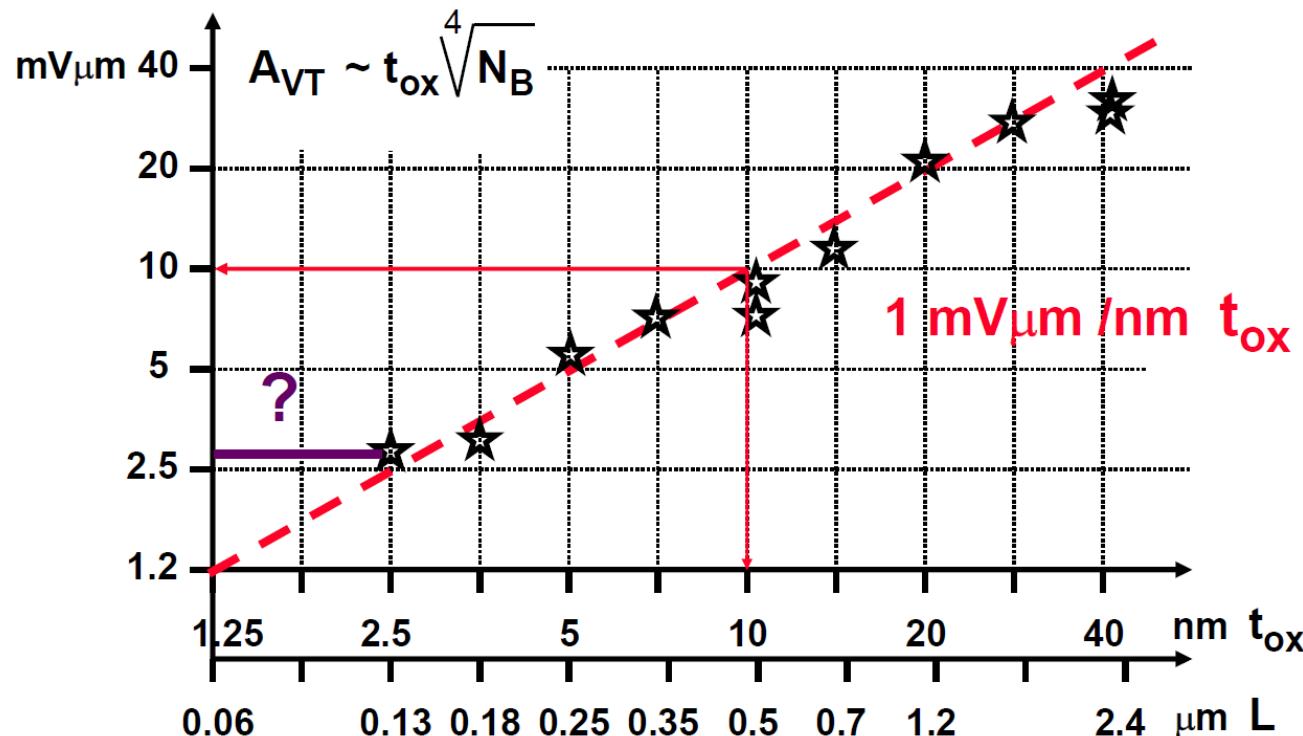
□估算0.25um工艺下、尺寸为16um/1um的PMOS差分对由阈值电压失配造成的大失调电压？（要求99.5%良率）

》》 阈值电压失配的标准差





阈值电压失配的系数 A_{VT}



- 某工厂 55nm 工艺的 $A_{VT} = 2.05e-9$

» 随机失调：工艺与尺寸的失配

$$I_{DS} = K' W/L (V_{GS} - V_T)^2$$

$$\frac{\Delta K'}{K'} = \frac{A_{K'}}{\sqrt{WL}}$$

$A_{K'} \approx 0.0056 \text{ um}$
+50 % for pMOS

$$\frac{\Delta W/L}{W/L} = A_{WL} \sqrt{\frac{1}{W^2} + \frac{1}{L^2}}$$

$A_{WL} \approx 0.02 \text{ mV um}$
+50 % for pMOS

- 参数 K' 造成的变化相对较小

- A_{WL} 与工艺的相关性不强

» NMOS的失配参数

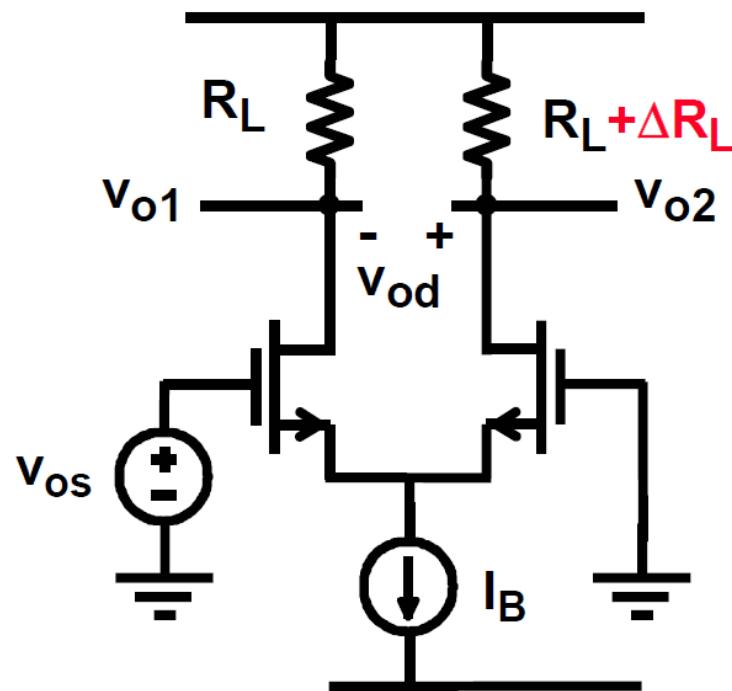
Techno L (μm)	2.5	1.2	0.7	0.5	0.35	0.25
t _{ox} (nm)	50	25	15	11	8	6
A _{VT} (mV μm)	30	21	13	7.1	6	⇒ 3
A _{WL} (% μm)	2.5	1.8	2.5	1.3	2	⇒ 1.8

A_{WL}的单位是um，可以听过设计尺寸或偏置电压减小其影响

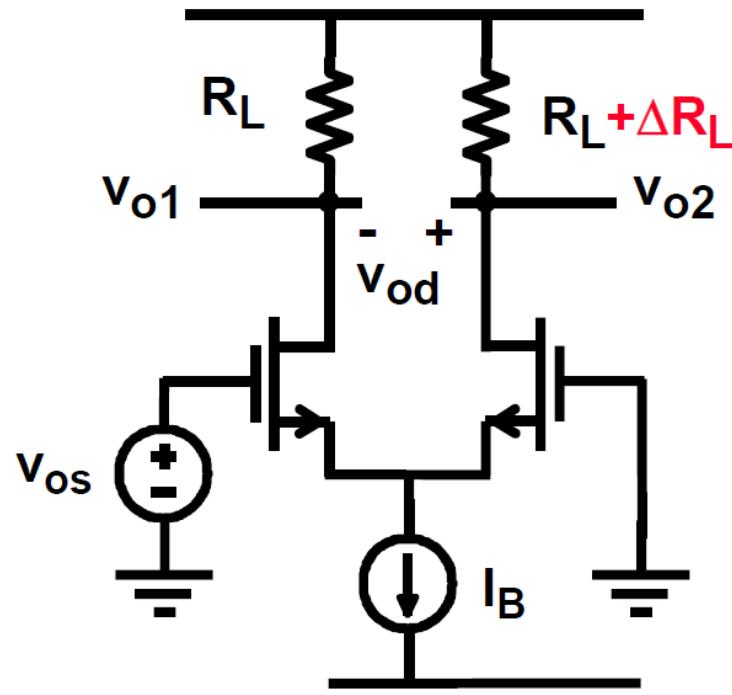
A_{VT}的单位是mV*um，只能通过设计尺寸减小其影响



差分对中的随机失调



》》》 差分对中的随机失调



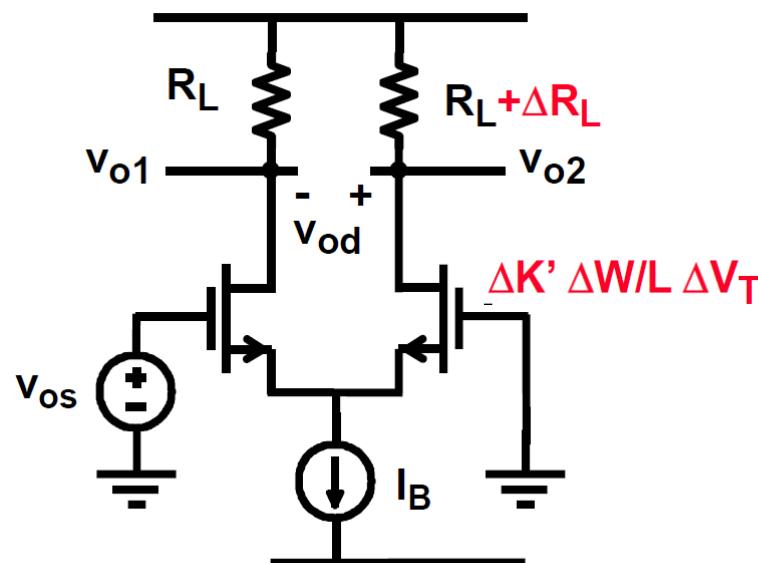
$$v_{od} = \frac{\Delta R_L}{R_L} \frac{I_B}{2}$$

$$v_{os} = \frac{v_{od}}{g_m R_L}$$

$$v_{os} = \frac{\Delta R_L}{R_L} \frac{I_B}{2g_m} \quad \cdot \text{ 需要减小 } V_{GS} - V_T$$

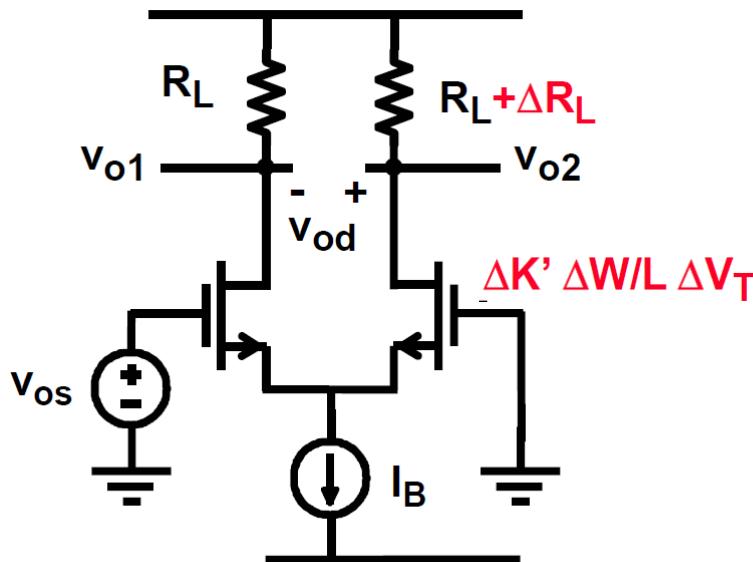
$$v_{os} = \frac{\Delta R_L}{R_L} \frac{V_{GS} - V_T}{2}$$

》》差分对中的随机失调



$$I_{DS} = K' W/L (V_{GS} - V_T)^2$$

》》》 差分对中的随机失调



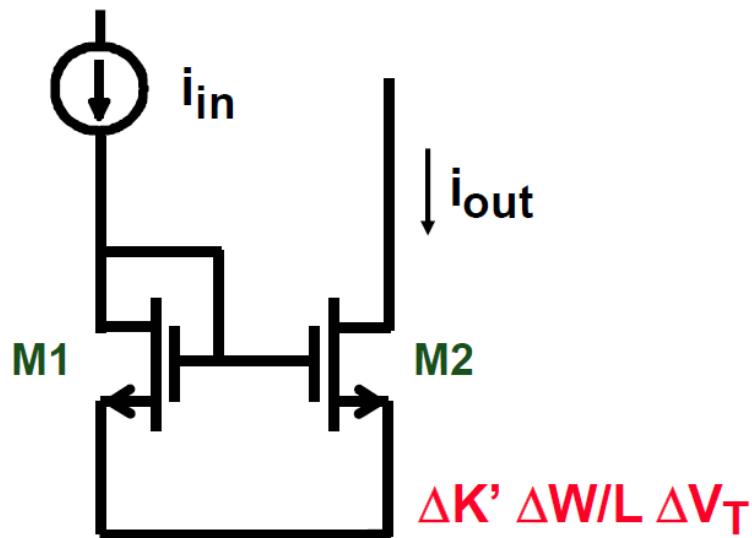
$$I_{DS} = K' W/L (V_{GS} - V_T)^2$$

差分对应尽可能的

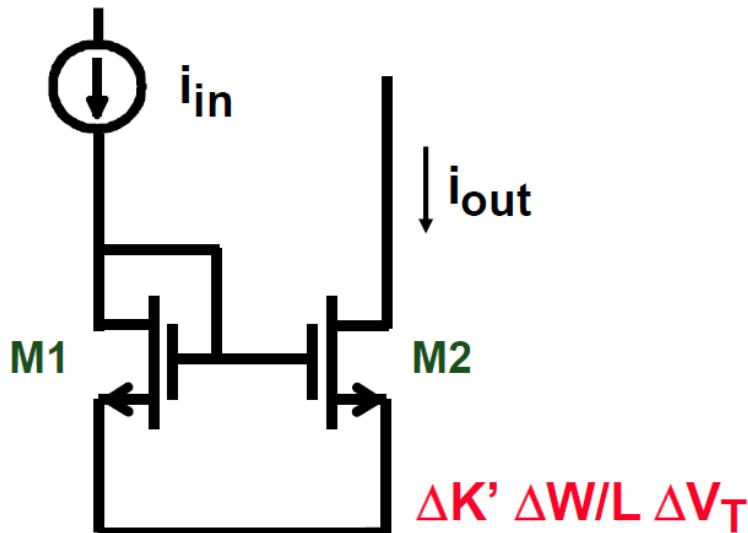
$$V_{GS} - V_T \downarrow$$

$$v_{OS} = \Delta V_T + \frac{V_{GS} - V_T}{2} \left(\frac{\Delta R_L}{R_L} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L} \right)$$

»» 电流镜中的随机失调



》》电流镜中的随机失调



$$\frac{\Delta I_{out}}{I_{out}} =$$

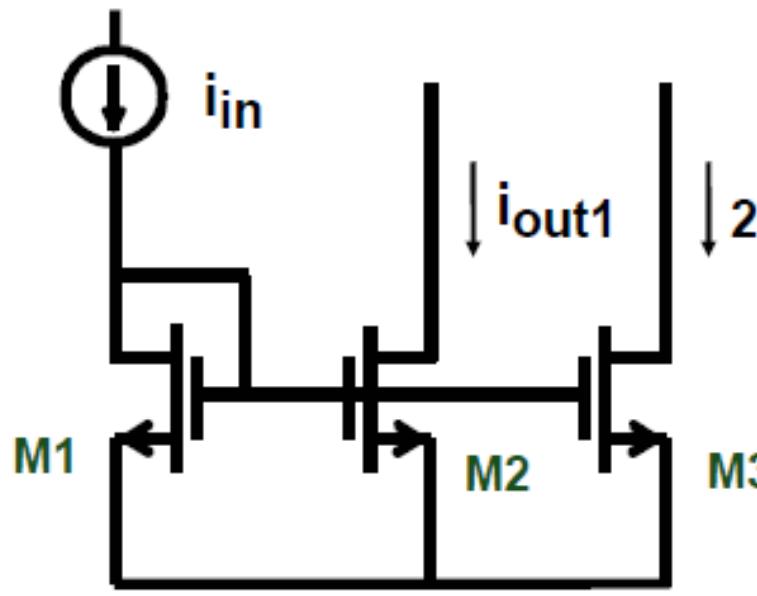
- A_{WL} 是主要失配源

$$\frac{\Delta V_T}{(V_{GS} - V_T)/2} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L}$$

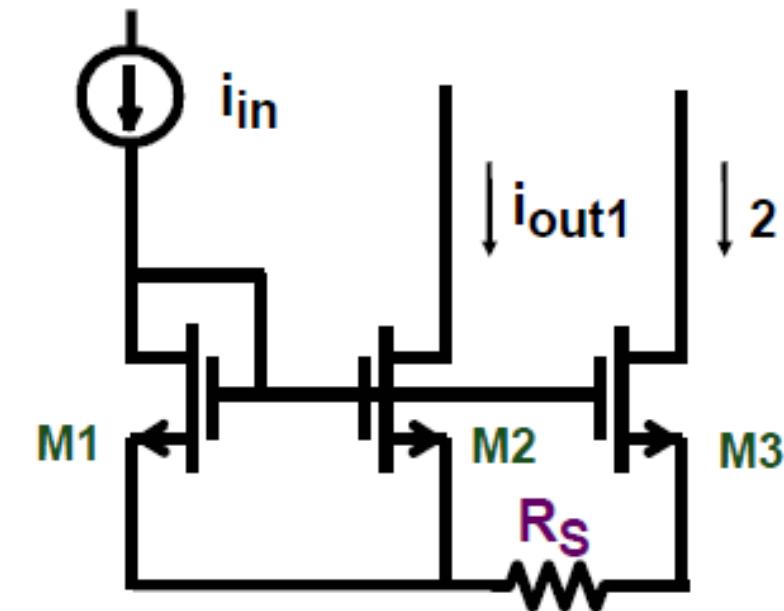
电流镜应尽可能的

$$V_{GS} - V_T \uparrow$$

» 电流镜中的其他失调因素



$\Delta K' \Delta W/L \Delta V_T$



$\Delta K' \Delta W/L \Delta V_T R_S$

》》 输出电流的失配

$$I_{DS} = K' W/L (V_{GS} - V_T)^2$$

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_T)^2$$



定义：总的电流失配由 β 失配和 V_T 失配造成

$$\frac{\Delta I_{DS}}{I_{DS}} =$$

$$\sigma^2 \left(\frac{\Delta I_{DS}}{I_{DS}} \right) =$$

》》 输出电流的失配

$$I_{DS} = K' W/L (V_{GS} - V_T)^2$$

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_T)^2$$



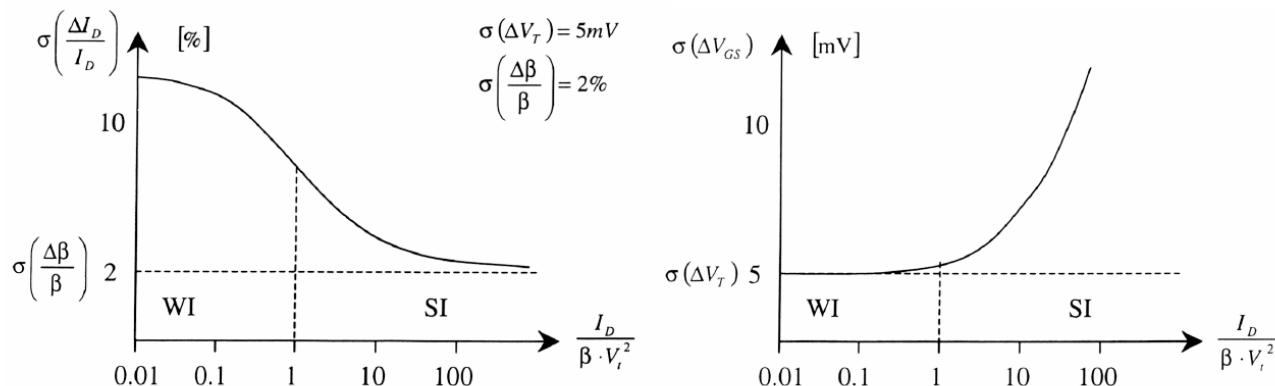
定义：总的电流失配由 β 失配和 V_T 失配造成

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta \beta}{\beta} - \Delta V_T \frac{2}{V_{GS} - V_T}$$

$$\sigma^2 \left(\frac{\Delta I_{DS}}{I_{DS}} \right) = \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) + \sigma^2 (\Delta V_T) \frac{4}{(V_{GS} - V_T)^2}$$

输出电流的失配

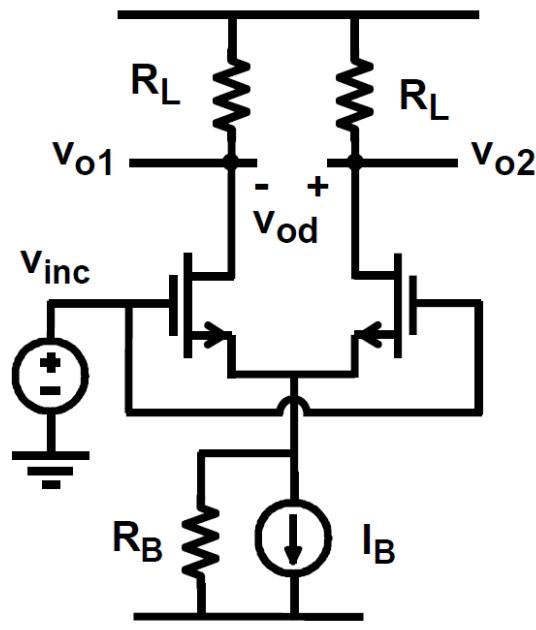
$$\sigma^2 \left(\frac{\Delta I_{DS}}{I_{DS}} \right) = \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) + \sigma^2 (\Delta V_T) \underbrace{\frac{4}{(V_{GS} - V_T)^2}}_{\text{in si}} \quad \text{or} \quad \underbrace{\frac{1}{(nkT/q)^2}}_{\text{in wi}}$$



- 弱反型区中, V_T 失配占主要因素; 强反型区中, β 失配占主要因素, 其中主要又是W/L的失配为主

» 共模抑制比

- 差分对的另一随机指标：共模抑制比（Common Mode Rejection Ration）



共模增益：

差模输出 V_{od} / 共模输入 V_{inc}

$$A_{dc} = \left. \frac{V_{od}}{V_{ic}} \right|_{V_{id} = 0} \approx 0$$

共模抑制比：

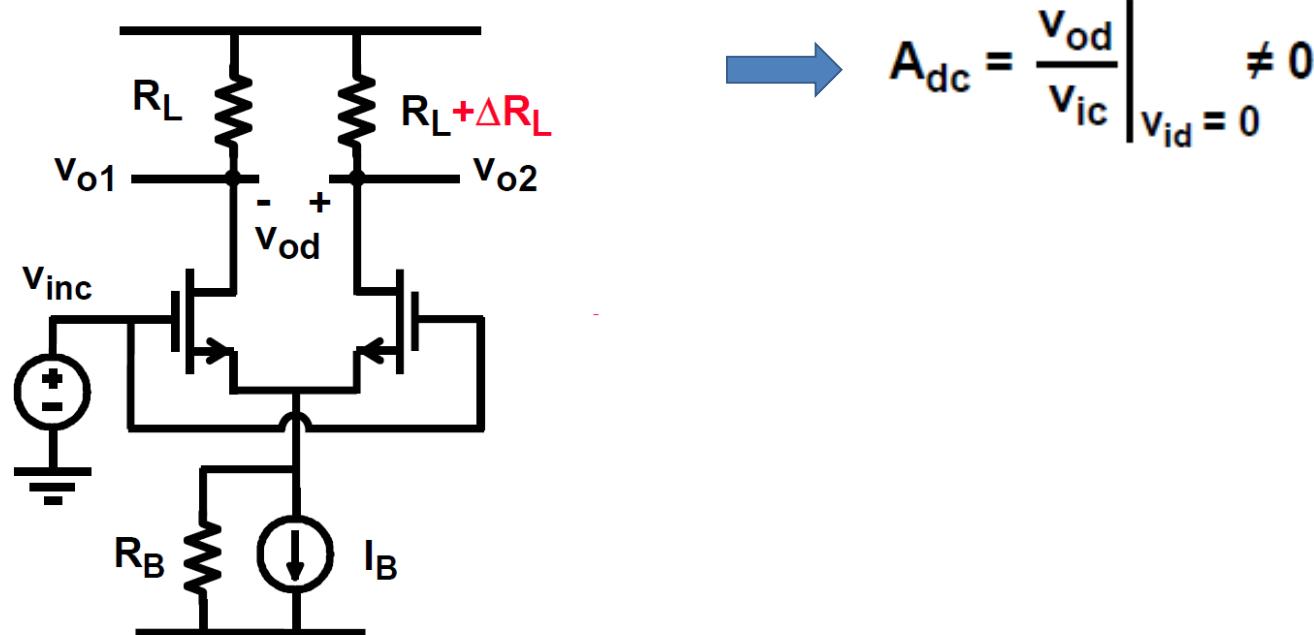
差模增益 / 共模增益

$$CMRR = \frac{A_{dd}}{A_{dc}} \approx \infty$$

》》共模抑制比

- 差分对的另一随机指标：共模抑制比（Common Mode Rejection Ration）

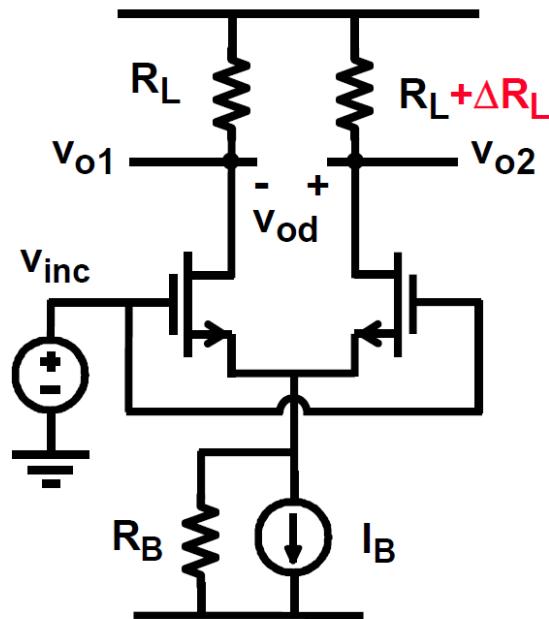
• 负载不对称



》》共模抑制比

- 差分对的另一随机指标：共模抑制比（Common Mode Rejection Ration）

• 负载不对称



$$\rightarrow A_{dc} = \left. \frac{v_{od}}{v_{ic}} \right|_{v_{id} = 0} \neq 0$$

共模偏置电流： $I_B = V_{INC}/R_B$

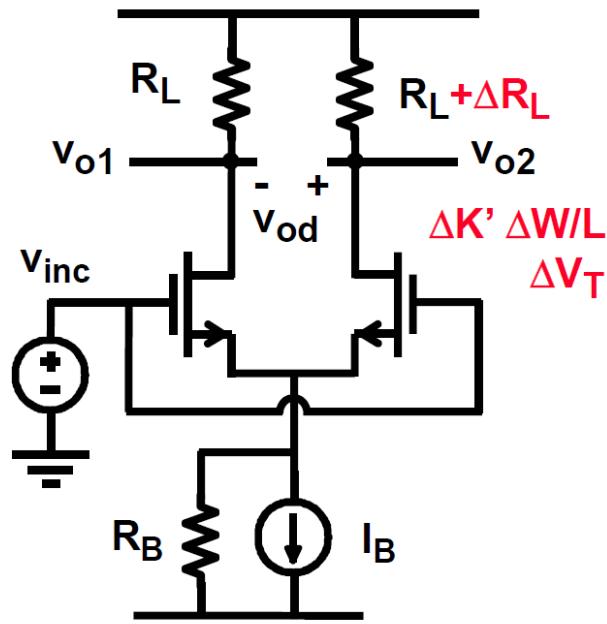
差模输出： $V_{od} = \Delta R_L \cdot I_B / 2$

$$A_{dc} = \frac{\Delta R_L}{2 R_B}$$

$$CMRR = \frac{2 g_m R_B}{\Delta R_L / R_L}$$

》》共模抑制比

- 差分对的另一随机指标：共模抑制比（Common Mode Rejection Ration）



- 负载不对称
- 差分对失调

$$CMRR = \frac{2g_m R_B}{\frac{\Delta R_L}{R_L}}$$



$$CMRR = \frac{2g_m R_B}{\frac{\Delta R_L}{R_L} + \frac{2V_{os}}{V_{GS} - V_T}}$$



随机失调与CMRR的关系

$$CMRR = \frac{2g_m R_B}{\frac{\Delta R_L}{R_L} + \frac{2V_{OS}}{V_{GS} - V_T}}$$

$$\rightarrow V_{OS} \cdot CMRR = V_{OS} \cdot \frac{2g_m R_B}{\frac{\Delta R_L}{R_L} + \frac{2V_{OS}}{V_{GS} - V_T}}$$

$$\rightarrow V_{OS} \cdot CMRR \approx (V_{GS} - V_T) g_m R_B$$

$$\rightarrow V_{OS} \cdot CMRR \approx V_E L_B$$

减小失调就是提高CMRR



随机失调与CMRR的关系

$$v_{OSr} \text{ CMRR}_r \approx V_E L_B \approx 10 \text{ V} \quad (\sim L_B)$$

10 mV 60 dB ≈ 10 V as for MOSTs

1 mV 80 dB ≈ 10 V as for Bipolar transistors

10 μ V 120 dB ≈ 10 V with trimming :
with laser
with Zener zap
with fusible links

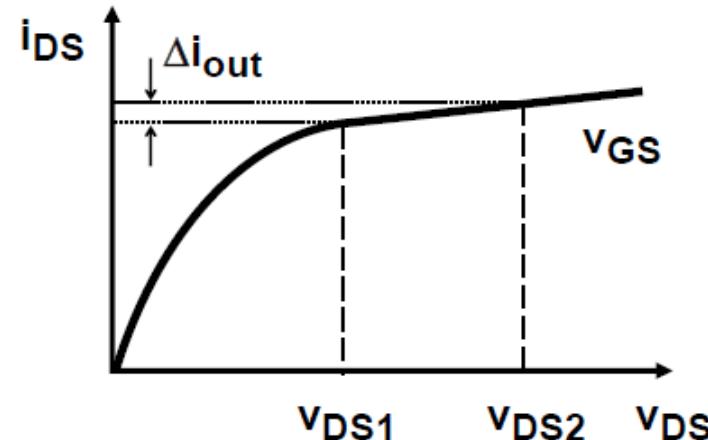
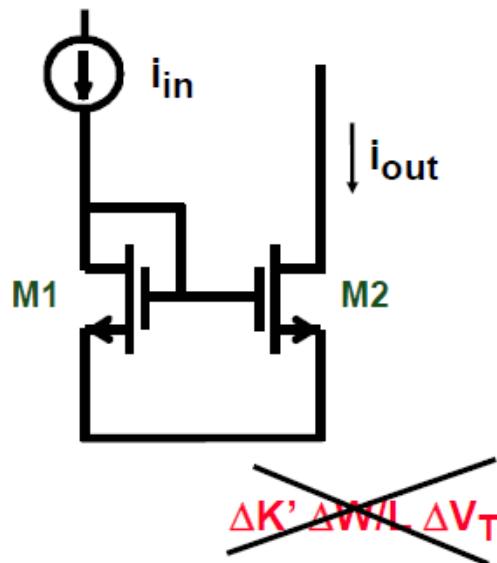
Low offset = High CMRR



失调与CMRR

- 随机性失调和 $CMRR_R$
- 系统性失调和 $CMRR_S$
- 设计守则

》》 电流镜中的系统失调

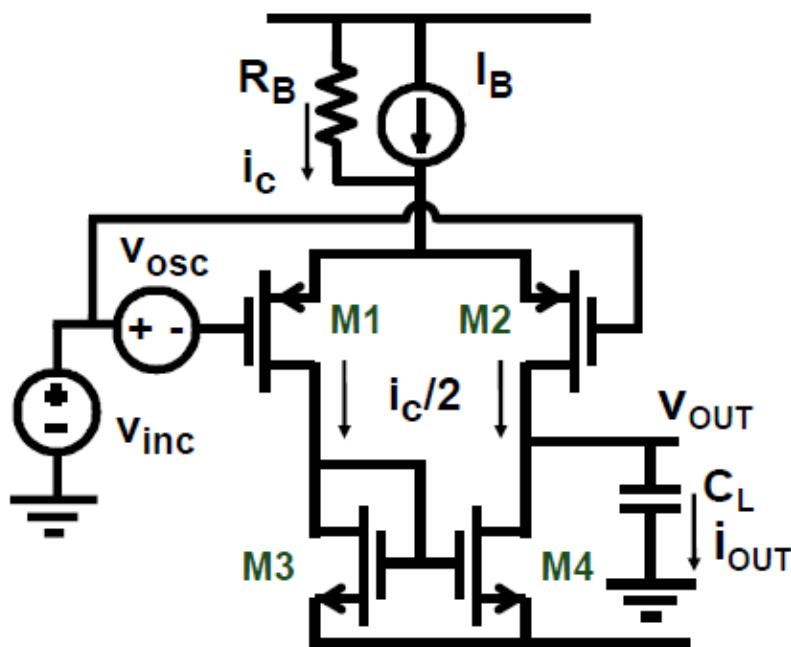


$$I_{out} \neq I_{in}$$

$$\frac{\Delta i_{out}}{i_{out}} = \frac{v_{DS2} - v_{DS1}}{V_E L_2}$$

》》》 差分运放中的系统性CMRR

- 不考虑任何随机性失调的情况下：



$$V_{OUT} = V_{GS3}$$

$$\Delta V_{GS3} = \frac{1}{2} \Delta I_B / g_{m3}$$

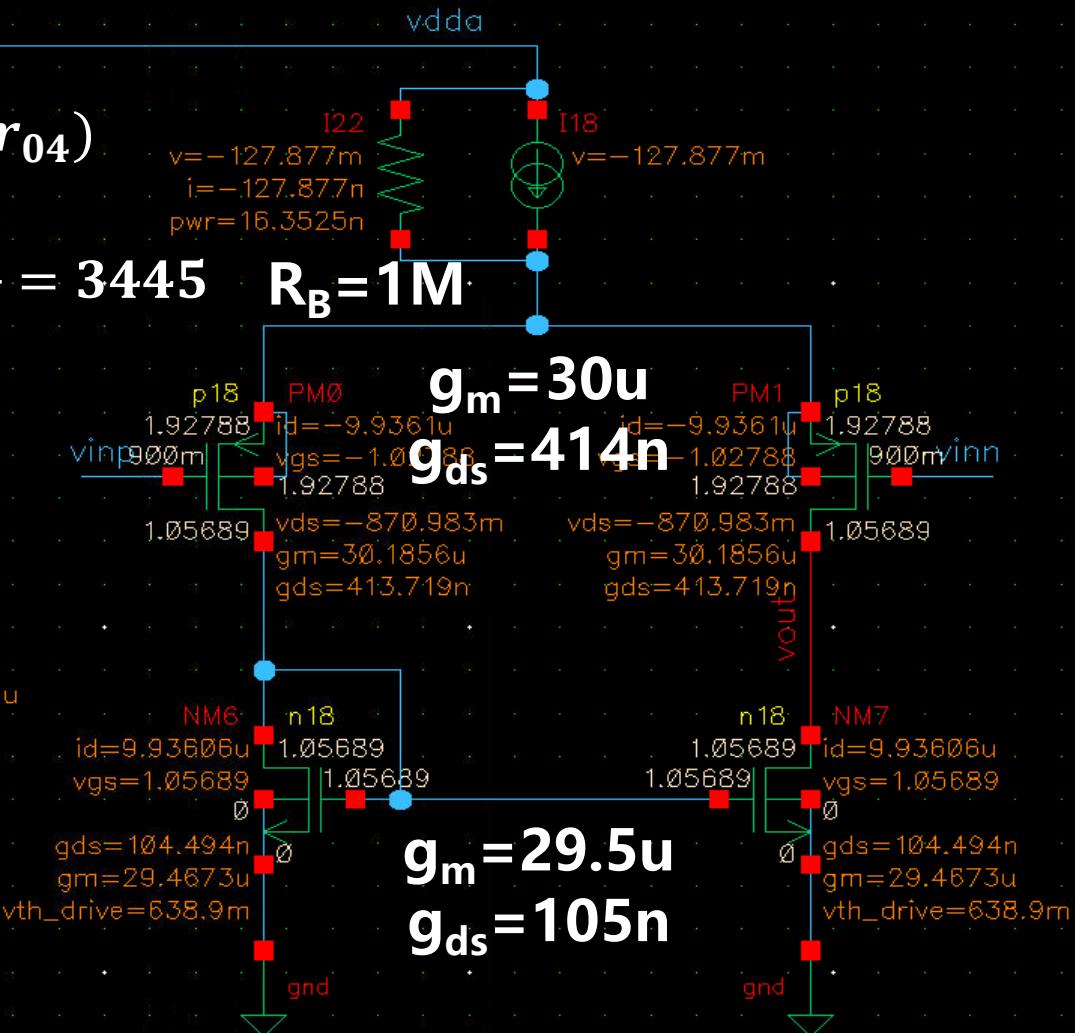
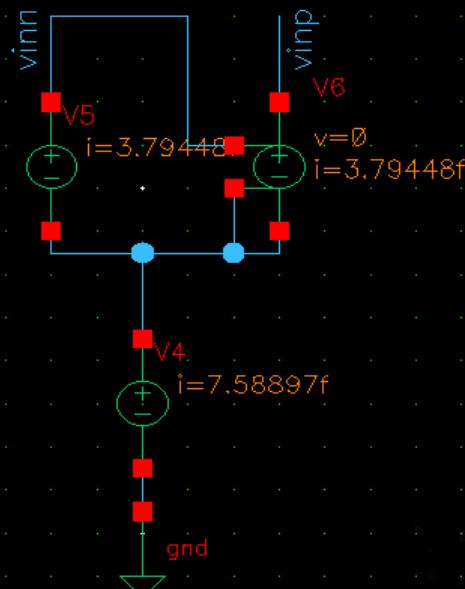
$$A_{dc} = \frac{1}{2g_{m3}R_B}$$

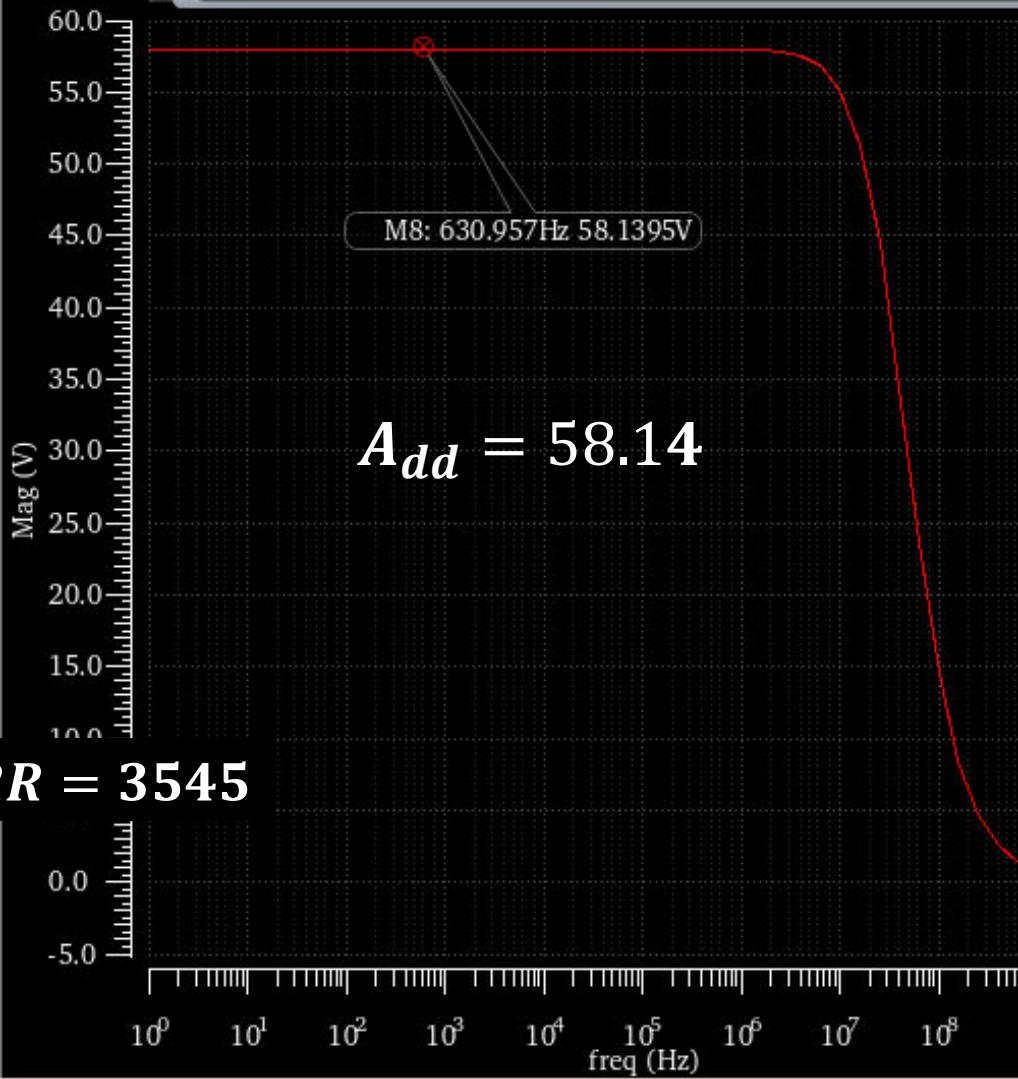
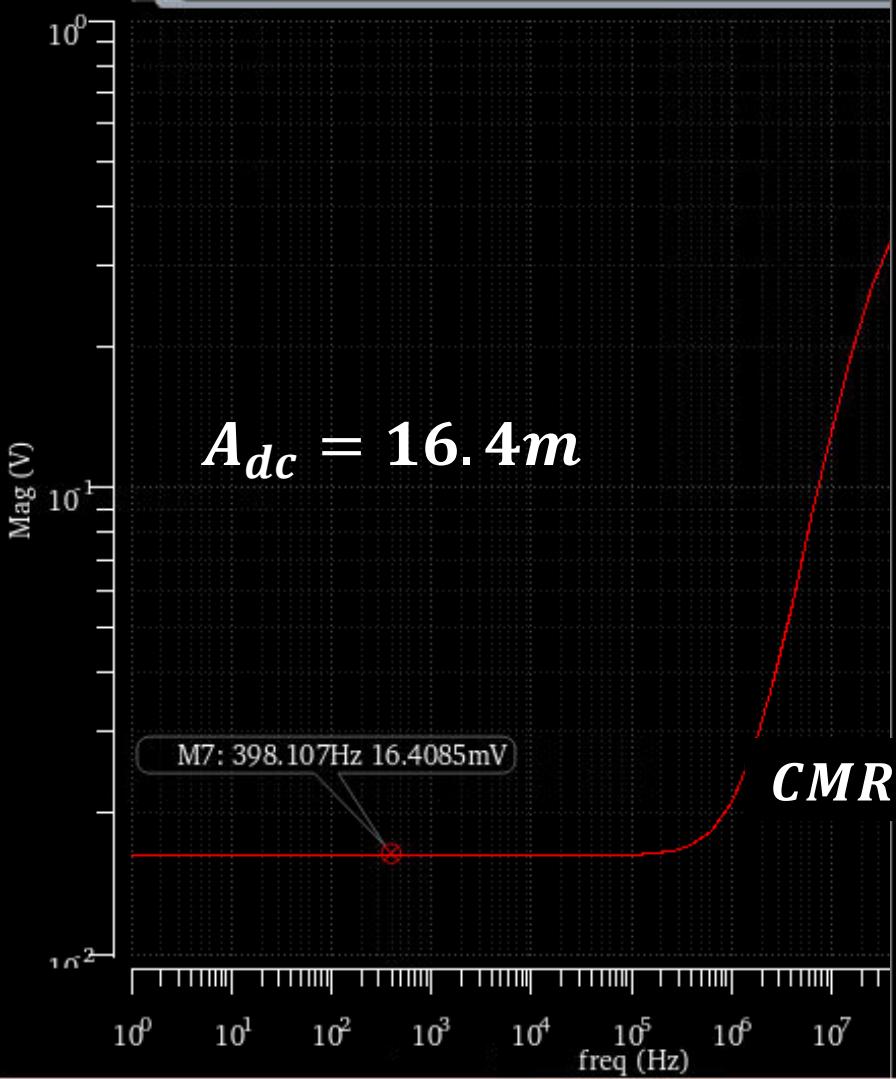
$$A_{dd} = g_{m1} \cdot (r_{02} || r_{04})$$

$$CMRR = 2g_{m1}g_{m3}R_B \cdot (r_{02} || r_{04})$$

$$CMRR = 2g_m1g_m3R_B \cdot (r_{02}||r_{04})$$

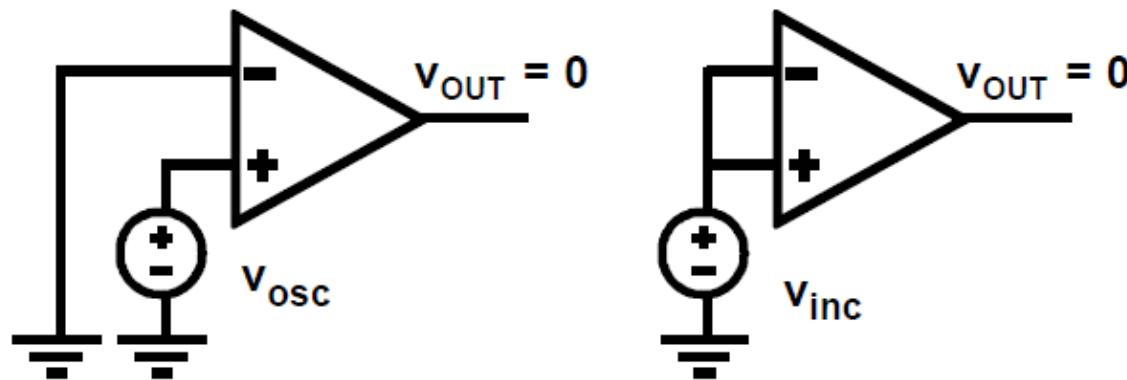
$$CMRR = \frac{2 \cdot 30\mu \cdot 29.8\mu \cdot 1M}{414n + 105n} = 3445 \quad R_B=1M$$



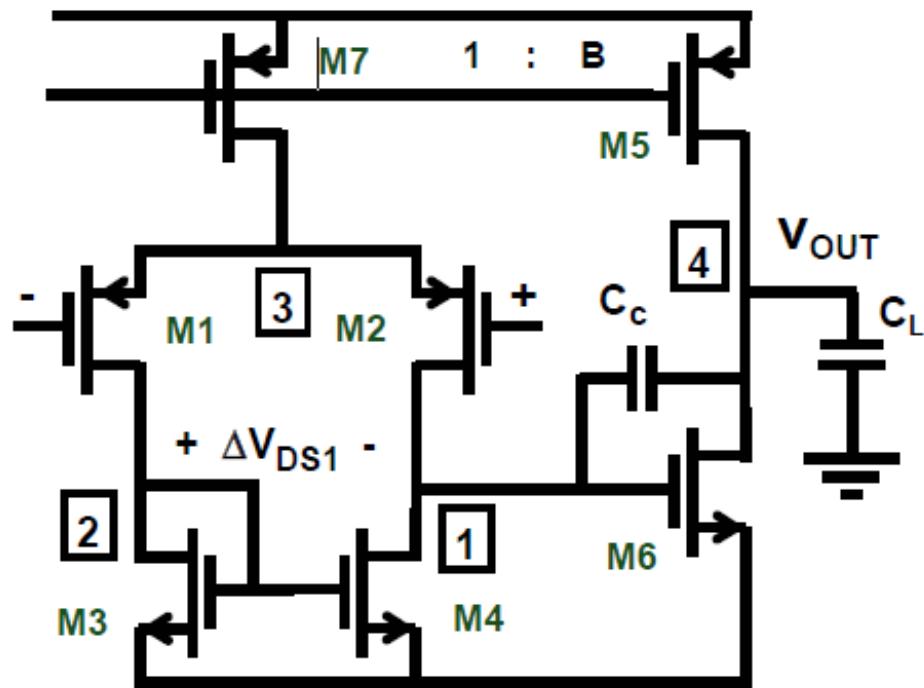


》》差分运放中的总CMRR

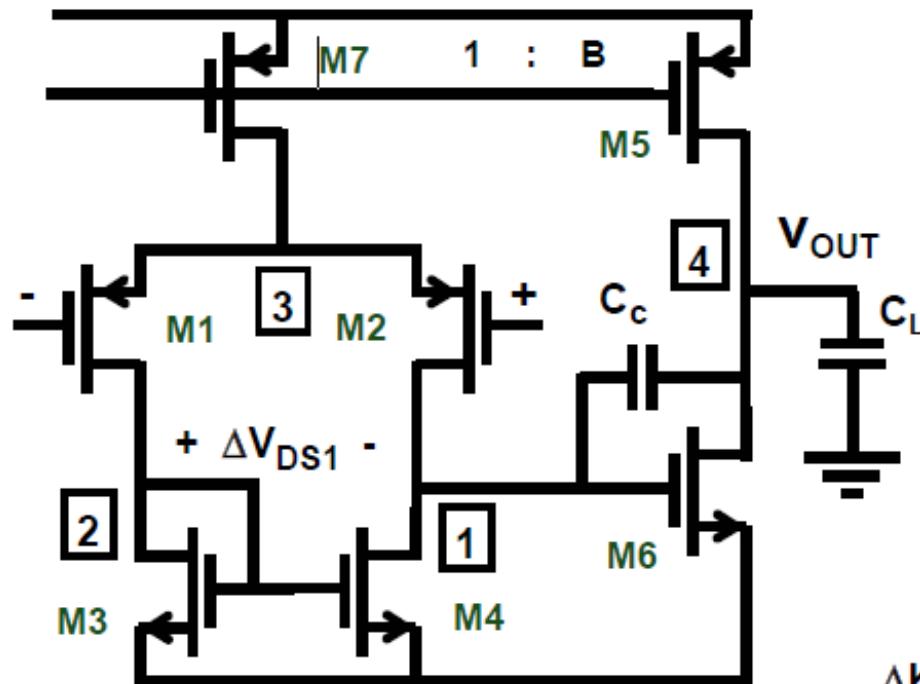
$$\frac{1}{\text{CMRR}} = \frac{1}{\text{CMRR}_r} + \frac{1}{\text{CMRR}_s}$$



》》两级运放中的失调现象



》》两级运放中的失调现象

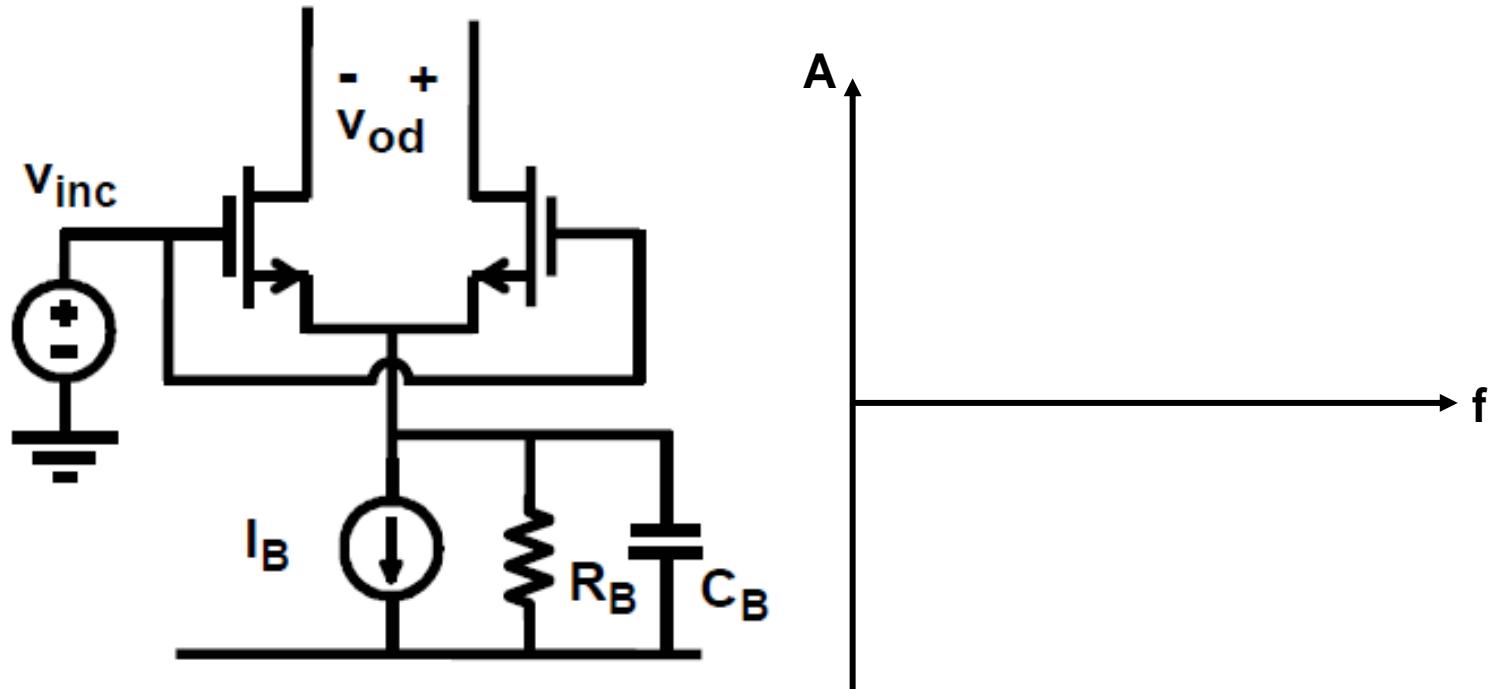


$$A_{v1} = g_{m1} r_{o2} // r_{o4}$$

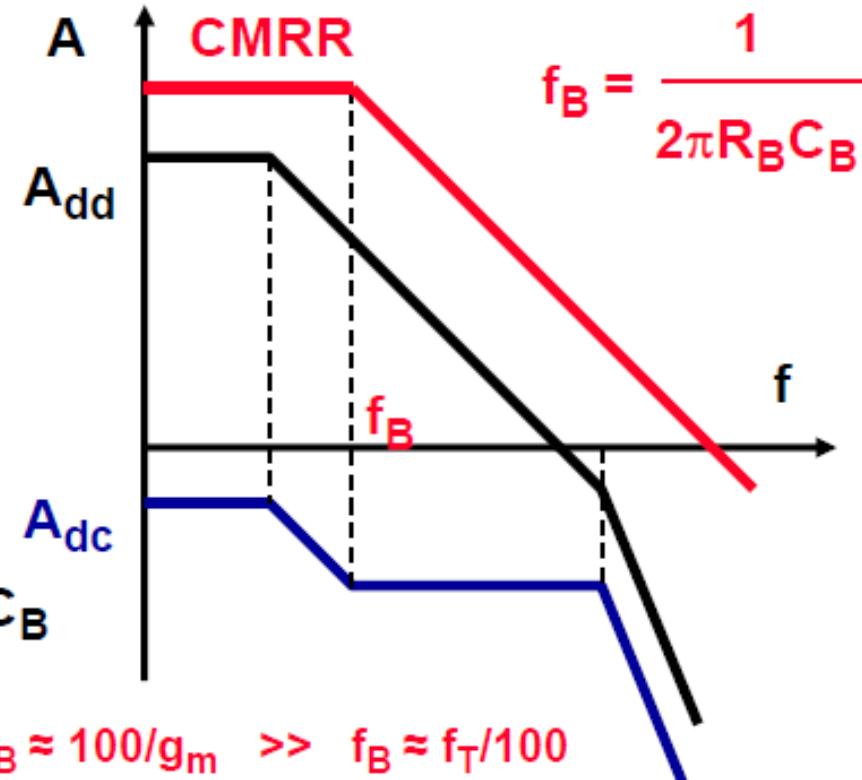
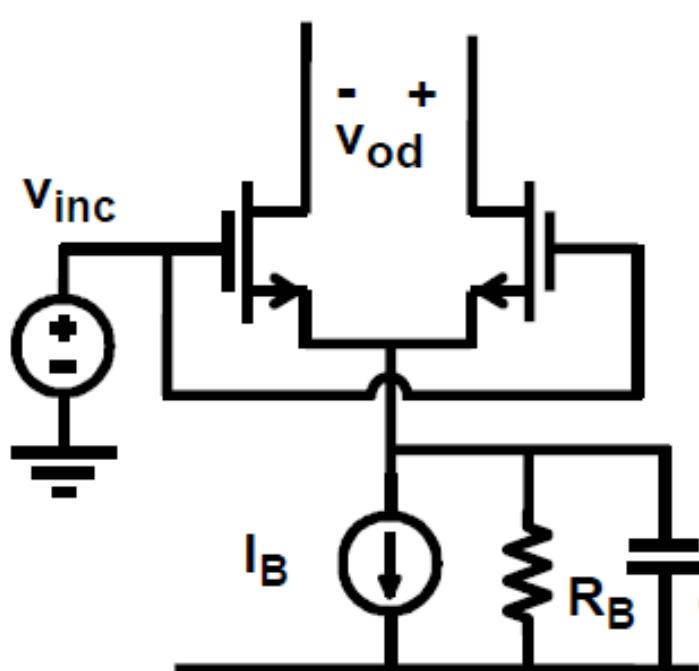
$$\begin{aligned} v_{OS} = & \frac{\Delta V_{DS1}}{A_{v1}} + \\ & \Delta V_{T1} + \frac{g_{m3}}{g_{m1}} \Delta V_{T3} * + \\ & + \frac{V_{GS1} - V_T}{2} S \end{aligned}$$

$$S = \frac{\Delta K'_n}{K'_n} + \frac{\Delta K'_p}{K'_p} + \frac{\Delta W/L_1}{W/L_1} + \frac{\Delta W/L_3}{W/L_3}$$

》》 CMRR的频率特性



» CMRR的频率特性





失调与CMRR

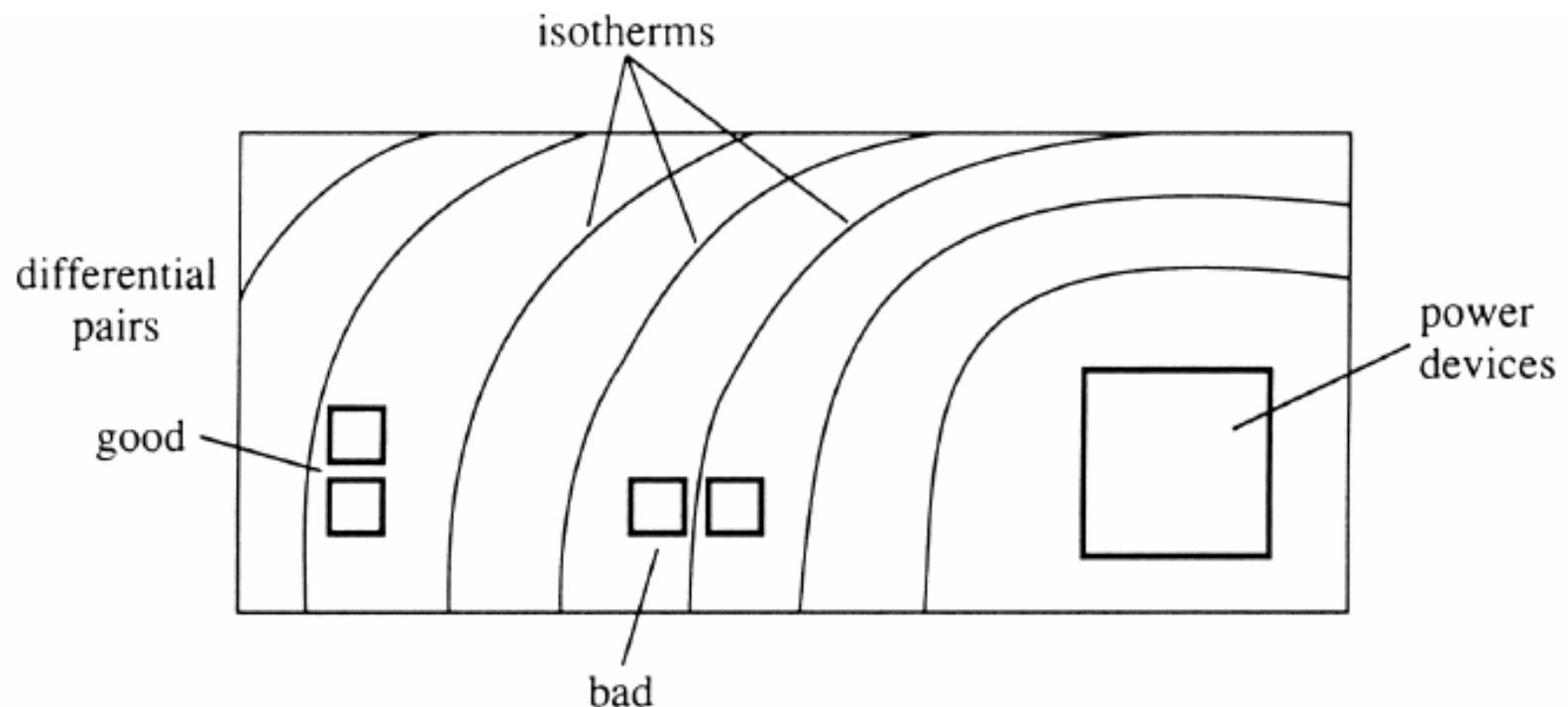
- 随机性失调和 $CMRR_R$
- 系统性失调和 $CMRR_S$
- **设计守则**



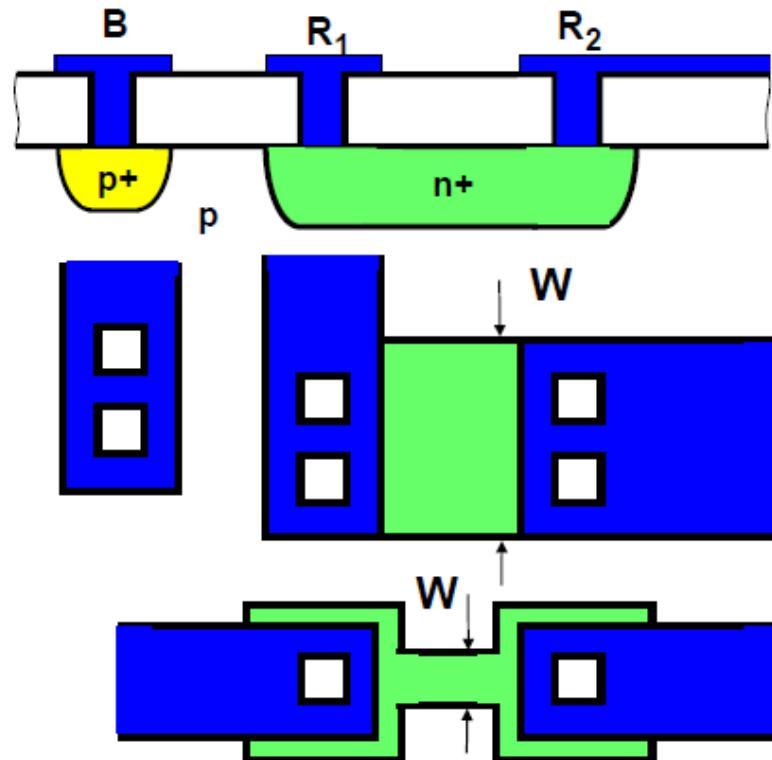
设计守则

- 相同的特性
- 相同的温度
- 增大尺寸
- 减小间距
- 同样的方向
- 同样的长宽比
- 中心对称
- Dummy

» 相同的温度



》》 电阻的版图



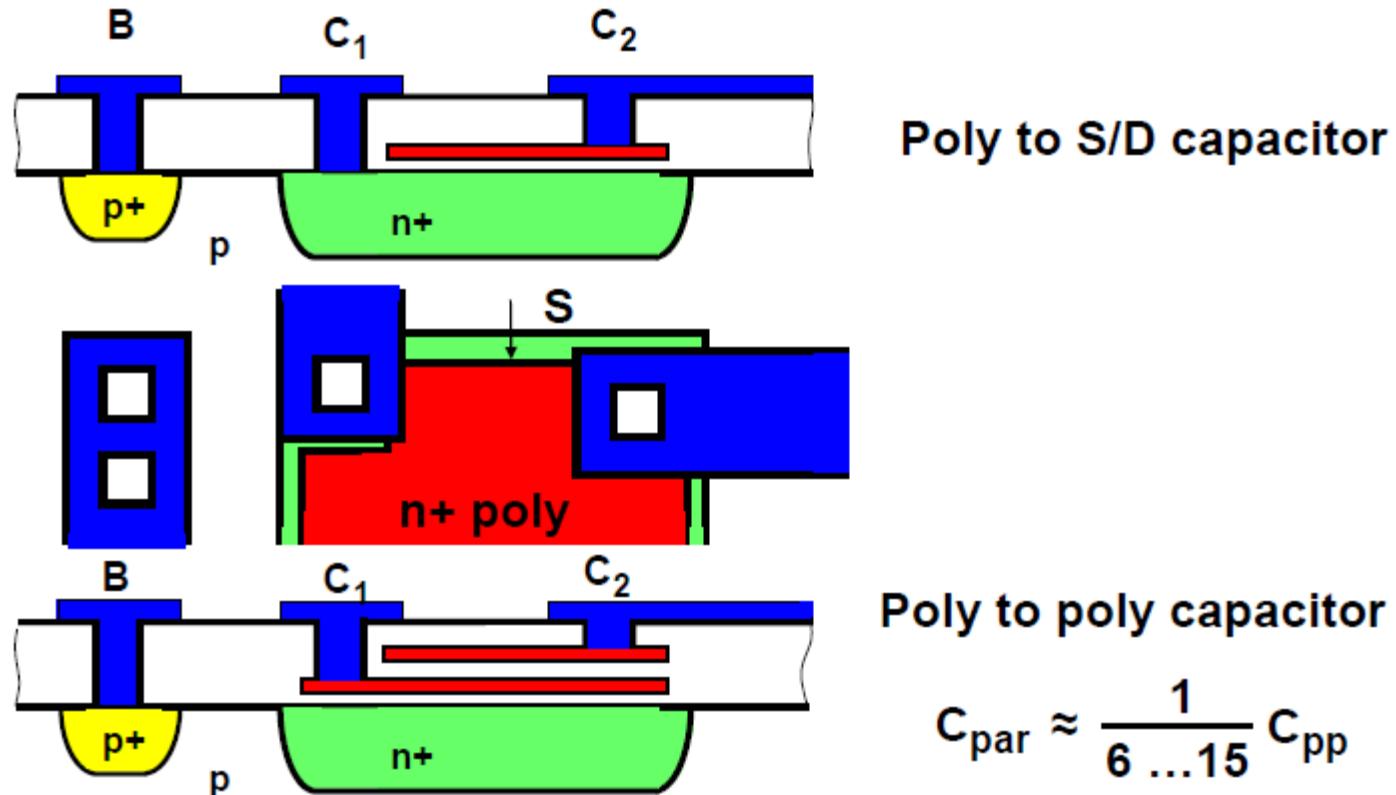
Source/drain
diffusion
resistor
in CMOS

Ref.: Laker, Sansen :
Design of analog ...,
MacGrawHill 1994
Table 2-6

》》 电阻的实现方式及对比

Process	Type	ρ □ Ω/□	absolute accuracy percent	temperature coefficient percent/°C	voltage coefficient percent/V	breakdown voltage V
CMOS	S/D diffusion	20-50	20	0.2	0.5	20
	well	2.5k	10	0.3	1	20
	poly gate	50	20	0.2	0.05	40
	poly resistance	1.5k	1	0.05	0.02	20
	aluminum	50m	20	0.01	0.02	90

》》电容的版图

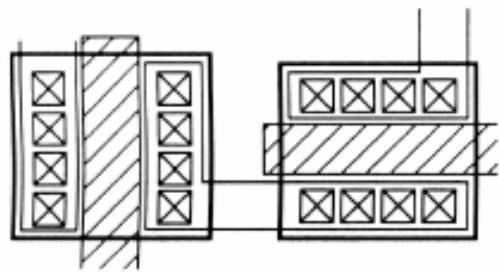


电容的实现方式及对比

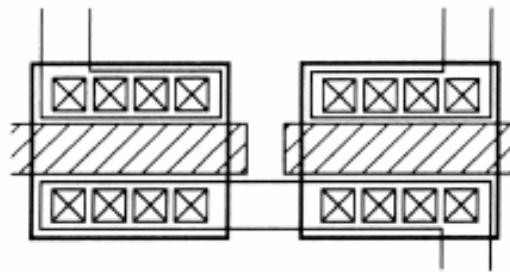
Process	Type	C Nf/cm ²	absolute accuracy percent	temperature coefficient percent/°C	voltage coefficient percent/V	breakdown voltage V
CMOS	$C_{ox}(50nm)$	70	5	0.002	0.005	40
	$C_{m,poly}$	12	10	0.002	0.005	40
	$C_{poly,poly}$	56	2	0.002	0.005	40
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20
	$C_{m,substrate}$	5.2	10	0.01	0.05	20
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20

Ref.:Laker,Sanse:
Design of analog...,
MacGrawHill 1994
Table 2-7

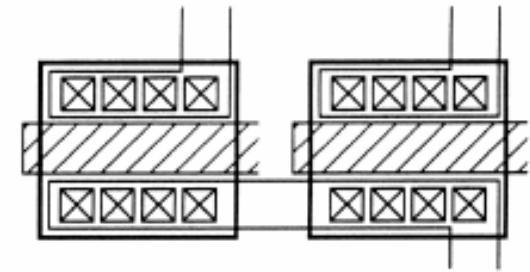
》》差分对的匹配



Bad



Better

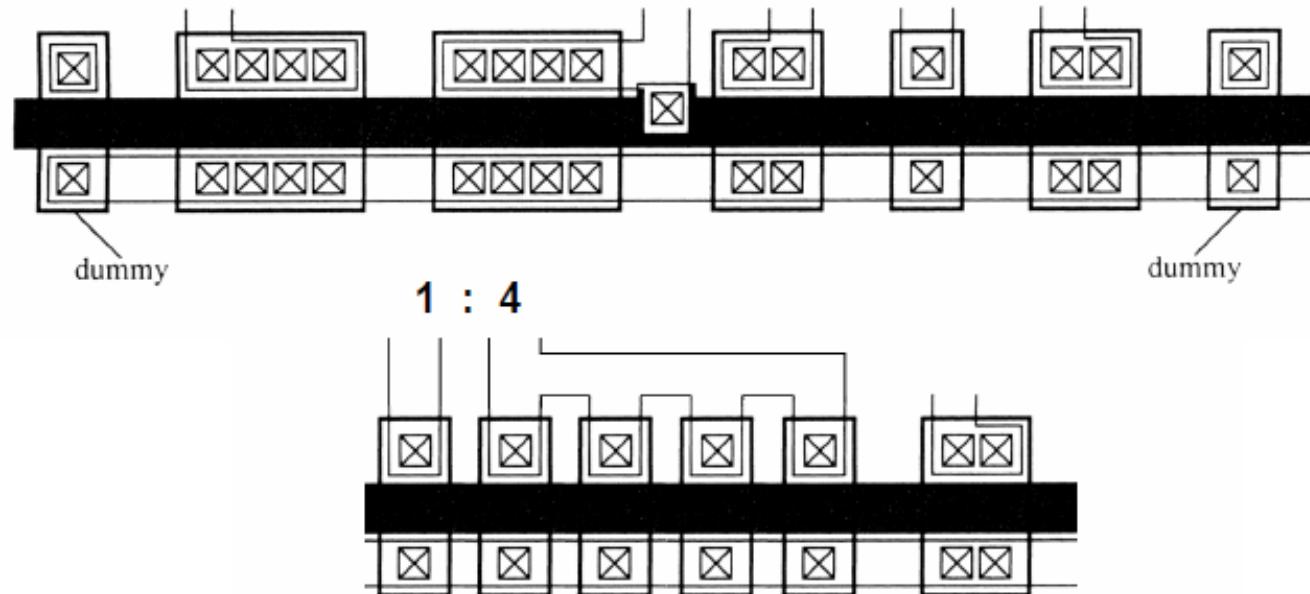


Better

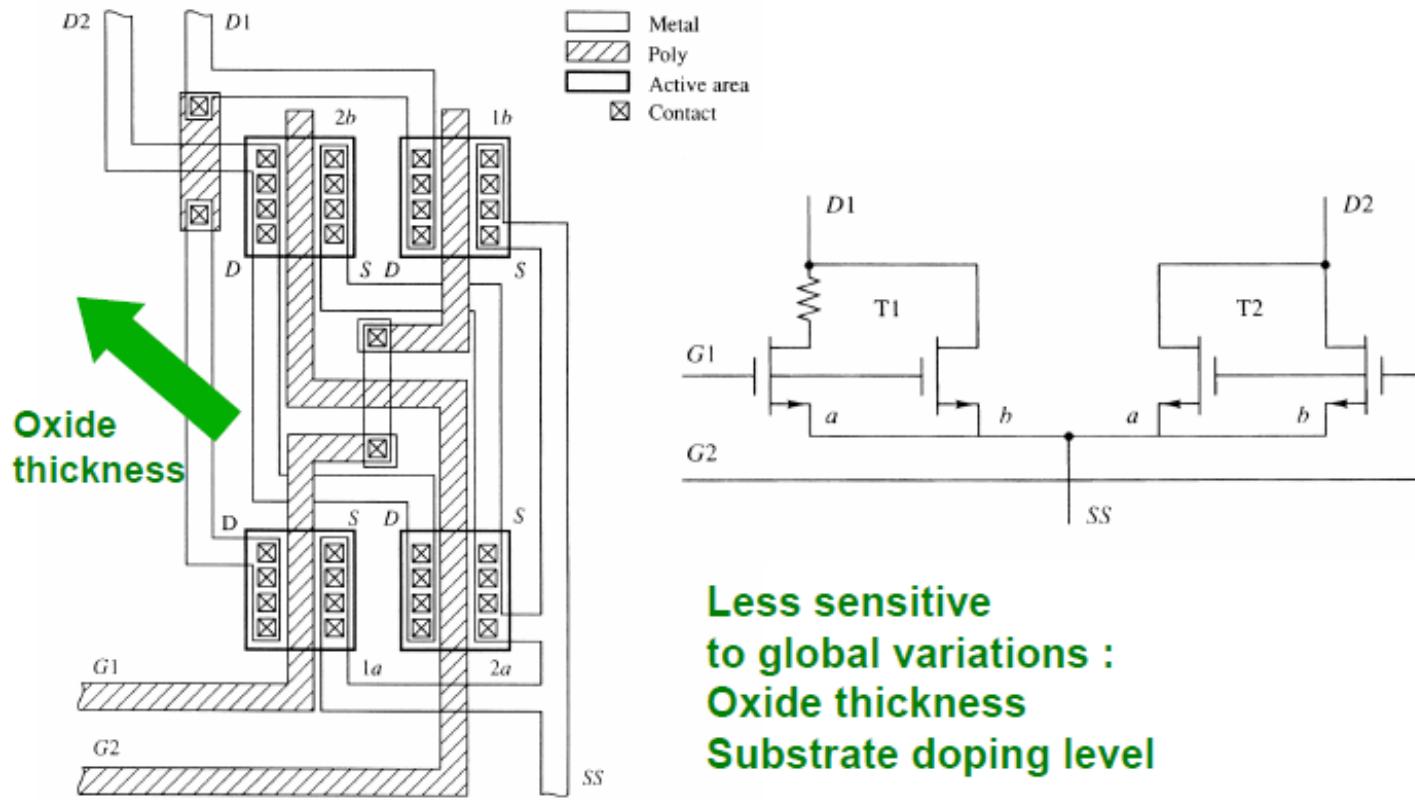
》》 同样的长宽比

Current mirror 4:4:2:1:2 with end dummies.

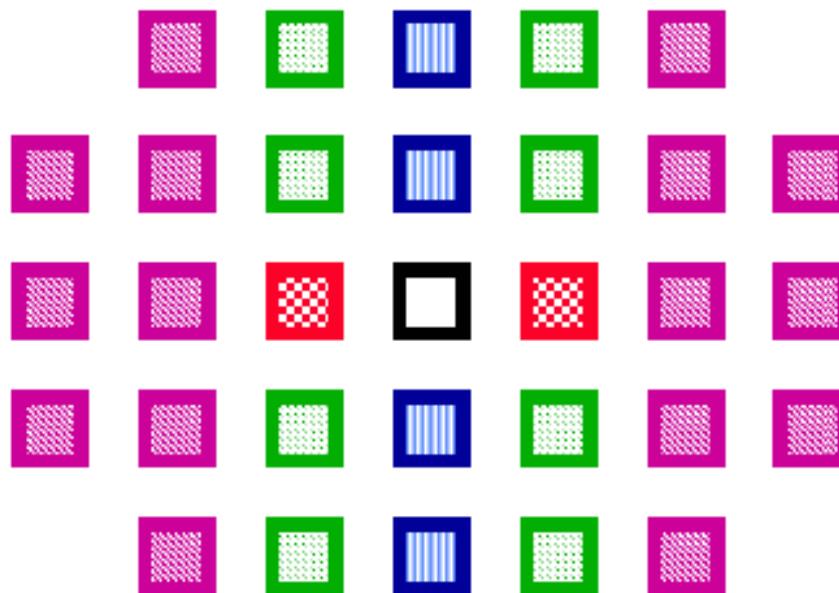
 Metal  Active area
 Poly  Contact



》》 中心对称的版图



》》 中心对称的版图



Ratio:

1
2
4
8
16

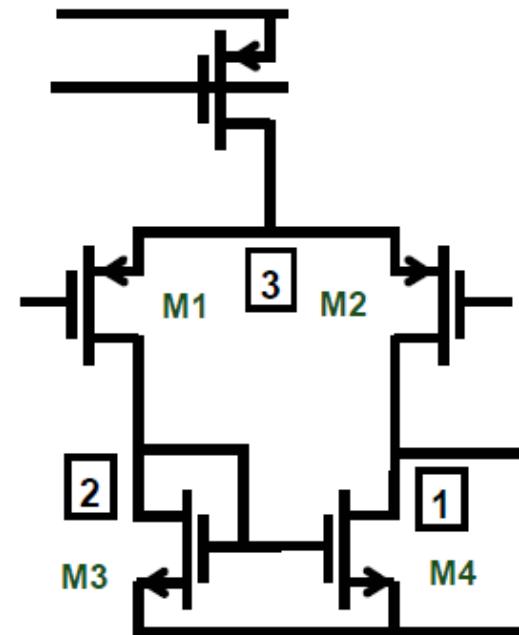


设计思路总结

1. 与噪声的设计一样，差分对需要 V_{GST} 尽量小，而电流镜则需要 V_{GST} 尽量大
2. 失调的优化与CMRR的优化相同，超高的CMRR往往需要后期的Calibration.
3. 在版图中选择合适的被动器件，以及优秀的版图技巧都能改善失调的现象。

》》课后作业

- 对一偏置电流为 $100\mu\text{A}$ 的五管OTA，共模电压为 0.9V ，设计晶体管的尺寸，
 1. 使其在单位增益负反馈时系统性失调小于 0.1mV ；
 2. 使其随机性失调的标准差 (std) 小于 1mV ；
 3. 使其共模抑制比大于 50dB 。



第5章 运放



CMOS模拟集成电路设计

第四章：运放的稳定性与系统性设计

胡远奇

©2020



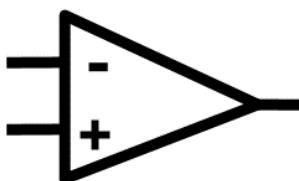
运放的稳定性与系统性设计

- **运放、反馈与稳定性的基本概念**
- 极点分离与零点补偿
- 三级运放稳定性问题简介
- 运放的系统性设计方法
- 运放的其他参数指标

》》运算放大器的分类

Opamp

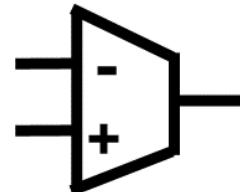
Operational
amplifier



$$A_v = \frac{V_{OUT}}{V_{IN}}$$

OTA

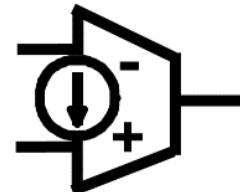
Operational
Transconduct.
amplifier



$$A_g = \frac{i_{OUT}}{V_{IN}}$$

OCA

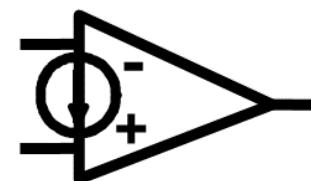
Operational
Current
amplifier



$$A_i = \frac{i_{OUT}}{i_{IN}}$$

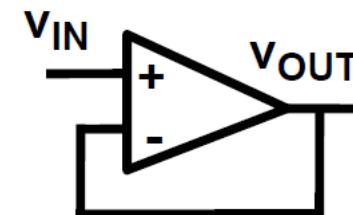
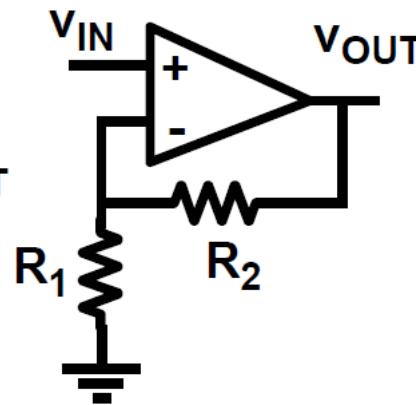
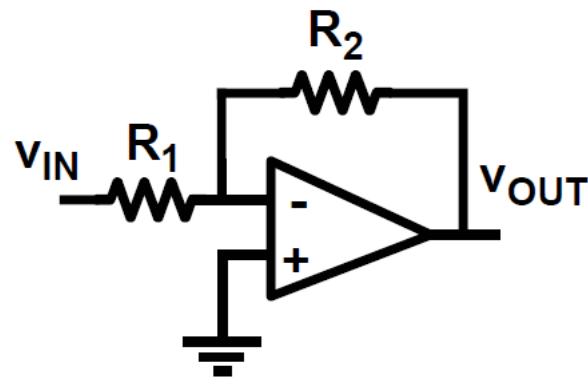
CM amp

Current
Mode
amplifier



$$A_r = \frac{V_{OUT}}{i_{IN}}$$

》》负反馈配置



$$A_v = -\frac{R_2}{R_1}$$

$$A_v = 1 + \frac{R_2}{R_1}$$

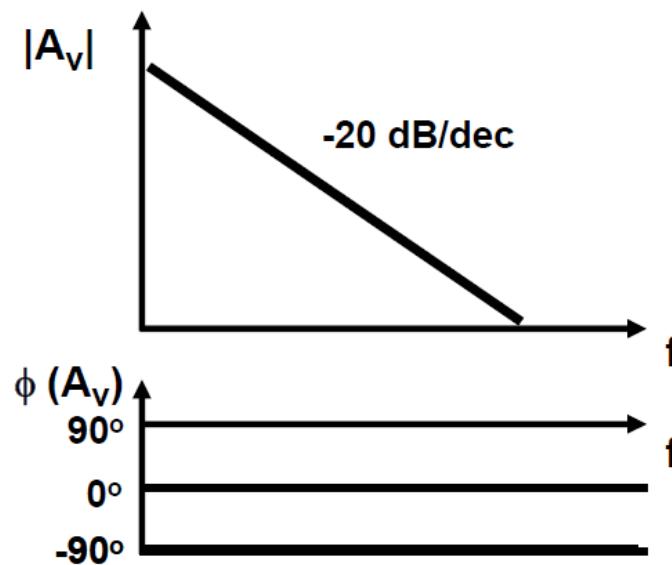
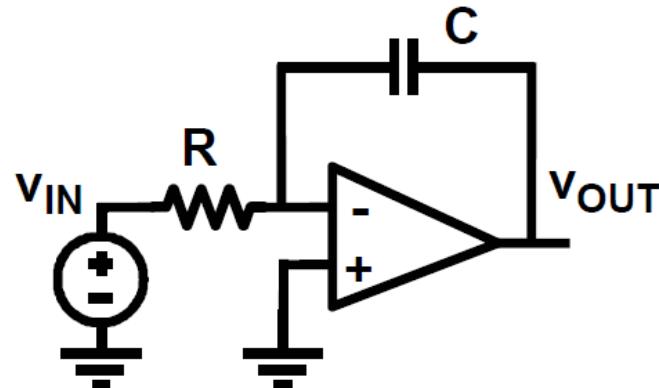
$$A_v = 1$$

$$R_{IN} = R_1$$

$$R_{IN} = \infty$$

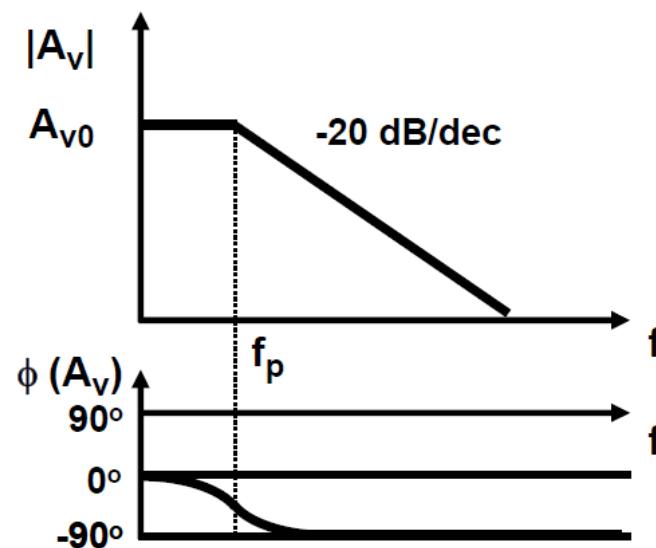
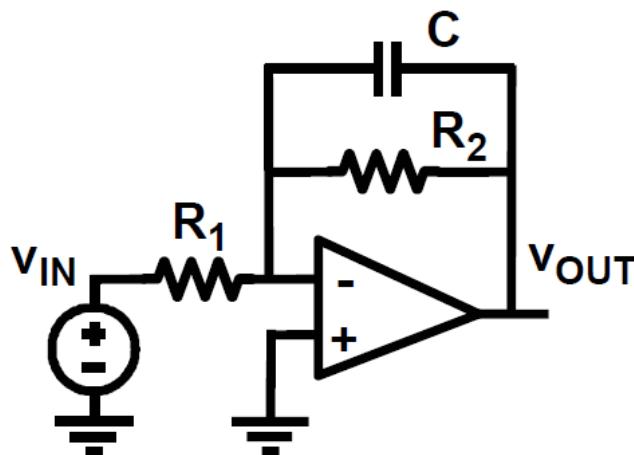
$$R_{IN} = \infty$$

》》 积分器 (Integrator)



□ 假设运放为理想运放，当 V_{IN} 为一个1V的阶跃输入信号时，
画出输出 V_{OUT} 的。

》》 低通濾波器 (Low-pass Filter / Lossy Integrator)



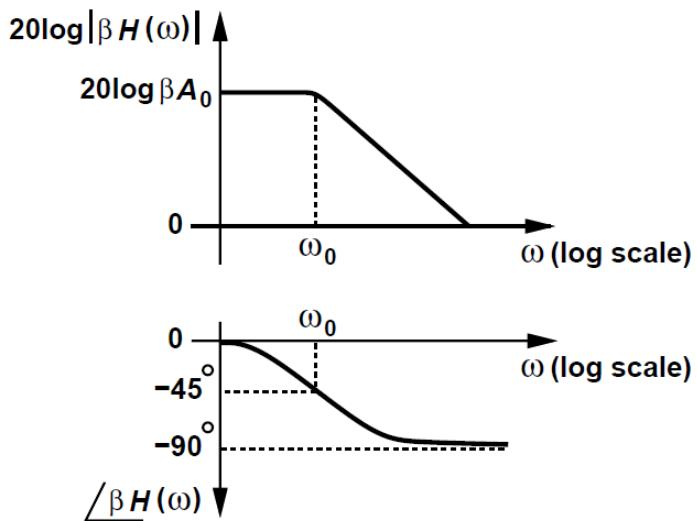
$$A_{v0} = - \frac{R_2}{R_1}$$

$$A_v = \frac{A_{v0}}{\left(1 + j \frac{f}{f_p}\right)}$$

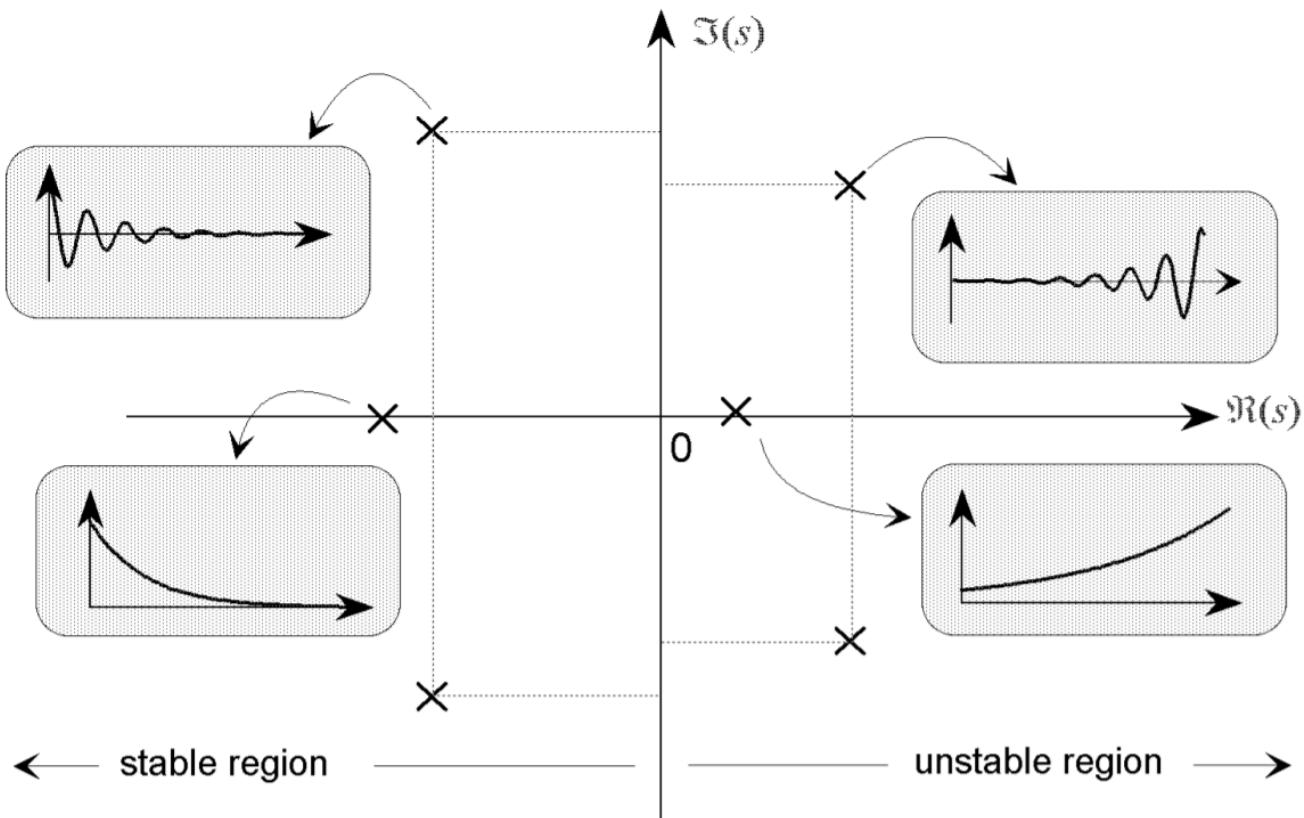
$$f_p = \frac{1}{2\pi R_2 C}$$

»» 波特图

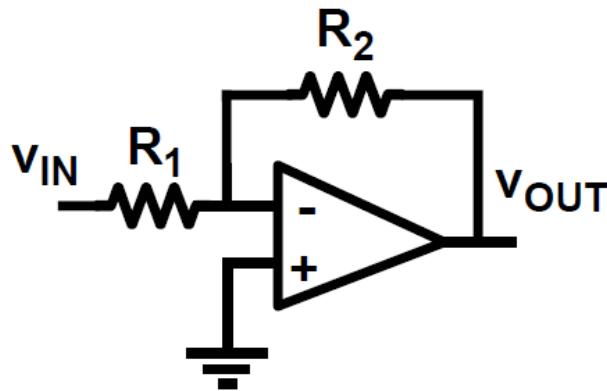
- **幅度**曲线的斜率在每个零点处变化+20dB/dec，在每个极点处变化-20dB/dec。
- **相位**在极点频率的1/10处变化，在极点处经历-45度的变化，并且在10倍极点处达到-90度的变化。
- 相位变化的速度**快于**幅度变化。



》》 极点对系统的影响



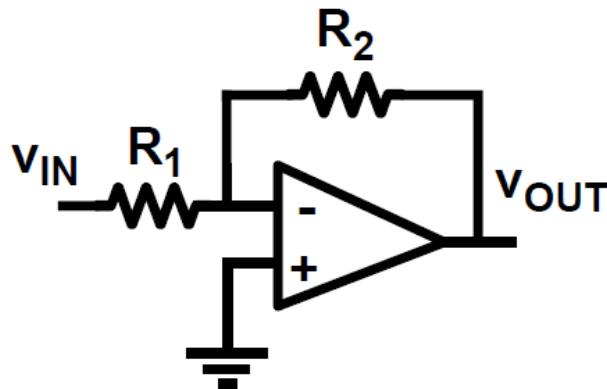
》》 增益与带宽的交换



□ 假设运放的增益带宽积为 GBW_0 ,
该反馈电路带宽为多少?

$$A_v = - \frac{R_2}{R_1}$$

》》增益与带宽的交换



$$A_v = - \frac{R_2}{R_1}$$

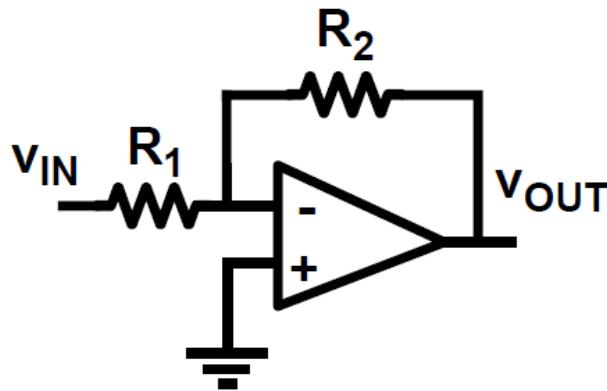
□ 假设运放的增益带宽积为 GBW_0 ,
该反馈电路带宽为多少?

$$A(s) = \frac{A_0}{\left(1 + \frac{s}{\omega_0}\right)}$$

$$H(s) = \frac{A_0 R_2}{A_0 R_1 + R_1 + R_2 + \frac{s(R_1 + R_2)}{\omega_0}}$$

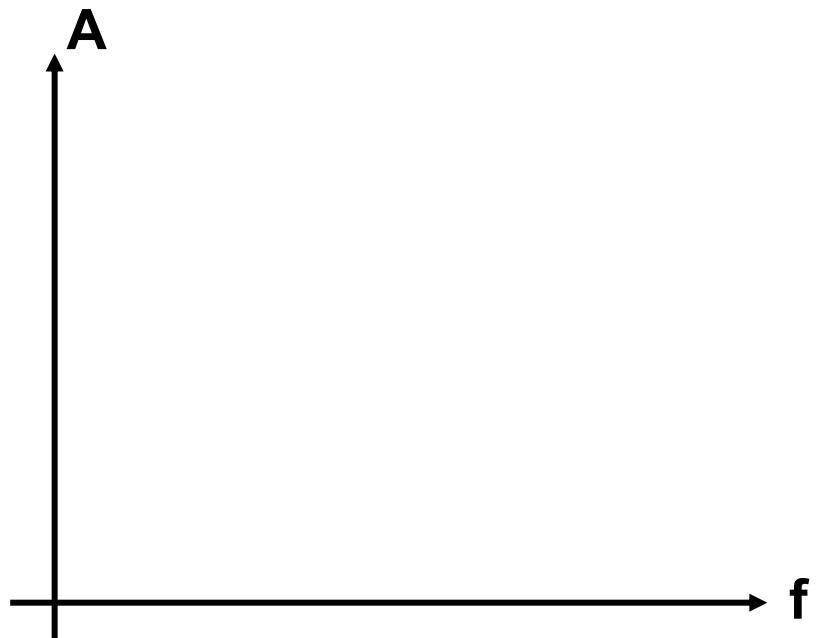
$$p'_d \approx \frac{A_0 \omega_0 \cdot R_1}{R_1 + R_2} = 2\pi GBW_0 \frac{R_1}{R_1 + R_2}$$

》》增益与带宽的交换



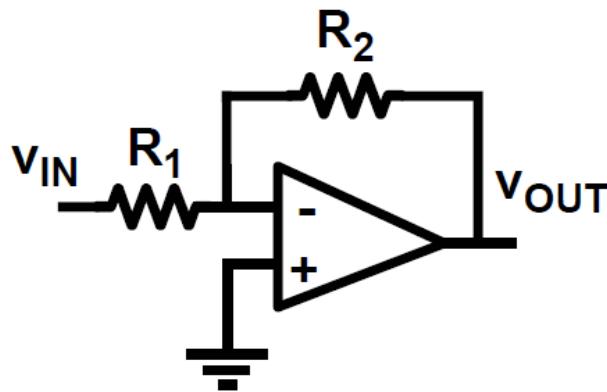
$$A_v = - \frac{R_2}{R_1}$$

GBW不变!



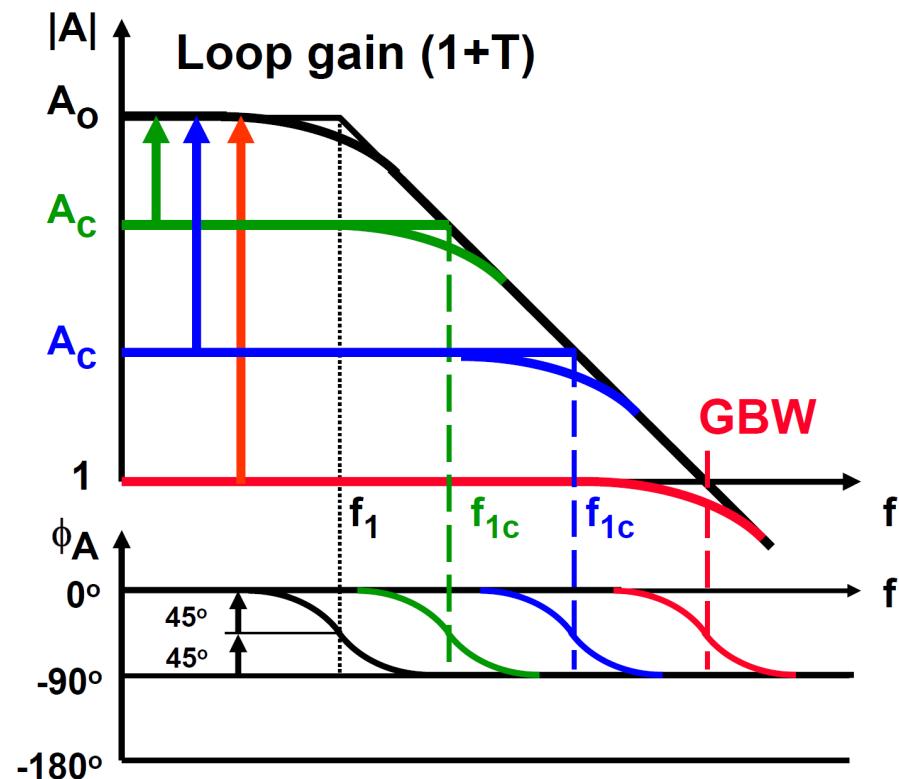
$$p'_d \approx \frac{A_0 \omega_0 \cdot R_1}{R_1 + R_2} = GBW_0 \frac{R_1}{R_1 + R_2}$$

》》 增益与带宽的交换

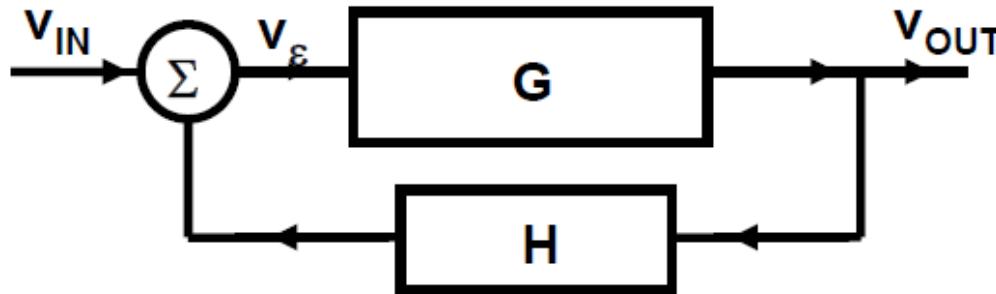


$$A_v = - \frac{R_2}{R_1}$$

GBW不变!

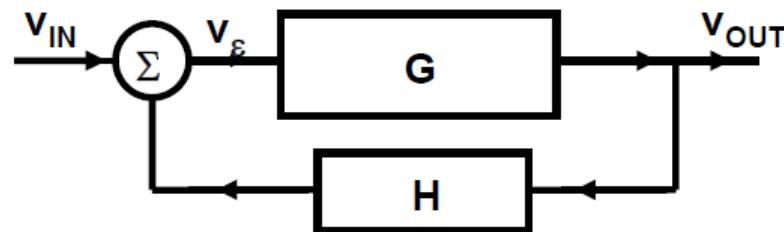
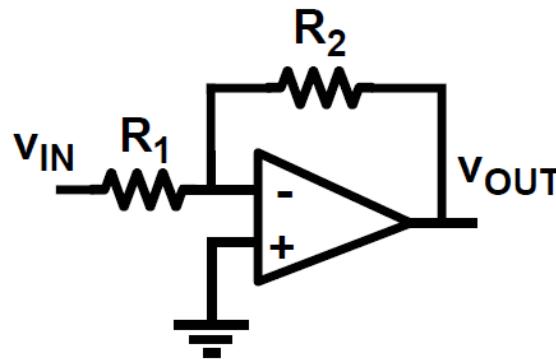


》》开环与闭环增益



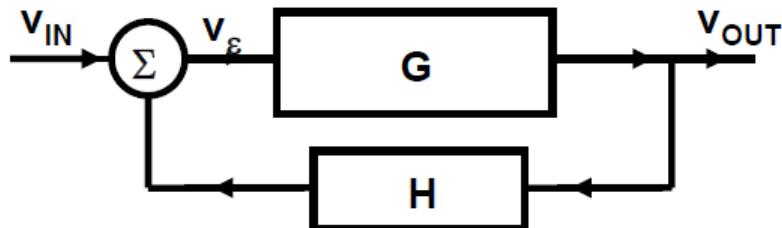
- **闭环增益:** $A_c = \frac{V_{OUT}}{V_{IN}} = \frac{G}{1 + GH}$
- **开环增益:** $A_o = G$
- **环路增益:** $A_L = GH$ ← **决定了反馈系统的所有特性!**

》》开环与闭环增益



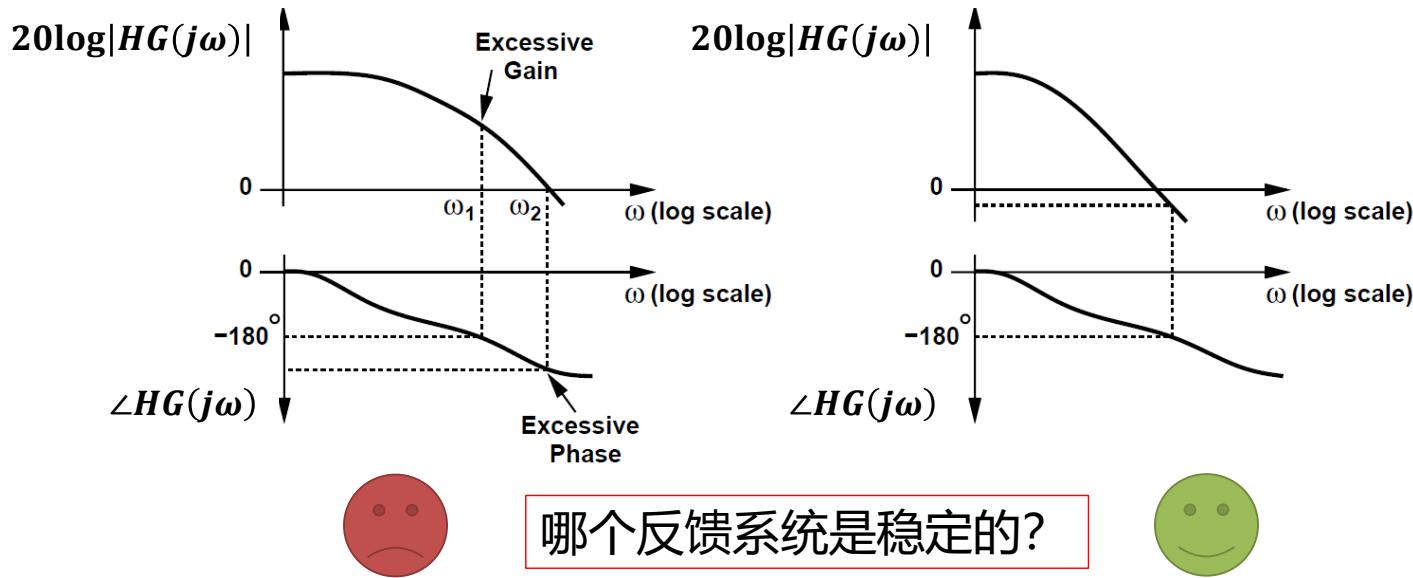
- **闭环增益:** $A_C = -R_2/R_1$ $H = R_1/(R_2 + R_1)$
- **开环增益:** $A_O = A_0$
- **环路增益:** $A_L = A_0 \cdot R_1/(R_2 + R_1)$ ← 通过反馈改变环路增益

» 反馈的稳定性判据



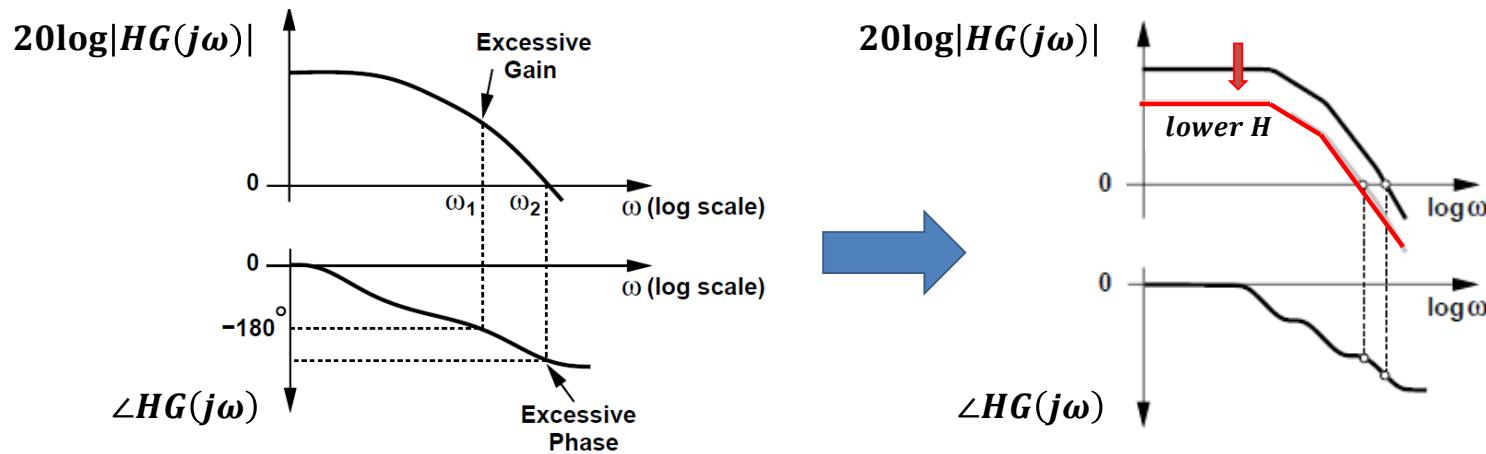
- 反馈系统存在潜在的不稳定性，并且可能会发生振荡。
- 闭环传递函数：
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{G(s)}{1 + HG(s)}$$
- “巴克豪森判据” -》 如果分母变为0会发生什么 $|HG(j\omega)| = 1$
 $\angle HG(j\omega) = -180^\circ$
- 负反馈本身提供 180° 相移

» 稳定性判定



- 增益为1和相位为-180度时的频率点分别称为“增益交点(GX)”和“相位交点(PX)”。
- PX必须落后于GX，GX等于开环系统中的单位增益带宽

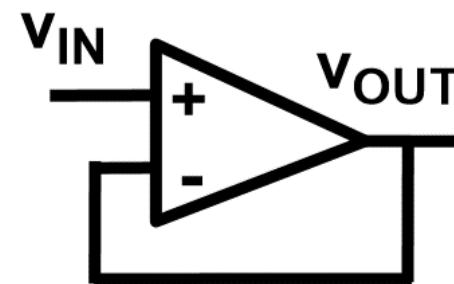
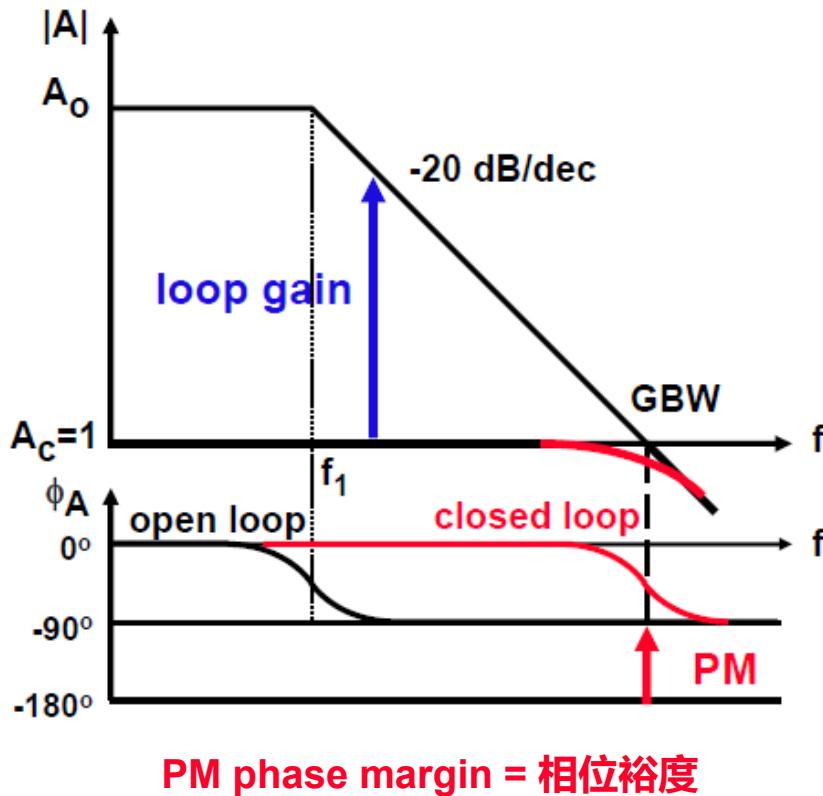
例1



□ 如果反馈系数减小，之前描述的系统是变得更稳定还是更不稳定？

解：如果 β 减少，使 $20\log\angle HG(\omega)$ 的图下移，GX向左移。由于相位不变，系统变得更稳定。

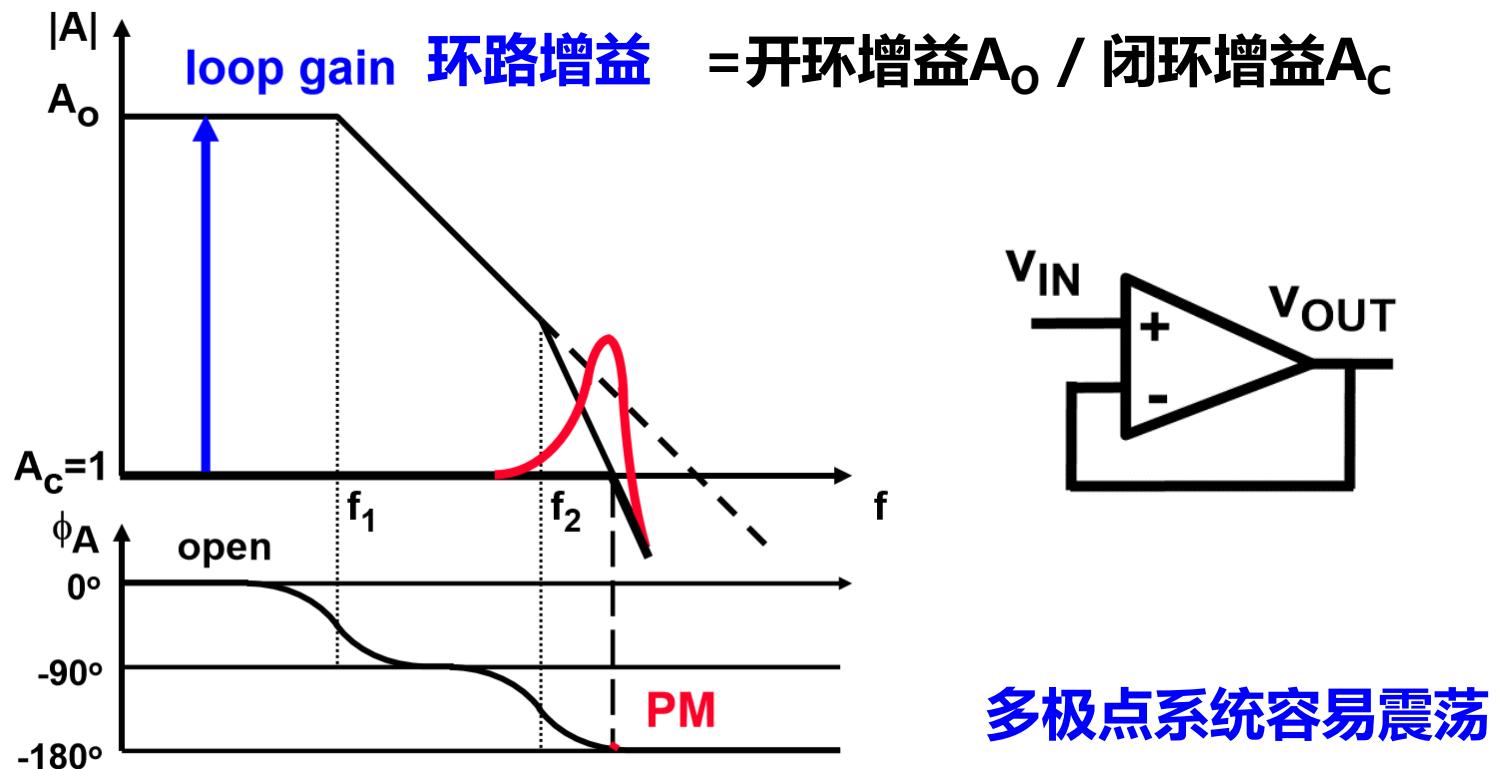
》》单极点系统



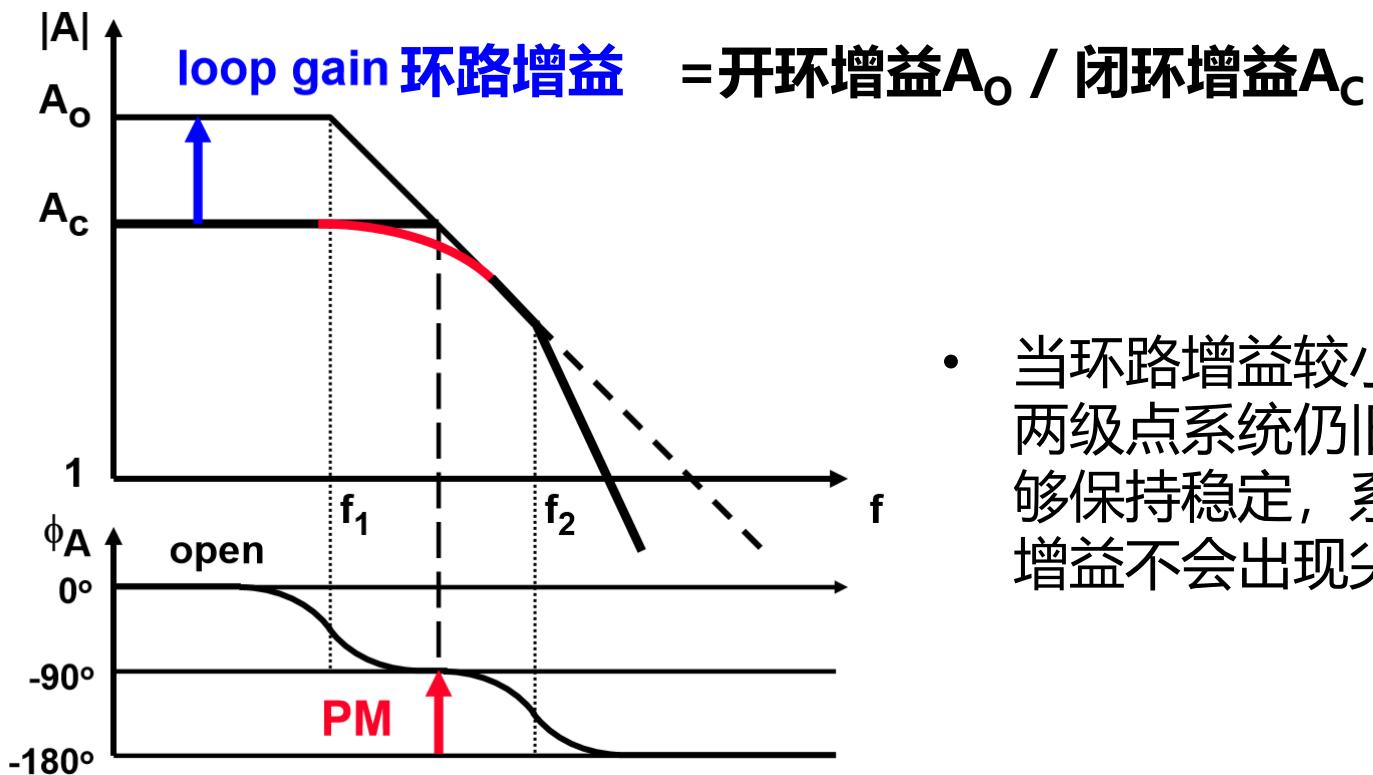
- 闭环增益 = 1
- 开环增益 = A_0

单极点系统天然稳定

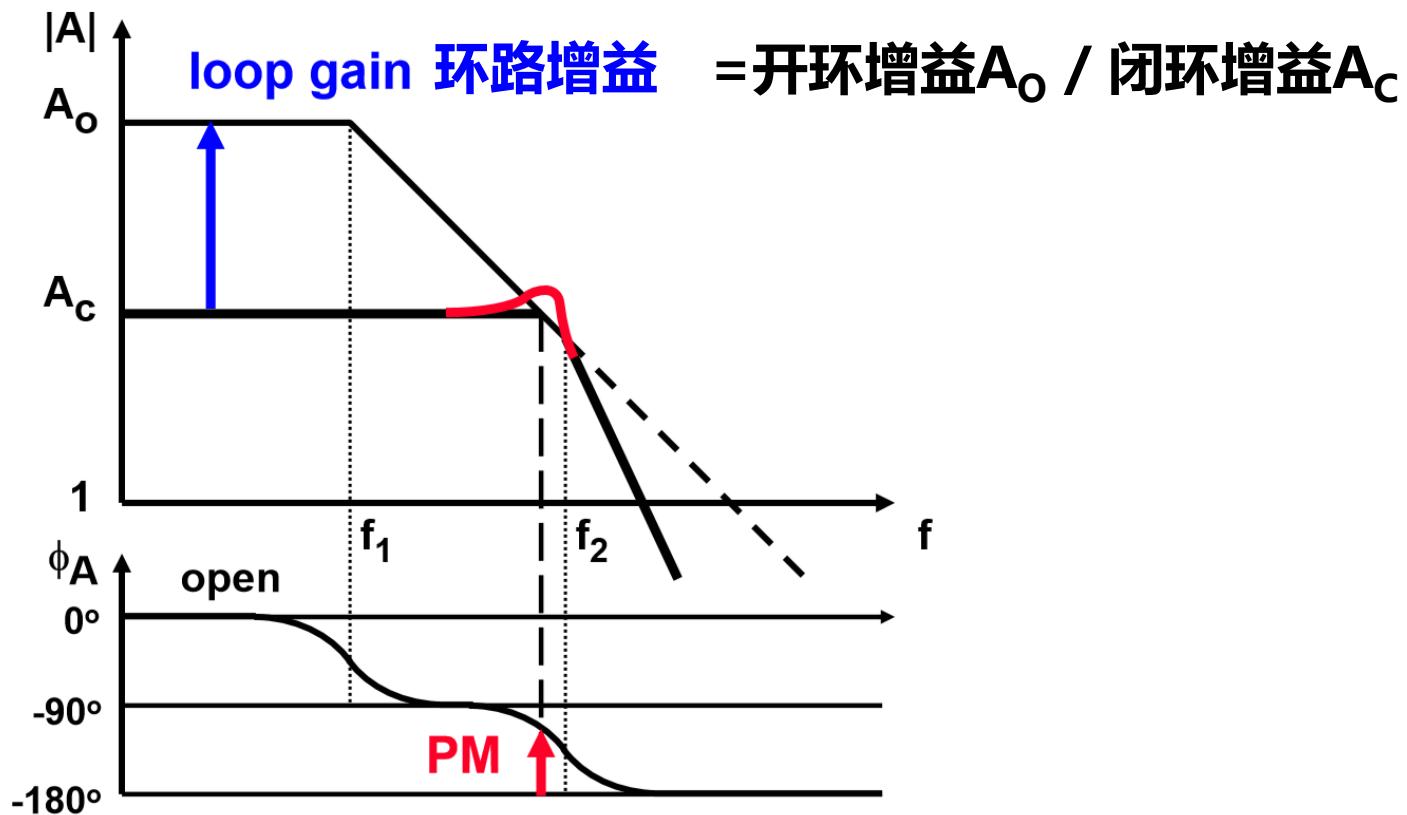
》》两极点系统



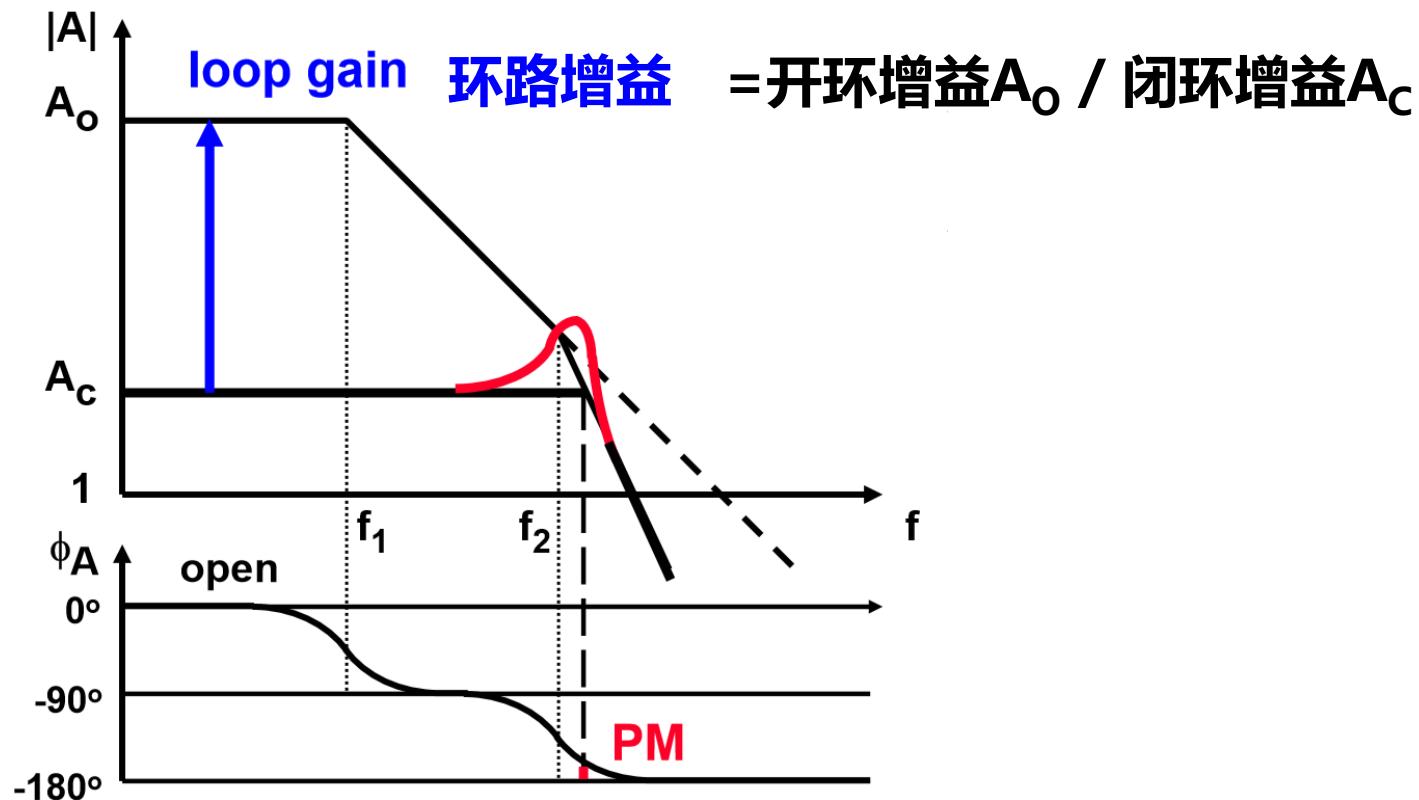
》》两极点系统



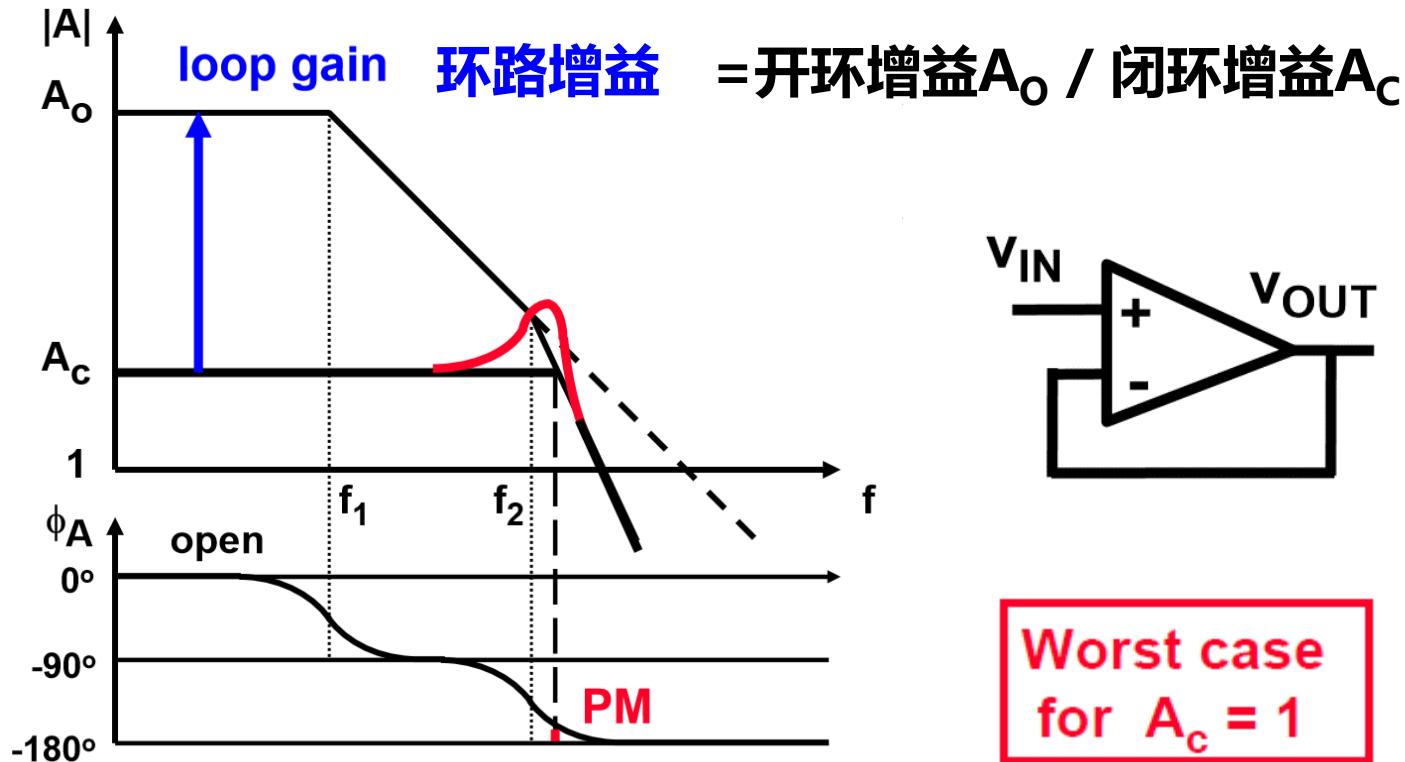
》》两极点系统



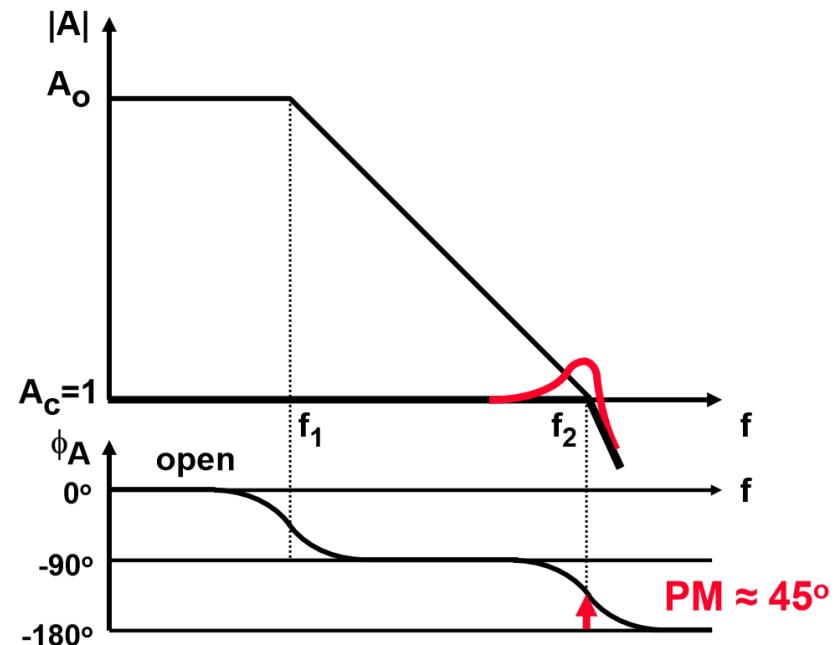
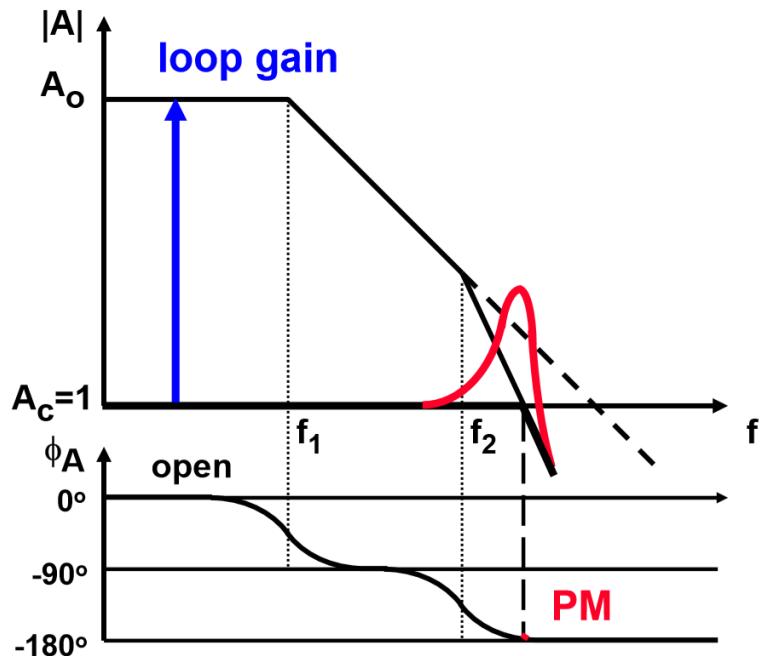
》》两极点系统



》》两极点系统

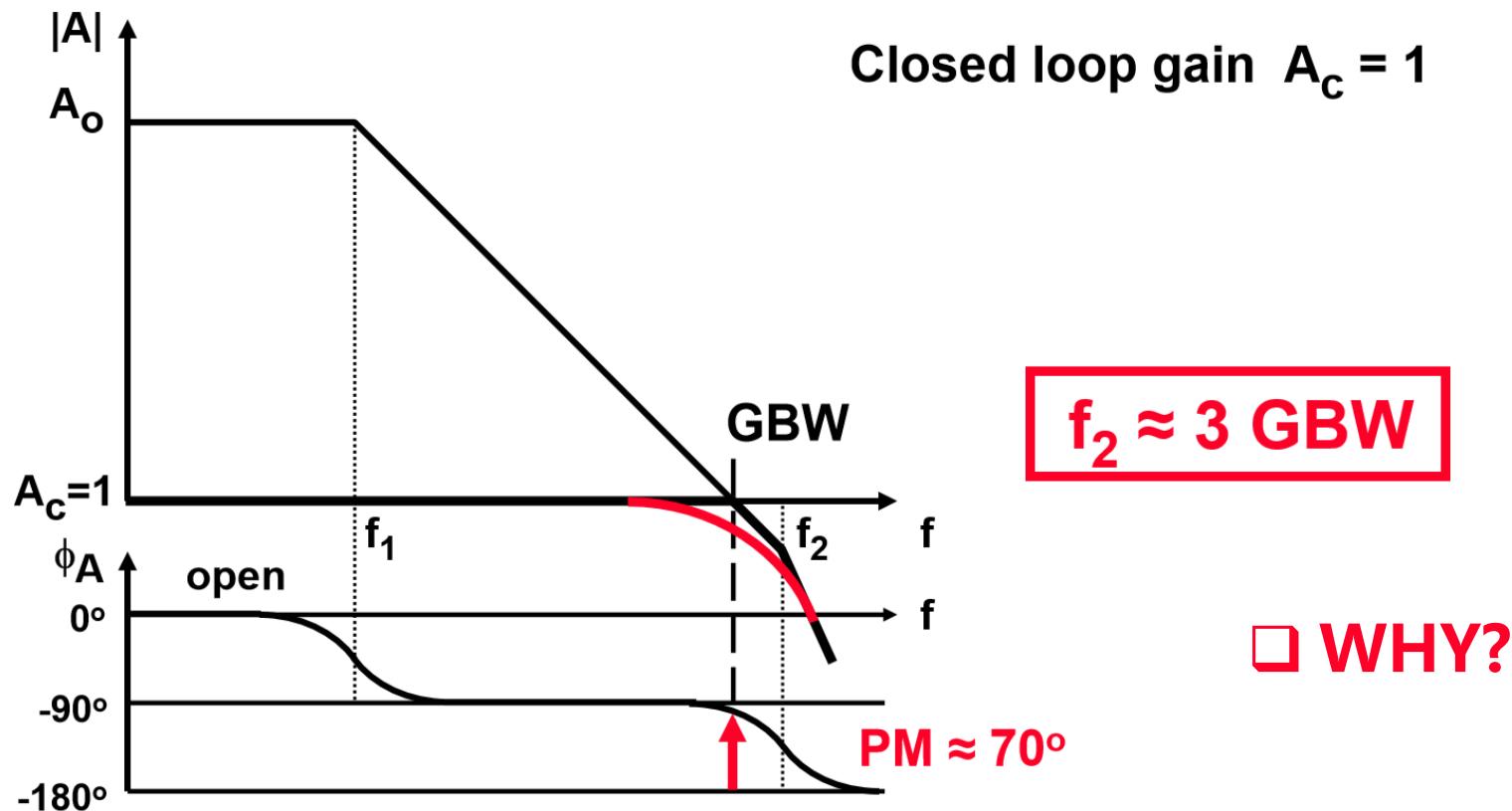


》》两极点系统：推远非主极点



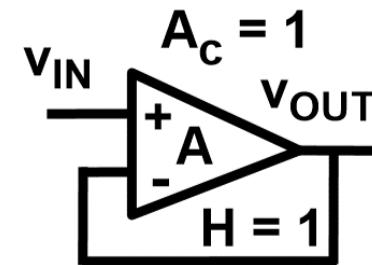
次极点刚好为增益带宽积

》》两极点系统：推远非主极点



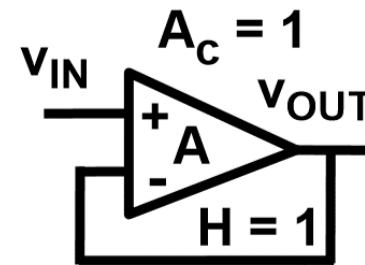
相位裕度的计算

$$\text{Open loop gain } A = \frac{A_o}{(1 + j \frac{f}{f_1})(1 + j \frac{f}{f_2})}$$



相位裕度的计算

$$\text{Open loop gain } A = \frac{A_o}{(1 + j \frac{f}{f_1})(1 + j \frac{f}{f_2})}$$



$$\begin{aligned}\text{Closed loop gain } A_c &= \frac{A}{1+A} \approx \frac{1}{1 + j \frac{f}{\text{GBW}} + j^2 \frac{f^2}{\text{GBW } f_2}} \\ &\approx \frac{1}{1 + j 2\zeta \frac{f}{f_r} + j^2 \frac{f^2}{f_r^2}}\end{aligned}$$

ζ is the damping ($=1/2Q$)

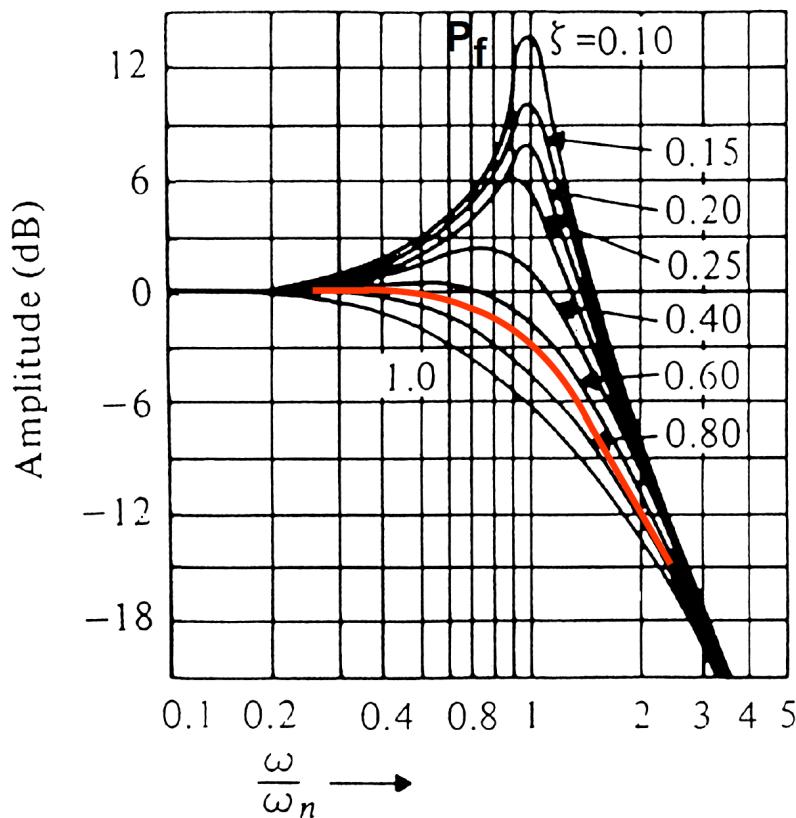
f_r is the resonant frequency

相位裕度的计算

$$f_r = \sqrt{GBW f_2} \quad PM (\circ) = 90^\circ - \arctan \frac{GBW}{f_2} = \arctan \frac{f_2}{GBW}$$

$\frac{f_2}{GBW}$	PM (°)	$\zeta = \frac{1}{2} \sqrt{\frac{f_2}{GBW}}$	P _f (dB)	P _t (dB)
0.5	27	0.35	3.6	2.3
1	45	0.5	1.25	1.3
1.5	56	0.61	0.28	0.73
2	63	0.71	0	0.37
3	72	0.87	0	0.04

》》 频域响应



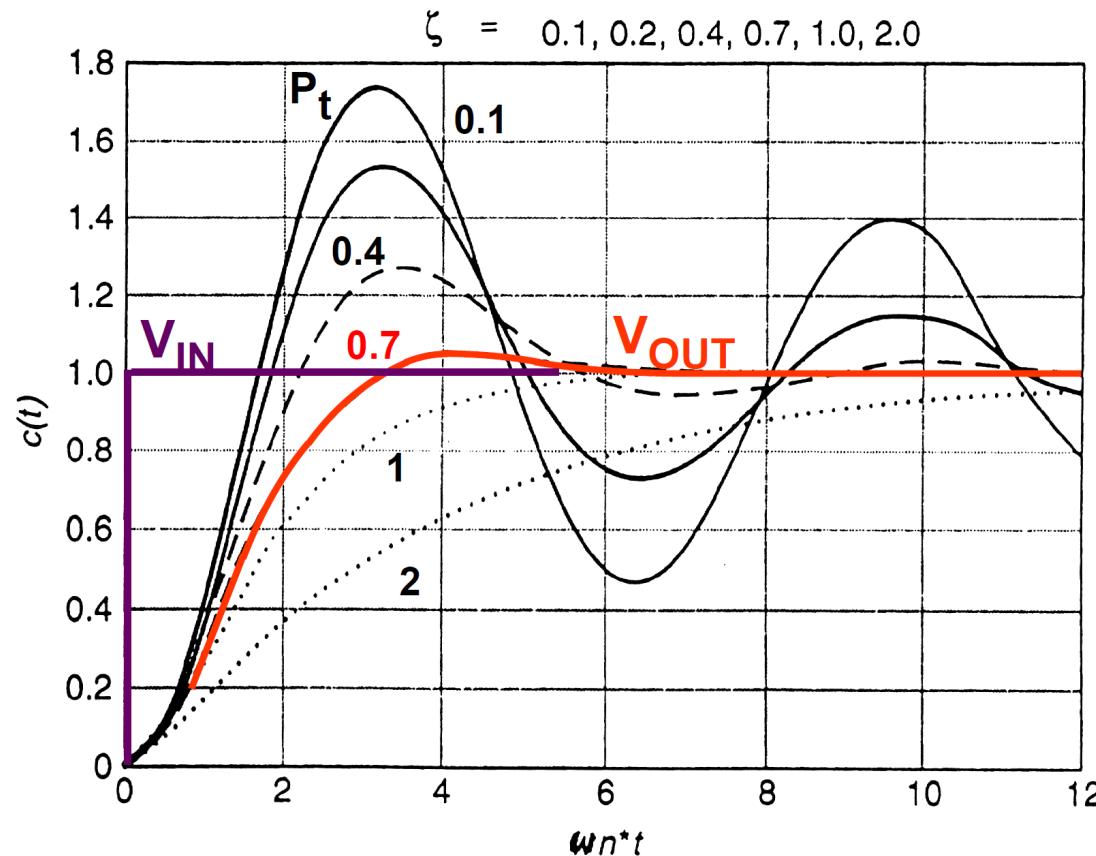
震荡

$$\zeta = Q = 0.7$$

带宽

$$P_f = \frac{1}{2 \zeta \sqrt{1 - \zeta^2}}$$

时域响应



$$\zeta = Q = 0.7$$

$$P_t =$$

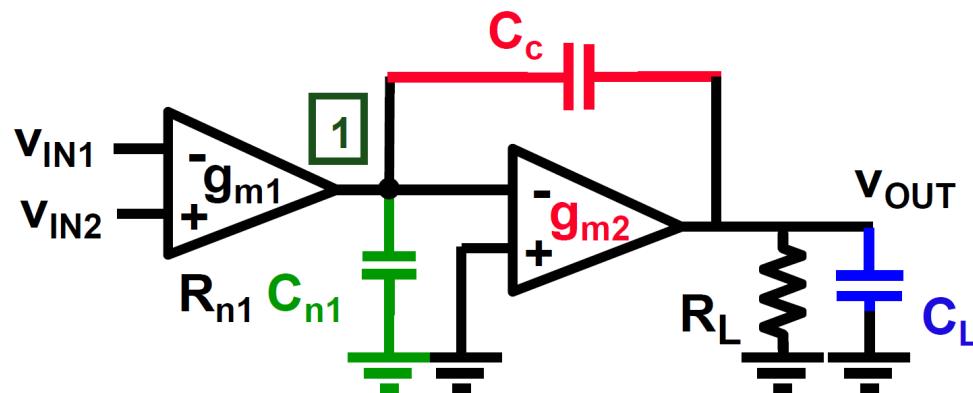
$$\frac{-\pi \zeta}{1 + e^{\sqrt{1 - \zeta^2}}}$$



运放的稳定性与系统性设计

- 运放、反馈与稳定性的基本概念
- **极点分离与零点补偿**
- 三级运放稳定性问题简介
- 运放的系统性设计方法
- 运放的其他参数指标

》》 标准两级运放



$$A_{v0} = -A_{v1}A_{v2}$$

$$A_{v1} = g_{m1}R_{n1}$$

$$A_{v2} = g_{m2}R_L$$

$$1 - \frac{C_c}{g_{m2}} s$$

$$A_v = A_{v0} \frac{1 - \frac{C_c}{g_{m2}} s}{1 + (R_{n1}C_{n1} + A_{v2}R_{n1}C_c + R_LC_L)s + R_{n1}R_LCCs^2}$$

$$CC = C_{n1}C_c + C_{n1}C_L + C_cC_L$$

》》 标准两级运放

$$A_v = A_{v0} \frac{1 - \frac{C_c}{g_{m2}} s}{1 + (R_{n1}C_{n1} + A_{v2}R_{n1}C_c + R_L C_L)s + R_{n1}R_L C_C s^2}$$

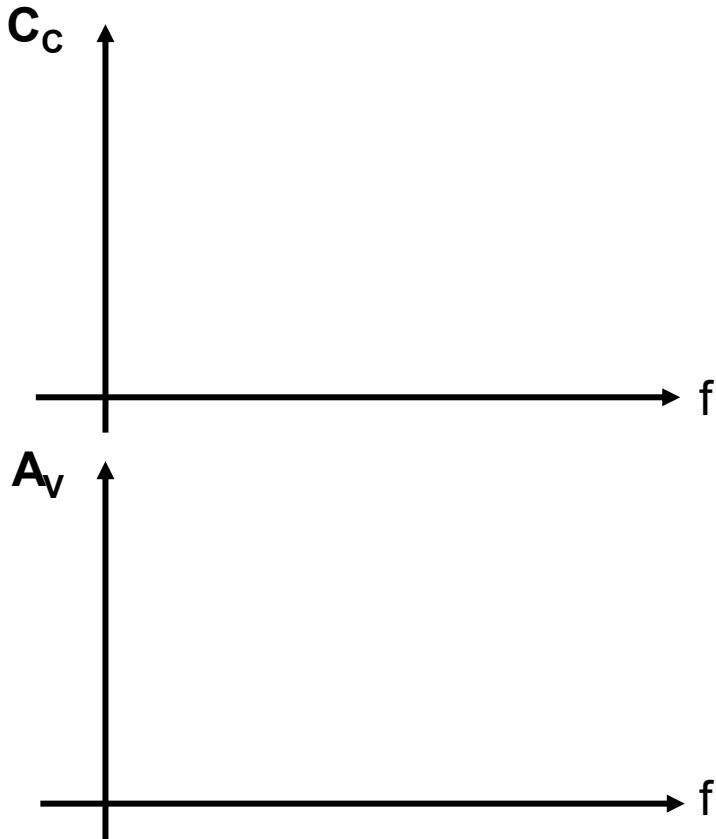
$$CC = C_{n1}C_c + C_{n1}C_L + C_cC_L$$

零点: $\frac{g_{m2}}{C_c}$

主极点: $-\frac{1}{R_{n1}C_{n1} + A_{v2}R_{n1}C_c + R_L C_L} \approx -\frac{1}{A_{v2}R_{n1}C_c}$

非主极点: $-\frac{R_{n1}C_{n1} + A_{v2}R_{n1}C_c + R_L C_L}{R_{n1}R_L C_C} \approx \frac{g_{m2}}{C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$

》》 极点分离技术：补偿电容Cc

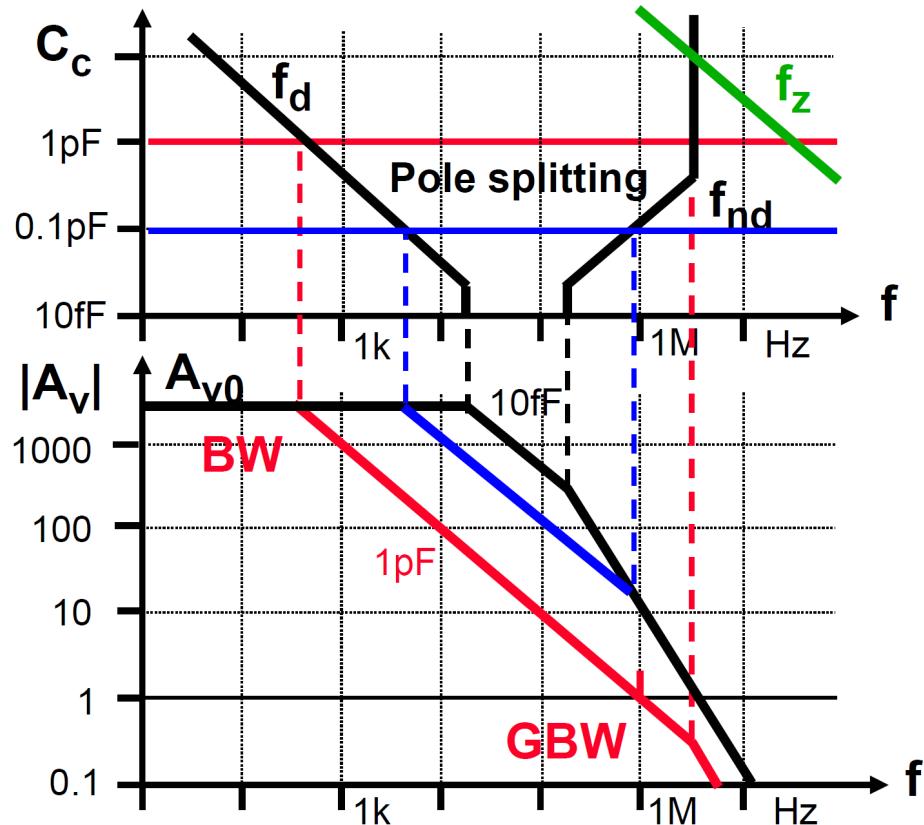


$$f_d = -\frac{1}{2\pi A_{v2} R_{n1} C_c}$$

$$f_{nd} = -\frac{g_{m2}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

$$f_z = \frac{g_{m2}}{C_c}$$

》》 极点分离技术：补偿电容Cc



$$f_d = -\frac{1}{2\pi A_{v2} R_{n1} C_c}$$

$$f_{nd} = -\frac{g_{m2}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

$$f_z = \frac{g_{m2}}{C_c}$$

»» 极点分离技术

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} = 3 GBW = \frac{g_{m2}}{2\pi C_L} \cdot \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

≈ 0.3

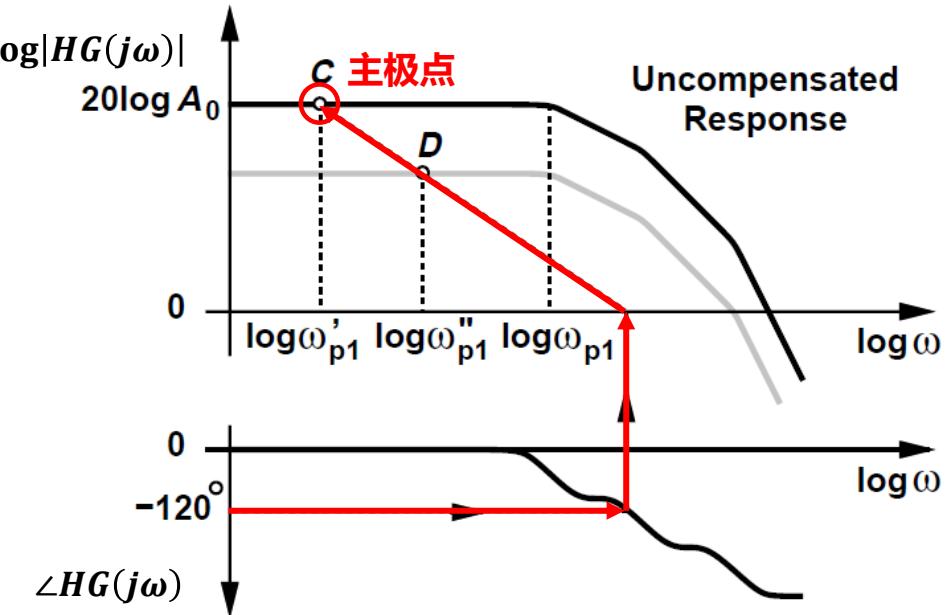
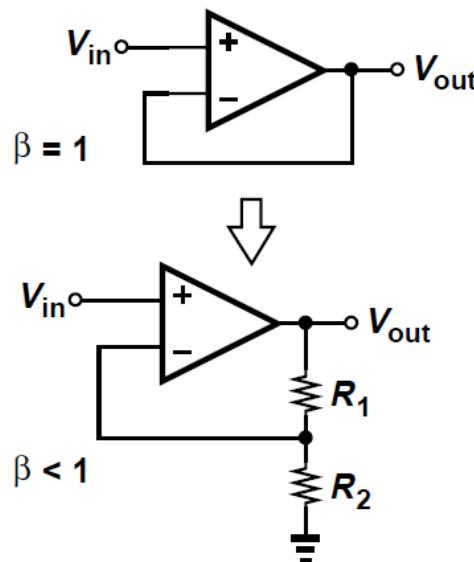
$$\frac{g_{m2}}{g_{m1}} \approx 4 \frac{C_L}{C_c}$$

Larger current in 2nd stage !

- 通常 C_c 至少是 C_{n1} 的3倍，结合 f_{nd} 需要是三倍的GBW，得到 g_{m2} 和 g_{m1} 的比值为4倍关系

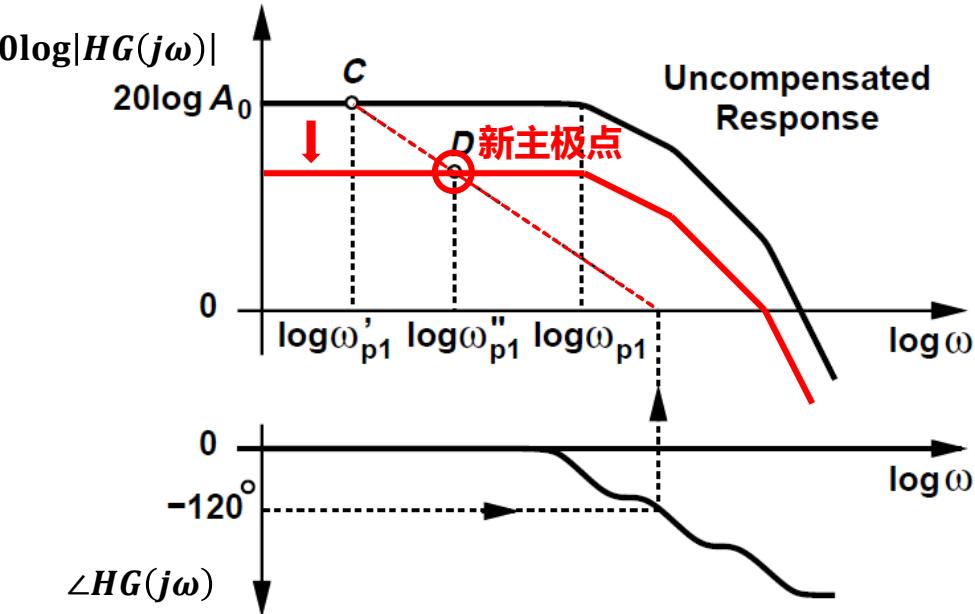
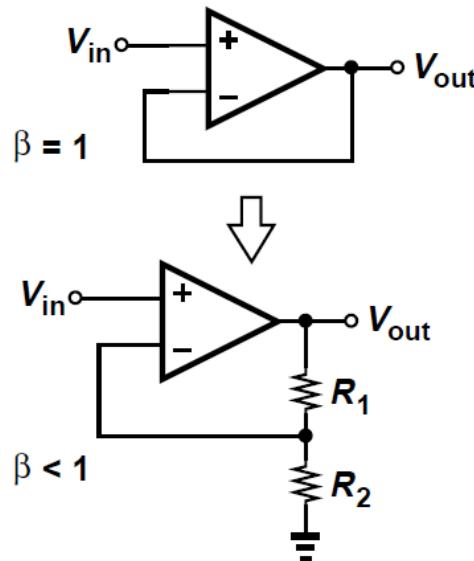
》》 极点分离技术与反馈

□ 对于一两级放大器，其单位增益反馈稳定。如果电路以 $\beta < 1$ 的反馈系数运行，那么其主极点可以放宽多少？



》》 极点分离技术与反馈

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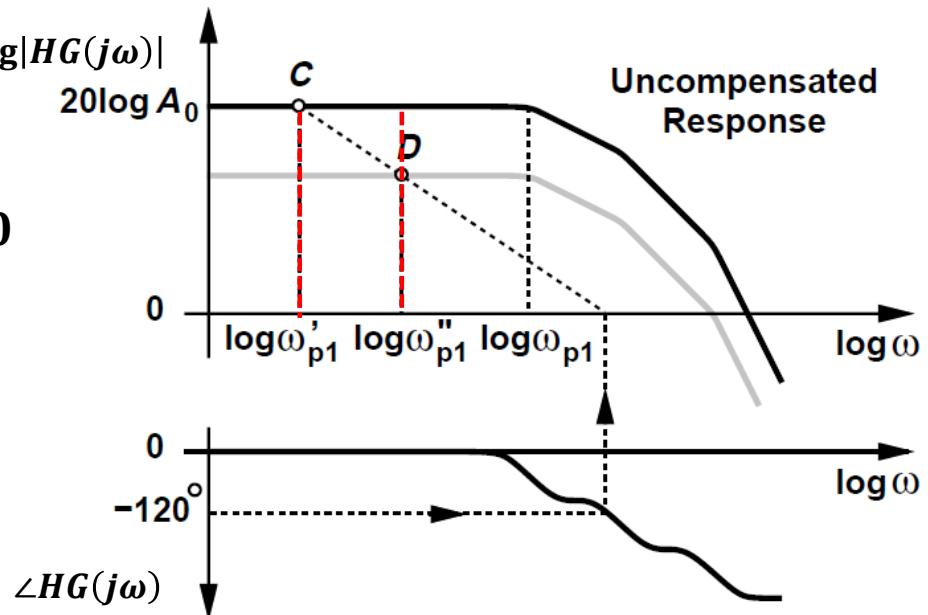
》》 极点分离技术与反馈

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$$\frac{20 \log A_0 - 20 \log(\beta A_0)}{\log \omega_{p1}'' - \log \omega_{p1}'} = 20$$



$$\frac{\omega_{p1}''}{\omega_{p1}'} = \frac{1}{\beta}$$



》》 稳定性与反馈



Low Power, 1 nV/ $\sqrt{\text{Hz}}$, $G \geq 10$ Stable, Rail-to-Rail Output Amplifier

Data Sheet

ADA4895-1/ADA4895-2

FEATURES

Low wideband noise

1 nV/ $\sqrt{\text{Hz}}$

1.6 pA/ $\sqrt{\text{Hz}}$

Low 1/f noise: 2 nV/ $\sqrt{\text{Hz}}$ at 10 Hz

Low distortion (SFDR): -96 dBc at 100 kHz, $V_{\text{OUT}} = 2 \text{ V p-p}$

Low power: 3 mA per amplifier

Low input offset voltage: 350 μV maximum

High speed

236 MHz, -3 dB bandwidth ($G = +10$)

943 V/ μs slew rate

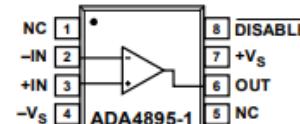
22 ns settling time to 0.1%

Rail-to-rail output

Wide supply range: 3 V to 10 V

Disable feature

FUNCTIONAL BLOCK DIAGRAMS



NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

10/08/102

Figure 1. ADA4895-1 Single Amplifier (8-Lead SOIC)

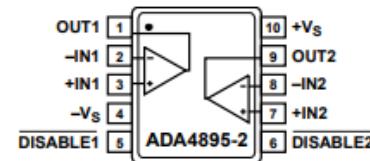
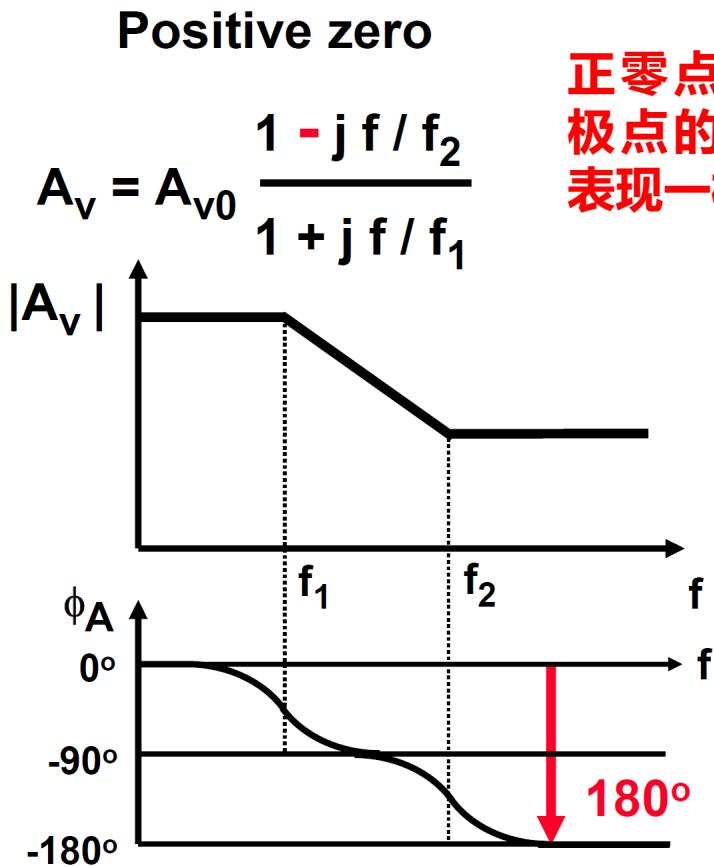
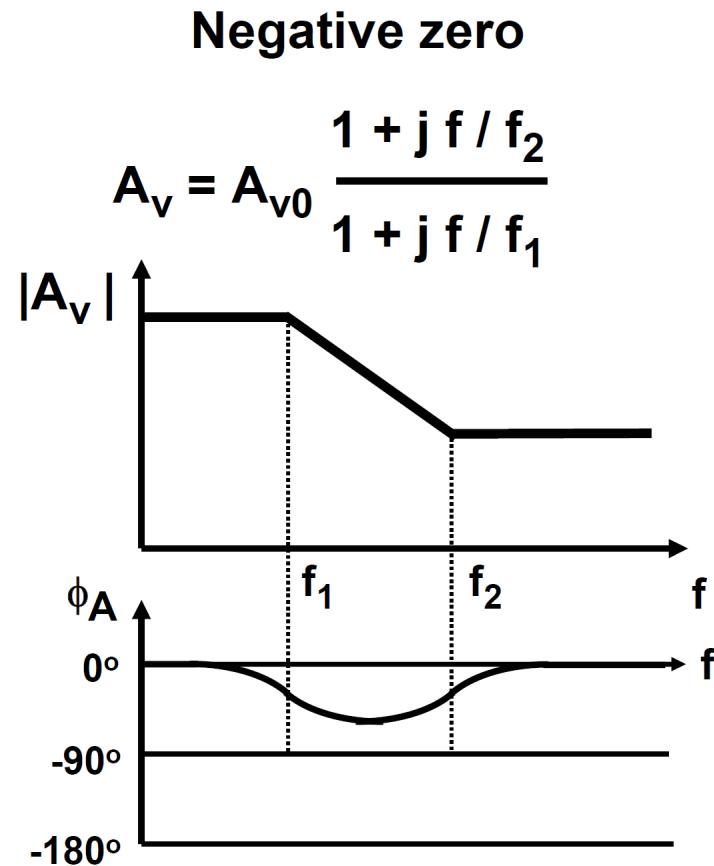


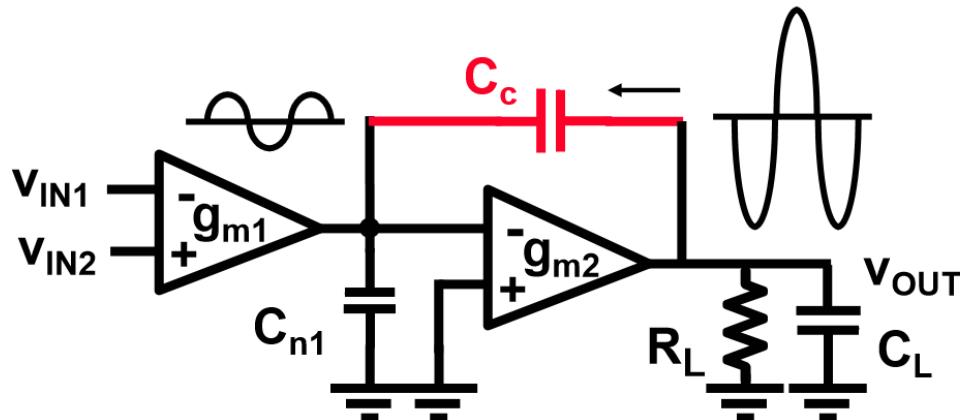
Figure 2. ADA4895-2 Dual Amplifier (10-Lead MSOP)

正零点的作用

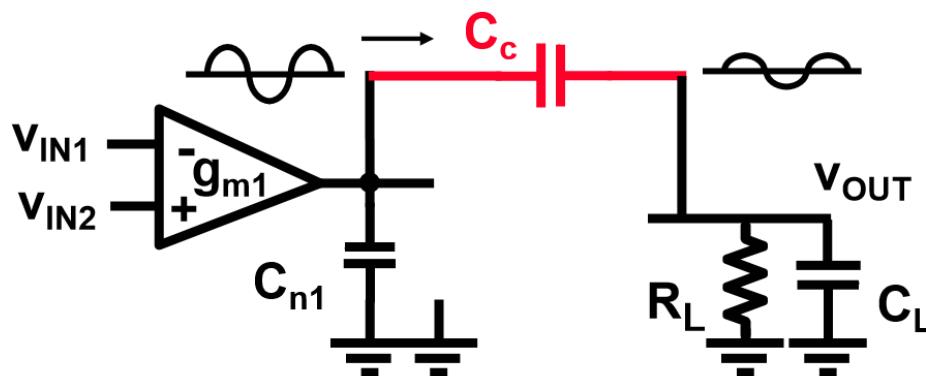


正零点和负极点的相位表现一样!

》》 正零点补偿技术



米勒效应基于运放的反馈

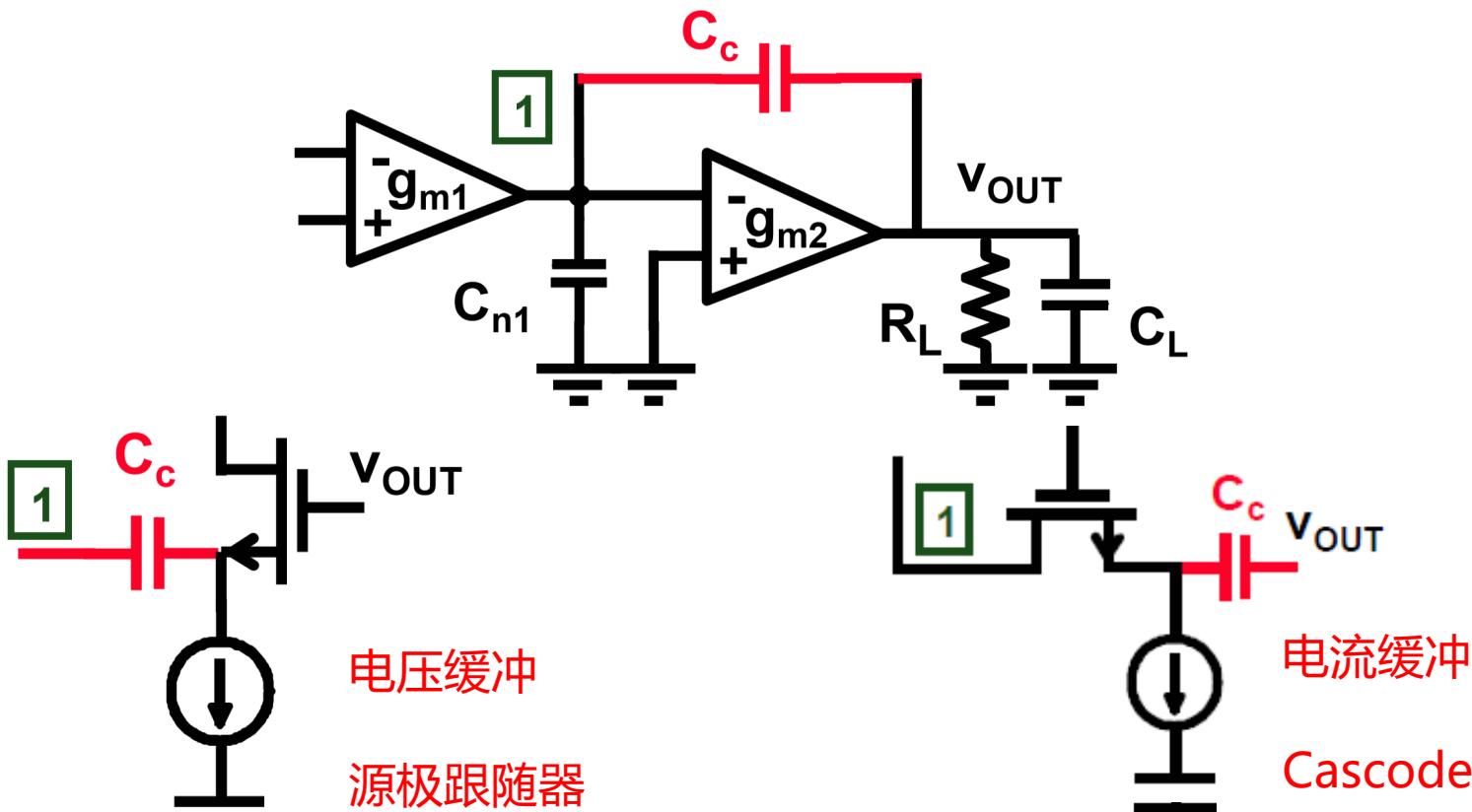


电容的前馈产生正的零点

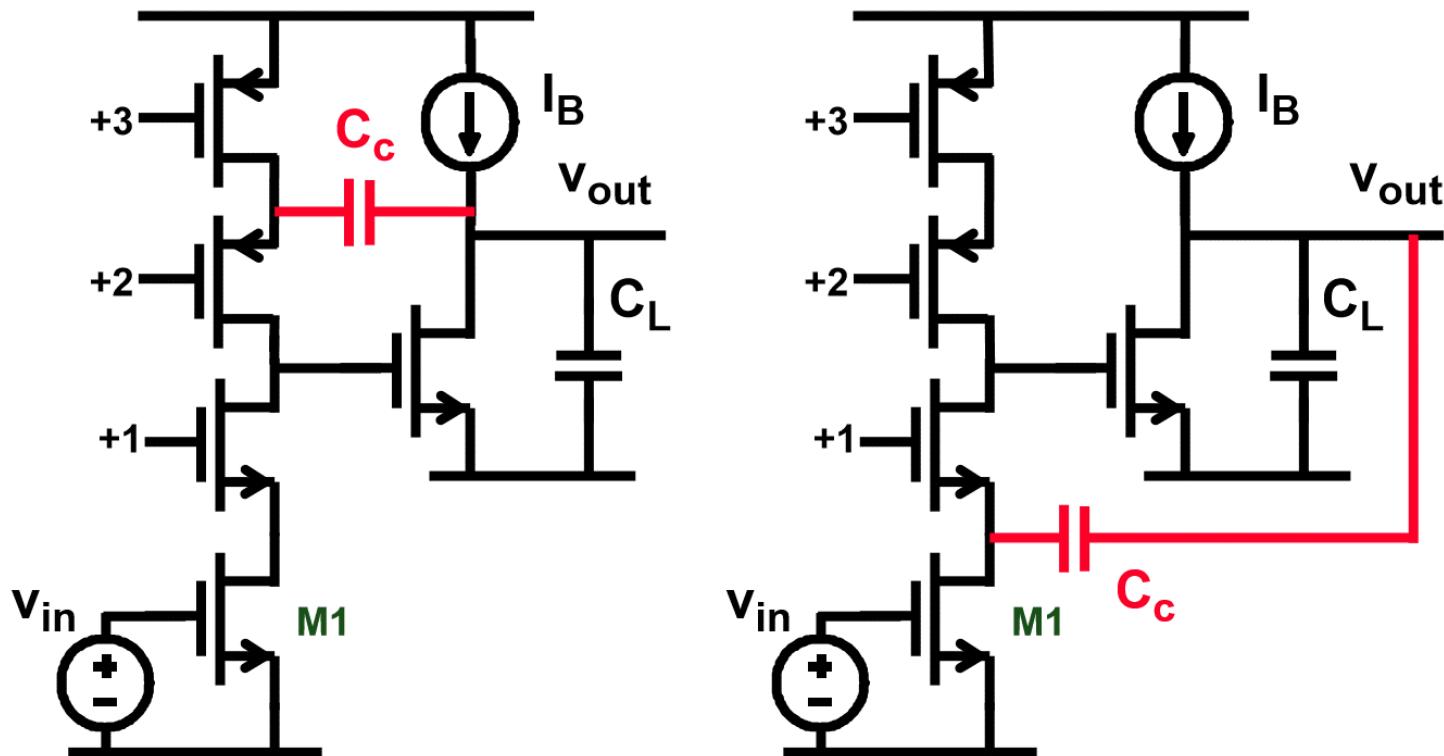
前馈的信号抵消反馈的信号

剪断前馈路径!

》》 正零点补偿技术

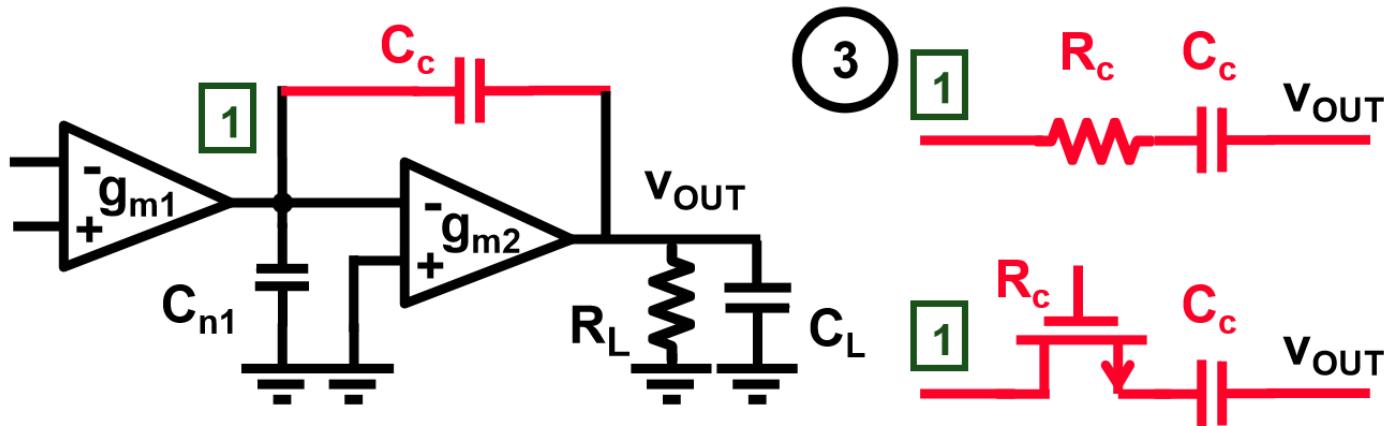


» 正零点补偿技术-Cascode

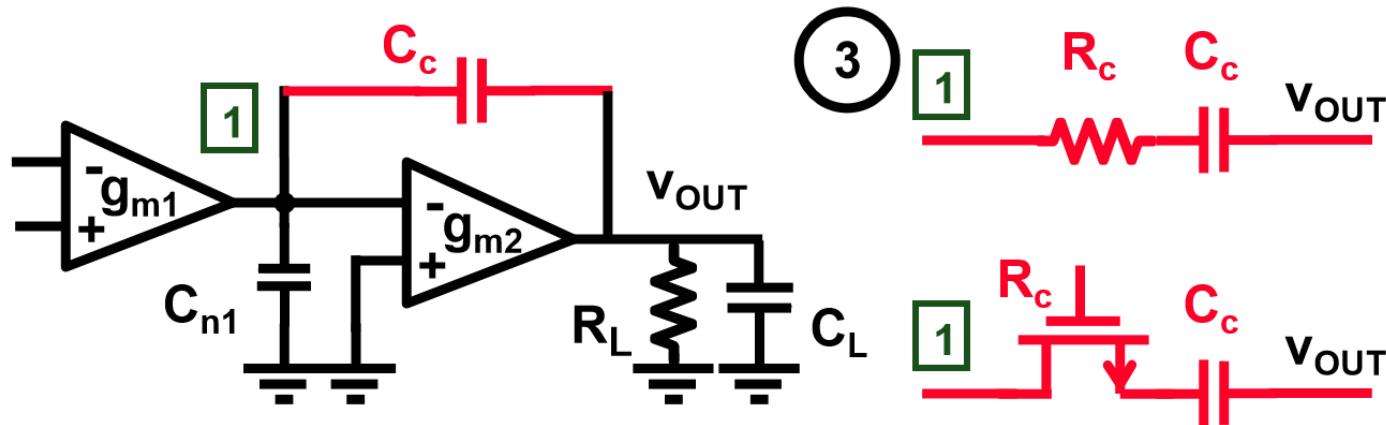


- Cascode级的使用没有额外的成本!

》》 正零点补偿技术-串联电阻



》》 正零点补偿技术-串联电阻



$$f_z = \frac{1}{2\pi C_c (1/g_{m2} - R_c)}$$

$R_c = 1/g_{m2}$ No zero

$R_c > 1/g_{m2}$ Negative zero

Ref. Senderovics, JSSC Dec 78, 760-766

» 正零点补偿技术-串联电阻

$$R_c \gg 1/g_{m2} \quad \rightarrow \quad f_z = - \frac{1}{2\pi C_c R_c}$$

$$f_z = 3 \text{ GBW} \quad \rightarrow \quad R_c = \frac{1}{3 g_{m1}}$$

Final choice :

$$\frac{1}{g_{m2}} < R_c < \frac{1}{3g_{m1}}$$

》》》 随堂练习

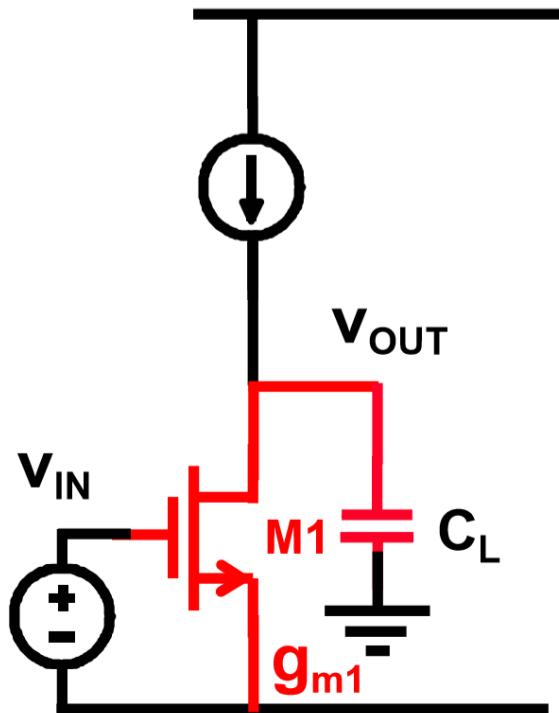
□ 已知技术指标为 $GBW=100MHz$, 负载电容 $10pF$ 。对于一个米勒补偿的两级放大器, 给出一个第一级跨导 g_{m1} , 第二级跨导 g_{m2} 和补偿电容 C_C 的组合。



运放的稳定性与系统性设计

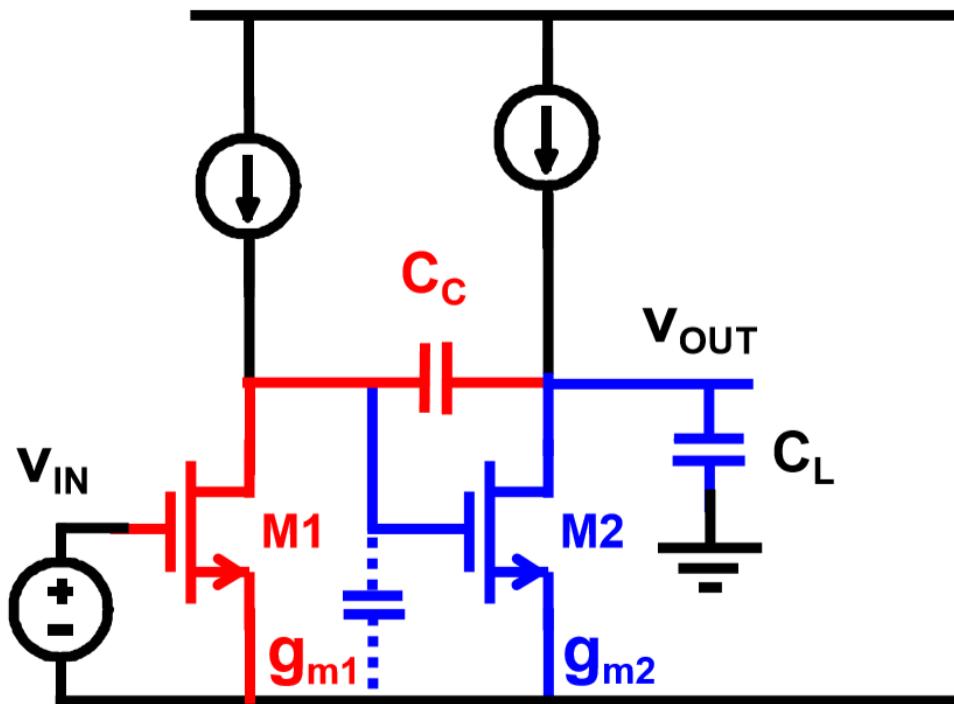
- 运放、反馈与稳定性的基本概念
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》》 三级运放的稳定性



$$GBW = \frac{g_{m1}}{2\pi C_L}$$

》》 三级运放的稳定性

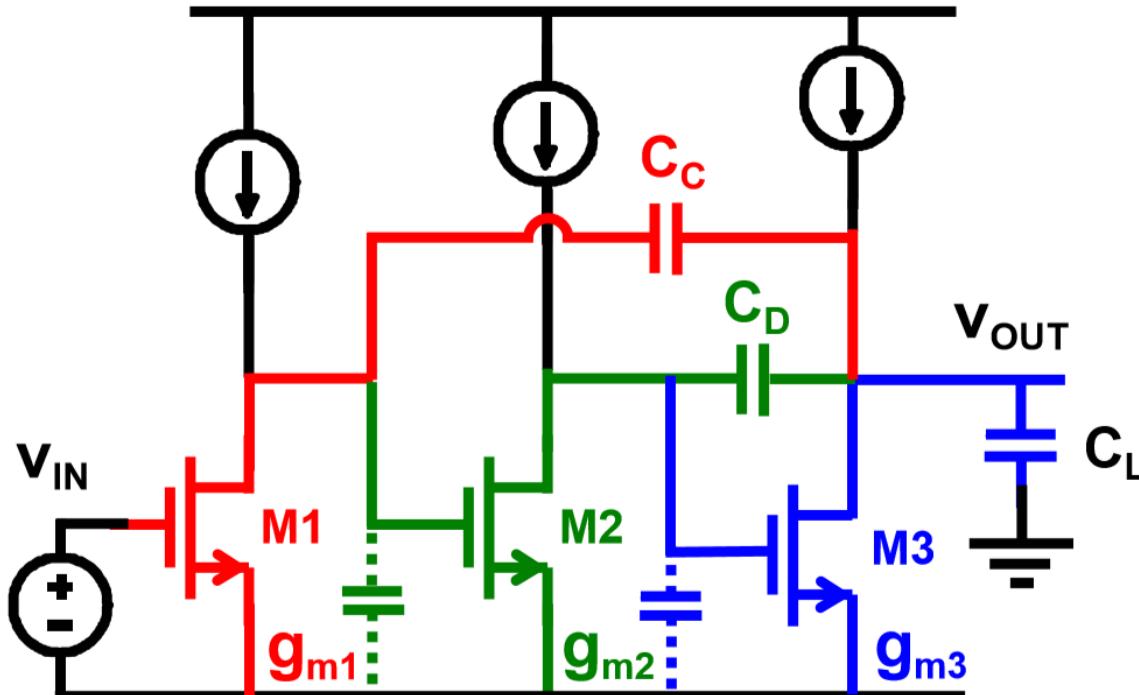


$$GBW = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd1} = \frac{g_{m2}}{2\pi C_L}$$

$$f_{nd1} = 3 GBW$$

》》 三级运放的稳定性



$$GBW = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd1} = \frac{g_{m2}}{2\pi C_D}$$

$$f_{nd2} = \frac{g_{m3}}{2\pi C_L}$$

$$f_{nd1} = 3 \text{ GBW}$$

$$f_{nd2} = 5 \text{ GBW}$$

»» 三级运放的稳定性

$$\text{GBW} = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd1} = 3 \text{ GBW} = \frac{g_{m2}}{2\pi C_D}$$

$$f_{nd2} = 5 \text{ GBW} = \frac{g_{m3}}{2\pi C_L}$$

Choose $C_D \approx C_C$!

$$\frac{g_{m2}}{g_{m1}} \approx 3$$

$$\frac{g_{m3}}{g_{m1}} \approx 5 \frac{C_L}{C_C}$$

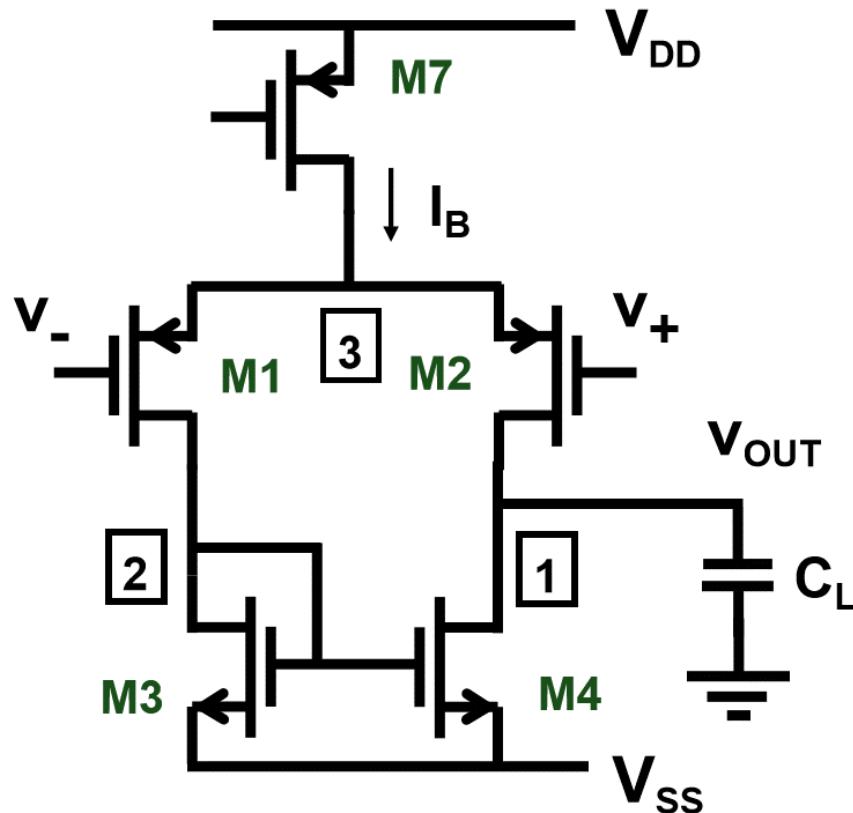
输出级更大的电流需求！



运放的稳定性与系统性设计

- 运放、反馈与稳定性的基本概念
- 极点分离与零点补偿
- 三级运放稳定性问题简介
- **运放的系统性设计方法**
- 运放的其他参数指标

》》 一级OTA的设计



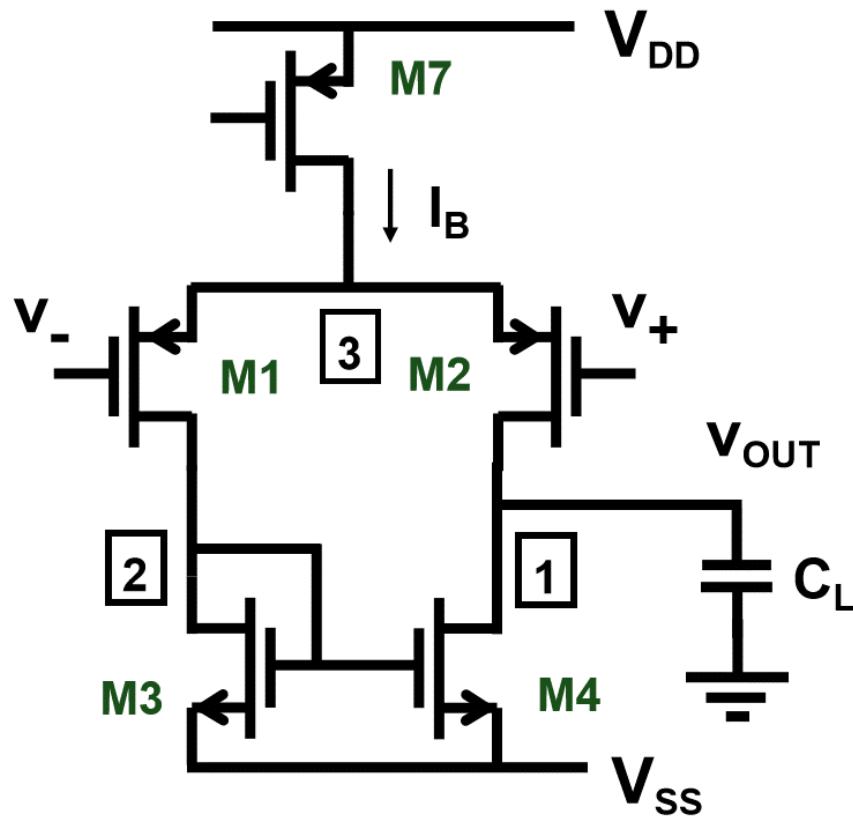
$$Av =$$

$$BW =$$

$$GBW =$$

- GBW的最大值?
- 如何衡量运放的性能?

》》 一级OTA的设计



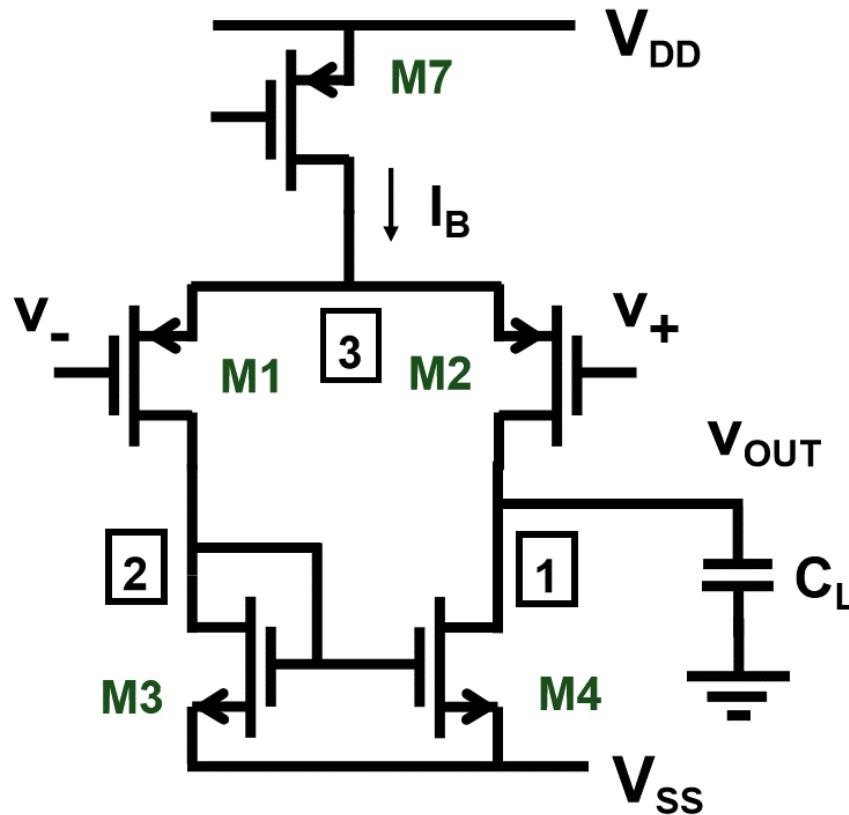
$$A_v = g_{m1} \frac{r_o}{2}$$

if $r_{o2} = r_{o4} = r_o$

$$BW = \frac{1}{2\pi \frac{r_o}{2} (C_L + C_{n1})}$$

$$GBW = \frac{g_{m1}}{2\pi (C_L + C_{n1})}$$

》》 一级OTA的设计



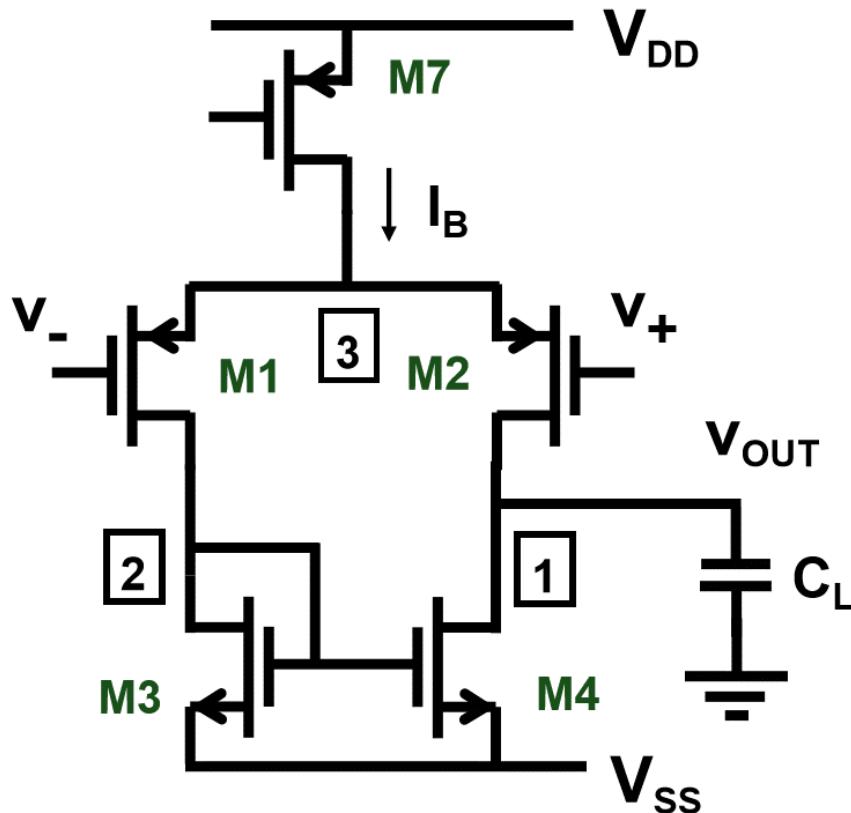
定义品质因素
Figure of Merit (FOM)

$$FOM = \frac{GBW \cdot C_L}{I_B}$$

□ 假设 $I_B=200\mu A$, $C_L=4pF$, C_{n1} 忽略不计, 求一阶OTA的FOM?

$$FOM \approx 800MHz \cdot pF/mA$$

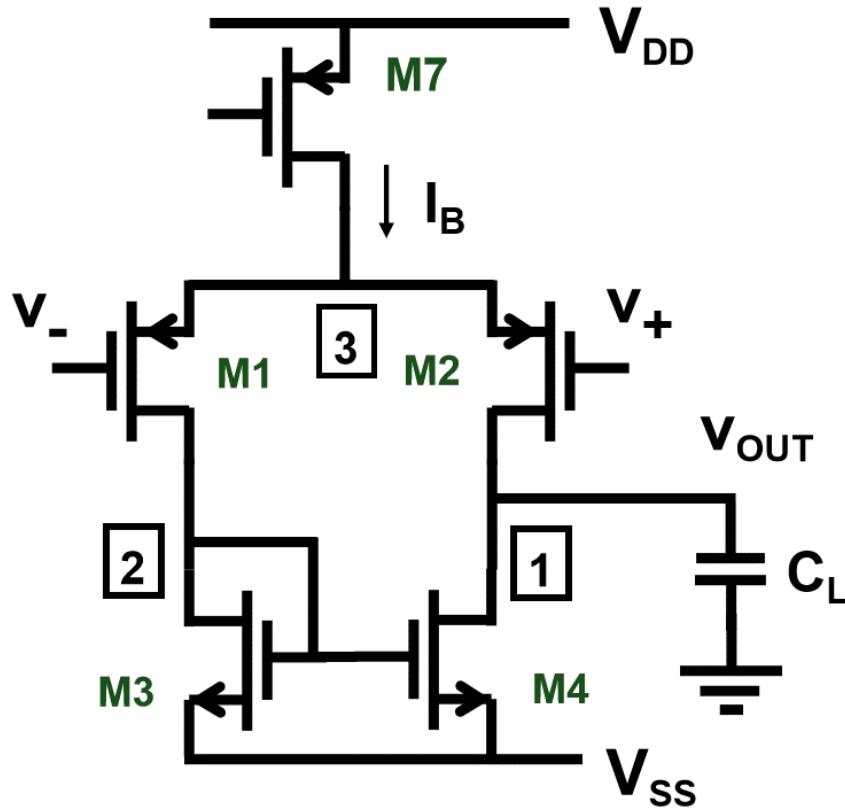
》》 一级OTA的设计： f_{nd}



$$f_{nd} =$$

- 该电路的寄生电容是否会产生非主极点？在哪里？
- 是否会使得该一阶OTA不稳定？

» 一级OTA的设计： f_{nd}



$$GBW = \frac{g_{m1}}{2\pi (C_L + C_{n1})}$$

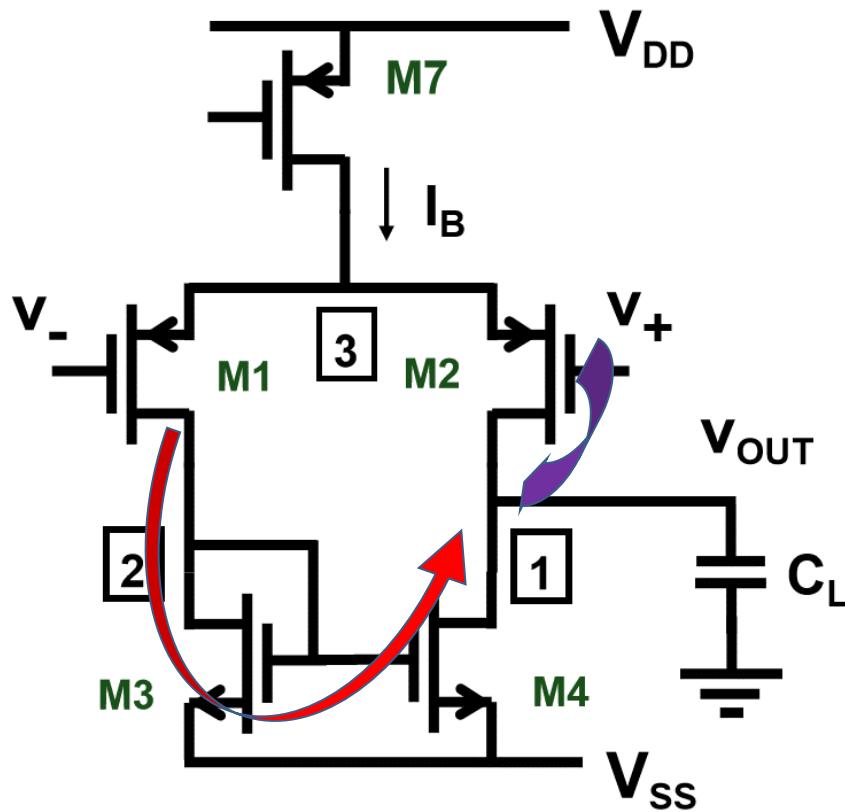
$$f_{nd} = \frac{g_{m3}}{2\pi C_{n2}}$$

$$\begin{aligned} C_{n2} &\approx 2C_{GS3} + C_{DB3} + C_{DB1} \\ &\approx 4 C_{GS3} \end{aligned}$$

$$f_{nd} \approx \frac{f_{T3}}{4}$$

✓ Net2 处非主极点
离主极点较远

» 极点-零点对 (pole-zero doublet)



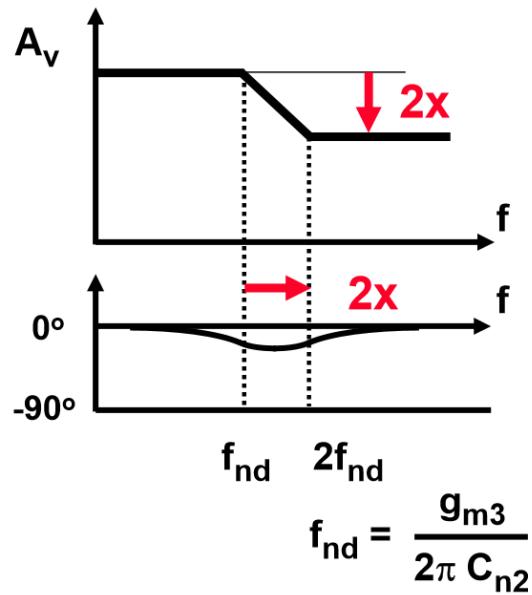
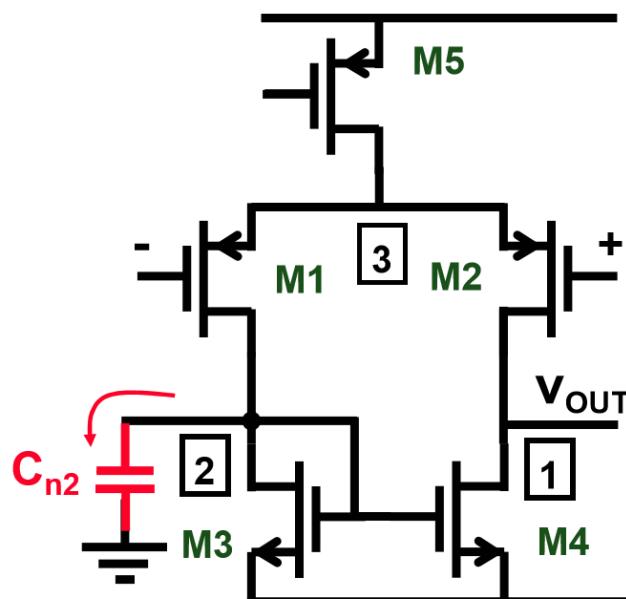
✓ Net2 的寄生电容同时会产生一个零点

$$H_f(s) = \frac{A_0}{1 + s/\omega_{p1}}$$

$$H_s(s) = \frac{A_0}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$

$$H_{f+s}(s) = \frac{A_0(2 + \frac{s}{\omega_{p2}})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$

》》 极点-零点对 (pole-zero doublet)



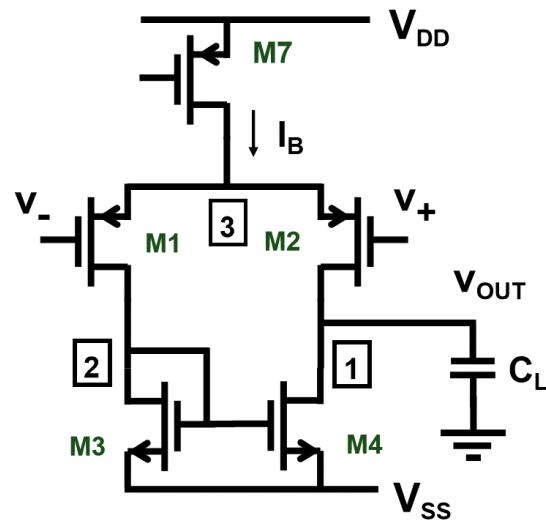
- 高频时，增益减半
- 虽然在频域上产生的作用忽略不计，但是在时域上会对稳定时间产生较大影响

$$PM = 90^\circ - \arctan \frac{GBW}{f_{nd}} + \arctan \frac{GBW}{2f_{nd}} \approx 85^\circ$$

》》 一级OTA的设计

按要求设计OTA中晶体管尺寸。要求 $GBW=100MHz$, $C_L=2pF$ 。

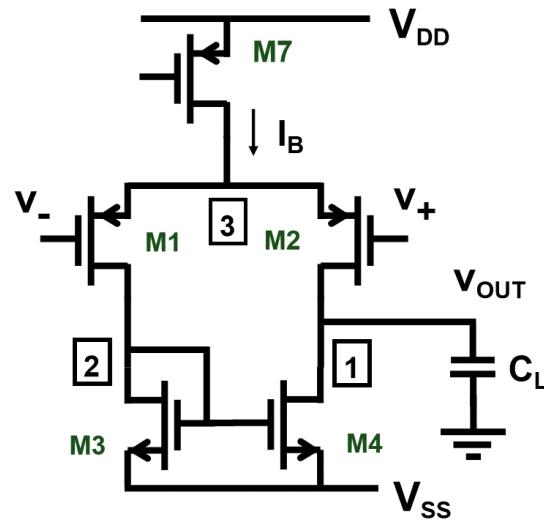
已知工艺参数为: $L_{min}=0.18\mu m$, $KP_n' = 280\mu A/V^2$, $KP_p' = 70\mu A/V^2$



》》 一级OTA的设计

按要求设计OTA中晶体管尺寸。要求 $GBW=100MHz$, $C_L=2pF$ 。

已知工艺参数为: $L_{min}=0.18\mu m$, $KP_n' = 280\mu A/V^2$, $KP_p' = 70\mu A/V^2$



$$g_m = GBW \cdot 2\pi C_L = 1.256mA/V$$

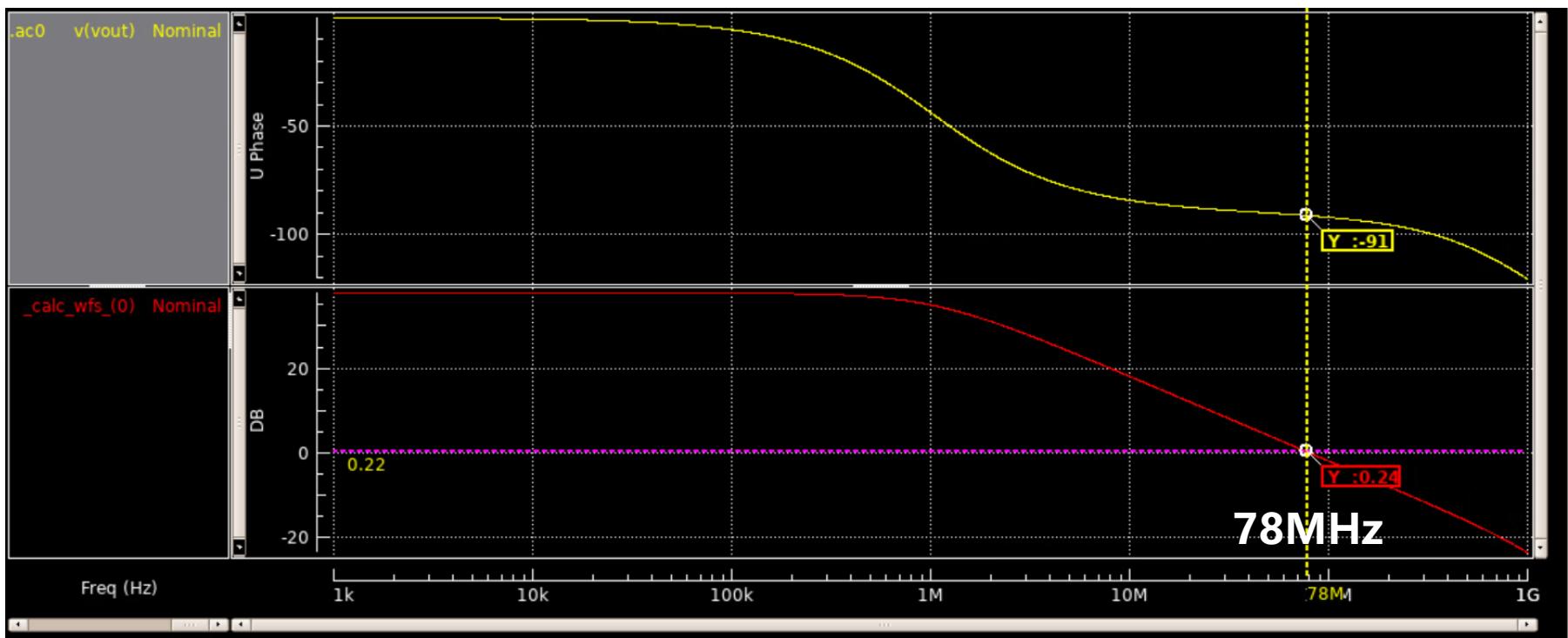
$$I_D = \frac{g_m}{10} = 125.6\mu A/V \quad I_B = 251.2\mu A/V$$

$$\left(\frac{W}{L}\right)_p \approx 80 \quad \left(\frac{W}{L}\right)_n \approx 20$$

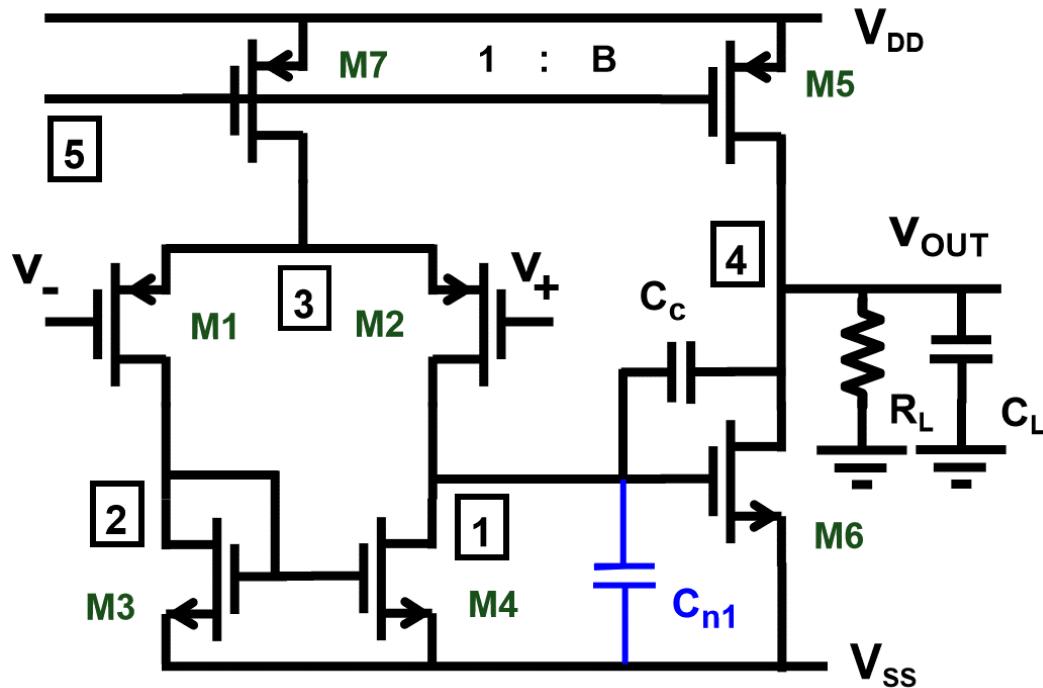
$$\left(\frac{W}{L}\right)_p = \frac{40}{500n} \quad \left(\frac{W}{L}\right)_n = \frac{10}{500n}$$

》》 一级OTA的设计

□ 仿真结果



》》 二级OTA的设计



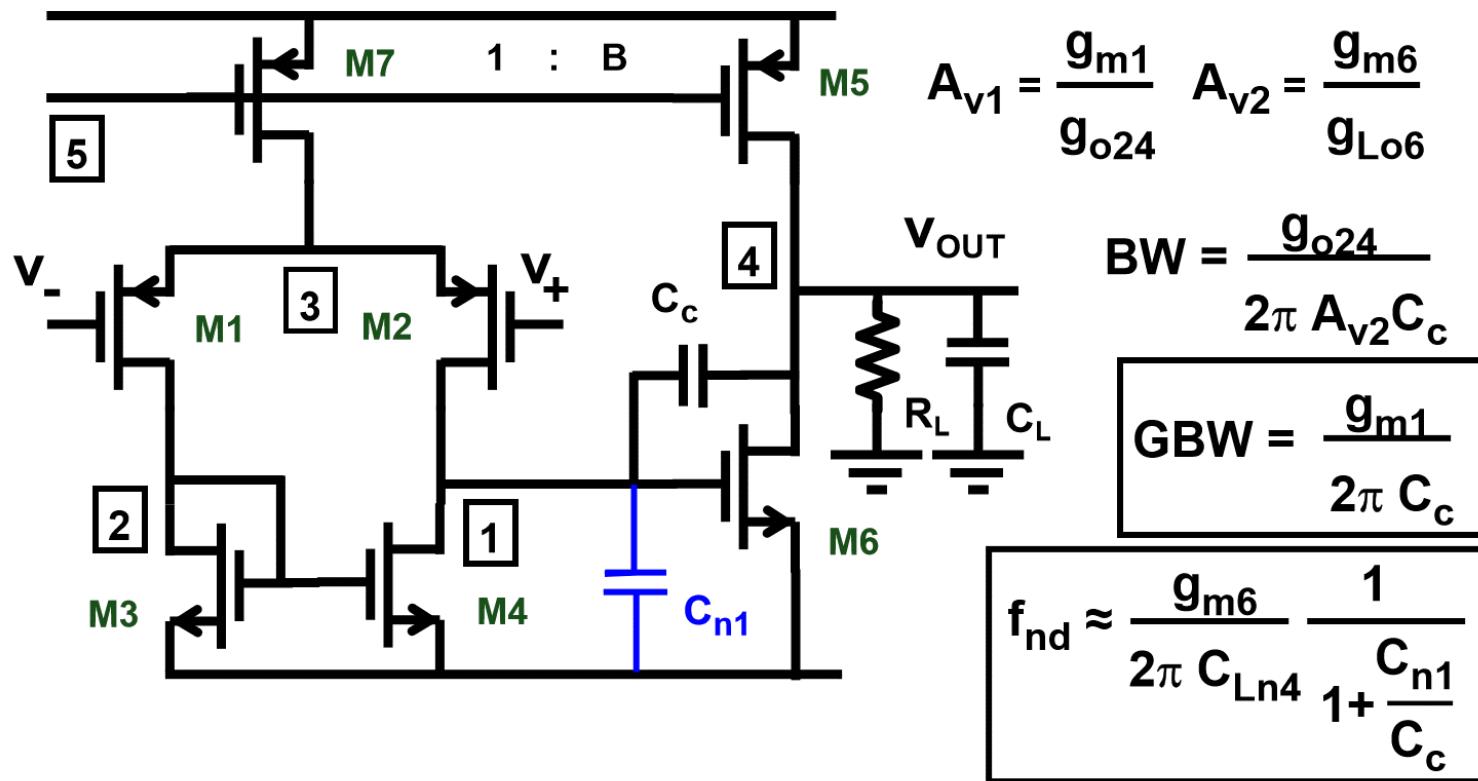
$$Av =$$

$$BW =$$

$$GBW =$$

□ 二阶体现在哪两个点上?

》》 二级OTA的设计



»» 如何设计优化GBW和PM

- 如何在一定的功耗下，获得最优的GBW？
- 已有两个公式，分别定义GBW和PM：

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

- 已有三个设计变量：

$$g_{m1}, \quad g_{m6}, \quad C_c$$

如何找到最优的解？

》》 如何设计优化GBW和PM

$$GBW = \frac{g_{m1}}{2\pi C_C} \quad f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

1. 先选择 g_{m1} , 根据公式解出 g_{m6} 和 C_C
2. 先选择 g_{m6} , 根据公式解出 g_{m1} 和 C_C
3. 先选择 C_C , 根据公式解出 g_{m1} 和 g_{m6}

C_C 受一定的选择范围限制:

1. 通常大于 $3 \times C_{n1}$
2. 通常小于 $C_L/2$

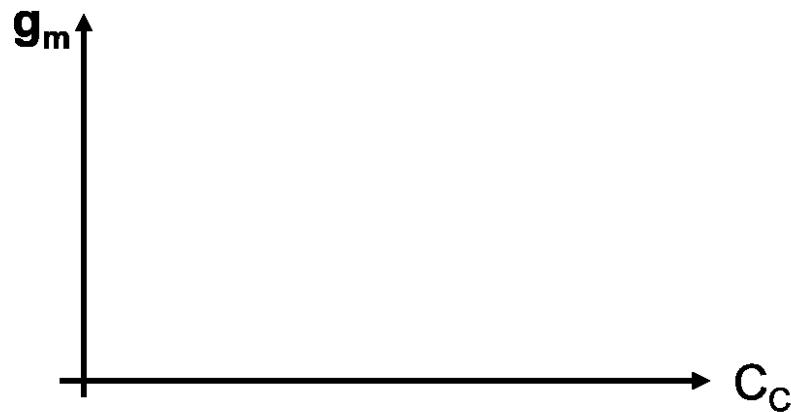
》》通过C_C设计优化GBW和PM

□ 要求GBW=1MHz, C_L=10pF。

$$GBW = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

假设C_{n1}恒定

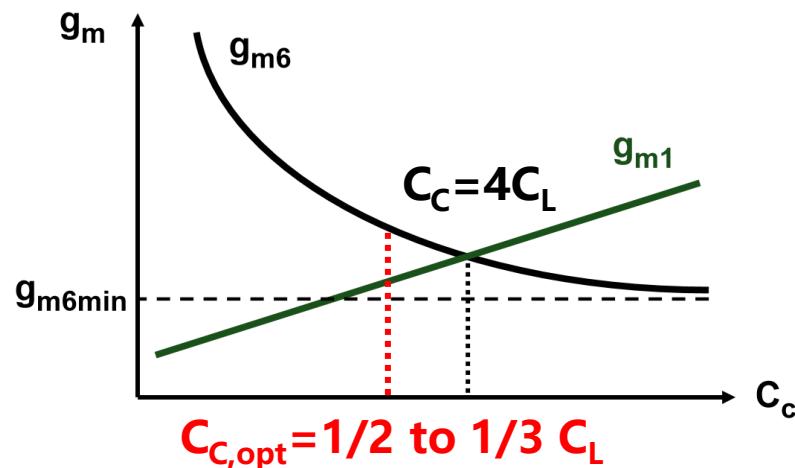


通过 C_C 设计优化GBW和PM

□ 要求 $GBW = 1\text{MHz}$, $C_L = 10\text{pF}$ 。

$$GBW = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$



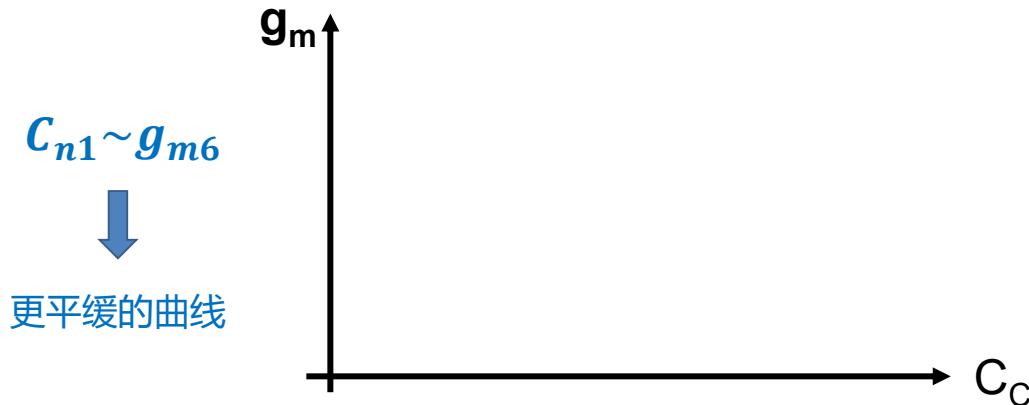
通过C_C设计优化GBW和PM

□ 要求GBW=1MHz, C_L=10pF。

$$GBW = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

假设C_{n1}变化

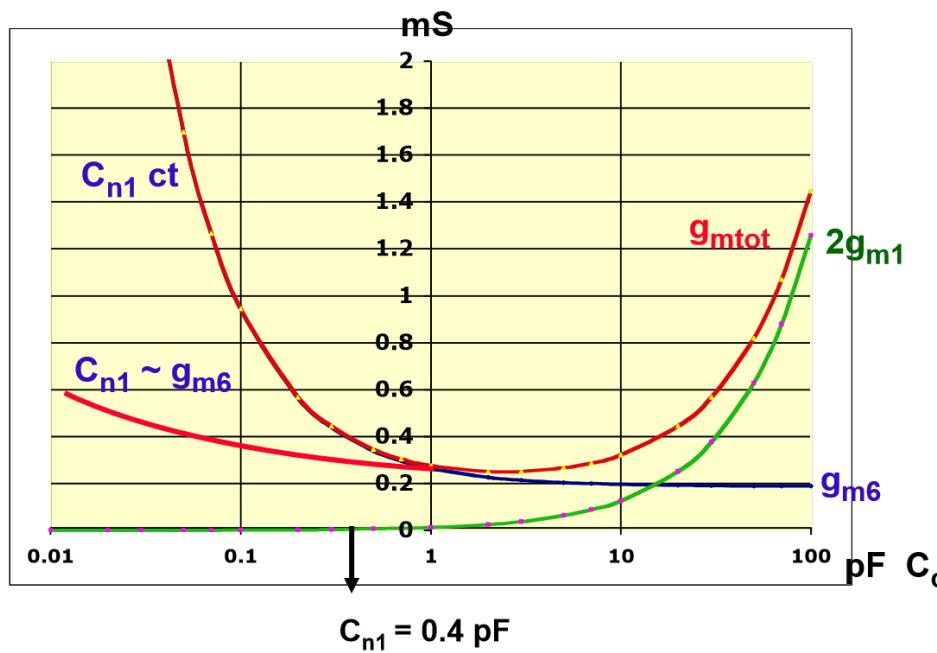


通过C_c设计优化GBW和PM

□ 要求GBW=1MHz, C_L=10pF。

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$



GBW = 1 MHz

C_L = 10 pF

C_{n1} = 0.4 pF

K' = 20 μ A/V²

V_{GS}-V_T = 0.2 V

L = 10 μ m

》》如何设计优化GBW和PM

$$GBW = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

1. 先选择 g_{m1} , 根据公式解出 g_{m6} 和 C_C
2. 先选择 g_{m6} , 根据公式解出 g_{m1} 和 C_C
3. 先选择 C_C , 根据公式解出 g_{m1} 和 g_{m6}

通过 g_{m6} 设计优化GBW和PM

□ 要求 $GBW=1\text{MHz}$, $C_L=10\text{pF}$ 。

$$GBW = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

假设 C_{n1} 恒定



通过 g_{m6} 设计优化GBW和PM

□ 要求GBW=1MHz, $C_L=10\text{pF}$ 。

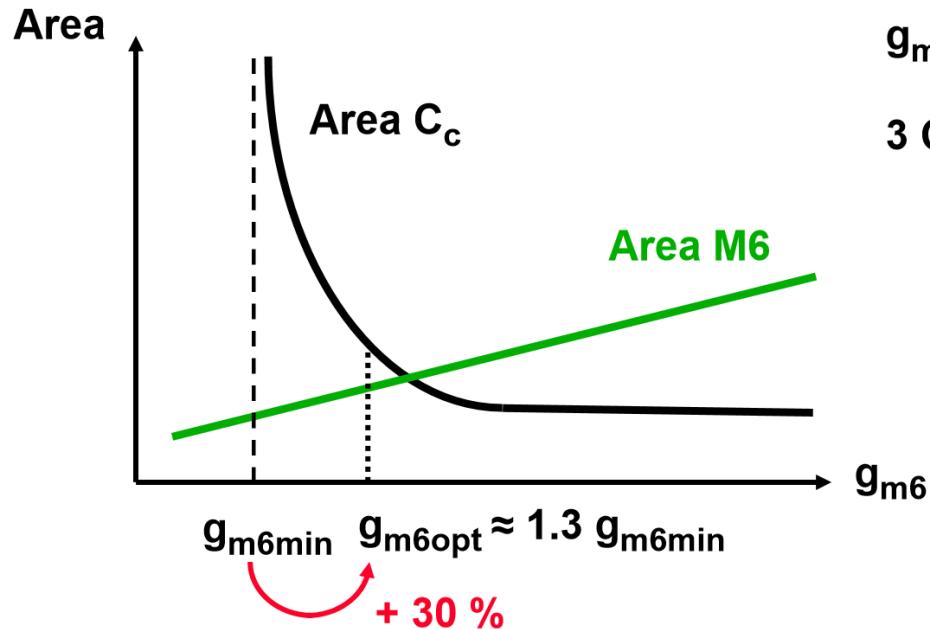
$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

假设 C_{n1} 恒定

$$g_{m6min} =$$

$$3 \text{ GBW} (2\pi C_L)$$



》》 如何设计优化GBW和PM

$$GBW = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

1. 先选择 g_{m1} , 根据公式解出 g_{m6} 和 C_C
2. 先选择 g_{m6} , 根据公式解出 g_{m1} 和 C_C
3. 先选择 C_C , 根据公式解出 g_{m1} 和 g_{m6}

➤对噪声有要求时, 通常先计算 g_{m1}

通过 g_{m1} 设计优化GBW和PM

□ 要求 $GBW=1\text{MHz}$, $C_L=10\text{pF}$ 。

$$GBW = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

假设 C_{n1} 恒定

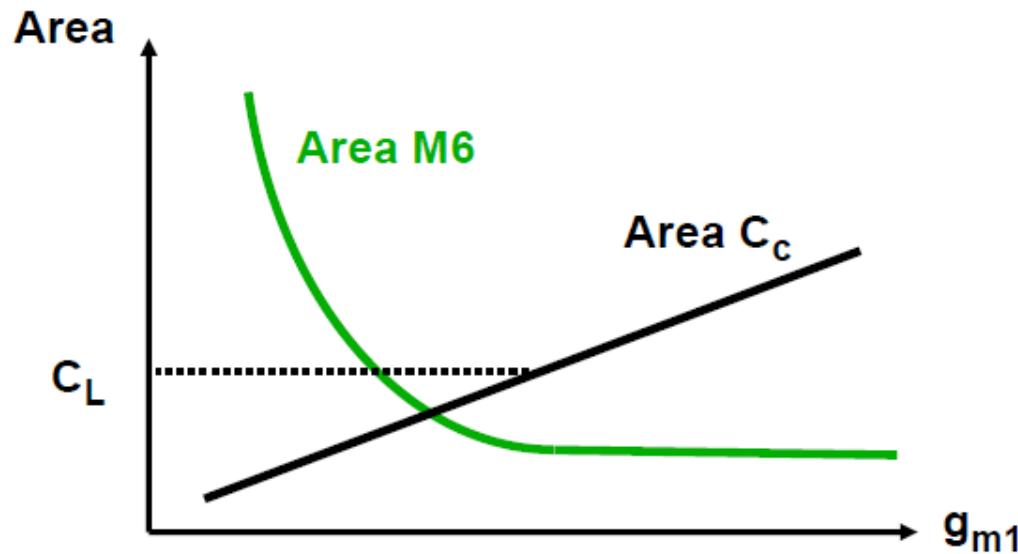


通过 g_{m1} 设计优化GBW和PM

□ 要求GBW=1MHz, $C_L=10\text{pF}$ 。

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}} \text{ 假设 } C_{n1} \text{ 恒定}$$



»» 高速米勒OTA设计

$$\text{GBW} = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + C_{n1}/C_c}$$

$$\text{GBW} = \frac{f_{T6}}{\alpha \beta \gamma (1 + 1/\beta)}$$

$$C_L = \alpha C_c$$

$$C_c = \beta C_{n1} = \beta C_{GS6}$$

$$f_{nd} = \gamma \text{GBW}$$

首先判断某个工艺是否满足指标要求 → 最小长度下的带宽

- GBW不取决于 C_L , 而是取决于输出级晶体管的特征频率

》》 高速米勒OTA设计

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$C_L = \alpha C_c \quad \alpha \approx 2$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + C_{n1}/C_c}$$

$$C_c = \beta C_{n1} = \beta C_{GS6} \quad \beta \approx 3$$

$$f_{nd} = \gamma GBW \quad \gamma \approx 2$$

$$C_{GS} = kW \quad k = 2fF/\mu m, \text{ for minL}$$

$$GBW = \frac{f_{nd}}{\gamma} = \frac{g_{m6}}{2\pi C_L} \frac{1}{\gamma (1 + 1/\beta)}$$

g_{m6}的表达式?

$$C_L = \alpha C_c = \alpha \beta C_{n1} = \alpha \beta C_{GS6} = \alpha \beta kW_6$$

$W_6 \uparrow$ if $C_L \uparrow$

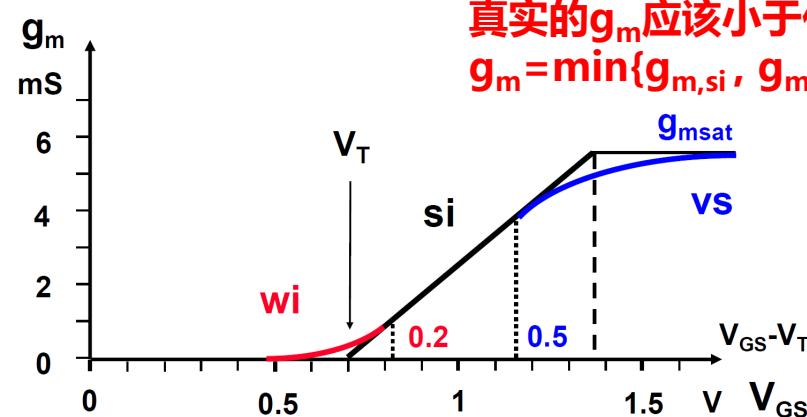
》》》 高速米勒OTA设计

强反型区(Strong Inversion)

$$g_{m,si} \approx \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

速度饱和区(Velocity Saturation)

$$g_{m,sat} = W C_{OX} v_{sat}$$



$$\frac{1}{g_m} = \frac{1}{g_{m,si}} + \frac{1}{g_{m,sat}}$$

当取最小长度时

$$g_m \approx \frac{W}{L} \frac{17 \cdot 10^{-5}}{1 + 2.8 \cdot 10^4 L / V_{GST}}$$

L in cm

»» 高速米勒OTA设计

消除 C_L :

$$GBW = \underbrace{\frac{g_{m6}}{2\pi kW_6}}_{f_{T6}} \frac{1}{\alpha \beta \gamma (1 + 1/\beta)}$$

$$g_m = \frac{W}{L} \frac{17 \cdot 10^{-5}}{1 + 2.8 \cdot 10^4 L / V_{GST}}$$

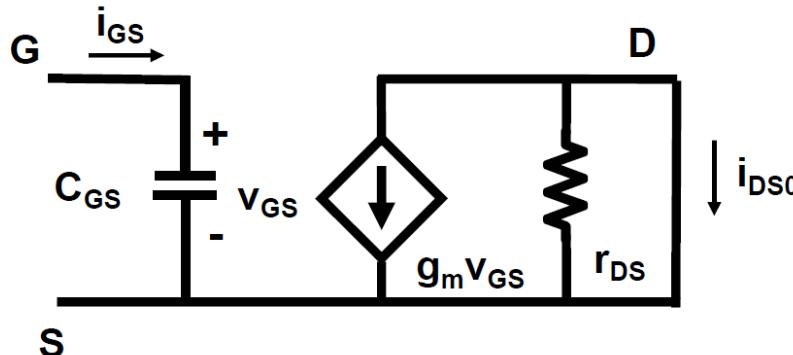
W, L in cm

$$GBW = \frac{1}{2\pi L_6} \frac{1}{\alpha \beta \gamma (1 + 1/\beta)} \frac{8.5 \cdot 10^6}{1 + 2.8 \cdot 10^4 L_6 / V_{GST6}}$$

L in cm

- GBW不取决于 C_L , 而是取决于输出级晶体管的特征尺寸和偏置

》》 特征频率 f_T , $i_{DS} = i_{GS}$



$$i_{GS} = v_{GS} C_{GS} s$$

$$i_{DS} = g_m v_{GS}$$

$$C_{GS} = \frac{2}{3} WLC_{ox} \quad g_m = 2K' \frac{W}{L} (V_{GS} - V_T) \quad K' = \frac{\mu C_{ox}}{2n}$$

$$f_T = \frac{g_m}{2\pi C_{GS}} = \frac{1}{2\pi} \frac{3}{2n} \frac{\mu}{L^2} (V_{GS} - V_T)$$

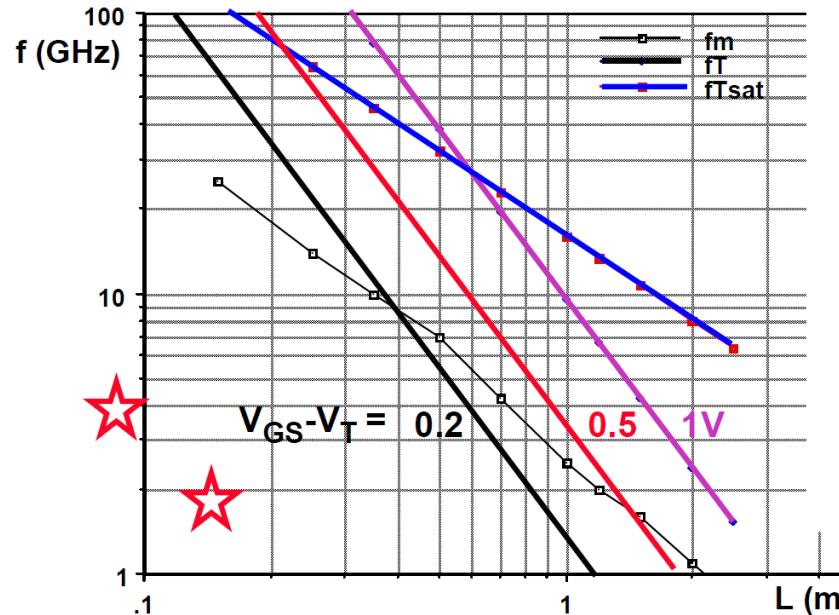
↑
反型区

or

$$\approx \frac{v_{sat}}{2\pi L}$$

↑
速度饱和区

》》》 高速米勒OTA设计



$$V_{GS} - V_T \approx 0.2 \text{ V}$$

$$\alpha \approx 2$$

$$\beta \approx 3$$

$$\gamma \approx 2$$

or 16 x

$$\text{GBW} \approx \frac{f_{T6}}{16}$$

- GBW通常只有 f_T 的1/16
- 如果我们需要5G的GBW，那么需要80G的 f_T ，该指标在0.2V的 V_{GST} 时需要0.1m工艺，而在0.5V的 V_{GST} 时只需要0.2um工艺



高速米勒OTA设计

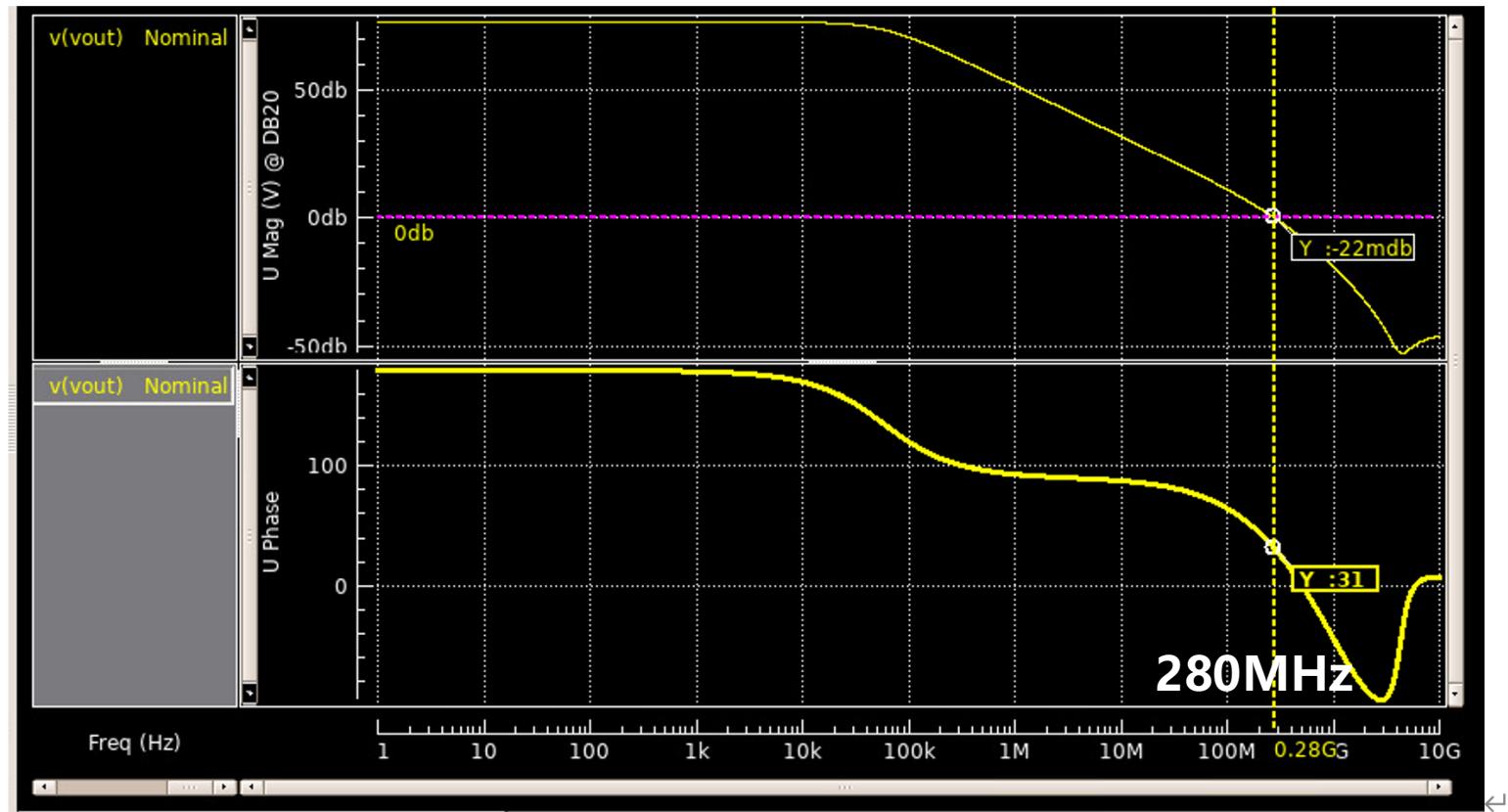
1. 选择 $\alpha \beta \gamma$
2. 找到满足GBW最小的 f_T
3. 选择一定 $V_{GS6}-V_T$ 下最大的 L_6
4. 根据 C_L 计算 W_6 和偏置电流 I_{DS6}
5. 通过选择的 α 和 C_L 计算 C_C
6. 通过 C_C 计算 g_{m1} 和 I_{DS1}
7. 噪声表现由 g_{m1} 和 C_C 决定

》》》 高速米勒OTA设计

□ 要求GBW=400MHz, $C_L=5\text{pF}$ 。

1. 选择 $\alpha \beta \gamma$
 - 2 3 2
2. 找到满足GBW最小的 f_T
 - $f_T=6.4\text{GHz}$
3. 选择一定 $V_{GS6}-V_T$ 下最大的 L_6
 - $V_{GST6}=0.2\text{V}, u=33\text{m}$
4. 根据 C_L 计算 W_6 和偏置电流 I_{DS6}
 - $K_n' = 280\mu\text{A/V}^2$
 - $W_6=220\text{um}, I_{DS6}=2.5\text{mA}$
5. 通过选择的 α 和 C_L 计算 C_C
 - $C_C=2.5\text{pF}$
6. 通过 C_C 计算 g_{m1} 和 I_{DS1}
 - $g_{m1}=6.28\text{mS}, I_{DS1}=0.63\text{mA}$
7. 噪声表现由 g_{m1} 和 C_C 决定

》》》 高速米勒OTA设计



》》低功耗米勒OTA设计

高速设计步骤：

1. 选择 $\alpha \beta \gamma$
2. 找到满足GBW最小的 f_T
3. 选择一定 $V_{GS6}-V_T$ 下最大的 L_6
4. 根据 C_L 计算 W_6 和偏置电流 I_{DS6}
5. 通过选择的 α 和 C_L 计算 C_C
6. 通过 C_C 计算 g_{m1} 和 I_{DS1}
7. 噪声表现由 g_{m1} 和 C_C 决定

低功耗设计步骤：

1.
$$f_T = \frac{2\mu kT/q}{2\pi L^2} \cdot \sqrt{i(1 - e^{\sqrt{i}})}$$
2. **尺寸设计** **偏置设计**
3. 根据情况选择反型系数 i
4. 根据 C_L 和 L_6 计算 W_6
5. 根据 I_{DST6} 和 反型系数 i 计算 I_{DS6}
- 6.
- 7.

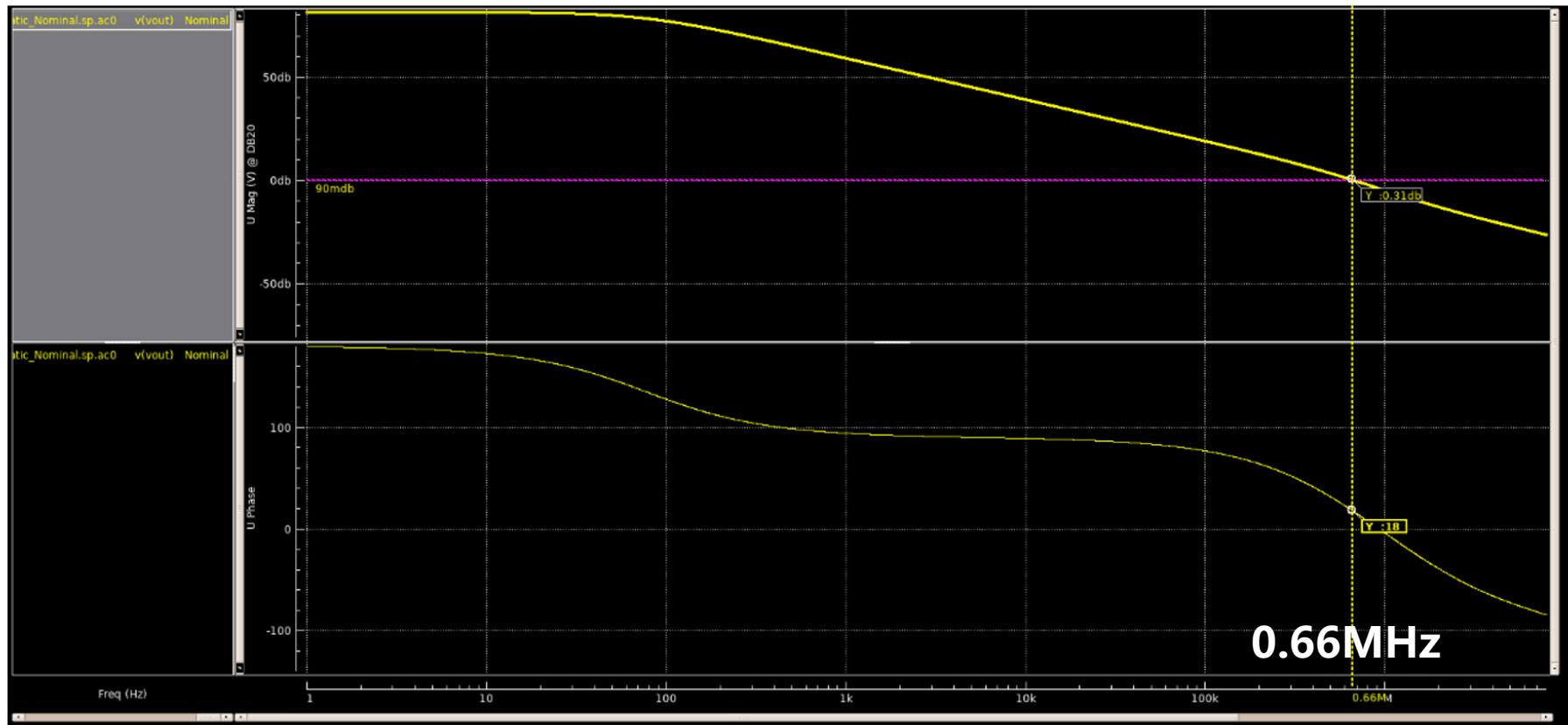


低功耗米勒OTA设计

□ 要求GBW=1MHz, $C_L=5\text{pF}$ 。

1. 选择 $\alpha \beta \gamma$
 - 2 3 2
2. 找到满足GBW最小的 f_T
 - $f_T=16\text{MHz}$
3. 根据增益要求选择 L_6
 - 得到 f_{TH6} $f_{TH6}=6.4\text{GHz}, i=2.5\text{m}$
4. 根据 C_L 和 L_6 计算 W_6
 - $W_6=220\text{um}$
5. 根据 I_{DST6} 和反型系数*i*计算 I_{DS6}
 - $I_{DST6}=0.31\text{mA}$
 - $I_{DS6}=0.8\mu\text{A}$
6. 通过选择的 α 和 C_L 计算 C_C
 - $C_C=2.5\text{pF}$
7. 通过 C_C 计算 g_{m1} 和 I_{DS1}
 - $I_{DS1}=0.6\mu\text{A}$

》》低功耗米勒OTA设计





运放的稳定性与系统性设计

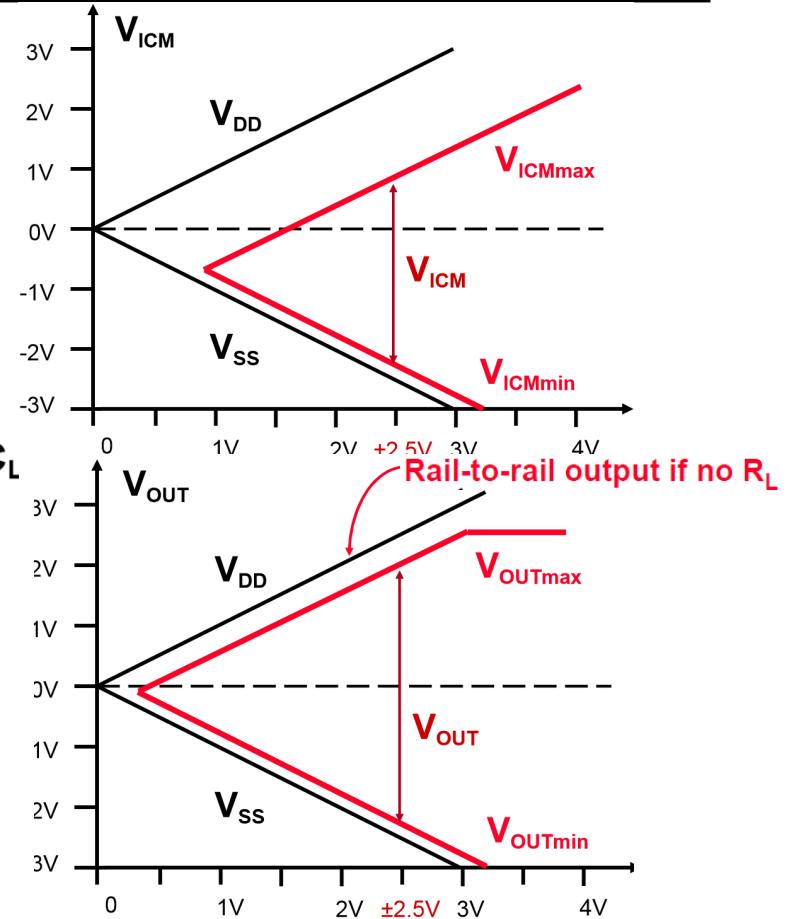
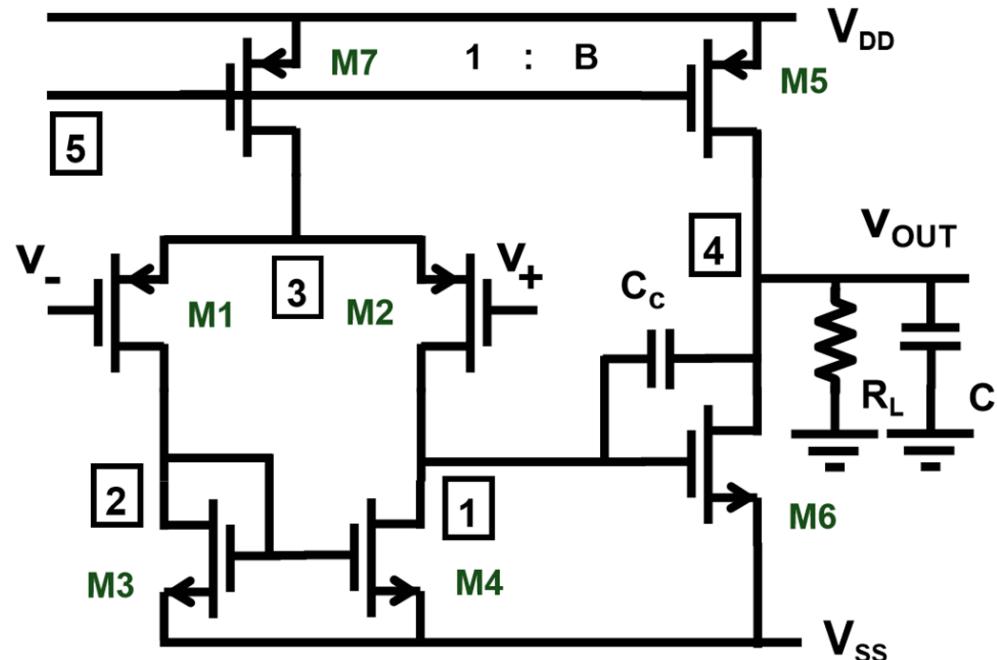
- 运放、反馈与稳定性的基本概念
- 极点分离与零点补偿
- 三级运放稳定性问题简介
- 运放的系统性设计方法
- **运放的其他参数指标**



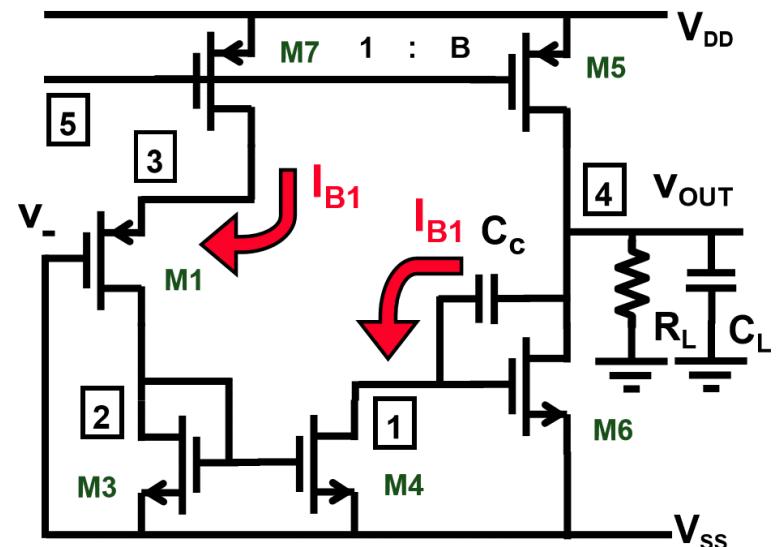
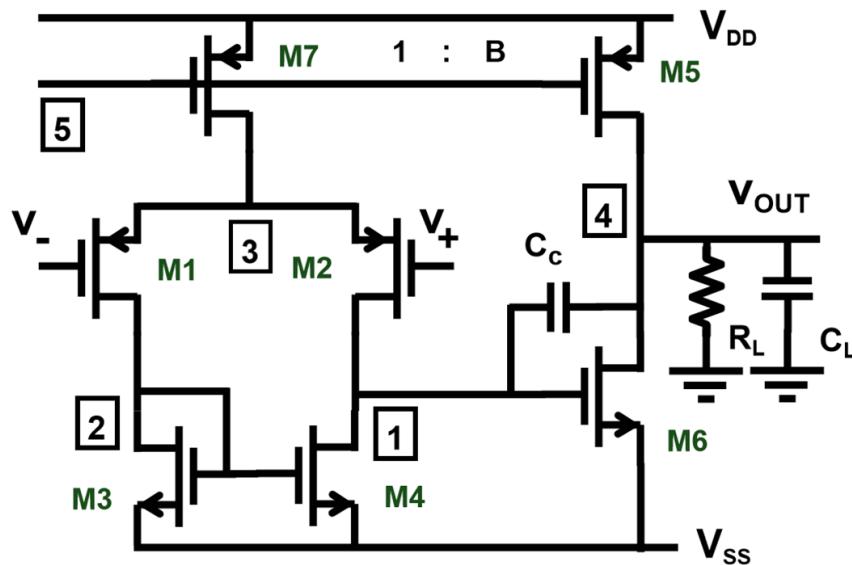
米勒运放的其他指标与分析

- 共模输入电压范围
- 输出电压范围
- 压摆率
- 输出阻抗
- 噪声

》》米勒运放：共模输入范围/输出范围



》》米勒运放：压摆率

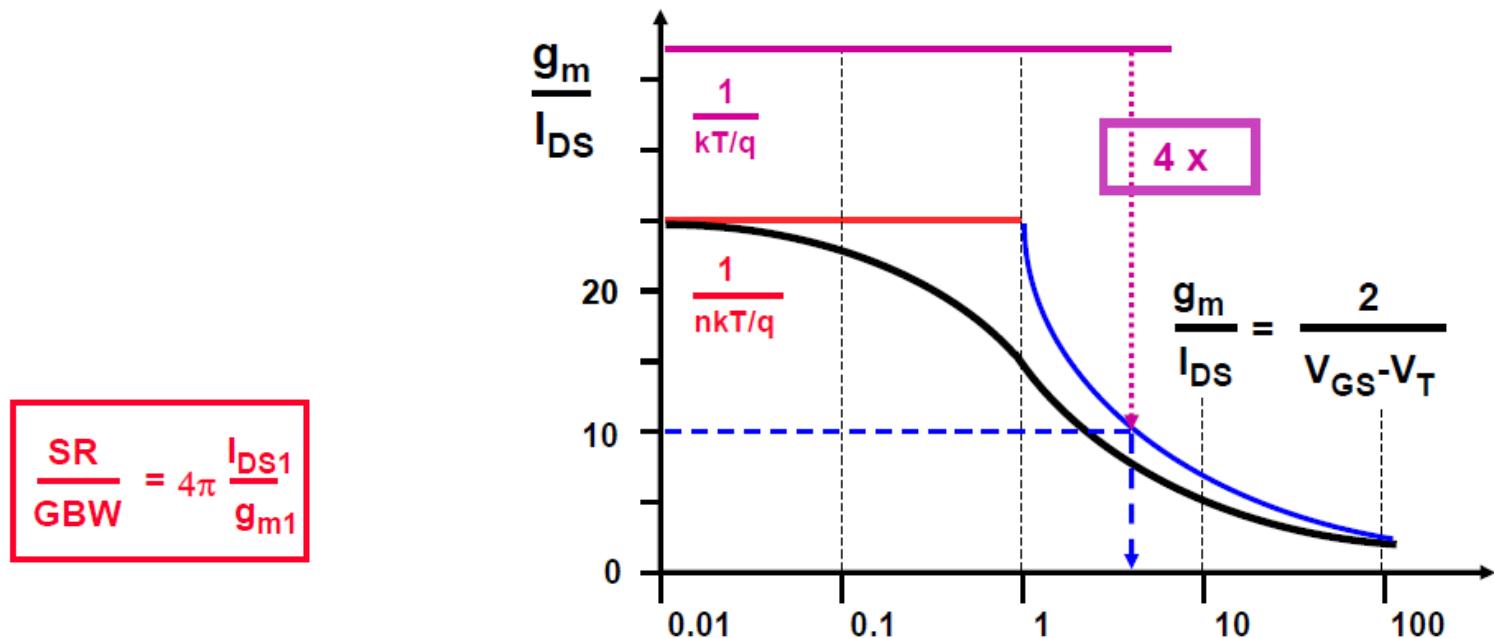


$$SR = \frac{\Delta V_{OUT}}{\Delta t}$$

$$SR = \frac{I_{B1}}{C_c}$$

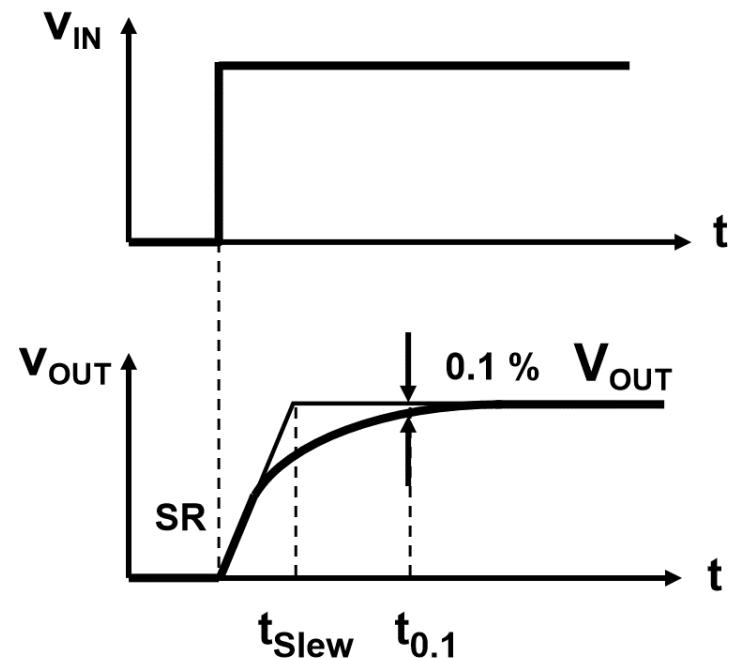
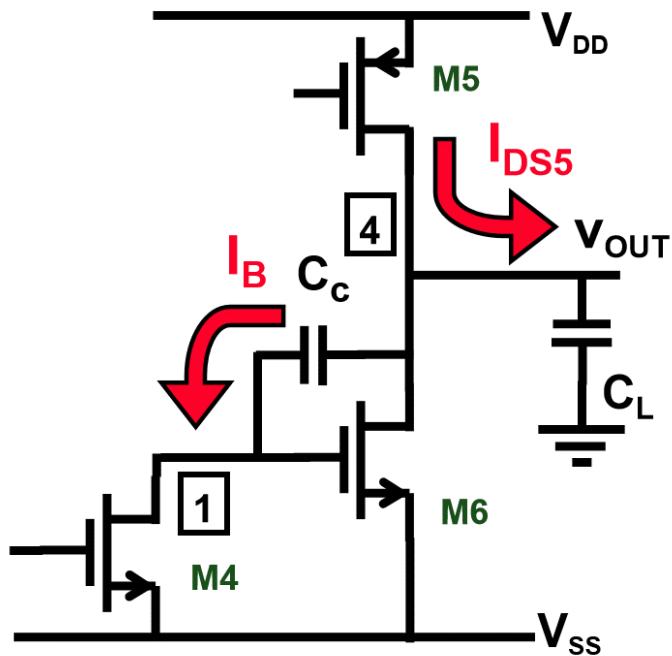
》》米勒运放：压摆率

□ 如何在GBW不变的情况下提高压摆率？



✓ 从始至终，高速设计始终要求大的 $V_{GS} - V_T$

》》米勒运放：压摆率



- 通常压摆率由补偿电容 C_C 决定
- 但是，外部电容也可以成为压摆率的瓶颈



设计思路总结

1. 初步分析

1. 所有节点上的直流电流和电压
2. 所有晶体管的小信号参数分析

2. 直流分析

1. 共模输入电压范围 vs. 电源电压
2. 输出电压范围 vs. 电源电压
3. 最大输出电流



设计思路总结

3. 交流及瞬态分析

1. 所有节点上的直流电阻和电容
2. 增益的频率响应
3. 增益带宽积 vs 偏置电流
4. 压摆率 vs 负载电阻
5. 输出电压范围 vs 频率
6. 建立时间
7. 输入阻抗 vs 频率
8. 输出阻抗 vs 频率



设计思路总结

4. 噪声和失调分析

1. 失调电压 vs 共模输入电压
2. CMRR vs 频率
3. 输入偏置电流
4. 等效输入电压噪声 vs 频率
5. 等效输入电流噪声 vs 频率
6. 容性/感性信号源的噪声优化
7. PSRR vs 频率
8. 失真



设计思路总结

5. 其他效应

1. 电感负载下的稳定性
2. 切换偏置晶体管 (biasing transistors)
3. 切换或扫描电源
4. 不同的电源、温度、工艺等

》》课后习题

□已知要求 $GBW=50MHz$, $C_L=5pF$ 。设计一相位裕度大于 70° 的米勒运放。通过仿真结果，给出该设计运放的：

1. FOM
2. 相位裕度
3. 输入等效总噪声

第 6 章 知识总结 1-5

核心知识点

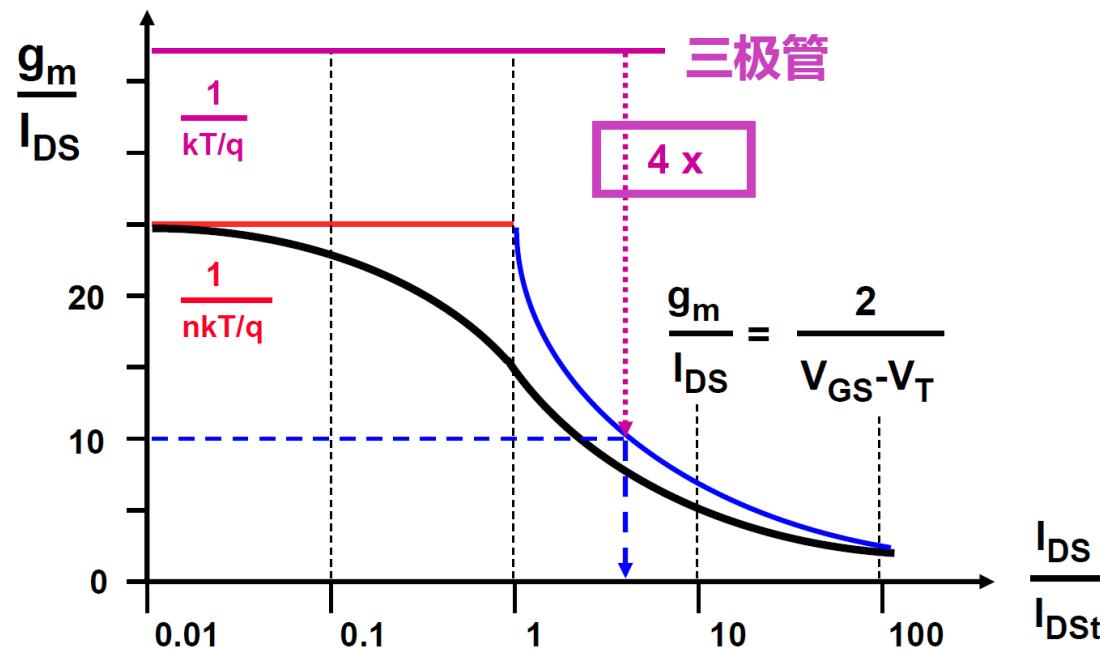
》》第一章: 晶体管

• 晶体管饱和状态下的基本公式

	弱反型区	强反型区	速度饱和区
电流ID	$I_{D0} \frac{W}{L} e^{\frac{V_{GS}}{nkT/q}}$	$\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$	$WC_{OX}v_{sat}(V_{GS} - V_{TH})$
跨导gm	$\frac{I_{D,wi}}{nkT/q}$	$\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) =$ $\sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DS}} = \frac{2I_{DS}}{V_{GS} - V_{TH}}$	$WC_{OX}v_{sat}$

》》第一章: 晶体管

- g_m/I_D 在所有区间内大约在 [25, 1] 的范围内变动，是设计的首要出发点。比如正常偏置下， $V_{GST}=0.2V$ ，则 $g_m/I_D=10$



》》第一章: 晶体管

- 特征频率由晶体管跨导 g_m 和寄生电容 C_{GS} 决定

$$f_T = \frac{g_m}{2\pi C_{GS}}$$

- 特征尺寸下:

反型区 →

$$= \frac{1}{2\pi} \frac{3}{2n} \frac{\mu}{L^2} (V_{GS} - V_T)$$

or

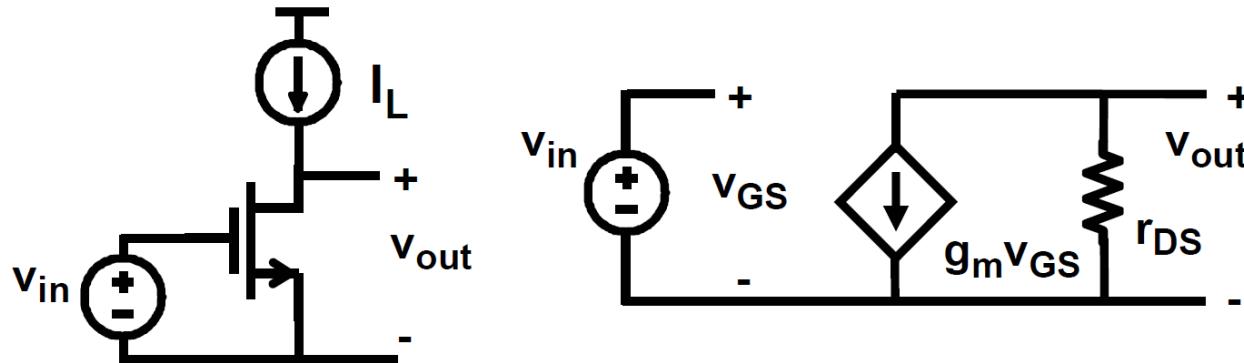
$$\approx \frac{V_{sat}}{2\pi L}$$

← 速度饱和区

- 在0.18um工艺下, 0.5V以下的 V_{GST} 可以认为没有进入速度饱和区

》》 第二章：模拟电路的基本构成

- 单晶体管放大器

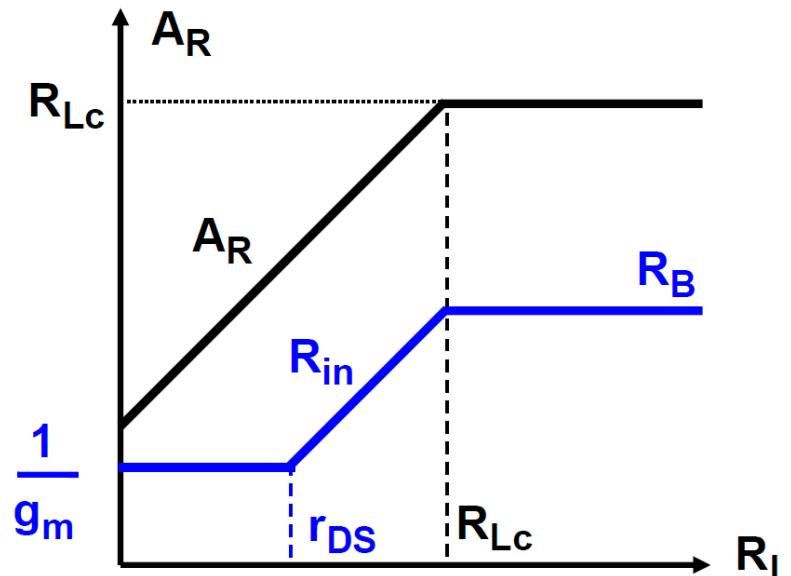
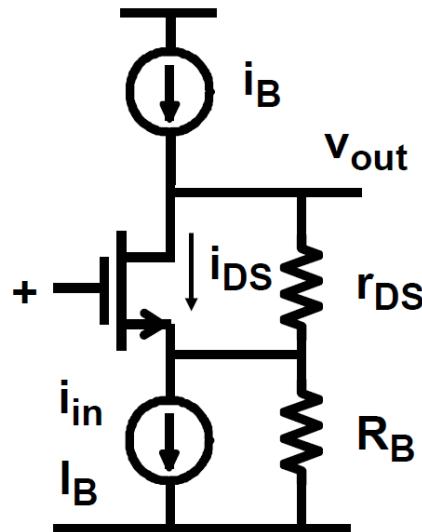


$$A_v = g_m r_{DS} = \frac{2 I_{DS}}{V_{GS} - V_T} \frac{V_E L}{I_{DS}} = \frac{2 V_E L}{V_{GS} - V_T}$$

• V_E 大约为40V/ μm

》》 第二章：模拟电路的基本构成

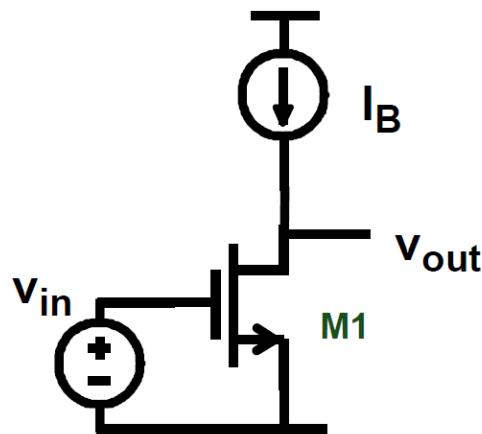
- Cascode (共源共栅极)



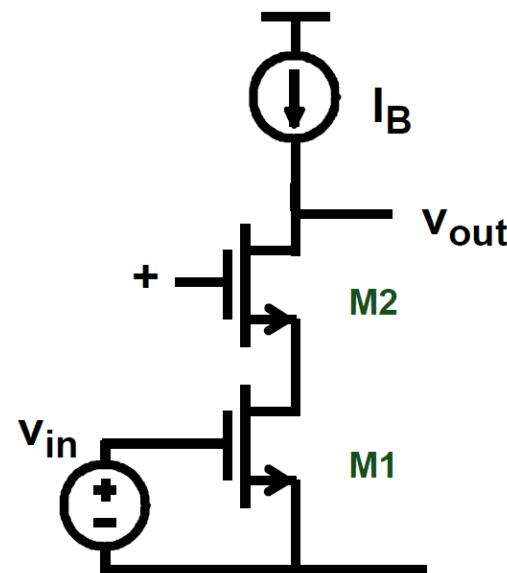
- 从源极看将漏极阻抗缩小A倍，最小至自身跨导倒数 $1/g_m$

》》 第二章：模拟电路的基本构成

- Cascode (共源共栅极)



$$A_v = (g_m r_{DS})_1$$

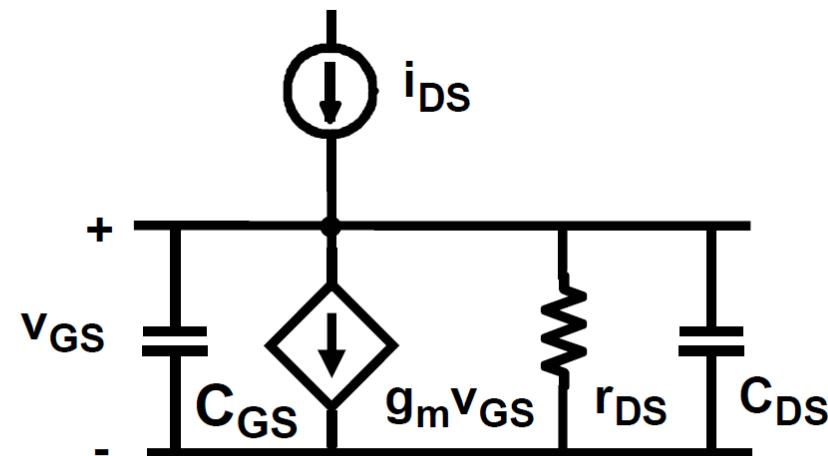
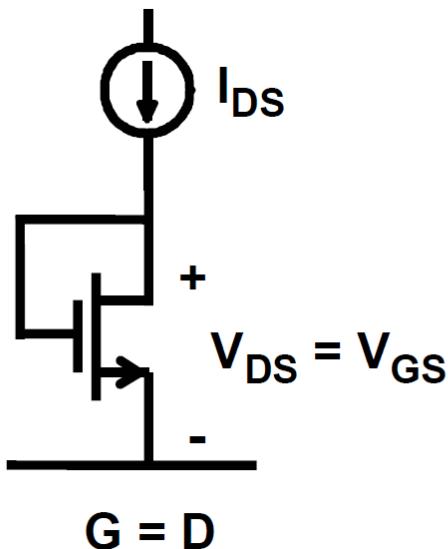


$$A_v = (g_m r_{DS})_1 (g_m r_{DS})_2$$

- 从漏极看将源极阻抗放大 A 倍

》》 第二章：模拟电路的基本构成

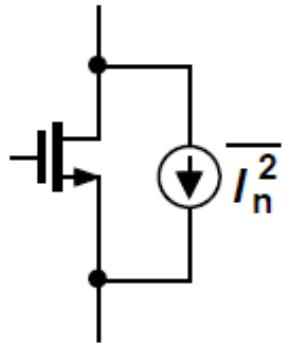
• 二极管连接的晶体管



输入电阻 $r_{ds} = 1/g_m \parallel r_{DS} \approx \boxed{1/g_m}$

》》 第三章：噪声

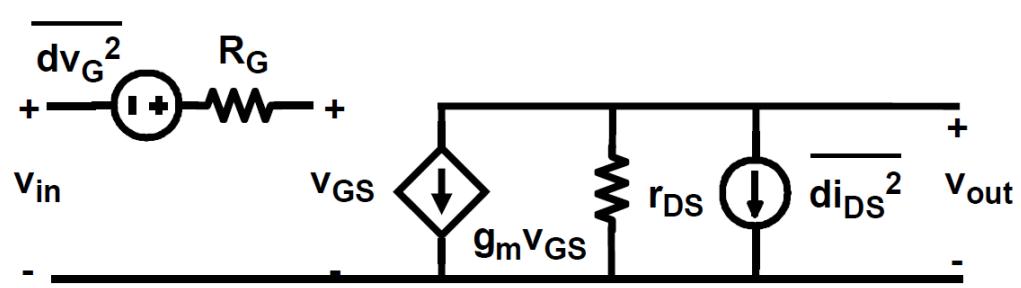
- 晶体管的热噪声



$$\overline{di_n^2} = 4kT/R = 4kT\gamma g_m$$

- 通道电流等效

- 热噪声由晶体管跨导 g_m 决定

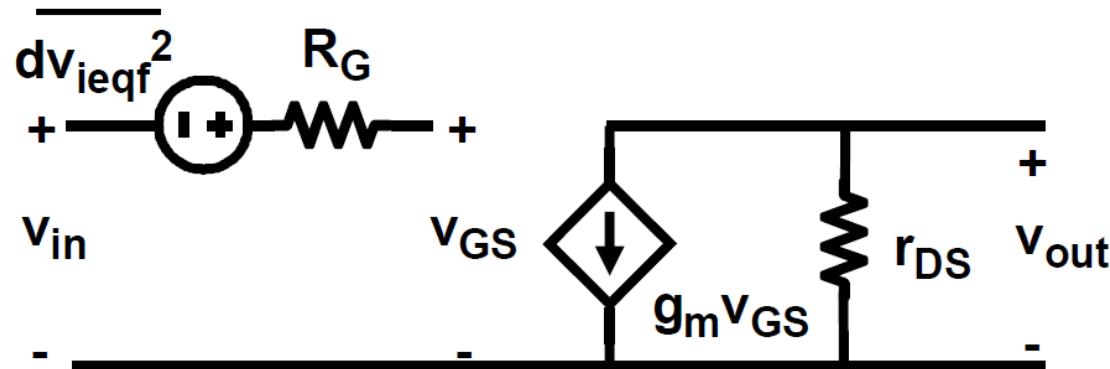


$$\overline{dv_{ieqn}^2} = 4kT\gamma/g_m$$

- 输入电压等效

》》 第三章：噪声

- 晶体管的闪烁噪声



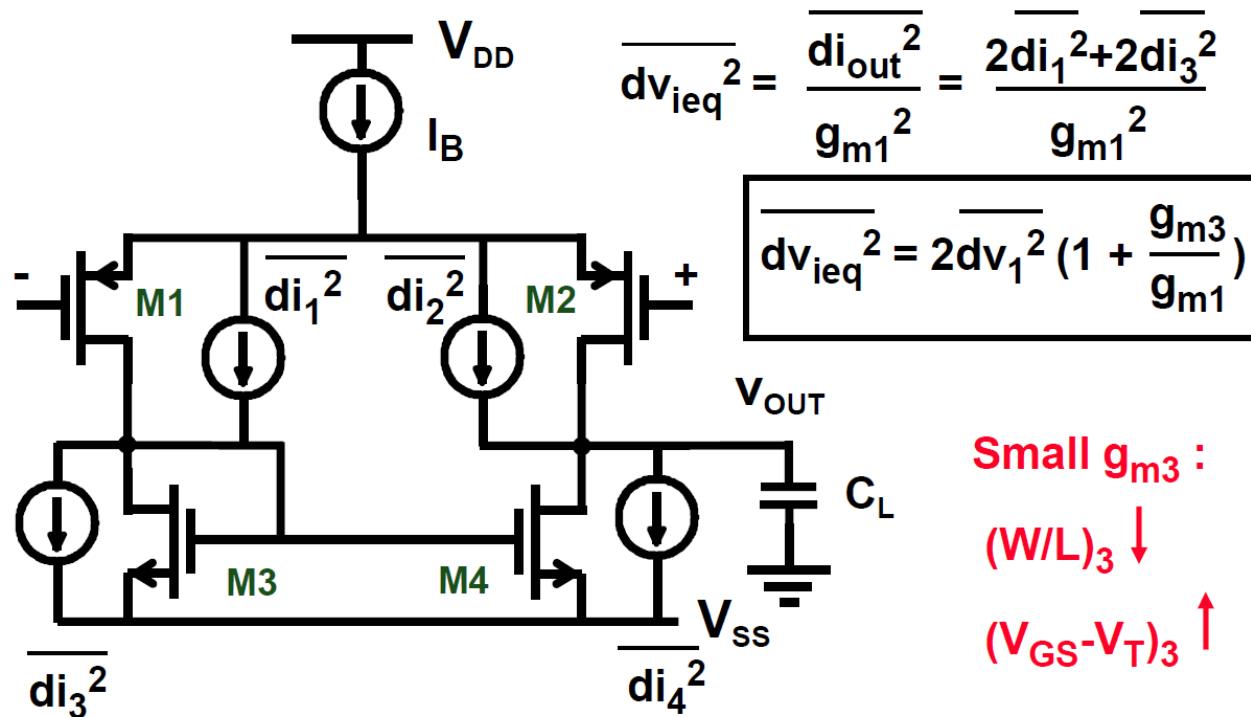
$$\overline{dV_{ieqf}^2} = \frac{K F_F}{W L C_{OX}^2} \frac{\delta f}{f}$$

• 输入电压等效

- 闪烁噪声由晶体管面积决定

第三章：噪声

- 输入等效噪声的换算：所有噪声在输出出累加，然后根据放大倍数转换到输入



》》 第四章：失调

- 随机失调由三部分组成：

$$I_{DS} = K' W/L (V_{GS} - V_T)^2$$

1. 阈值电压 V_{TH} 的偏差

2. 晶体管尺寸的偏差

3. 半导体参数的偏差，基本可以忽略

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}} \quad 1$$

$$A_{VT} \sim t_{ox} \sqrt[4]{N_B}$$

$$\frac{\Delta W/L}{W/L} = A_{WL} \sqrt{\frac{1}{W^2} + \frac{1}{L^2}} \quad 2$$

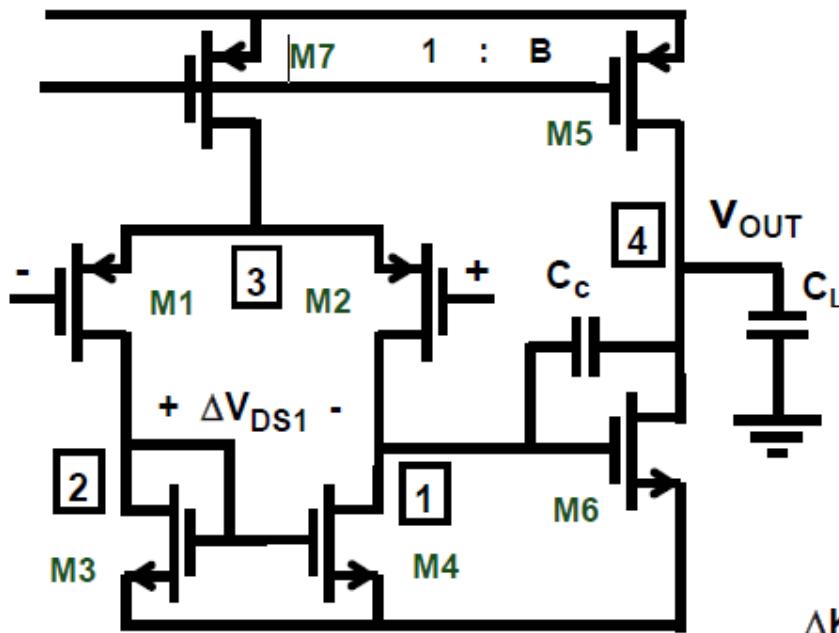
$$A_{WL} \approx 0.02 \text{ mV um}$$

$$\frac{\Delta K'}{K'} = \frac{A_{K'}}{\sqrt{WL}} \quad 3$$

$$A_{K'} \approx 0.0056 \text{ um}$$

第四章：失调

- 等效输入随机失调的主要构成：



$$A_{v1} = g_{m1} r_{02} / r_{04}$$

$$v_{os} = \frac{\Delta V_{DS1}}{A_{v1}} +$$

$$\boxed{\Delta V_{T1} + \frac{g_{m3}}{g_{m1}} \Delta V_{T3}}$$

$$+ \frac{V_{GS1} - V_T}{2} S$$

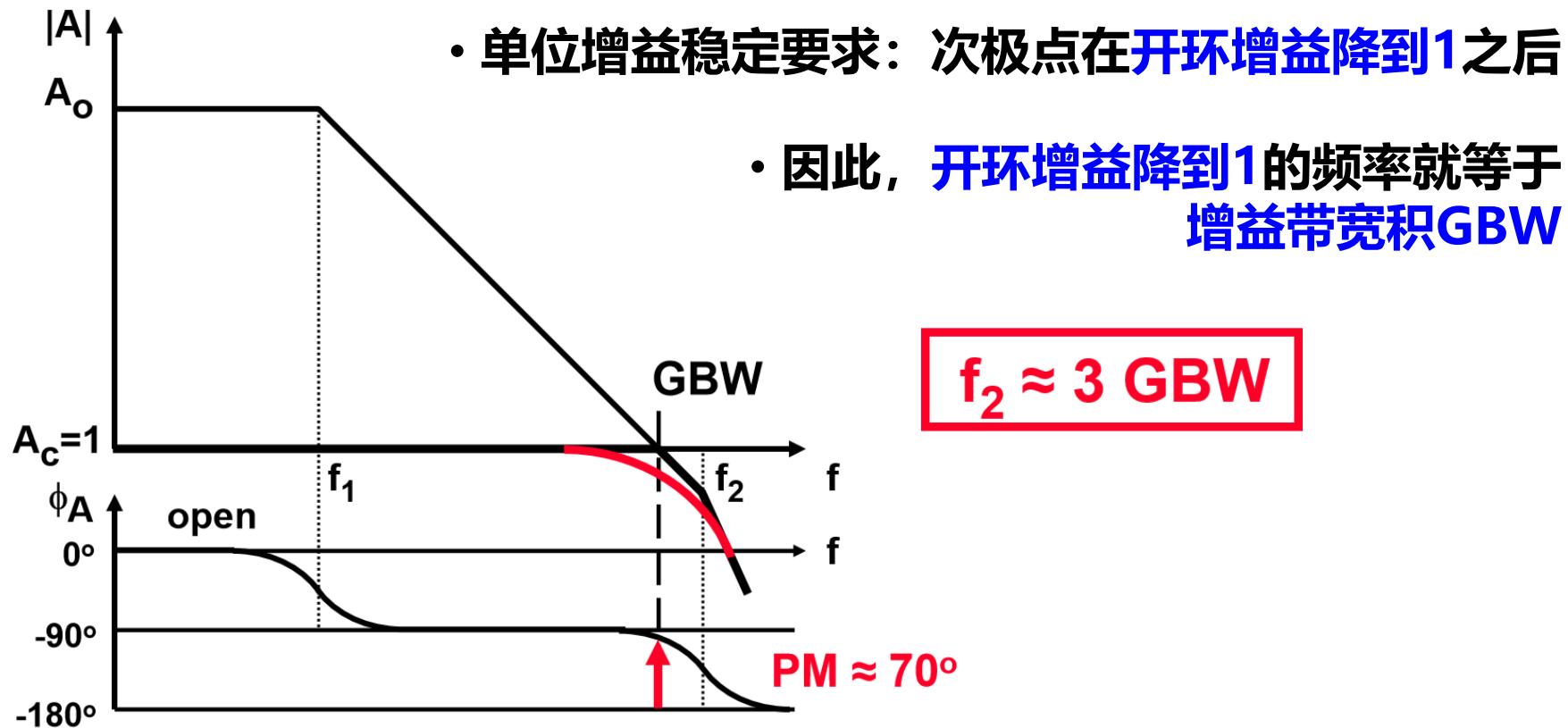
$$S = \frac{\Delta K'_n}{K'_n} + \frac{\Delta K'_p}{K'_p} + \frac{\Delta W/L_1}{W/L_1} + \frac{\Delta W/L_3}{W/L_3}$$

1. 差分对的阈值电压失调

2. 电流镜的阈值电压失调，经过跨导比例转换

3. 所有尺寸的因素，经过差分对过驱动电压转换

》》 第五章：运放的稳定性与系统性设计





第五章：运放的稳定性与系统性设计

- 次极点的选择取决于系统的要求

$\frac{f_2}{GBW}$	PM (°)	$\zeta = \frac{1}{2} \sqrt{\frac{f_2}{GBW}}$	P _f (dB)	P _t (dB)
0.5	27	0.35	3.6	2.3
1	45	0.5	1.25	1.3
1.5	56	0.61	0.28	0.73
2	63	0.71	0	0.37
3	72	0.87	0	0.04



第五章：运放的稳定性与系统性设计

- 两级运放的GBW由第一级跨导 g_{m2} 和补偿电容 C_c 决定
- 次极点由第二级跨导 g_{m2} 和负载电容 C_L 决定

$$\text{GBW} = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} = 3 \text{ GBW} = \frac{g_{m2}}{2\pi C_L} \cdot \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

$$\frac{g_{m2}}{g_{m1}} \approx 4 \frac{C_L}{C_c}$$

≈ 0.3

Larger current in 2nd stage !

》》 第五章：运放的稳定性与系统性设计

$$GBW = \frac{g_{m1}}{2\pi C_c} \quad f_{nd} = 3 \text{ } GBW = \frac{g_{m2}}{2\pi C_L} \cdot \frac{1}{1 + \frac{C_{n1}}{C_c}}$$

• 为什么 C_c 不能太大?

- C_c 太大会使 g_{m1} 的要求过大，导致功耗激增

• 为什么 C_c 不能太小?

- C_c 太小会 f_{nd} 中的系数 $(1 + C_{n1}/C_c)$ 快速上升，导致 f_{nd} 下降

》》 第五章：运放的稳定性与系统性设计

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

C_c的选择=>

$$C_L = \alpha C_c$$

$\alpha \approx 2$

$$C_c = \beta C_{n1} = \beta C_{GS6} \quad \beta \approx 3$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + C_{n1}/C_c}$$

$$f_{nd} = \gamma GBW$$

$\gamma \approx 2$

$$C_{GS} = kW$$

$k = 2fF/um$, for minL

$$GBW = \frac{f_{nd}}{\gamma} = \frac{g_{m6}}{2\pi C_L} \frac{1}{\gamma (1 + 1/\beta)}$$

$$C_L = \alpha C_c = \alpha \beta C_{n1} = \alpha \beta C_{GS6} = \alpha \beta kW_6$$

$W_6 \uparrow$ if $C_L \uparrow$

》》第五章：运放的稳定性与系统性设计

1. 选择 $\alpha \beta \gamma$ ← 根据运放应用的具体要求确定
2. 找到满足GBW最小的 f_T
3. 根据增益要求选择 L_6
 - 得到 f_{TH6}← 如果没有增益要求，可以使用最小长度。根据所选择长度计算晶体管可以支持的频率。
4. 根据 C_L 和 L_6 计算 W_6 ← 如若没有面积限制，宽度越宽越好，直至 $C_{GS}(C_{n1})$ 的限制
5. 根据 I_{DSH6} 和 反型系数 i 计算 I_{DS6}
 - $K_n' = 280\mu A/V^2$← 根据计算所得长宽比，得到该尺寸强反型区的跨导 gm ；根据该跨导和所需跨导的比例，计算偏置电流。
6. 通过选择的 α 和 C_L 计算 C_C
7. 通过 C_C 计算 g_{m1} 和 I_{DS1}

第7章 全差分放大器



CMOS模拟集成电路设计

第七章：运放的高级设计： 全差分放大器

胡远奇

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全差分放大器

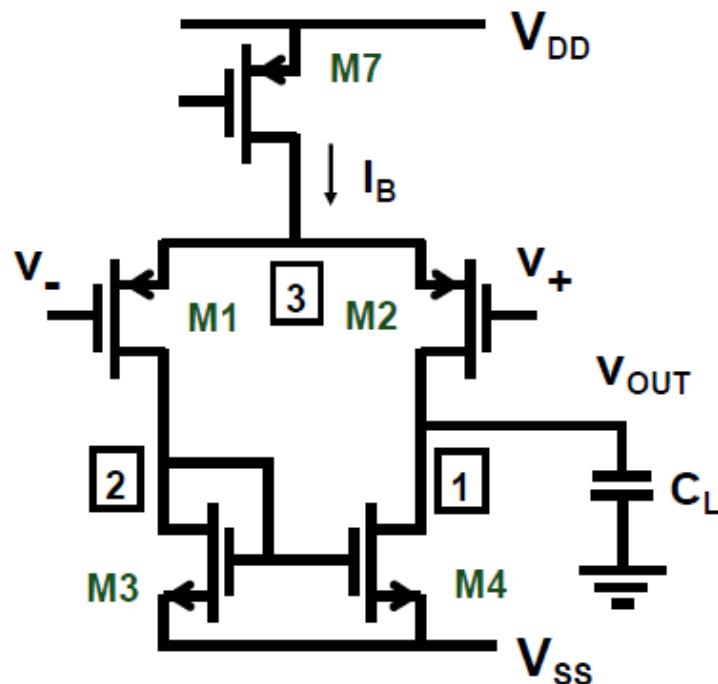
- 基本概念
- 通过线性区晶体管的共模反馈
- 通过误差放大器的共模反馈



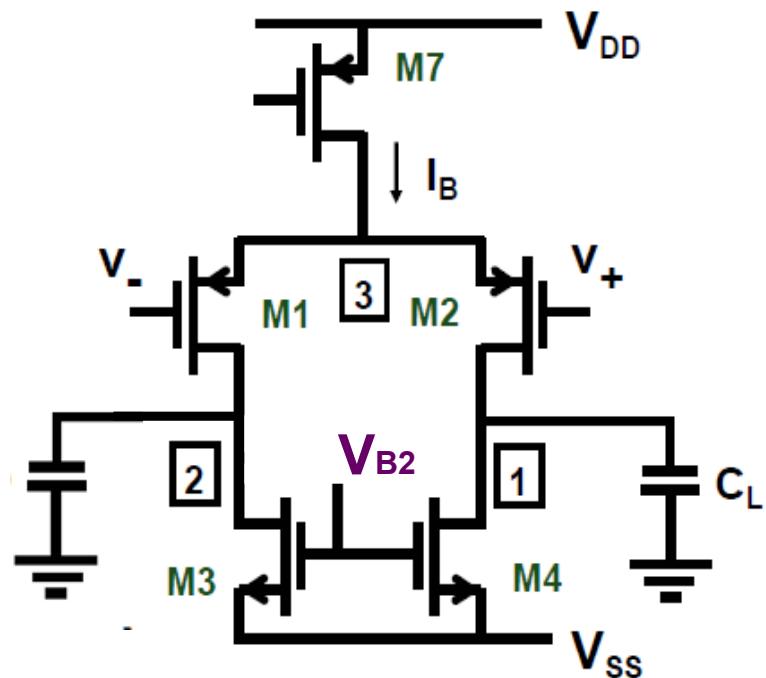
全差分运放

- 什么是全差分运放?
 - 相比于单端输出，全差分运放有两个差分输出端口。
 - 能够更好的抵抗电源上和共模上的噪声。
 - 数模混合电路通常要求**全差分**的电路实现!
- 需要更高的功耗
- 需要**共模反馈!**
(Common-Mode Feedback, CMFB)

》》全差分运放：简单示例

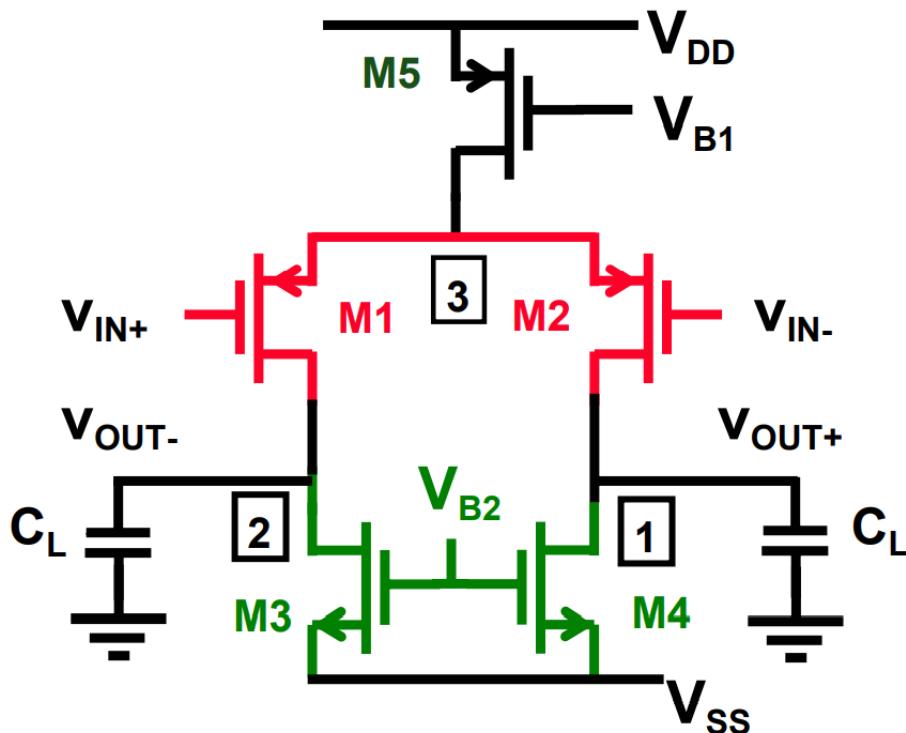


单端输出



差分输出

》》全差分运放：简单示例

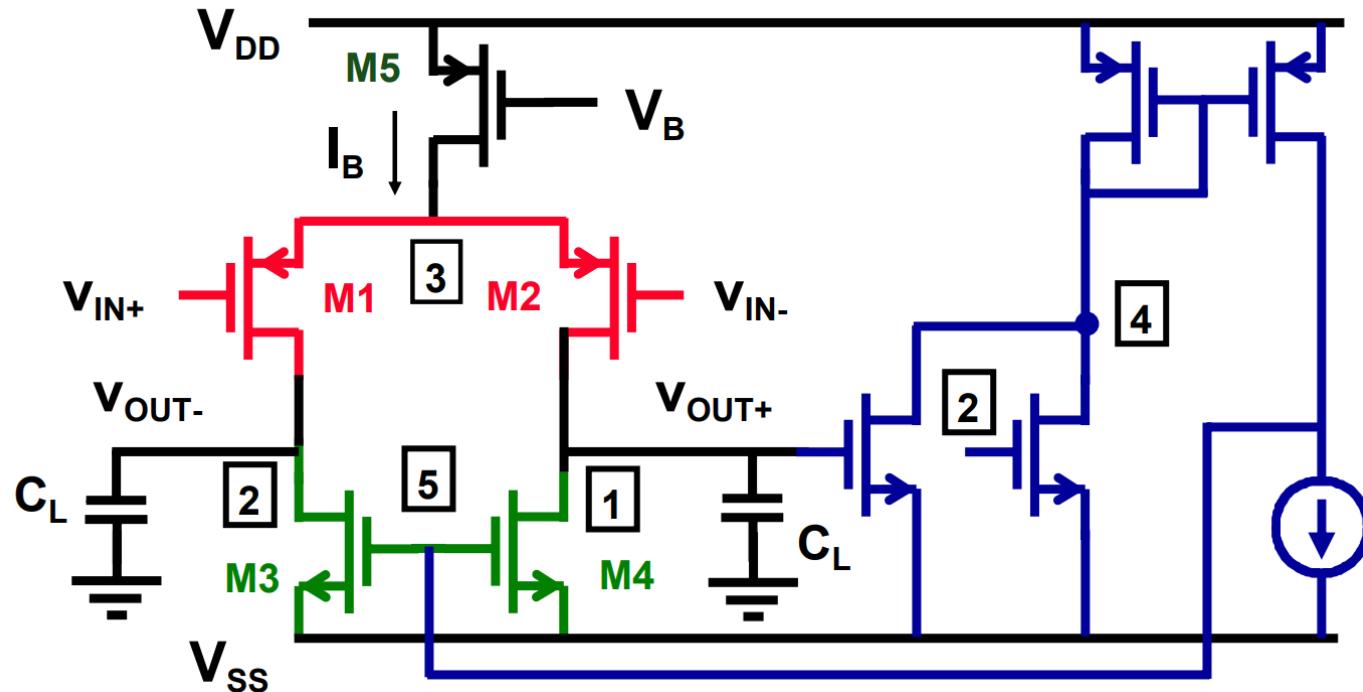


差分对
没有电流镜结构

问题：
如何使M1-M4均保持在饱和区？

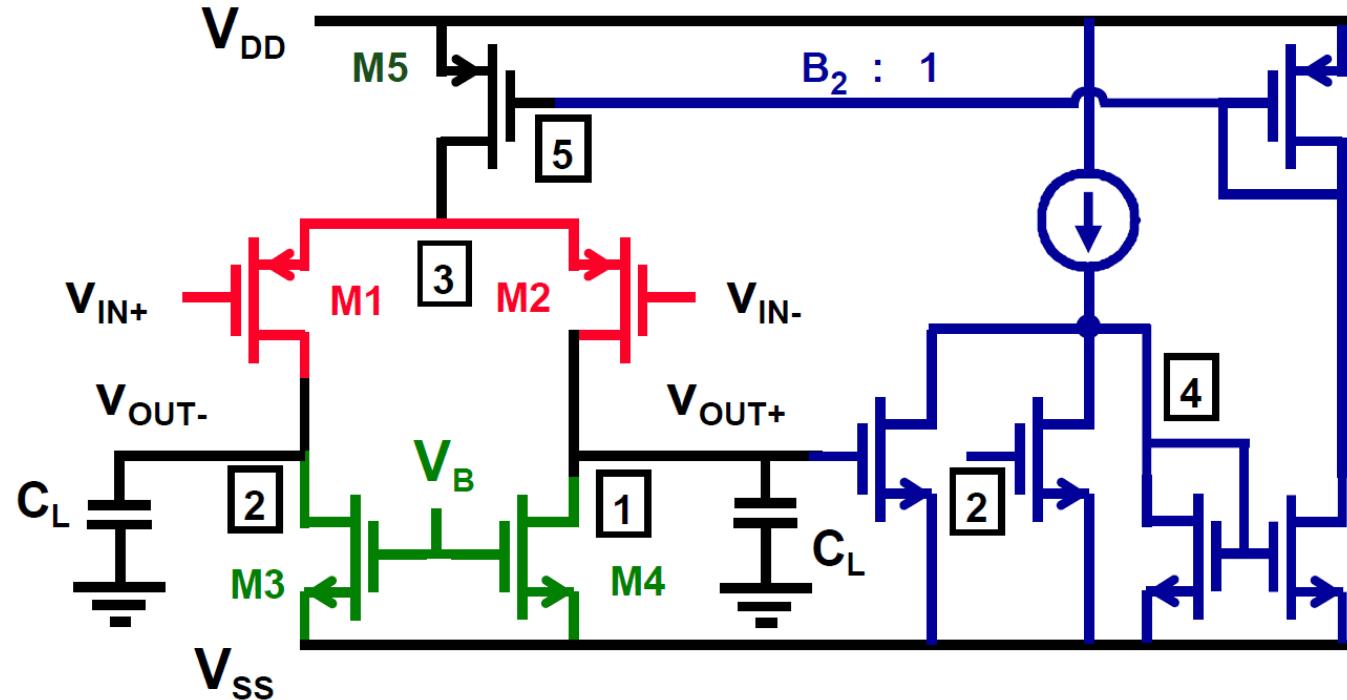
↓
控制共模输出
↓
差分对和有源负载的电流偏置需要完全一样

》》全差分运放：共模反馈示例



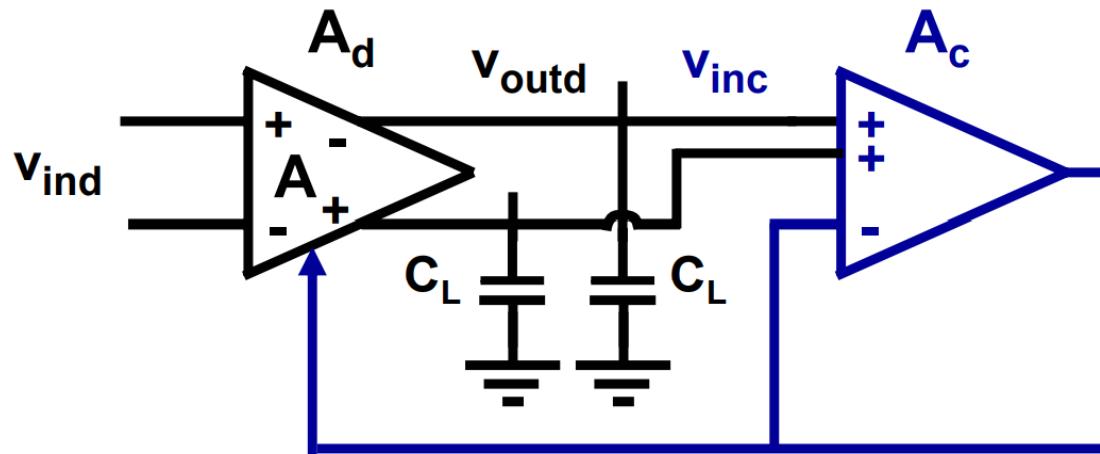
- 对差分输出 V_{OUT+} 和 V_{OUT-} 进行采样，并取**平均值**【4】
- 形成环路，通过负反馈控制共模偏置 (**任意一处**)

》》全差分运放：共模反馈示例



- 对差分输出 V_{OUT+} 和 V_{OUT-} 进行采样，并取**平均值**【4】
- 一级运放 -> 更稳定

》》共模反馈



单位增益下的共模反馈 => $\text{CMRR} = A_{CM}$

三个任务：

1. 检测差分输出电压
2. 取出共模信号成分
3. 将共模信号反馈回差分电路

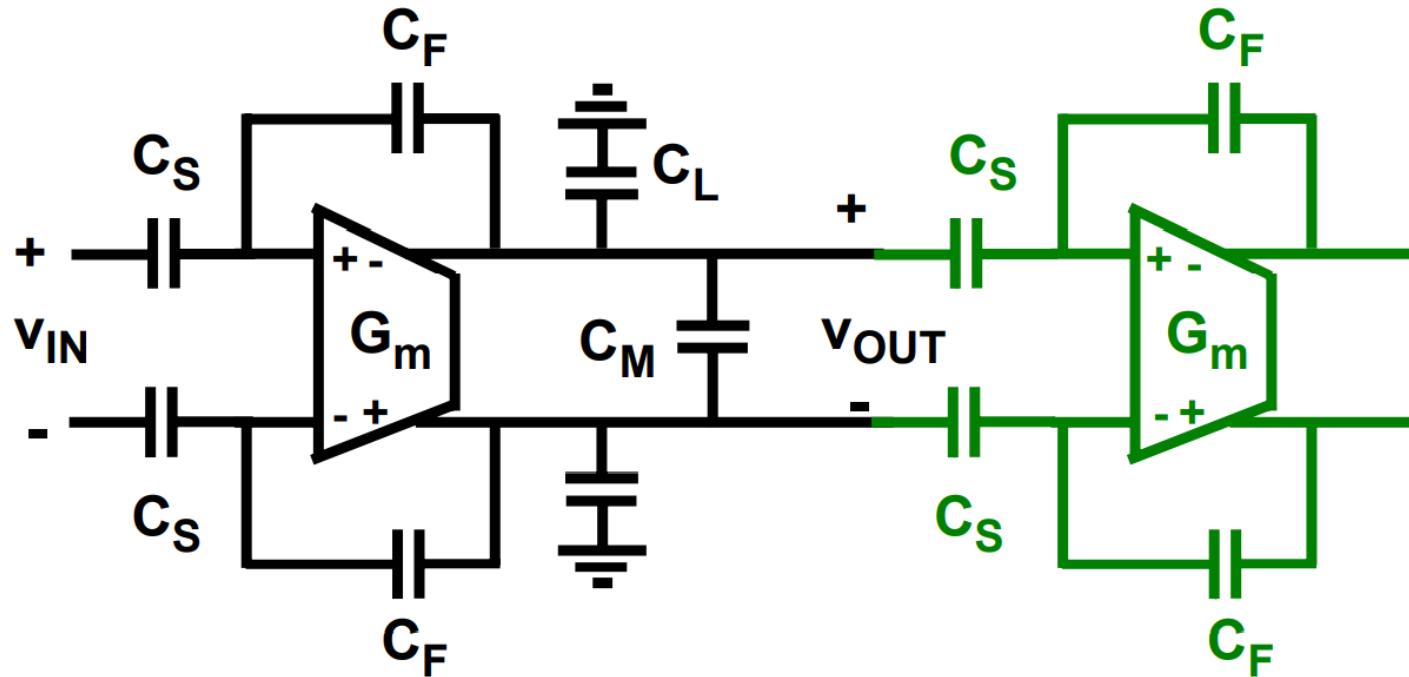


共模反馈的基本要求

- 高速: $\text{GBW}_{\text{CM}} > \text{GBW}_{\text{DM}}$
 - 根据应用有所不同, e.g SDM ADC
- 低功耗: $P_{\text{CM}} < P_{\text{DM}}$
 - 与高速的要求矛盾
- 输出范围将被更小的一项所限制:
 - 差分运放的输出
 - 共模运放的输入范围

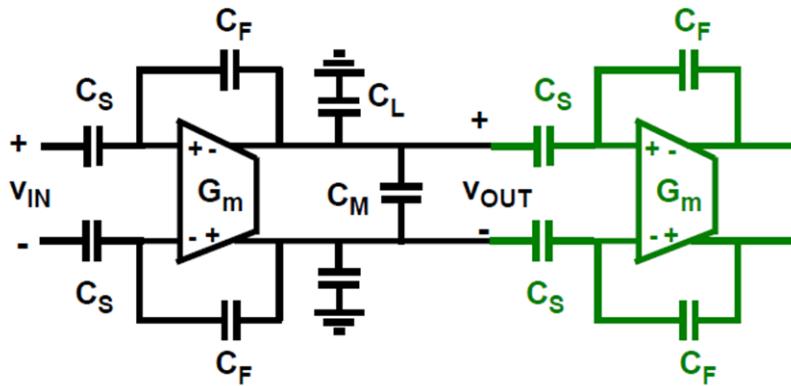
》》共模反馈的负载

- 共模与差模放大器经常会驱动不同的负载。



两级运放级联

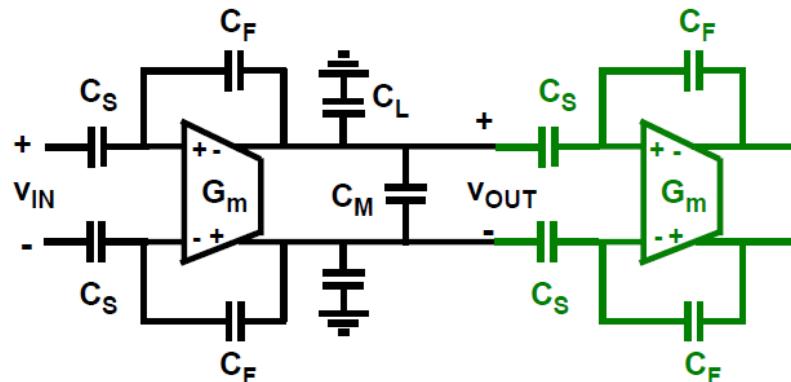
》》共模反馈的负载



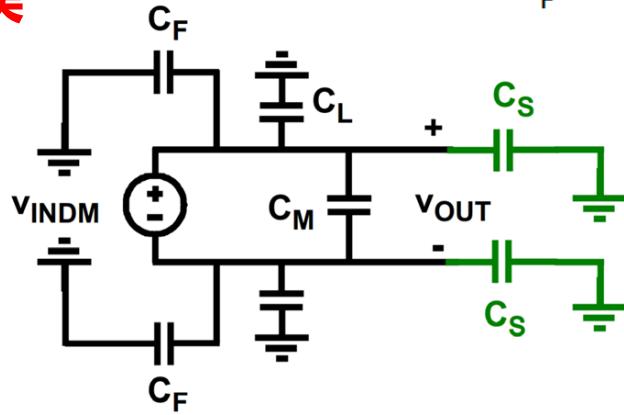
对于差分信号而言，
运放的输入就是**虚地**

对于共模信号而言，
信号通路可以**合并**

》》共模反馈的负载

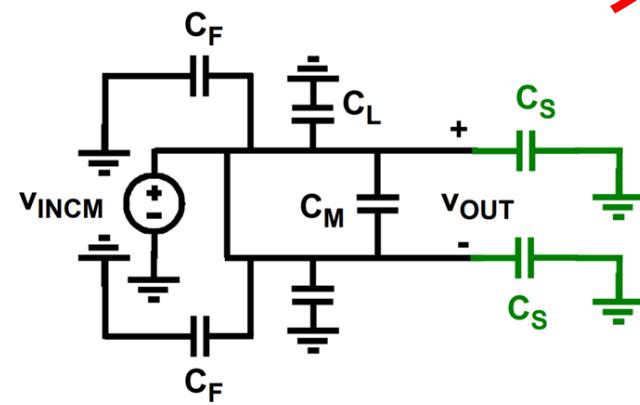


差模



$$C_{INDM} = 2C_M + C_F + C_L + C_S$$

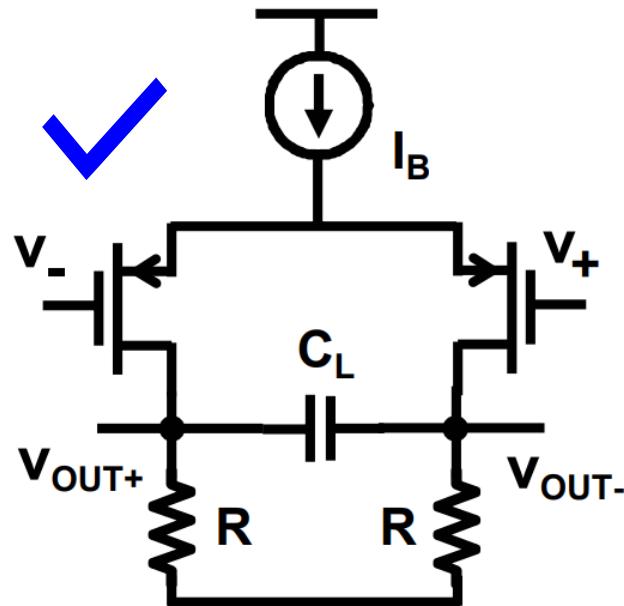
共模



$$C_{INCM} = 2(C_F + C_L + C_S)$$

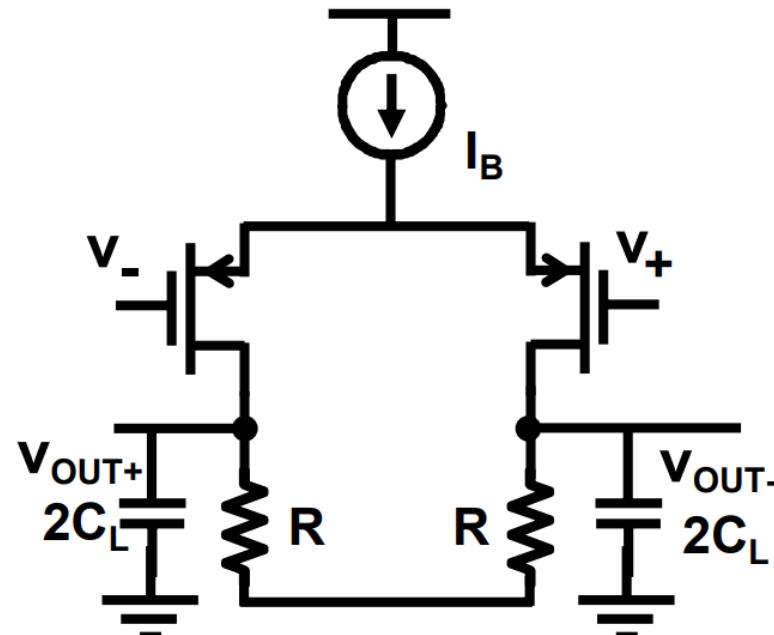


共模反馈：差模和共模的GBW



$$GBW_{DM} = \frac{g_m}{2\pi 2C_L}$$

$$C_{LCM} = 0$$



$$GBW_{DM} = \frac{g_m}{2\pi 2C_L}$$

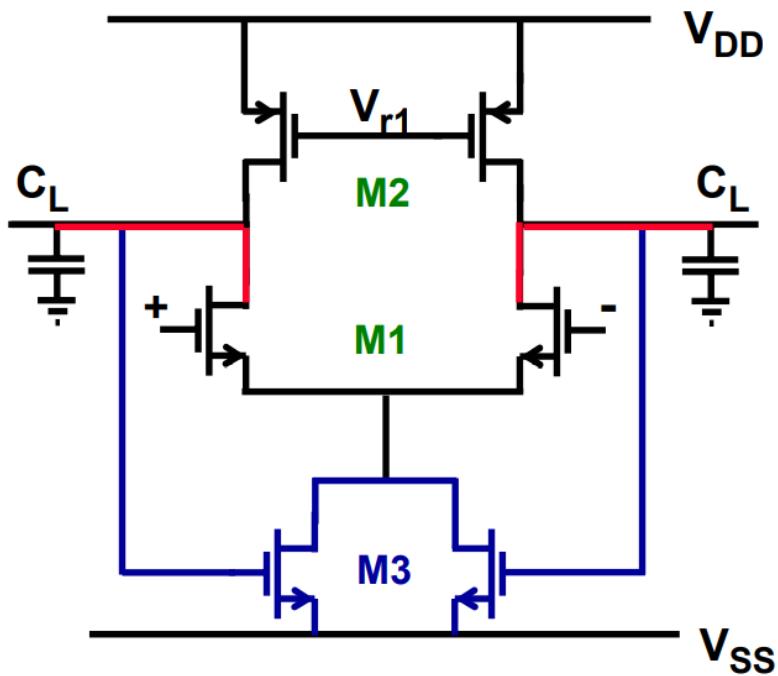
$$C_{LCM} = 4 C_L$$



全差分放大器

- 基本概念
- **通过线性区晶体管的共模反馈**
- 通过误差放大器的共模反馈

》》共模反馈：线性区晶体管



差分输出

共模反馈

M3处于线性区：

$$V_{DS3} < 200mV$$

$$V_{GS3} = (V_{DD} + V_{SS})/2$$

$$I_{DS} = KP(V_{GS} - VT) V_{DS}$$

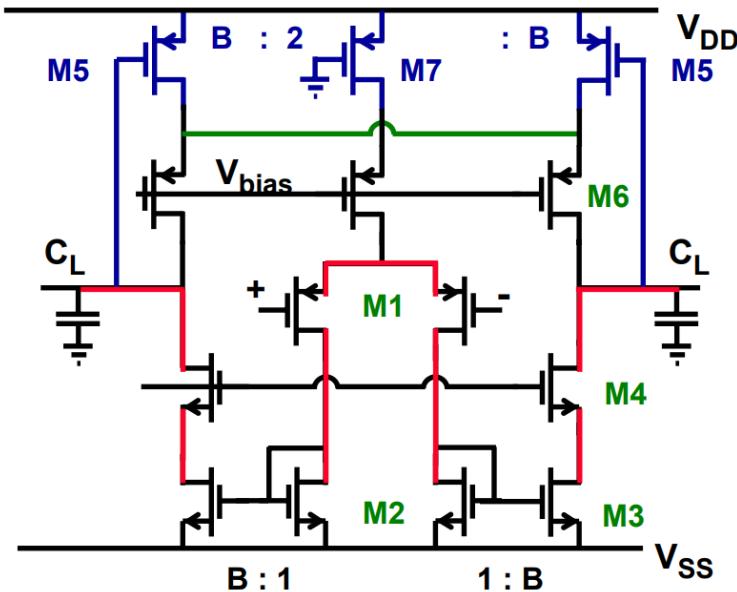
共模跨导？



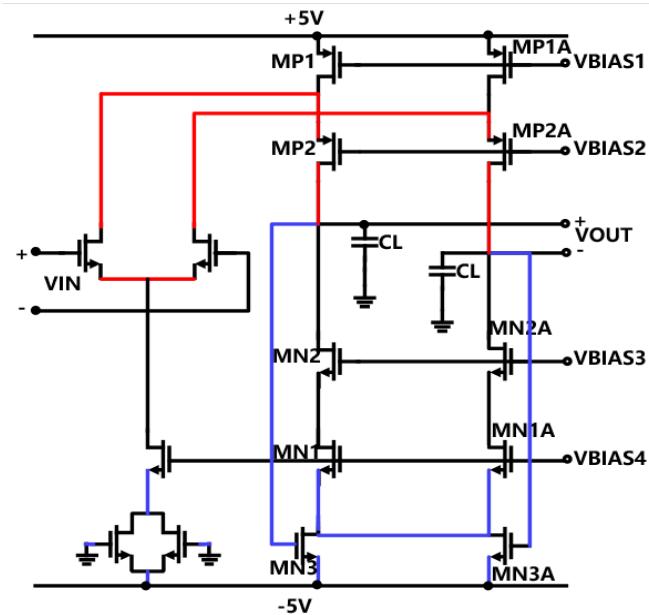
$$g_{m3} = KP V_{DS3}$$

$$GBW_{CM} = \frac{g_{m3}}{2\pi C_L} < GBW_{DM} = \frac{g_{m1}}{2\pi C_L}$$

》》共模反馈：线性区晶体管



差分输出



共模反馈

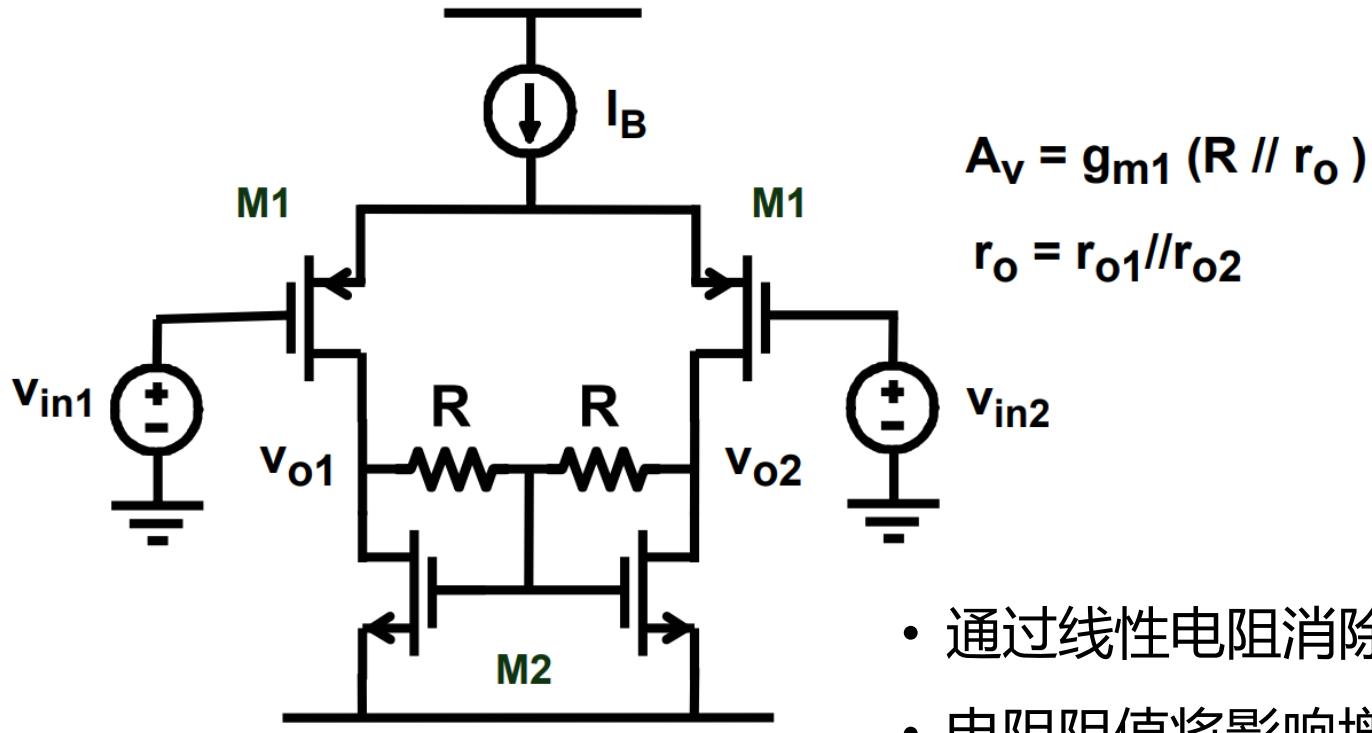
- 线性区晶体管的共模反馈可以与其他技术融合使用，且**没有额外的功耗**，但是**共模GBW始终偏低！**



全差分放大器

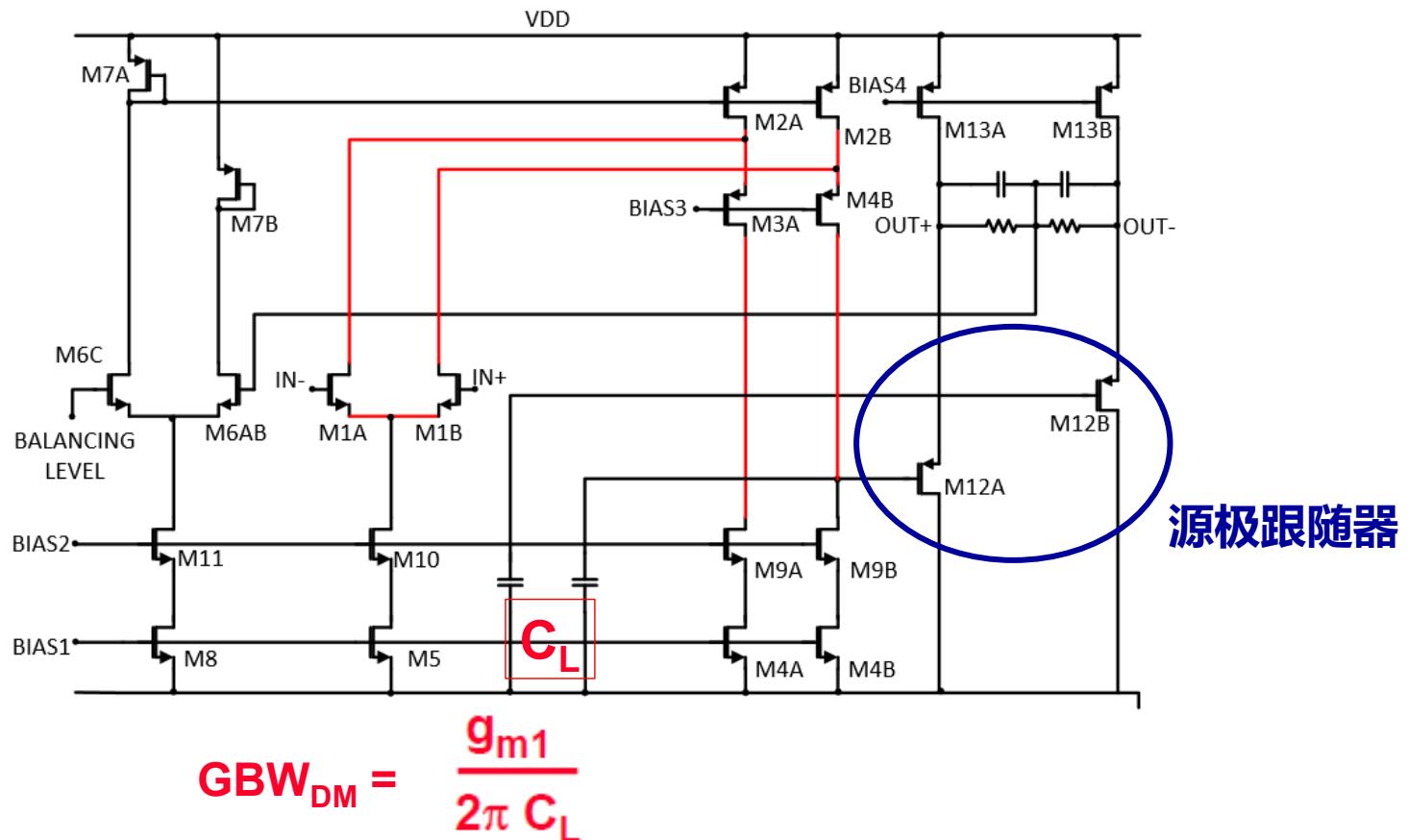
- 基本概念
- 通过线性区晶体管的共模反馈
- **通过误差放大器的共模反馈**

» 电阻性共模反馈

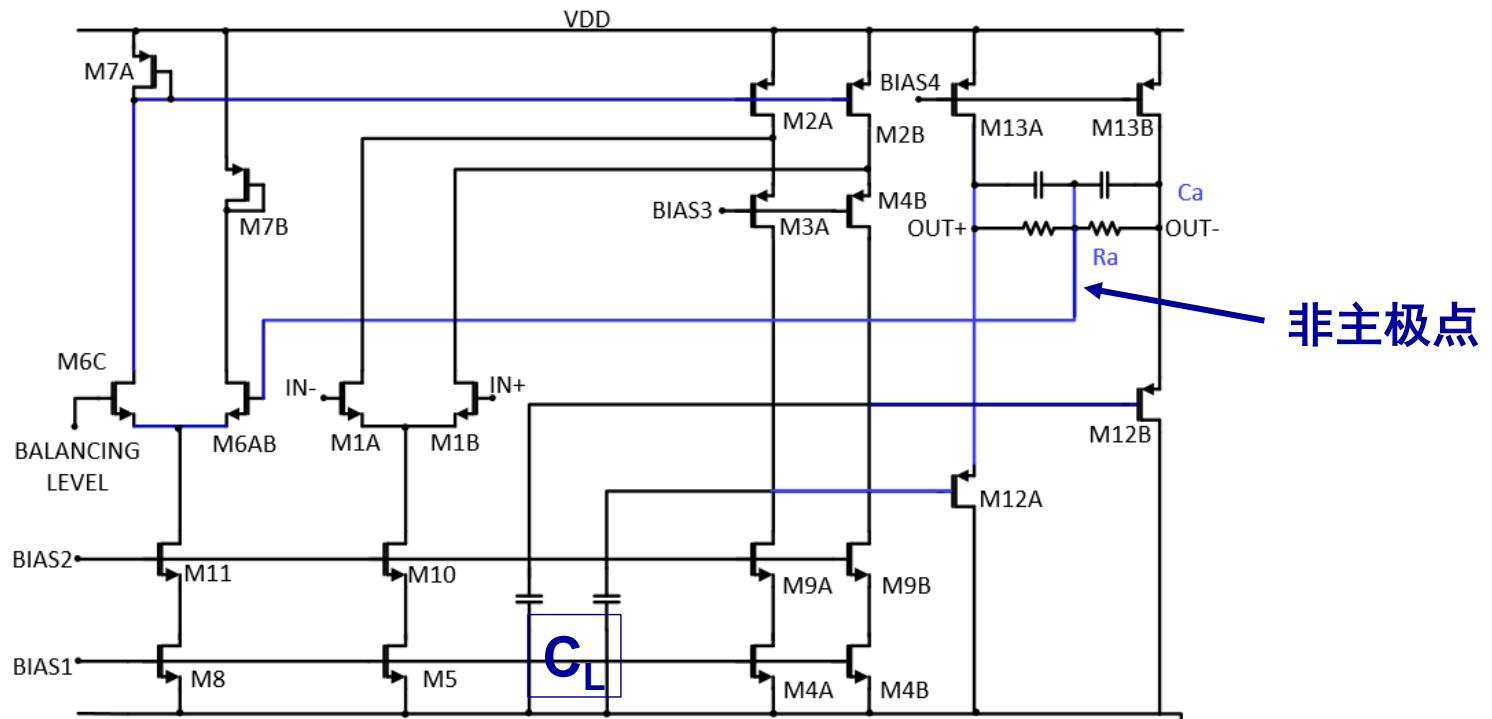


- 通过线性电阻消除差分信号
- 电阻阻值将影响增益
- 如何隔离输出端与采样电阻?

》》共模反馈+源极跟随器

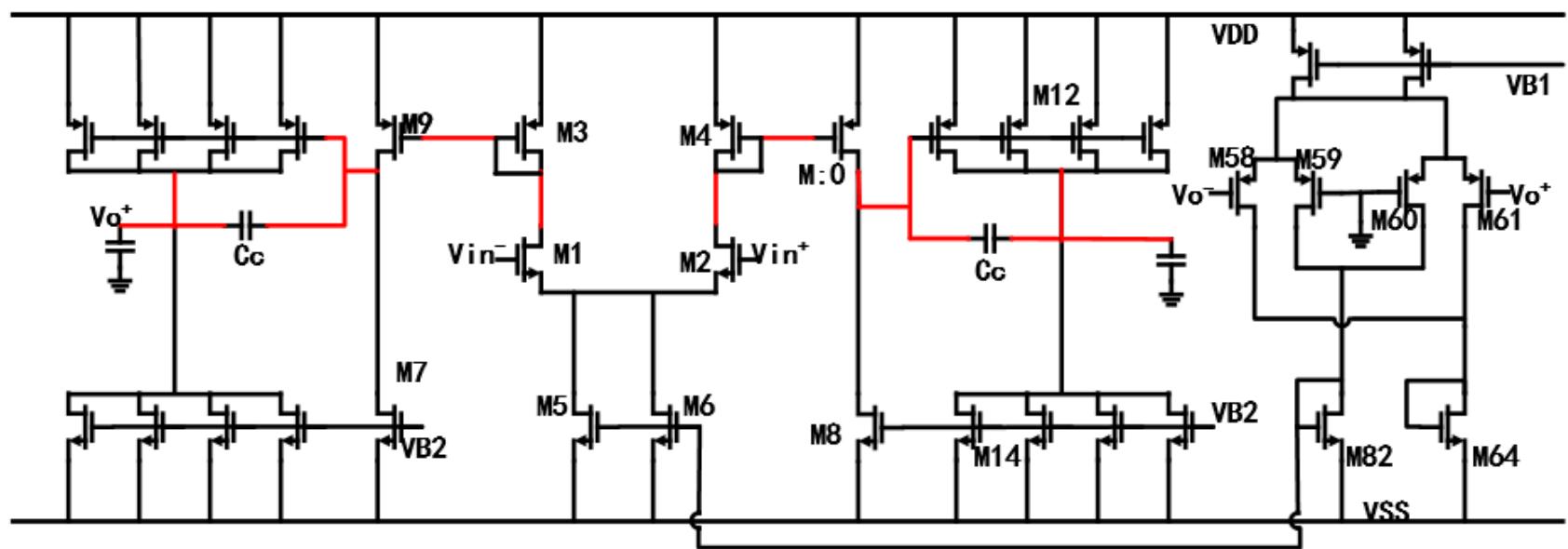


》》共模反馈+源极跟随器



$$GBW_{CM} = \frac{g_{m6}}{4\pi C_L} \quad f_{ndCM} = \frac{4}{2\pi R_a(C_{GS6} + C_a)} \quad f_z = \frac{1}{2\pi R_a C_a}$$

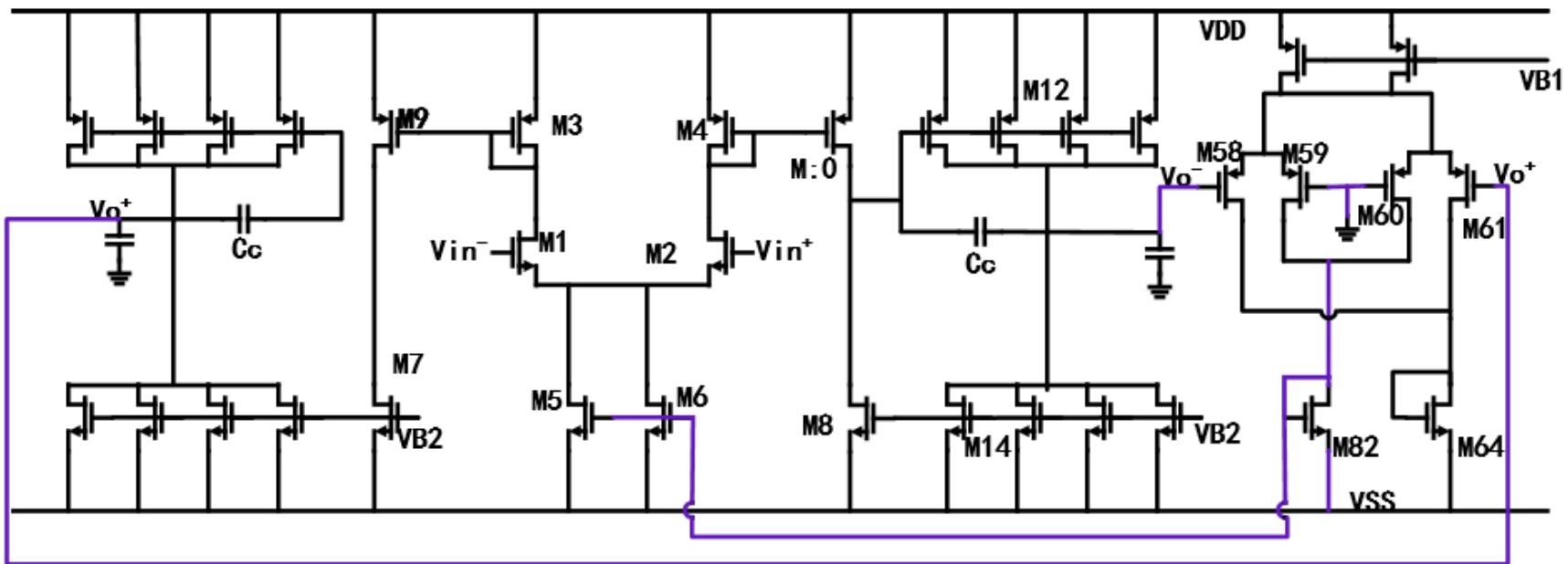
》》共模反馈+误差放大器



- 不使用源极跟随器

$$GBW_{DM} = \frac{g_{m1}}{2\pi C_c}$$

》》共模反馈+误差放大器



- 不使用源极跟随器
- 更好的功耗表现

$$GBW_{CM} = \frac{g_{m58}}{4\pi C_c}$$

- 差分对线性区十分有限
- $2.8 * V_{GST}$



共模反馈技术比较

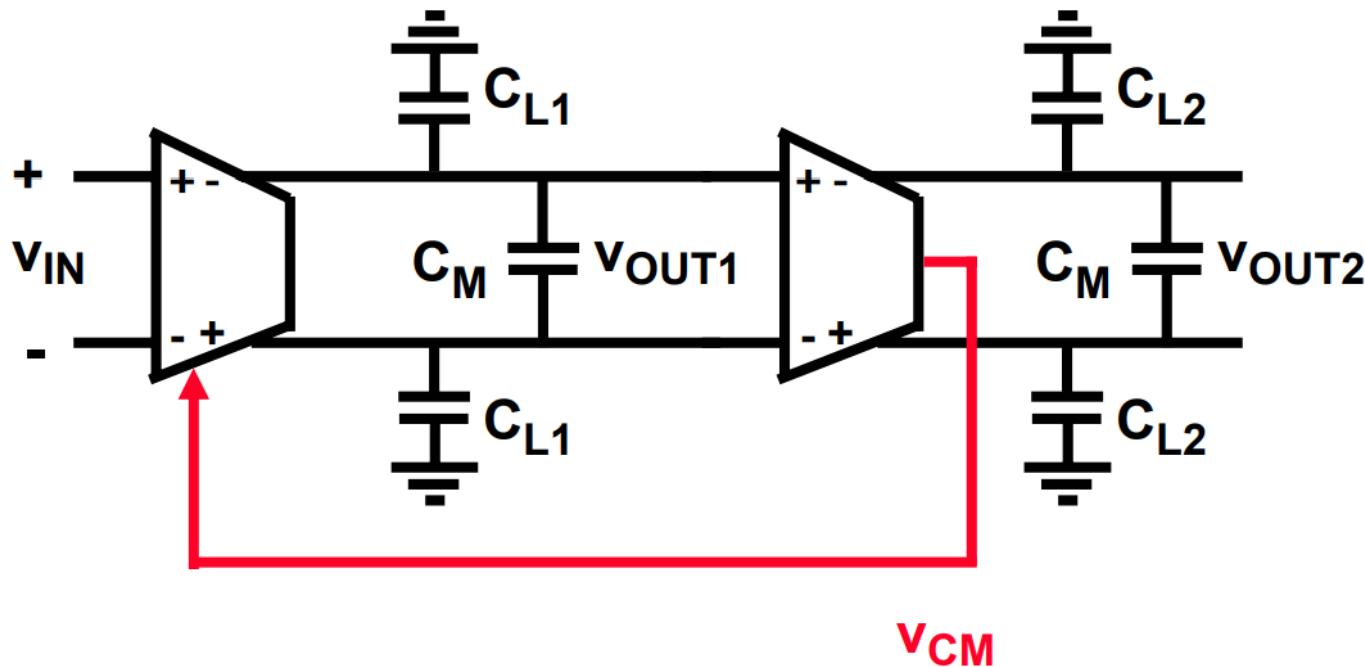
类型	线性晶体管	误差运放+源极跟随器	误差运放+双差分对
GBW_{CM}/GBW_{DM}	<0.1	>1	>1
匹配要求	<1%	<6%	<6%
输出范围	$0.8V_{DD}$	$0.4V_{DD}$	$0.4V_{DD}$
受限于	Cascode	源极跟随器	差分输入范围
功耗	1 Amp	3 Amp	2 Amp



全差分放大器

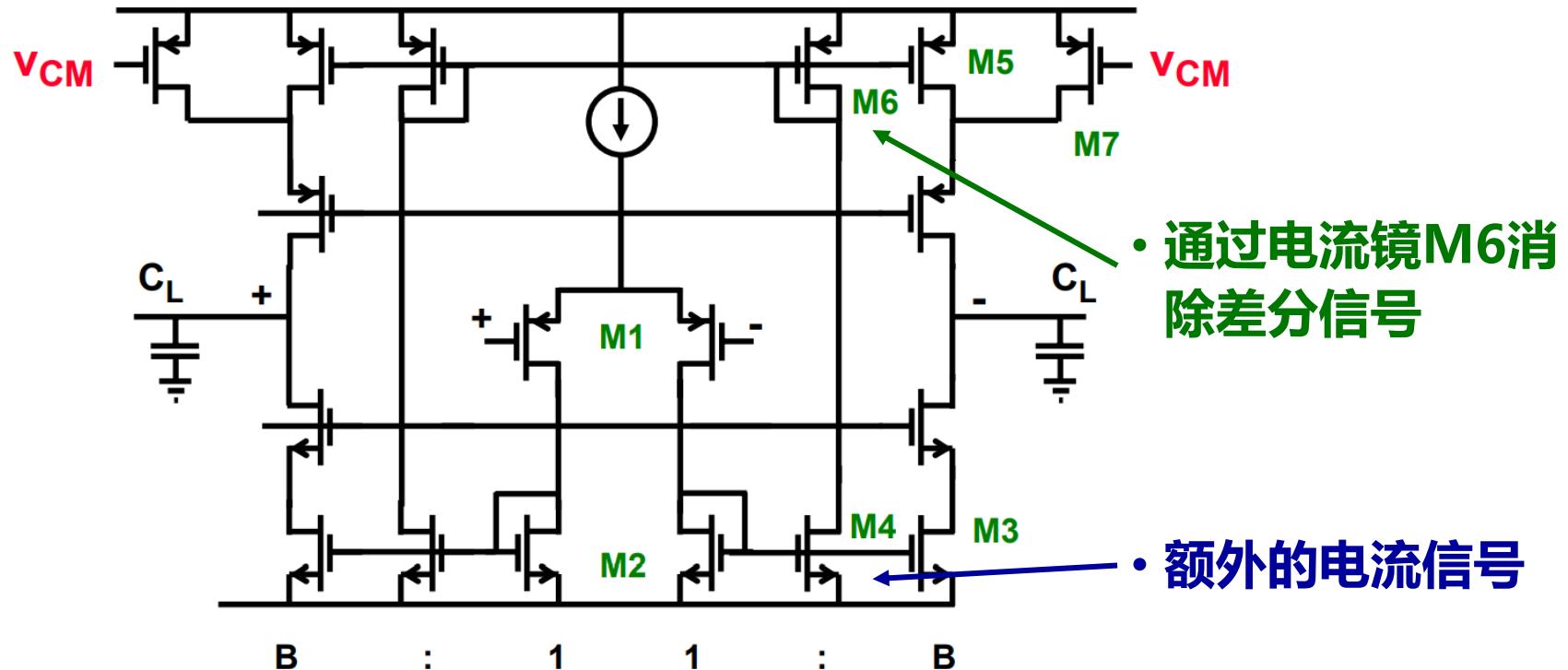
- 基本概念
- 通过线性区晶体管的共模反馈
- 通过误差放大器的共模反馈
- **其他**

》》多级差分系统级联

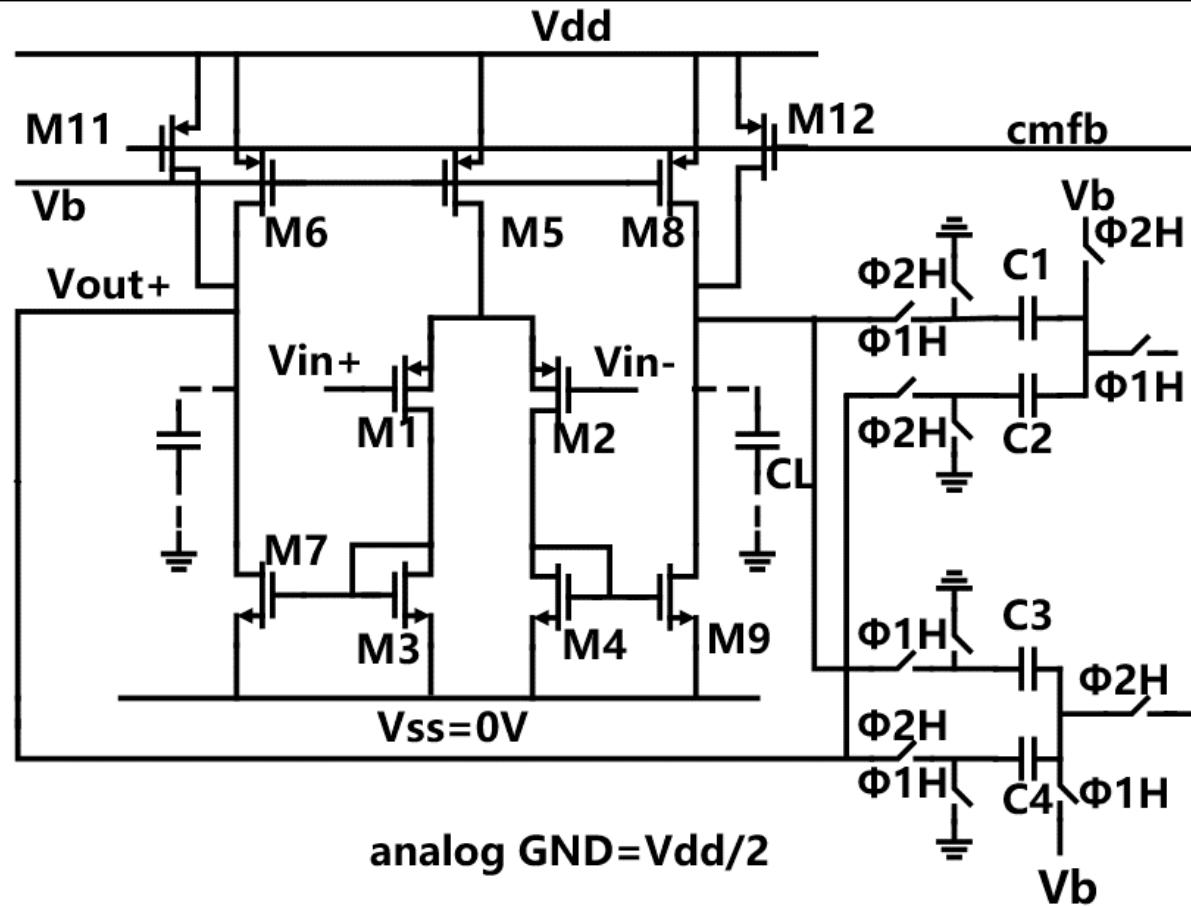


- 级联的两个差分运放可以共用一套共模反馈！

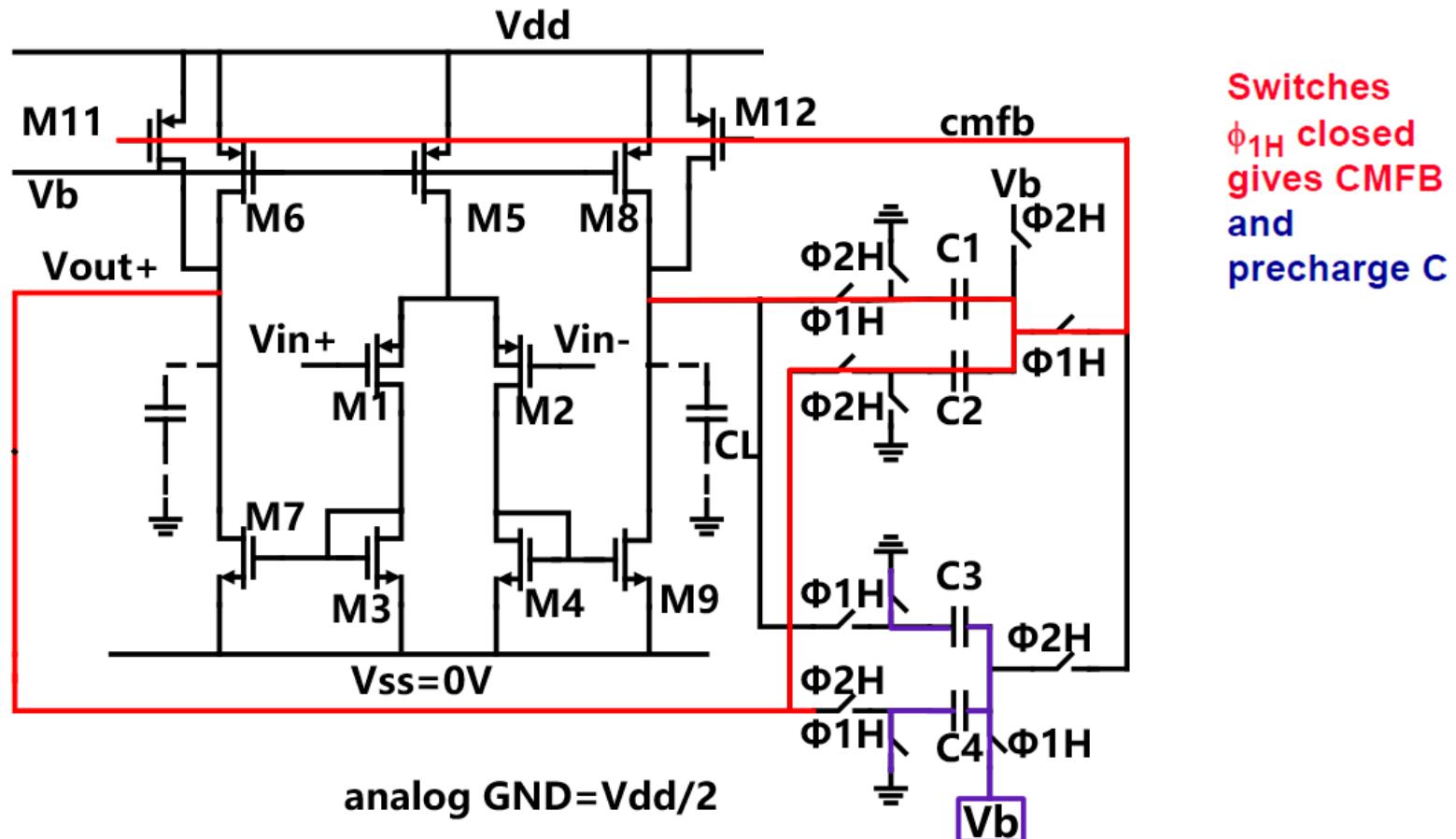
》》 其他共模反馈技术



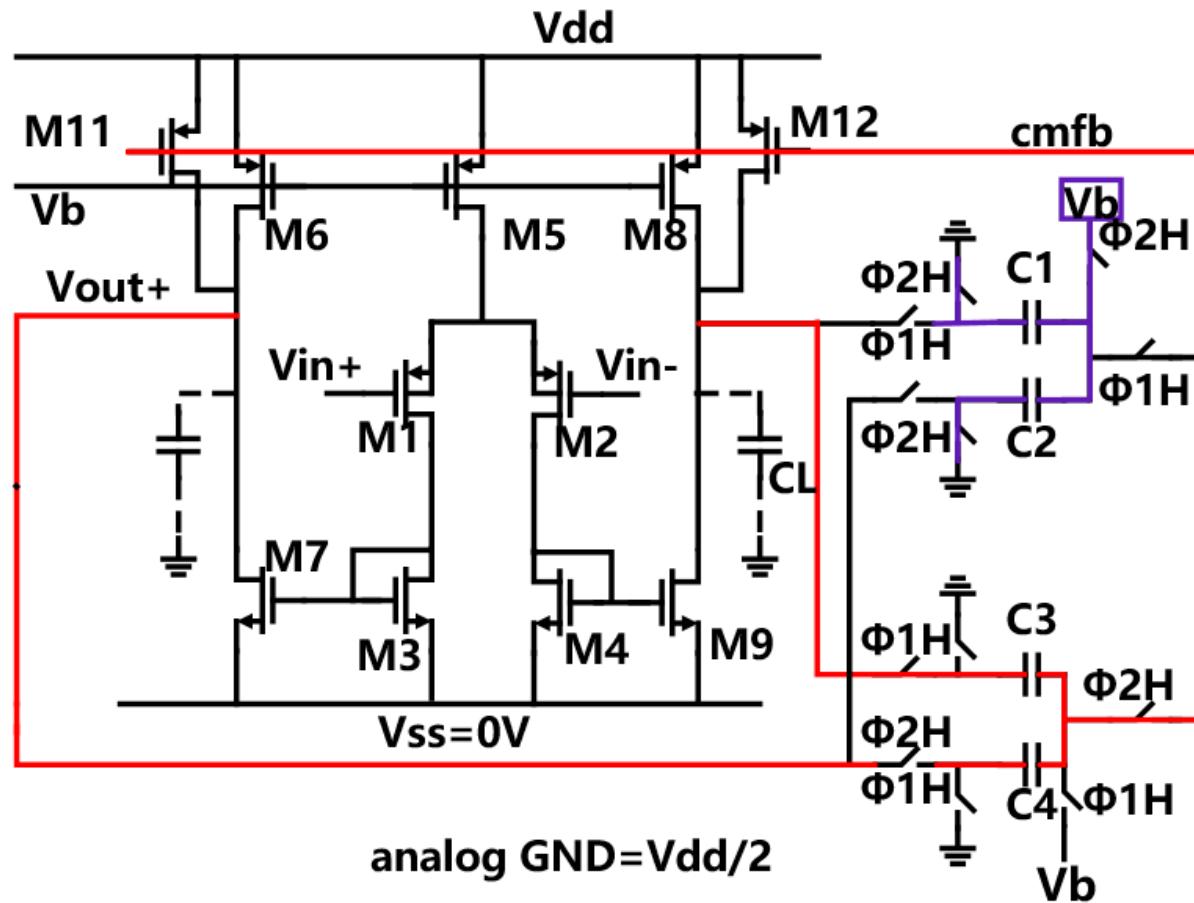
》》 其他共模反馈技术



》》 其他共模反馈技术



》》 其他共模反馈技术

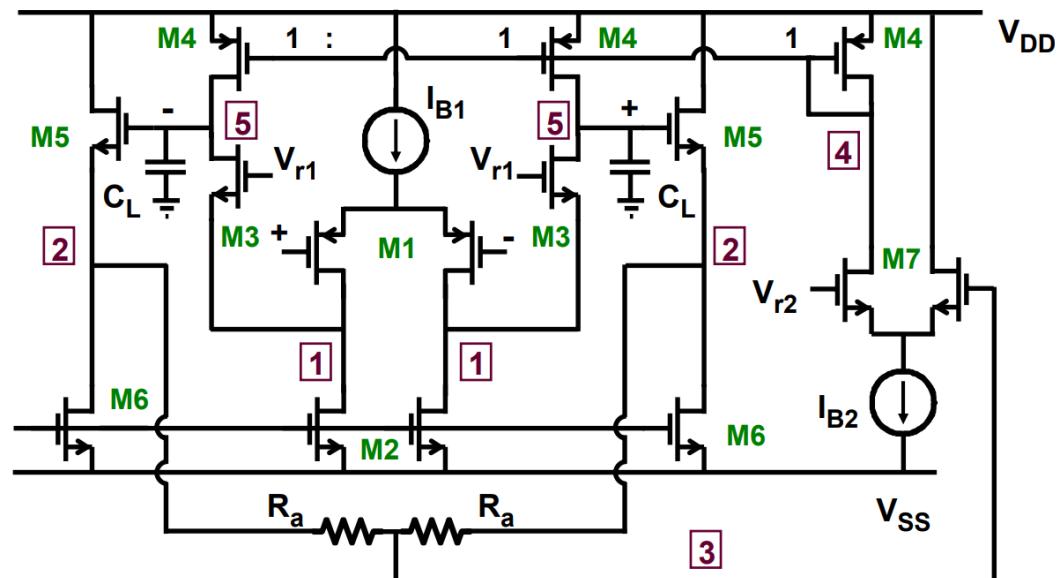


Switches
 Φ_{2H} closed
gives CMFB
and
precharge C

课后习题

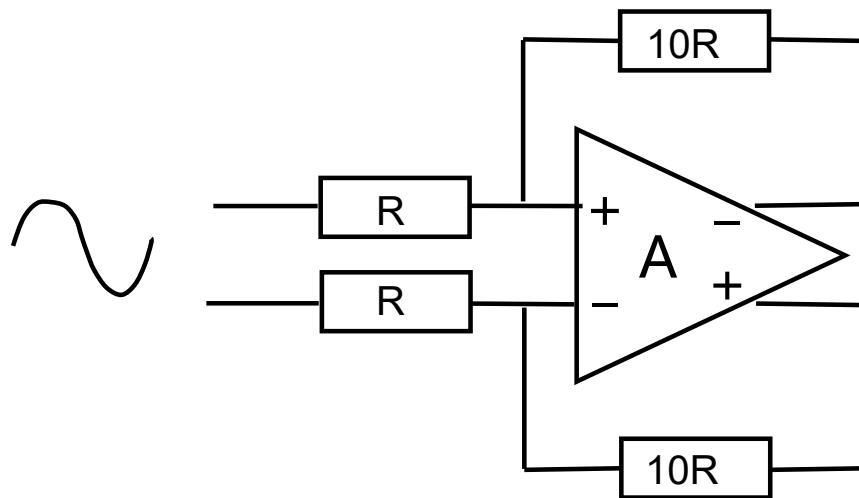
□ 已知要求 $GBW_{DM}=50MHz$, $GBW_{CM}=100MHz$, $C_L=5pF$ 。设计一共模&差模相位裕度均大于70°的运放。通过仿真给出：

- 差模增益
- 功耗
- 共模抑制比CMRR



课后习题

□ 将上述设计的差分运放，通过电阻设置成10倍放大，观察输入差模和共模信号分别有100mVpp, 10kHz的正弦信号时，差模输出信号的大小，并分析是否符合预期。



第8章 轨到轨



CMOS模拟集成电路设计

第七章：运放的高级设计： 轨到轨输入

胡远奇

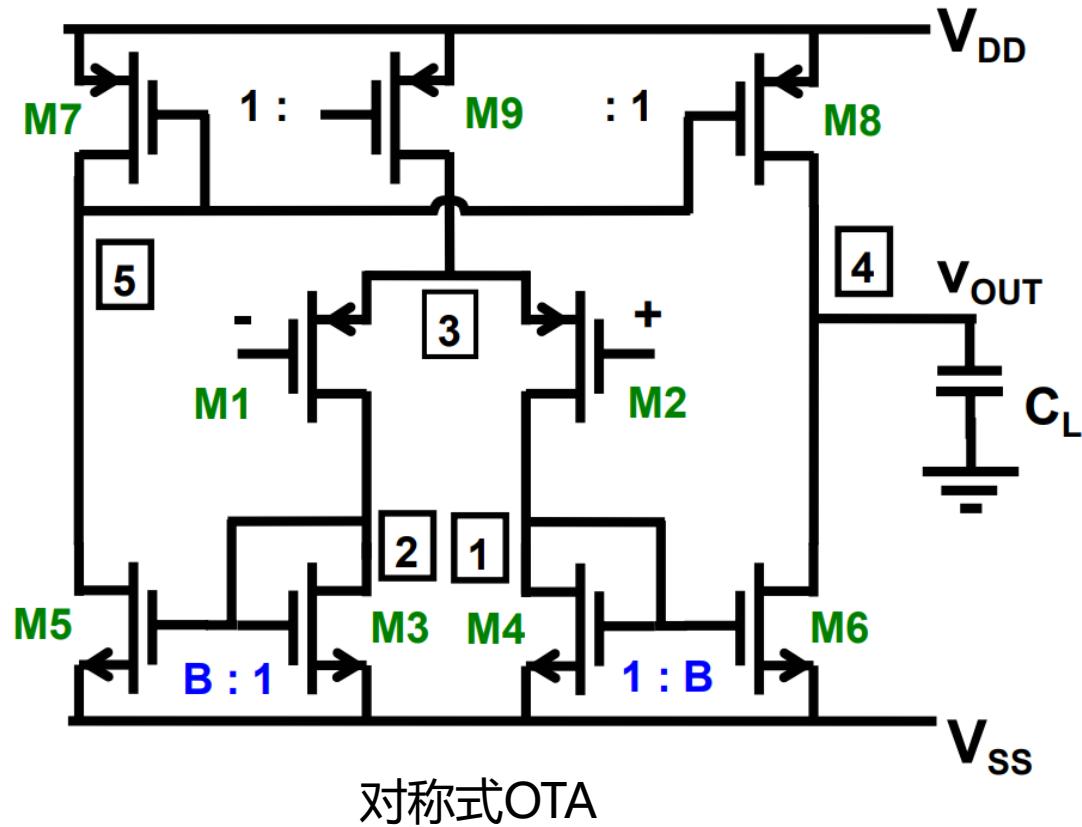
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轨到轨输入

- 为什么需要轨到轨 (Rail-to-Rail) 的输入
- 跨导平衡技术：
 - 3倍电流技术
 - 稳压二极管/齐纳二极管 (Zener Diodes)
 - 亚反型区中的电流调节技术
 - 电流调制技术：反馈调制
 - 超低电源电压中的轨到轨输入技术

》》为什么需要轨到轨输入?



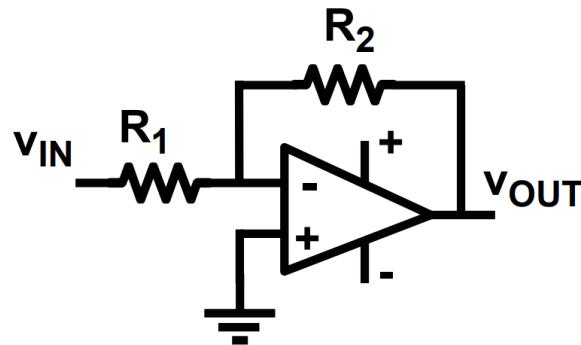
输出范围=?

轨到轨输出!

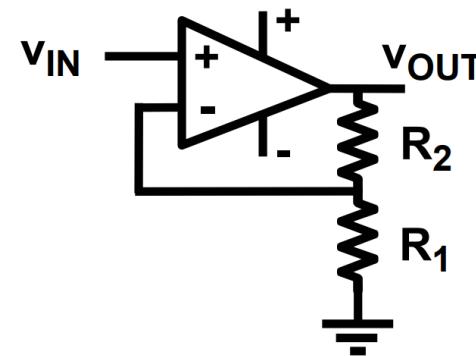
输入范围=?

损失 $V_{GS1} + V_{DSat9}$

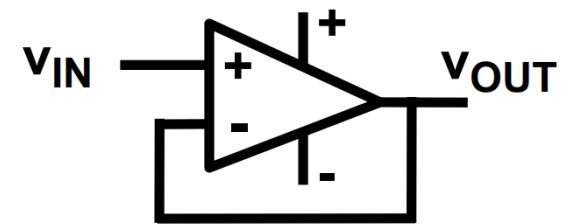
》》何时需要轨到轨输入?



No!

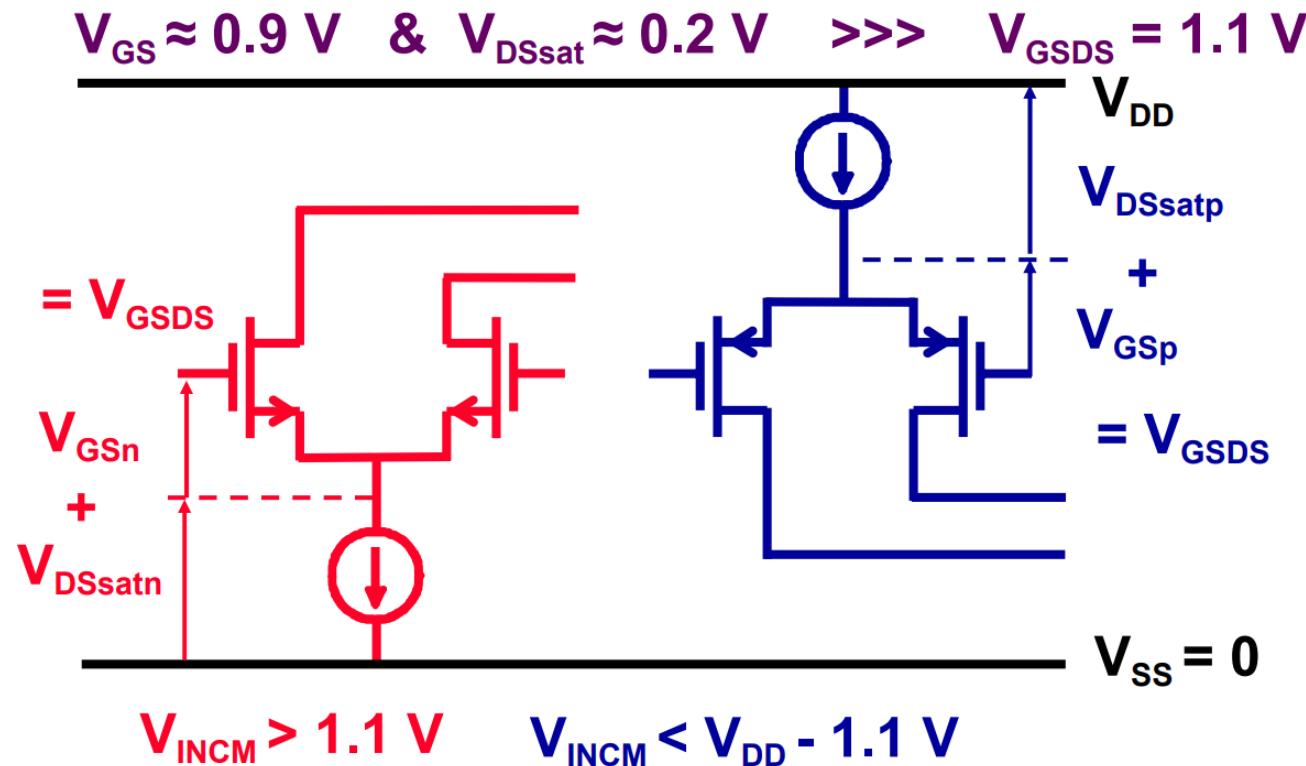


No!



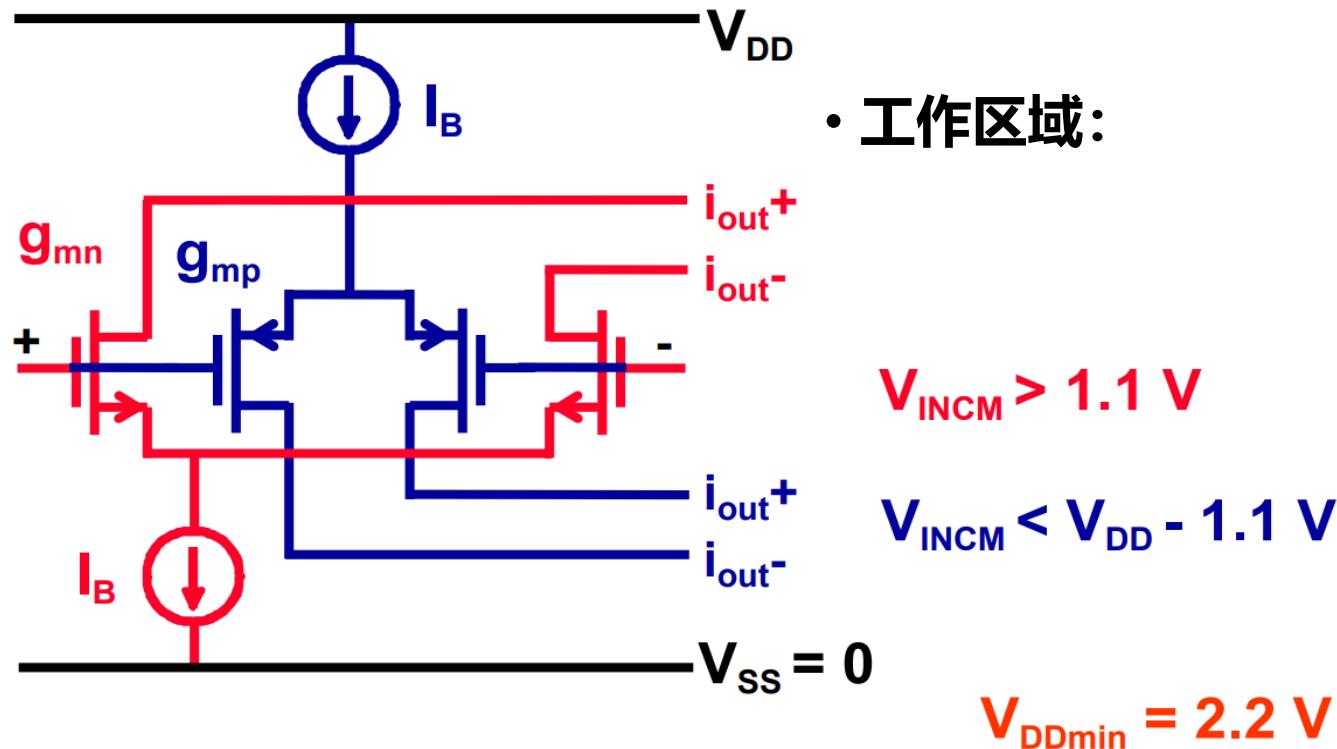
Yes!

》》互补差分对结构



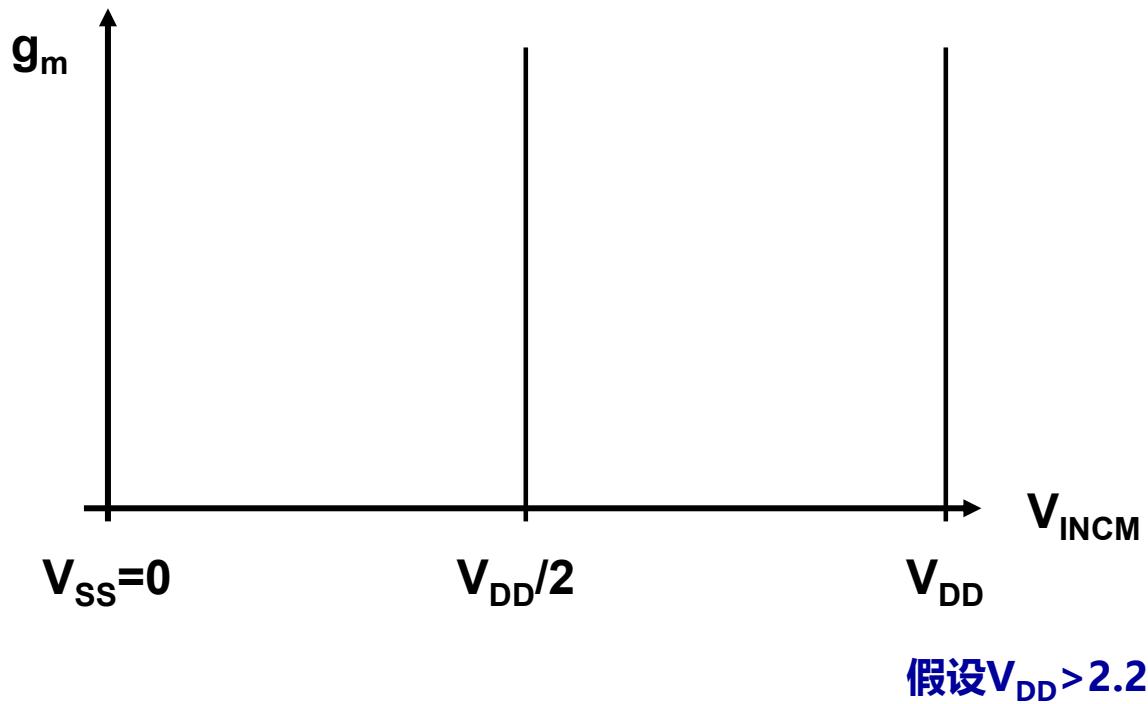
- 互补差分对是轨到轨输入的基本解决思路

》》互补差分对结构

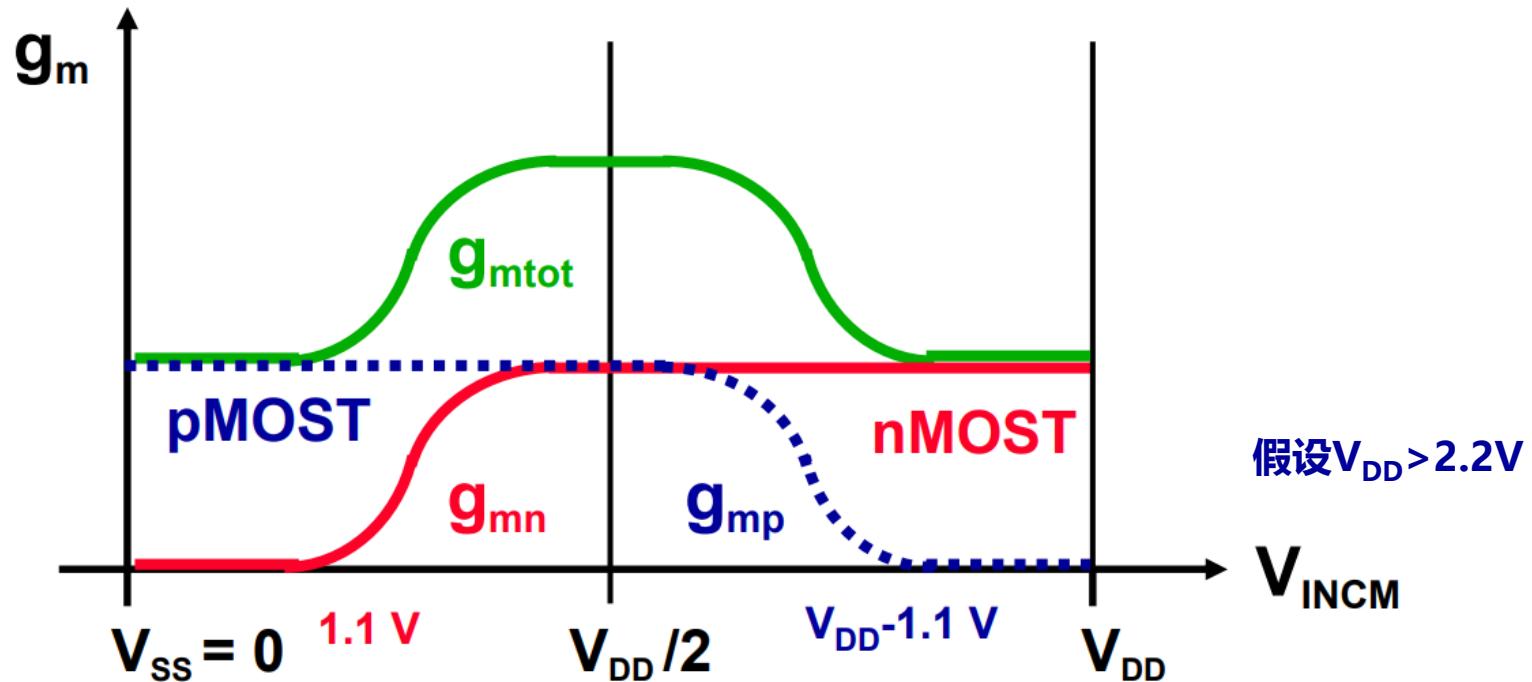


- 当 $VDD > 2.2 \text{ V}$ 时，共模输入范围能够覆盖从 VSS 到 VDD 的全部区域

》》互补差分对结构：挑战

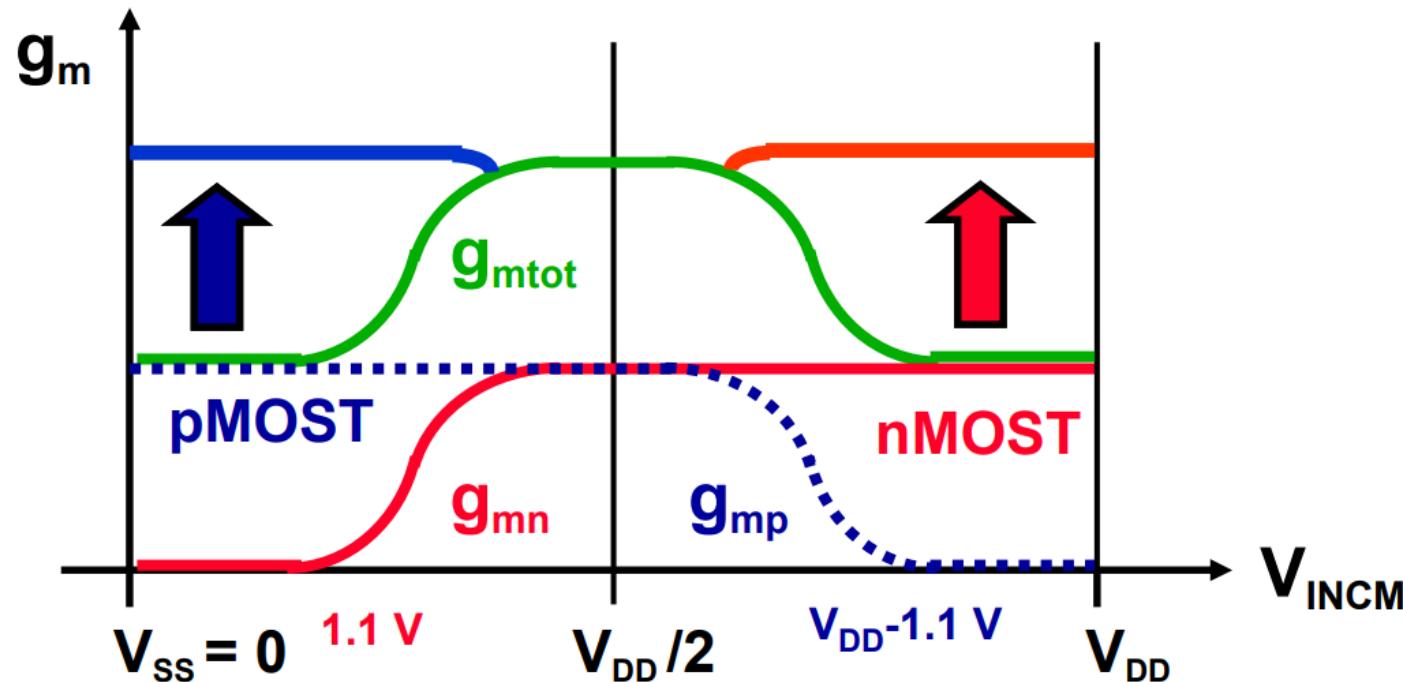


》》互补差分对结构：挑战



- 当VCM接近电源上下限时，只有一组差分对导通！
- 变化的跨导gm会导致大量的非线性失真！

》》互补差分对结构：挑战



- **解决方案：**提升两边区域的跨导，使得总跨导恒定

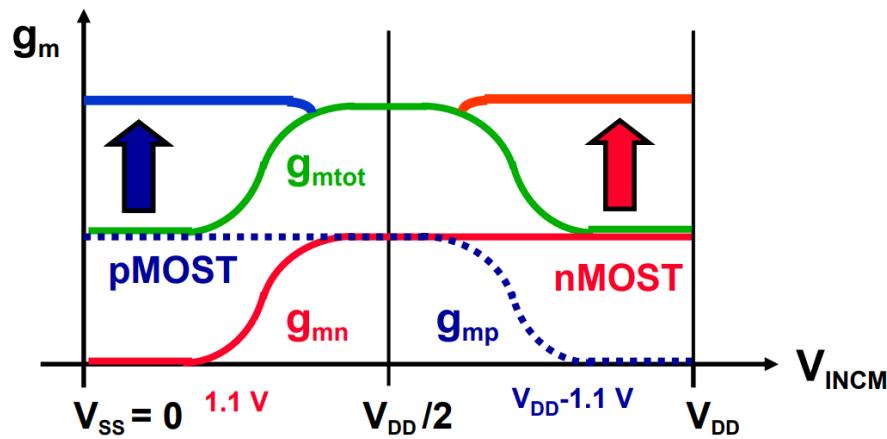


轨到轨输入

- 为什么需要轨到轨 (Rail-to-Rail) 的输入
- 跨导平衡技术：
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 - 电流调制技术：反馈调制
 - 超低电源电压中的轨到轨输入技术

》》跨导补偿技术

$$g_{mN} + g_{mP} = \text{Constant}$$



$$g_m \approx \mu_0 C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) = \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_{DS}} = \frac{2I_{DS}}{V_{GS} - V_{TH}}$$

》》跨导补偿技术

NMOS

$$g_{mn} + g_{mp} = ct1$$

PMOS

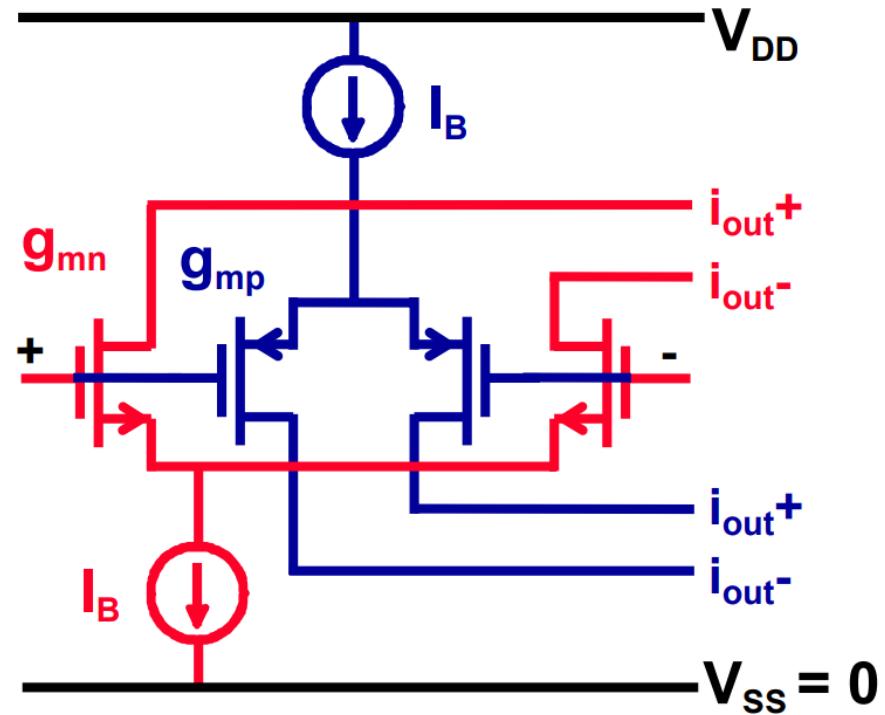
$$\sqrt{2 K'_n \frac{W_n}{L_n} I_{Bn}} + \sqrt{2 K'_p \frac{W_p}{L_p} I_{Bp}} = ct1$$

$$\sqrt{K'_n I_{Bn}} + \sqrt{K'_p I_{Bp}} = ct2$$

$$\sqrt{I_{Bn}} + \sqrt{I_{Bp}} = ct3$$

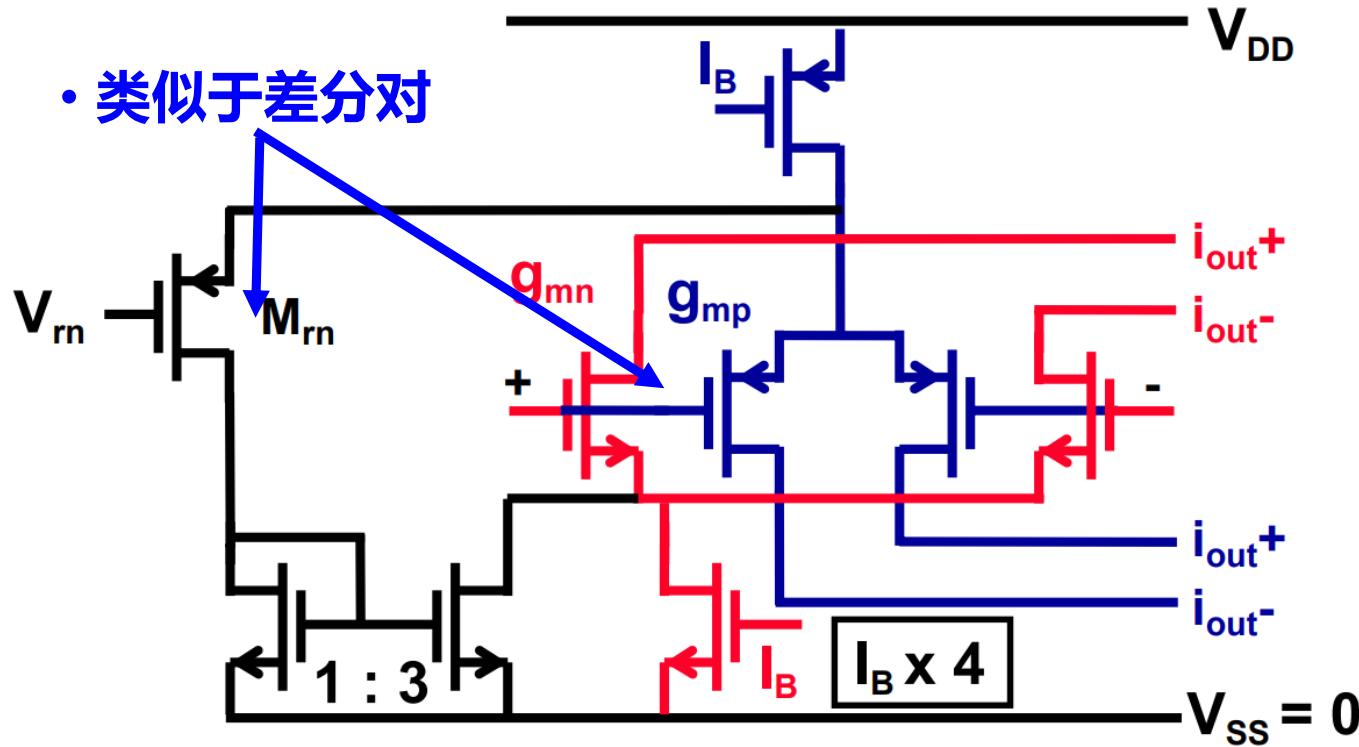
1. 令NMOS和PMOS的跨导**相同**
2. 在近轨区域，令NMOS/PMOS的跨导**翻倍**
3. 需要额外**3倍**的电流

》》跨导补偿技术



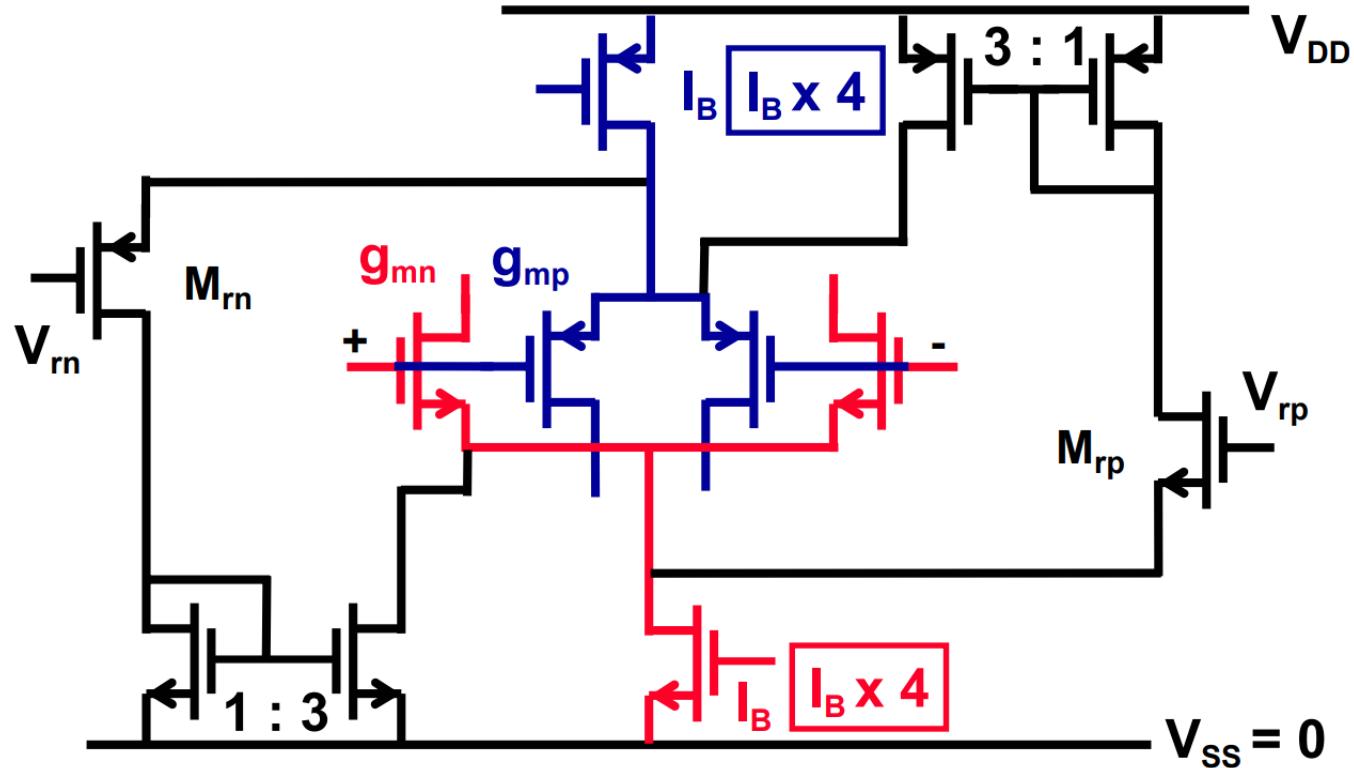
- 如何自适应的调整偏置电流?

》》跨导补偿技术



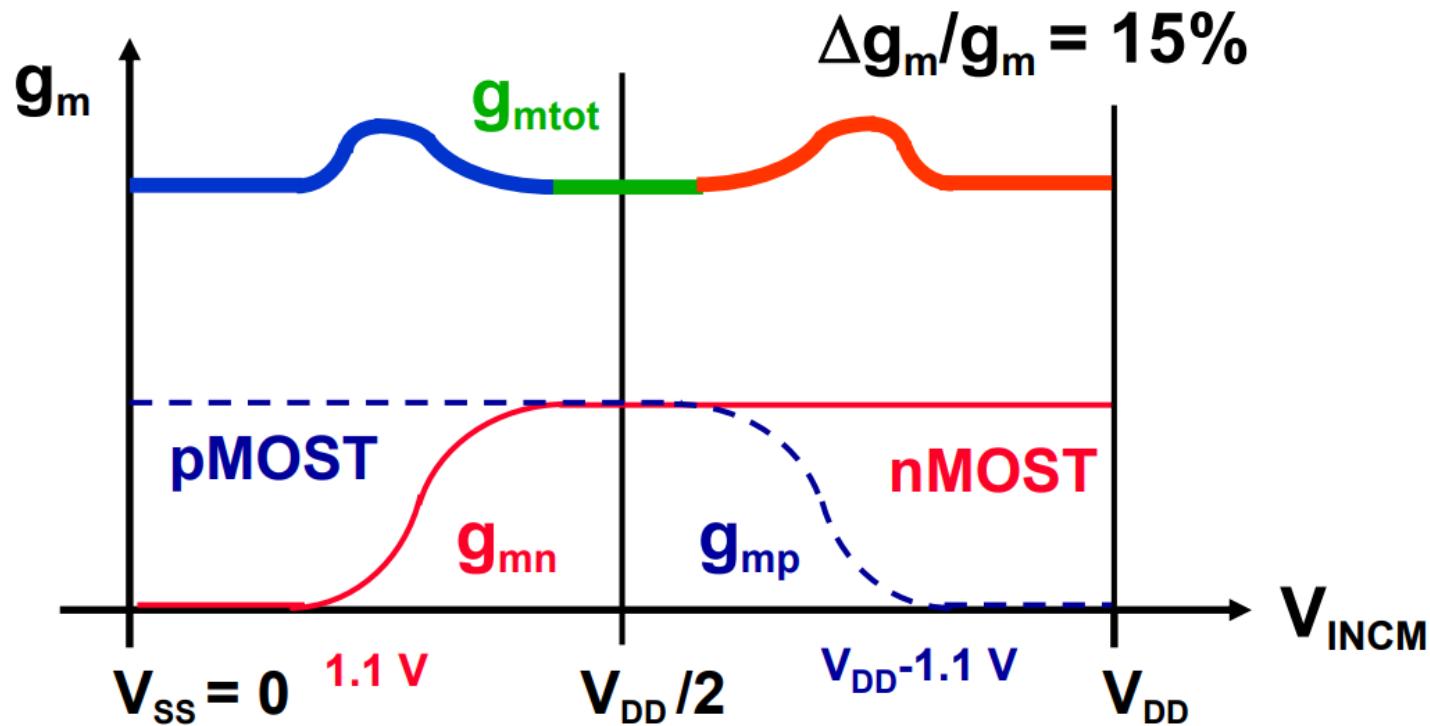
- 分流控制电压 V_{rn} 决定PMOS偏置电流何时进入3x电流镜

》》跨导补偿技术



- 互补型的3x电流镜方案

》》 3x 电流镜的平滑性



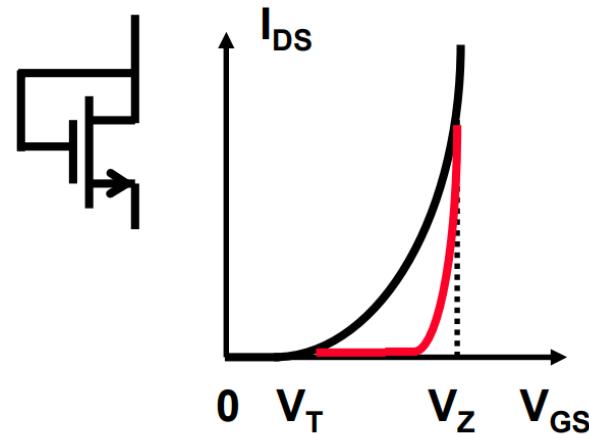
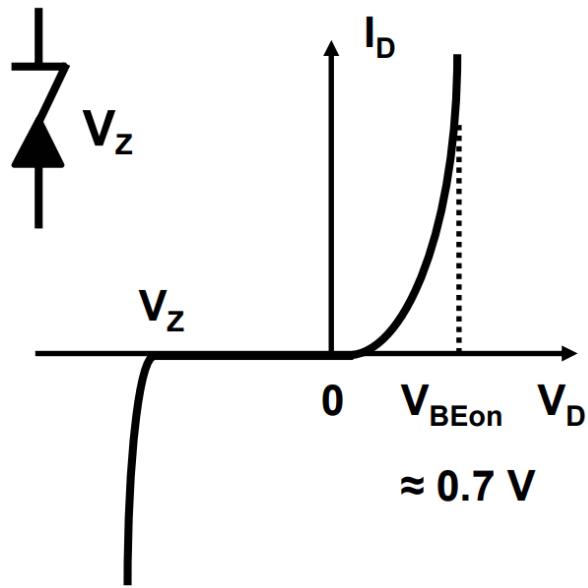
$$g_{m\text{tot}} \sim \sqrt{(4 - 3x) I_B} + \sqrt{x I_B} \quad \Delta g_m/g_m = 15\% \quad (x=1/3)$$



轨到轨输入

- 为什么需要轨到轨 (Rail-to-Rail) 的输入
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 - 电流调制技术：反馈调制
 - 超低电源电压中的轨到轨输入技术

》》 稳压二极管



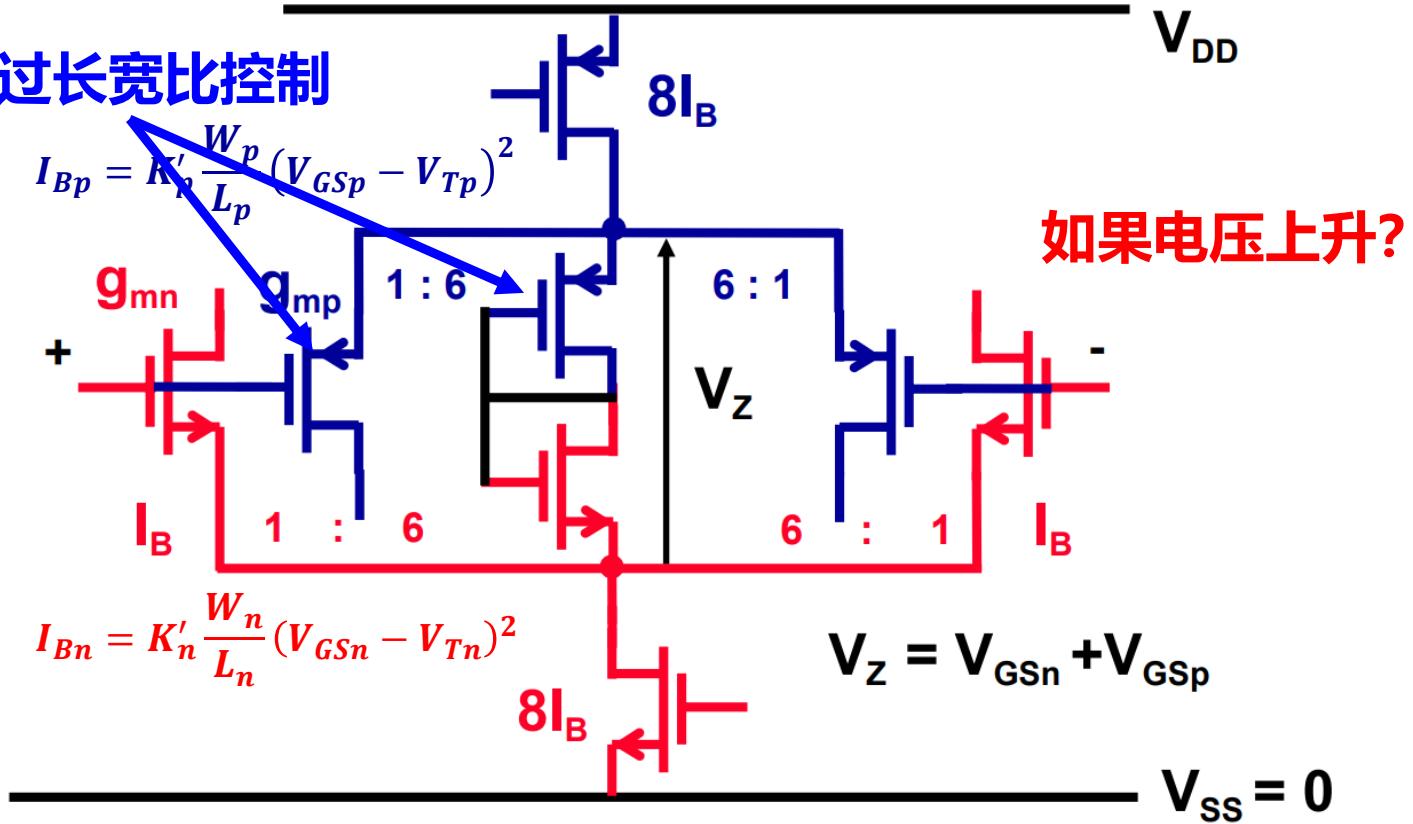
Electronic Zener

- 利用PN结反向击穿状态，其**电流**可在很大范围内**变化**，而**电压**基本**不变**

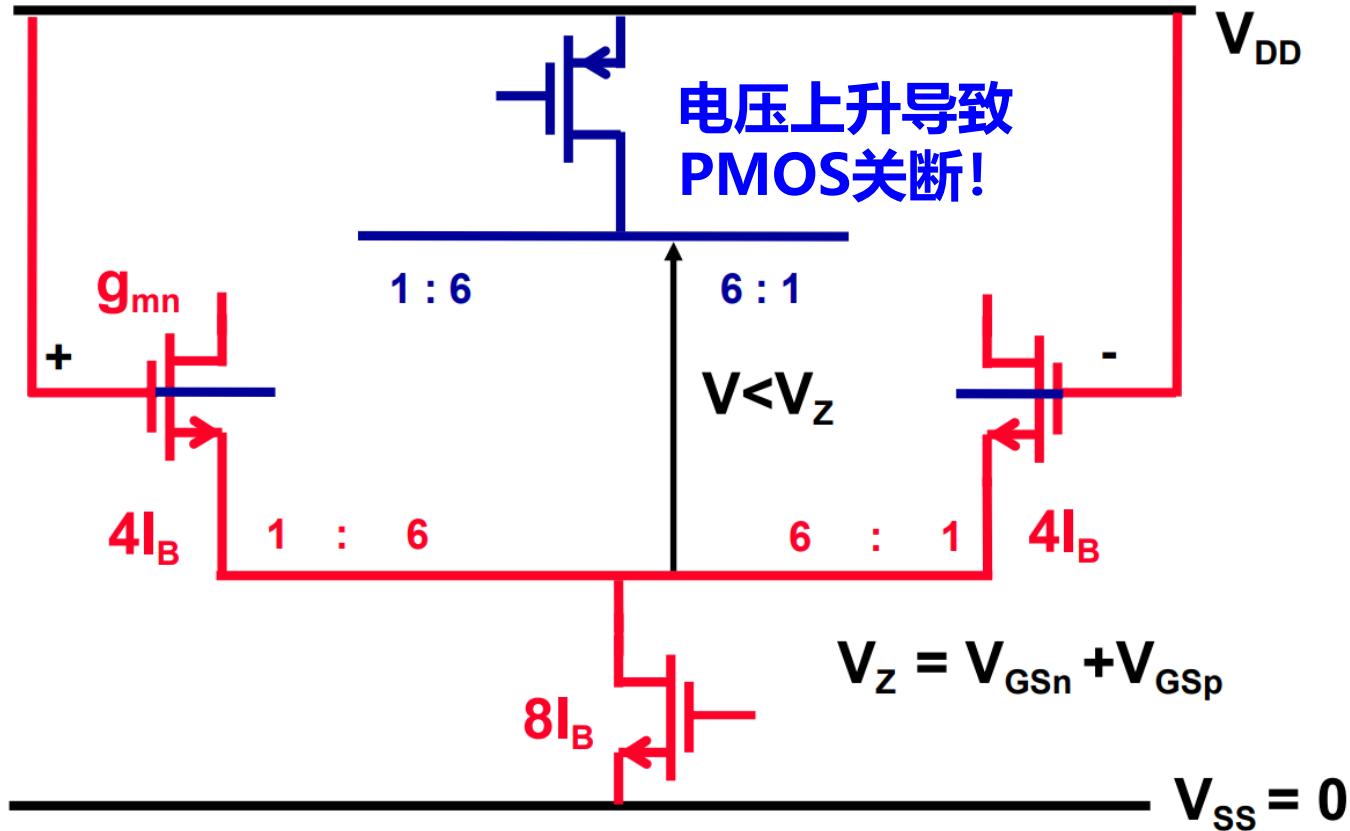
- 单一二极管连接的三极管无法提供突变的V-I曲线
- 多晶体管组合形成**电子稳压二极管**

通过稳压二极管的跨导补偿

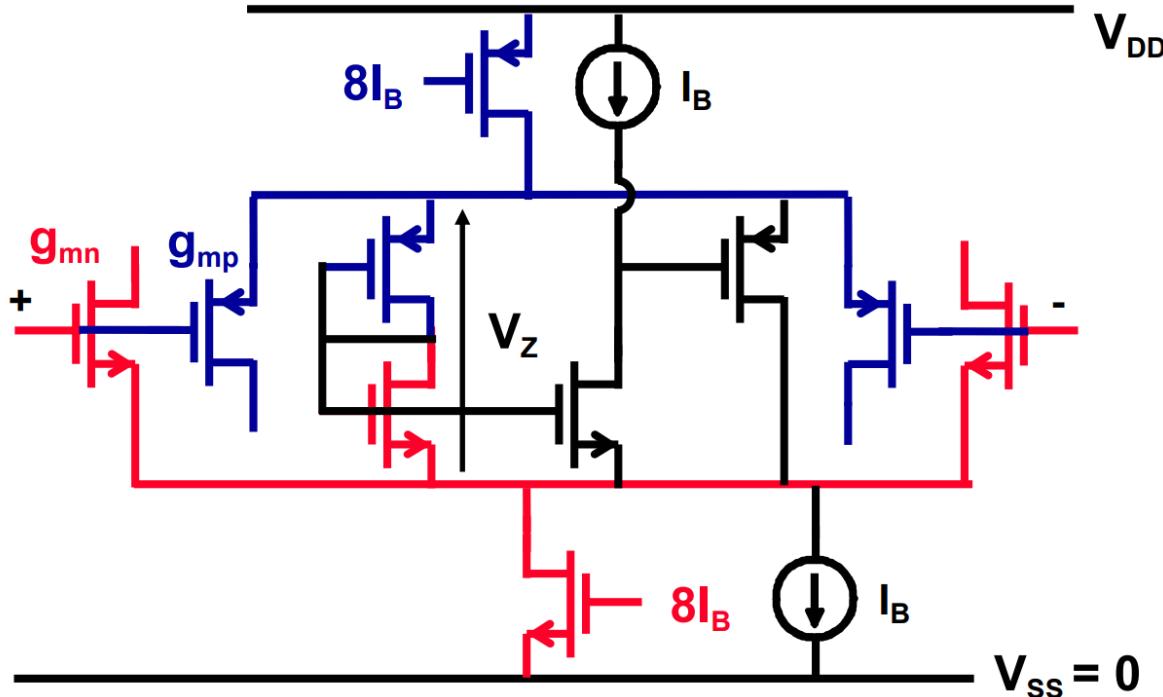
- 通过长宽比控制



通过稳压二极管的跨导补偿

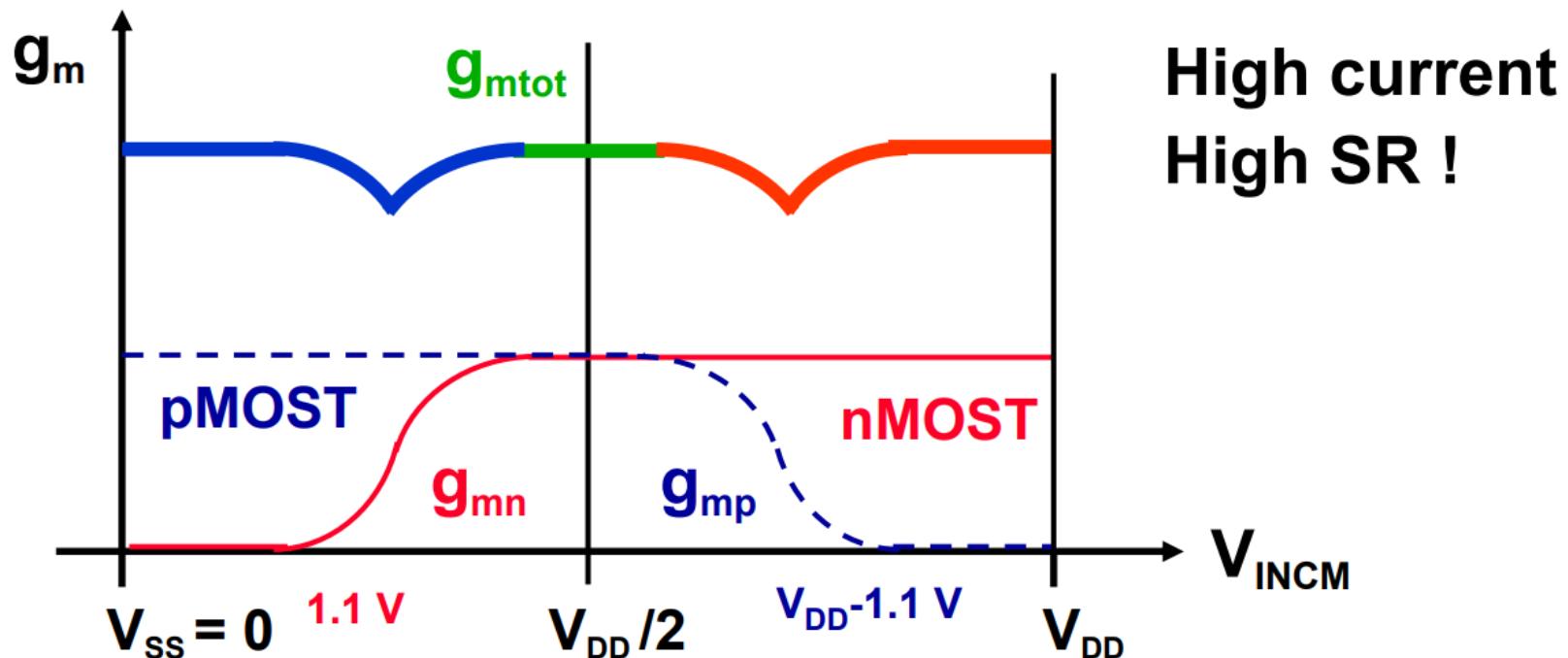


通过稳压二极管的跨导补偿



- 通过运放和源极跟随器加快电压的变化
- 该组合是正反馈还是负反馈？

》》通过稳压二极管的跨导补偿



双晶体管串联: $\Delta g_m/g_m = 25\%$ 正反馈运放: $\Delta g_m/g_m = 6\%$



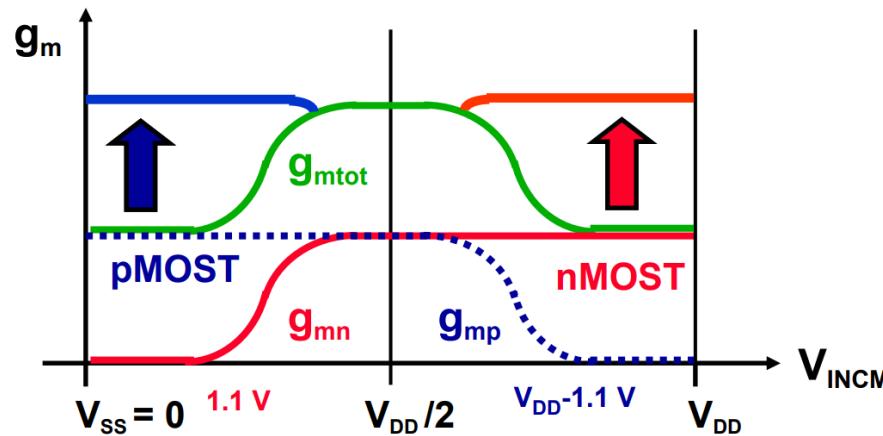
轨到轨输入

- 为什么需要轨到轨 (Rail-to-Rail) 的输入
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 - 超低电源电压中的轨到轨输入技术



亚反型区中的跨导平衡

$$g_{mN} + g_{mP} = \text{Constant}$$



$$g_{m,wi} = \frac{I_{D,wi}}{nkT/q}$$

》》 亚反型区中的跨导平衡

NMOS

$$g_{mn} + g_{mp} = ct$$

$$\frac{I_{Bn}}{n_n kT/q} + \frac{I_{Bp}}{n_p kT/q} = ct$$

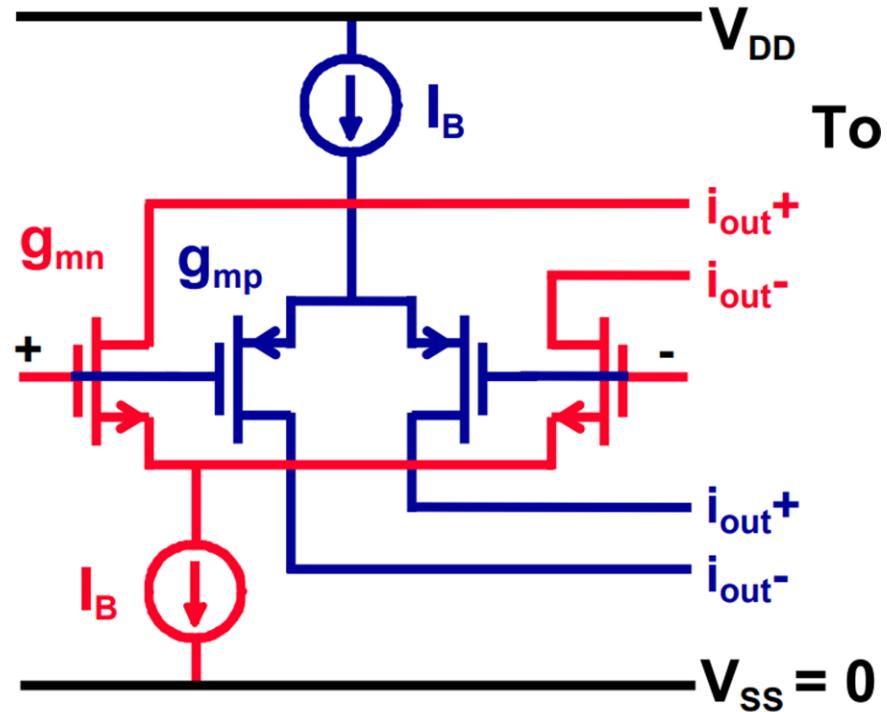
$$I_{Bn} + \frac{n_n}{n_p} I_{Bp} = ct$$

$$n = 1 + \frac{C_D(V_{BS})}{C_{ox}}$$

- 系数 n_n 和 n_p 不同，且随偏置电压变化而变化

》》 亚反型区中的跨导平衡

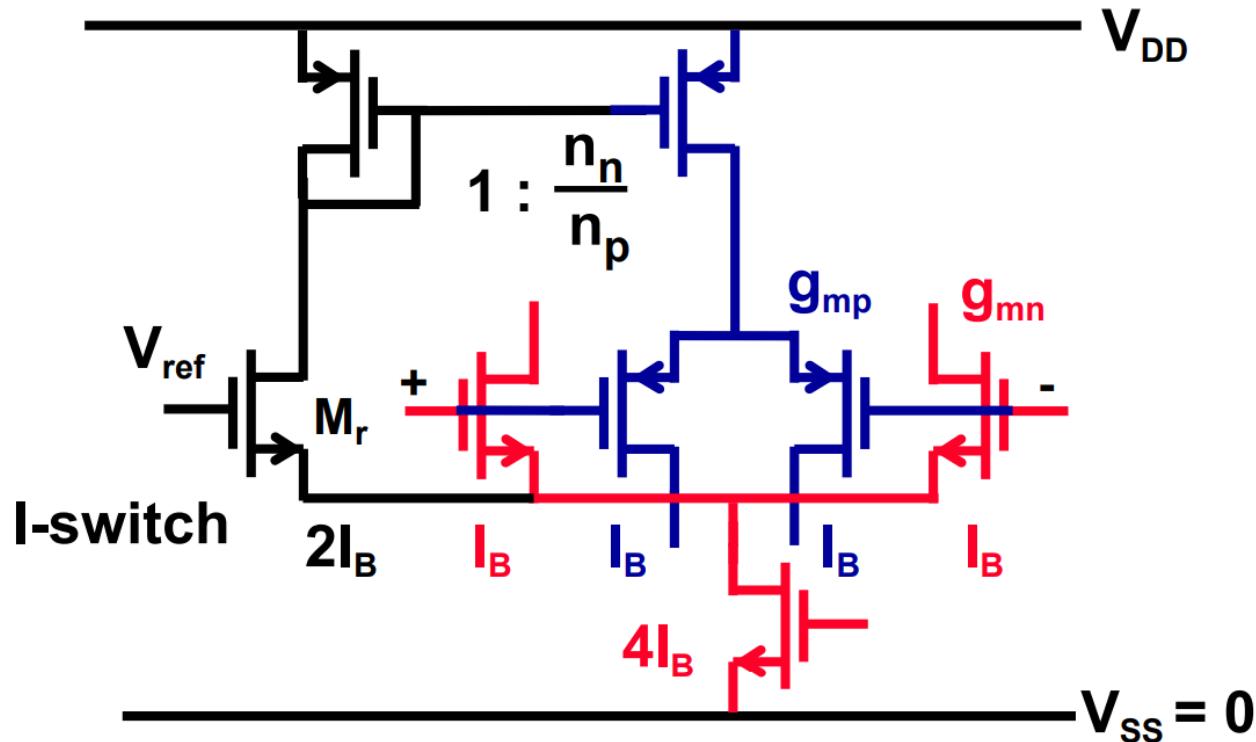
$$\frac{I_{Bn}}{n_n kT/q}$$
$$\frac{I_{Bp}}{n_p kT/q}$$



- 如何自适应的调整偏置电流?

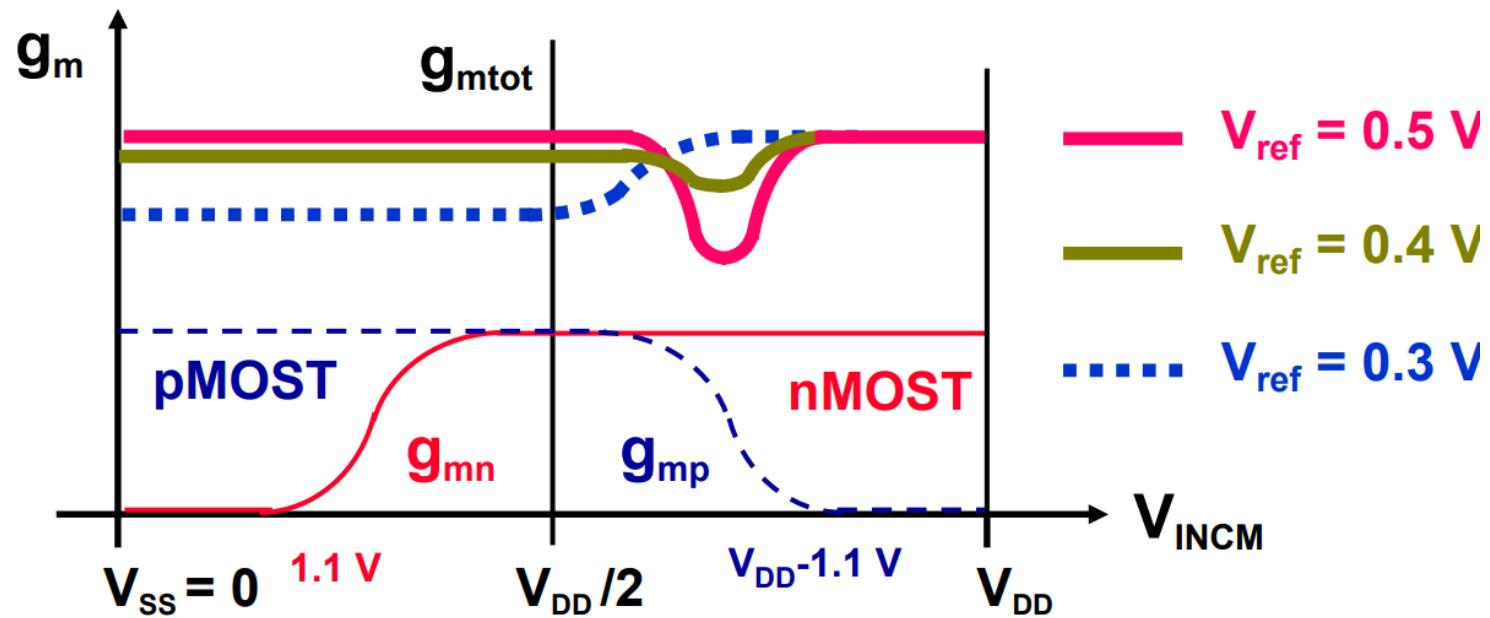


亚反型区中的跨导平衡



- 要求共模输入接近 V_{ref}

》》 亚反型区中的跨导平衡



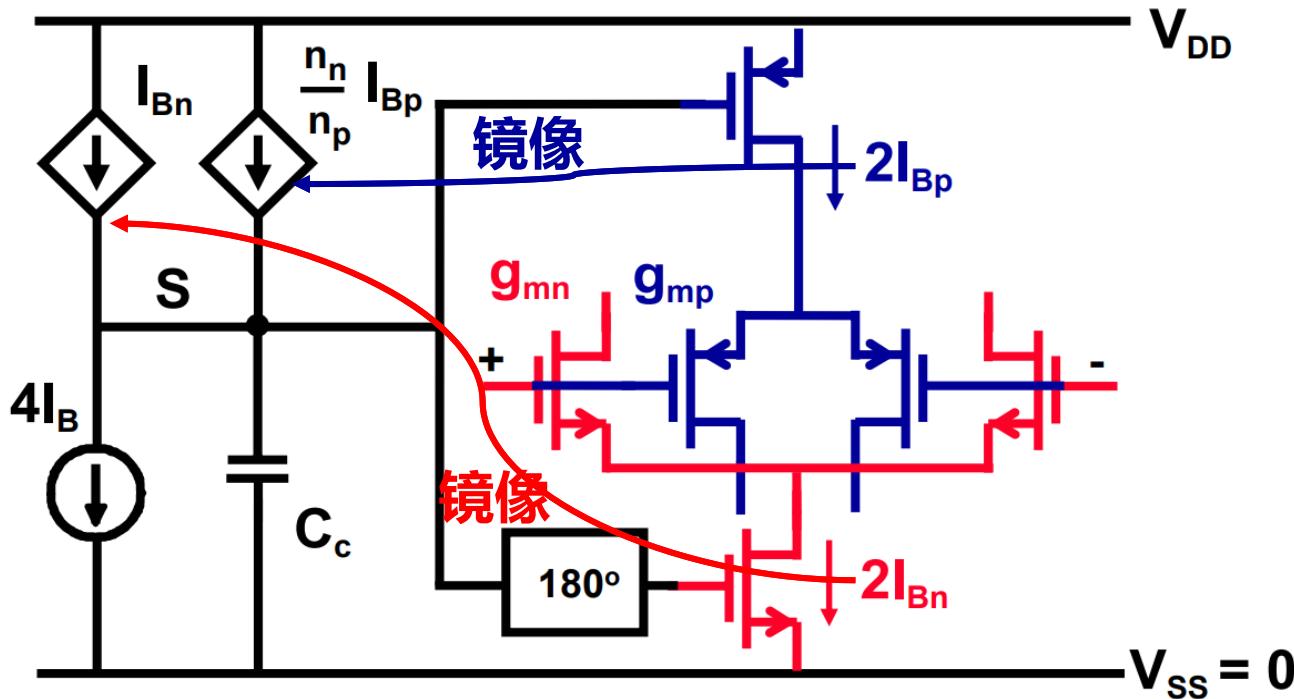
Current switch : V_{ref} very critical !



轨到轨输入

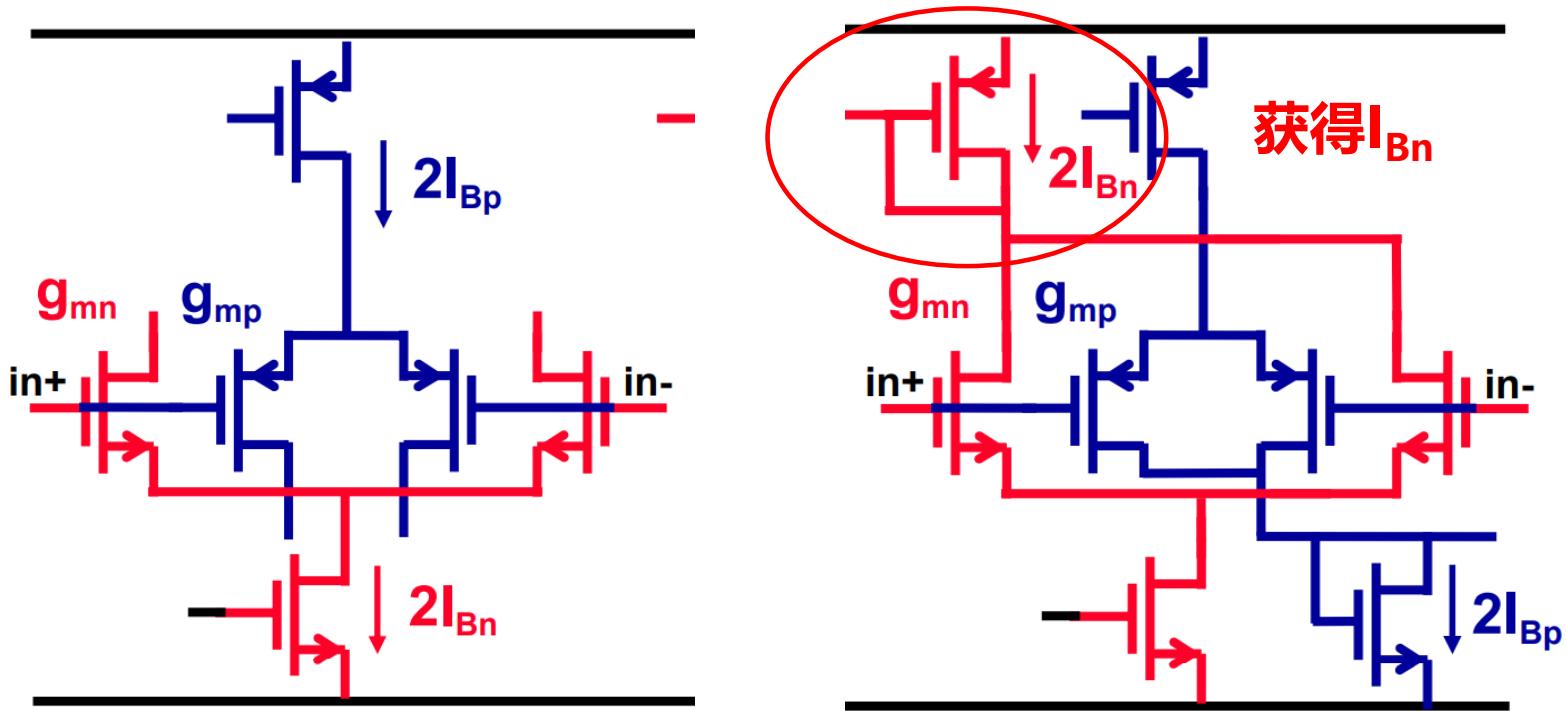
- 为什么需要轨到轨 (Rail-to-Rail) 的输入
- **跨导平衡技术：**
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- 超低电源电压中的轨到轨输入技术

» 电流调制技术：反馈调制



- 通过反馈使得跨导总和不变！

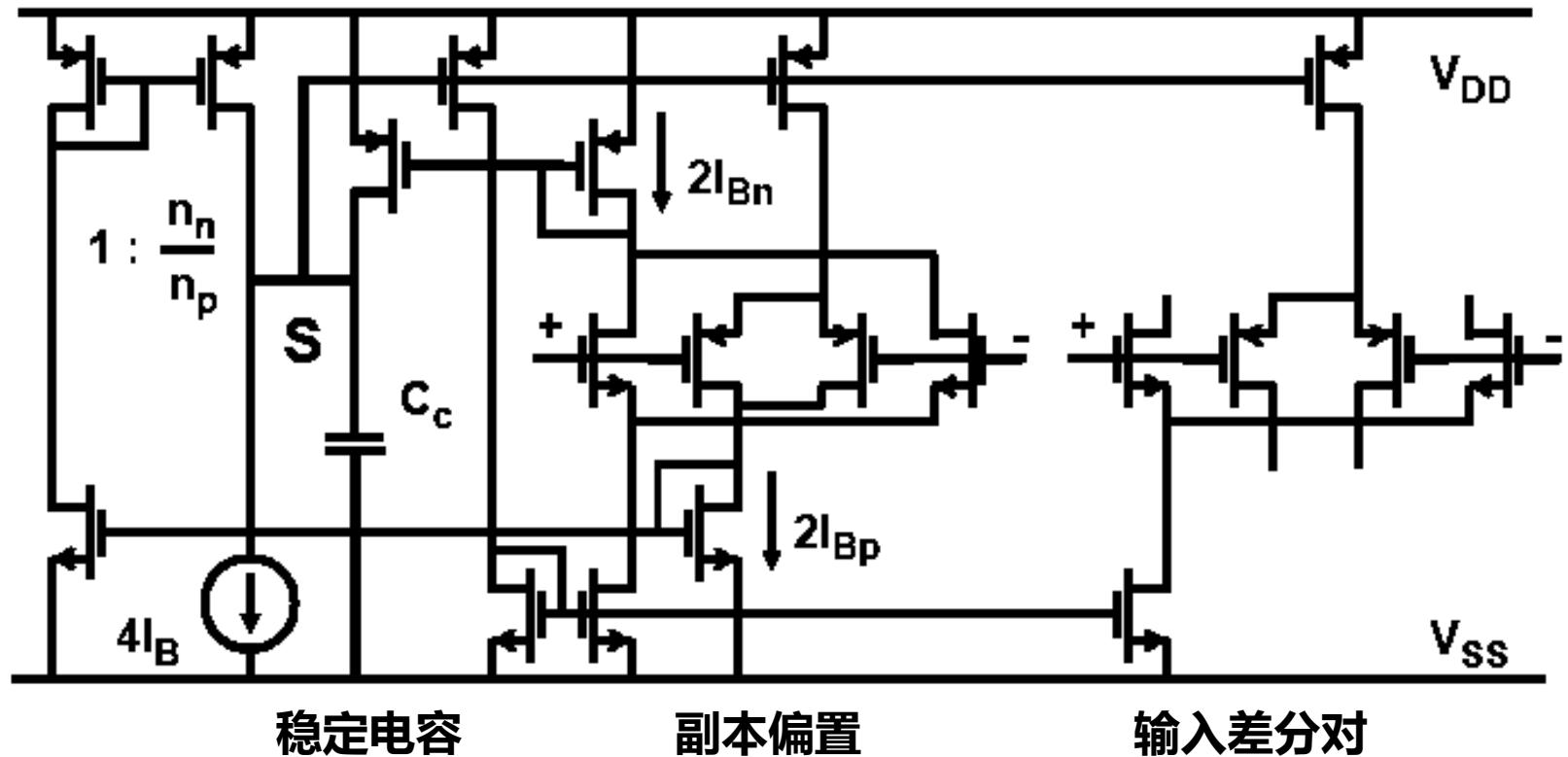
» 电流调制技术：反馈调制



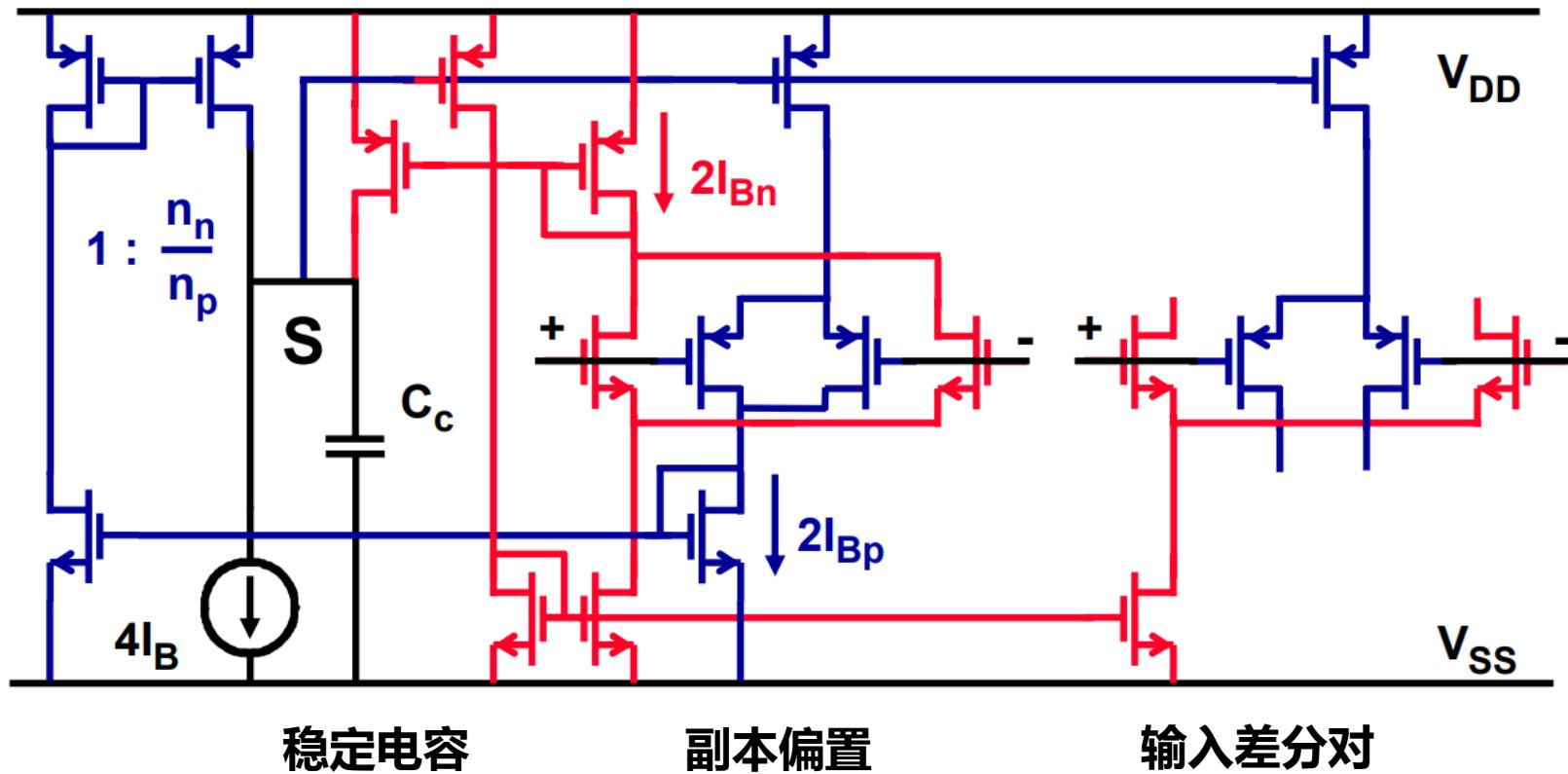
• 如何测量到 I_{Bp} 和 I_{Bn} ?

→ 使用副本 (Replica)

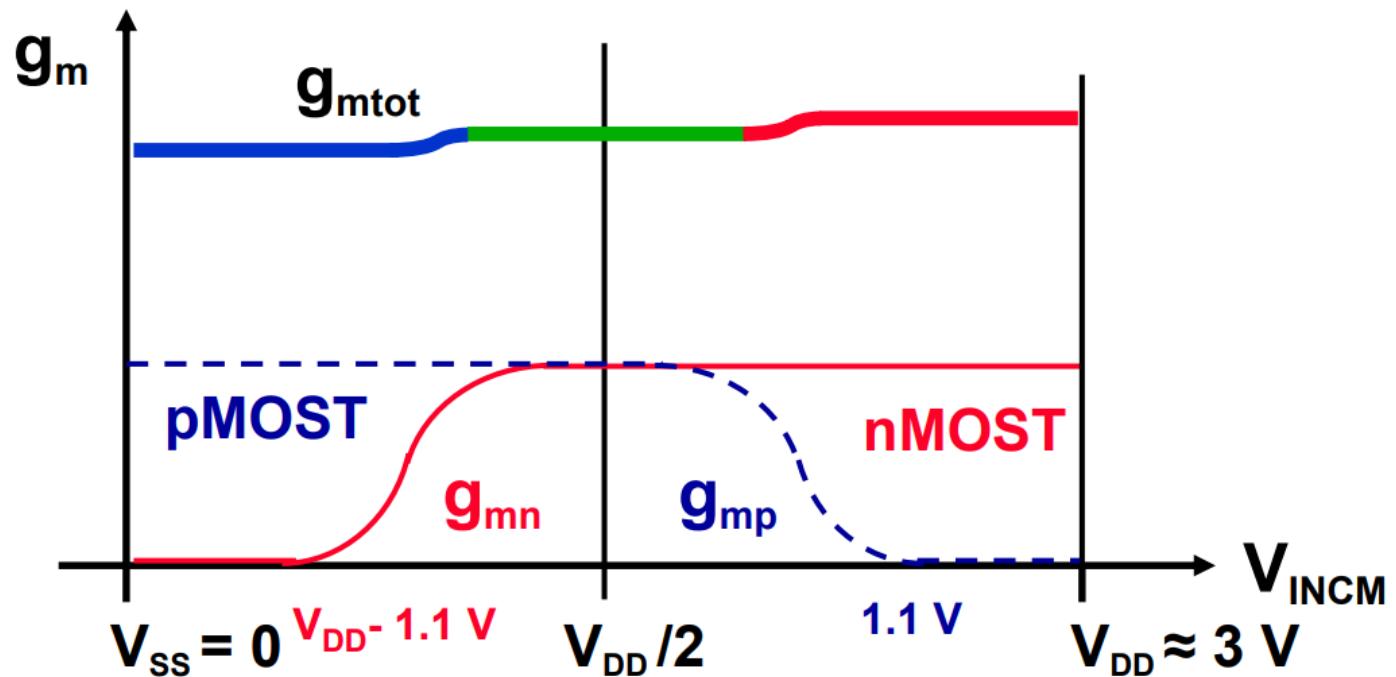
》》 电流调制技术：反馈调制



》》 电流调制技术：反馈调制

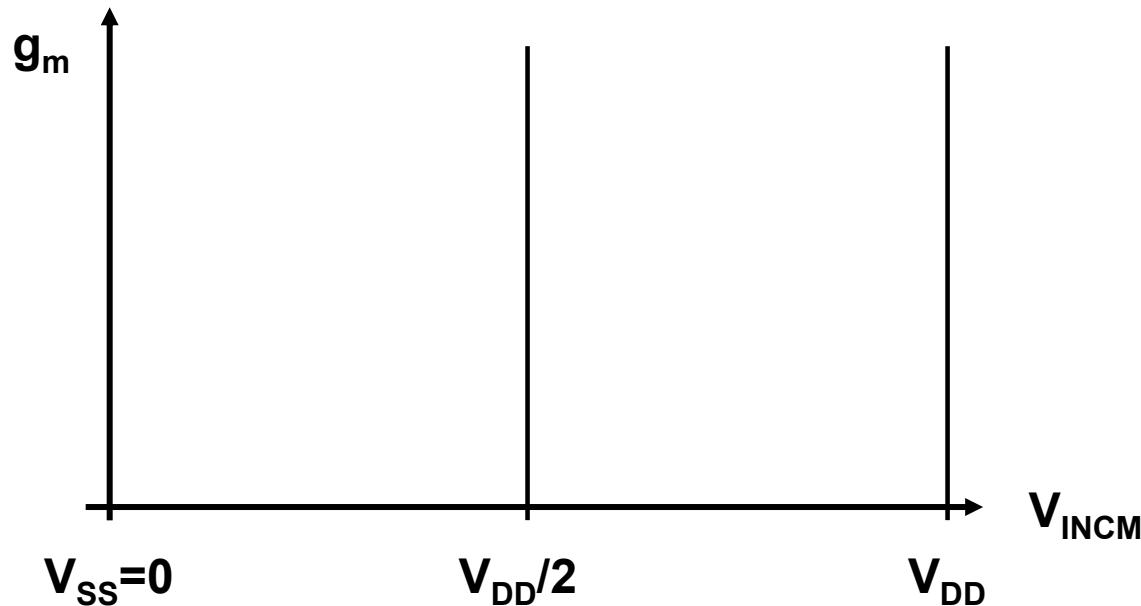


》》 反馈调制的性能



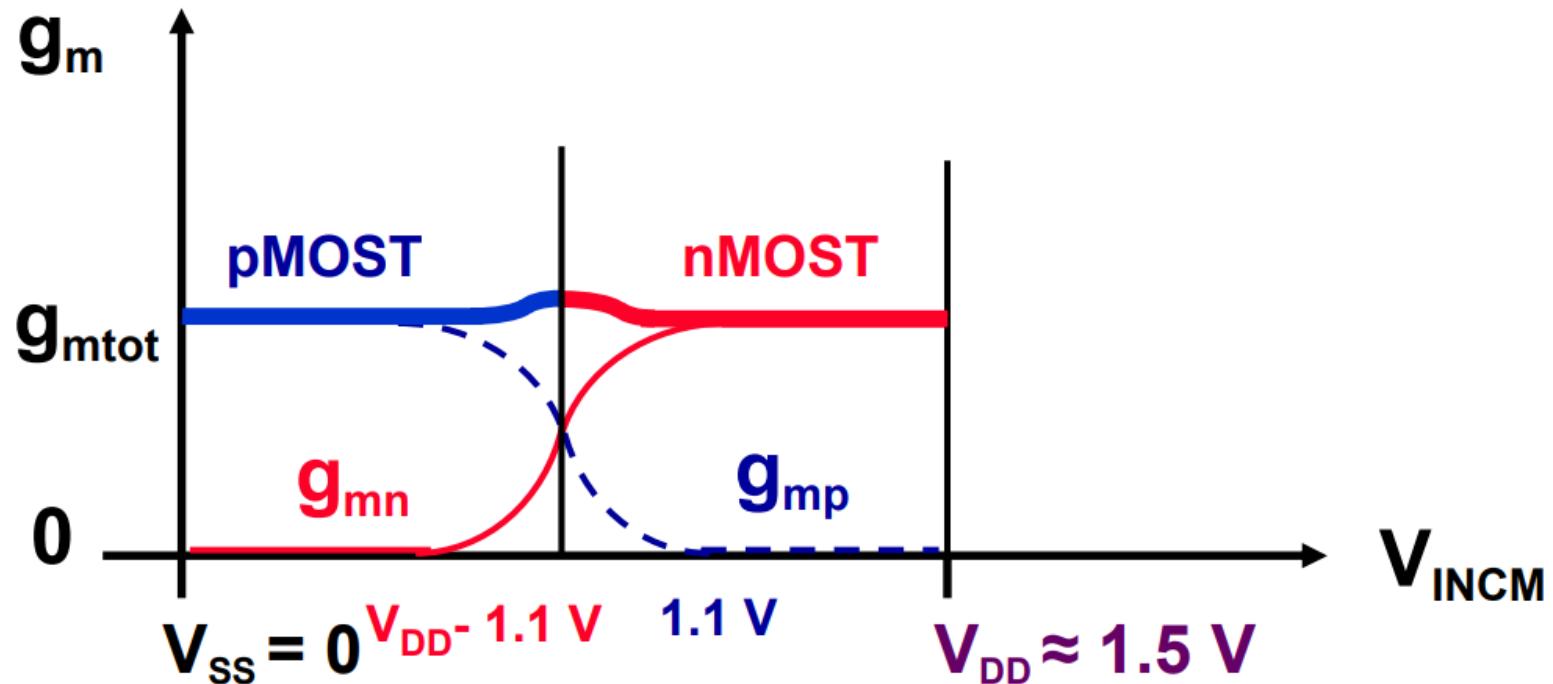
由于亚反型区中反型系数n的偏差： $\Delta g_m/g_m \approx 4\%$ 由反型系数n的不匹配造成

»» 互补差分对结构：挑战



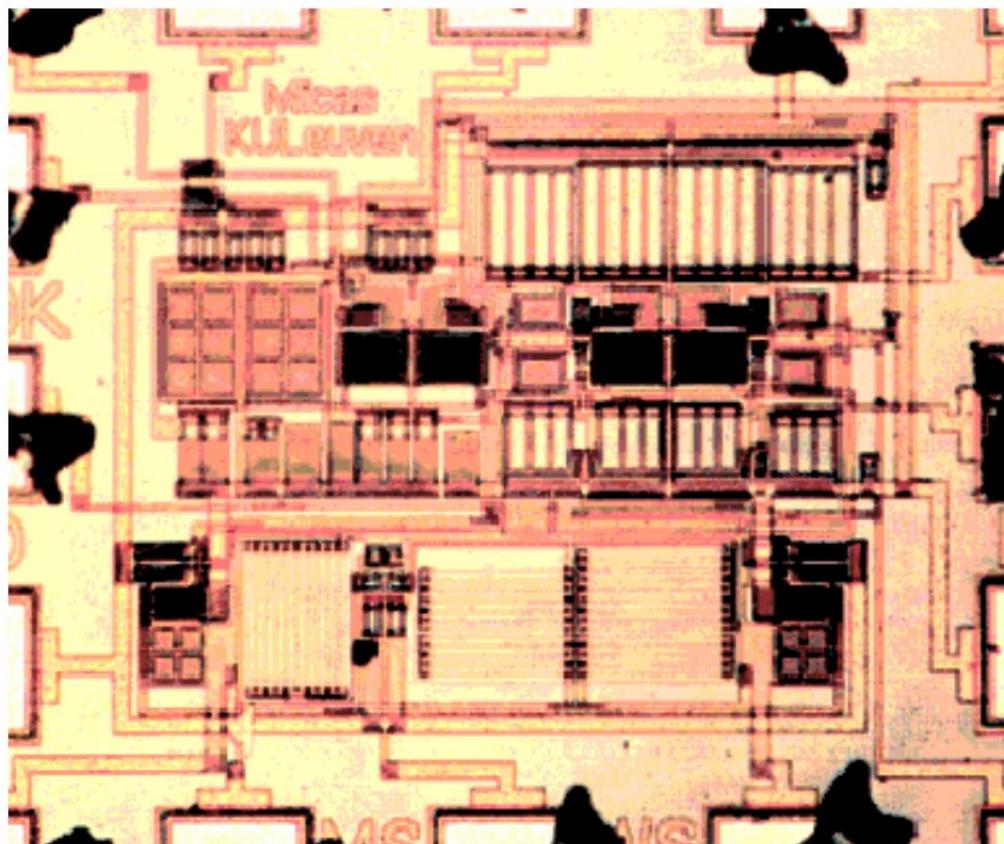
假设 $V_{DD} < 2.2V$ → 在 $V_{DD}/2$ 时两个晶体管均无法开启

» 反馈调制的性能



由于亚反型区中反型系数n的偏差: $\Delta g_m/g_m \approx 4\%$

》》 电流反馈调制实例



$V_{DD} = 1.5 \text{ V}$

$I_{TOT} = 0.2 \text{ mA}$

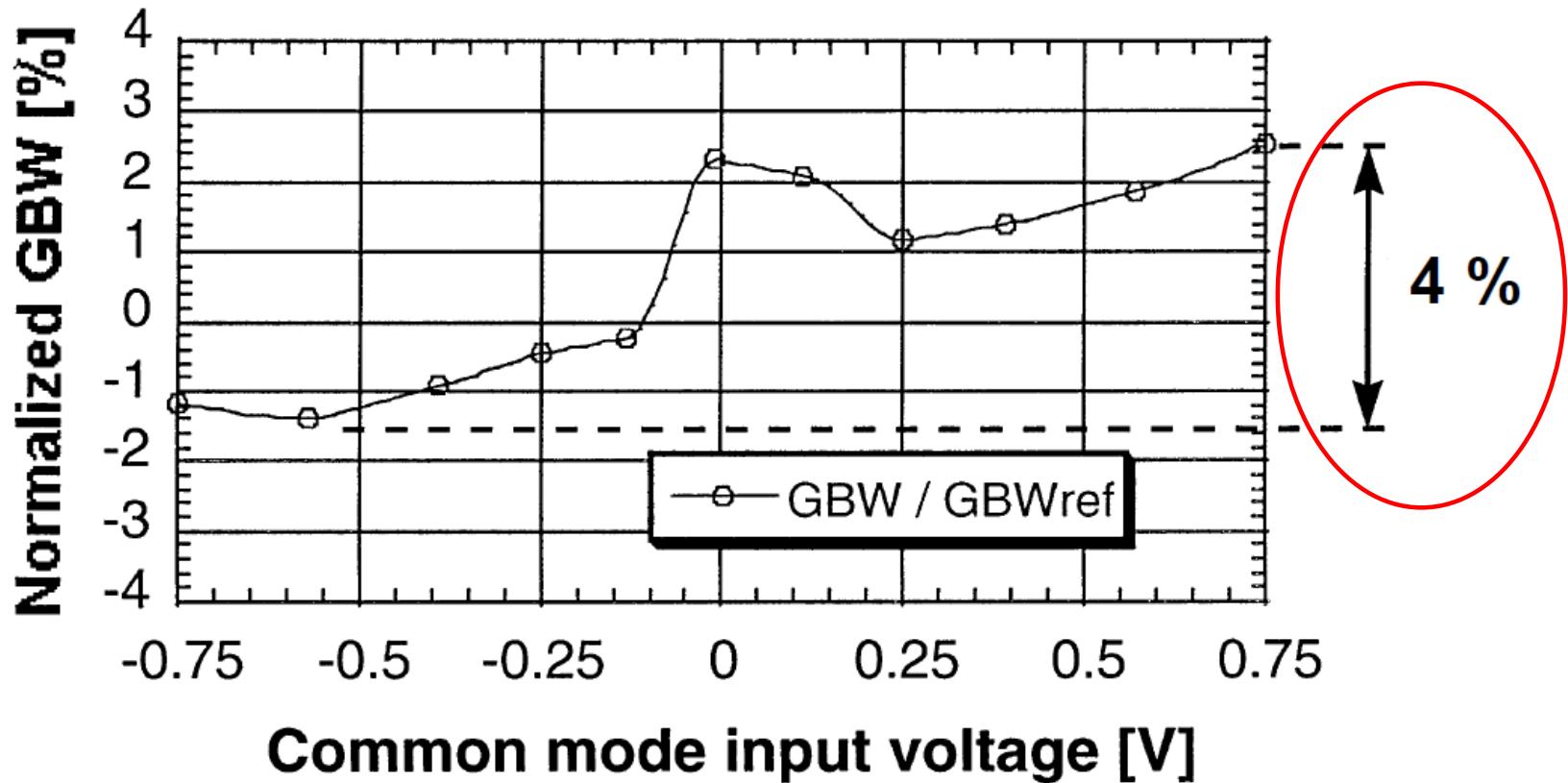
$\Delta g_m/g_m = 4 \text{ \%}$

$\text{GBW} = 4.3 \text{ MHz}$

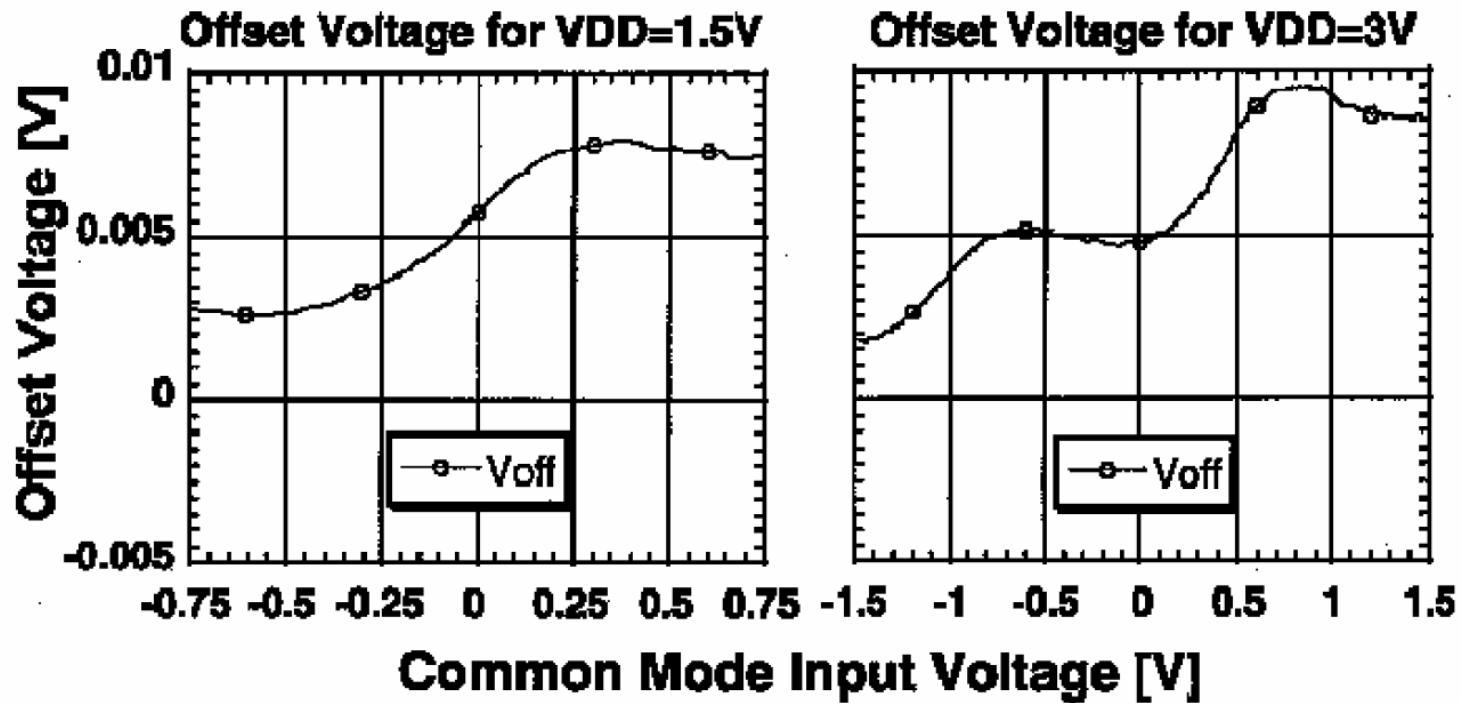
$C_L = 15 \text{ pF}$

E.Peeters et al, CICC 1997

》》 GBW的误差



» GBW和输入失调的误差



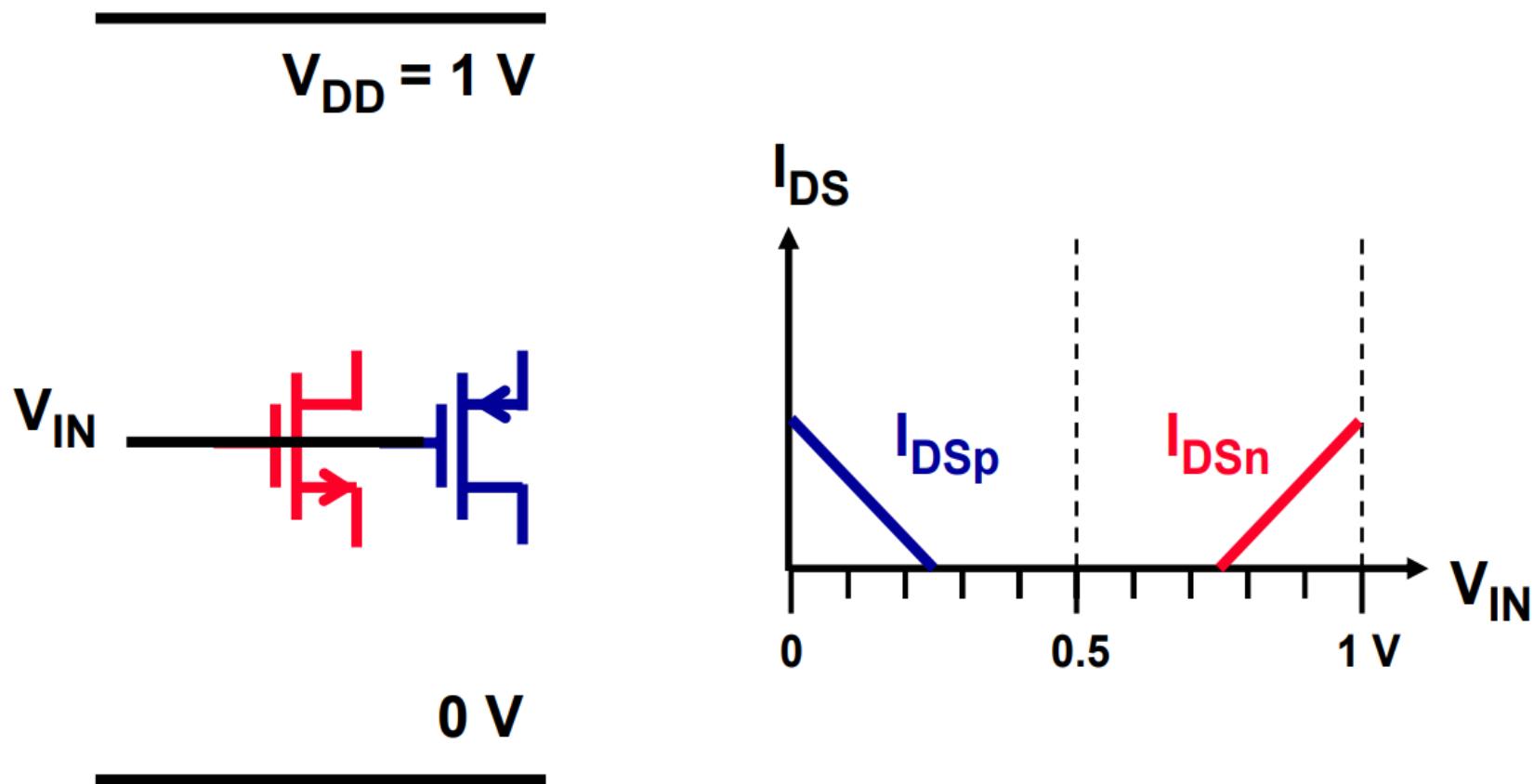
- 5mV的输入失调电压会极大的影响运放的性能



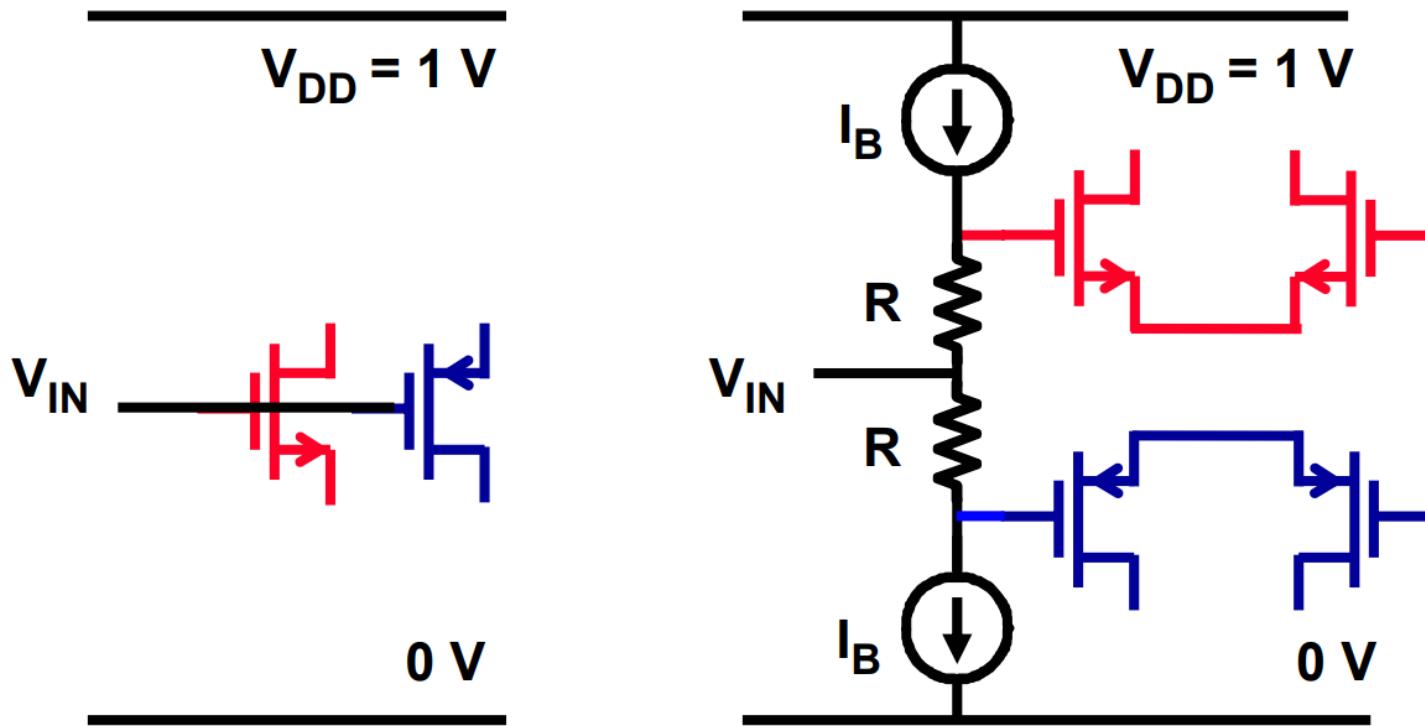
轨到轨输入

- 为什么需要轨到轨 (Rail-to-Rail) 的输入
- **跨导平衡技术：**
 - 3倍电流技术
 - 稳压二极管/齐纳二极管 (Zener Diodes)
 - 亚反型区中的电流调节技术
 - 电流调制技术：反馈调制
 - **超低电源电压中的轨到轨输入技术**

》》超低电源电压下的轨到轨输入

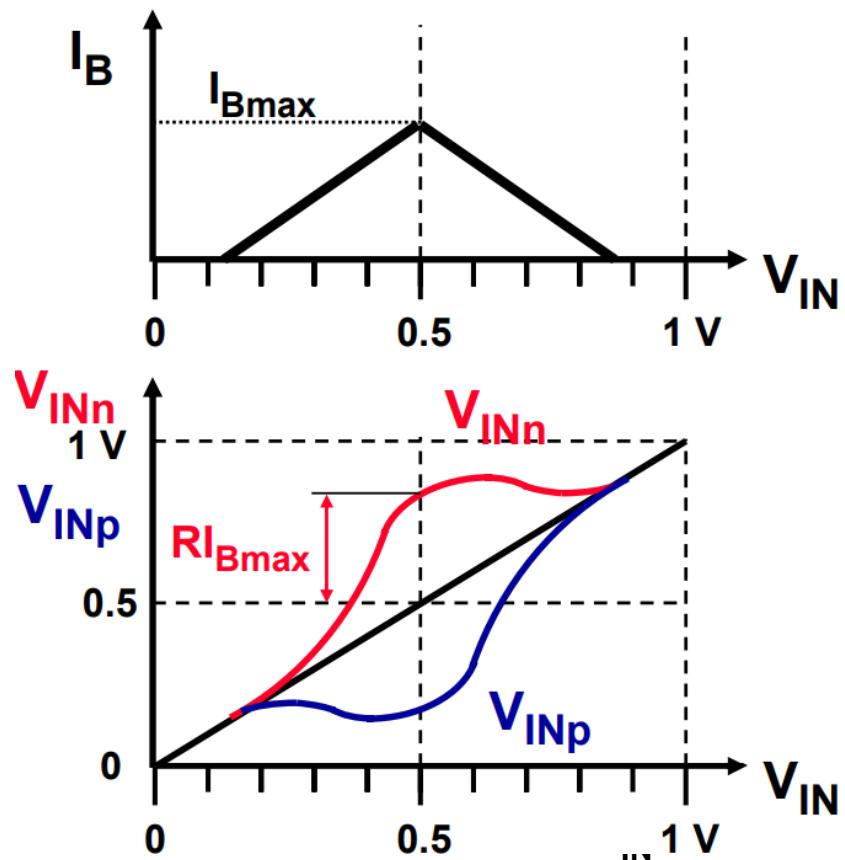
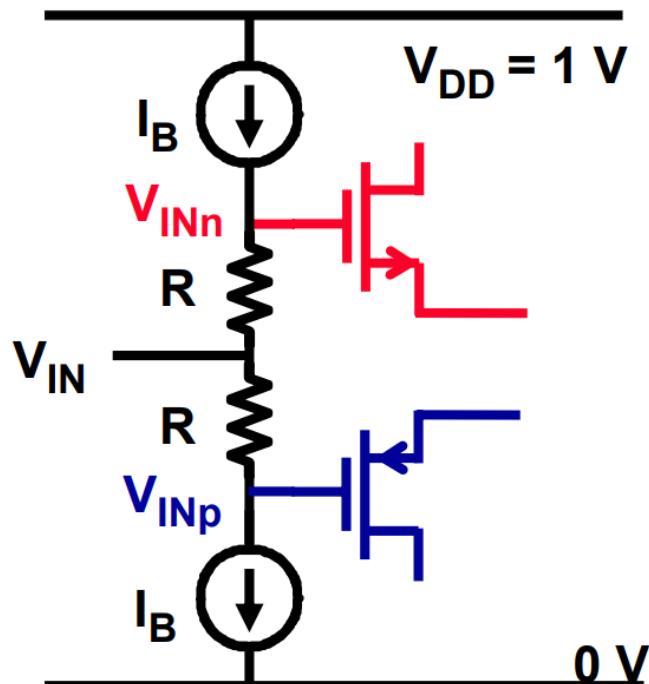


》》超低电源电压下的轨到轨输入



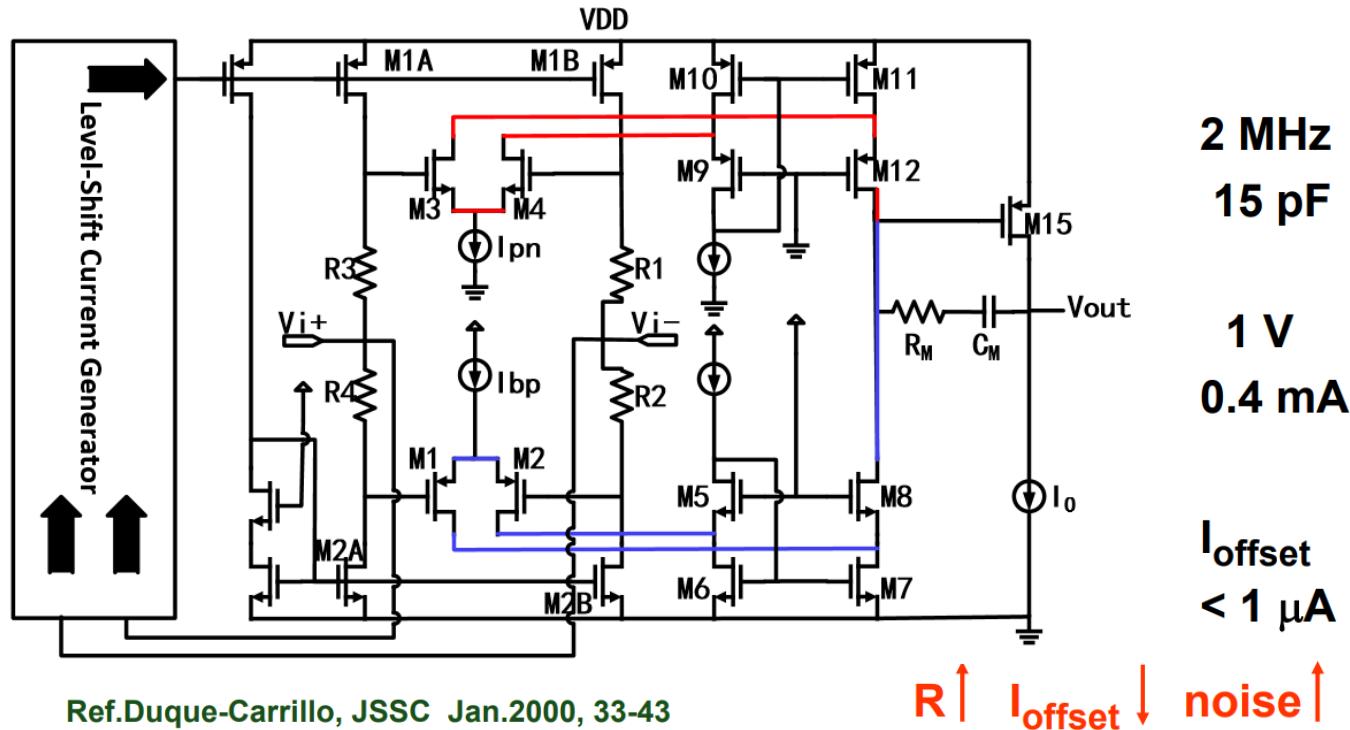
需要加入电压偏移电路 (Level Shifter)

》》超低电源电压下的轨到轨输入



Ref.Duaue-Carrillo. JSSC Jan.2000. 33

》》超低电源电压下的轨到轨输入：实例



- 需要在**匹配、噪声和功耗**方面平衡



课后作业

- 设计一轨到轨输入运放，要求指标：
 - $V_{DD} = 1.8V$
 - $GBW = 100MHz, C_L = 10pF$
- 完成设计后给出以下参数：
 - PM?
 - FOM?
 - 0.4V-1.4V区间内的系统失调电压
 - 0.4V-1.4V区间内的GBW偏差

第 9 章 Class A-B

第 10 章 全差分放大器



CMOS模拟集成电路设计

第七章：运放的高级设计： Class-AB级

胡远奇

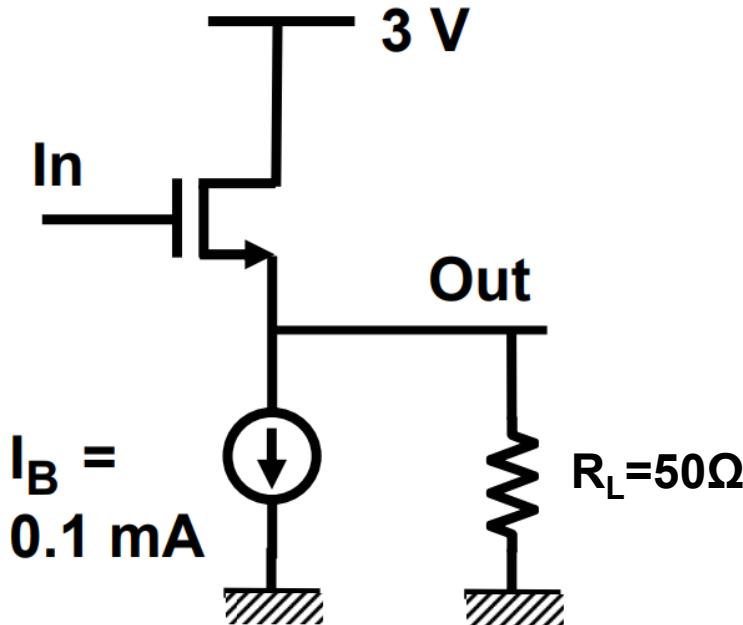
©2020



Class-AB级

- 什么是Class-AB级
- 静态电流控制方法
 - 交叉耦合差分对
 - 动态偏置技术
 - 线性跨导回路

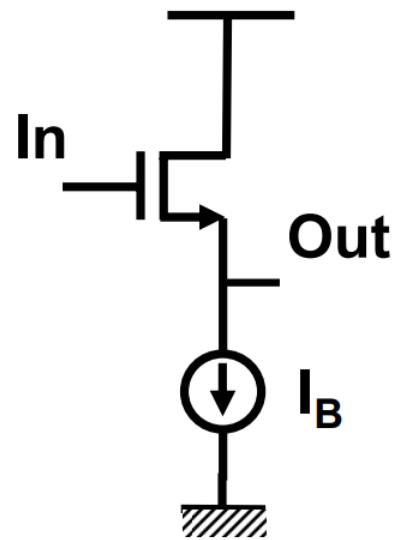
》》为什么需要推挽输出



当输出电阻较大时： $V_{OUT} = V_{IN} - V_{GS}$

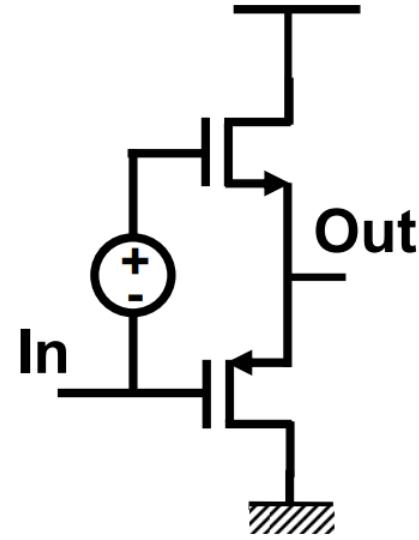
- 当输出电阻较小时：
 - 例如耳机索尼耳机阻抗 6 Ohm
 - 输出级可以向外输出 (source) 大电流，从而形成正向摆幅
 - 输出级无法向内吸收 (sink) 大电流，负向摆幅受限
 - 1V的负向摆幅，要求至少20mA的电流 (50ohm负载)，意味着静态功耗的增加

》》 输出级的形式



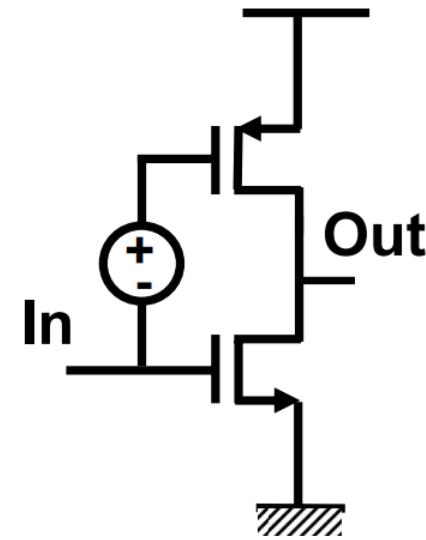
$$I_{\max} < I_B$$

$$V_{Out} = V_{In} - V_{GS}$$



Push-Pull

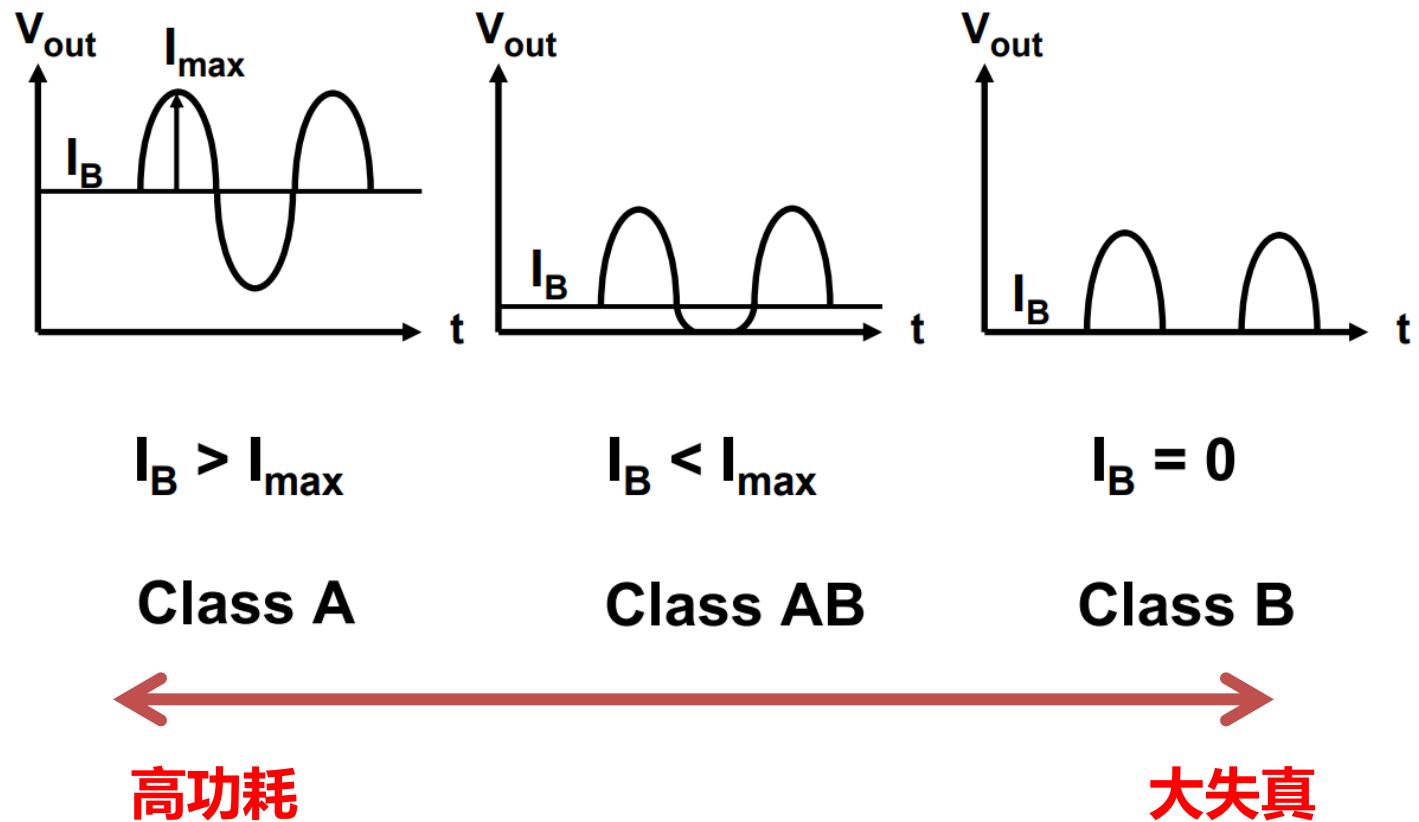
$$V_{out,\max} = V_{DD} - 2V_{GS}$$



Amplifier

Rail-to-rail

Class A, AB, B

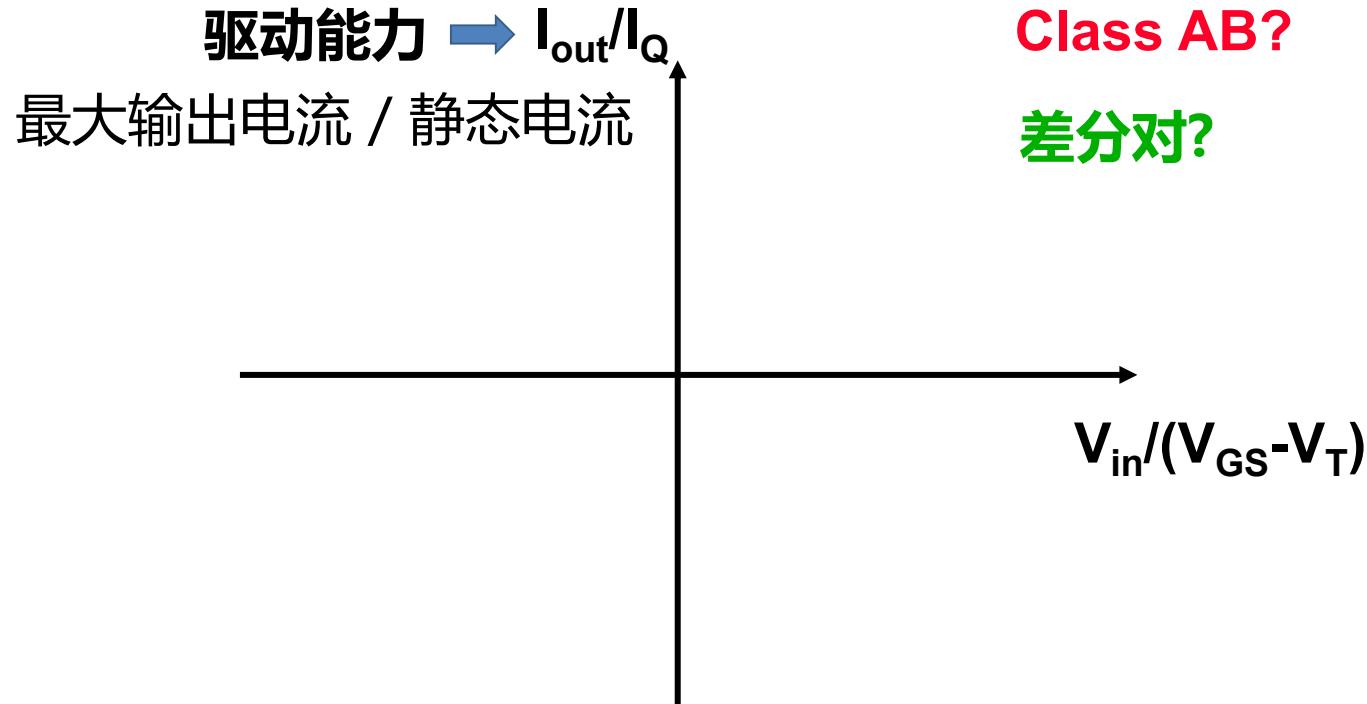




Class-AB 级的要求

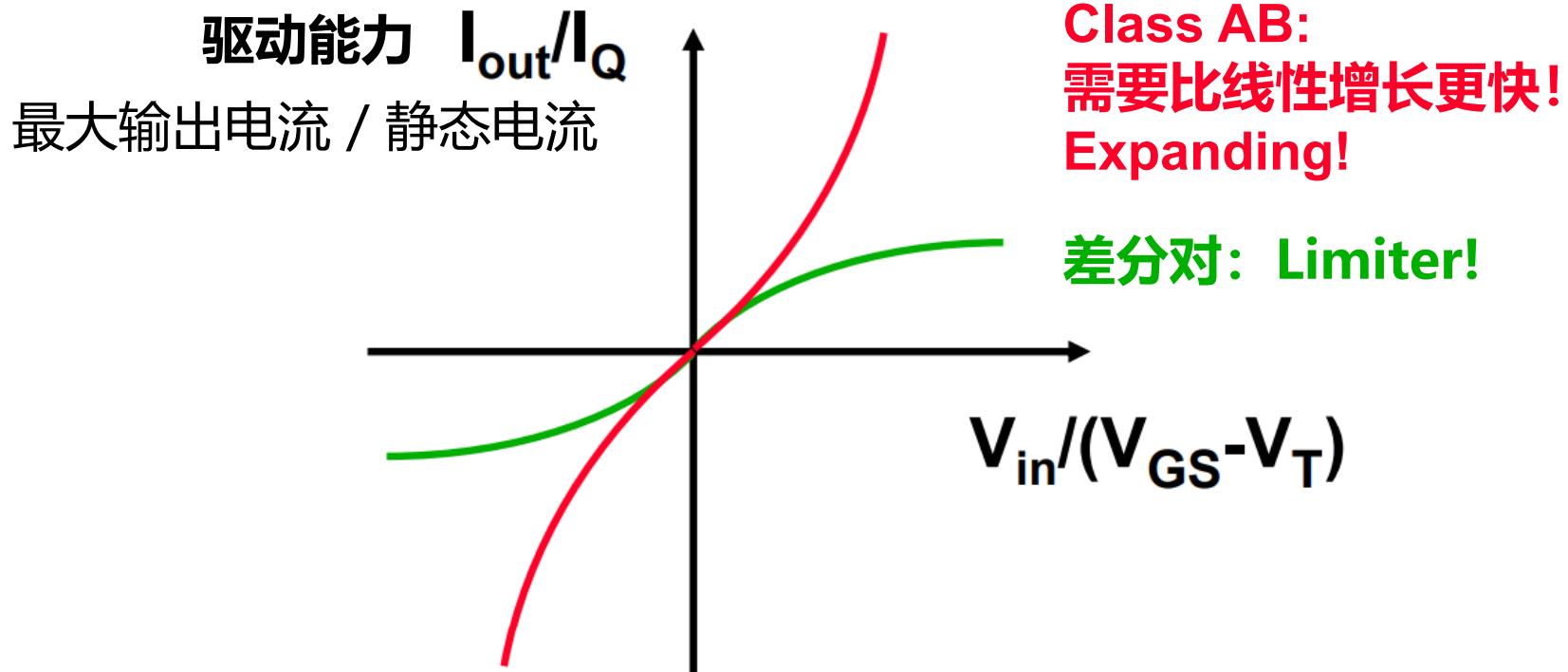
- ✓ 轨到轨的输出
- ✓ 静态电流的精准控制
 - ✓ 低功耗
 - ✓ 独立于电源电压
- ✓ 大电流驱动能力 I_{max}/I_Q
- ✓ 尽量小的面积

»» Class-AB 输出级



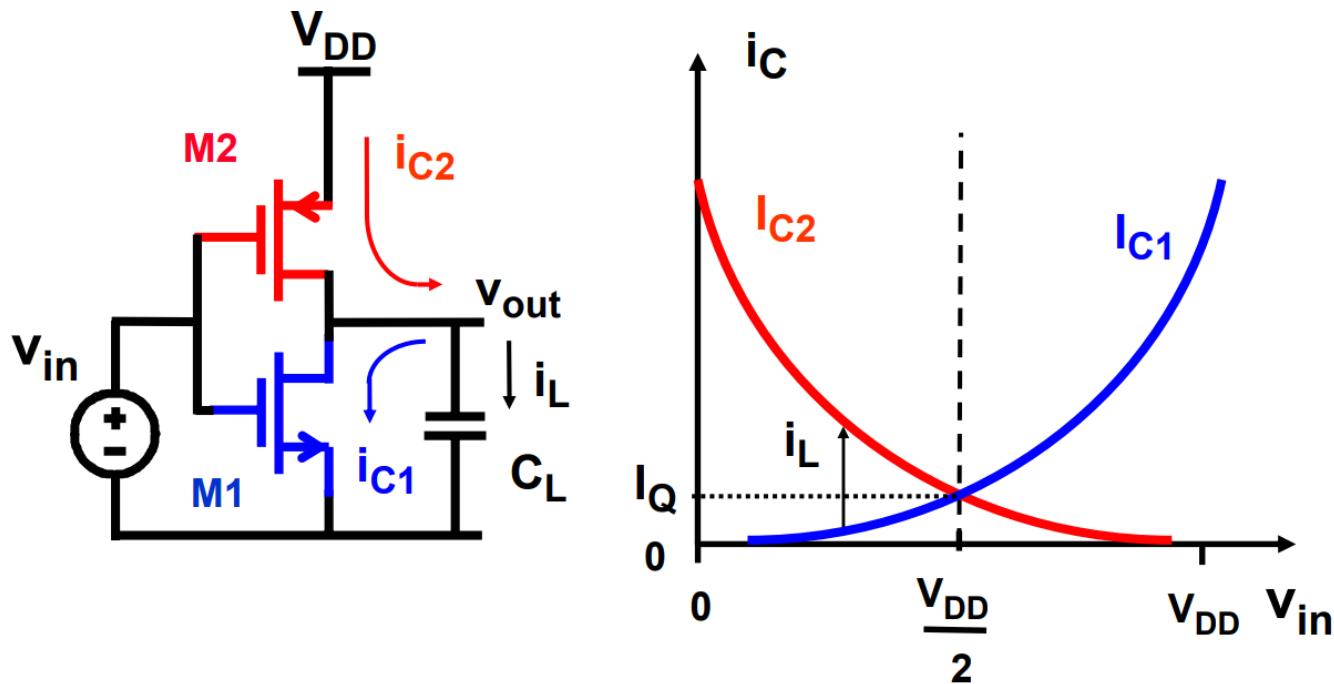
Class-AB:大失真->必须通过反馈修正->3级运放

»» Class-AB 输出级



Class-AB:大失真->必须通过反馈修正->3级运放

Class-AB 输出级：反相器



问题1： I_Q 无法控制

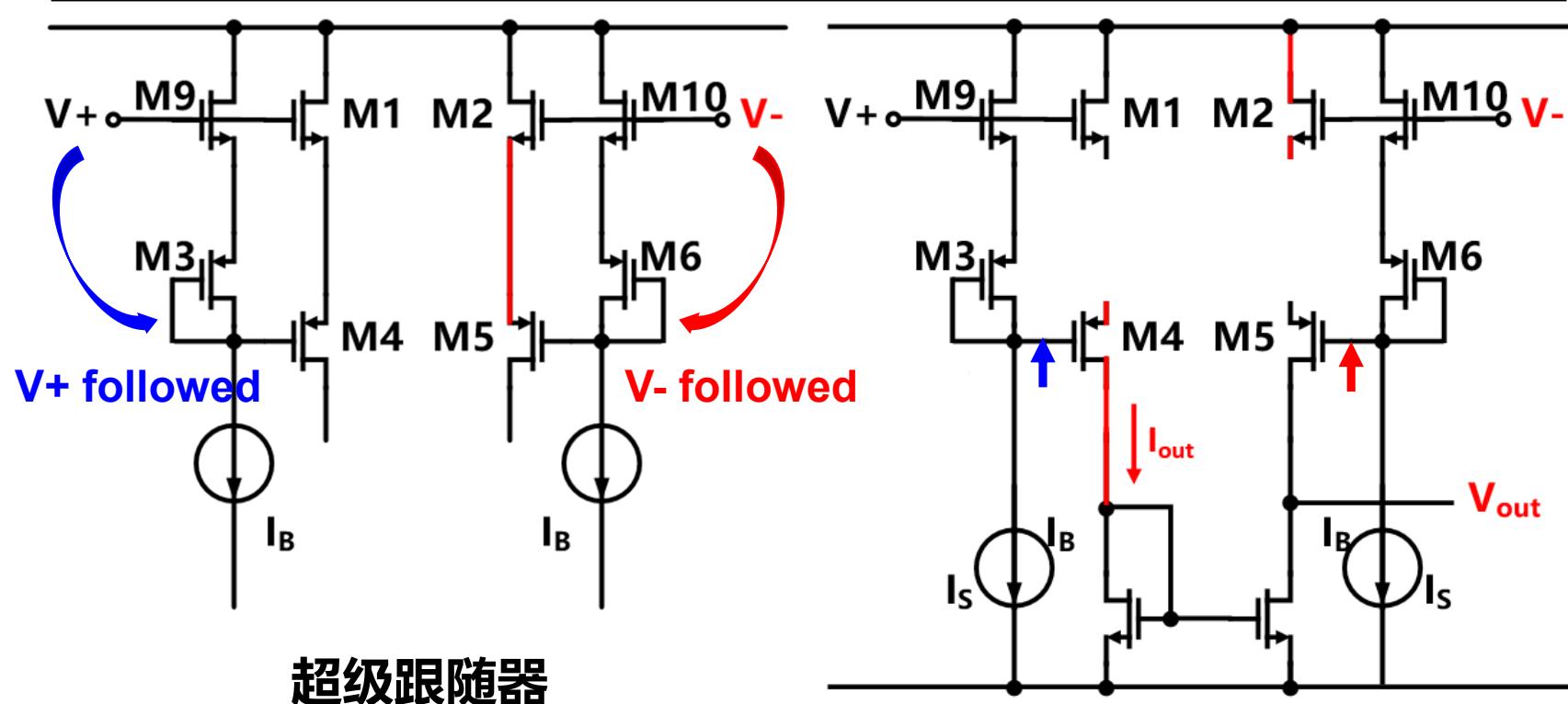
问题2：输出与电源电压直接相关



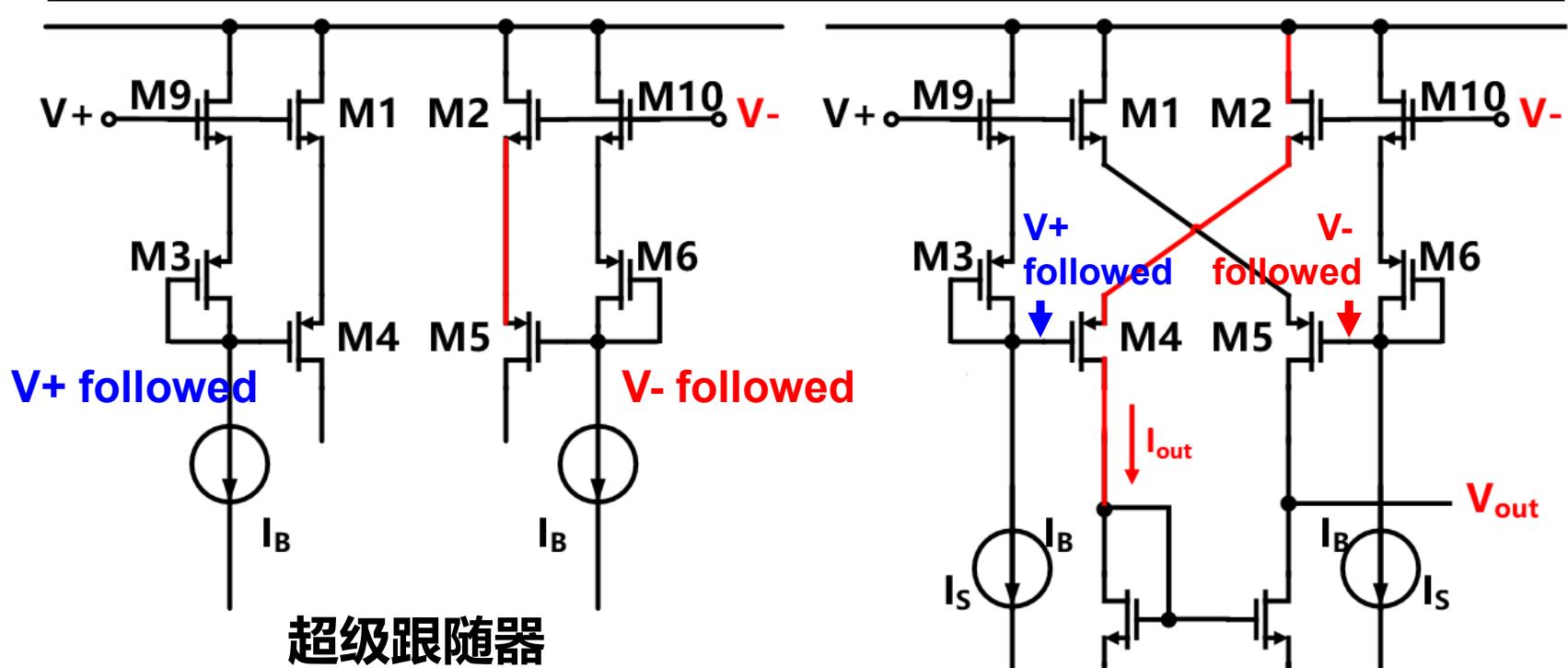
Class-AB级

- 什么是Class-AB级
- 静态电流控制方法
 - 交叉耦合差分对
 - 动态偏置技术
 - 线性跨导回路

》》 交叉耦合差分对

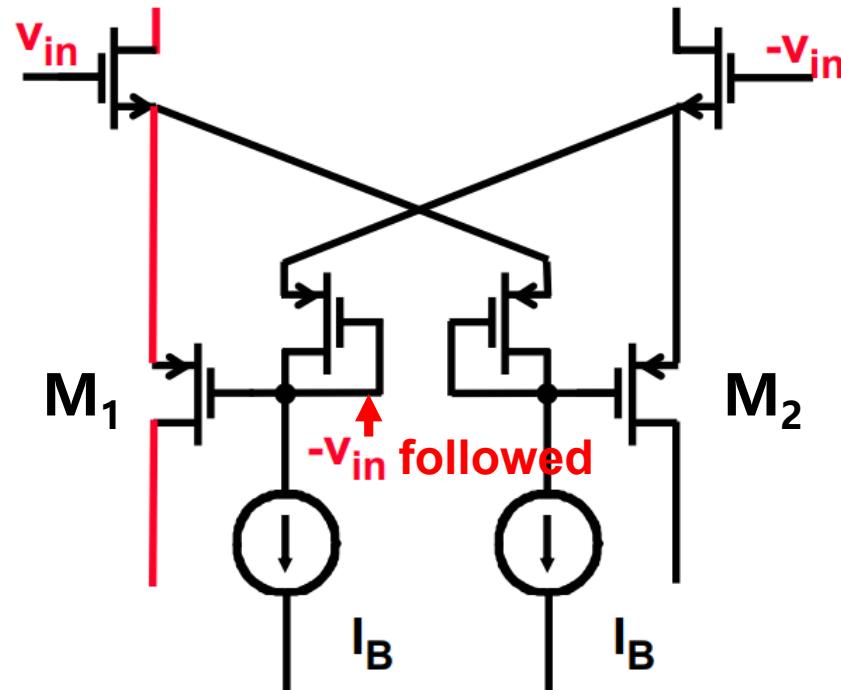


》》 交叉耦合差分对



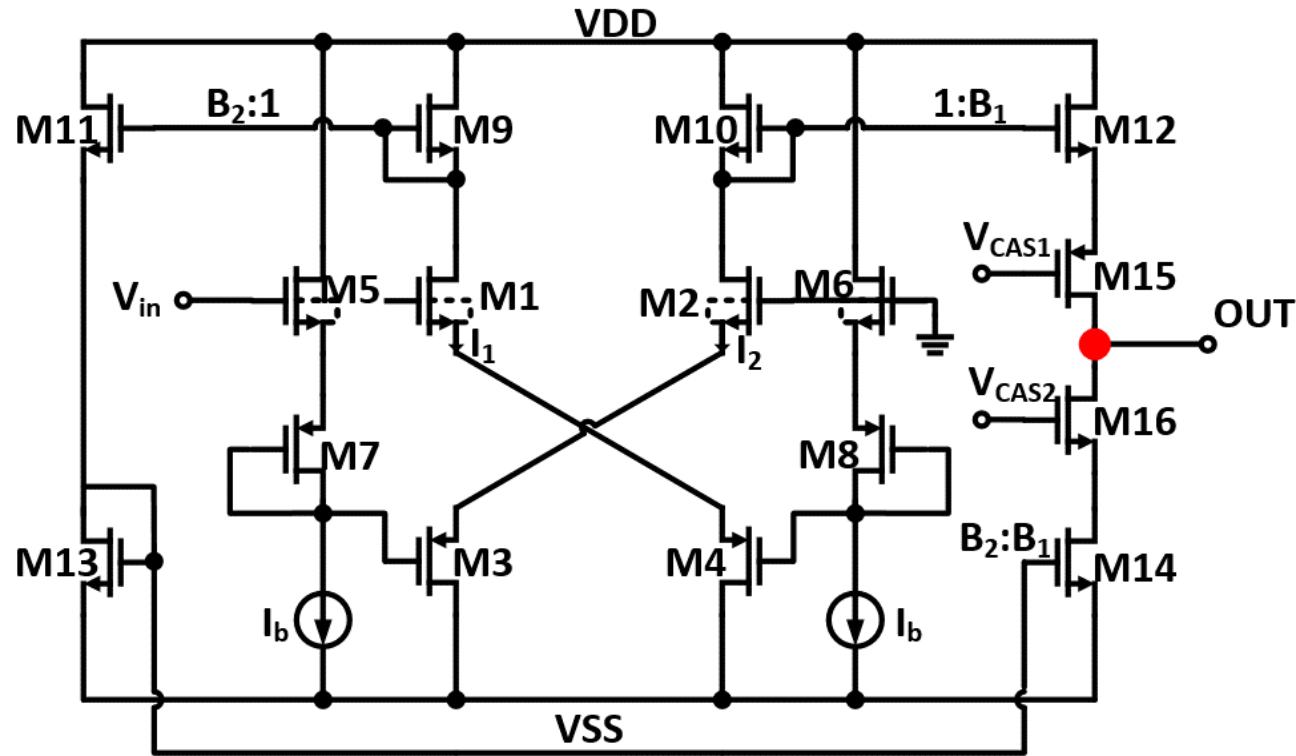
- V_{in} 作用在晶体管 M_{1-5} 和 M_{2-4} 的 V_{GS} 上，实现大电流输出；静态电流通过电流镜得到控制

》》 交叉耦合差分对



- V_{in} 作用在晶体管M₁和M₂的 V_{GS} 上，实现大电流输出；对称性不如前者

Class-AB 输入级电路



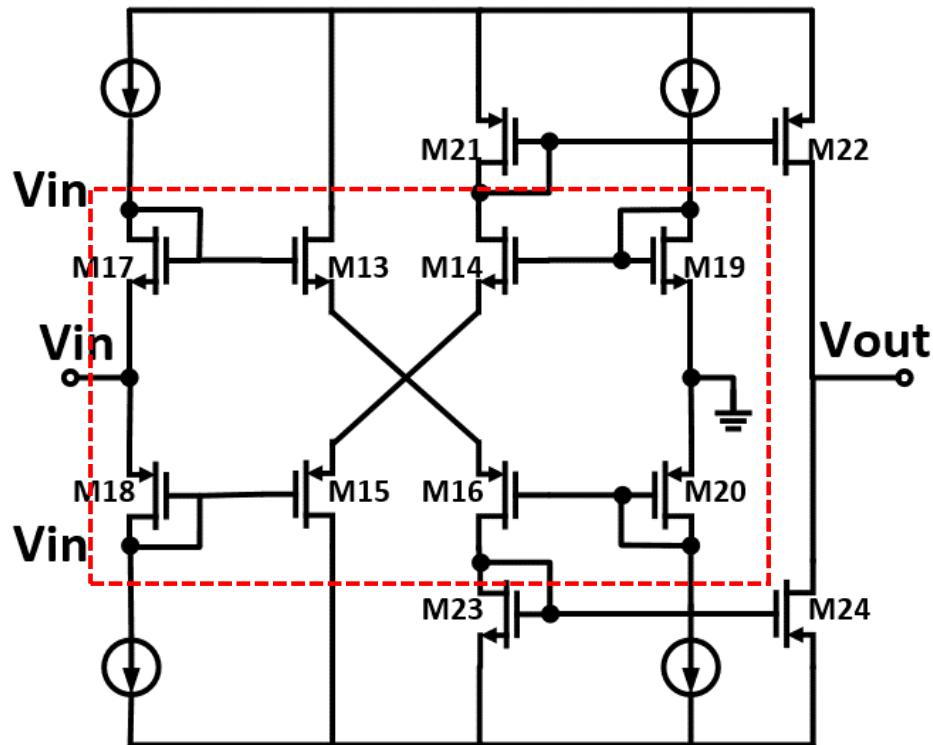
$$GBW = \frac{g_{m1}}{2\pi C_L}$$

SR ↑↑

- 由于Class-AB的特性，Slew Rate显著上升



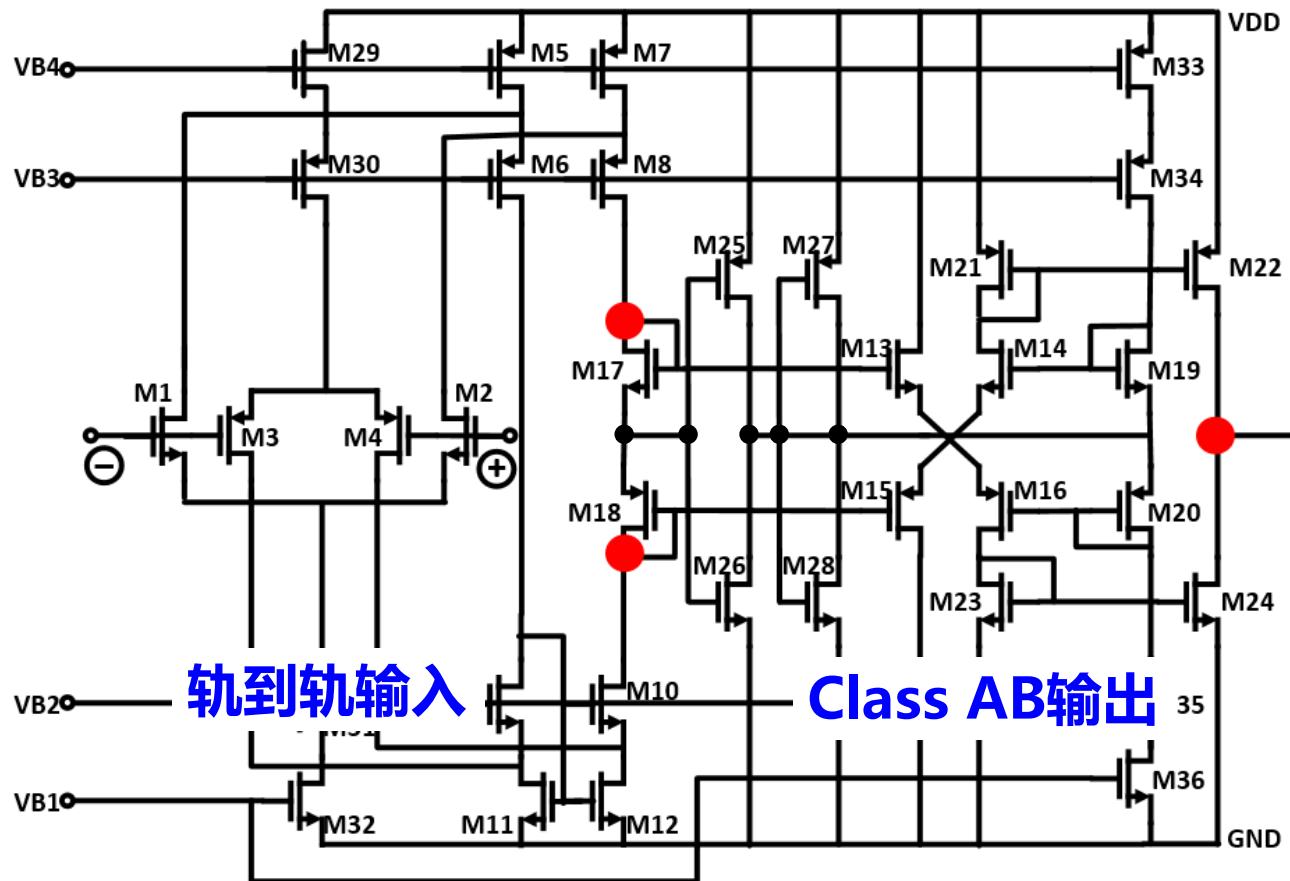
单端输入的Class AB (Double-Push)



- M₁₃-M₂₀共同组成交叉耦合电路
- M₁₃-M₁₆为核心耦合对
- M₁₇-M₂₀为静态电流控制电路

- 静态电流由输入端的电流镜控制

»» Double-Push



● 高阻抗点

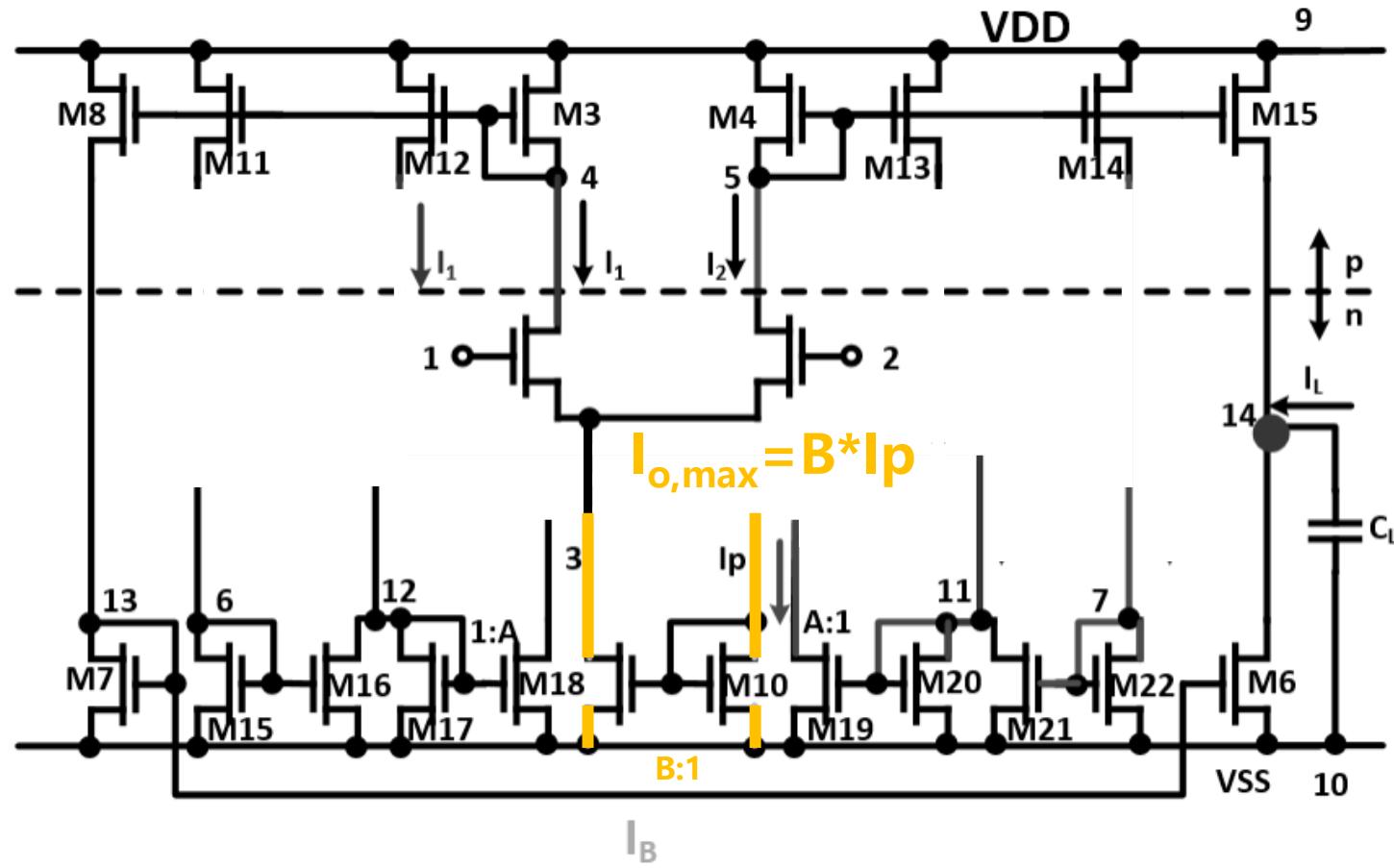
Ref. Fischer, JSSC
June 87, 330-340



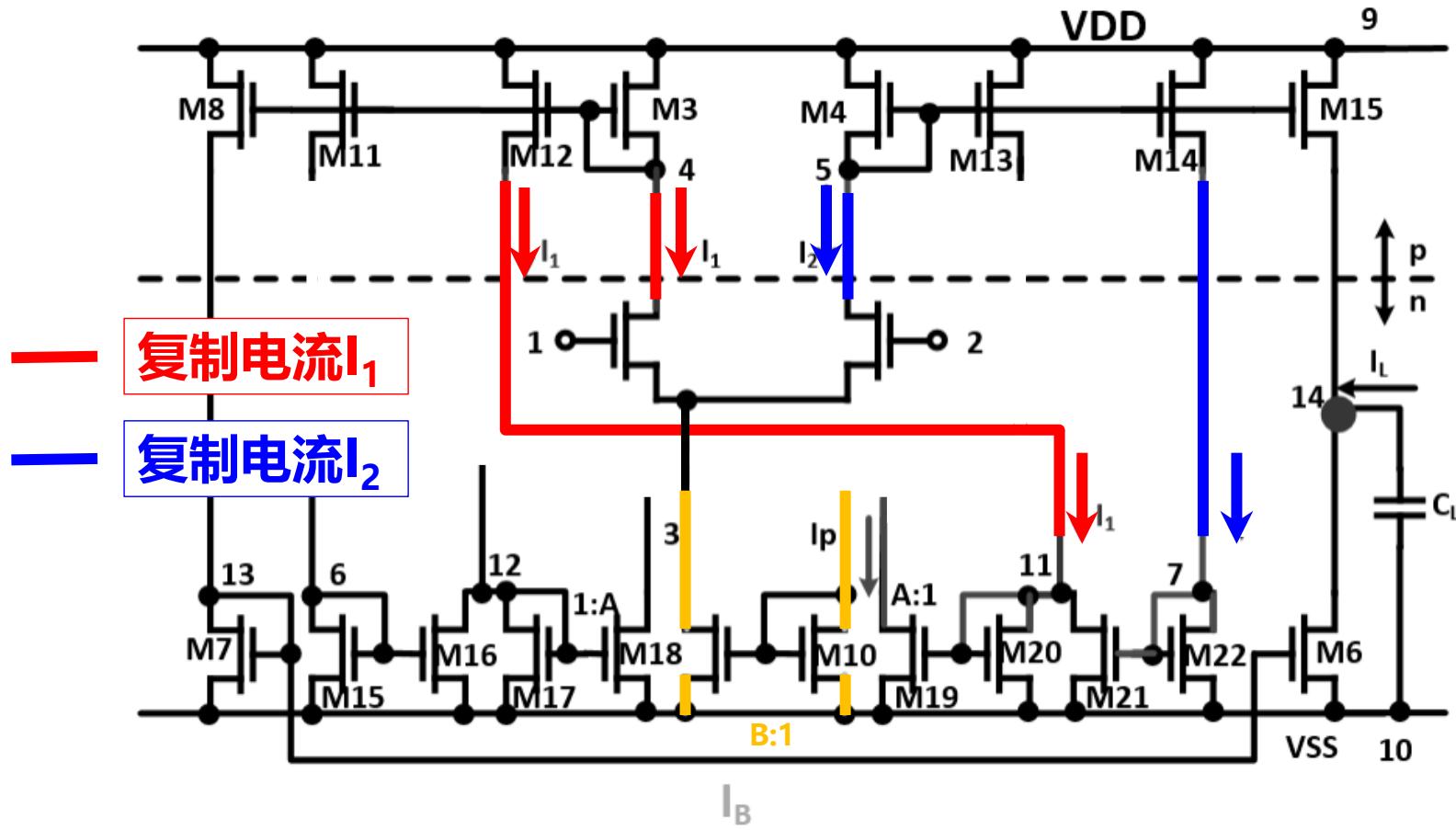
Class-AB级

- 什么是Class-AB级
- 静态电流控制方法
 - 交叉耦合差分对
 - 动态偏置技术
 - 线性跨导回路

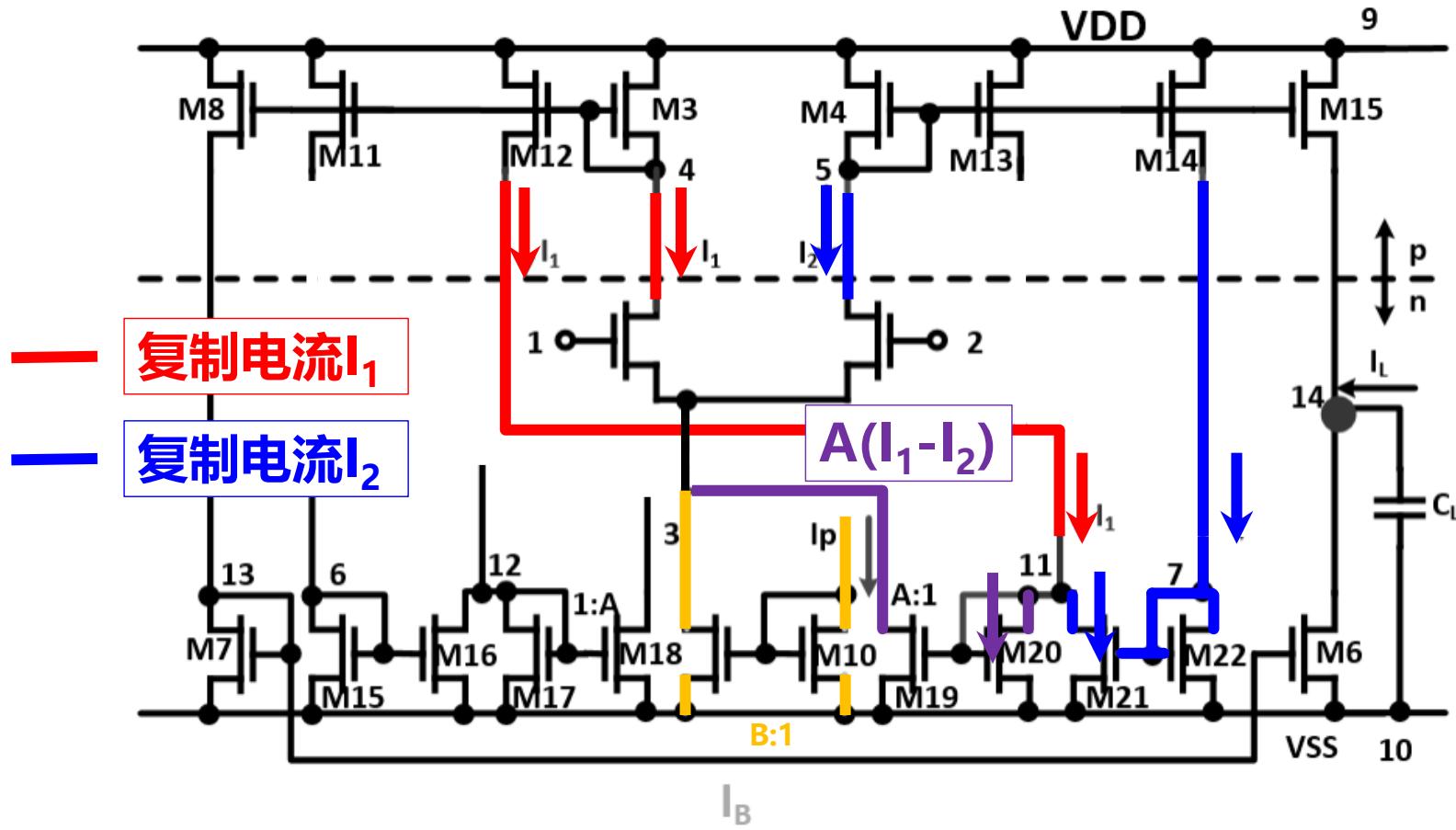
》》 动态偏置技术



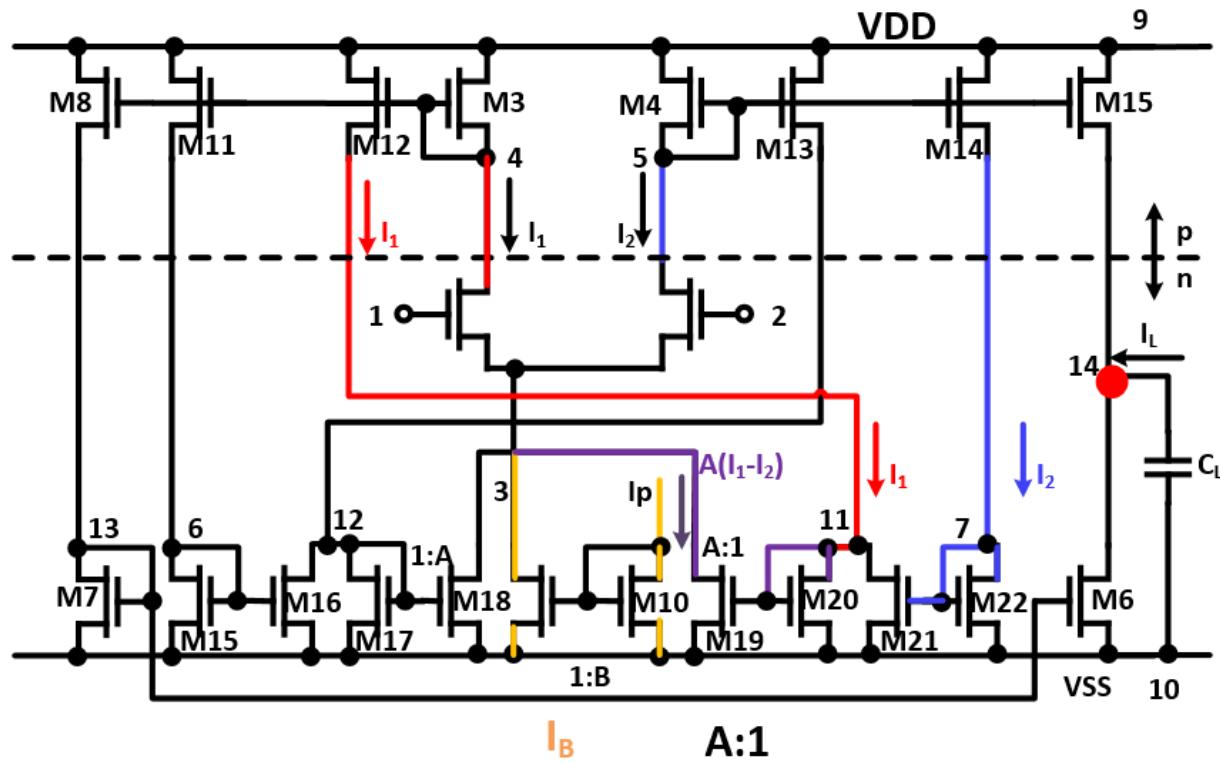
》》 动态偏置技术



》》 动态偏置技术

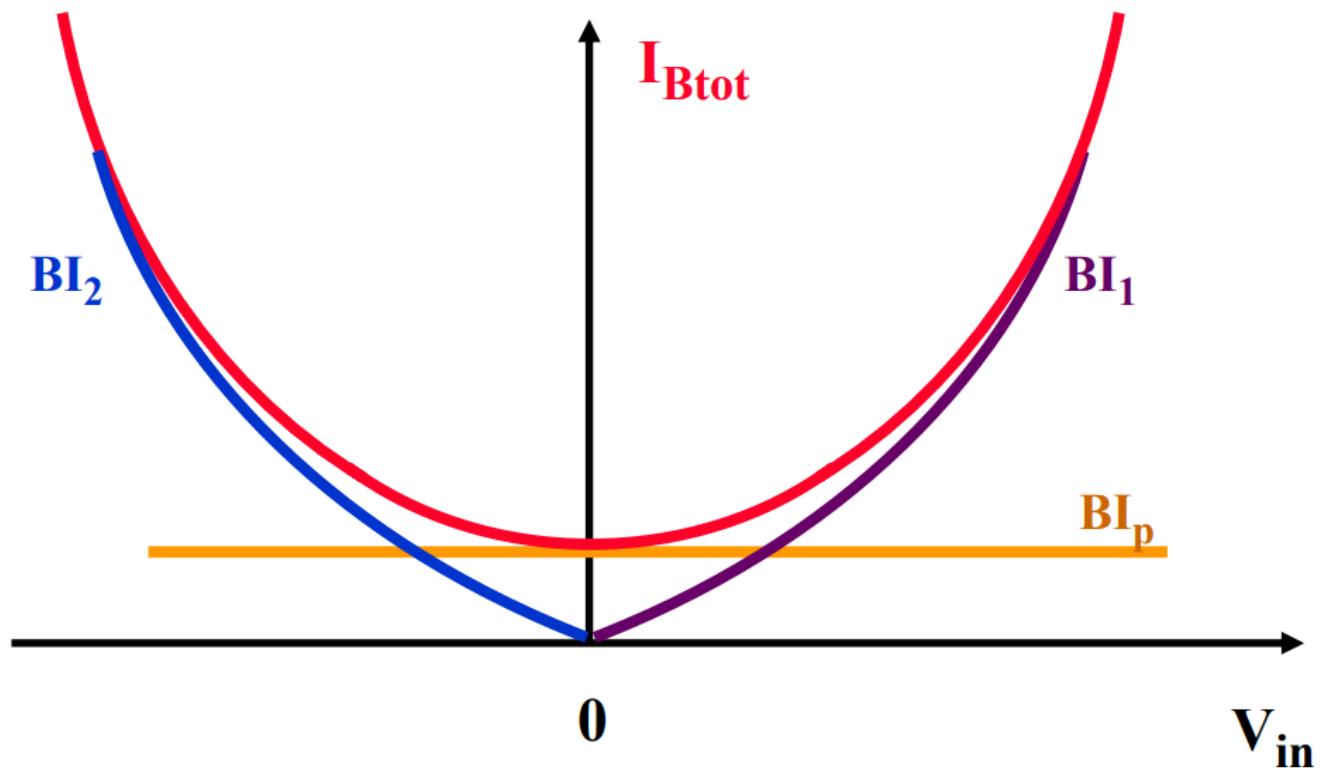


》》 动态偏置技术

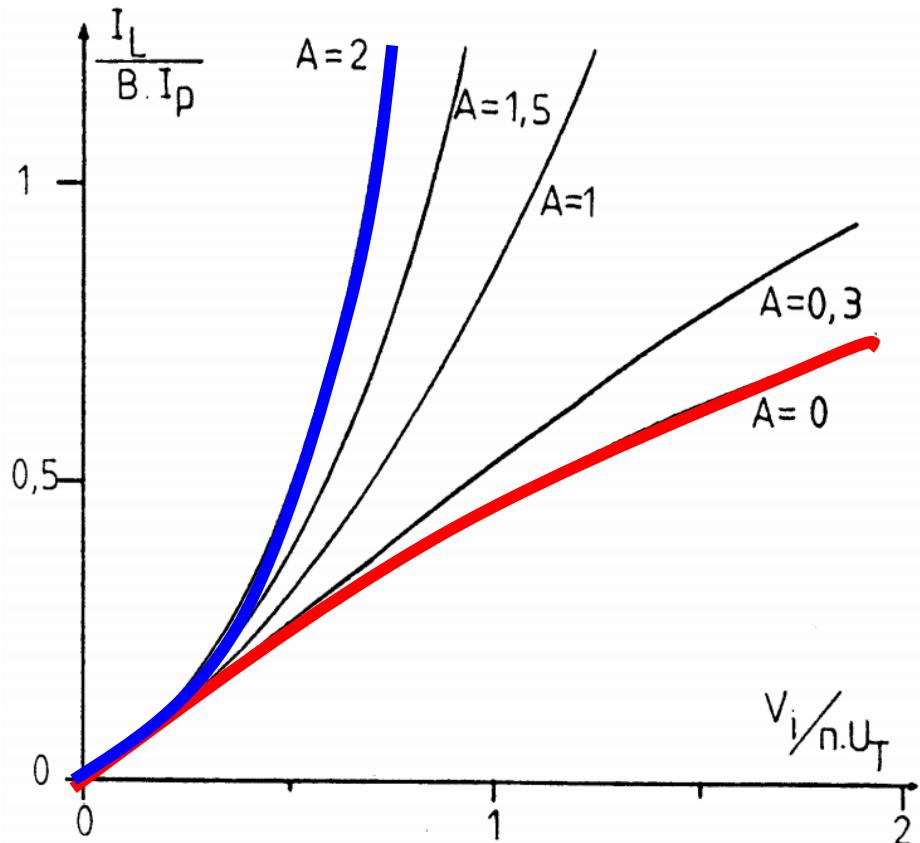


- 偏置电流由差分电流的差控制
- 差分电流通过电流镜M₁₇₋₁₈和M₁₉₋₂₀的比例放大A倍

» 动态偏置技术



》》 动态偏置技术



- **A=0时，没有动态偏置技术，输出电流受限**
- **A越大，Class-AB的效果越明显**
- **由于失配的存在（Mismatch），放大系数A不能过大，通常不能超过10**

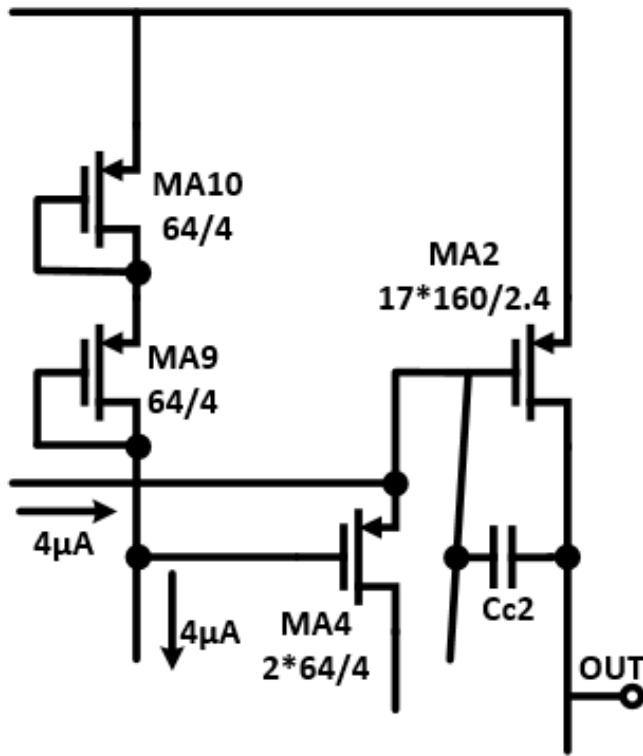


Class-AB级

- 什么是Class-AB级
- 静态电流控制方法
 - 交叉耦合差分对
 - 动态偏置技术
 - 线性跨导回路

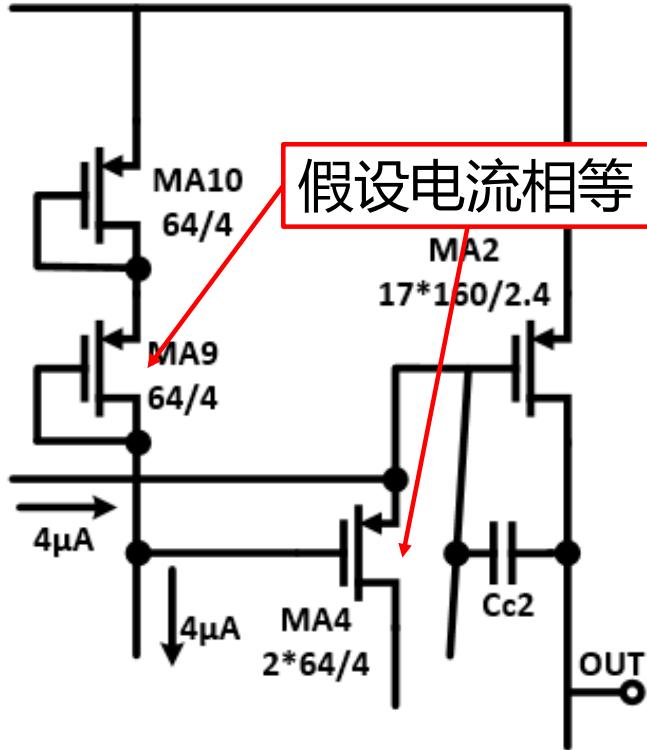


静态电流控制技术:线性跨导回路



线性跨导回路：

》》 静态电流控制技术:线性跨导回路



线性跨导回路:

$$V_{GS2} + V_{GS4} = V_{GS9} + V_{GS10}$$

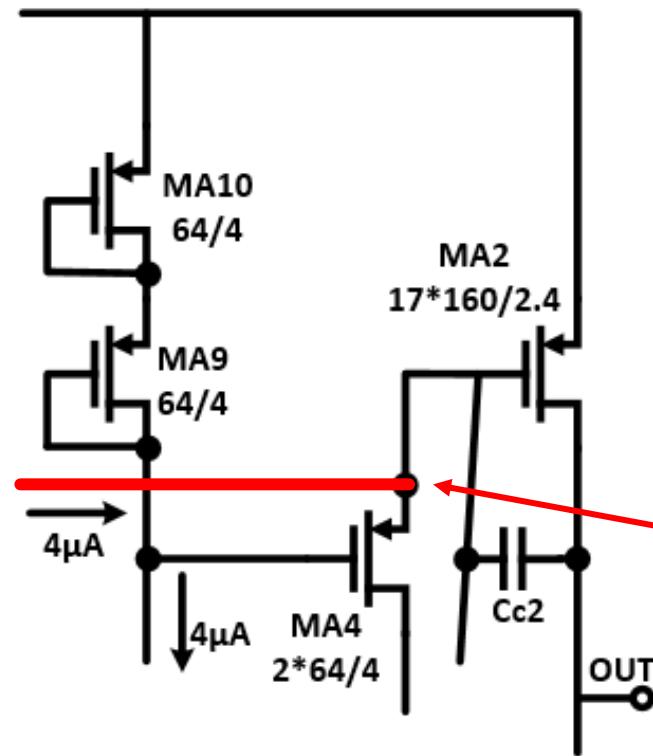
$$V_{GS2} - V_T = \sqrt{\frac{I_{DS2}}{K'_p W/L_2}}$$

$$\sqrt{\frac{I_{DS2}}{W/L_2}} + \sqrt{\frac{I_{DS4}}{W/L_4}} = 2 \sqrt{\frac{I_{DS9}}{W/L_9}}$$

$$\frac{I_{DS2}}{I_{DS9}} = \frac{W/L_2}{W/L_9} \left(2 - \frac{1}{\sqrt{2}}\right)^2 \approx 118$$

- 偏置电流由回路**器件比例**和**偏置电流**控制

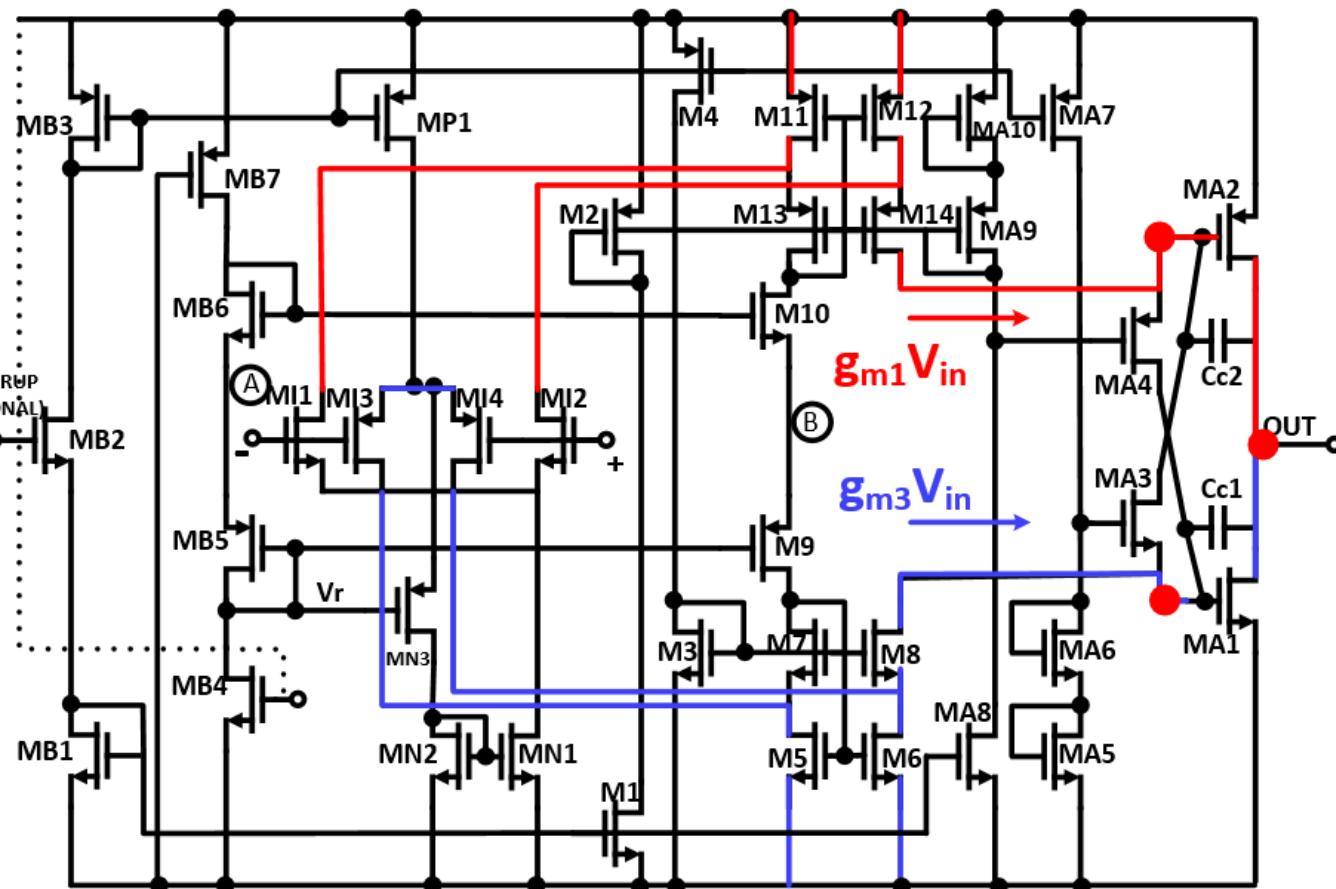
》》 静态电流控制技术:线性跨导回路



$$\frac{I_{DS2}}{I_{DS9}} = \frac{W/L_2}{W/L_9} \left(2 - \frac{1}{\sqrt{2}}\right)^2 \approx 118$$

- I_{DS2} 达到最大值时, I_{DS4} 趋于0,
晶体管MA4接近截止
- 输入信号

》》 静态电流控制技术:线性跨导回路



- 轨到轨



- Class-AB

14 MHz
/ 11pF

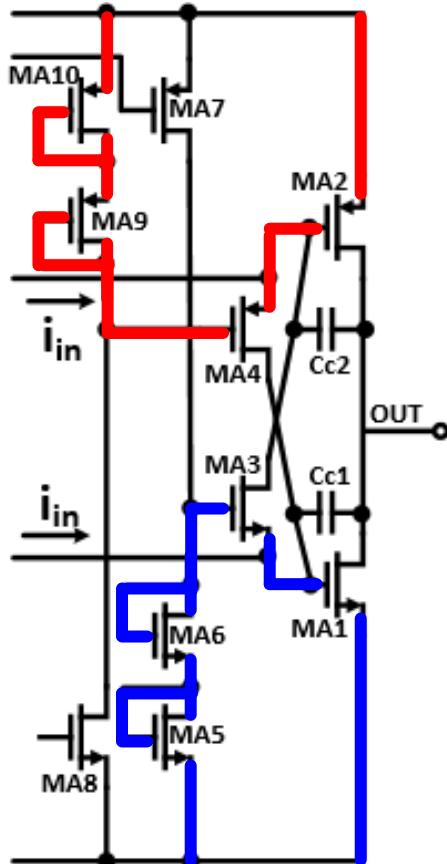
5.6 MHz
/ 100pF

4 V/ μ s

36 nV/ \sqrt{Hz}

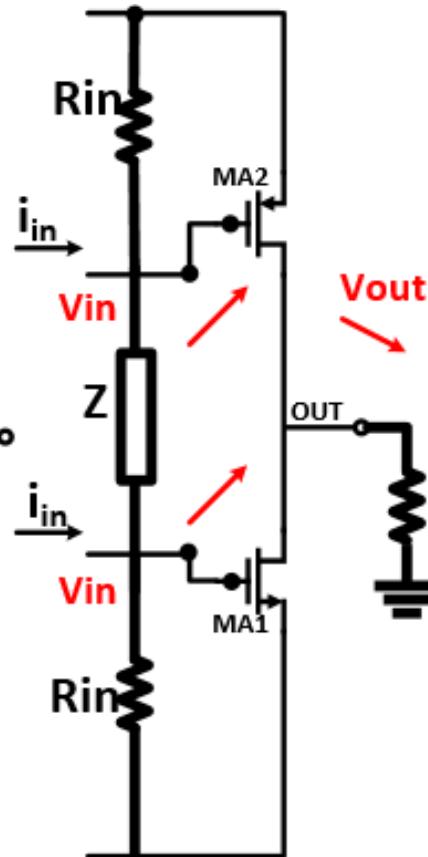
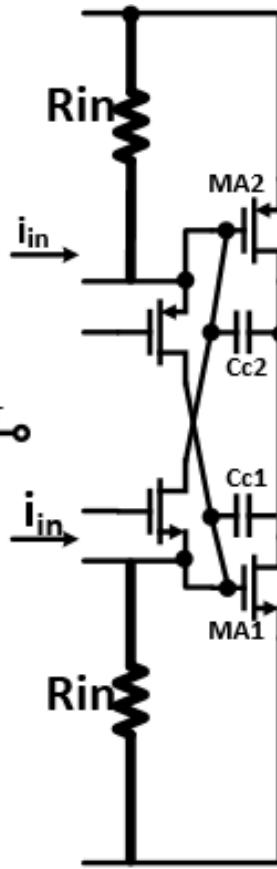
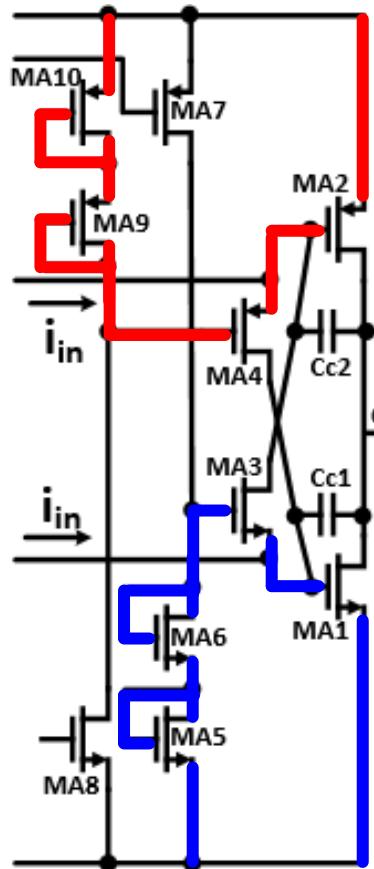
5 V
0.4 mA

» 线性跨导回路：输出级增益



- PMOS和NMOS线性跨导回路的输入电流相位相同，极性一致
- 对于小信号模型而言： $i_{in} = i_{MA4} + i_{MA3}$
- 由于相位一致，MA4和MA3被自举(Bootstrap)，使得其等效阻抗无穷大
- 晶体管MA4和MA3只用来提供静态偏置
- 该输出级增益即为MA1和MA2晶体管的自增益，或跨导与负载电阻的乘积

》》 线性跨导回路：输出级增益



$$i_{in} = g_{m1} v_{+}$$

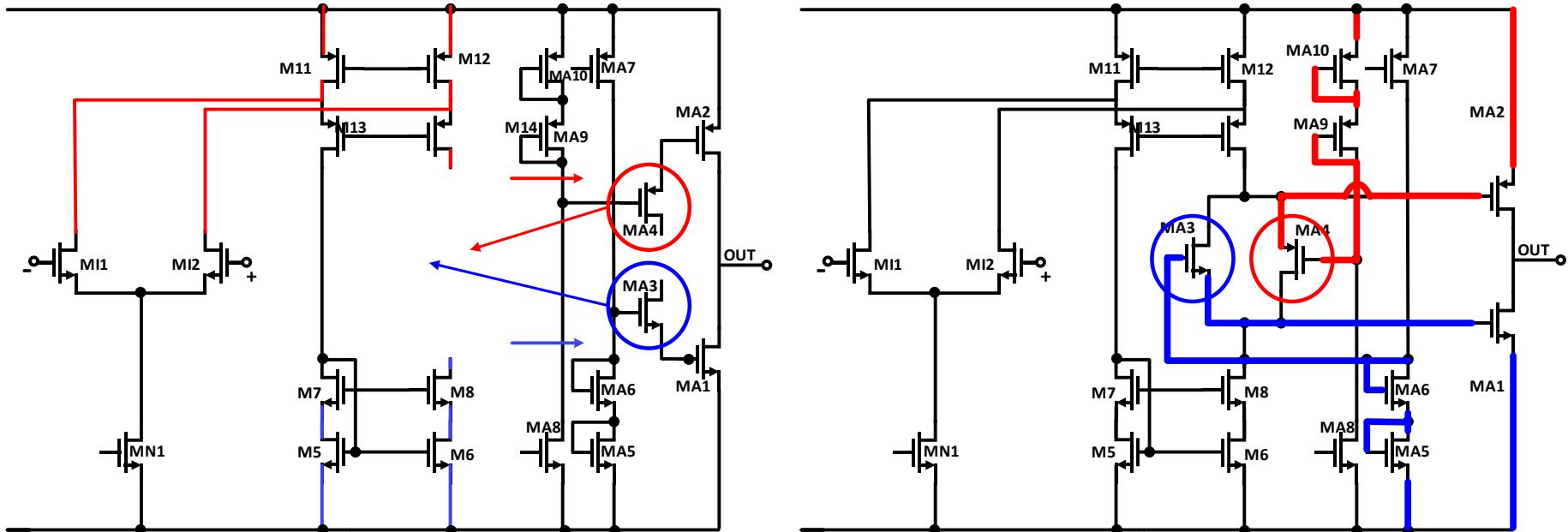
$$\frac{v_{in}}{i_{in}} = R_{in}$$

$$\frac{v_{out}}{v_{in}} = 2g_{mA1}R_L$$

$$A_v = 2g_{m1}R_{in}g_{mA1}R_L$$

》》 线性跨导回路：输出级增益

- 可以将偏置晶体管M3A和M4A并联，使其各自的电流动态调整

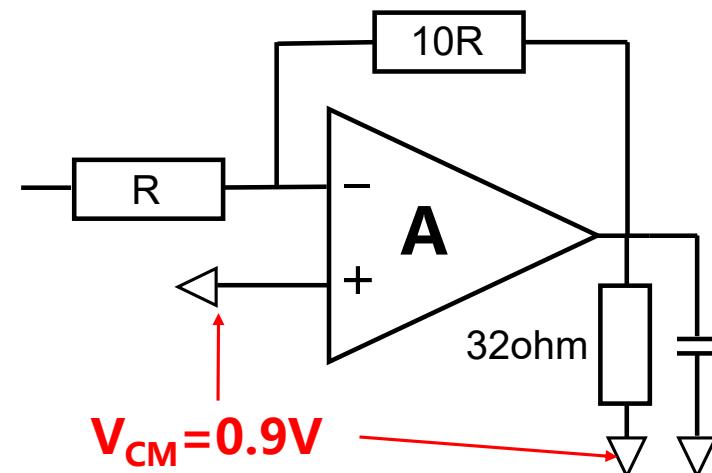


课后习题

- 设计一个线性跨导回路的Class-AB运放，其中：
 - $V_{DD} = 1.8V, V_{SS} = 0V, V_{CM} = 0.9V$
 - $C_L = 10pF, R_L = 32\text{ohm}$
 - 差模输入 $V_{pp} = 100\text{mV}$, 输入频率200kHz, 放大倍数10

要求指标：

- 要求输出正弦波峰-峰值大于950mV
- 运放静态功耗小于1.5mA



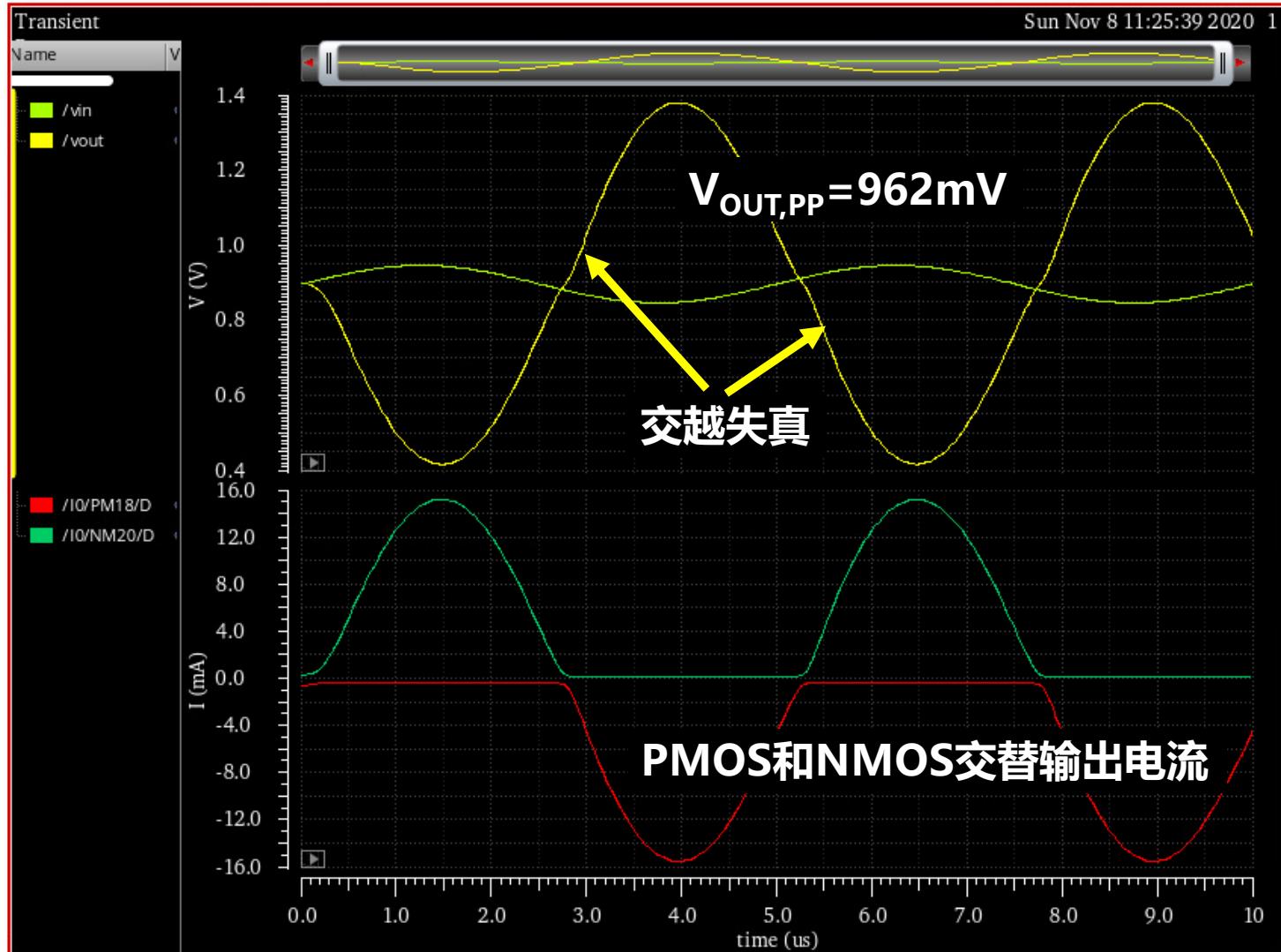
》》课后习题

• 思路：

1. 根据 $\times 10$ 的放大倍数和下式，确定所需的DC增益，建议留出**5倍冗余**

$$V_{out} = -\frac{10 \cdot A_0}{A_0 + 11} \cdot V_{in}$$

2. 根据 $\times 10$ 的放大倍数和输入频率估计GBW，建议**5倍冗余**
3. 根据所需要的输出电流预估线性跨导回路尺寸和偏置
 - 峰值输出时， $V_{DS}=0.4V$ ，因此峰值下 **$V_{GST} < 0.4V$**

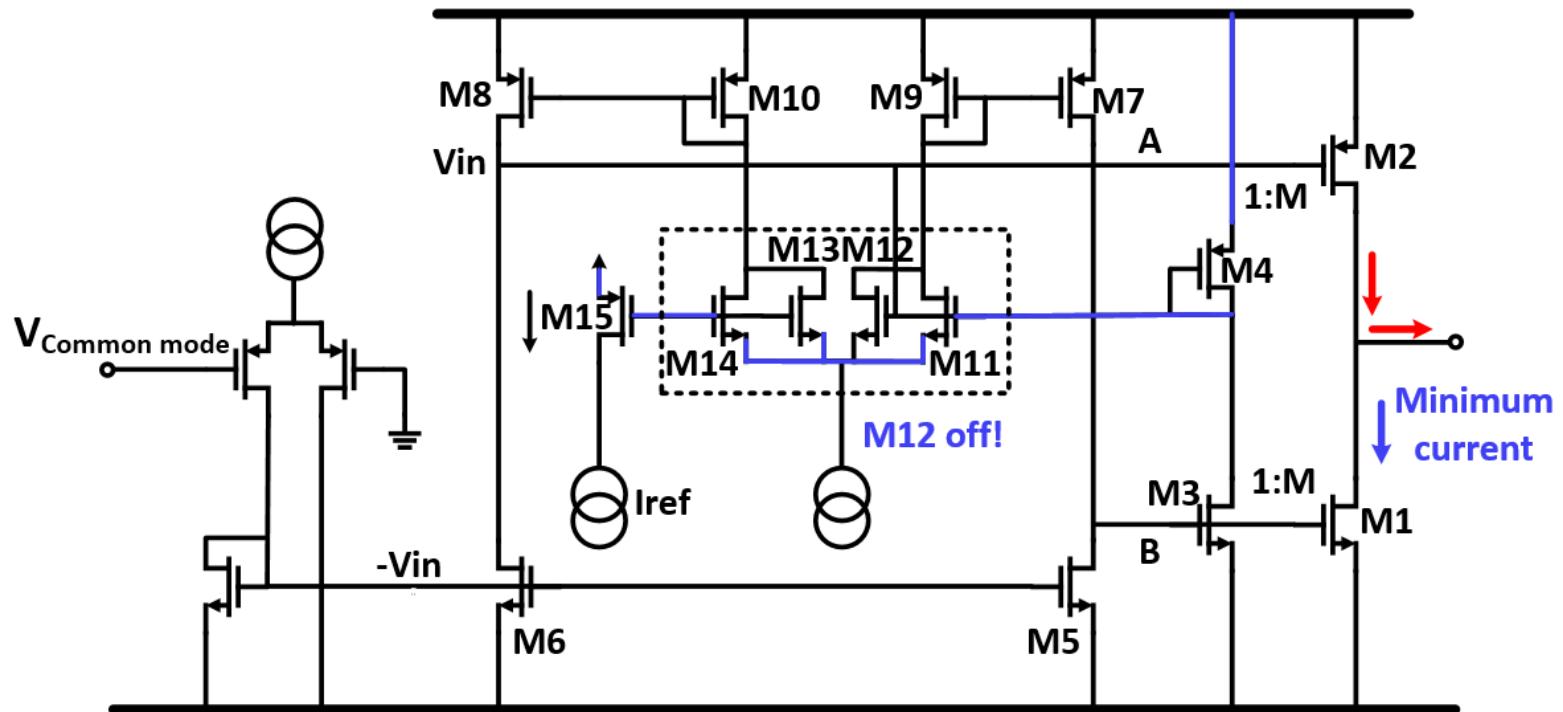




Class-AB级

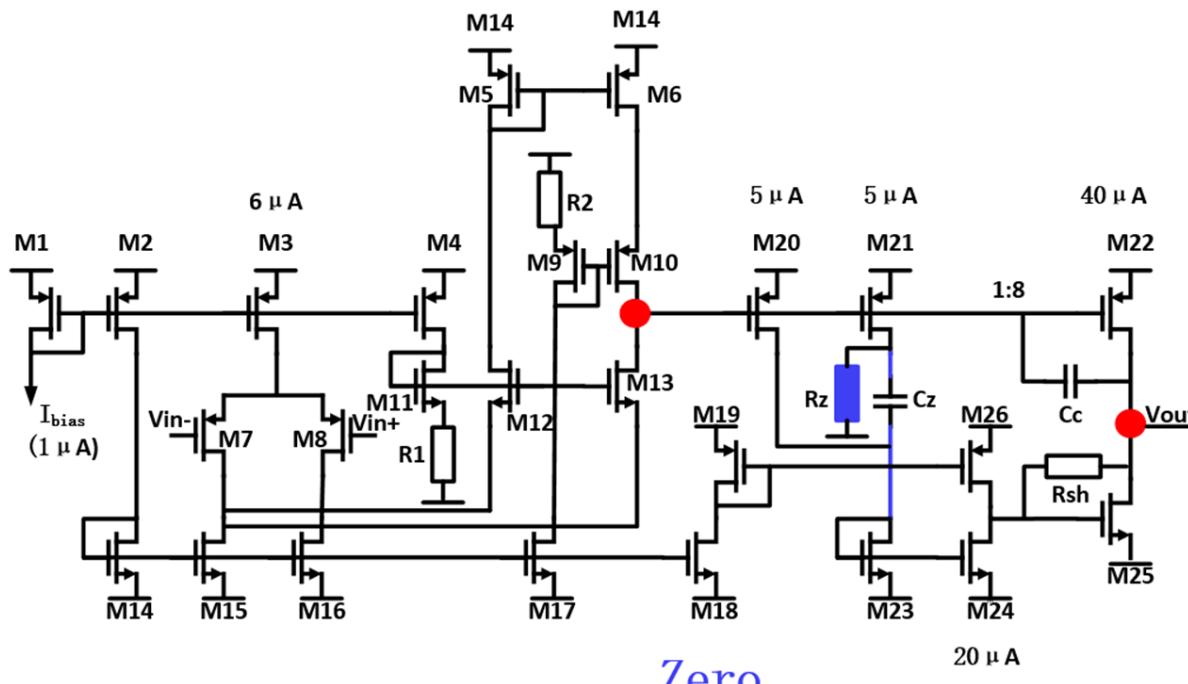
- 什么是Class-AB级
- 静态电流控制方法
 - 交叉耦合差分对
 - 动态偏置技术
 - 线性跨导回路
- 其他

》》 线性跨导回路:多回路叠加



- ✓ M3/M4检测输出电流
- ✓ 防止一侧输出晶体管在另一侧大电流输出时关断

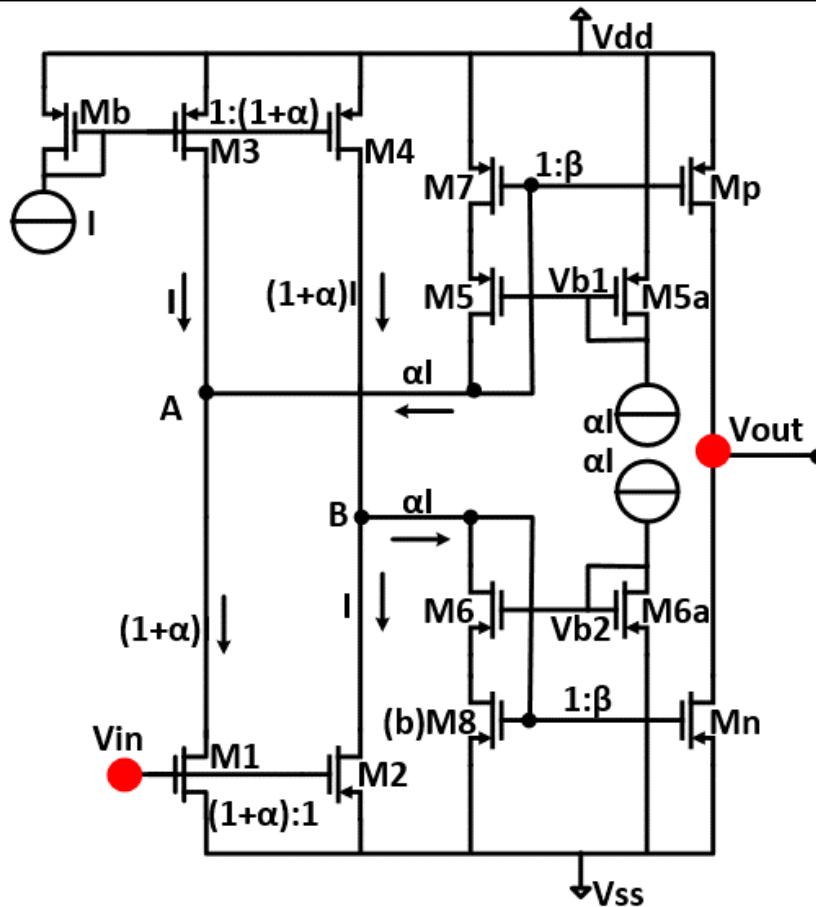
》》低电压实现I



Ref. Van Dongen, JSSC Dec.95, 1333-1337

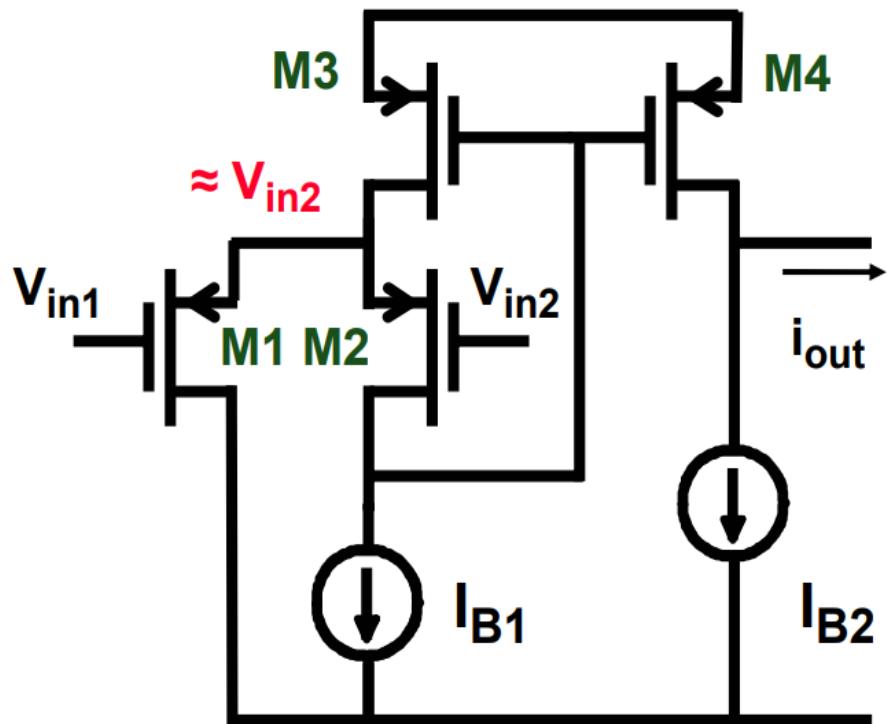
- ✓ 第一级输出直接驱动Class-AB级的输入
- ✓ 静态电流的驱动没有很好的控制

》》低电压实现II



- 静态电流控制优秀
- 在A点和B点获得最大摆幅，使得输出电流远大于静态电流
- $\alpha=0.2$
 - 取值在增益和失配间平衡
- $\beta=120$

》》低电压实现III



M2是一个源极跟随器

$$V_{GS1} = V_{in1} - V_{in2}$$

$$i_{out} \sim (V_{in1} - V_{in2})^2$$

>>> Class AB

第 11 章 ADC & DAC



北京航空航天大學
BEIHANG UNIVERSITY

| 微电子学院

CMOS模拟集成电路设计

第十章：奈奎斯特转换器： ADC & DAC

胡远奇

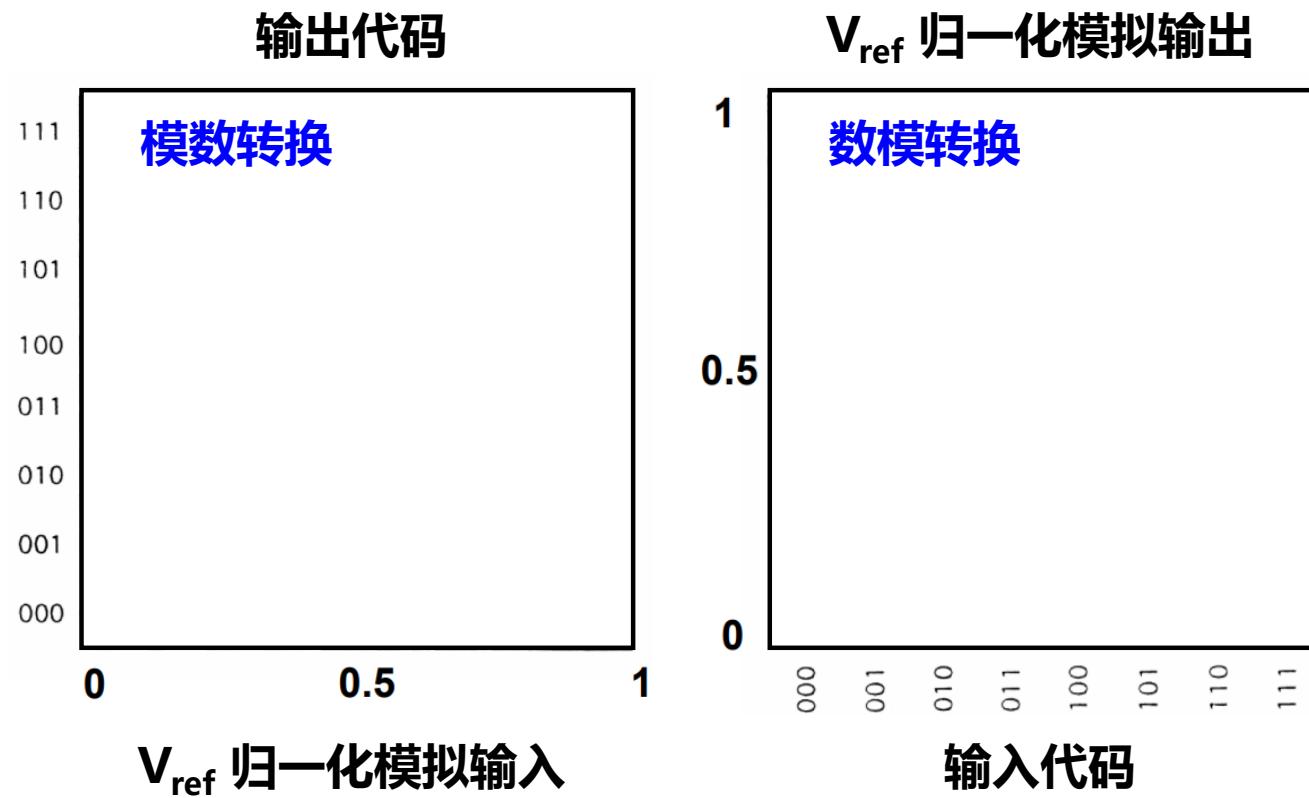
©2020



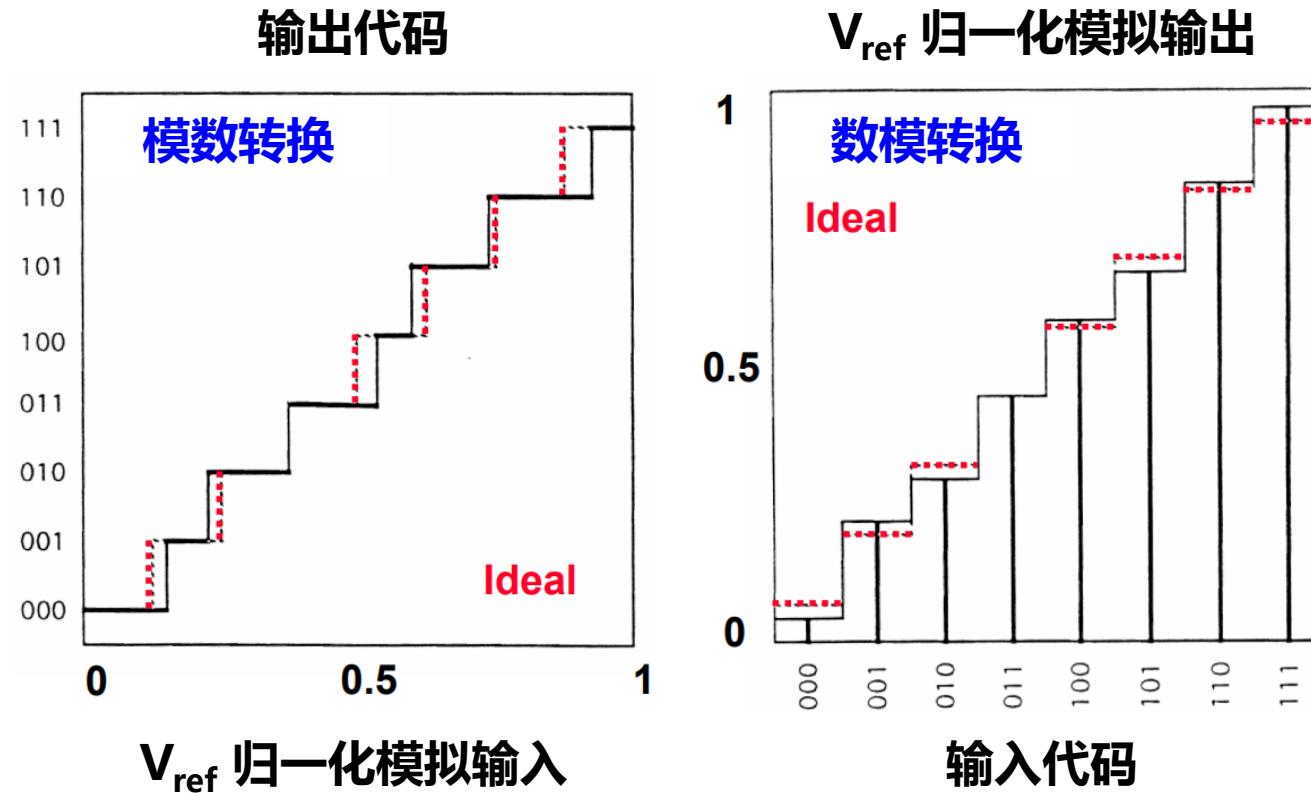
ADC & DAC

- 定义
- 数字-模拟转换器
 - 电阻式
 - 电容式
 - 电流驱动
- 模拟-数字转换器
 - 积分式
 - 逐次渐进式
 - Flash

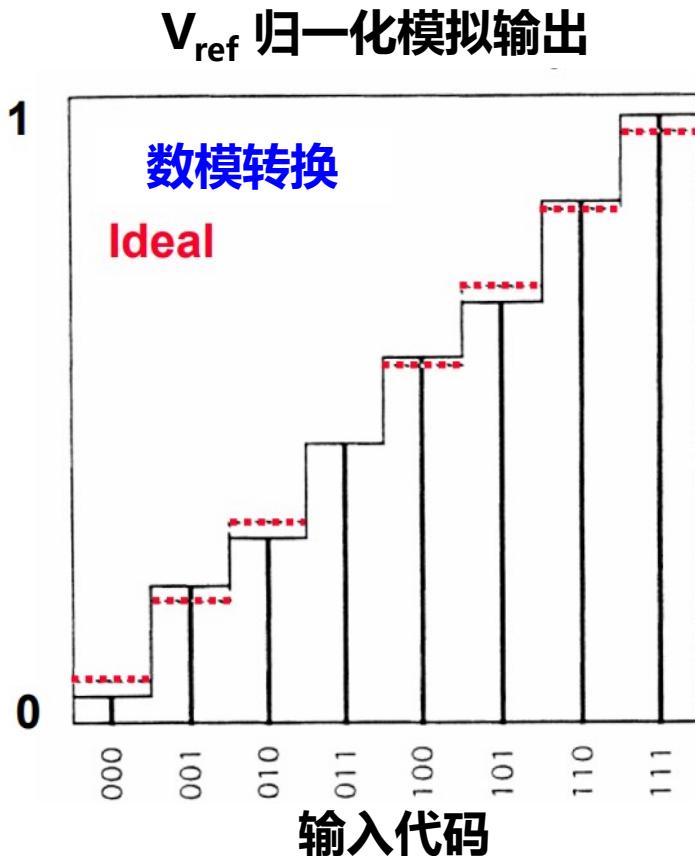
»» ADC & DAC



»» ADC & DAC



》》 DAC的分辨率



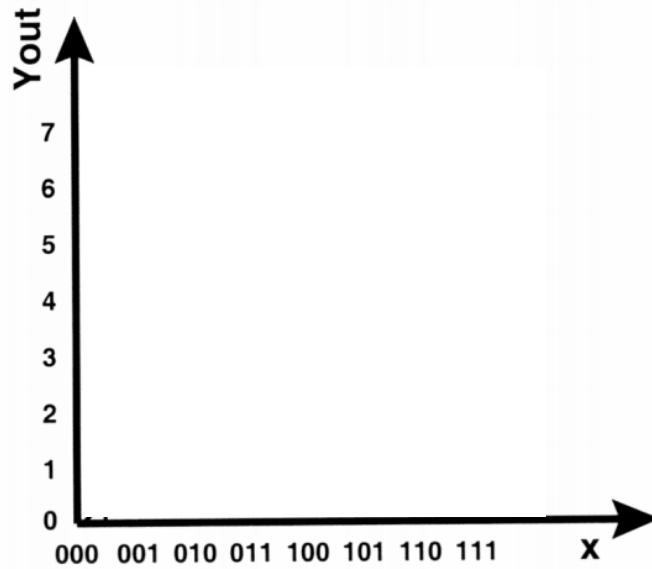
$$\begin{aligned} V_{\text{OUT}} &= V_{\text{REF}} B_{\text{IN}} \\ &= V_{\text{REF}} \left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \dots + \frac{b_N}{2^N} \right) \end{aligned}$$

$$V_{\text{LSB}} = \frac{V_{\text{REF}}}{2^N}$$

b₁ 最高有效位
Most Significant bit (MSB)

b_N 最低有效位
Least Significant bit (LSB)

» 量化误差(Quantisation Error)

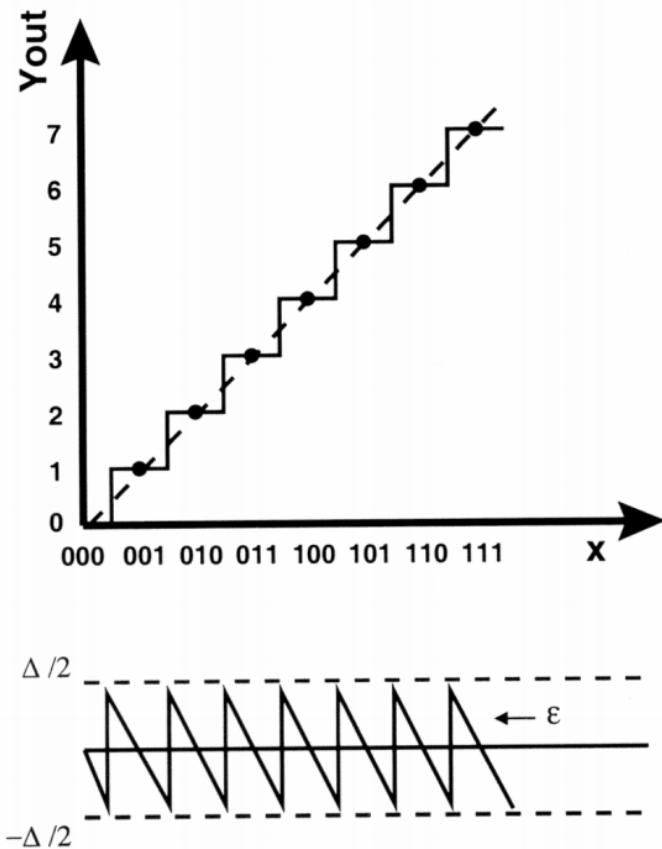


$$P_{\text{Noise}} =$$

$$P_{\text{Signal}} =$$

误差

》》量化误差



$$P_{\text{Noise}} = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} \varepsilon^2 d\varepsilon = \frac{\Delta^2}{12}$$

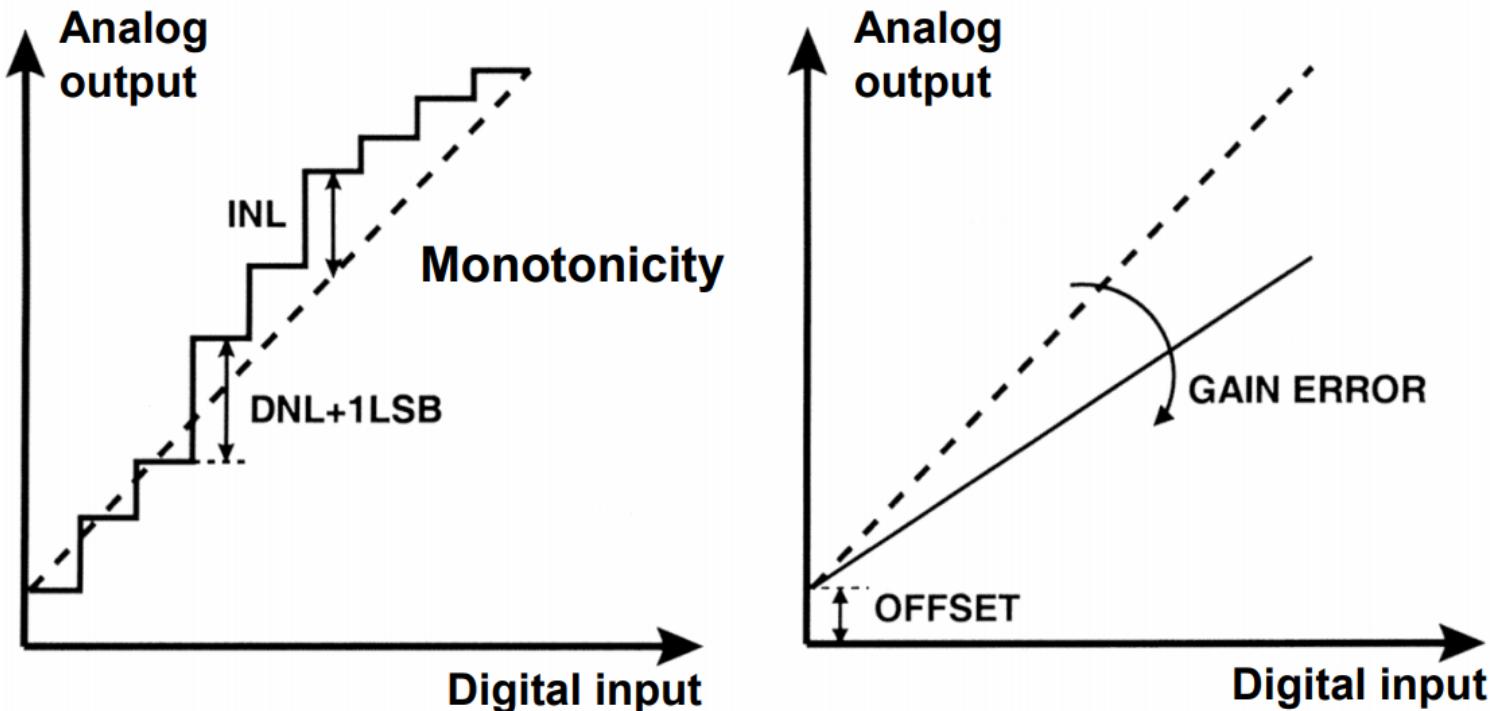
$$V_{\text{ptp}} = 2^N \Delta$$

$$P_{\text{Signal}} = \frac{V_{\text{ptp}}^2}{8}$$

$$\text{SNR} = \frac{3}{2} 2^{2N}$$

$$\text{SNR} = 6 N + 1.76 \text{ dB}$$

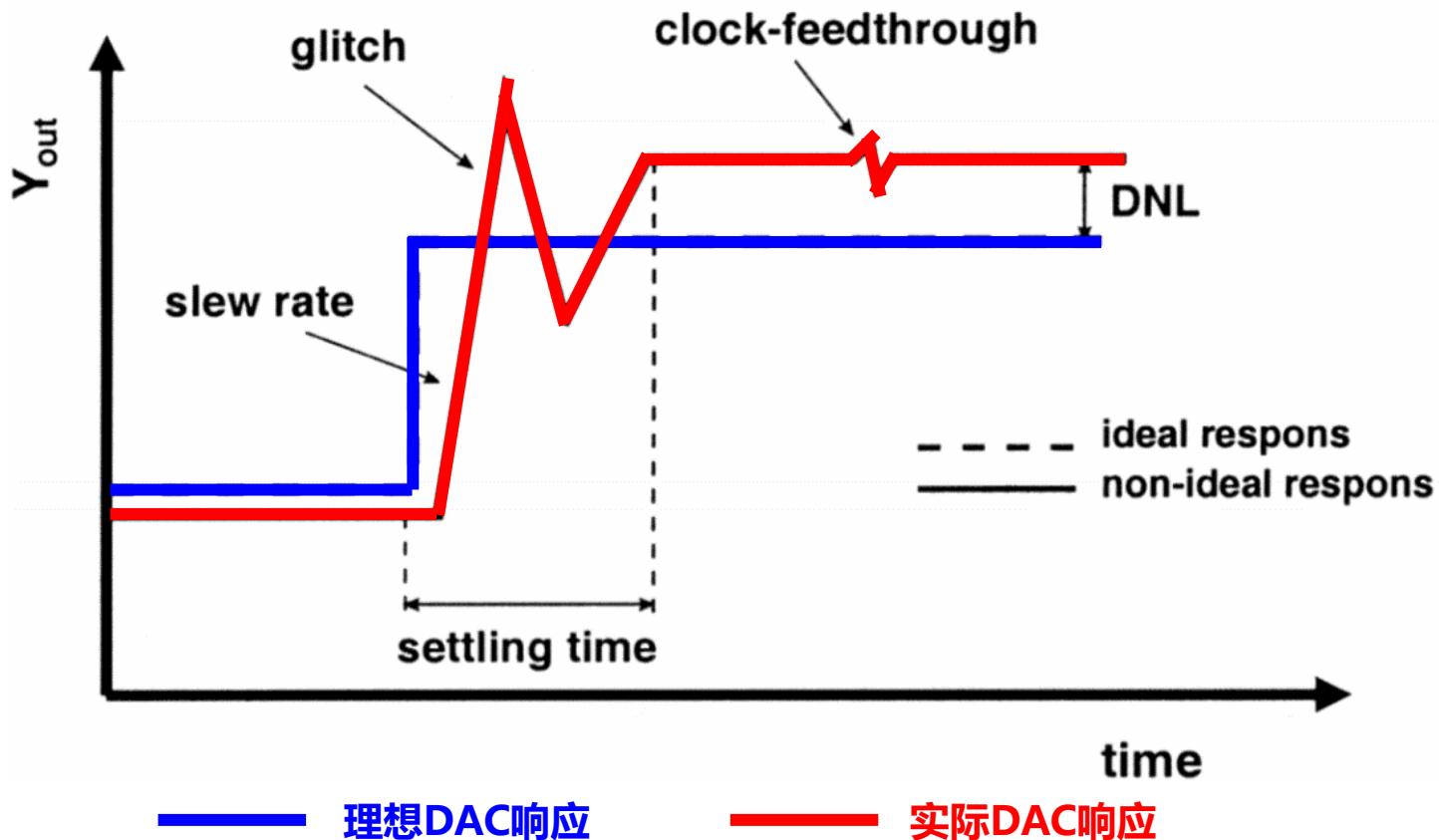
» 静态指标: INL & DNL



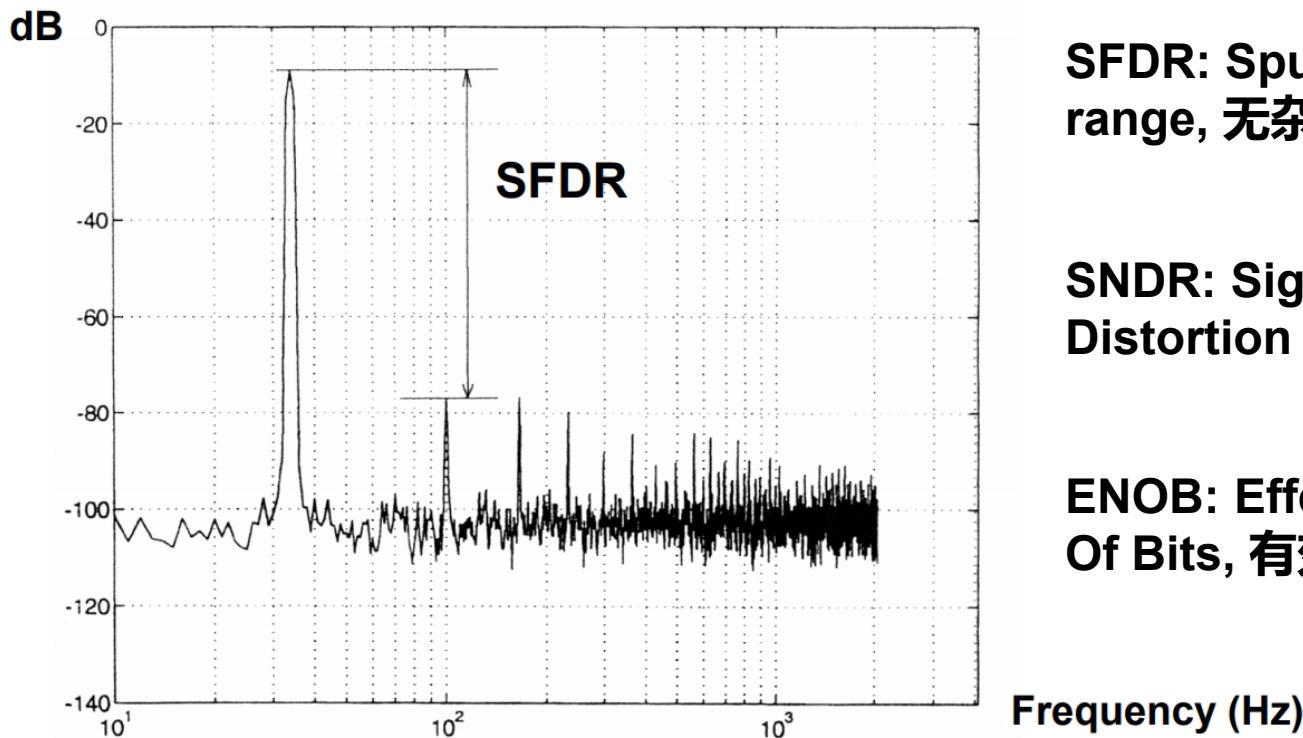
差分非线性度 (Differential Nonlinearity) : $DNL = Y_{OUT}(B) - Y_{OUT}(B-1) - 1 \text{ LSB}$

积分非线性度 (Integral Nonlinearity) : $INL = Y_{OUT}(B) - Y_{OUT,id}(B)$

》》 动态指标



》》 频谱内容

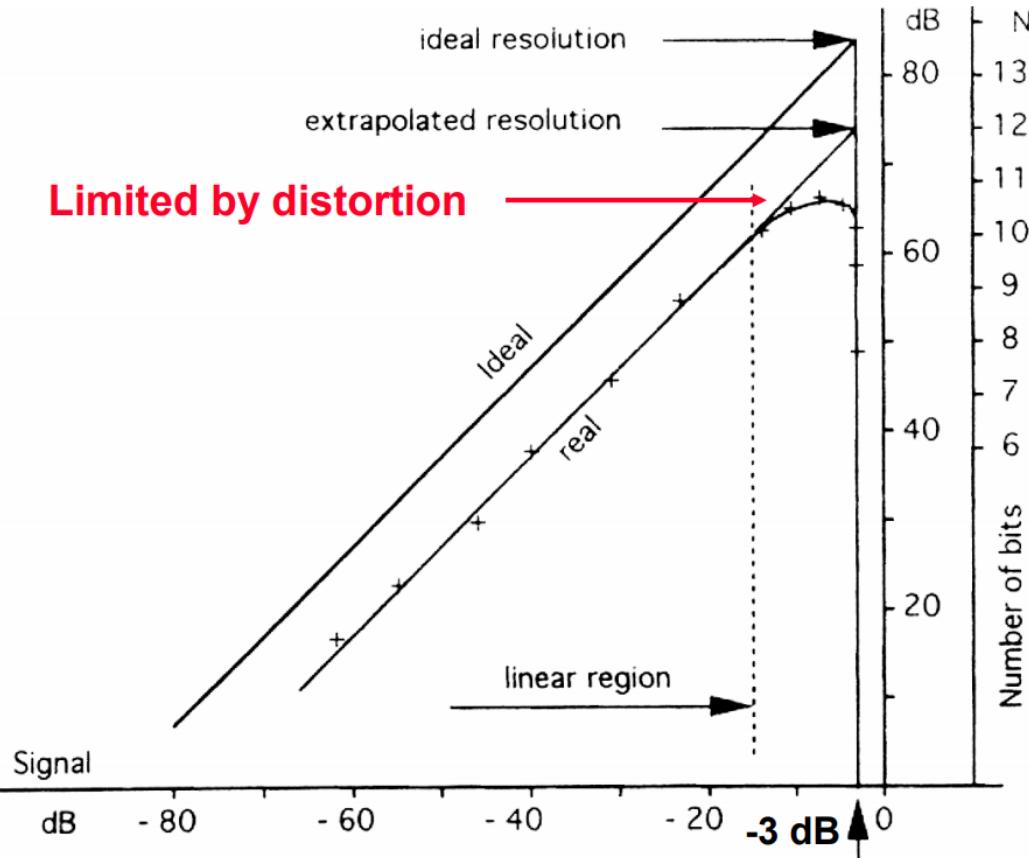


SFDR: Spurious free dynamic range, 无杂散动态范围

SNDR: Signal to Noise & Distortion Ratio, 信噪失真比

ENOB: Effective Number Of Bits, 有效位数

信噪比与输入信号的关系



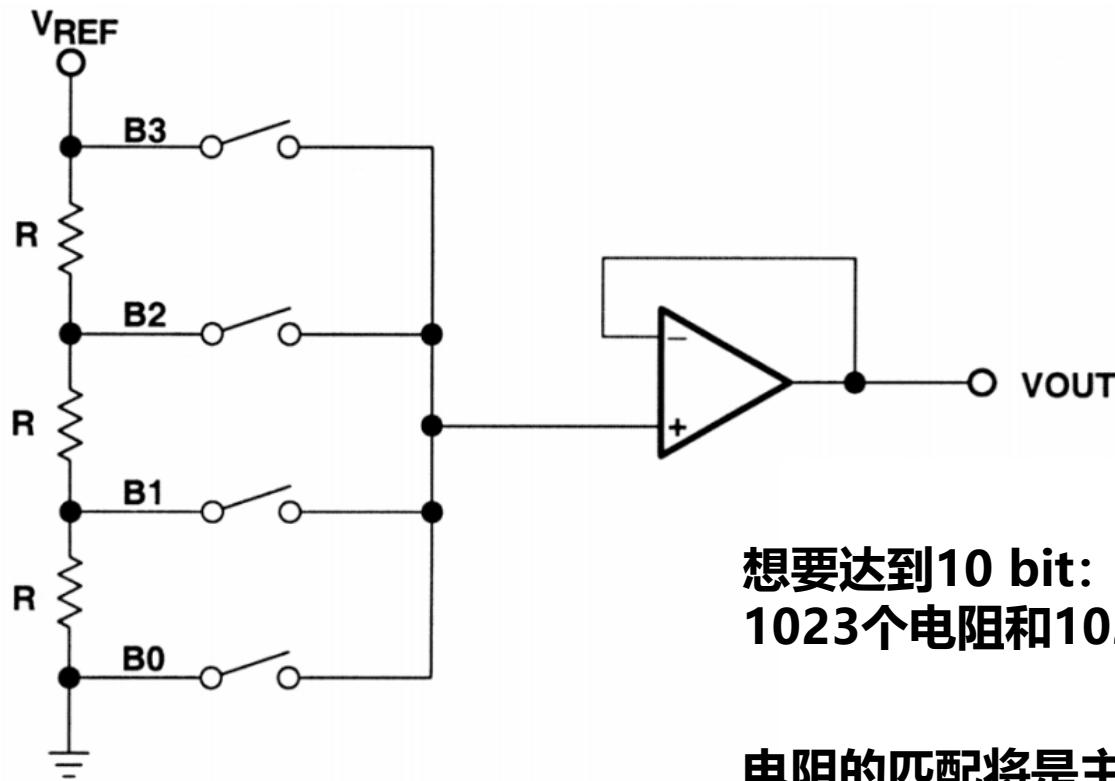
系统的有效分辨率被大输入信号的失真所限制，原本可以达到**74dB/12位**分辨率的系统，最终只实现了**66dB/10.6位**



ADC & DAC

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 - 积分式
 - 逐次渐进式
 - Flash

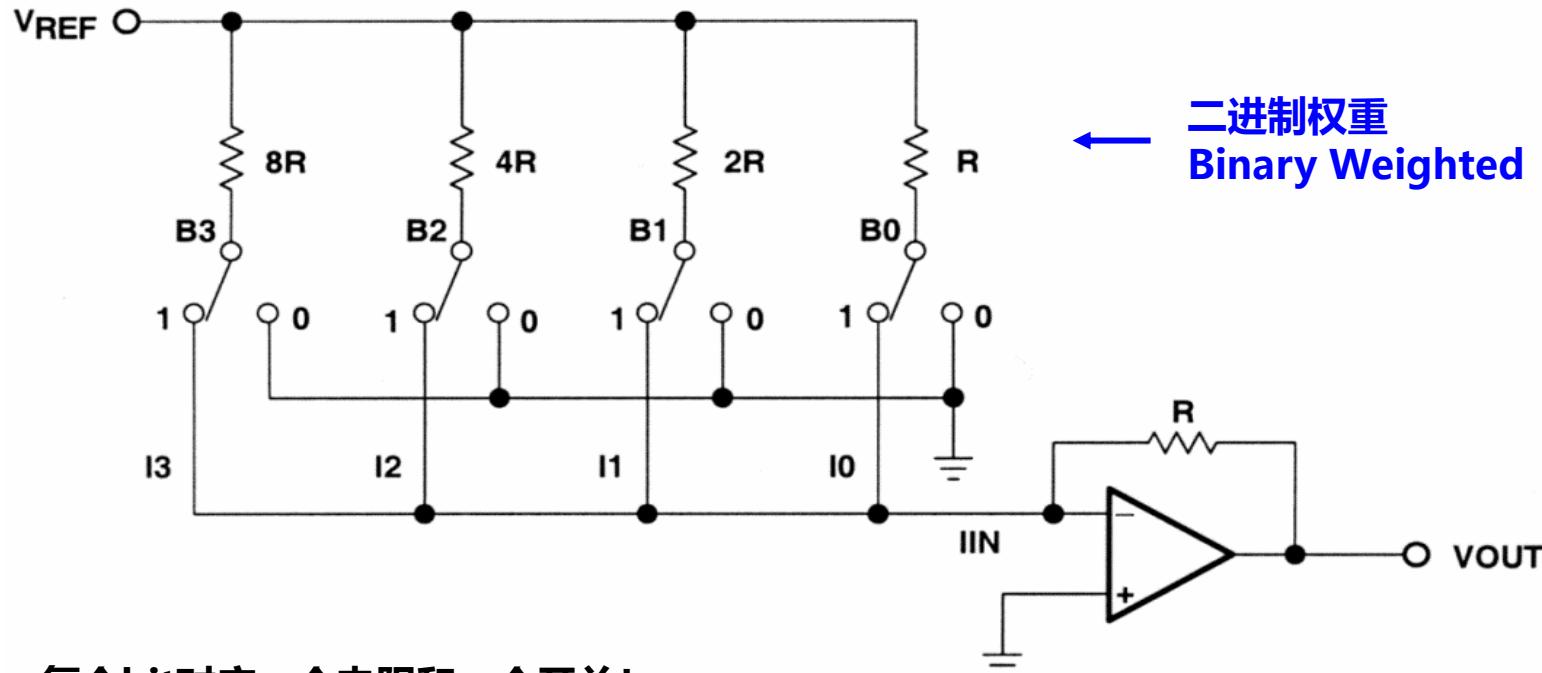
》》 电阻操控型DAC



想要达到10 bit:
1023个电阻和1024个开关!

电阻的匹配将是主要的问题!

》》二进制权重电阻的DAC

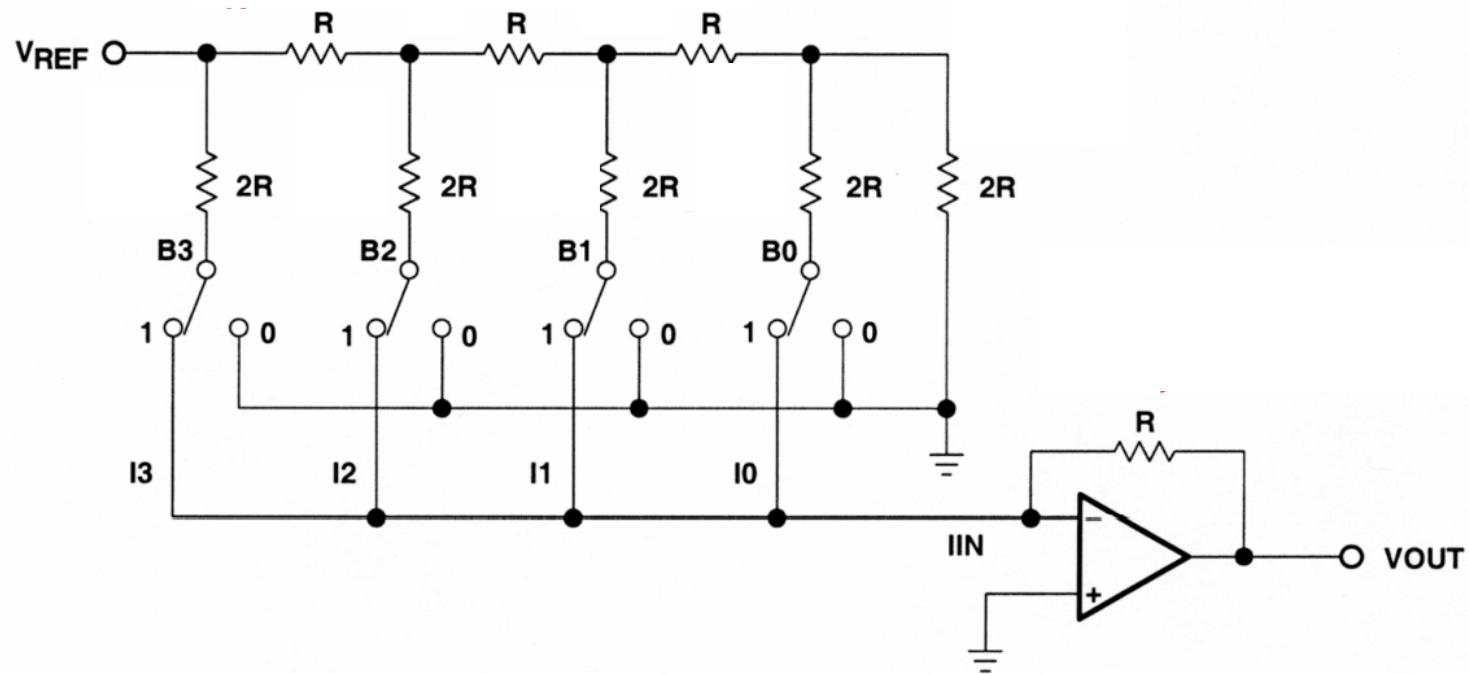


每个bit对应一个电阻和一个开关!

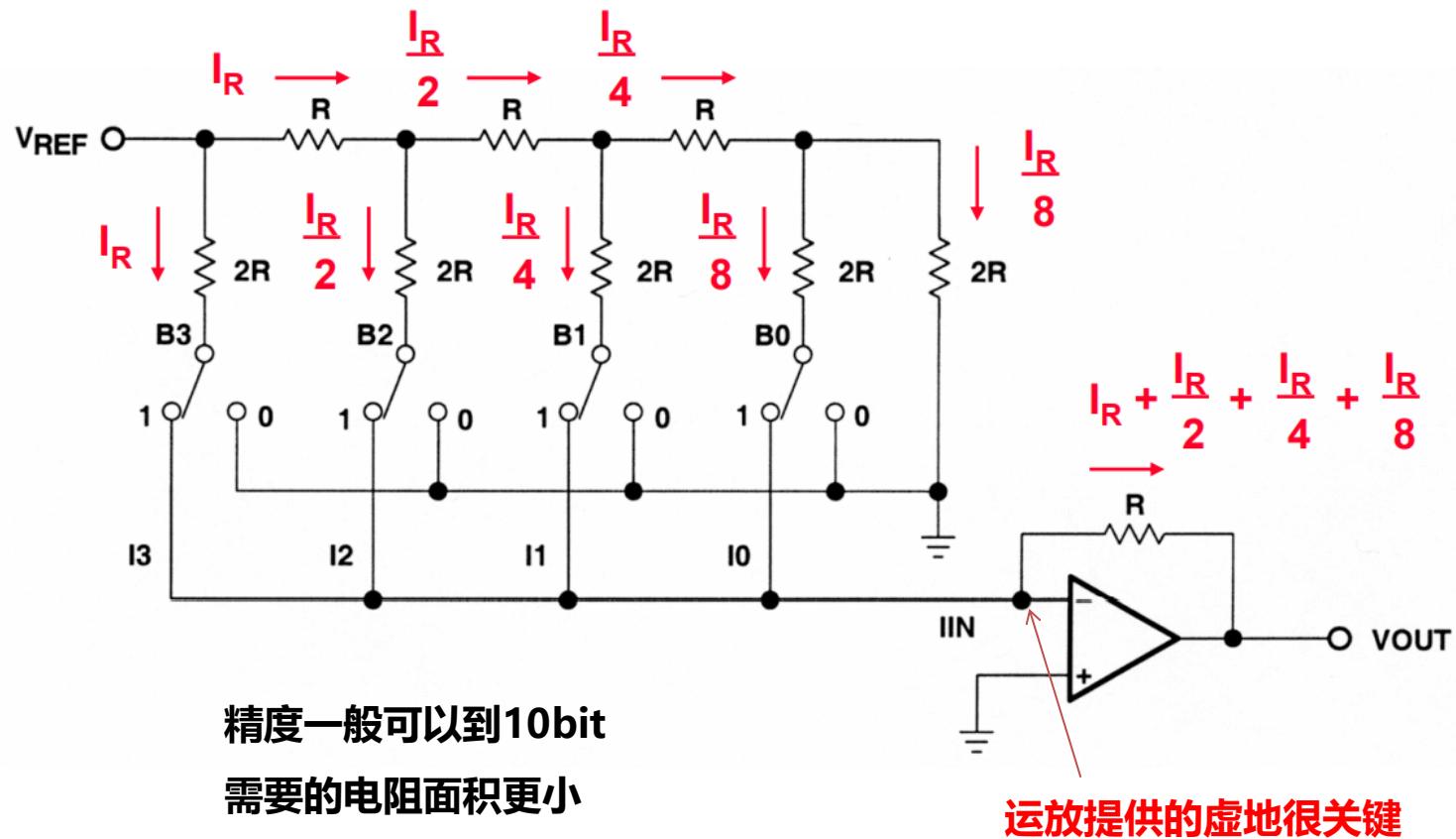
对匹配的要求更高! ➡ 匹配的精度极限一般在6-8 bits

二进制权重中**单一性**没法得到保证!

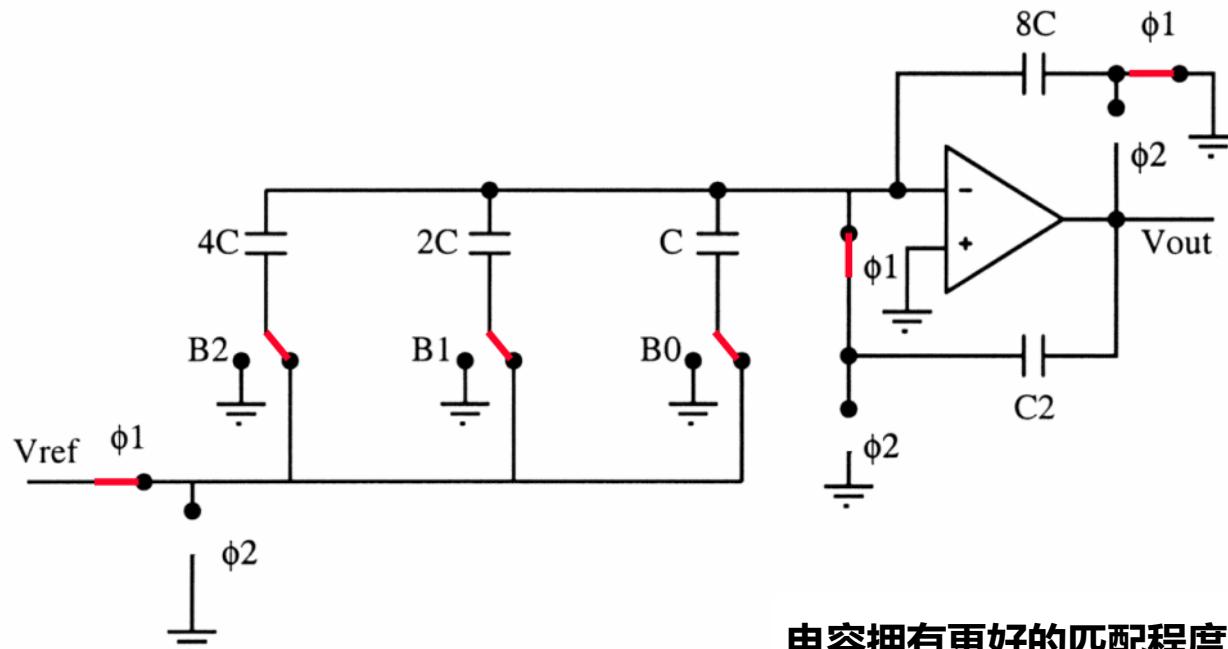
》》 R-2R 阶梯型DAC



»» R-2R 阶梯型DAC



》》电容的实现方式



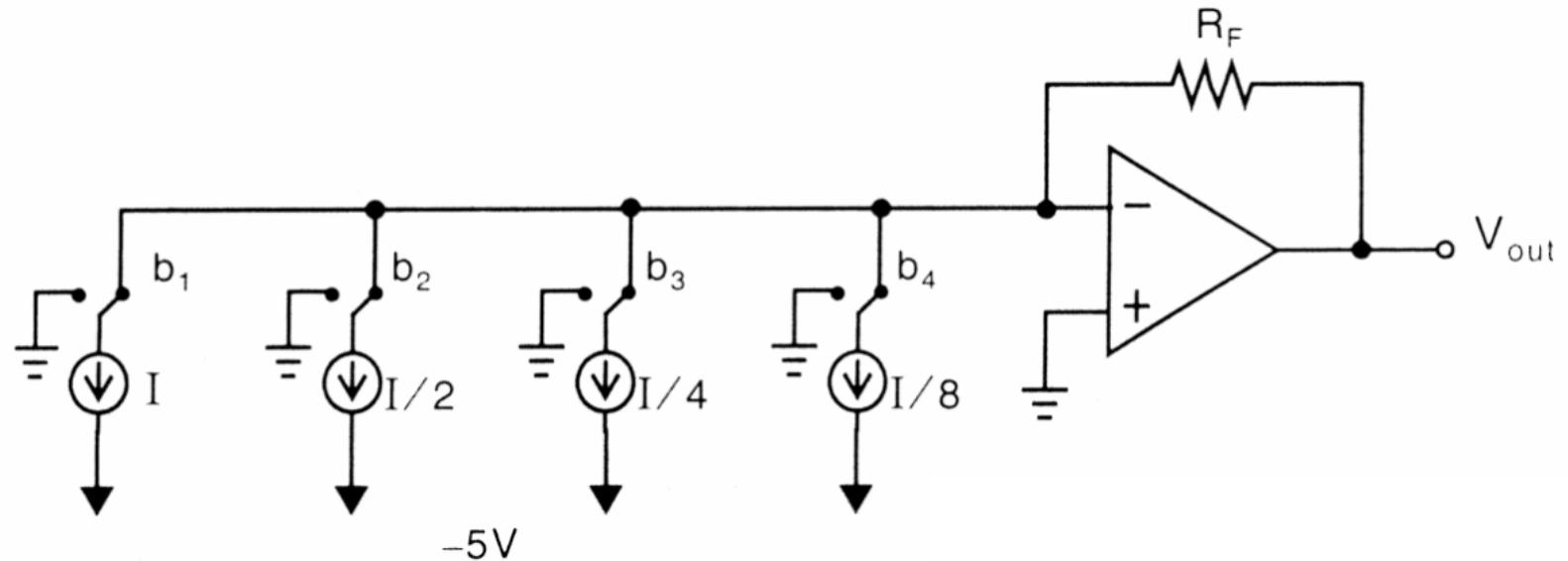
Phase Φ1: 电容采样

电容拥有更好的匹配程度！

通常能获得比电阻高2bit的精度

Phase Φ2: 电容放大

» 电流转向DAC



□ 转换精度的限制是什么?

□ 一致性的能否得到保证?



- 电流镜的匹配
- 不能



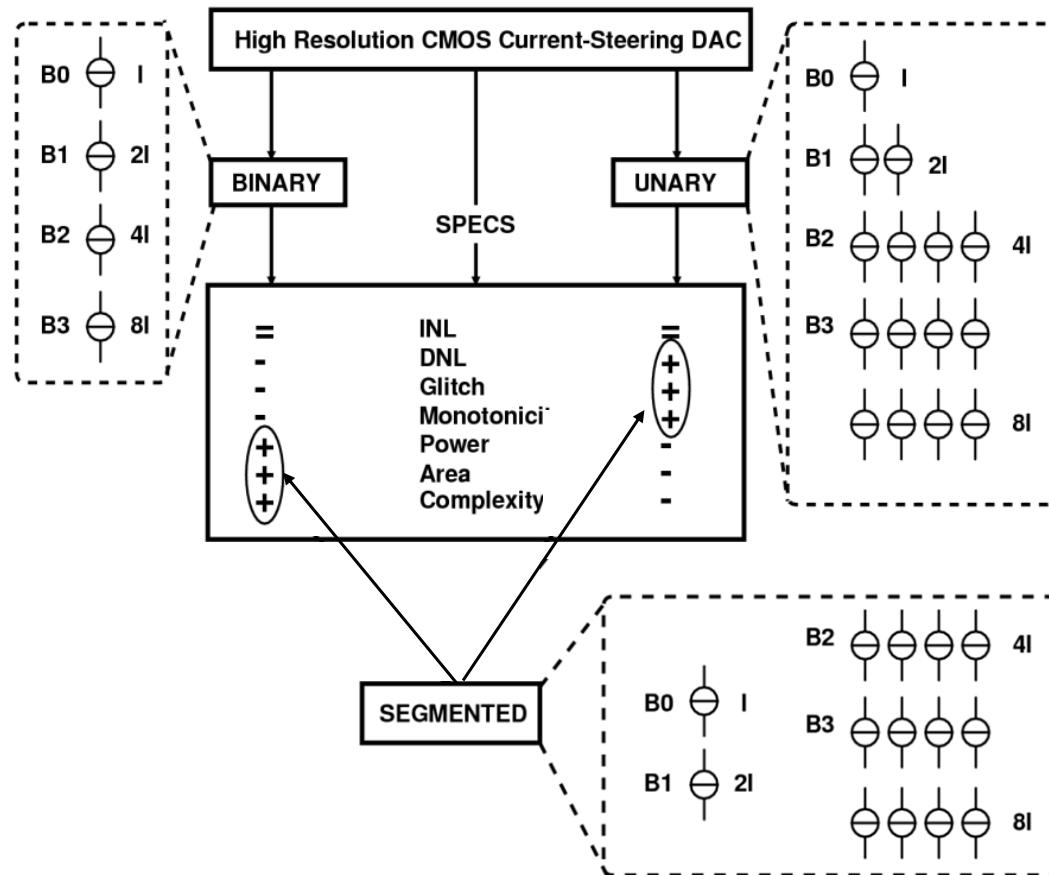
二进制和热码编码

Decimal	Binary			Thermometer Code						
	b_1	b_2	b_3	d_1	d_2	d_3	d_4	d_5	d_6	d_7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

单调性可以得到保证！

以更多的基本元件、开关和逻辑器件为代价

》》组合方案



$$\sigma(\Delta I) =$$

Binary

$$\sqrt{2^N - 1} \frac{\sigma(I)}{I} \text{ LSB}$$

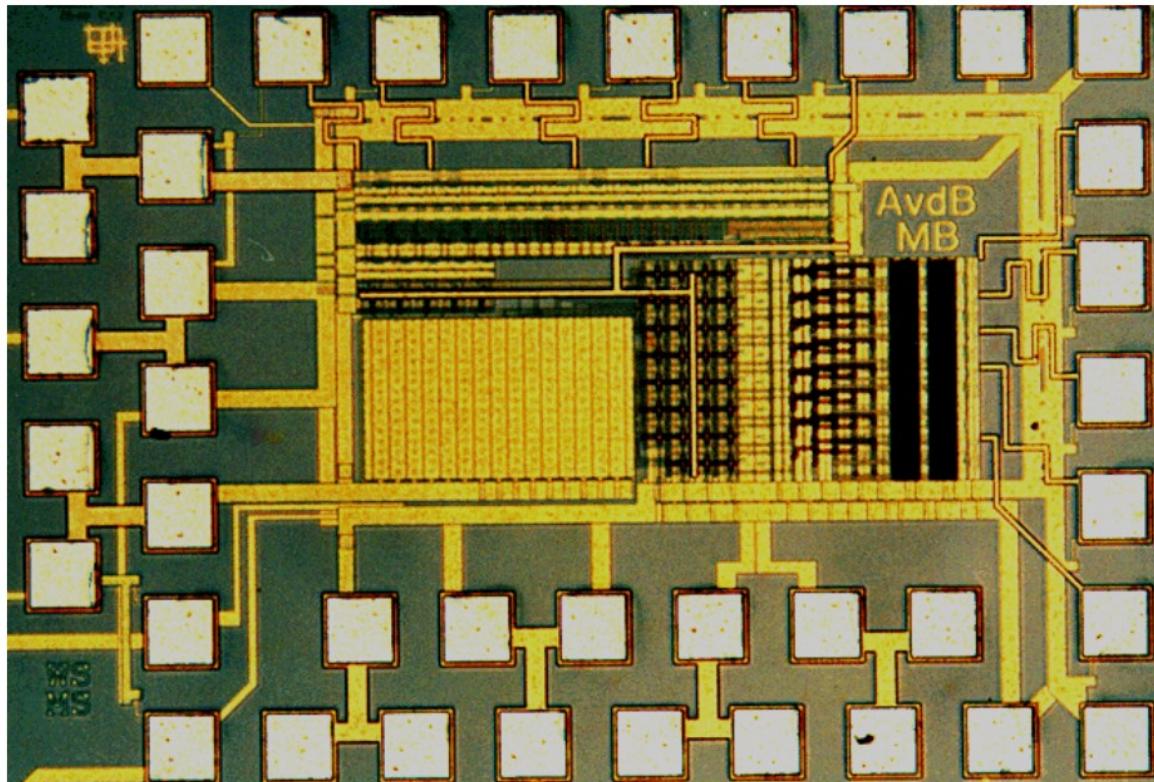
Unary

$$\frac{\sigma(I)}{I} \text{ LSB}$$

Segmented
B LSBs & N-B MSBs

$$\sqrt{2^{B+1} - 1} \frac{\sigma(I)}{I} \text{ LSB}$$

》》 电流转向DAC案例



Current steering
DAC
10-bit
1 GS/s
0.35 μm CMOS
110 mW

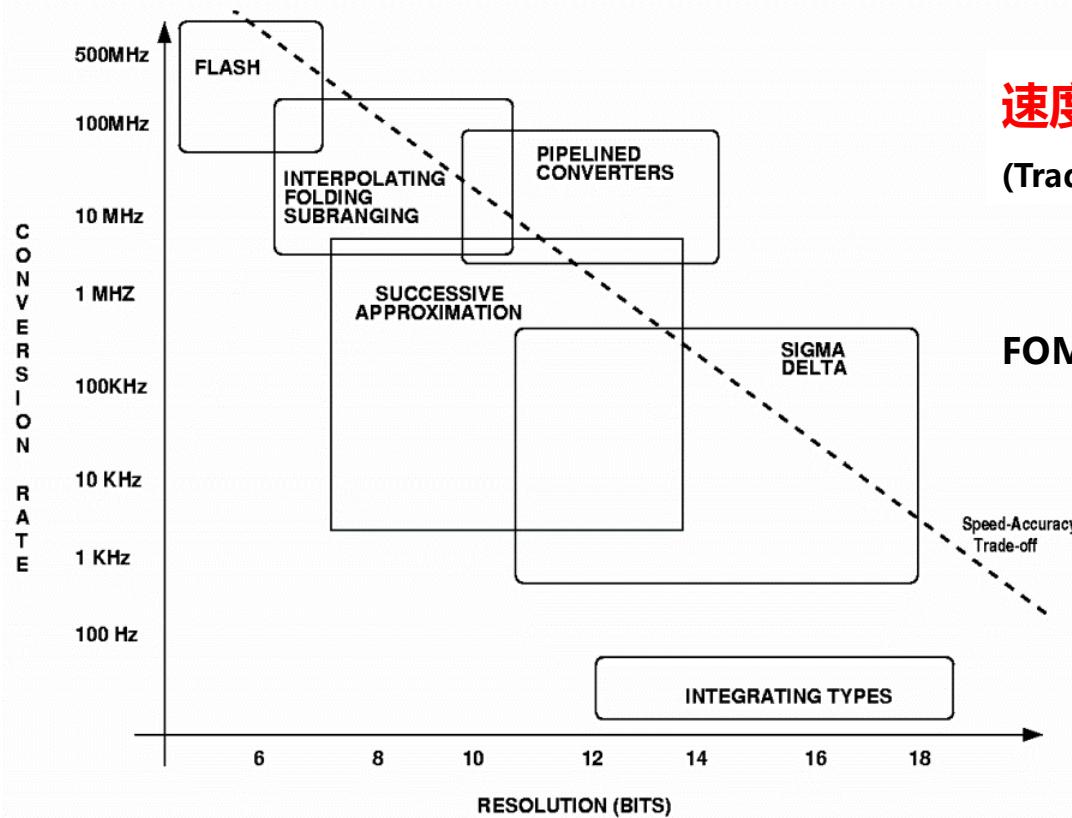
Van den Bosch, ..., JSSC, March 01, 315-324



ADC & DAC

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 - Flash

ADC的种类

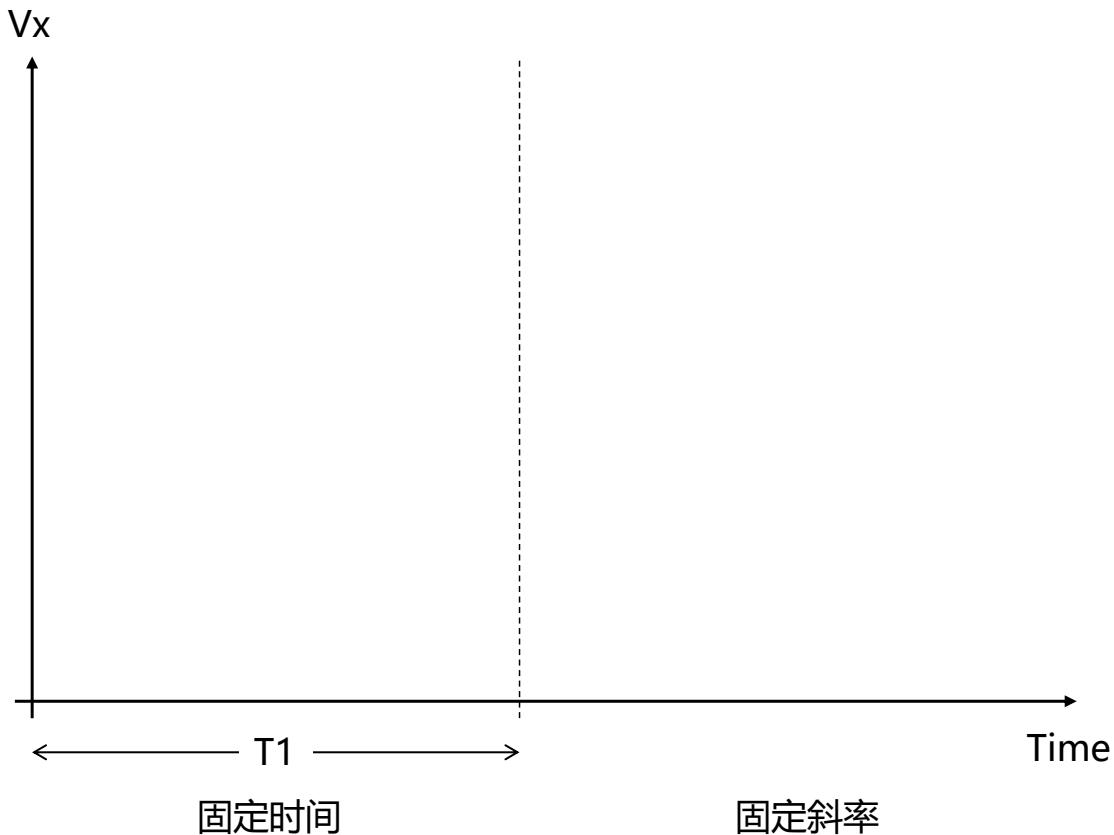


速度与精度的平衡

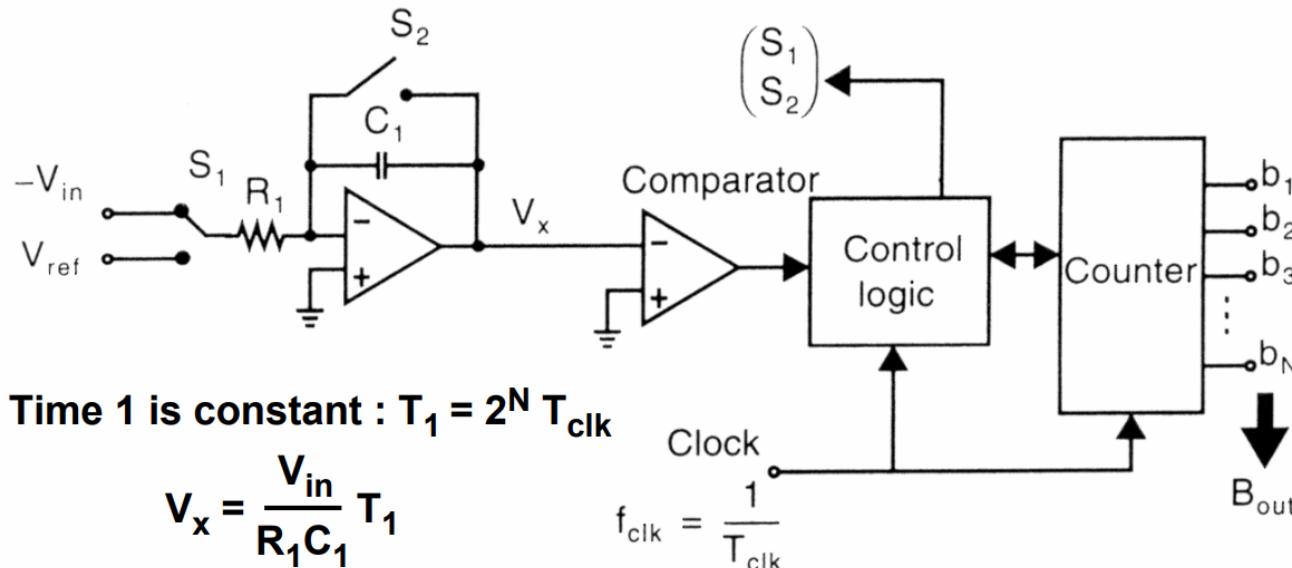
(Tradeoff between Speed and Resolution)

$$FOM = \frac{2^N 2BW}{P}$$

》》 积分型ADC (Dual-slope)



》》 积分型ADC (Dual-slope)



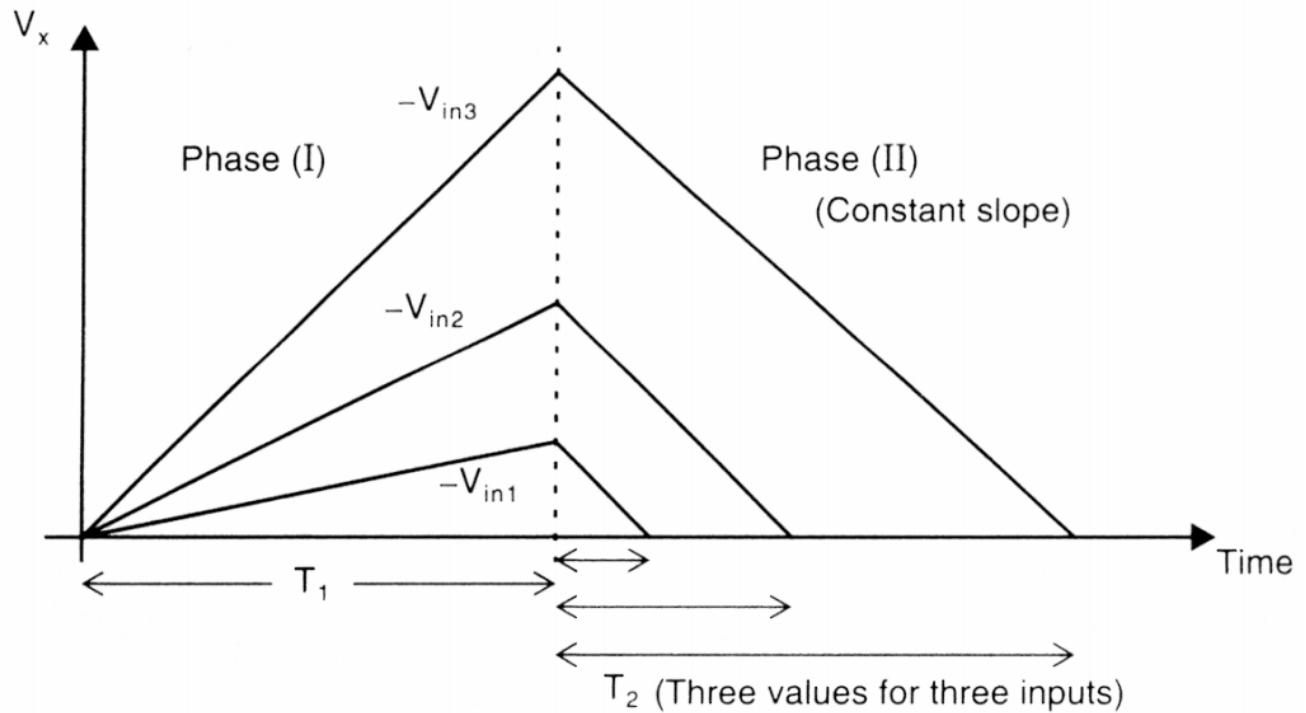
Time 2 : V_x decreases with constant slope :

$$V_x = \frac{V_{\text{ref}}}{R_1 C_1} T_2$$

$$T_2 = T_1 \frac{V_{\text{in}}}{V_{\text{ref}}} \quad \Rightarrow \quad B_{\text{out}} = \frac{V_{\text{in}}}{V_{\text{ref}}}$$

相同的硬件，没有匹配的问题！

》》 积分型ADC (Dual-slope)



$$\text{Time 1 : } V_x = \frac{V_{in}}{R_1 C_1} T_1$$

$$\text{Time 2 : } V_x = \frac{V_{ref}}{R_1 C_1} T_2$$

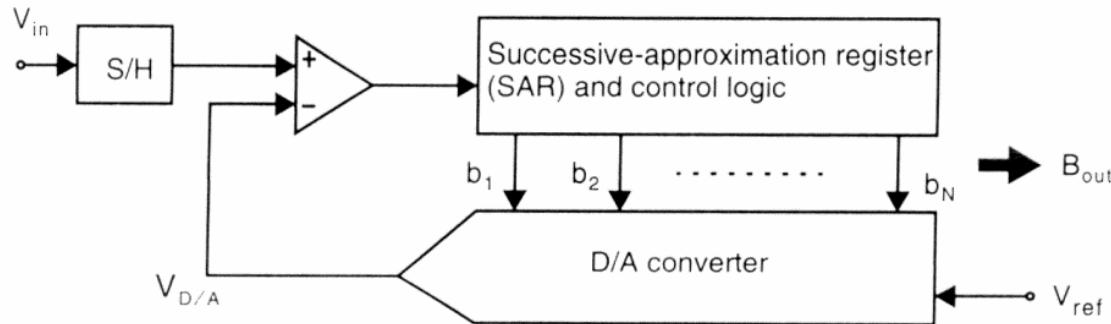
$$T_2 = T_1 \frac{V_{in}}{V_{ref}}$$



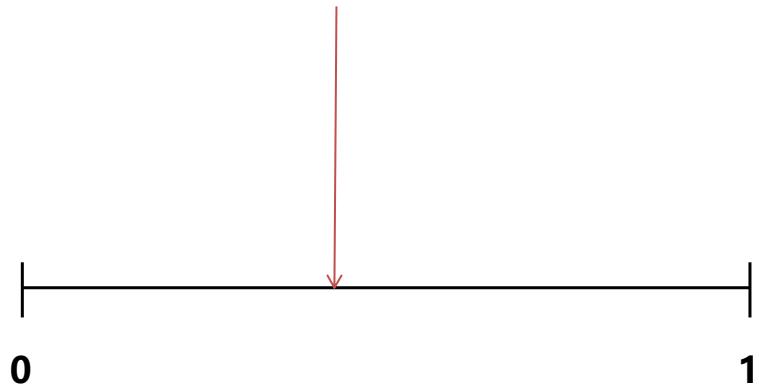
积分型ADC (Dual-slope)

- 优点：
 - 高分辨率
 - 高线性度
 - 低电路复杂度
- 缺点：
 - 十分慢！
 - 通常在电压表中使用

逐次逼近型ADC



$V_{in}=0.4$



假设全量程为1，每次比较剩余量的1/2：

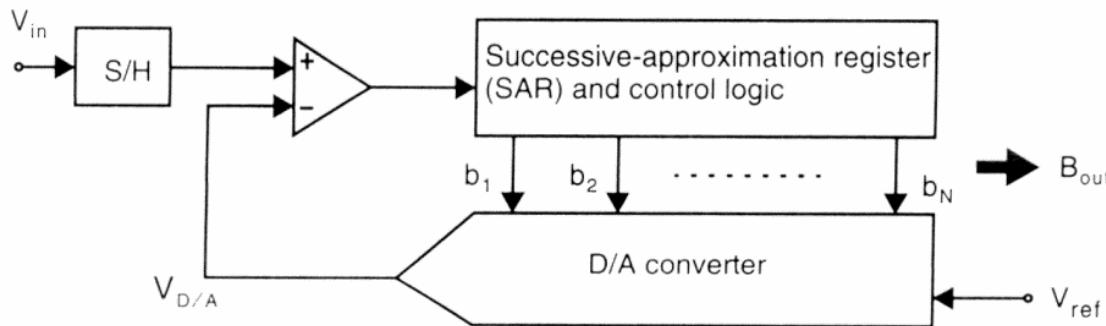
>0.5? : 0 $b_1=0$

>0.25? : 1 $b_2=1$

>0.375? : 1 $b_3=1$

>0.4375? : 1 $b_4=0$

逐次逼近型ADC



假设全量程为1，每次比较剩余量的 $1/2$:

- N-bit ADC仅需N个时钟周期
- 对比较器的失调电压敏感
- DAC的实现决定ADC的精度

>0.5? : 0 b1=0

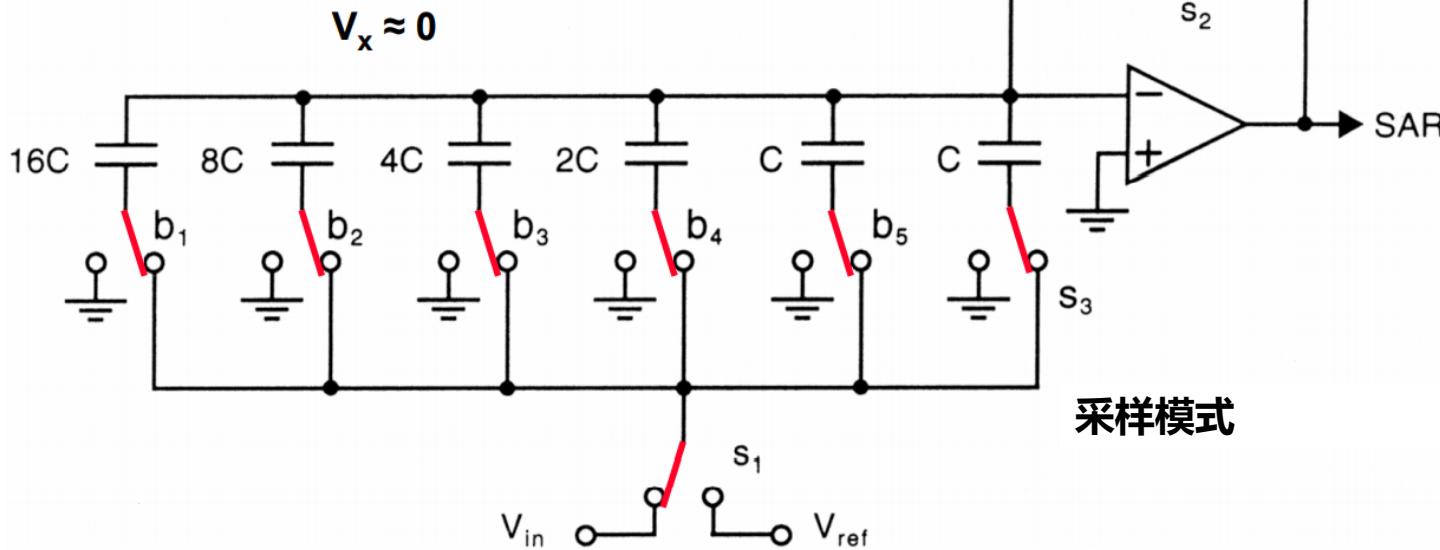
>0.25? : 1 b2=1

>0.375? : 1 b3=1

>0.4375? : 1 b4=0

》》 5-bit 电荷重分布 ADC

$$\Sigma = 2^N C$$

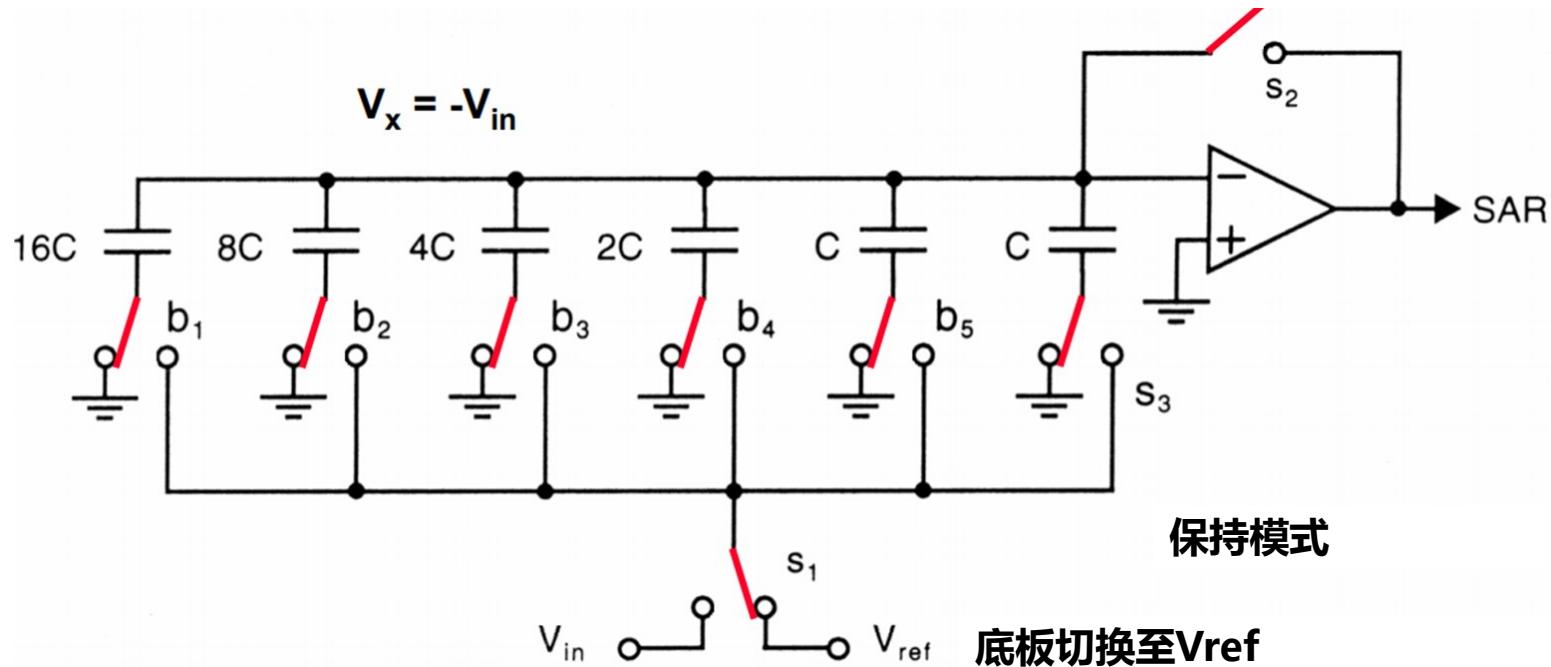


分辨率由电容的匹配决定，通过可以达到10-12 bits

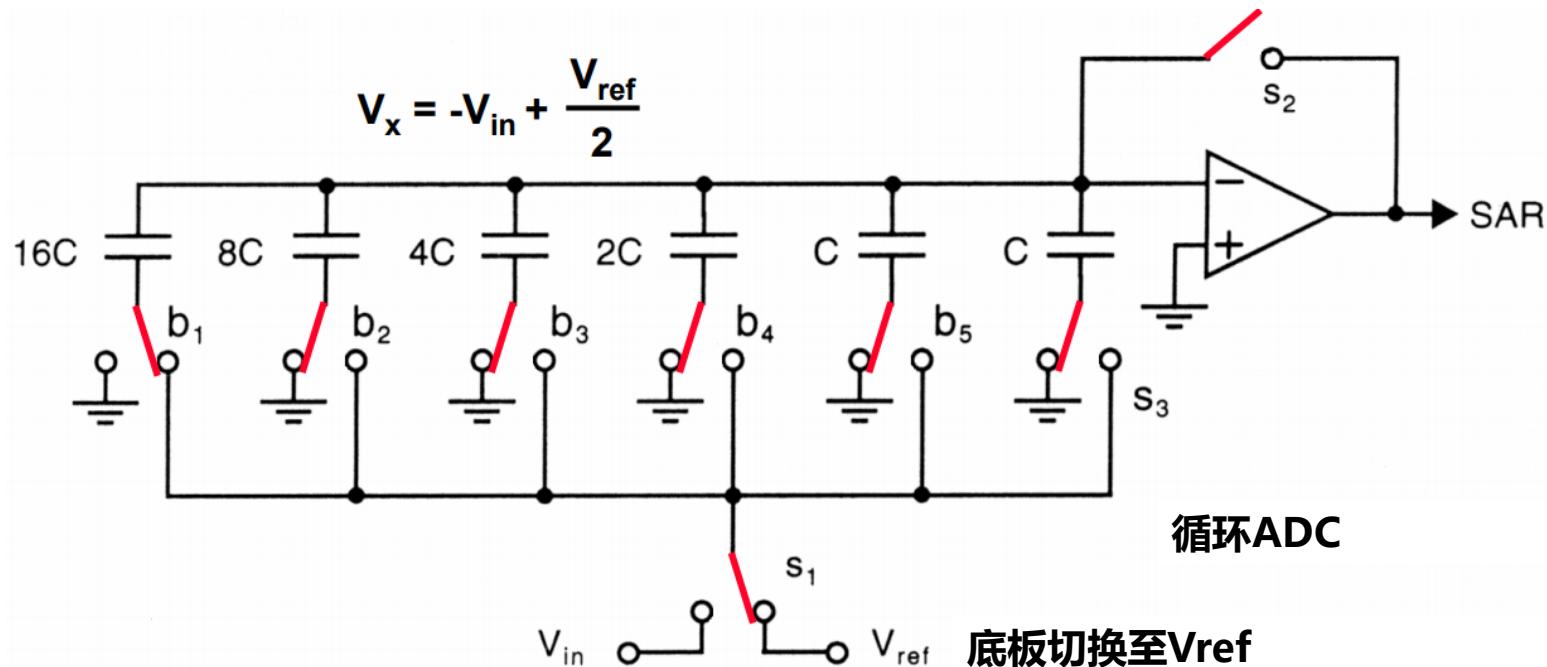
速度由开关电阻和电容组成的时间常数决定

电路较简单，功耗较低

》》 5-bit 电荷重分布 ADC



》》 5-bit 电荷重分布 ADC

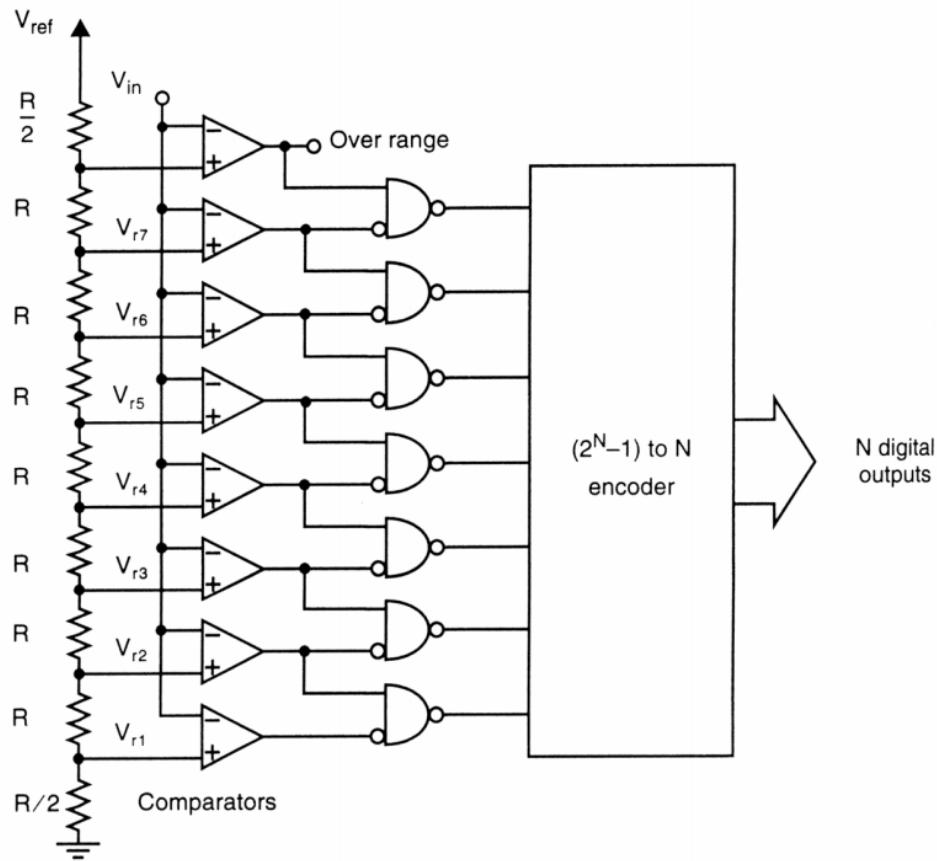


if $V_{in} > V_{ref}/2$
if $V_{in} < V_{ref}/2$

$SAR \Rightarrow 1$
 $SAR \Rightarrow 0$

leave C_{b1} to V_{ref} : try C_{b2}
leave C_{b1} to Gnd : try C_{b2}

Flash ADC



3-bit Flash ADC

速度最快，仅需1个时钟周期

需要 2^N 个比较器

精度通常在6-8bit

大输入电容！

»» ADC 设计总体思路

晶体管： $\sigma^2(\text{Error}) \sim \frac{1}{WL}$

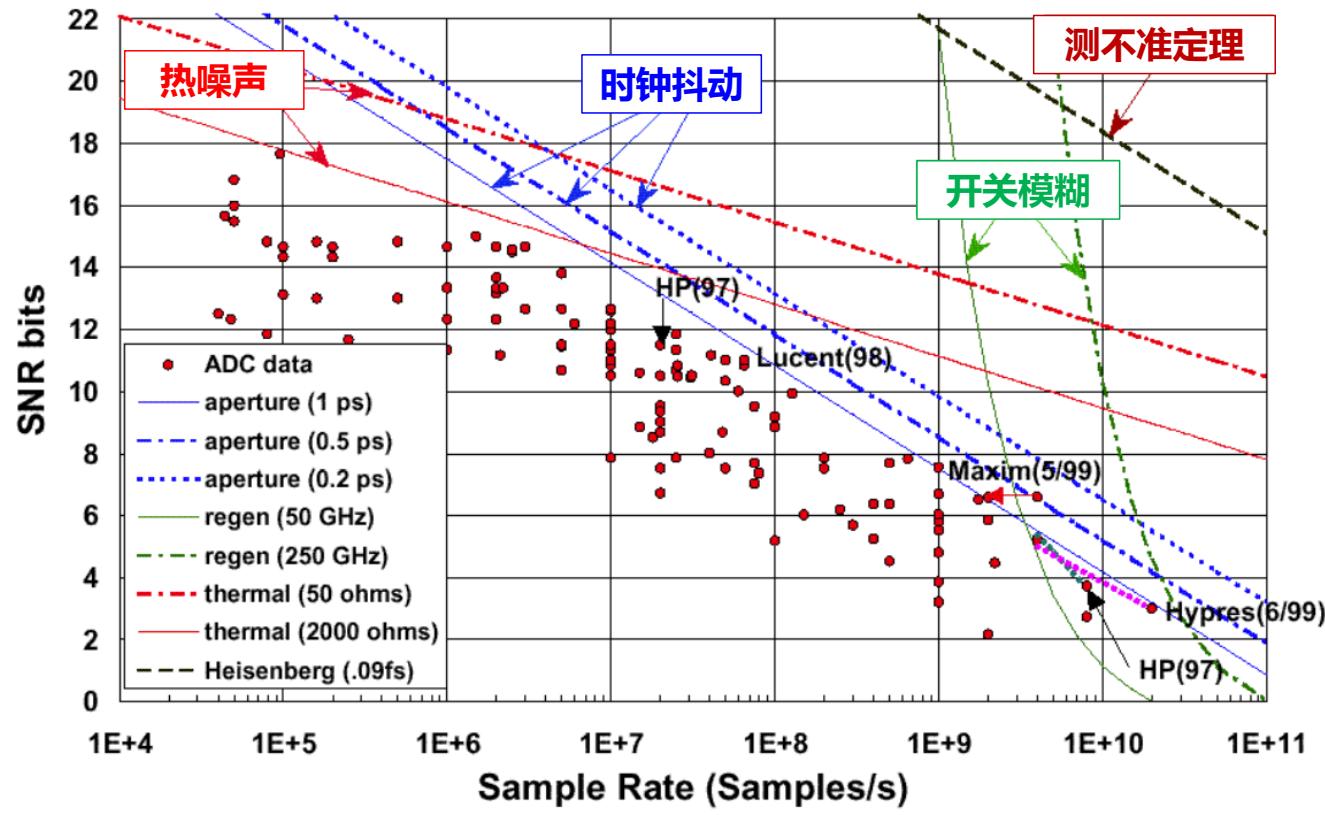
$$\sigma_{VT} = \frac{A_{VT}}{\sqrt{WL}}$$

精度² ~ WL

设计：增加W，增加I_{DS}和功耗
减小L，加快速度

速度 x 精度
功耗 = 工艺水平

ADC的限制



目前的设计均离理论极限还有空间!



作业

- 设计一个5BIT的SAR ADC，通过电容的方式实现采样与DA反馈。
 - 输入区间0-1.8V
 - 采样频率大于1MSPS
 - 可以采用理想比较器
 - 数字逻辑部分用verilog实现

第二部分

作业反馈

第 12 章 HW01-02

形式问题

1. 需要展示及介绍测试平台。
2. 对于自己假设的参数，如 V_{TH} ，需要提前说明。
3. 没有给出推算过程或逻辑，直接给出结果的一律无效。
4. 尽量使用工程单位um, nm, fF等，而不是数学单位e-6
5. 请将作业整理到一个PDF，题号回答清晰，建议全电子版书写；手写作业请确保字迹清晰，字迹模糊无法辨认的直接判错。
6. 作业迟交最高按60%分值计算，请确保按时提交作业。

Homework 1

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- $V_{GS}=0.8V$, 强反转区的 gm 推导:

$$\left\{ \begin{array}{l} L_{min} = 0.35 \mu m \\ KP_n \approx 300 \mu A/V^2 \end{array} \right. \quad \rightarrow \quad KP_n \approx 600 \mu A/V^2$$

$$I_D = \frac{1}{2} KP_n \frac{W}{L} (V_{GS} - VTH)^2$$

$$I_D = 200 \mu A, \Big|_{V_{TH}=0.46V} \quad g_m = 1.2 mA/V, \Big|_{V_{TH}=0.46V}$$

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- **$V_{GS}=0.8V$** , 强反转区的 r_0 推导:

$$r_0 \approx \frac{1}{\lambda I_{DS}} = \frac{V_E \cdot L}{I_{DS}}$$

$$V_{En} = 4 \text{ V}/\mu\text{mL}$$

$$r_0 \approx \frac{4 \cdot 0.18}{200u} = 3.6K\Omega$$

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- **$V_{GS}=0.8V$** , 强反转区的 gm 和 r_0 检验:

	估算	仿真
I_d	200u	100u
g_m	1.2m	0.42m
r_0	3.6K	100K

×估算与仿真有较大差距

```
region = Saturati
id = 100.3509u
ibs = -1.6822e-20
ibd = -43.4021n
vgs = 800.0000m
vds = 1.8000
vbs = 0.0000
vth = 456.4051m
vdsat = 232.2942m
vod = 343.5949m
gm = 423.2997u
gds = 11.2628u
gmb = 98.3501u
cdtot = 988.0917a
cg tot = 1.9084f
cstot = 2.4746f
cbtot = 2.1628f
cgs = 1.3013f
cg d = 341.0737a
```

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- 估算参数矫正

```
* GENERAL PARAMETERS
*
+CACM    = 1
+LMIN    = 1.5E-7          LMAX    = 1.0E-5
+WMAX    = 1.0E-4          TNOM    = 25.0
+TOX     = '3.87E-09+DTOX_N18' TOXM    = 3.87E-09
+NCH    = 3.8094000E+17    LLN     = 1.1205959
+WLN    = 1.0599999         WWN     = 0.8768474
+LL     = 2.6352781E-16    LW      = -2.2625584E-16
+WINT   = -1.4450482E-09   WL      = -2.3664573E-16
+WWL    = -4.0000000E-21   MOBMOD  = 1
+XL     = '1.8E-8+DXL_N18' XW      = '0.00+DXW_N18'

* MOBILITY PARAMETERS
*
+VSAT   = 8.2500000E+04    PVSAT   = -8.3000000E-10
+LUA    = 7.7349790E-19    PUA     = -1.0000000E-24
+UC     = 1.2000000E-10    PUC     = 1.5000000E-24
+PRWB   = 0.2400000        PRWC    = 0.4000000
+U0     = '(3.4000000E-02)*(1+0.05*Sigma)'    LU0
+A0     = 0.8300000         KETA    = -3.0000000E-03
+A1     = 0.00               A2      = 0.9900000
+B0     = 6.0000000E-08    B1      = 0.00
*
```

✓ 棚极厚度预估正确

$$\mu_p \approx 250 \text{ cm}^2/\text{Vs}$$

$$\mu_n \approx 600 \text{ cm}^2/\text{Vs}$$

✗ 载流子流速高估近一倍

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- 参数矫正

	调整后估算	仿真
I_d	113u	100u
g_m	0.68m	0.42m
r_0	6.4K	89K

```
* ROUT PARAMETERS
*
+PCLM      = 1.2000000          PPCLM     = 2.9999999E-15
+PDIBLC2   = 3.8000000E-03      PPDIBLC2 = 2.7000001E-16
+DROUT     = 0.5600000          PSCBE1    = 3.4500000E+08
+PVAG      = 0.00               DELTA     = 1.0000000E-02
+ALPHA1    = 0.1764000          LALPHA1  = 7.6250000E-09
*
```

$$V_{En} = 4 \text{ V}/\mu\text{mL}$$

- V_{En} 在此工艺中调整为 $40V/\mu m$

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- $V_{GS}=0.5V$, 弱反转区的 gm 推导:

$$I_{D,wi} = I_{D0} \frac{W}{L} e^{\frac{V_{GS}}{nkT/q}}$$

$$g_{m,wi} = \frac{I_{D,wi}}{nkT/q}$$

- ×n作为一个跟反转程度有关的量, 随 V_{GS} 变化, 无法预估
- × I_{D0} 未知

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- **$V_{GS}=0.5V$** , 弱反转区的 gm 推导: (利用已有强反型区结果)

$$I_{DS} = K' \frac{W}{L} V_{GSTt}^2 \cdot \ln^2(1 + e^v), \quad v = \frac{V_{GST}}{V_{GSTt}} \quad V_{GSTt} = 2n \frac{kT}{q} \approx 70mV$$

已有 $I_D = 113\mu A, \Big|_{V_{GST}=0.34V}$ \rightarrow $\ln^2(1 + e^v) \approx 5^2 = 25$

 ↓ $v = 0.7, \Big|_{V_{GST}=0.04V}$

$I_D = 5.5\mu A, \Big|_{V_{GST}=0.04V}$ \leftarrow $\ln^2(1 + e^v) \approx 1.1^2 = 1.2$

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

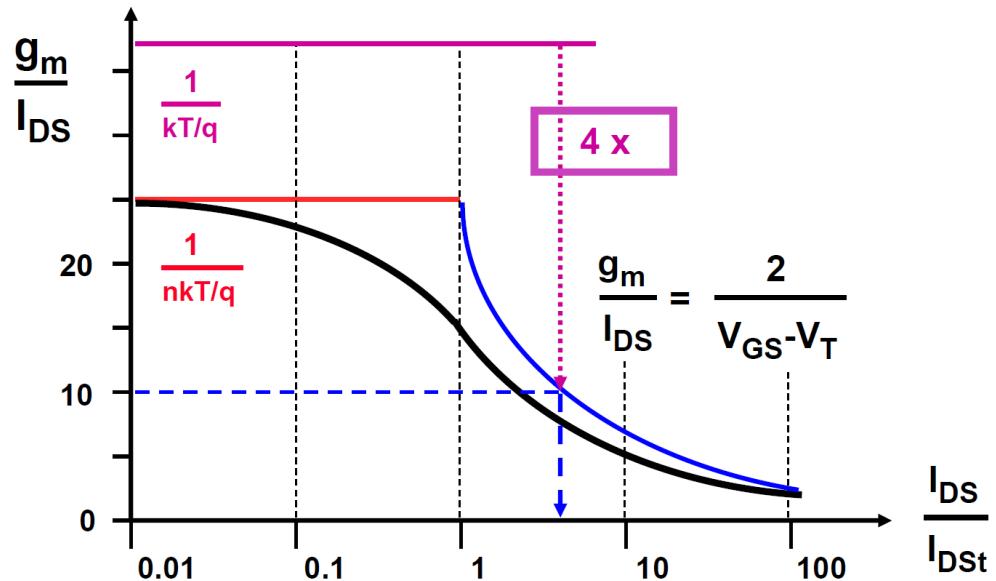
- **$V_{GS}=0.5V$** , 弱反转区的 gm 推导:

$$I_D = 5.5 \mu A, \Big|_{V_{GST}=0.04V}$$

$$\ln^2(1 + e^v) \approx 1.2$$

反型系数*i*: $i = \frac{I_{DS}}{I_{DSt}} = \ln^2(1 + e^v)$

$$g_m = 82.5 \mu V, \Big|_{V_{TH}=0.46V}$$



2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- **$V_{GS}=0.5V$** , 弱反转区的 r_0 推导:

$$r_0 \approx \frac{1}{\lambda I_{DS}} = \frac{V_E \cdot L}{I_{DS}}$$

$V_{en}=40V/\mu m$

$$r_0 \approx \frac{40 \cdot 0.18}{5.5u} = 1.3M\Omega$$

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- $V_{GS}=0.5V$, 弱反转区的 gm 和 r_0 检验:

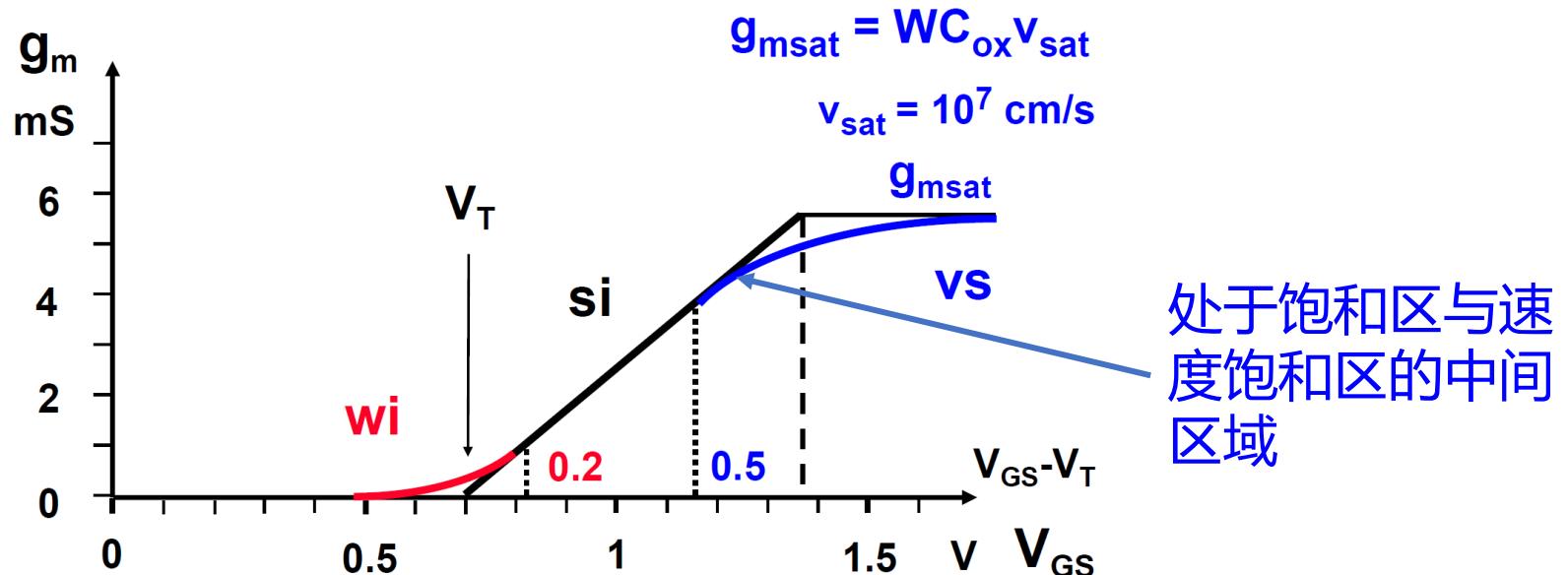
	估算	仿真
Id	5.5u	2u
gm	82.5u	28u
r0	1.3M	11M

✓估算基本正确

```
[ NMO ]
region = Saturati
id = 2.0072u
ibs = -3.3839e-22
ibd = -902.0821p
vgs = 500.0000m
vds = 1.8000
vbs = 0.0000
vth = 404.6511m
vdsat = 116.1837m
vod = 95.3489m
gm = 28.8373u
gds = 85.4506n
gmb = 8.4268u
cdtot = 976.6265a
cg tot = 6.8587f
cstot = 7.1026f
cbtot = 4.5589f
cgs = 4.9752f
cg d = 343.2256a
```

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- $V_{GS}=1.1V$, 速度饱和区的 gm 推导:



2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- **$V_{GS}=1.1V$** , 速度饱和区的 gm 推导:

$$\frac{1}{g_m} = \frac{1}{g_{m,si}} + \frac{1}{g_{m,sat}}$$



$$g_{m,si} = 2KP_n \frac{W}{L} V_{GST} = 2.67m$$



$$g_{m,sat} = WC_{OX}v_{sat} = 1m$$



$$g_m = 0.73m$$

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- $V_{GS}=1.1V$, 速度饱和区的 r_0 推导:

$$\frac{g_{m,si}}{I_D} = \frac{2}{V_{GST}}$$

$$\frac{g_{m,sat}}{I_D} = \frac{1}{V_{GST}}$$

$$I_D \approx \frac{1}{1.8} \cdot g_m \cdot V_{GST} = 260\mu A$$

$$r_0 \approx \frac{1}{\lambda I_{DS}} = \frac{V_E \cdot L}{I_{DS}}$$

$$V_{en}=40V/\mu m$$

$$r_0 \approx \frac{40 \cdot 0.18}{0.26m} = 28K\Omega$$

2. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的 g_m 和 r_0 。

- **$V_{GS}=1.1V$** , 速度饱和区的 gm 和 r_0 检验:

	估算	仿真
I_d	260u	240u
g_m	730u	500u
r_0	28K	62.5K

```
[ NMO ]
region = Saturati
id = 240.4028u
ibs = -3.9974e-20
ibd = -56.8244n
vgs = 1.1000
vds = 1.8000
vbs = 0.0000
vth = 456.5229m
vdsat = 341.4154m
vod = 643.4771m
gm = 496.4637u
gds = 16.0068u
gmb = 116.4091u
cdtot = 988.2450a
cgton = 1.9310f
cstot = 2.4969f
cbtot = 2.1538f
cgs = 1.3361f
cgd = 340.8963a
    240.4028u
```

✓估算基本正确

3. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的特征频率 f_T , 并通过AC仿真得到所求的特征频率。

$$f_T = \frac{g_m}{2\pi C_{GS}}$$

$$C_{GS} \approx \frac{2}{3} WL C_{ox} \quad \approx 2W \text{ fF}/\mu m \text{ for Lmin}$$

$$L_{min} C_{ox} \approx L_{min} \frac{\epsilon_{ox}}{t_{ox}} \approx 50 \epsilon_{ox} \approx 2 \text{ fF}/\mu m$$

$$f_T = \frac{g_m}{4\pi \cdot 1u \cdot fF/\mu m}$$

3. 估算 $V_{GS}=0.5V$, $0.8V$ 和 $1.1V$ 且 $V_{DS}=1.8V$ 时, $W/L=1\mu m/0.18\mu m$ 的NMOS的特征频率 f_T , 并通过AC仿真得到所求的特征频率。

$$f_T = \frac{g_m}{4\pi \cdot 1u \cdot fF/\mu m}$$

V_{GS}	仿真 gm	算术 fT	仿真 fT
0.5V	28u	1.1G	12G
0.8V	420u	16.7G	36G
1.1V	500u	19.9G	41G

- 真实的 $C_{gs}=1.3fF$, 比我们预估的 $2fF$ 略小
- 弱反型区中的 C_{gs} 不能用 C_{ox} 类推

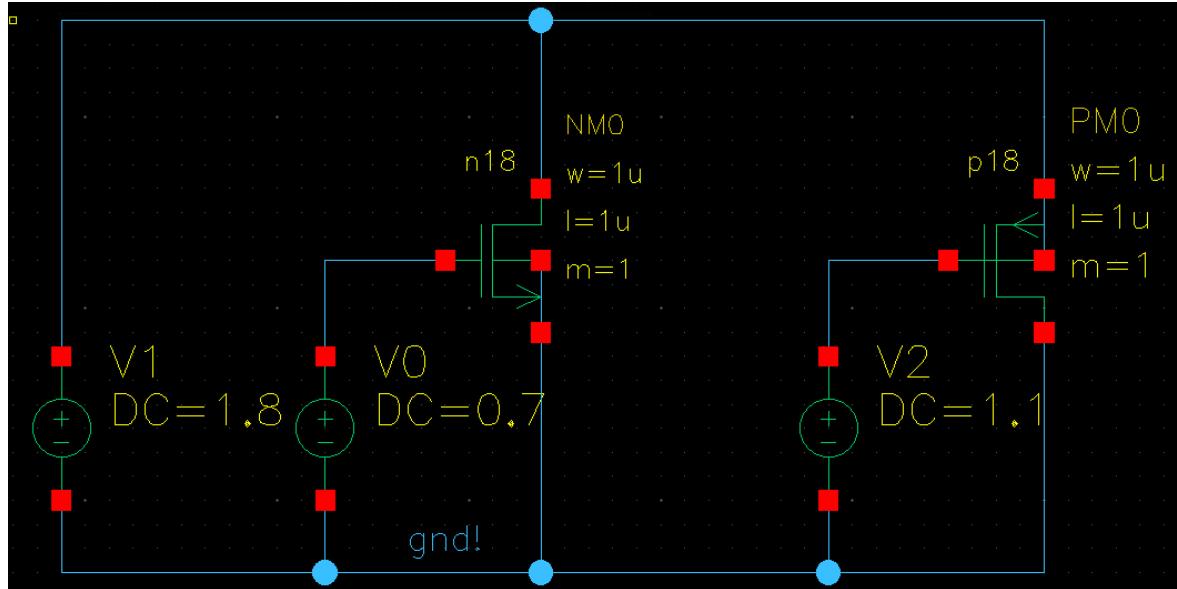
Homework 2

- 利用仿真结果，找到我们所使用工艺的 $u_{0p,n}$, C_{ox} , V_{THn} , V_{THp}

```

region = Saturati
id = 12.9769u
ibs = -2.1864e-21
ibd = -2.8580n
vgs = 700.0000m
vds = 1.8000
vbs = 0.0000
vth = 404.6616m
vdsat = 261.9176m
vod = 295.3384m
gm = 78.3552u
gds = 298.4982n
gmb = 22.6287u
cdtot = 976.9014a
cgtot = 7.3556f
cstot = 7.8072f
cbtot = 4.5240f
cgs = 5.6599f

```



```

region = Saturati
id = -2.4713u
ibs = 1.7020e-22
ibd = 11.4903p
vgs = -700.0000m
vds = -1.8000
vbs = 0.0000
vth = -422.6200m
vdsat = -250.9069m
vod = -277.3800m
gm = 16.0855u
gds = 61.2616n
gmb = 5.1132u
cdtot = 1.1470f
cgtot = 7.1159f
cstot = 8.3443f
cbtot = 4.1553f
cgs = 6.0843f

```

$$C_{oxn} = 8.55m \quad \leftarrow \quad C_{GS} \approx \frac{2}{3} W L C_{ox} \quad \rightarrow \quad C_{oxp} = 9.12m$$

$$u_{0n} = \frac{26u}{8.55m \cdot 0.09} = 33m \quad \leftarrow \quad I_D = \frac{1}{2} u_0 C_{GS} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad \rightarrow \quad u_{0p} = \frac{4.94u}{9.12m \cdot 0.073} = 7.4m$$

- 利用仿真结果，找到我们所使用工艺的 $u_{0p,n}$, C_{ox} , V_{THn} , V_{THp}

NMOS

```
* GENERAL PARAMETERS
*
+CALCACM = 1
+LMIN = 1.5E-7
+WMAX = 1.0E-4
+TOX = '3.87E-09+DTOX_N18'
+NCH = 3.8694000E+17
```

$$KP_n \approx 280 \mu A/V^2$$

```
* MOBILITY PARAMETERS
*
+VSAT = 8.2500000E+04      PVSAT = -8.1
+LUA = 7.7349790E-19       PUA = -1.1
+UC = 1.2000000E-10        PUC = 1.5
+PRWB = -0.2400000          PRWG = 0.4
+U0 = '(3.4000000E-02)*(1+0.05*Sigma)'
+A0 = 0.8300000            KETA = -3.
```

$$C_{oxn} = 8.55m$$

$$C_{GS} \approx \frac{2}{3} W L C_{ox}$$

$$C_{oxp} = 9.12m$$

$$u_{0n} = \frac{26u}{8.55m \cdot 0.09} = 33m$$

$$I_D = \frac{1}{2} u_0 C_{GS} \frac{W}{L} (V_{GS} - V_{TH})^2$$

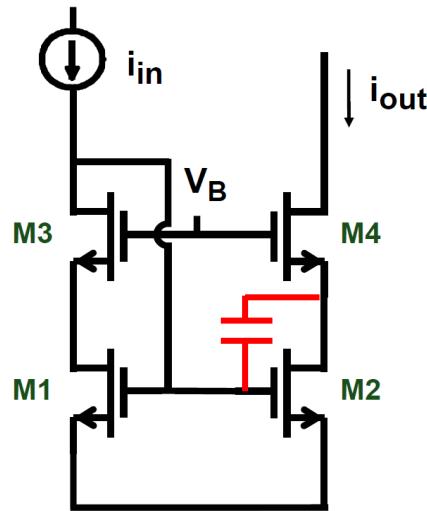
$$u_{0p} = \frac{4.94u}{9.12m \cdot 0.073} = 7.4 m$$

```
* GENERAL PARAMETERS
*
+CALCACM = 1
+LMIN = 1.5E-7
+WMAX = 1.0E-4
+TOX = '3.74E-09+DTOX_P18'
+NCH = 5.5000000E+17
```

$$KP_p \approx 70 \mu A/V^2$$

```
* MOBILITY PARAMETERS
*
+VSAT = 1.0000000E+05      UA = 2
+PUA = -2.0000000E-24      UB = 1
+WUC = 3.1668000E-17       PUC = -
+PRWB = -0.4000000          PRWG = 6
+U0 = '(8.6610000E-03)*(1+0.05*Sigma)'
+A0 = 1.0000000            KETA = 2
```

- 通过公式描述 V_B 的取值范围 (提示: 晶体管M1-M4均需要工作在饱和区)



$$\left\{ \begin{array}{l} V_{DS1} > V_{GS1} - V_{TH1} \\ V_{DS3} > V_{GS3} - V_{TH3} \end{array} \right.$$

$$V_{GS3} + V_{GS1} - V_{TH1} < V_B < V_{GS1} + V_{TH3}$$

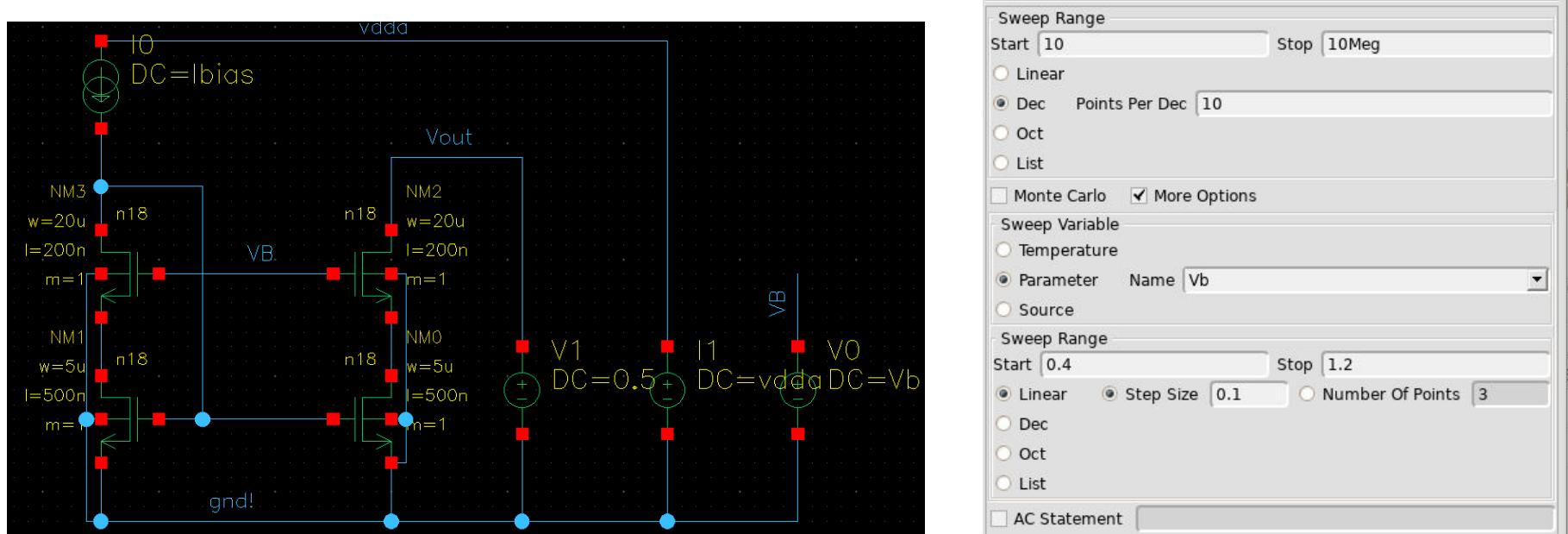
$$V_{GS3} - V_{TH1} < V_B - V_{GS1} < V_{TH3}$$

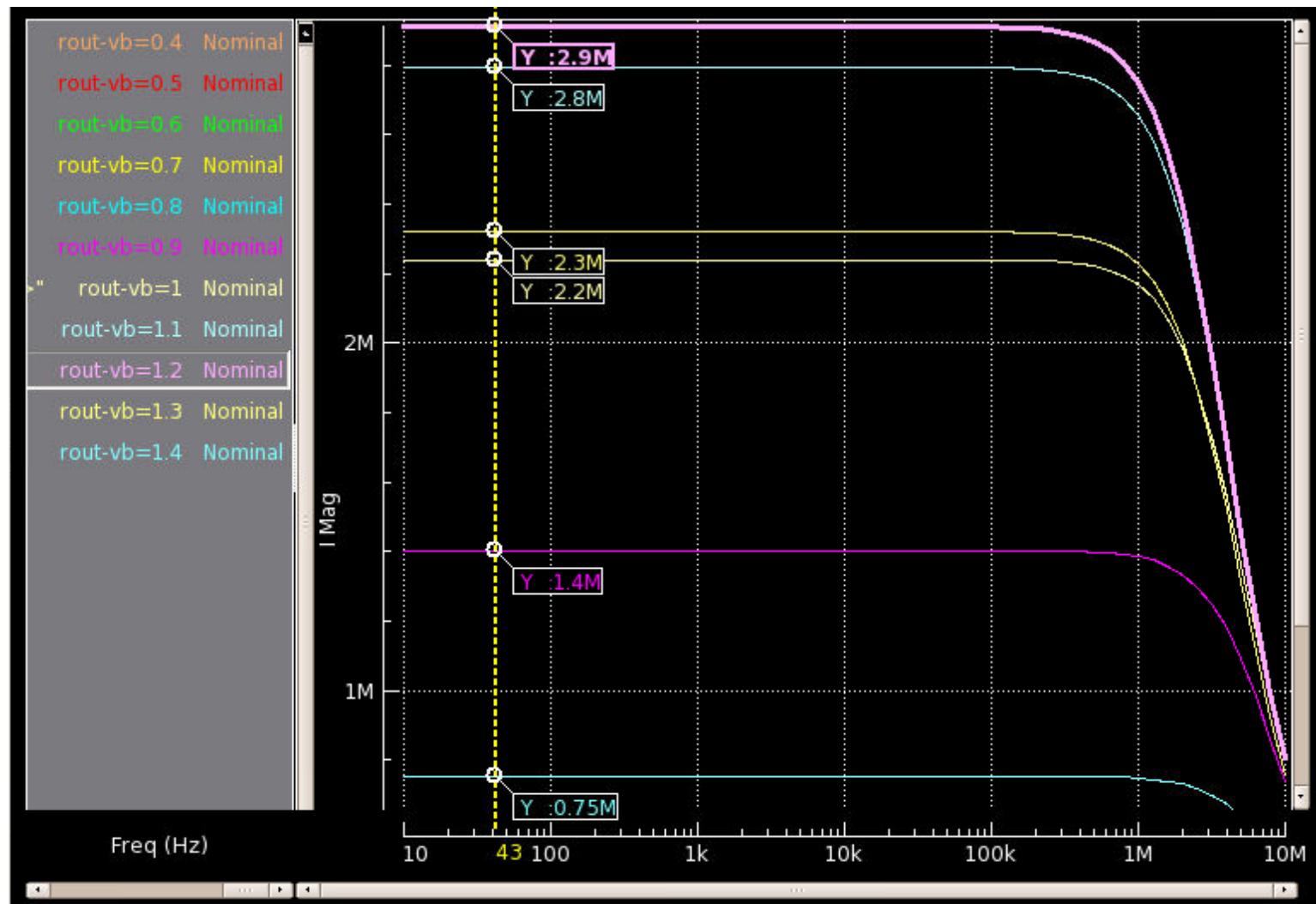
减小 V_{GS3} 以增加 V_B 的取值范围

改变 V_{GS1} 以改变 V_B 的电势偏移

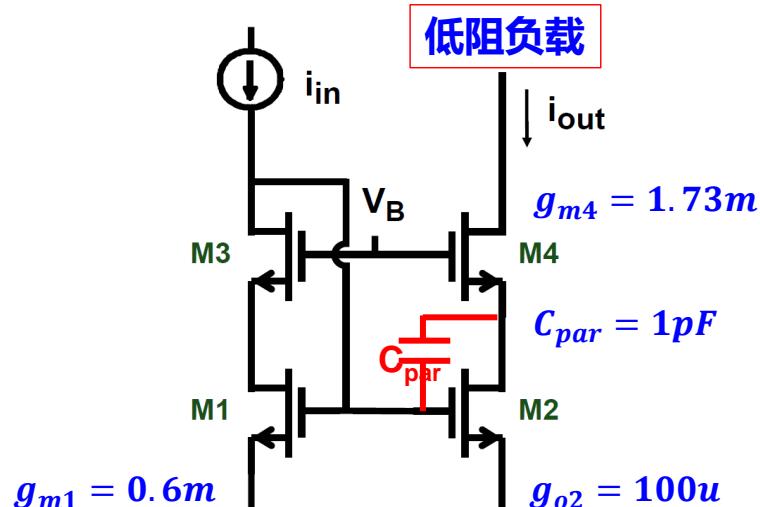
令 $V_{GS3} = 0.4V, V_{GS1} = 0.6V$ 得 $0.6 < V_B < 1$

- 通过公式描述 V_B 的取值范围 (提示: 晶体管M1-M4均需要工作在饱和区)

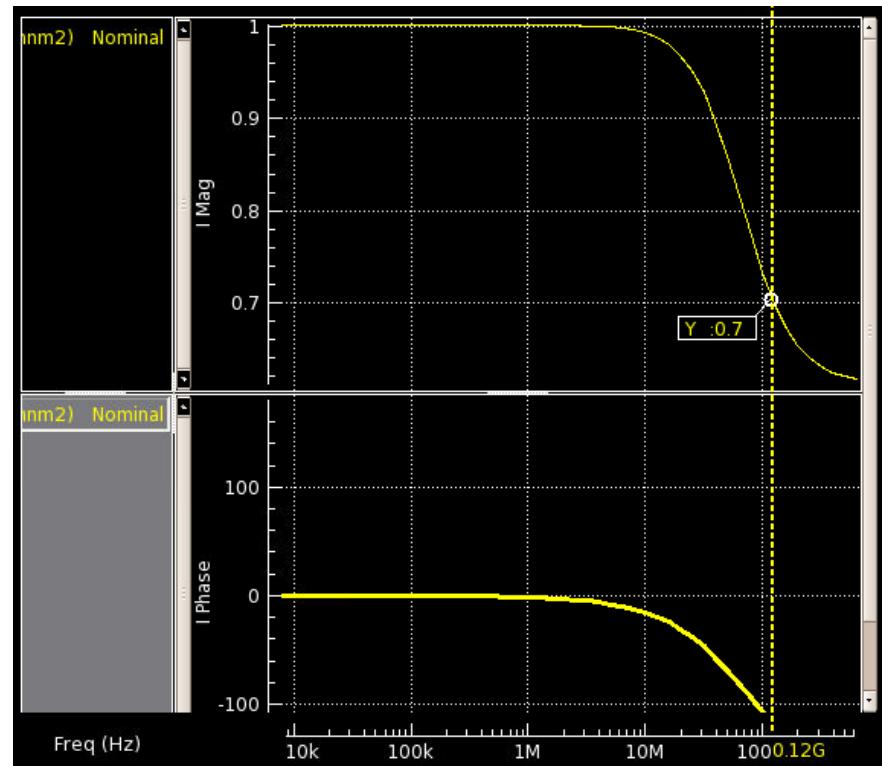




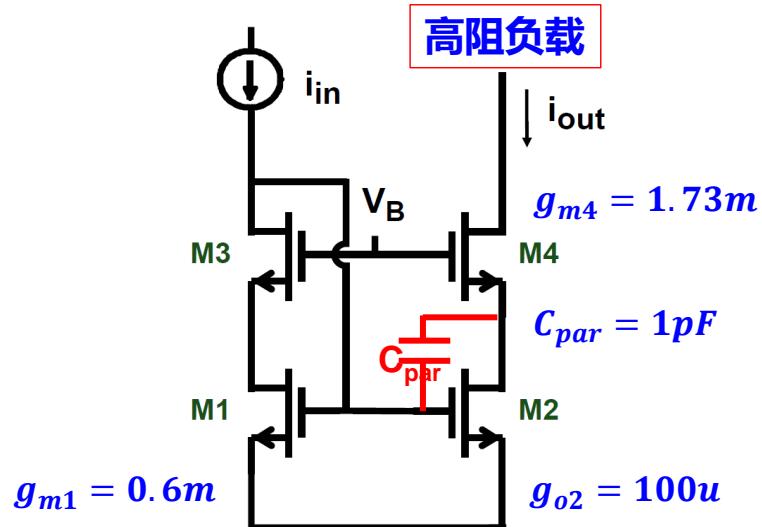
- 在Cascode电流镜中，假设有寄生电容 C_{par} ，利用公式估算并用仿真验证该电流镜的频率特性。（可以自由设置偏置、晶体管的尺寸以及寄生电容）



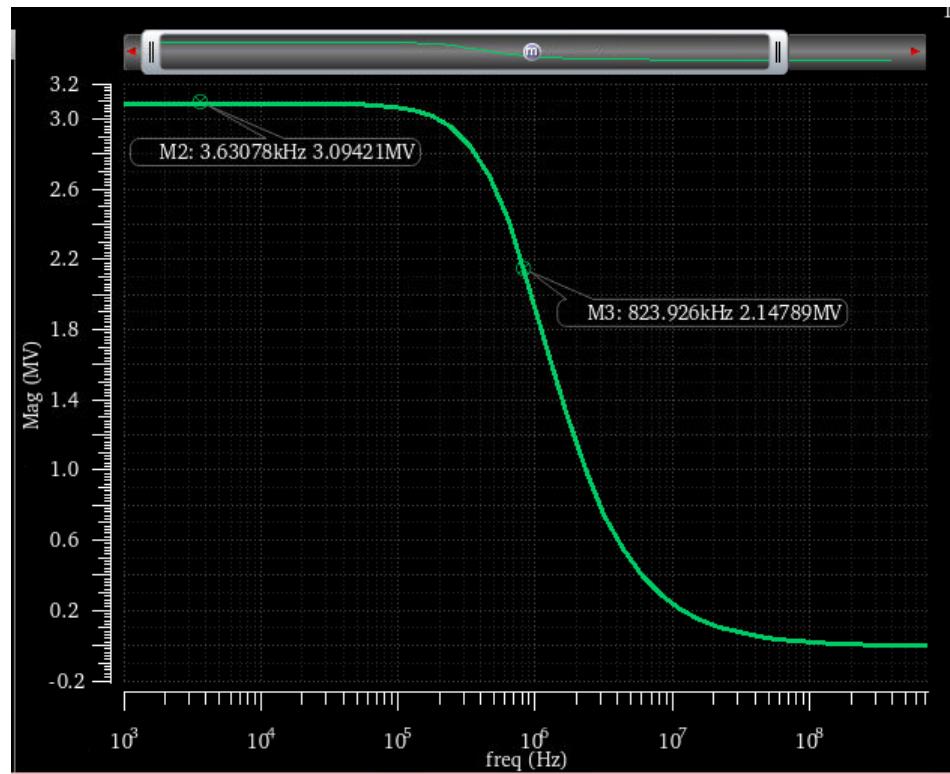
$$f_c = \frac{g_{m4}}{2\pi \cdot (1 + B) \cdot C_{par}} = 0.14GHz$$



- 在Cascode电流镜中，假设有寄生电容 C_{par} ，利用公式估算并用仿真验证该电流镜的频率特性。（可以自由设置偏置、晶体管的尺寸以及寄生电容）



$$f_c = \frac{g_{o2}}{2\pi \cdot (1 + B) \cdot C_{par}} = 796\text{kHz}$$

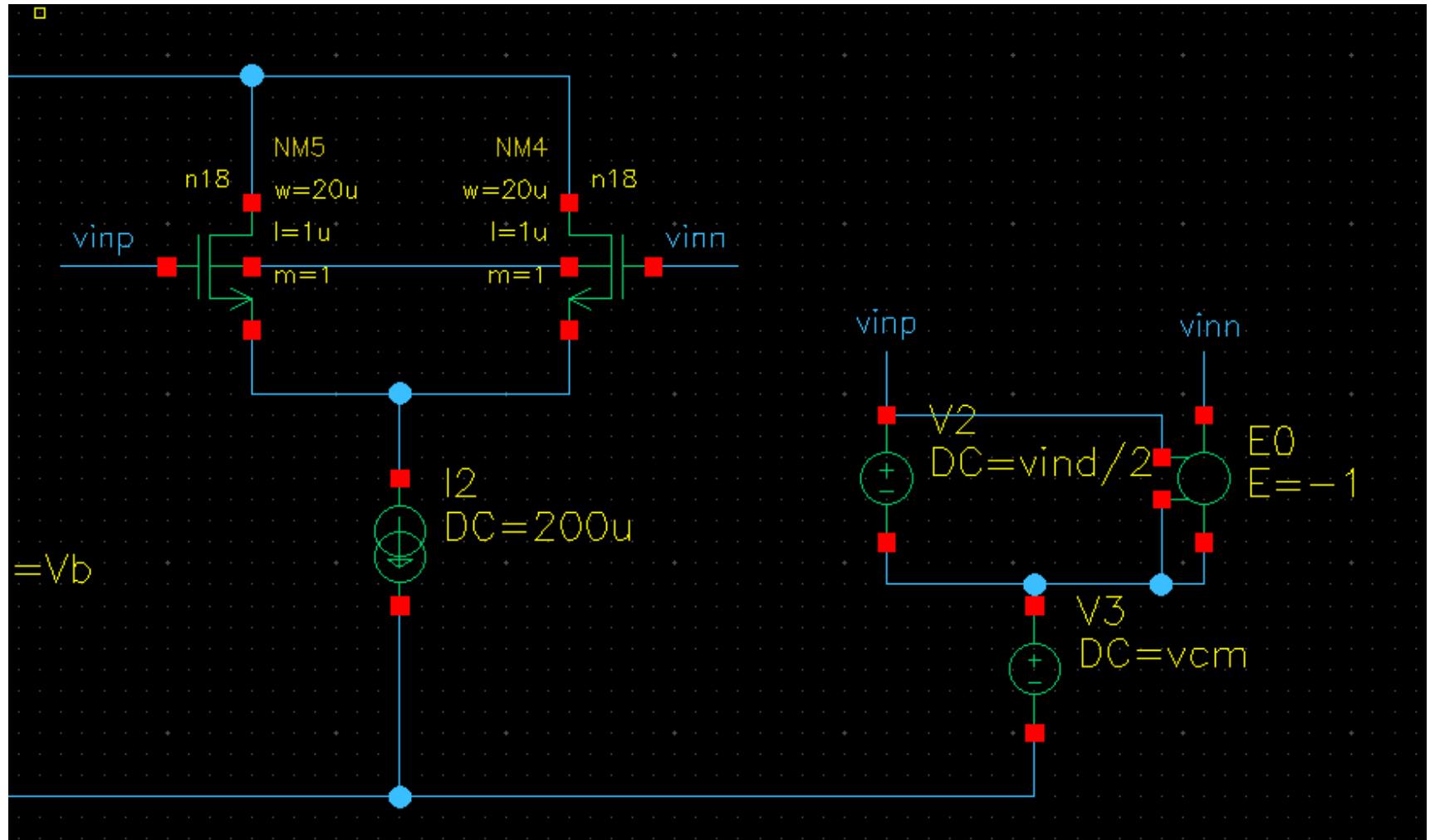


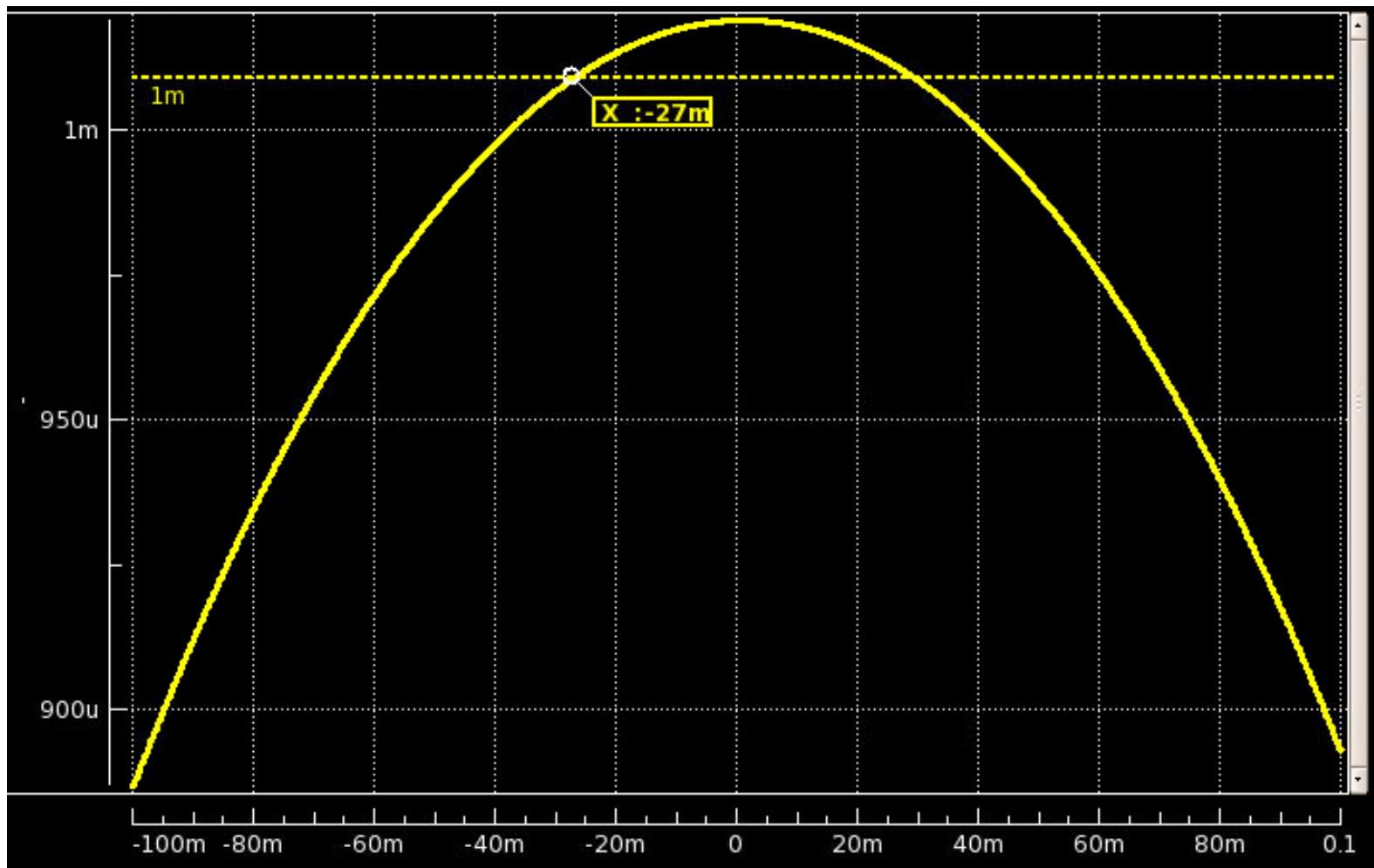
- 假设差分对偏置电流为200uA, W/L=20um/1um, 根据理论分析和仿真验证。
 - 计算 $g_m > 99\% * g_{m,\max}$ 的区间。
 - 计算差分输出电流为198uA时的差分输入电压。
 - 如果需要把问题2中求得的电压扩大一倍, 差分对的W需要如何修改?

$$\frac{i_{Od}}{I_B} = \frac{v_{Id}}{(V_{GS}-V_T)} \sqrt{1 - \frac{1}{4} \left(\frac{v_{Id}}{V_{GS}-V_T} \right)^2}$$

$$\sqrt{1 - \frac{1}{4} \left(\frac{V_{ID}}{V_{GST}} \right)^2} = 99\%$$

$$V_{ID} = 0.28 \cdot V_{GST} \quad \rightarrow \quad V_{ID} = 53m$$



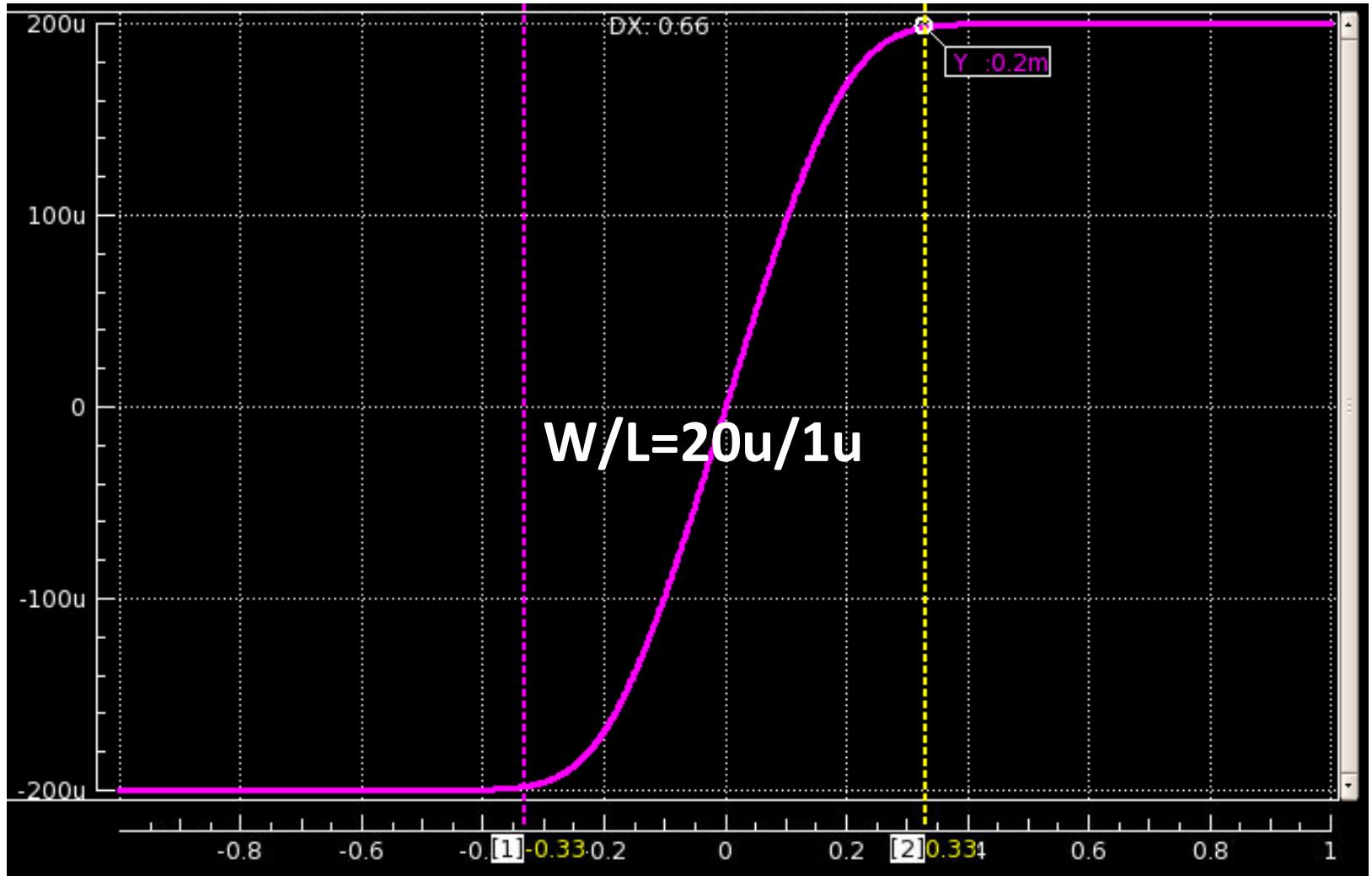


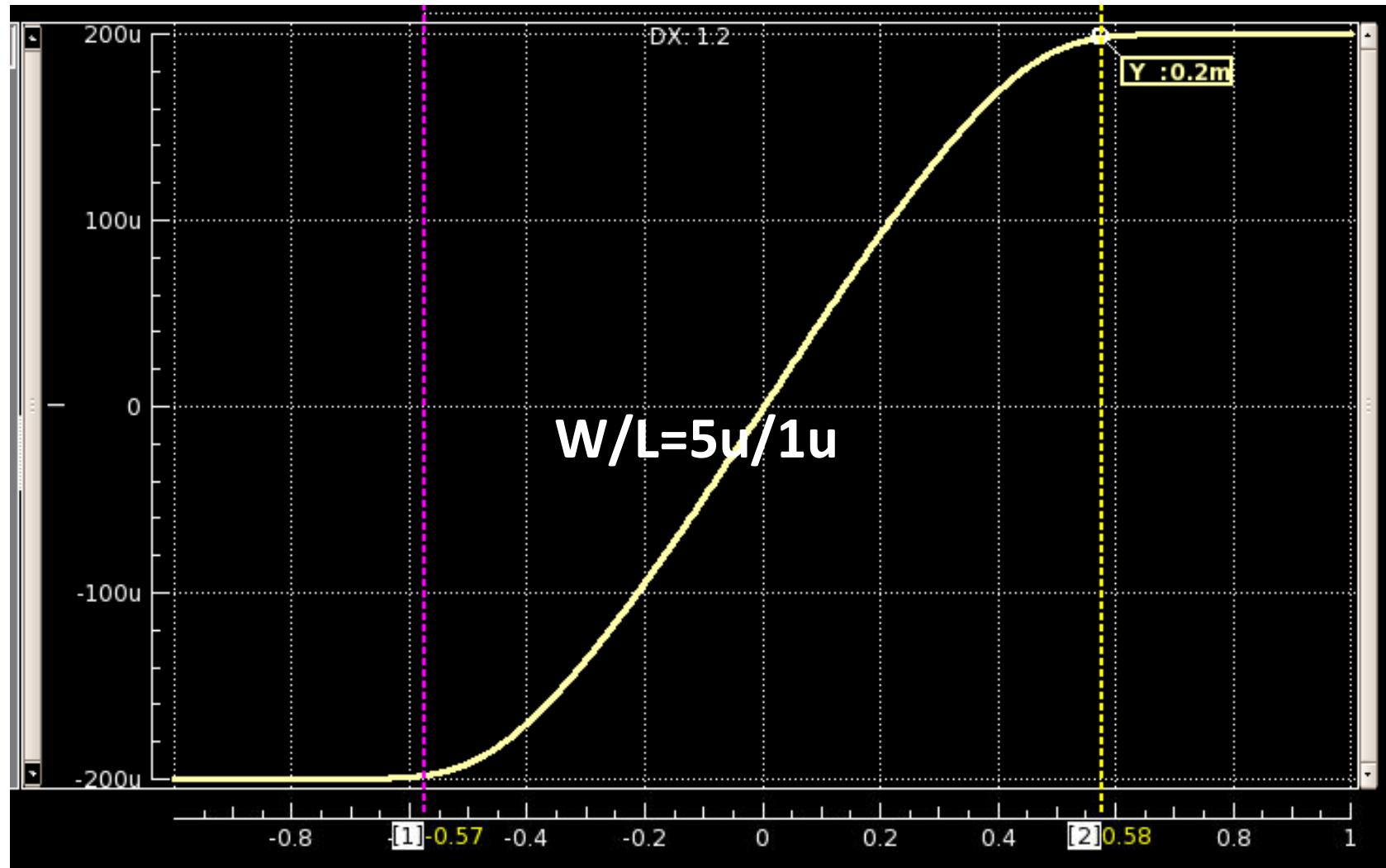
- 假设差分对偏置电流为200uA, W/L=20um/1um, 根据理论分析和仿真验证。
 - 计算 $g_m > 99\% * g_{m,\max}$ 的区间。
 - 计算差分输出电流为198uA时的差分输入电压。
 - 如果需要把问题2中求得的电压扩大一倍, 差分对的W需要如何修改?

$$\frac{i_{Od}}{I_B} = \frac{V_{Id}}{(V_{GS}-V_T)} \sqrt{1 - \frac{1}{4} \left(\frac{V_{Id}}{V_{GS}-V_T} \right)^2}$$

$$V_{ID} = \sqrt{2} \cdot V_{GST} \quad \rightarrow \quad V_{ID} = 380m$$

V_{GST} 扩大一倍 \Rightarrow 晶体管宽长减小到原来的1/4

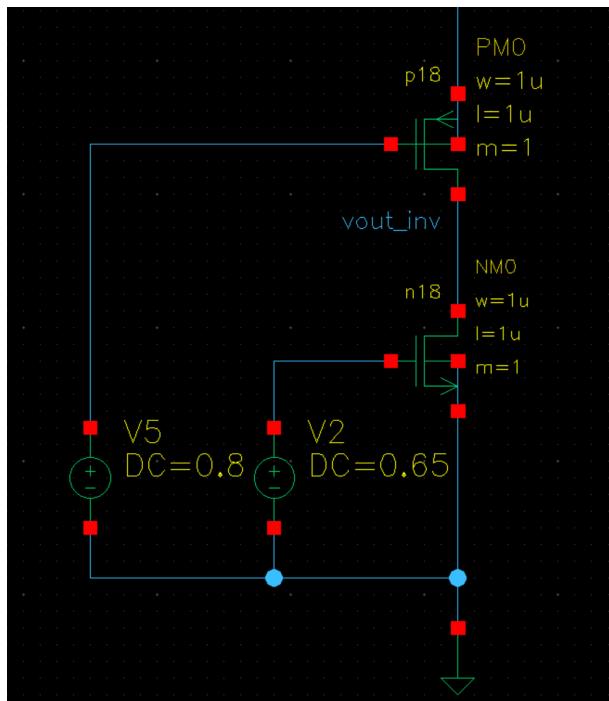




第 13 章 HW03

Homework 3

- 自由确定晶体管的尺寸，通过仿真寻找NMOS和PMOS的 $1/f$ 噪声系数KF，以及热噪声系数 γ



```
#####
noise analysis result at frequency 1.0000 #####
hierarchy
device          0:mpm0
rd              1.0068e-20
rs              228.7918a
id              1.1199p
rx              1.7474x
fn              1.1552u
total           1.1552u

hierarchy
device          0:mnn0
rd              1.5904e-20
rs              1.1918f
id              2.1533p
rx              1.7325x
fn              713.4537n
total           713.4559n

#### output noise voltage = 1.8687u volt^2/Hz
#### output rms noise   = 1.3670m volt/Hz^(1/2)
#### equivalent input noise at vv2 = 11.6463u /Hz^(1/2)
#### transfer function v(vout_inv)/vv2 = 117.3763

#### integral value of noise from 1.0000Hz to 1.0000Hz
#### total output noise voltage = 0.0000 volt
#### total input noise at vv2 = 0.0000 volt
```

- 如何确定噪声的单位？

- 自由确定晶体管的尺寸，通过仿真寻找NMOS和PMOS的1/f噪声的系数KF，以及热噪声系数 γ

• 如何确定噪声的单位？

- 利用噪声的随机特性
- 对于不相关的噪声，总噪声为每个噪声功率之和
- fn的单位应该是V²/hz

```
#####
noise analysis result at frequency 1.0000 #####
hierarchy
device      0:mpm0
rd          1.0068e-20
rs          228.7918a
id          1.1199p
rx          1.7474x
fn          1.1552u
total       1.1552u

hierarchy
device      0:mnm0
rd          1.5904e-20
rs          1.1918f
id          2.1533p
rx          1.7325x
fn          713.4537n
total       713.4559n

#### output noise voltage           = 1.8687u volt^2/Hz
#### output rms noise             = 1.3670m Volt/Hz^(1/2)
#### equivalent input noise at vv2 = 11.6463u /Hz^(1/2)
#### transfer function v(vout_inv)/vv2 = 117.3763

#### integral value of noise from 1.0000Hz to 1.0000Hz
#### total output noise voltage     = 0.0000 volt
#### total input noise at vv2       = 0.0000 volt
```

- 自由确定晶体管的尺寸，通过仿真寻找NMOS和PMOS的1/f噪声的系数KF，以及热噪声系数γ

• 如何确定噪声的单位？

- 利用闪烁噪声的频率特性

$$\overline{dv_{ieqf}^2} = \frac{KF_F}{WL C_{ox}^2} \frac{df}{f}$$

- fn的单位应该是V²/hz

```
#####
noise analysis result at frequency 1.0000 #####
hierarchy
device      0:mpm0
rd          1.0068e-20
rs          228.7918a
id          1.1199p
rx          1.7474x
fn          1.1552u
total       1.1552u

#####
noise analysis result at frequency 10.0000 #####
hierarchy
device      0:mnm0
rd          1.5904e-20
rs          1.1918f
id          2.1533p
rx          1.5499x
fn          108.4840n
total       108.4862n

hierarchy
device      0:mpm0
rd          1.0068e-20
rs          228.7918a
id          1.1199p
rx          1.4997x
fn          85.5010n
total       85.5021n

#### output noise voltage           = 193.9883n volt^2/Hz
#### output rms noise             = 440.4410u volt/Hz^(1/2)
#### equivalent input noise at vv2 = 3.7524u /Hz^(1/2)
#### transfer function v(vout_inv)/vv2 = 117.3763
```

- 自由确定晶体管的尺寸，通过仿真寻找NMOS和PMOS的1/f噪声系数KF，以及热噪声系数 γ

• 如何计算KF?

$$\overline{dv_{ieqf}^2} = \frac{KF_F}{WL C_{ox}^2} \frac{df}{f}$$

- 公式描述的是等效输入噪声
- 仿真给出的是输出噪声

$$\begin{aligned}
 KF_N &= \frac{fn}{A_0^2} \cdot WL C_{ox}^2 \cdot freq \\
 &= \frac{0.71u}{117^2} \cdot 1p \cdot 8.85^2u \cdot 1 \\
 &= 4.0 \times 10^{-27} C/m^2
 \end{aligned}$$

```

#####
noise analysis result at frequency 1.0000 #####
hierarchy
device          0:mpm0
rd               1.0068e-20
rs               228.7918a
id               1.1199p
rx               1.7474x
fn               1.1552u
total            1.1552u

hierarchy
device          0:mnm0
rd               1.5904e-20
rs               1.1918f
id               2.1533p
rx               1.7325x
fn               713.4537n
total            713.4559n

#### output noise voltage           = 1.8687u volt^2/hz
#### output rms noise              = 1.3670m volt/hz^(1/2)
#### equivalent input noise at vv2 = 11.6463u /hz^(1/2)
#### transfer function v(vout_inv)/vv2 = 117.3763

#### integral value of noise from 1.0000hz to 1.0000hz
#### total output noise voltage     = 0.0000 volt
#### total input noise at vv2       = 0.0000 volt

```

- 自由确定晶体管的尺寸，通过仿真寻找NMOS和PMOS的1/f噪声系数KF，以及热噪声系数 γ

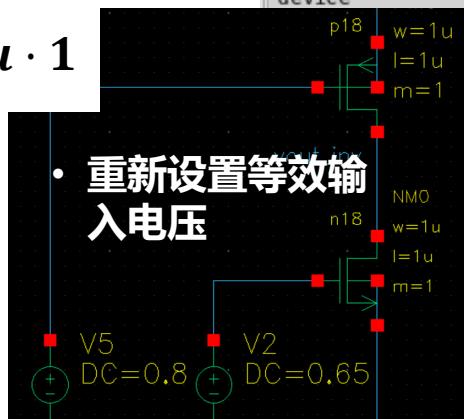
• 如何计算KF?

$$KF_P = \frac{fn}{A_0^2} \cdot WLC_{ox}^2 \cdot freq$$

$$= \frac{1.15u}{50^2} \cdot 1p \cdot 9.12^2u \cdot 1$$

$$= 3.8 \times 10^{-26} C/m^2$$

• 结果与课本偏差较大！



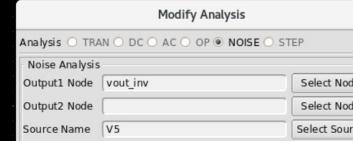
```
#### output noise voltage
#### output rms noise
#### equivalent input noise at vv5
#### transfer function v(vout_inv)/vv5
```

```
= 1.8687u volt^2/Hz
= 1.3670m volt/Hz^(1/2)
= 27.3104u /Hz^(1/2)
= 50.0542
```

```
#####
noise analysis result at frequency 1.0000 #####
hierarchy
device          0:mpm0
rd              1.0068e-20
rs              228.7918a
id              1.1199p
rx              1.7474x
fn              1.1552u
total           1.1552u
```

```
hierarchy
device
```

```
0:mnn0
```



• 根据gm和gds计算增益

```
IDS = 0.201e-22
ibd = 6.5092e-19
vgs = -1.0000
vds = -899.1993m
vbs = 0.0000
vth = -422.6265m
vdSAT = -481.9577m
vod = -57.3735m
gm = 28.2327u
gds = 251.0466n
gmb = 9.3614u
cdtot = 1.3095f
cgtot = 7.3278f
cstot = 8.5795f
cbtot = 4.2295f
cgs = 6.419815f
cgd = 416.9815a
i1 = -9.0953u
i2 = 0.0000
i3 = 9.0953u
i4 = 899.2000f
```

```
[NMO]
region = Saturated
id = 9.0953u
ibs = -1.5327e-21
ibd = -89.5292f
vgs = 650.0000m
vds = 900.8007m
vbs = 0.0000
vth = 404.6679m
vdSAT = 225.1058m
vod = 245.3321m
gm = 66.2151u
gds = 313.0362n
gmb = 19.1639u
cdtot = 1.1068f
cg tot = 7.3172f
cstot = 7.7587f
cbtot = 4.6647f
```

- 自由确定晶体管的尺寸，通过仿真寻找NMOS和PMOS的 $1/f$ 噪声系数 K_f ，以及热噪声系数 γ

Freq (Hz)	1	10	100	1k	10k	100k	1M
NMOS (V^2/Hz)	0.71u	108n	16.5n	2.5n	381p	58p	8.81p
PMOS(V^2/Hz)	1.15u	85.5n	6.3n	0.47n	34.7p	2.56p	0.19p

• PMOS: Corner Freq = 200kHz

```
#####
noise analysis result at frequency 199.5262k #
hierarchy
device      0:mnm0
rd          1.5904e-20
rs          1.1917f
id          2.1533p
rx          57.4178k
fn          32.9574p
total        35.1119p

hierarchy
device      0:mpm0
rd          1.0068e-20
rs          228.7852a
id          1.1199p
rx          14.5679k
fn          1.1748p
total        2.2948p
```

• NMOS: Corner Freq = 5MHz

```
#####
noise analysis result at frequency 5.0119x #
hierarchy
device      0:mnm0
rd          1.5814e-20
rs          1.1705f
id          2.1148p
rx          20.4112k
fn          2.3170p
total        4.4330p

hierarchy
device      0:mpm0
rd          1.0155e-20
rs          224.7017a
id          1.0999p
rx          10.2238k
fn          30.1403f
total        1.1302p
```

- 自由确定晶体管的尺寸，通过仿真寻找NMOS和PMOS的1/f噪声系数KF，以及热噪声系数 γ

• 如何计算 γ ？

• 噪声id是什么？

Name (Alias)	Units	Default	Description
RX			<p>Transfers the function of thermal noise to the output.</p> <p>This is not noise, but is a transfer coefficient, which reflects the contribution of thermal noise to the output. For example:</p> $V(\text{output}) = I(\text{local}) * rx(\text{from local to output})$ <p>Where $V(\text{output})$ is the noise voltage at the output port, $I(\text{local})$ is the local noise current in the specific noise element.</p> <p>It is clear that rx should have a unit of impedance, therefore we call it transimpedance. By summarizing all the contributions (power) from each independent noisy element, we can get the total noise contribution(power) at the output port.</p>
ID	V ² /Hz		Output channel thermal noise: ID = RX ² P (channel thermal noise) ² .
FN	V ² /Hz		Output flicker noise: FN = RX ² P (flicker noise) ² .
IFEX			Noise due to floating body
LGS			Shot noise due to lgs
LGD			Shot noise due to lgd

```
#####
noise analysis result at frequency 1000.0000k #####
hierarchy
device      0:mmn0
rd          1.5901e-20
rs          1.1900f
id          2.1518p
rx          32.0974k
fn          8.8115p
total       10.9645p

hierarchy
device      0:mpm0
rd          1.0071e-20
rs          228.6261a
id          1.1191p
rx          11.0020k
fn          189.7389f
total       1.3090p

#####
output noise voltage           = 12.2735p volt^2/hz
#####
output rms noise              = 3.5034u volt/hz^(1/2)
#####
equivalent input noise at vv5 = 70.0167n /hz^(1/2)
#####
transfer function v(vout_inv)/vv5 = 50.0361

#####
integral value of noise from 100.0000khz to 1000.0000khz
#####
total output noise voltage    = 4.4767m volt
#####
total input noise at vv5      = 89.4462u volt
```

- 自由确定晶体管的尺寸，通过仿真寻找NMOS和PMOS的1/f噪声系数KF，以及热噪声系数 γ
- 如何计算 γ ？

$$\overline{dv_{ieqn}^2} = 4kT\gamma/g_m$$

- 公式描述的是等效输入噪声
- 仿真给出的是输出噪声

$$\gamma = \frac{id}{A_0^2} \cdot g_m$$

$$\gamma_p = \frac{1.12p/50^2 \cdot 28u}{1.656 \times 10^{-20}} = 0.76$$

$$\gamma_n = \frac{2.15p/117^2 \cdot 66u}{1.656 \times 10^{-20}} = 0.63$$

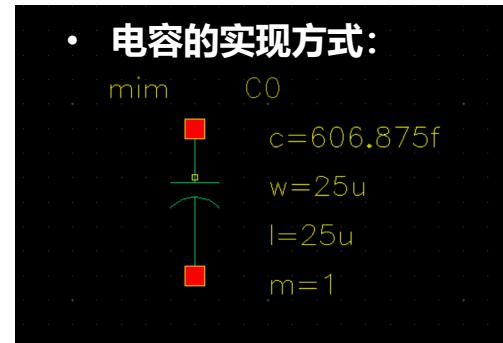
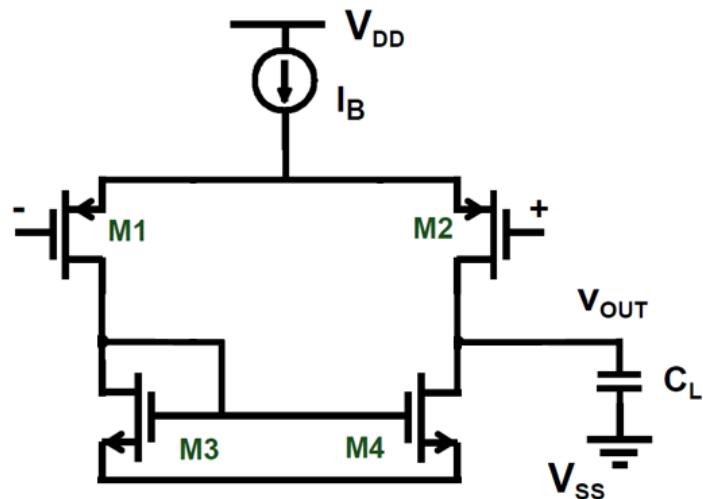
```
#####
noise analysis result at frequency 1000.0000k #####
hierarchy
device      0:mmm0
rd          1.5901e-20
rs          1.1900f
id          2.1518p
rx          32.0974k
fn          8.8115p
total        10.9645p

hierarchy
device      0:mpm0
rd          1.0071e-20
rs          228.6261a
id          1.1191p
rx          11.0020k
fn          189.7389f
total        1.3090p

#### output noise voltage           = 12.2735p volt^2/hz
#### output rms noise             = 3.5034u volt/hz^(1/2)
#### equivalent input noise at vv5 = 70.0167n /hz^(1/2)
#### transfer function v(vout_inv)/vv5 = 50.0361

#### integral value of noise from 100.0000khz to 1000.0000khz
#### total output noise voltage     = 4.4767m volt
```

- 对一偏置电流为100uA的五管OTA，通过晶体管的设计，使其等效输入噪声的80%来源于差分对M1和M2。
- 观察什么噪声？**
 - 总的噪声积分**
 - 可以先用带宽内高频的热噪声来计算**



$$\overline{dv_{ieqn,p}^2} = \frac{4kT}{g_{m,p}}, \quad \overline{dv_{ieqn,n}^2} = \frac{4kT}{g_{m,n}} \left(\frac{g_{m,n}}{g_{m,p}} \right)^2$$

1:4

$$g_{m,p} : g_{m,n} = 4 : 1$$

- 对一偏置电流为100uA的五管OTA，通过晶体管的设计，使其等效输入噪声的80%来源于差分对M1和M2。

$$g_m \approx \mu_0 C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) = \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_{DS}} = \frac{2I_{DS}}{V_{GS} - V_{TH}}$$

NMOS

```
* GENERAL PARAMETERS
*
+CALCACM = 1
+LMIN = 1.5E-7
+WMAX = 1.0E-4
+TOX = '3.87E-09+DTOX N18'
+NCH = 3.869400E+17
```

$$KP_n \approx 280 \mu A/V^2$$

PMOS

```
* GENERAL PARAMETERS
*
+CALCACM = 1
+LMIN = 1.5E-7
+WMAX = 1.0E-4
+TOX = '3.74E-09+DTOX P18'
+NCH = 5.500000E+17
```

$$KP_p \approx 70 \mu A/V^2$$

$$g_{m,p} : g_{m,n} = 4 : 1$$



$$KP_p \left(\frac{W}{L} \right)_p : KP_n \left(\frac{W}{L} \right)_n = 16 : 1$$



$$\left(\frac{W}{L} \right)_p : \left(\frac{W}{L} \right)_n = 64 : 1$$

$$C_{oxn} = 8.55m$$

$$C_{GS} \approx \frac{2}{3} W L C_{ox}$$

$$C_{oxp} = 9.12m$$

$$u_{0n} = \frac{26u}{8.55m \cdot 0.09} = 33m \quad I_D = \frac{1}{2} u_0 C_{GS} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad u_{0p} = \frac{4.94u}{9.12m \cdot 0.073} = 7.4m$$

- 对一偏置电流为100uA的五管OTA，通过晶体管的设计，使其等效输入噪声的80%来源于差分对M1和M2。

$$I_D \approx \frac{1}{2} \mu_0 C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad \rightarrow \quad \left(\frac{W}{L}\right)_n = \frac{1u}{500n} \quad \left(\frac{W}{L}\right)_p = \frac{64u}{500n}$$

NMOS

```
* GENERAL PARAMETERS
*
+CALCACM = 1
+LMIN = 1.5E-7
+WMAX = 1.0E-4
+TOX = '3.87E-09+DTOX N18'
+NCH = 3.869400E+17
```

$$KP_n \approx 280uA/V^2$$

PMOS

```
* GENERAL PARAMETERS
*
+CALCACM = 1
+LMIN = 1.5E-7
+WMAX = 1.0E-4
+TOX = '3.74E-09+DTOX P18'
+NCH = 5.500000E+17
```

$$KP_p \approx 70uA/V^2$$

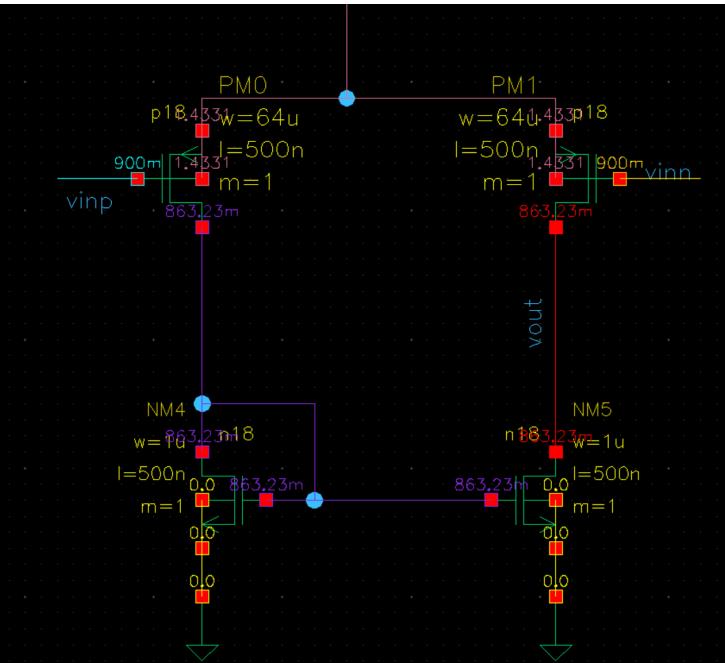
```
* MOBILITY PARAMETERS
*
+VSAT = 8.250000E+04 PVSAT = -8.
+LUU = 7.734979E-19 PUA = -1.
+UC = 1.200000E-10 PUC = 1.5
+PRWB = -0.2400000 PRWG = 0.4
+U0 = '(3.400000E-02)*(1+0.05*Sigma)*
+A0 = 0.8300000 KETA = -3.
```

$$C_{oxn} = 8.55m$$

$$C_{GS} \approx \frac{2}{3} W L C_{ox}$$

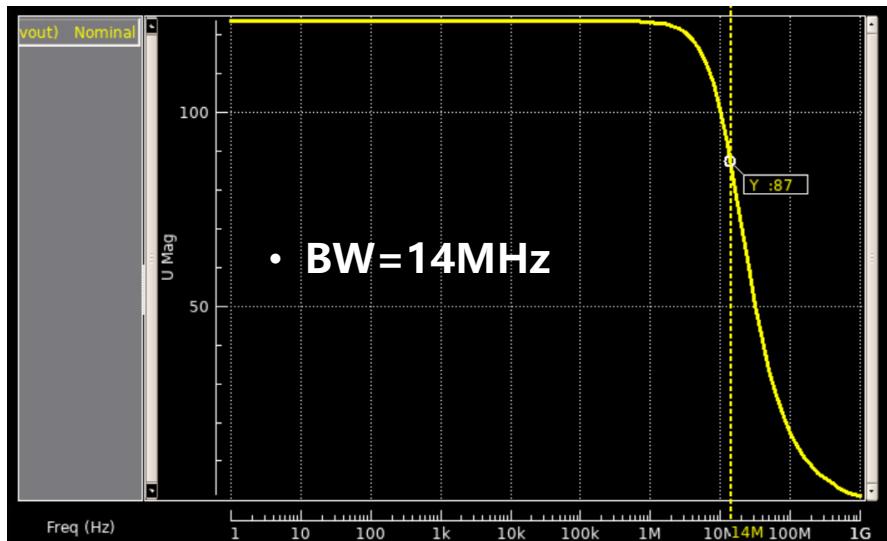
$$C_{oxp} = 9.12m$$

$$u_{0n} = \frac{26u}{8.55m \cdot 0.09} = 33m \quad I_D = \frac{1}{2} u_0 C_{GS} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad u_{0p} = \frac{4.94u}{9.12m \cdot 0.073} = 7.4m$$



- 对一偏置电流为100uA的五管OTA，通过晶体管的设计，使其等效输入噪声的80%来源于差分对M1和M2。

$$\left(\frac{W}{L}\right)_n = \frac{1u}{500n} \quad \left(\frac{W}{L}\right)_p = \frac{64u}{500n}$$



```
#####
noise analysis result at frequency 1.0000x #####
hierarchy
device      0:mnm5
rd          1.0525e-20
rs          89.4038a
id          67.3377f
rx          10.7077k
fn          1.1576p
total       1.2250p

hierarchy
device      0:mnm4
rd          9.8855e-21
rs          83.9735a
id          63.2477f
rx          10.3775k
fn          1.0873p
total       1.1506p

hierarchy
device      0:pmmp0
rd          8.7610e-22
rs          76.3880a
id          212.5966f
rx          1.0673k
fn          3.7697f
total       216.4426f

hierarchy
device      0:mpm1
rd          8.7623e-22
rs          76.3878a
id          212.5949f
rx          1.0673k
fn          3.7697f
total       216.4410f

#####
output noise voltage = 2.8085p volt^2/Hz
output rms noise   = 1.6759u volt/hz^(1/2)
equivalent input noise at vv4 = 6.7998n /hz^(1/2)
transfer function v(vout)/vv4 = 246.4585
```

- 对一偏置电流为100uA的五管OTA，通过晶体管的设计，使其等效输入噪声的80%来源于差分对M1和M2。

$$\overline{d\nu_{n,p}^2} = 432.88f \text{ } V^2/\text{Hz}$$

- 由于NMOS的1/f噪声远大于热噪声，差分对噪声占比只有15%

```
#####
noise analysis result at frequency 1.0000x #####
hierarchy
device      0:mnm5
rd          1.0525e-20
rs          89.4038a
id          67.3377f
rx          10.7077k
fn          1.1576p
total       1.2250p

hierarchy
device      0:mnm4
rd          9.8855e-21
rs          83.9735a
id          63.2477f
rx          10.3775k
fn          1.0873p
total       1.1506p

hierarchy
device      0:pmmp0
rd          8.7610e-22
rs          76.3880a
id          212.5966f
rx          1.0673k
fn          3.7697f
total       216.4426f

hierarchy
device      0:mpm1
rd          8.7623e-22
rs          76.3878a
id          212.5949f
rx          1.0673k
fn          3.7697f
total       216.4410f

#####
output noise voltage           = 2.8085p volt^2/Hz
##### output rms noise          = 1.6759u Volt/Hz^(1/2)
##### equivalent input noise at vv4 = 6.7998n /hz^(1/2)
##### transfer function v(vout)/vv4 = 246.4585
```

- 对一偏置电流为100uA的五管OTA，通过晶体管的设计，使其等效输入噪声的80%来源于差分对M1和M2。

$$\left(\frac{W}{L}\right)_p = \frac{64u}{500n}$$

$$\left(\frac{W}{L}\right)_n = \frac{1u}{500n}$$

↓ 增加电流镜面积

$$\left(\frac{W}{L}\right)_n = \frac{5u}{5u}$$

$$\left(\frac{W}{L}\right)_n = \frac{10u}{5u}$$

减小电流镜gm

- 通过同样的方法计算，差分对的噪声为总噪声的78%

```
##### noise analysis result at frequency 1.0000x #####
hierarchy
device      0:mpm0
rd          2.0698e-21
rs          140.3950a
id          394.9633f
rx          1.4545k
fn          6.8883f
total        401.9920f

hierarchy
device      0:mpm1
rd          2.0674e-21
rs          140.3925a
id          394.9424f
rx          1.4544k
fn          6.8879f
total        401.9707f

hierarchy
device      0:mmm5
rd          7.8555e-22
rs          62.9005a
id          92.4460f
rx          2.6765k
fn          27.2611f
total        119.7700f

hierarchy
device      0:mmm4
rd          7.3669e-22
rs          59.2449a
id          87.0605f
rx          2.5974k
fn          25.6730f
total        112.7928f

#####
### output noise voltage           = 1.0365p volt^2/Hz
### output rms noise             = 1.0181u volt/Hz^(1/2)
### equivalent input noise at vv4 = 3.0484n /Hz^(1/2)
### transfer function v(vout)/vv4 = 333.9804

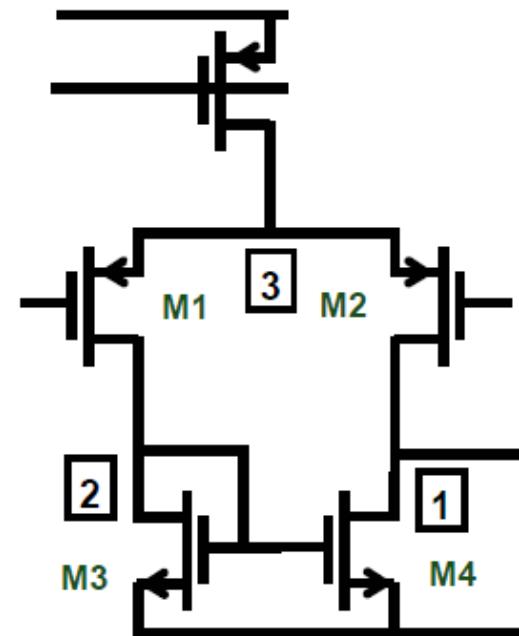
#####
### integral value of noise from 1.0000hz to 1.0000xHz
### total output noise voltage   = 1.3404m volt
### total input noise at vv4     = 3.9953u volt
```

第 14 章 HW04-05

Homework 4

》》课后作业

- 对一偏置电流为 $100\mu A$ 的五管OTA，共模电压为 $0.9V$ ，设计晶体管的尺寸，
 1. 使其在单位增益负反馈时系统性失调小于 $0.1mV$ ；
 2. 使其随机性失调的标准差 (std) 小于 $1mV$ ；
 3. 使其共模抑制比大于 $50dB$ 。



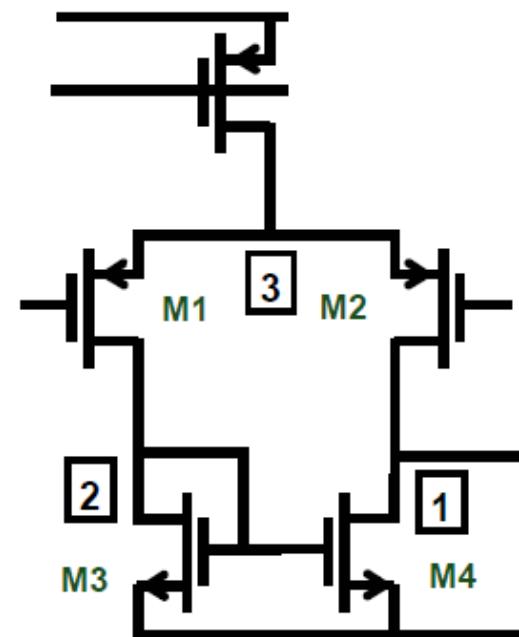
课后作业

- 对一偏置电流为100uA的五管OTA，共模电压为0.9V，设计晶体管的尺寸，
 - 使其在单位增益负反馈时系统性失调小于0.1mV；

消除系统性失调 $\rightarrow V_2 = V_1 = 0.9V$

$$V_{GST3,4} = 500mV$$

$$\left(\frac{W}{L}\right)_{3,4} = 1.4:1$$

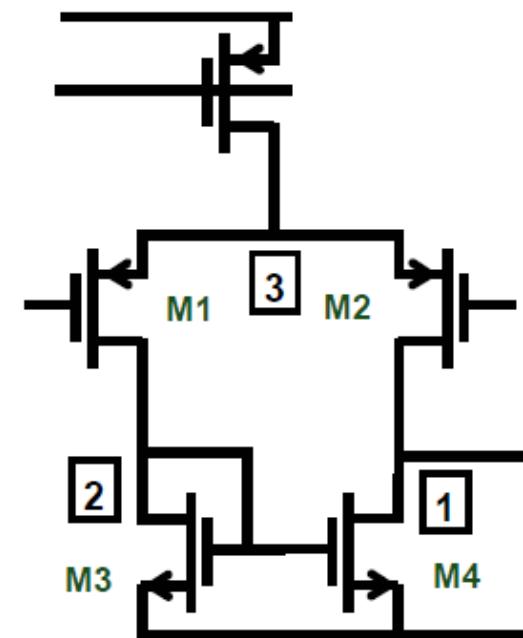


课后作业

- 对一偏置电流为100uA的五管OTA，共模电压为0.9V，设计晶体管的尺寸，
 - 使其随机性失调的标准差 (std) 小于 **1mV**；

$$V_{OS} = \Delta V_{T1} + \frac{g_{m3}}{g_{m1}} \Delta V_{T3} + \frac{V_{GST1}}{2} S$$

$$S = \frac{\Delta W/L_1}{W/L_1} + \frac{\Delta W/L_3}{W/L_3}$$



课后作业

- 对一偏置电流为100uA的五管OTA，共模电压为0.9V，设计晶体管的尺寸，
2. 使其随机性失调的标准差 (std) 小于
1mV；

$$V_{OS} = \Delta V_{T1} + \frac{g_{m3}}{g_{m1}} \Delta V_{T3} + \frac{V_{GST1}}{2} S$$

$$S = \frac{\Delta W/L_1}{W/L_1} + \frac{\Delta W/L_3}{W/L_3}$$

1. 将S项忽略

2. 令 $gm1=gm3$, 简化设计

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}} \quad \text{2 (mV*um)}$$

$$\frac{\Delta W/L}{W/L} = A_{WL} \sqrt{\frac{1}{W^2} + \frac{1}{L^2}}$$

1.8 (%*um)

+50 % for pMOST

课后作业

- 使其随机性失调的标准差 (std) 小于**1mV**;

考慮差分对，考慮正态分布

$$\sigma V_{T1} = \sigma V_{T3} = 0.5mV$$

$$WL_3 = 16\mu m^2$$

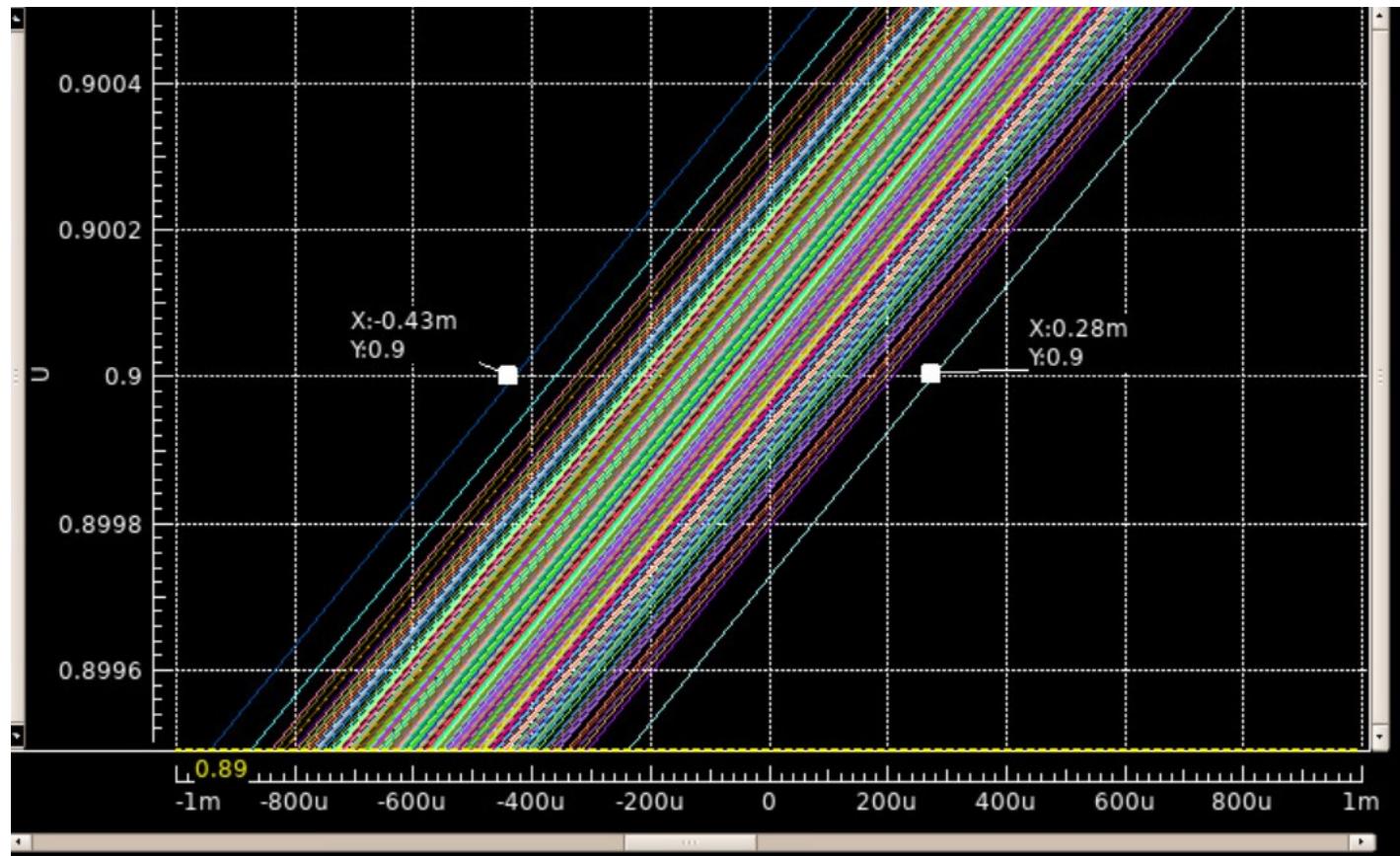
$$WL_1 = 36\mu m^2$$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{4.7u}{3.4u} \quad \left(\frac{W}{L}\right)_{1,2} = \frac{36u}{1u}$$

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}}$$

← 2 (mV*um)

》》》 仿真结果



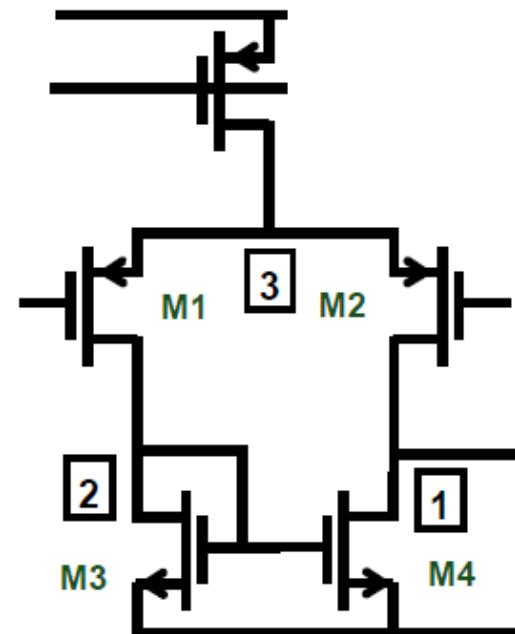
课后作业

- 对一偏置电流为100uA的五管OTA，共模电压为0.9V，设计晶体管的尺寸，
 - 使其共模抑制比大于 **50dB**。

$$CMRR_s = 2g_{m1}g_{m3}R_B \cdot (r_{02}||r_{04})$$

$$\begin{aligned} g_{m1} &= 635u, & g_{m3} &= 208u, \\ g_{ds2} &= 1.89u, & g_{ds4} &= 0.85u \end{aligned}$$

$$R_B > \sim 3K\Omega$$

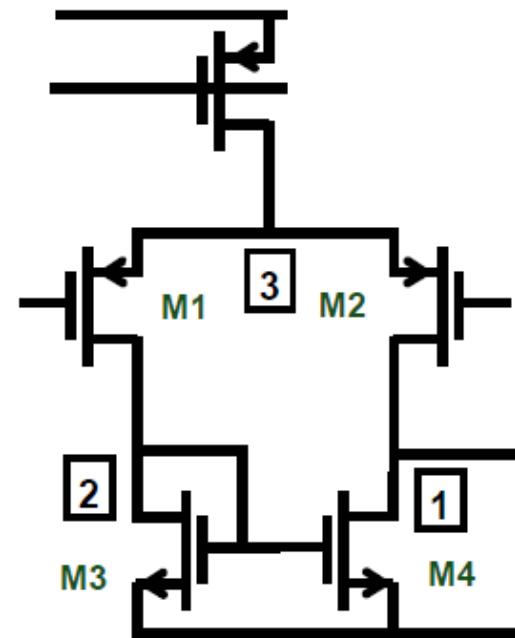


课后作业

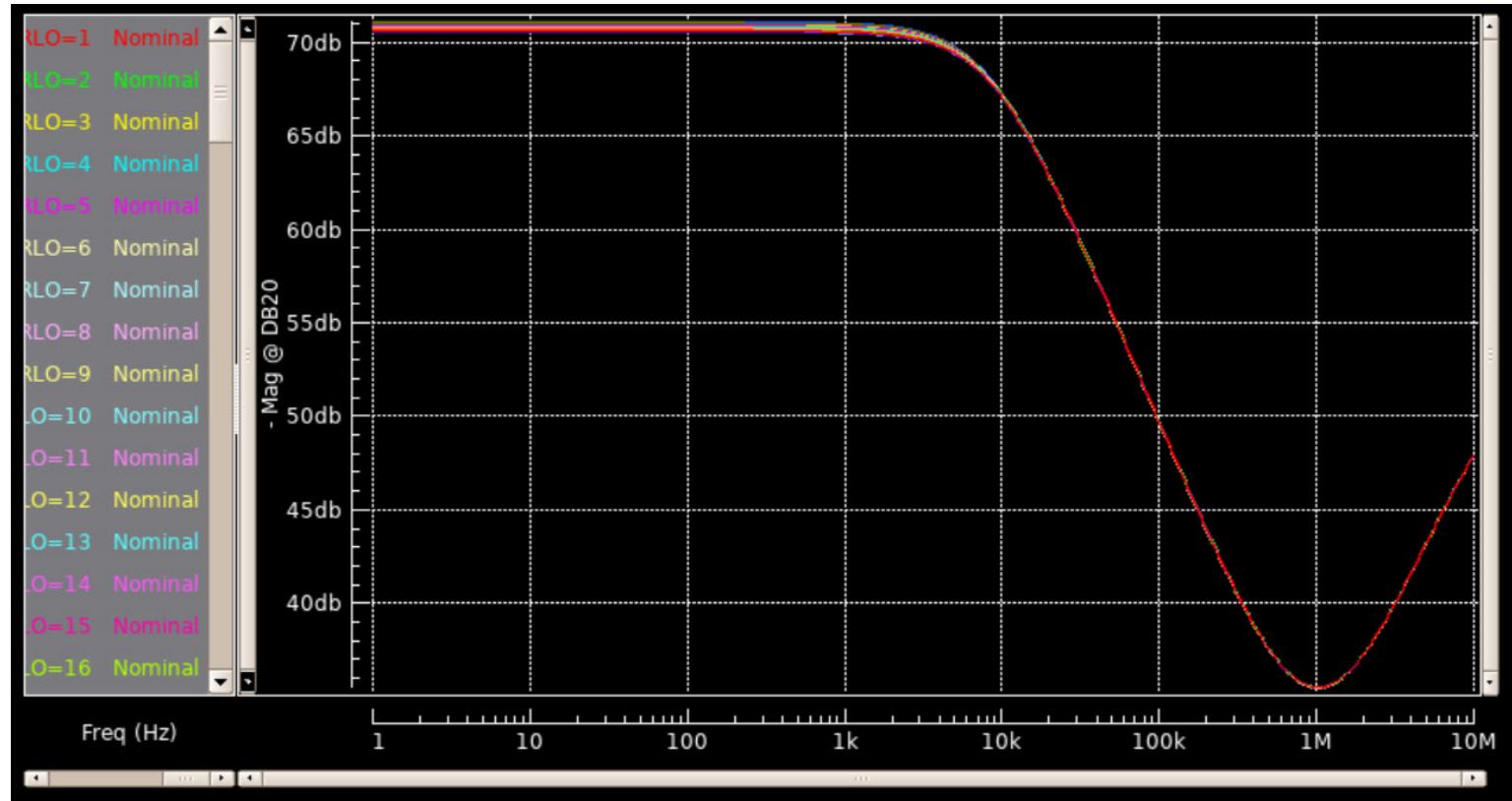
- 对一偏置电流为100uA的五管OTA，共模电压为0.9V，设计晶体管的尺寸，
 - 使其共模抑制比大于 **50dB**。

$$CMRR_r = \frac{V_E L_B}{V_{OS}}$$

$$L_B > \sim 10nm$$

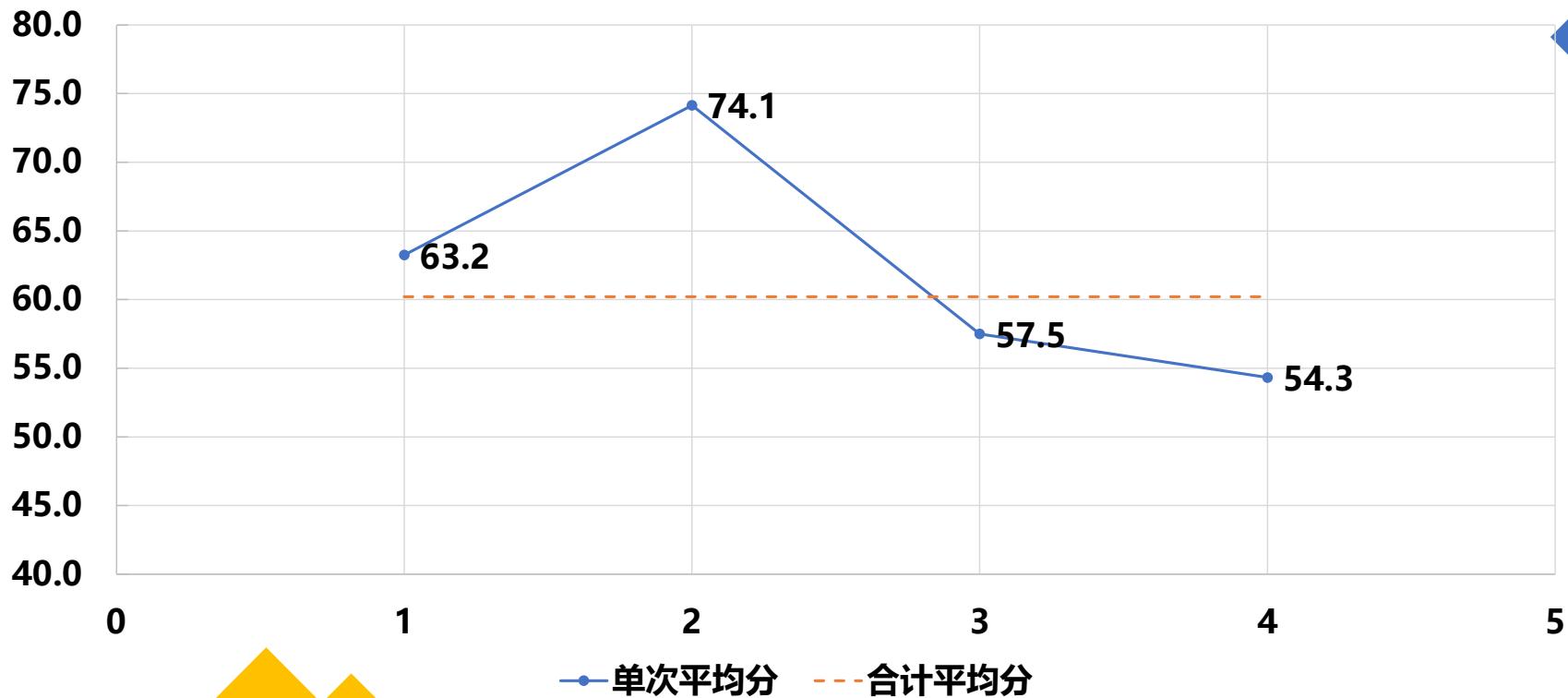


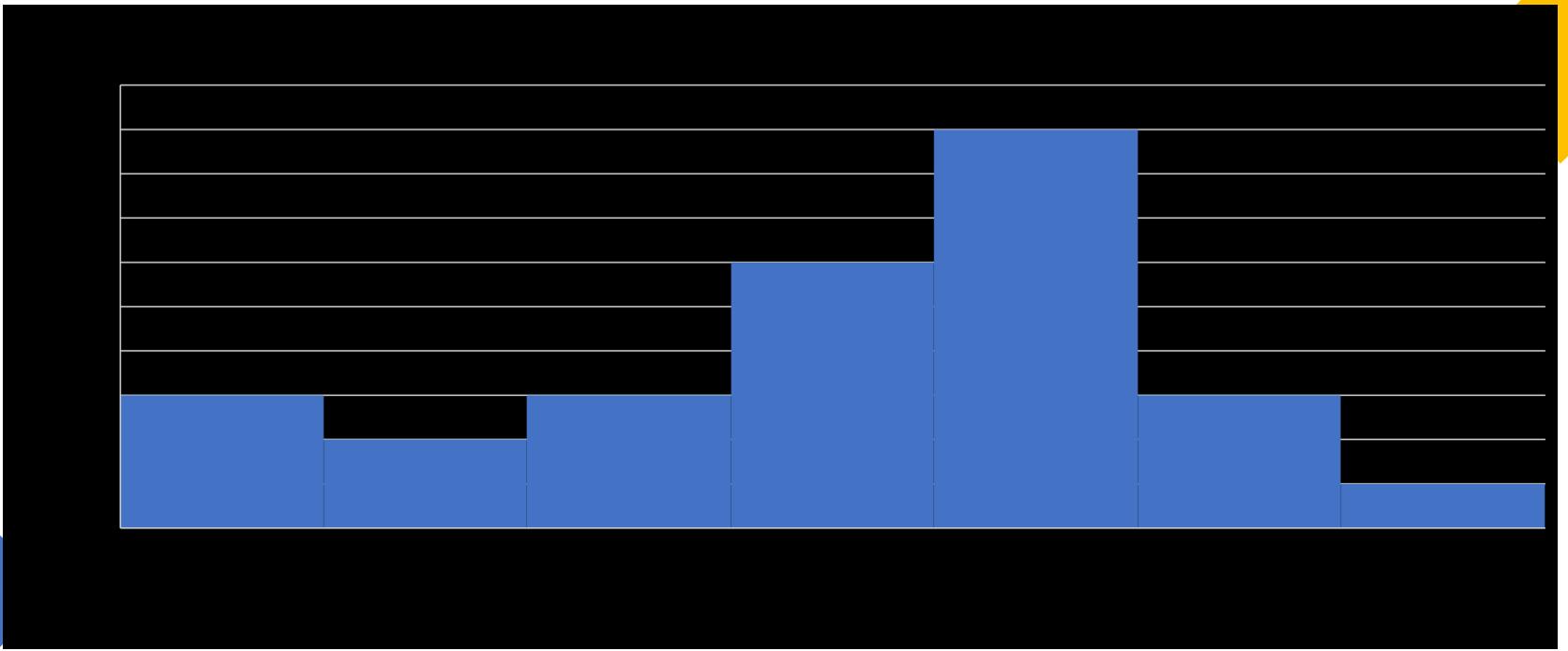
》》》 仿真结果



Homework Analysis 1-4

作业平均分





Homework 5

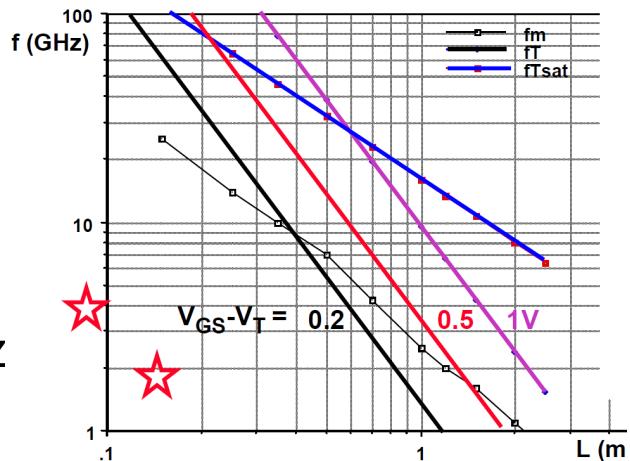
- 已知要求 $GBW=50MHz$, $CL=5pF$ 。设计一相位裕度大于70°的米勒运放。通过仿真结果，给出该设计运放的：

1. FOM
2. 相位裕度
3. 输入等效总噪声

1. 选择 $\alpha \beta \gamma$
2. 找到满足 GBW 最小的 f_T
3. 根据增益要求选择 L_6
 - 得到 f_{TH6}
4. 根据 C_L 和 L_6 计算 W_6

- 2 3 3
- $f_T = 1.2GHz$
- $L_6 = 0.2\mu m$
- $f_{TH6} = 30GHz \Rightarrow i = 0.04$
- **$W_6 = 375\mu m$**

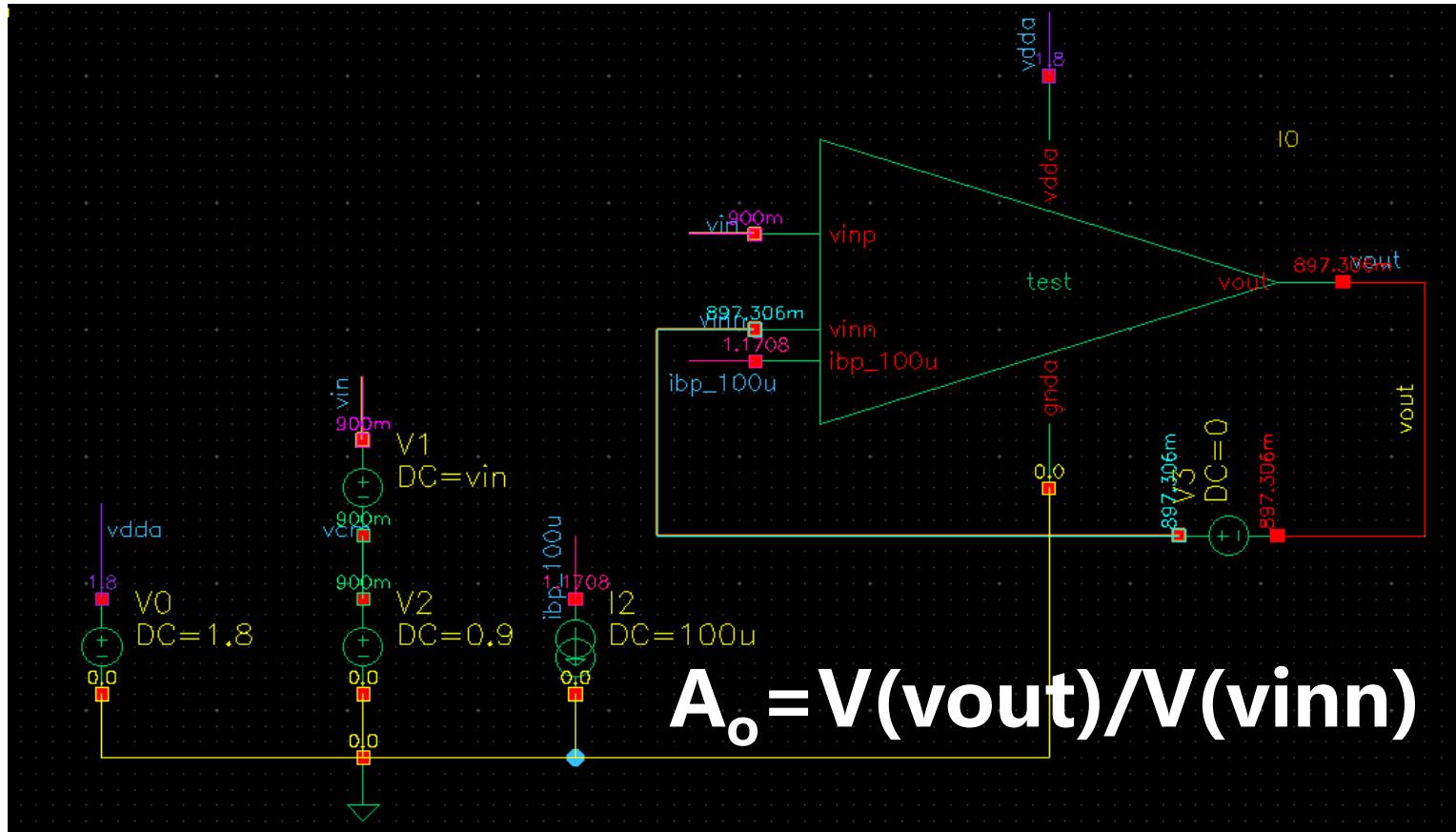
$$C_{GS} = 2kW, k = 2fF/\mu m, \text{for minL}$$



- 已知要求 $GBW=50MHz$, $CL=5pF$ 。设计一相位裕度大于70°的米勒运放。通过仿真结果，给出该设计运放的：

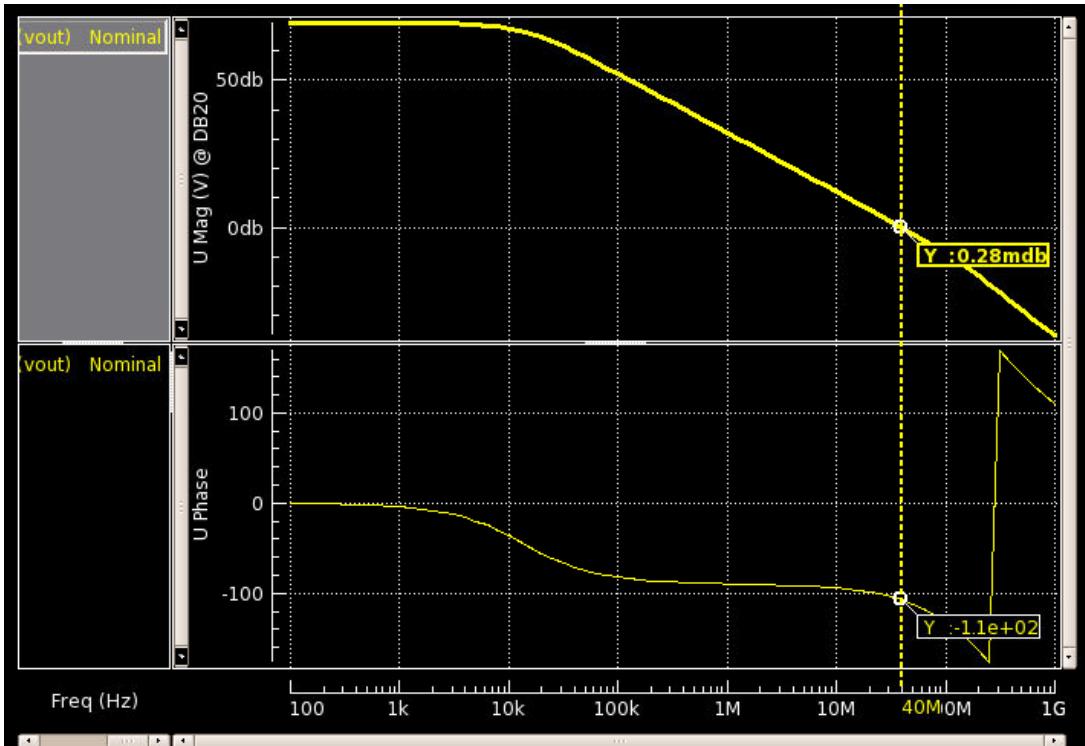
1. FOM
2. 相位裕度
3. 输入等效总噪声
5. 根据 I_{DSH6} 和反型系数*i*计算 I_{DS6}
 - $KP_n = 280\mu A/V^2$
 - $I_{DS6} = 10.5m * 0.04 = 420\mu A$
6. 通过选择的 α 和 C_L 计算 C_C
 - $C_C = 2.5pF$
7. 通过 C_C 计算 g_{m1} 和 I_{DS1}
 - $g_{m1} = 785\mu$
 - $I_{DS1} = 78.5\mu A$
 - $W1/L1 = 28\mu/0.5\mu$

Loop Gain仿真



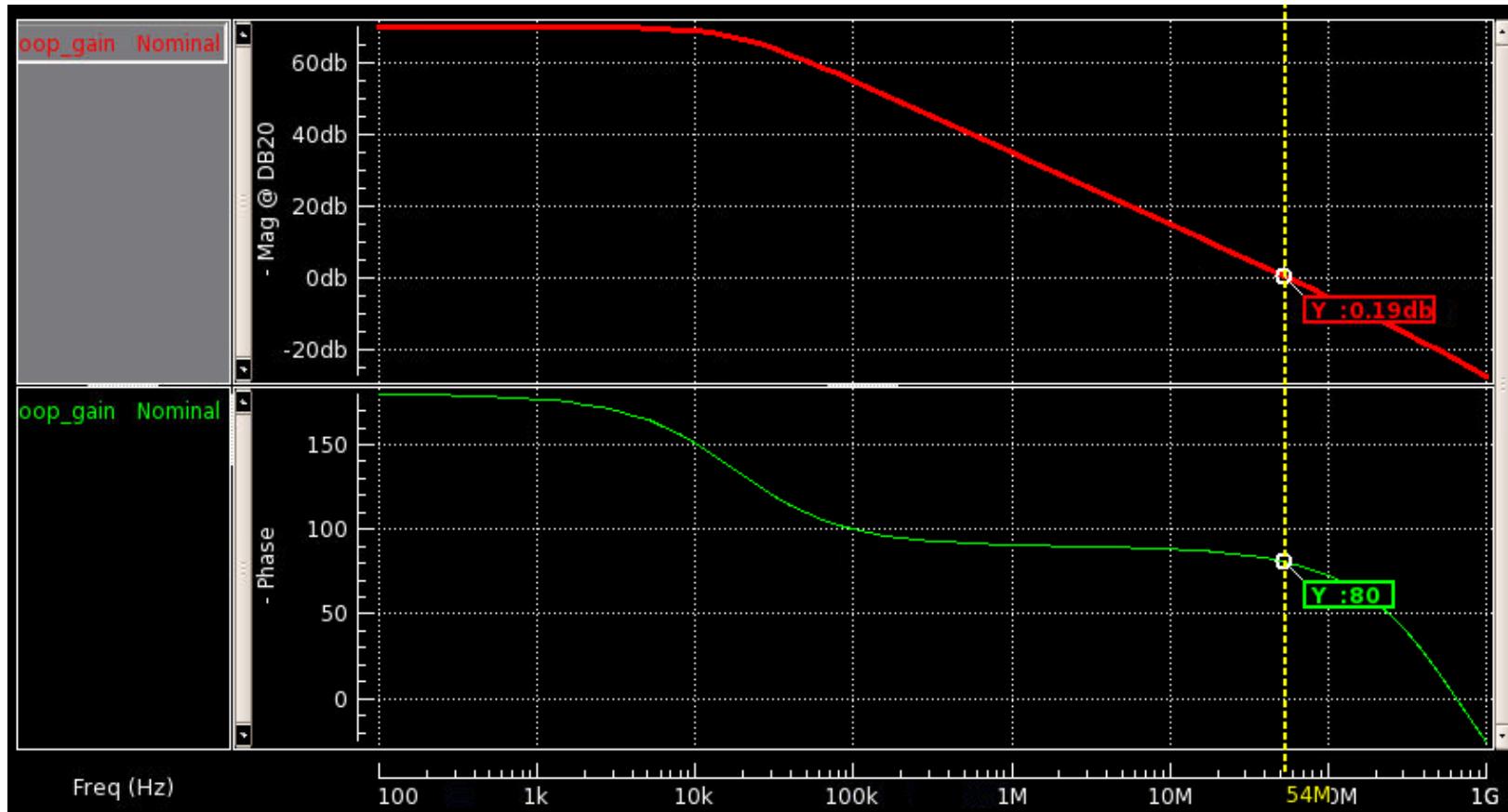
仿真结果

```
[ PM0 ]
region = Saturati
id = -78.1278u
ibs = 5.6807e-20
ibd = 14.4282a
vgs = -639.5856m
vds = -879.1882m
vbs = 0.0000
vth = -443.6520m
vdsat = -193.9362m
vod = -195.9335m
gm = 702.9307u
gds = 3.8089u
gmb = 224.1048u
cdtot = 34.9319f
cgtot = 108.1365f
cstot = 134.3769f
cbtot = 83.6754f
cgs = 89.2852f
cgd = 11.7448f
i1 = -78.1278u
i2 = 0.0000
i3 = 78.1278u
i4 = 879.2027f
```



```
[ NM2 ]
region = Cutoff
id = 406.0396u
ibs = -2.6970e-19
ibd = -289.8949p
vgs = 421.6335m
vds = 920.4203m
vbs = 0.0000
vth = 473.4460m
vdsat = 54.1268m
vod = -51.8125m
gm = 8.8316m
gds = 170.2431u
gmb = 2.3050m
cdtot = 338.3632f
cgtot = 488.4598f
cstot = 515.2213f
cbtot = 629.1785f
cgs = 221.5820f
cgd = 137.2870f
i1 = 406.0399u
i2 = 0.0000
i3 = -406.0396u
i4 = -312.9054p
```

仿真结果



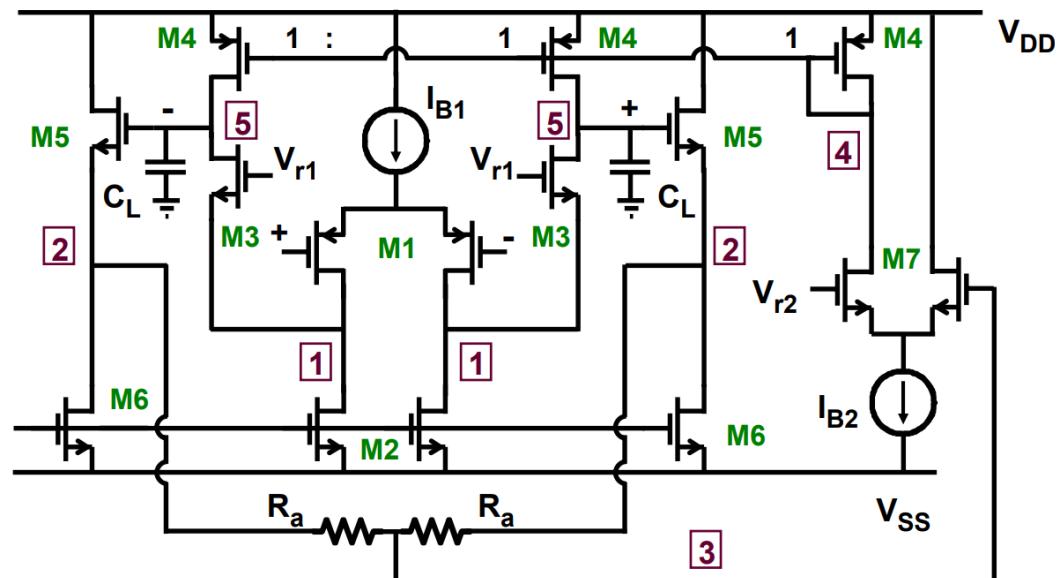
第 15 章 HW06

Homework 6

课后习题

□ 已知要求 $GBW_{DM}=50MHz$, $GBW_{CM}=100MHz$, $C_L=5pF$ 。设计一共模&差模相位裕度均大于70°的运放。通过仿真给出：

- 差模增益
 - 功耗
 - 共模抑制比CMRR
-
- 差模-蓝色
 - 共模-红色
 - 偏置-黑色



电路图过于老旧，其架构不适合我们工艺所要求的1.8V电源电压

$$V_{OUT} - V_{GS5} = V_{r2}$$

$$V_{r2} - V_{GS7} > V_{DSat}$$

$$V_{OUT} + V_{GS1} < V_{DD} - V_{DSat}$$

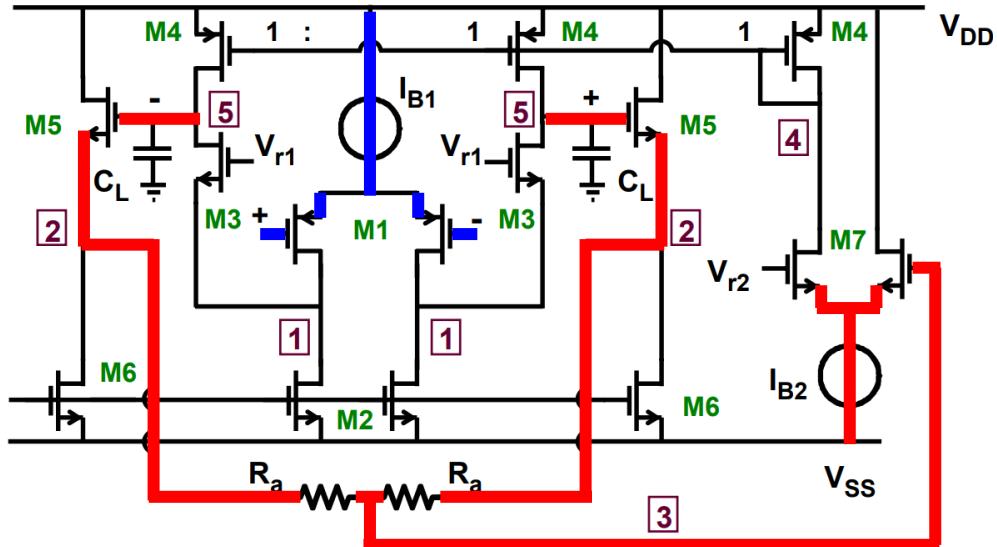
$$V_{GS5} + V_{GS7} + V_{DSat} < V_{OUT} < V_{DD} - V_{DSat} - V_{GS1}$$

假设 $V_{GS} = 0.7$, $V_{DSat} = 0.2V \rightarrow 1.6V < V_{OUT} < 1.1V$

方案1：使用3.3V电源

方案2：弱反型区电路

方案3：修改电路



Homework 6

Solution 1: Using 3.3V supply

- $\text{GBW}_{DM} = 50\text{MHz}, C_L = 5\text{pF}$

$$GBW_{DM} = \frac{g_{m1}}{2\pi C_L}$$

$$g_{m1} = GBW_{DM} \cdot 2\pi C_L = 1.57\text{mA/V}$$

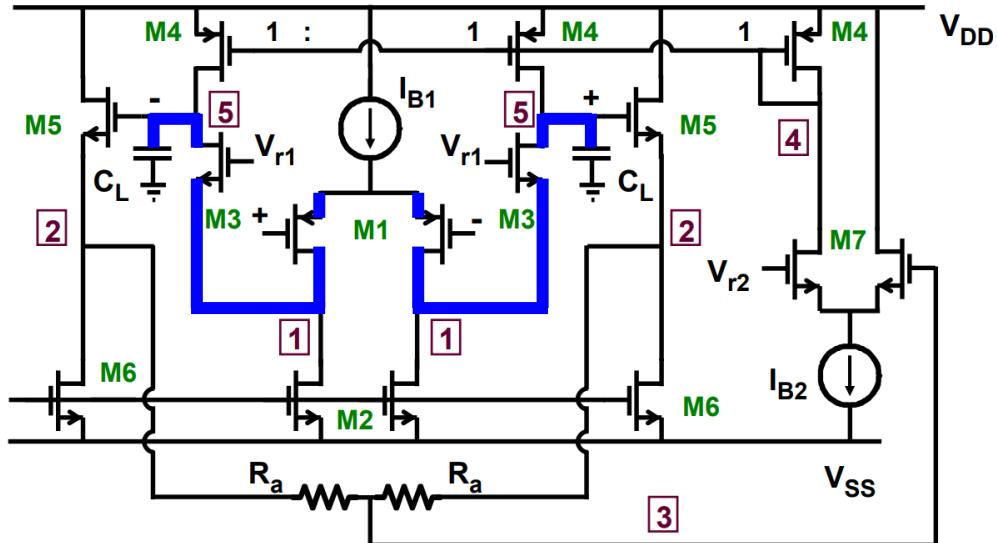
合理假设 $g_m/I_D = 10, V_{GST} = 0.2$

$$I_{D1} = 157\mu\text{A}$$

又根据 $I_D = \frac{1}{2} K P_P \frac{W}{L} (V_{GS} - V_{TH})^2$

得到 $\left(\frac{W}{L}\right)_1 = \frac{2I_D}{K P_P \cdot (V_{GS} - V_{TH})^2} = \frac{2 \cdot 157\mu\text{A}}{70\mu\text{A} \cdot 0.04} = 112$

不妨先设 $\left(\frac{W}{L}\right)_1 = \frac{56\mu\text{A}}{500n}$



- $\text{GBW}_{CM} = 100\text{MHz}, C_L = 5\text{pF}$

$$GBW_{CM} = \frac{g_{m7}}{4\pi C_L}$$

$$g_{m7} = GBW_{CM} \cdot 4\pi C_L = 6.28mA/V$$

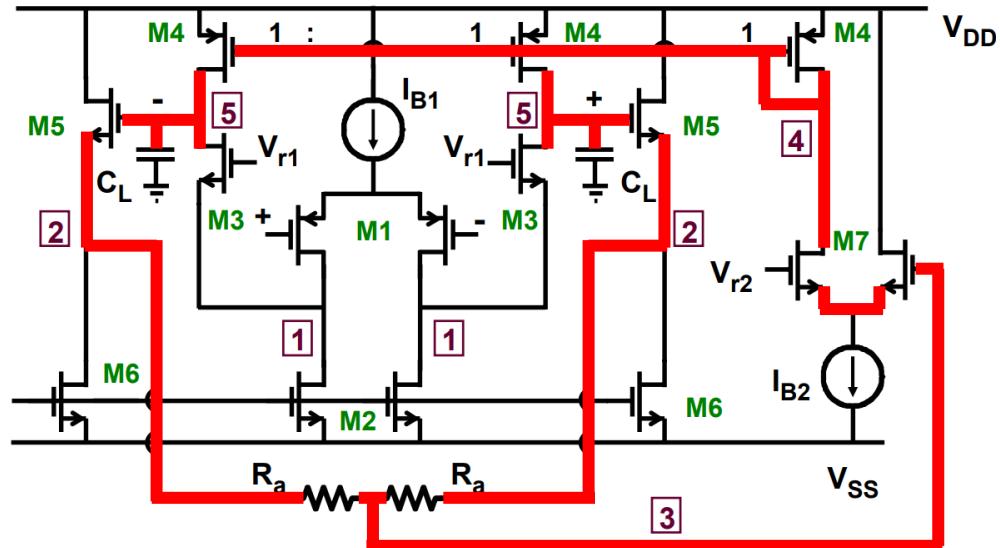
合理假设 $g_m/I_D = 10, V_{GST} = 0.2$

$$I_{D7} = 628\mu A$$

还根据 $I_D = \frac{1}{2} K P_N \frac{W}{L} (V_{GS} - V_{TH})^2$

得到 $\left(\frac{W}{L}\right)_7 = \frac{2I_D}{K P_N \cdot (V_{GS} - V_{TH})^2} = \frac{2 \cdot 628\mu}{280\mu \cdot 0.04} = 112$

不妨再设 $\left(\frac{W}{L}\right)_7 = \frac{56\mu}{500n}$



已知 $I_{D7} = 628\mu A$

得到 $I_{D4} = 628\mu A$

$I_{D3} = 628\mu A$

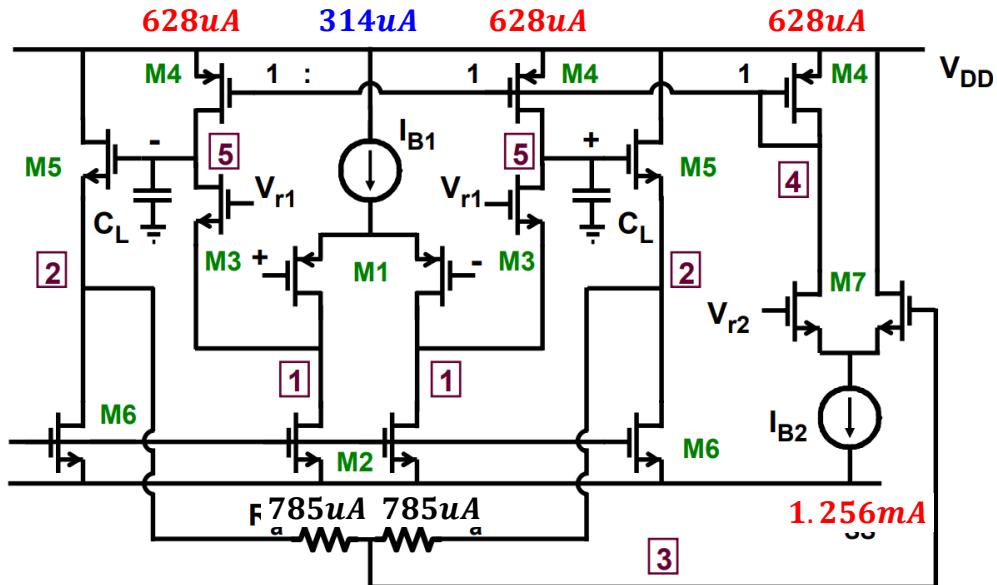
$I_{B2} = 1.256mA$

已知 $I_{D1} = 157\mu A$

得到 $I_{B1} = 314\mu A$

根据 I_{D4} 和 I_{D1} 得到 $I_{D2} = 785\mu A$

全部假设 $g_m/I_D = 10$, $V_{GST} = 0.2$



$$r_{DS} = \frac{V_E L}{I_{DS}} = \frac{40 \cdot 0.5}{628\mu A} \approx 30k$$

晶体管	M1	M2	M3	M4	M5	M6	M7
尺寸(um)	56/0.5	70/0.5	56/0.5	224/0.5	?	?	56/0.5

源极跟随器的频率响应较为复杂，具体内容参考《电子电路》课件CH6+频率响应，这里不做具体要求：

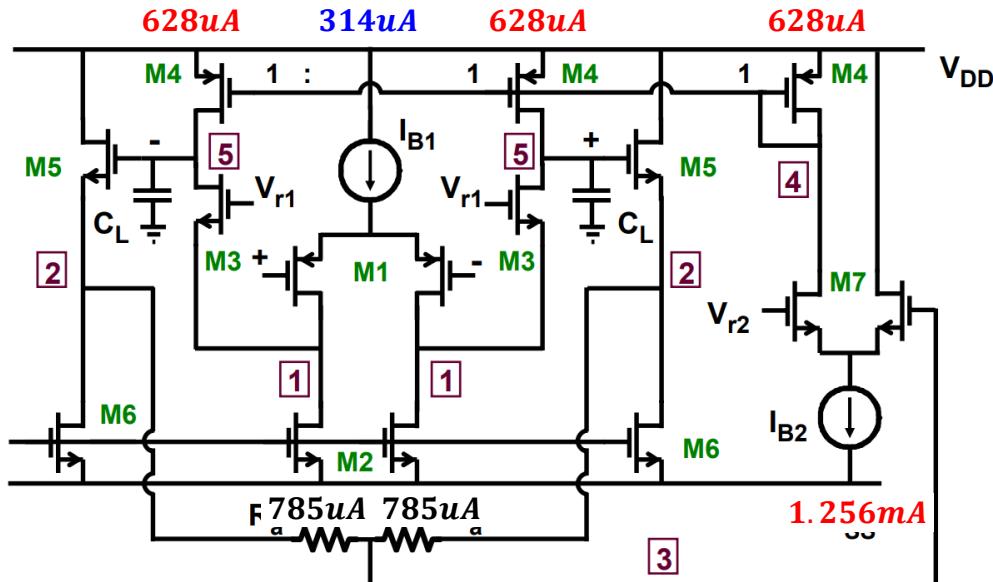
源随器主极点：

$$\frac{1}{R_S C_{GD} + \frac{C_L + C_{GS}}{g_m}}$$

源随器主极点就是Net5处极点

因为源随器的 C_L 的较小， g_m 和 C_{GS} 的要求就是特征频率

因此， $W/L=36\mu/180n$, $I_D=1.12mA$ 可以支持50GHz → 降低电流至112uA

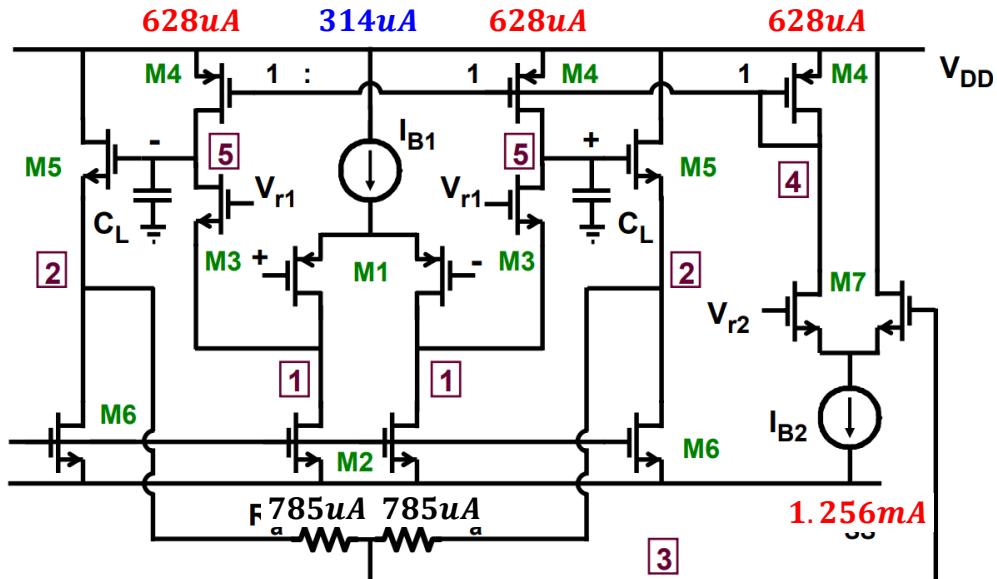


晶体管	M1	M2	M3	M4	M5	M6	M7
尺寸(um)	56/0.5	70/0.5	56/0.5	224/0.5	36/0.18	10/0.5	56/0.5

源极跟随器的频率响应较为复杂，具体内容参考《电子电路》课件CH6+频率响应，这里不做具体要求：

源随器驱动能力：

112 μ A的驱动电流，如果想要支持1Vpp的摆幅，电阻 R_a 至少需要4.46K Ohm，考虑到负载电阻上的电流消耗， R_a 取10K Ohm.



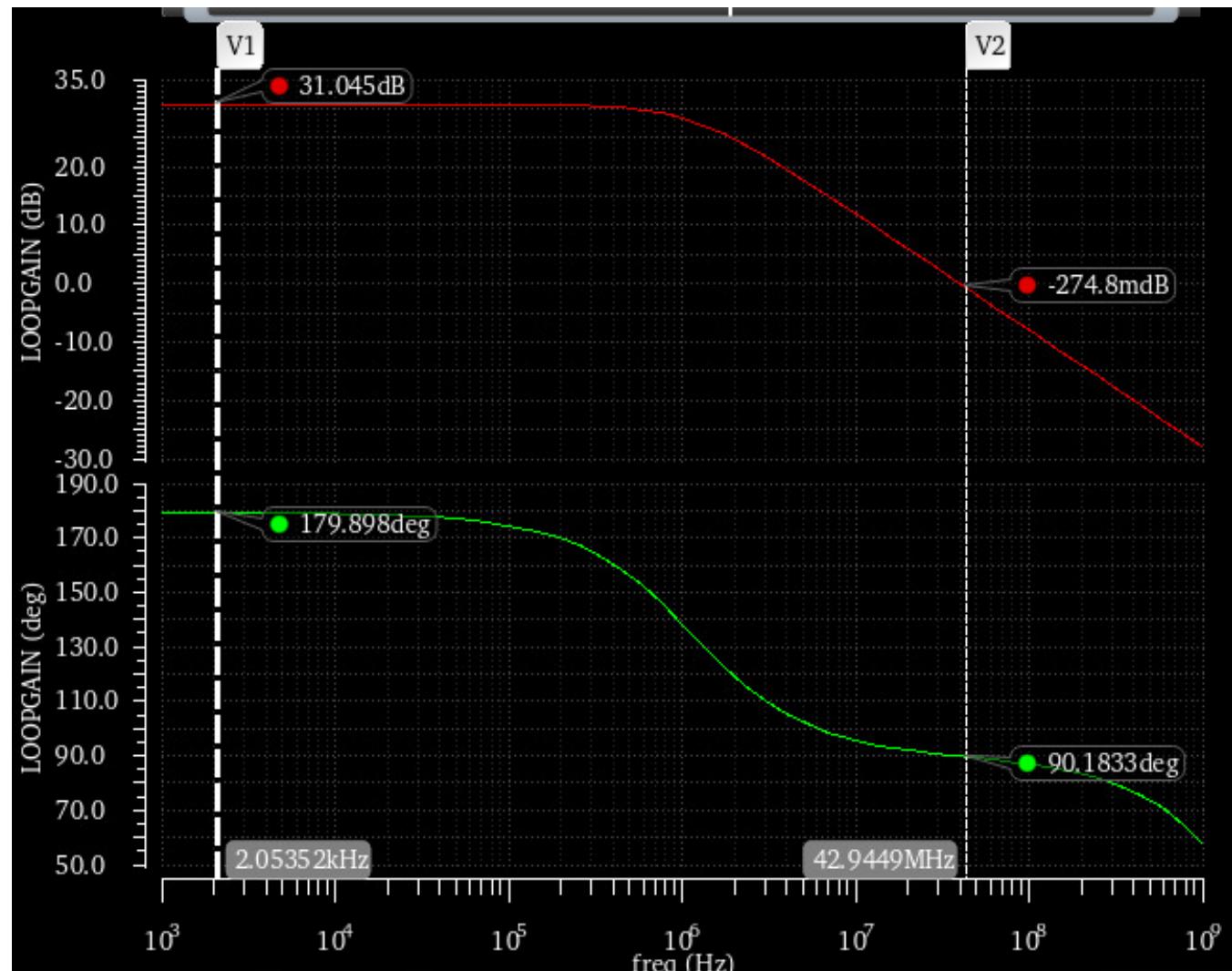
晶体管	M1	M2	M3	M4	M5	M6	M7
尺寸(μ m)	56/0.5	70/0.5	56/0.5	224/0.5	36/0.18	10/0.5	56/0.5

仿真得到：

- $r_{04} = 25.5K$
- $g_{m1} = 1.41m$

计算得到：

- $A_0 = 31.1dB$
- $GBW = 44.9M$



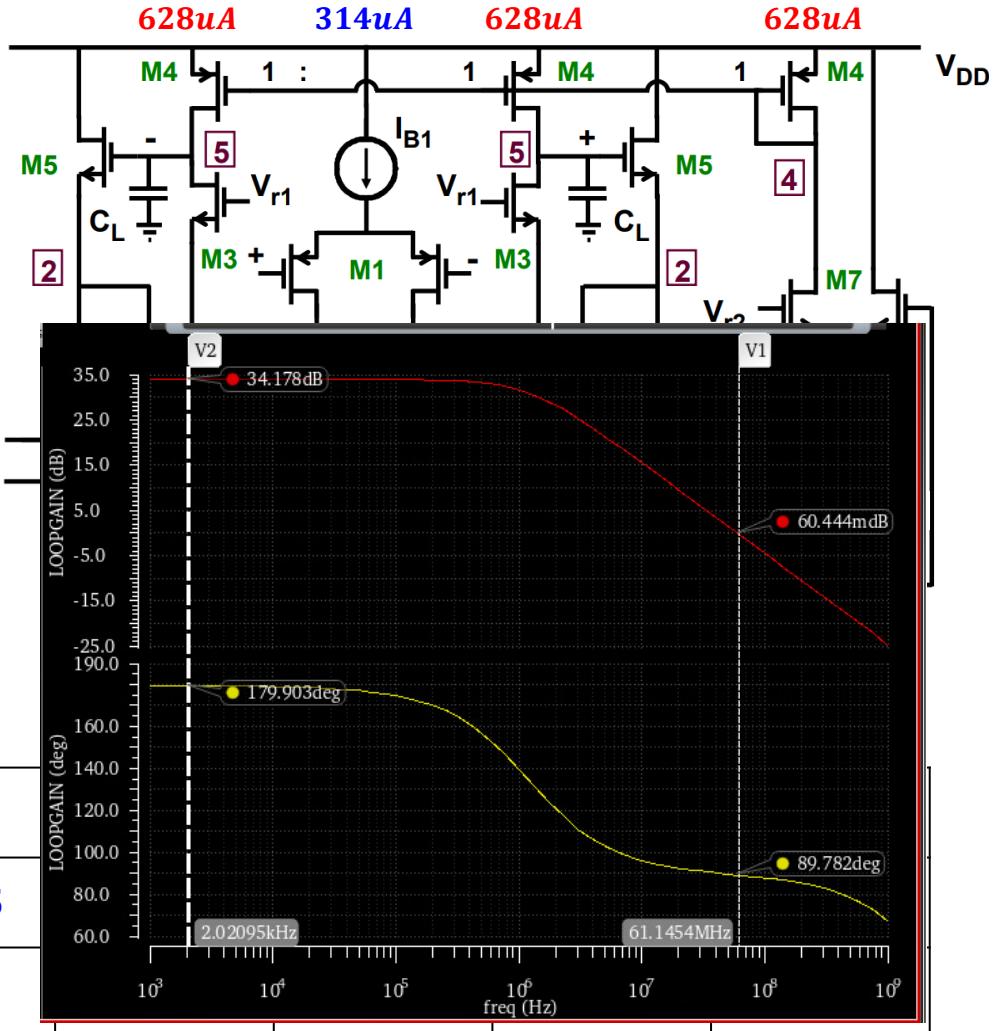
增加 g_{m1} by 增加电流 I_{B1}
或增加 $(W/L)_1$

修改 $(W/L)_1=56/0.25$ 后

- $A_0 = 34.2 \text{ dB}$
- $\text{GBW} = 61.1 \text{ M}$

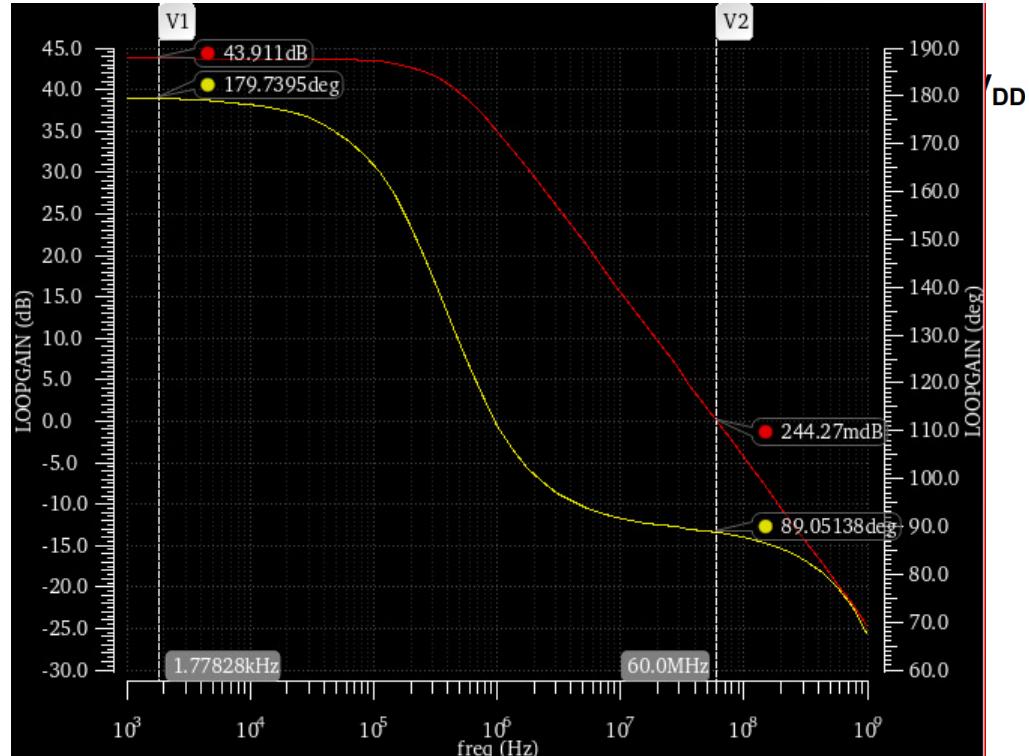
✓ 增益的瓶颈在于M4的
电阻值，因此降低M1
的长度不会降低增益

晶体管	M1	M2	M3
尺寸(um)	56/0.5	70/0.5	56/0.5
	56/0.25		

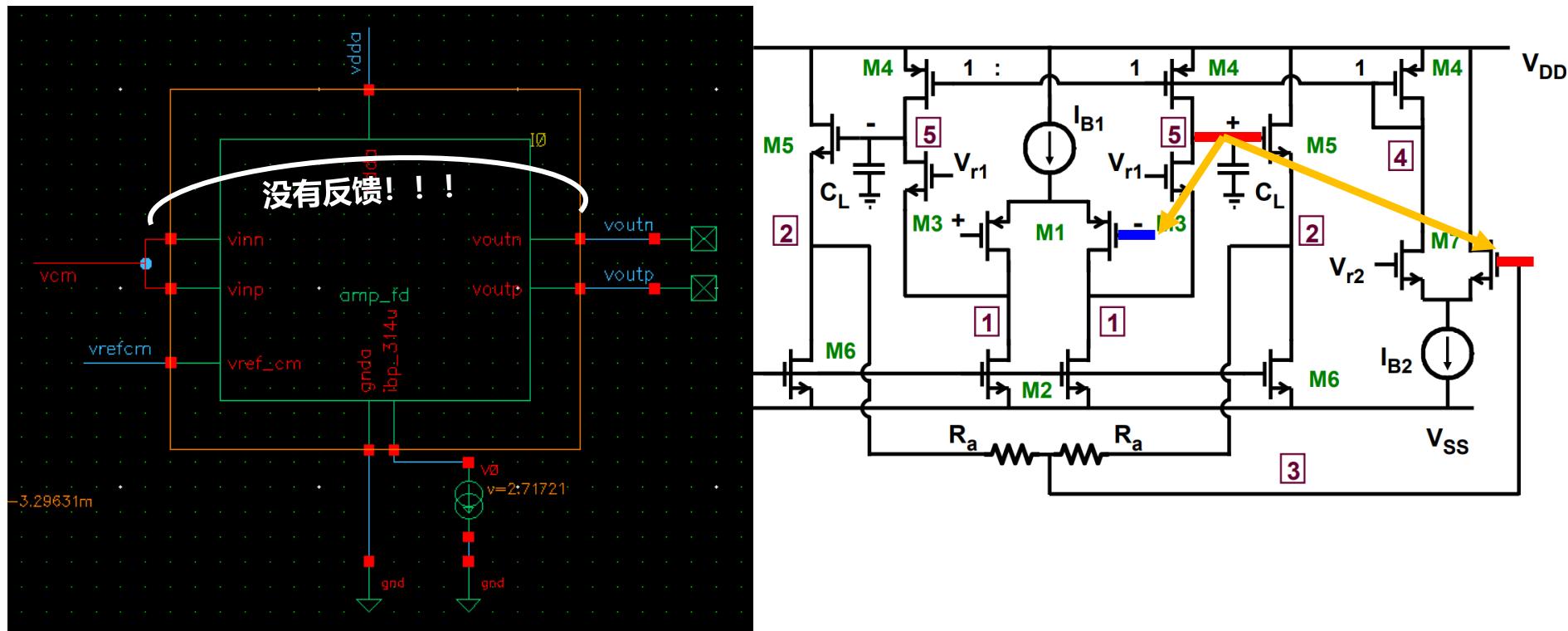


增加 r_{04} by 增加 L_4

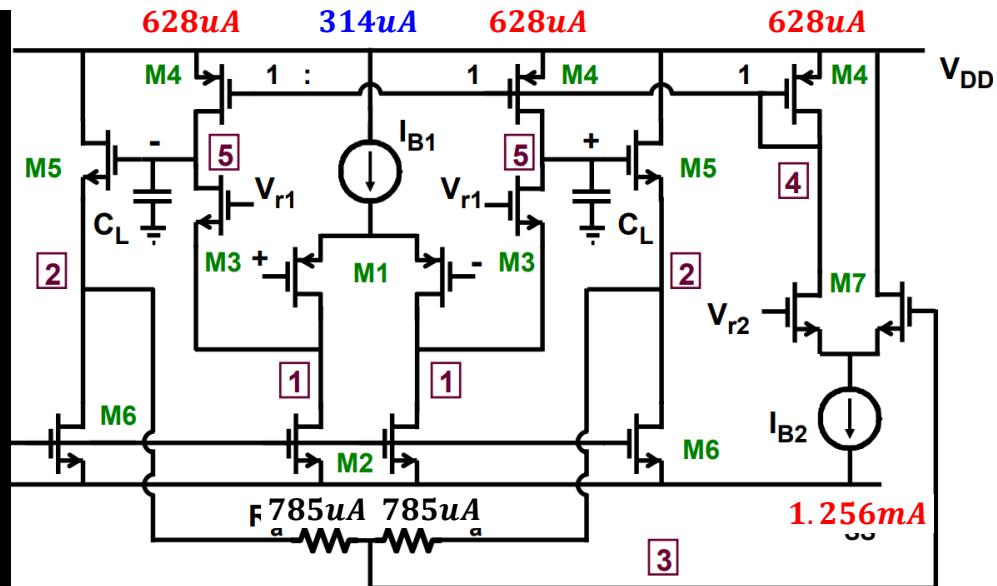
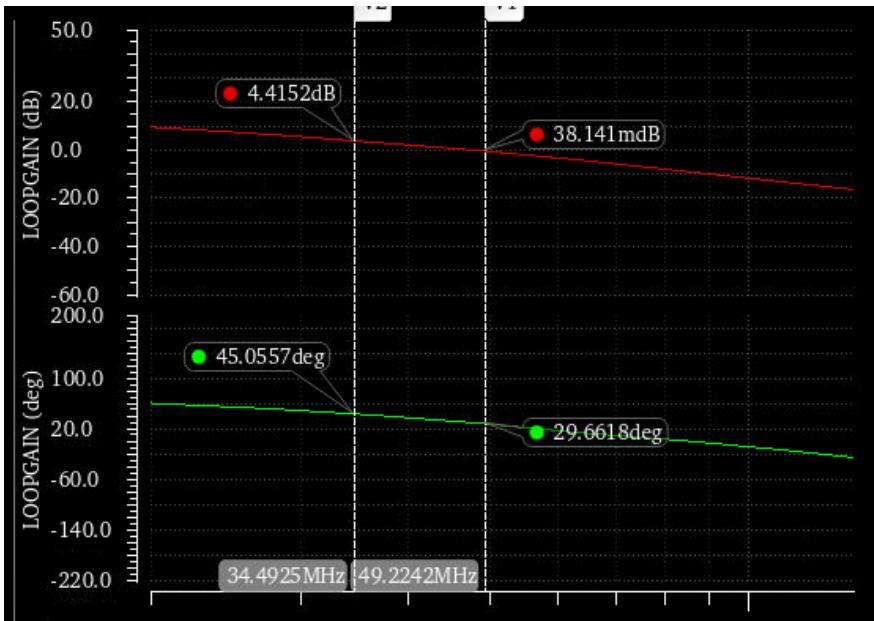
- ✓ r_{04} 上升至78K
- ✓ GBW保持不变，增益上升9dB至43.9dB



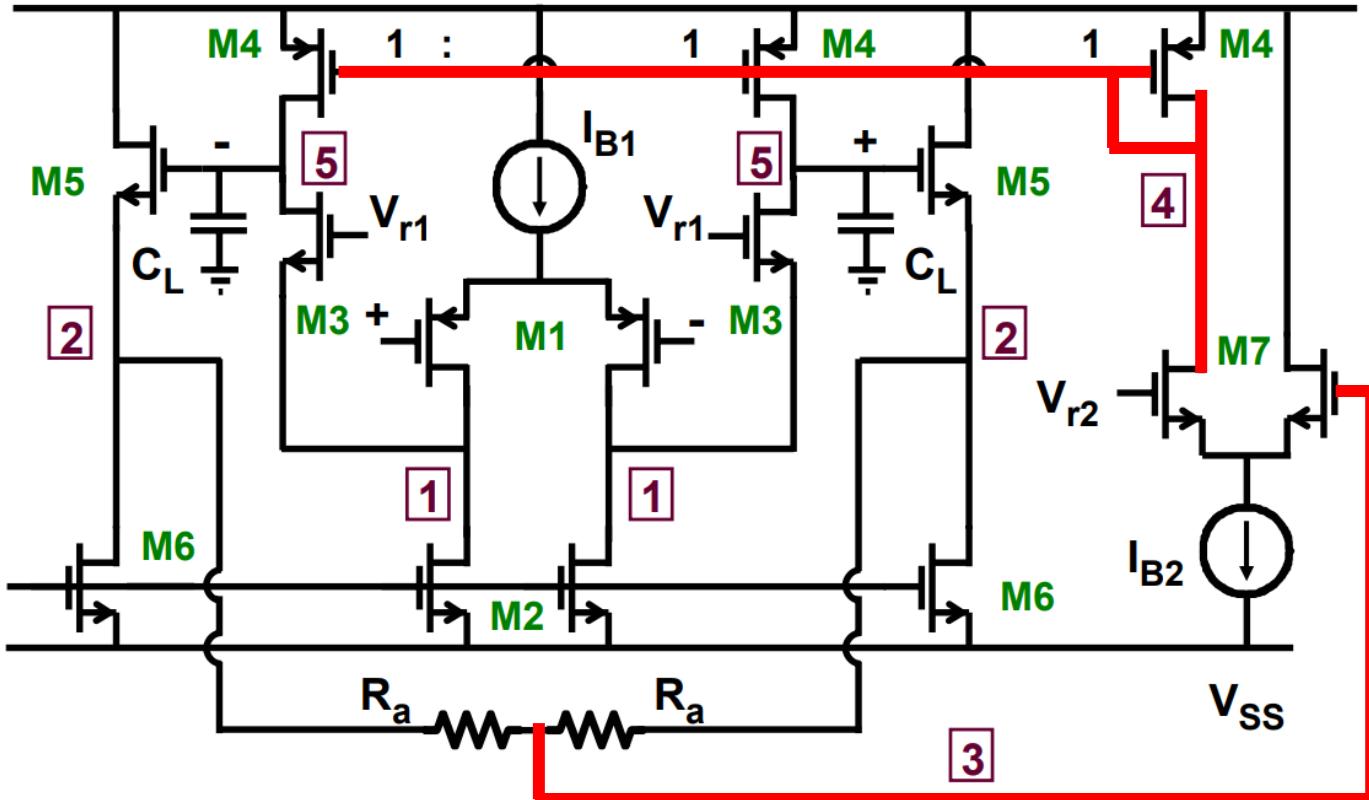
晶体管	M1	M2	M3	M4	M5	M6	M7
尺寸(um)	56/0.5	70/0.5	56/0.5	224/0.5	36/0.18	10/0.5	56/0.5
	56/0.25			224/2			



共模测试，差分信号采取开环设置，否则 V_{out} 的值在作用在共模反馈差分对M7的同时，也将通过差模反馈回路作用到M1



- 经过仿真, $g_{m7}=5.6\text{mA/V}$, 略低于所需要的 6.28mA/V 。
- 发现相位裕度只有29度, 次极点出现在34.5M左右(相移135度)。



V-- 可能出现次极点的位置?

- Net3
RC组成的次极点显而易见
- Net4
Net4对于差模信号回路只是偏置；但是，对于共模反馈却是信号回路的一部分

Net3: 反馈电阻R=10K的情况下

- $C_{GS7} = 130f$
- $f_{nd} = 244M$

Net4:

- $C_{G4} = 2.74pF$
- $g_{m4} = 2.39m$
- $f_{nd} = 46M$

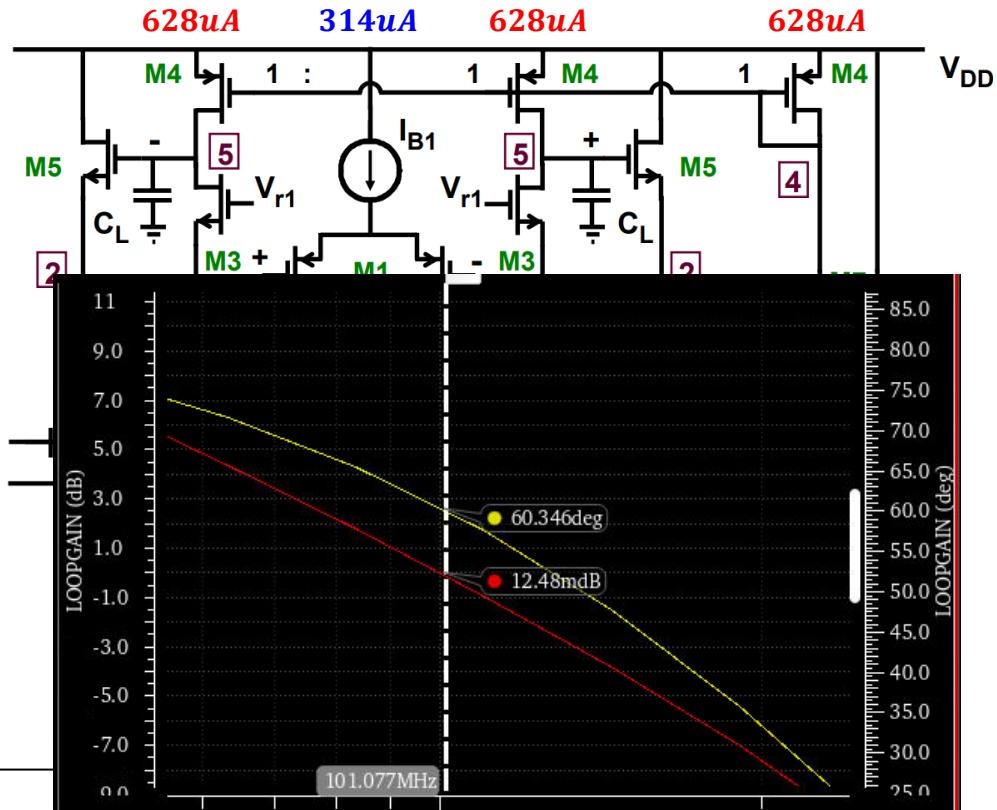
减小M4的尺寸，会使得增益再次减小，在没有增益要求的时候，可以如此修改。

W/L₄重新改小一半，Net5：

- $C_{G4}=0.67\text{pF}$
- $\text{PM}=65$
- $f_{nd}=130\text{M}$

在稍修改M7尺寸后

- $\text{GBW}=101\text{M}$
- $\text{PM}=60.3$



晶体管	M1	M2	M3	M4	M5	M6	M7
尺寸(um)	56/0.5	70/0.5	56/0.5	224/2	36/0.18	10/0.5	56/0.5
修改后	56/0.25			112/1			80/0.2

课后习题

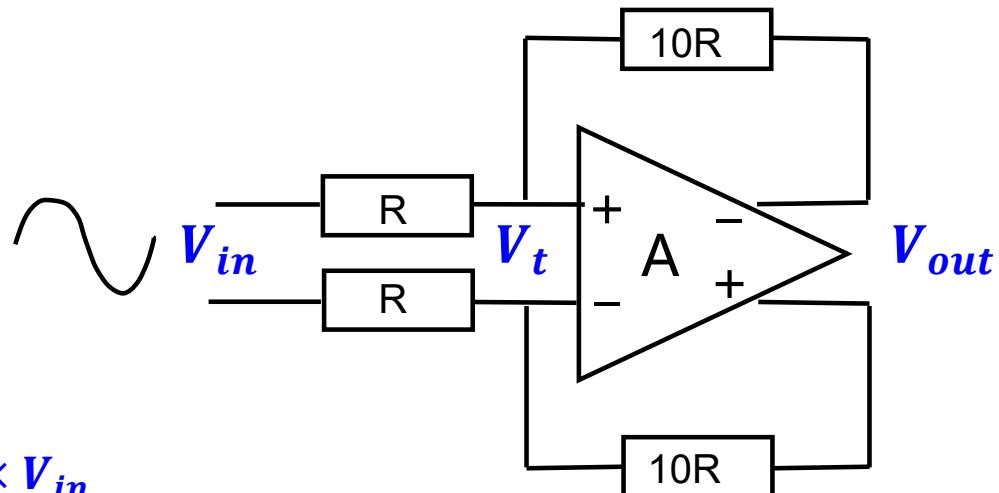
□ 将上述设计的差分运放，通过电阻设置成10倍放大，观察输入差模和共模信号分别有100mVpp, 10kHz的正弦信号时，差模输出信号的大小，并分析是否符合预期。

$$\left\{ \begin{array}{l} \frac{V_{out} - V_t}{10R} = \frac{V_t - V_{in}}{R} \\ V_{out} = -A \cdot V_t \end{array} \right.$$

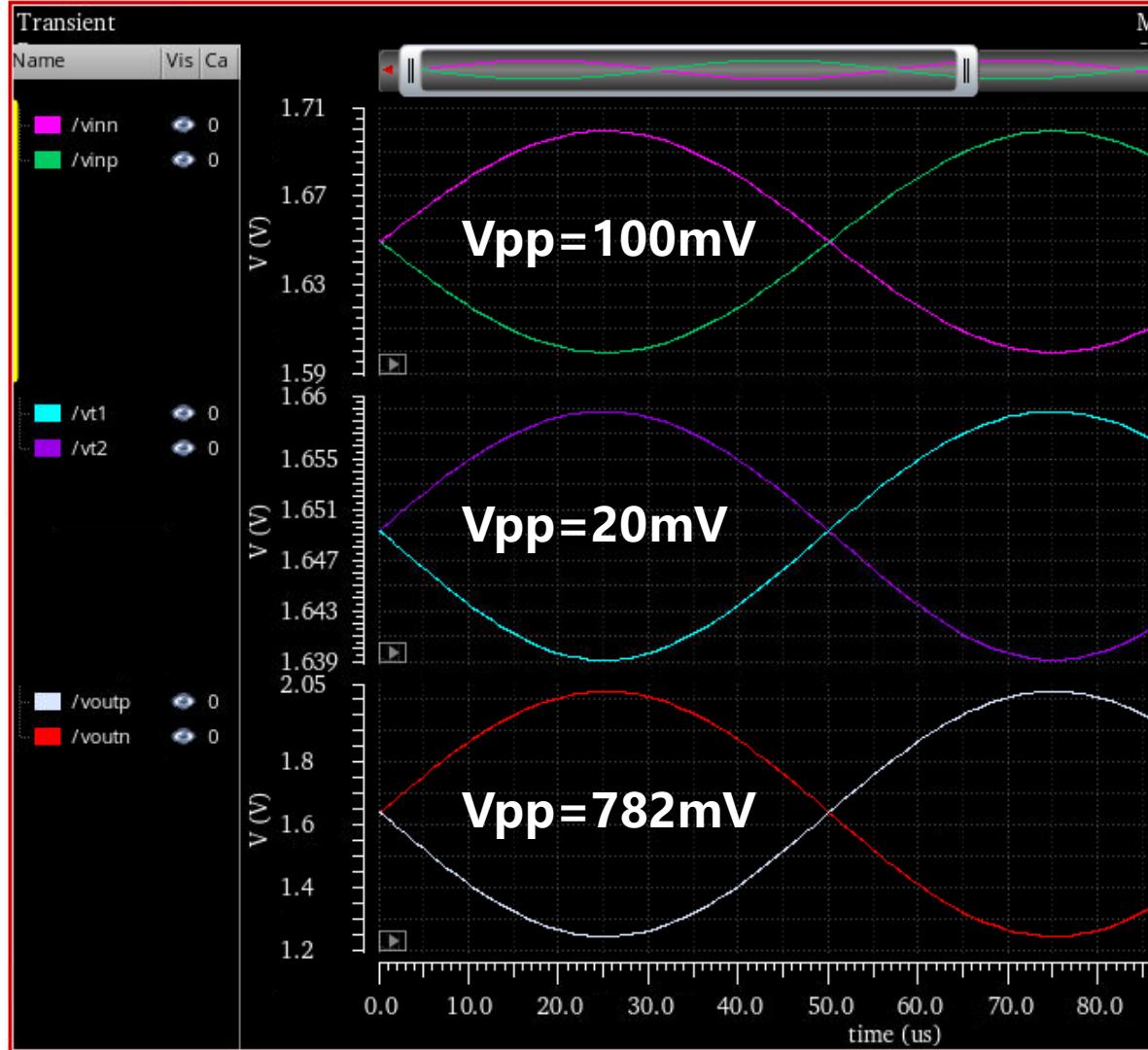
从之前的仿真结果知晓：

- $A_0 = 34.2 \text{dB} = 51$

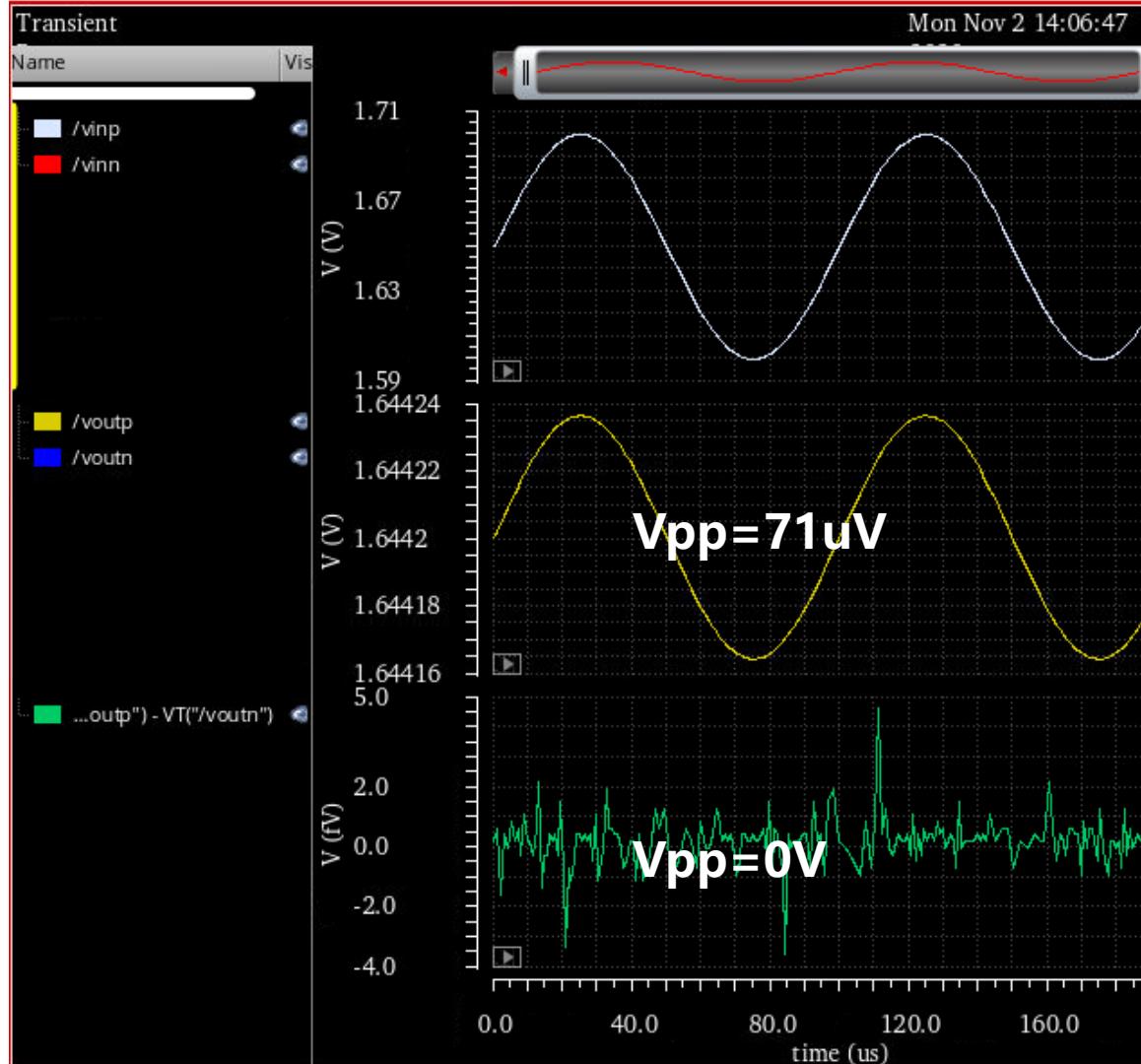
$$V_{out} = -\frac{10 \cdot A}{A + 11} \cdot V_{in} = -8.2 \times V_{in}$$



- 输入：差分100mV
- 由于有限的增益，导致运放的输入端无法实现“虚短”的特性，出现了20mV的输入
- 由于有限的增益，运放无法按电阻的比例进行放大



- 输入：共模100mV
- 由于电路的全对称结构，因此没有系统性失调的存在，差分输出约等于0
- 输出的共模变化为71uV，由于共模反馈环路的存在，共模输入/共模输出的CMRR从原来的18dB增加到57dB，增加量即为共模反馈的环路增益（39dB）



Homework 6

Solution 2: Using Weak Inversion

电路图过于老旧，其架构不适合我们工艺所要求的1.8V电源电压

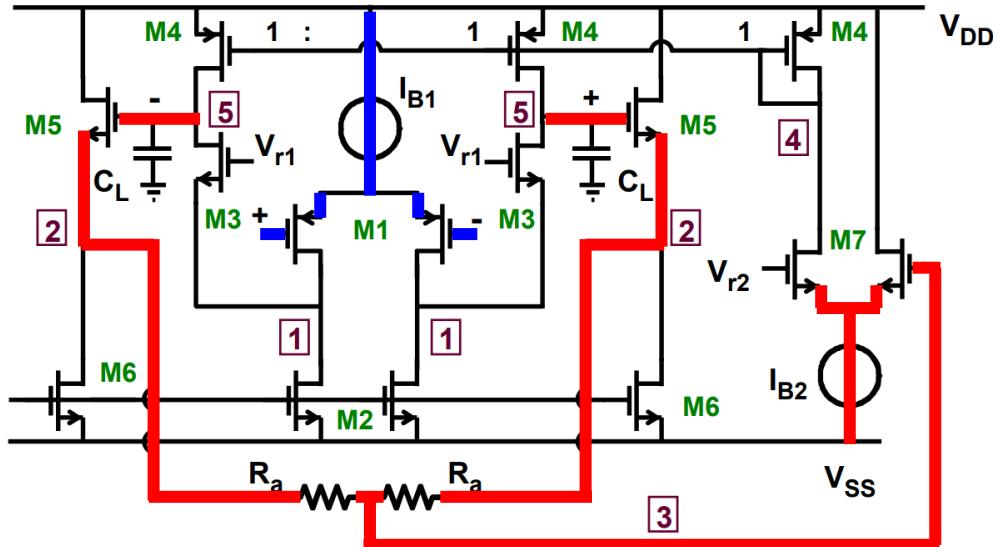
$$V_{OUT} - V_{GS5} = V_{r2}$$

$$V_{r2} - V_{GS7} > V_{DSat}$$

$$V_{OUT} + V_{GS1} < V_{DD} - V_{DSat}$$

$$V_{GS5} + V_{GS7} + V_{DSat} < V_{OUT} < V_{DD} - V_{DSat} - V_{GS1}$$

假设 $V_{GS} = 0.3V$, $V_{DSat} = 0.1V \rightarrow 0.7V < V_{OUT} < 1.4V$



- $\text{GBW}_{DM} = 50\text{MHz}$, $C_L = 5\text{pF}$

$$GBW_{DM} = \frac{g_{m1}}{2\pi C_L}$$

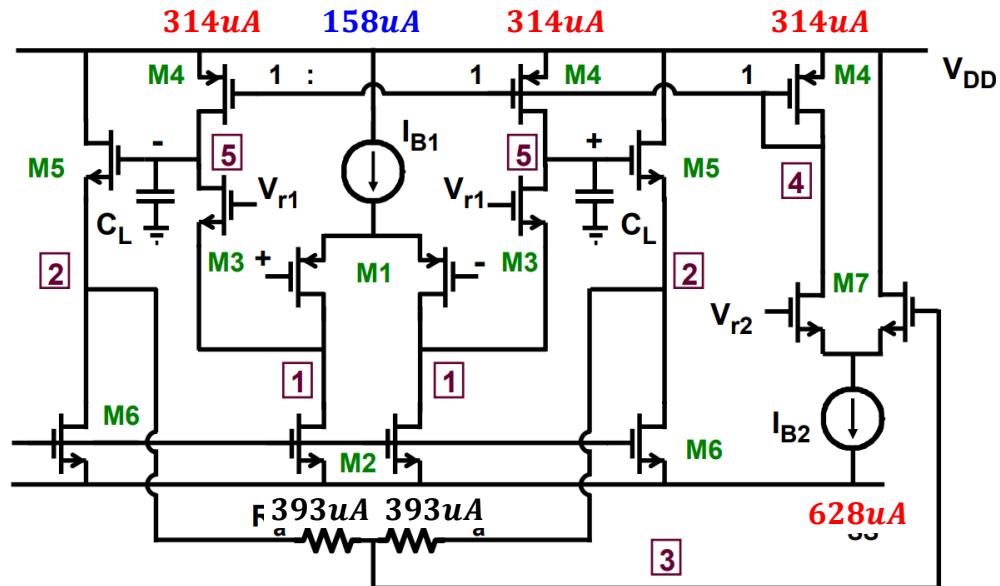
$$g_{m1} = GBW_{DM} \cdot 2\pi C_L = 1.57\text{mA/V}$$

$$g_{m7} = GBW_{CM} \cdot 4\pi C_L = 6.28\text{mA/V}$$

合理假设 $g_m/I_D = 20$

$$I_{D1} = 79\mu\text{A}$$

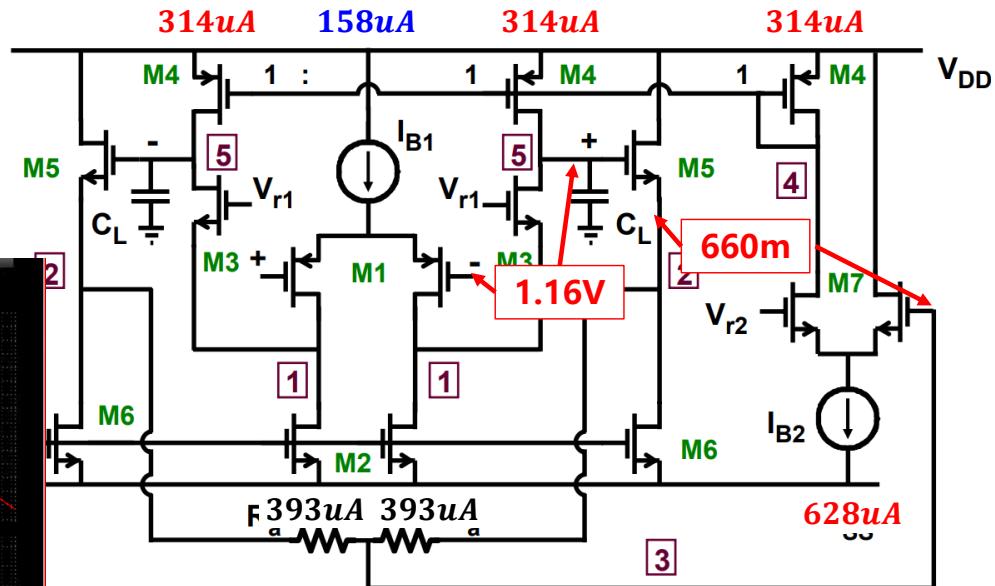
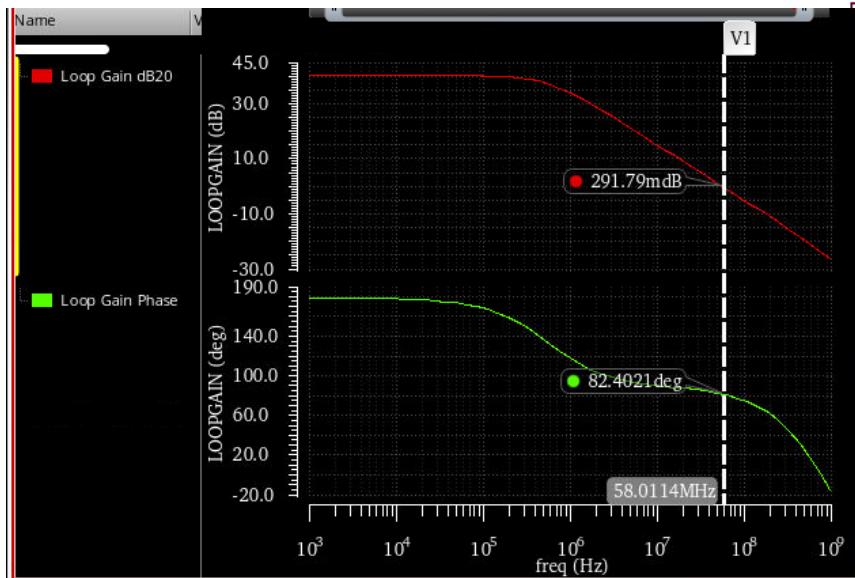
$$I_{D7} = 314\mu\text{A}$$



晶体管	M1	M2	M3	M4	M5	M6	M7
尺寸(um)	?	35/0.5	56/0.5	56/0.5	?	10/0.5	?

仿真得到：

- GBW_{DM} = 58M
- PM = 82



晶体管	M1	M2	M3	M4	M5	M6	M7
尺寸(um)	224/0.2	35/0.5	56/0.5	56/0.5	144/0.18	10/0.5	224/0.2

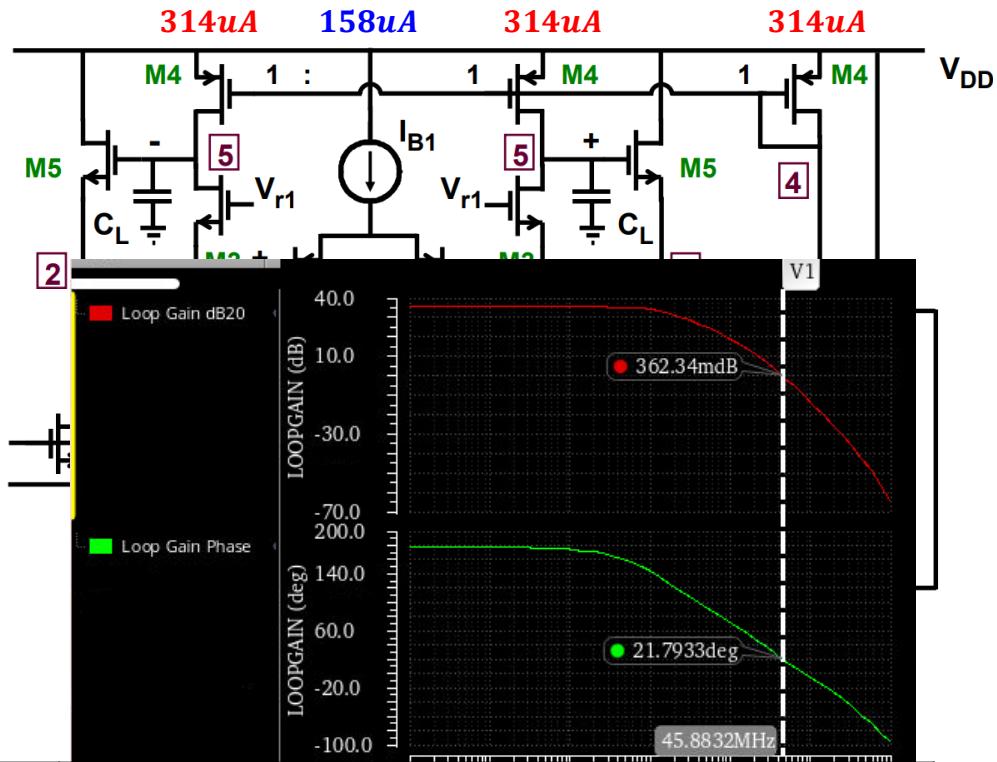
仿真得到：

- **GBW_{CM}=48M**
 - **PM=22**

显然次极点出现导致GBW不足以及PM过小。

通过同样的分析，发现Net4的极点在800M，Net3的极点在38M。

因此需要：1.减小 R_a 的阻值；2.增加 g_{m5} 的值；3.增加 I_5 以增加驱动能力



课后习题

- 将上述设计的差分运放，通过电阻设置成10倍放大，观察输入差模和共模信号分别有100mVpp, 10kHz的正弦信号时，差模输出信号的大小，并分析是否符合预期。

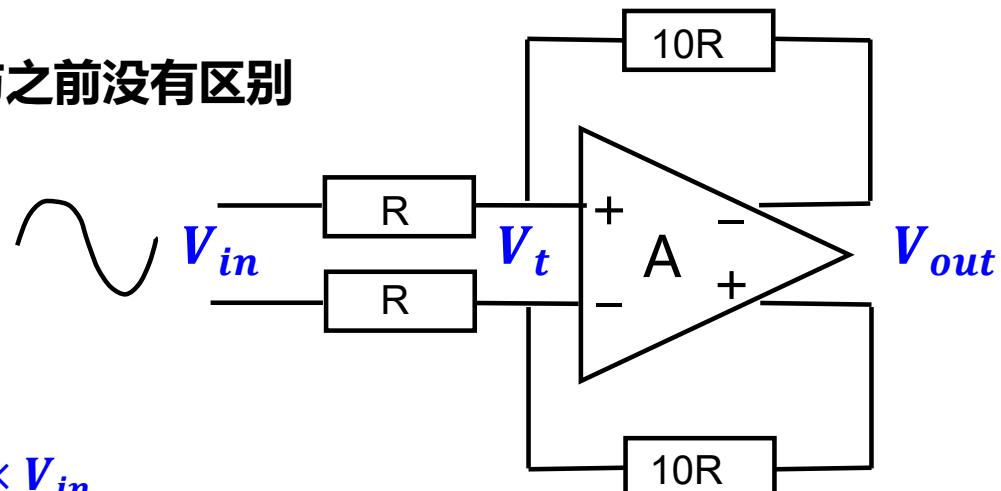
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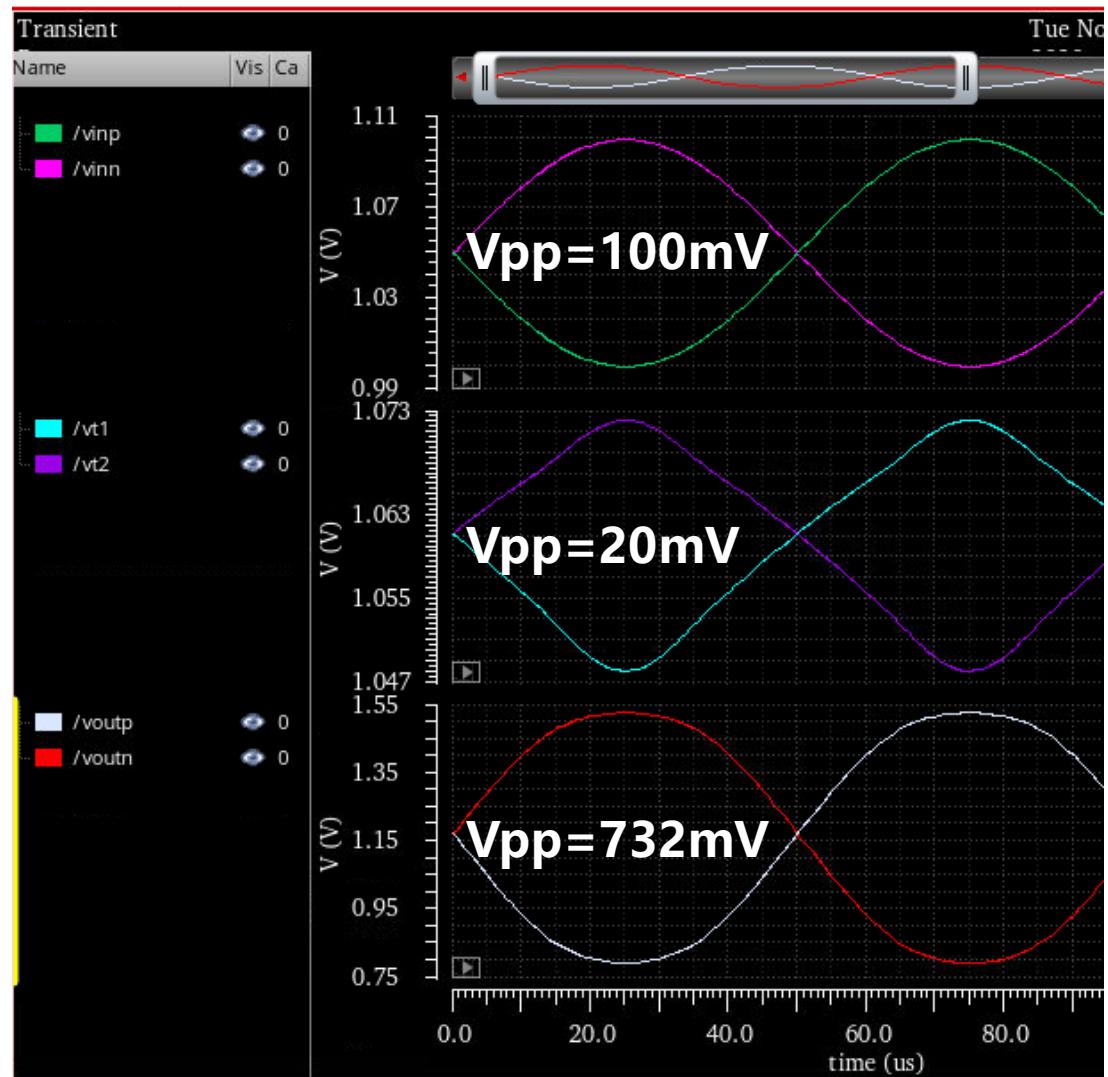
与之前没有区别

$$\left\{ \begin{array}{l} \frac{V_{out} - V_t}{10R} = \frac{V_t - V_{in}}{R} \\ V_{out} = -A \cdot V_t \end{array} \right.$$

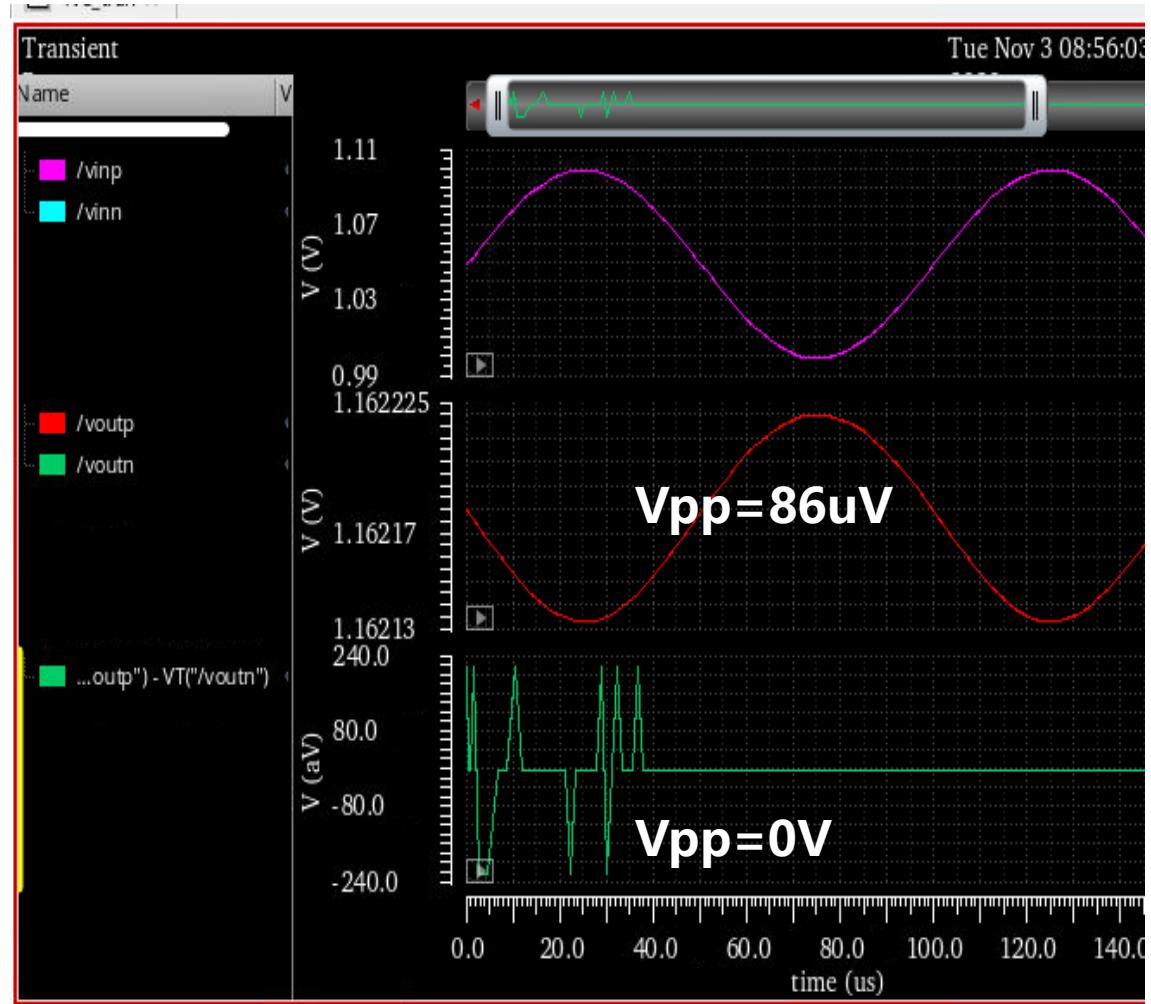
$$V_{out} = -\frac{10 \cdot A}{A + 11} \cdot V_{in} = -8.2 \times V_{in}$$



- 输入：差分100mV
- 由于驱动力以及电压裕度的不足，输出信号出现了明显的失真



- 输入：共模100mV
- 由于电路的全对称结构，因此没有系统性失调的存在，差分输出约等于0
- 输出的共模变化为86uV，由于共模反馈环路的存在，共模输入/共模输出的CMRR表现优异。



Homework 6

Solution 3: Using different circuit configuration

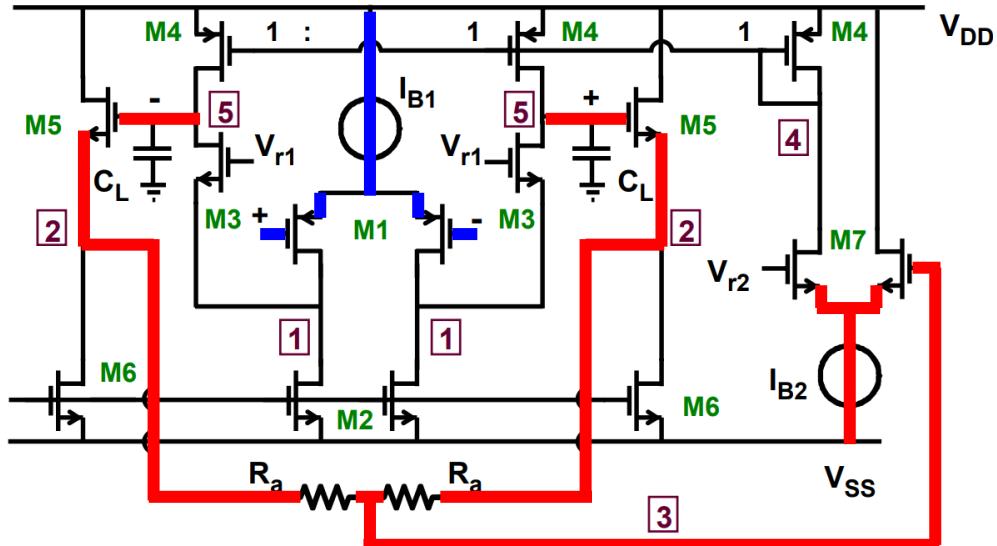
电路图过于老旧，其架构不适合我们工艺所要求的1.8V电源电压

$$V_{OUT} - V_{GS5} = V_{r2}$$

$$V_{r2} - V_{GS7} > V_{DSat}$$

$$V_{OUT} + V_{GS1} < V_{DD} - V_{DSat}$$

$$V_{GS5} + V_{GS7} + V_{DSat} < V_{OUT} < V_{DD} - V_{DSat} - V_{GS1}$$



✓ 我们可以在共模反馈回路中使用PMOS差分对！

采用PMOS后，电路的静态工作区间要求变成了：

$$V_{OUT} - V_{GS5} = V_{r2} > V_{DSat}$$

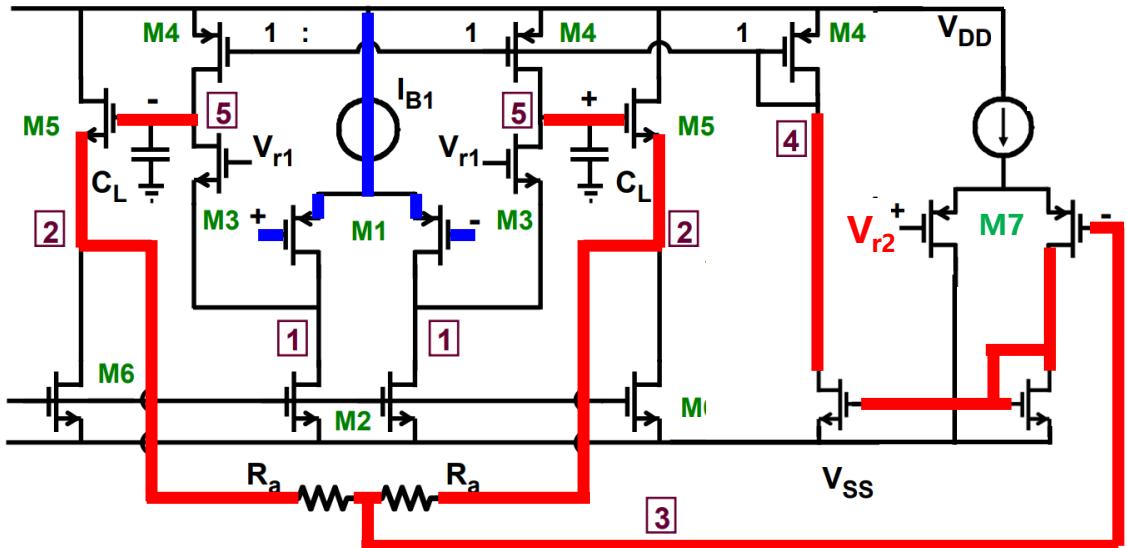
$$V_{r2} < V_{DD} - V_{DSat} - V_{GS7}$$

$$V_{OUT} + V_{GS1} < V_{DD} - V_{DSat}$$

$$\begin{cases} V_{OUT} < V_{DD} - V_{DSat} - V_{GS1} \\ V_{GS5} + V_{DSat} < V_{OUT} < V_{DD} - V_{DSat} + V_{GS5} - V_{GS7} \end{cases}$$

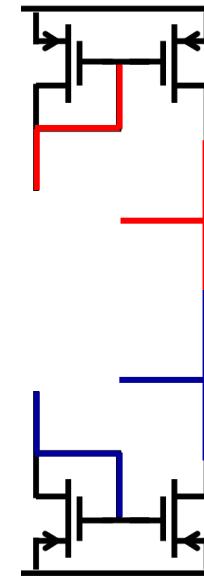
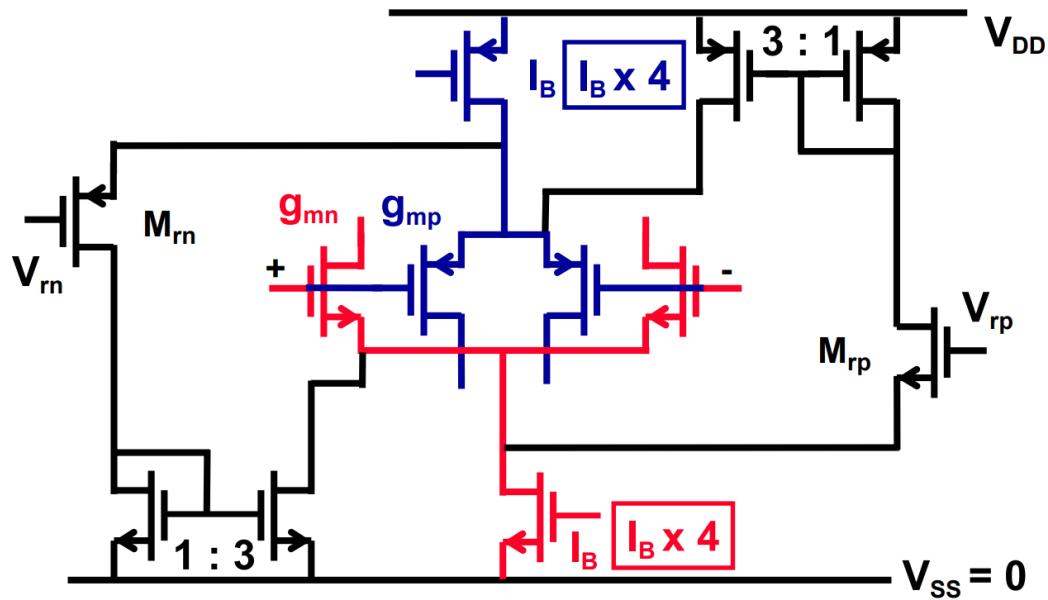
$$V_{GS5} + V_{DSat} < V_{OUT} < V_{DD} - V_{DSat} - V_{GS1}$$

✓ 输出范围增大了一个 V_{GS}



Homework 7

- 设计一轨到轨输入的单级运放，要求指标：
 - $V_{DD} = 1.8V$
 - $GBW = 100MHz, C_L = 10pF, PM = 60$
- 因为 GBW 较高，采用强反型区，因此使用下图电路：
- 单级运放，采用最简单的电流镜有源负载



第 16 章 HW07

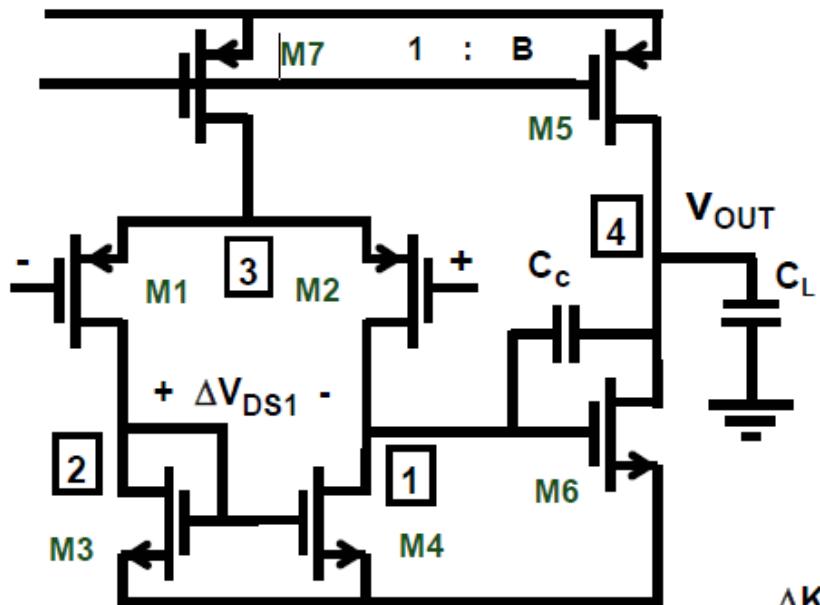
Homework 7



课后作业

- 设计一轨到轨输入运放，要求指标：
 - $V_{DD} = 1.8V$
 - $GBW = 100MHz, C_L = 10pF$
- 完成设计后给出以下参数：
 - PM?
 - FOM?
 - 0.4V-1.4V区间内的系统失调电压
 - 0.4V-1.4V区间内的GBW偏差

- 0.4V-1.4V区间内的系统失调电压



$$A_{v1} = g_{m1} r_{o2} // r_{o4}$$

$$v_{OS} = \frac{\Delta V_{DS1}}{A_{v1}}$$

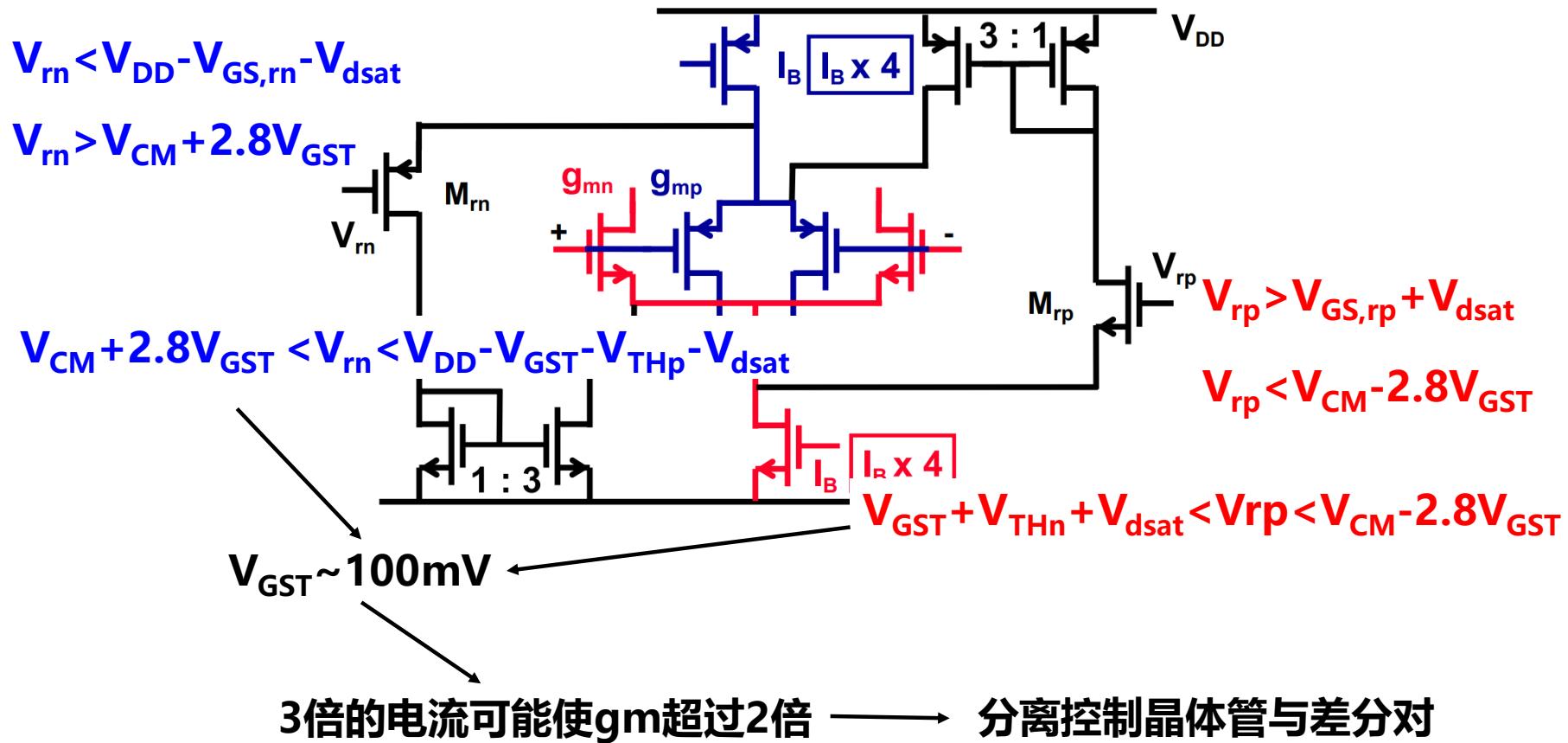
$$\Delta V_{T1} + \frac{g_{m3}}{g_{m1}} \Delta V_{T3}^* +$$

$$+ \frac{V_{GS1} - V_T}{2} S$$

$$S = \frac{\Delta K'_n}{K'_n} + \frac{\Delta K'_p}{K'_p} + \frac{\Delta W/L_1}{W/L_1} + \frac{\Delta W/L_3}{W/L_3}$$

- 系统性失调由电流镜两边晶体管 V_{DS} 的不同造成
- 对于1.4V和0.4V的 V_{DS} 进行优化
- 可以通过提升增益减小 v_{OS}

- 0.4V-1.4V区间内的GBW偏差



- 设计一轨到轨输入的单级运放，要求指标：

- $V_{DD} = 1.8V$
- $GBW = 100MHz, C_L = 10pF, PM = 60$

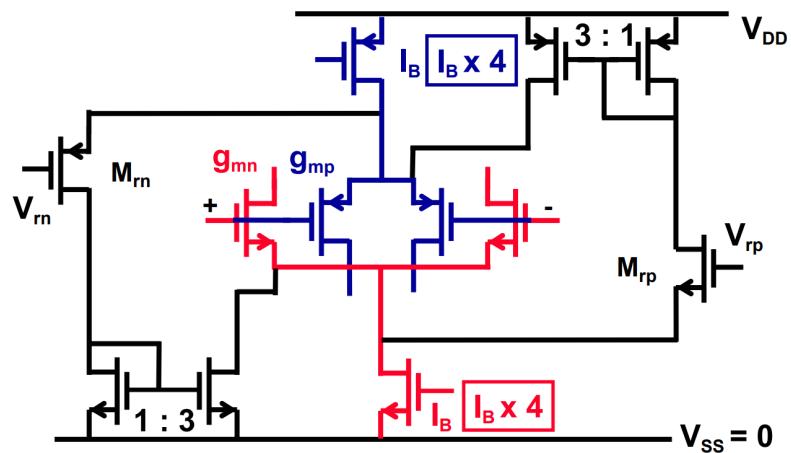
$$g_m = GBW \cdot 2\pi \cdot C_L = \\ 75M \cdot 6.28 \cdot 10p = 4.71mA/V$$

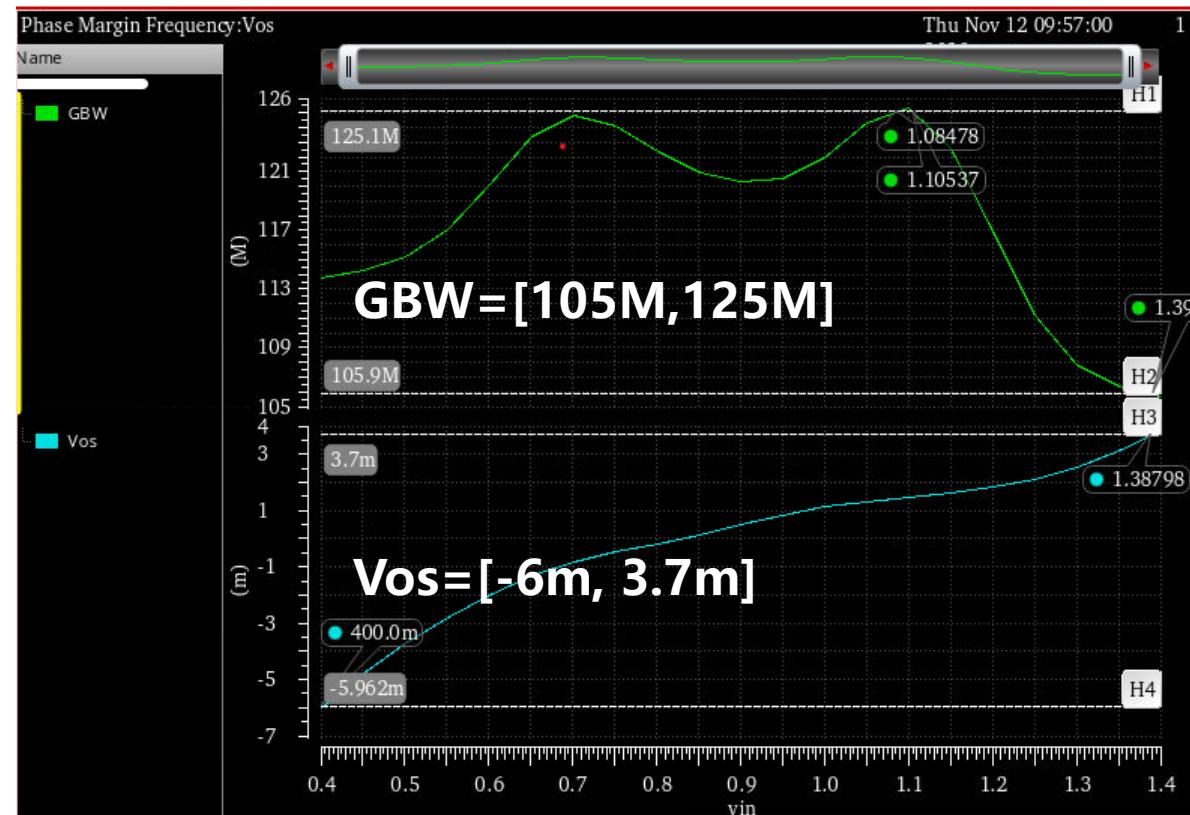
$$I_D = \frac{g_m}{10} = 480\mu A$$

$$\left(\frac{W}{L}\right)_n = \frac{150\mu}{1\mu} \quad \quad \quad \left(\frac{W}{L}\right)_p = \frac{300\mu}{0.5\mu}$$

- 增大 M_{rn} 和 M_{rp} 的宽长比，不妨设：

$$\left(\frac{W}{L}\right)_{rn} = \frac{150\mu}{0.2\mu} \quad \quad \quad \left(\frac{W}{L}\right)_{rp} = \frac{600\mu}{0.2\mu}$$





作业中出现的问题：

- GBW的设计只满足 $>100M$, 没有做到平衡
- 通过改变电流镜比例来克服线性区的问题欠妥
- 只使用最小长度, 导致 V_{os} 变化偏大
- FOM的计算没有囊括所有电流

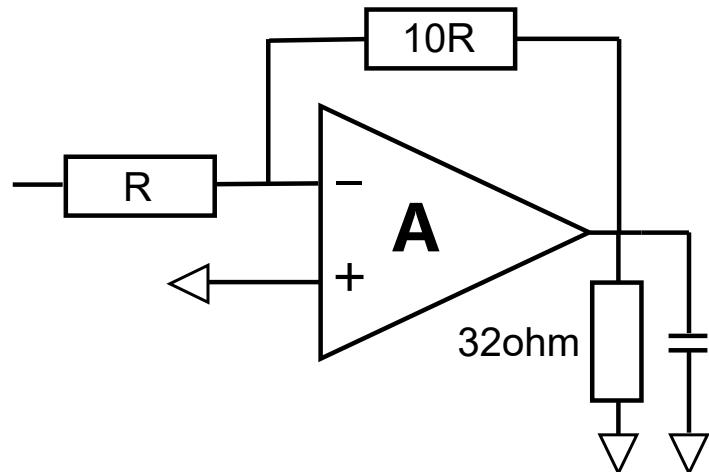
$$FOM = 120M * 10p / 3.25m = 369 \text{ MHz}\cdot\text{pF}/\text{mA}$$

第 17 章 HW08

Homework 8

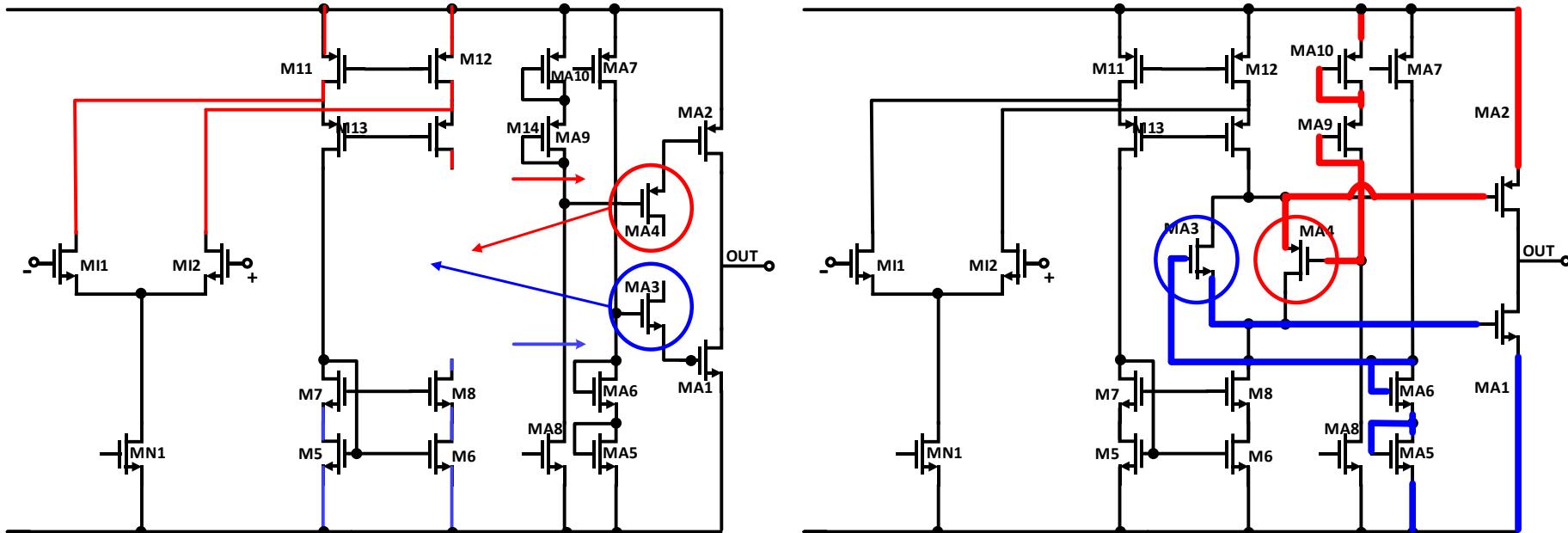
- 设计一个线性跨导回路的Class-AB运放，其中：
 - $V_{DD} = 1.8V$, $V_{SS} = 0V$, $V_{CM} = 0.9V$
 - $C_L = 10pF$, $R_L = 32\text{ohm}$
 - 差模输入 $V_{pp} = 100\text{mV}$, 输入频率200kHz, 放大倍数10

- 要求指标：
 - 要求输出正弦波峰-峰值大于950mV
 - 运放静态功耗小于1.5mA



》》 线性跨导回路：输出级增益

- 可以将偏置晶体管M3A和M4A并联，使其各自的电流动态调整



- 思路：

1. 根据x10的放大倍数和下式，确定所需的DC增益

$$V_{out} = -\frac{10 \cdot A_0}{A_0 + 11} \cdot V_{in}$$

- 根据公式，DC增益至少需要210，按照**1000**设计比较保险

2. 根据x10的放大倍数和输入频率估计GBW

- GBW最低要求为 $10 \cdot 200K = 2M$ ，按照**10M**进行设计

3. 根据所需要的输出电流预估线性跨导回路尺寸和偏置

- 按照1Vpp的输出电压，峰值电流需要 $0.5/32 = 15mA$

- 峰值输出时， $V_{DS} = 0.4V$ ，因此峰值下 $V_{GS} < 0.4 + V_{TH}$

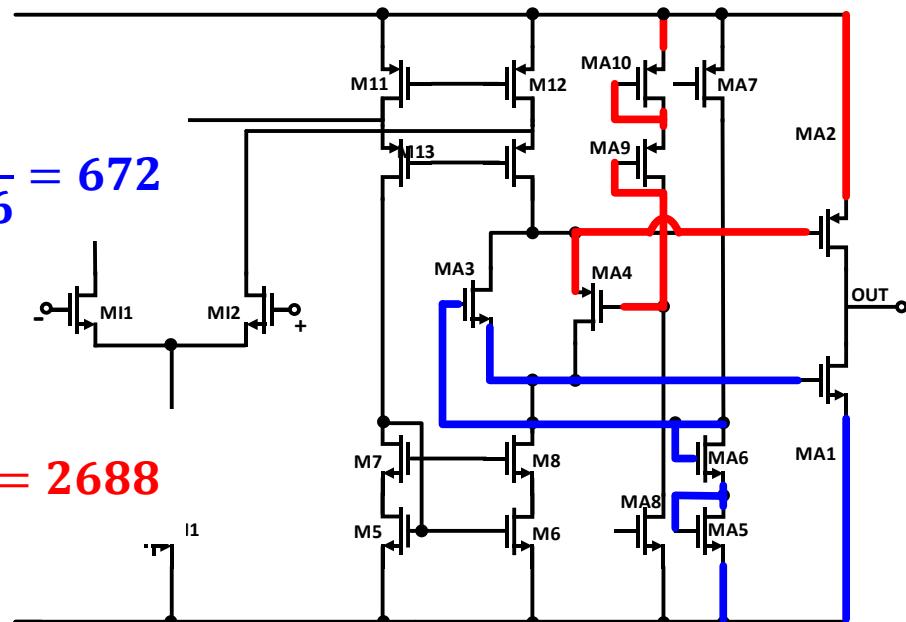
- 根据所需要的输出电流预估线性跨导回路尺寸和偏置
 - 峰值输出时, $V_{DS}=0.4V$, 因此尺寸设计按照 $V_{GST}=0.4V$

$$I_{D,A1} = 15mA$$

$$\left(\frac{W}{L}\right)_{A1} = \frac{2I_D}{KP_N \cdot (V_{GS} - V_{TH})^2} = \frac{2 \cdot 15m}{280u \cdot 0.16} = 672$$

$$I_{D,A2} = 15mA$$

$$\left(\frac{W}{L}\right)_{A2} = \frac{2I_D}{KP_P \cdot (V_{GS} - V_{TH})^2} = \frac{2 \cdot 15m}{70u \cdot 0.16} = 2688$$



- 根据x10的放大倍数和输入频率估计GBW
 - GBW最低要求为 $10 \times 200\text{K} = 2\text{M}$, 按照10M进行设计; $C_L = 10\text{pF}$

$$f_{nd} = 3 \cdot GBW = 30\text{MHz}$$

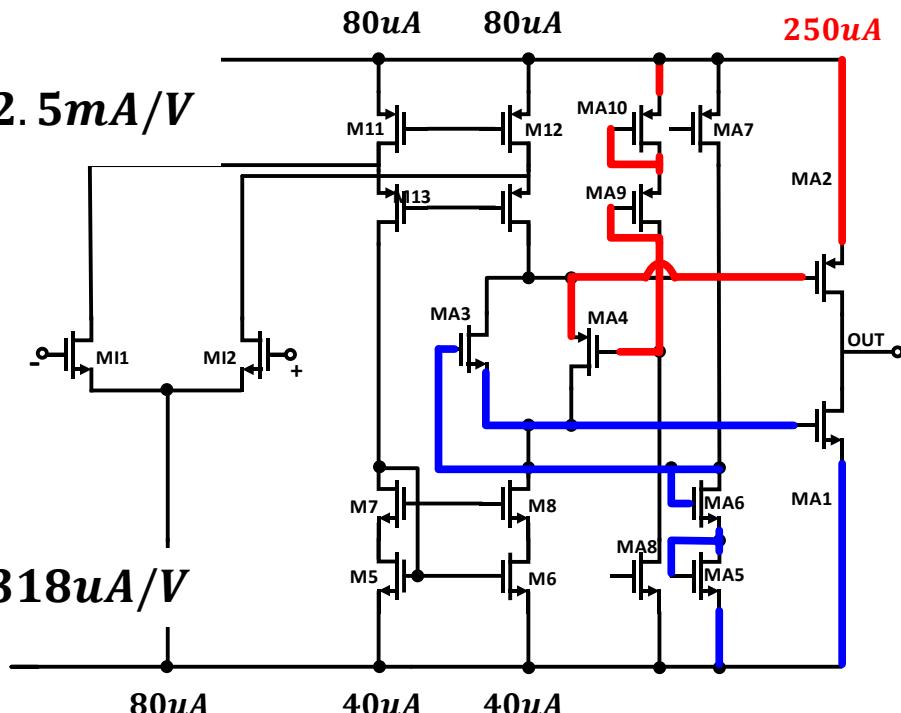
$$g_{m,A1/2} = \frac{4}{3} f_{nd} \cdot 2\pi C_L = 40M * 62.8p = 2.5mA/V$$

$$I_{dDC,A1/2} = 250\mu A$$

- 静态电流是峰值电流的1/60
- 在此情况下 $V_{GST} = 50\text{mV}$, 晶体管开始趋于弱反型区

$$g_{m,I1/2} = GBW \cdot 2\pi C_C = 10M * 31.8p = 318\mu A/V$$

$$I_{dDC,I1/2} = 40\mu A$$



- 根据x10的放大倍数和输入频率估计GBW
 - GBW最低要求为 $10 \times 200\text{K} = 2\text{M}$, 按照10M进行设计; $C_L = 10\text{pF}$

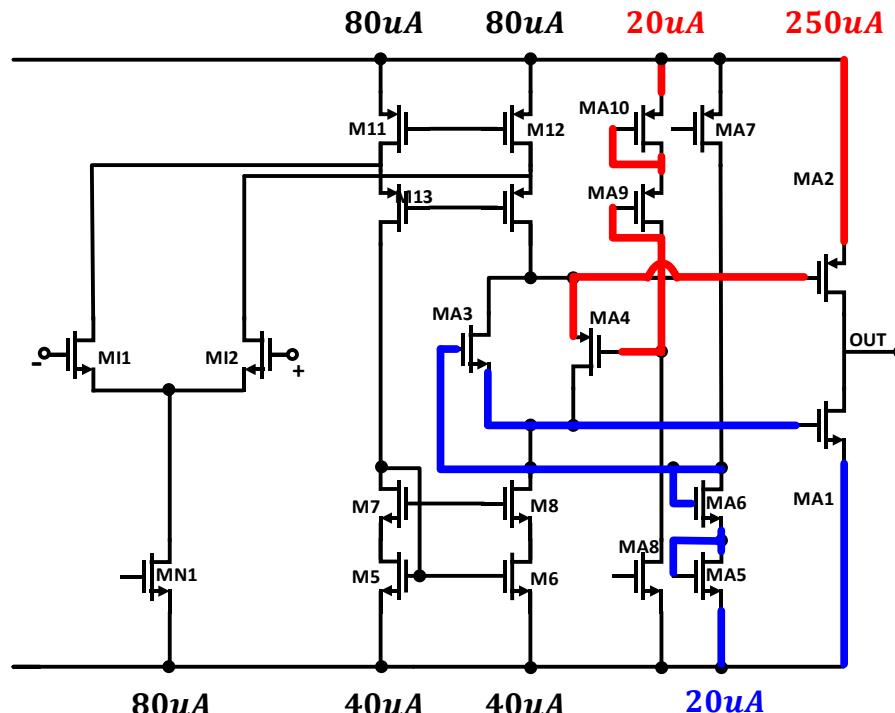
- 假设 M_{A4} 的尺寸是 $M_{A9/10}$ 的两倍,
 $I_{DS9} = I_{DS4}$, 则有电流关系:

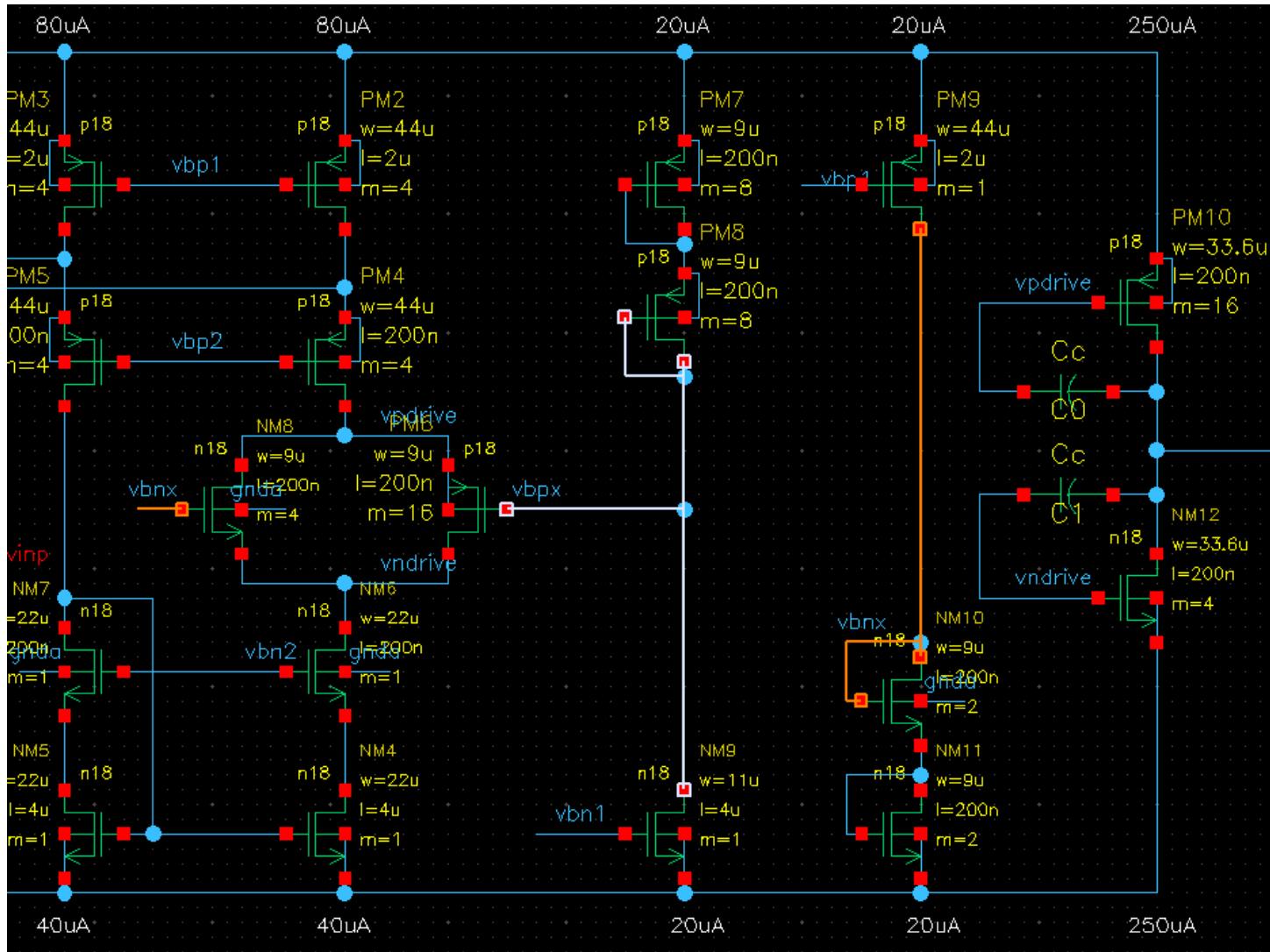
$$\frac{I_{DS2}}{I_{DS9}} = \frac{W/L_2}{W/L_9} \left(2 - \frac{1}{\sqrt{2}}\right)^2$$

- 令 M_{A3} 和 M_{A4} 平分40uA电流, 则可求得 M_{A5-10} 的尺寸:

$$\left(\frac{W}{L}\right)_{A5/6} = 90 \quad \left(\frac{W}{L}\right)_{A9/10} = 360$$

$$\left(\frac{W}{L}\right)_{A3} = 180 \quad \left(\frac{W}{L}\right)_{A4} = 720$$

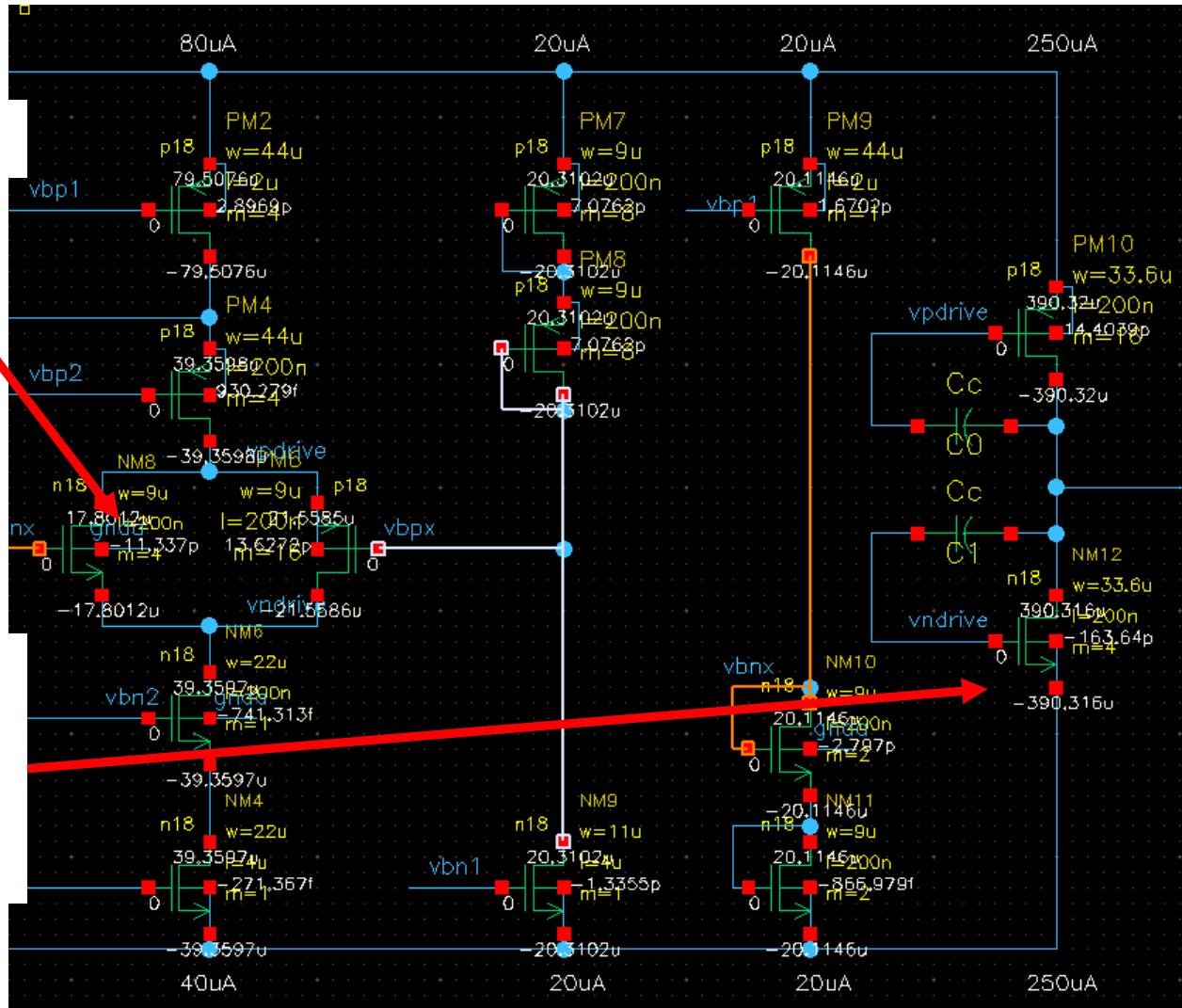




- DC电流偏置基本正确!

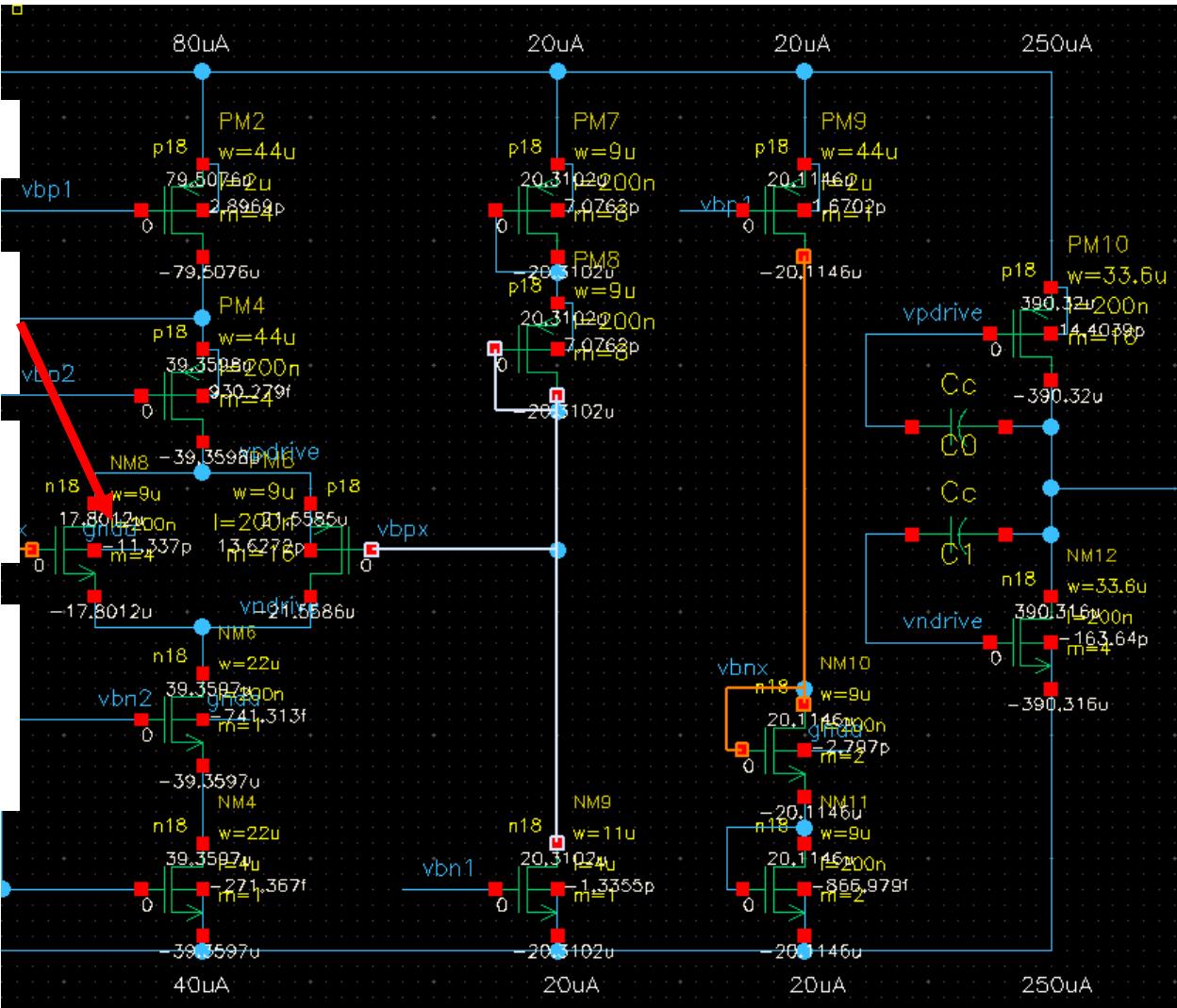
- P-N电流基本平衡

- 输出级静态电流比设计大50%，主要由于二次项的关系在接近弱反型区后不在成立



• P-N偏置电流调整思路

- 从NMOS通过的电流较小，意味着：
- 电路需要更小的 V_{GSn} 才能使得P-N达到平衡
- 增加(W/L)_n即可在较大的电流下提供更小的 V_{GSn}



- 增加(W/L)_n: 从原来的36u/0.2u增加至48u/0.2u
- P-N电流基本上平衡
- 输出级电流也会有所变化

