Systematic Design of Operational Amplifiers

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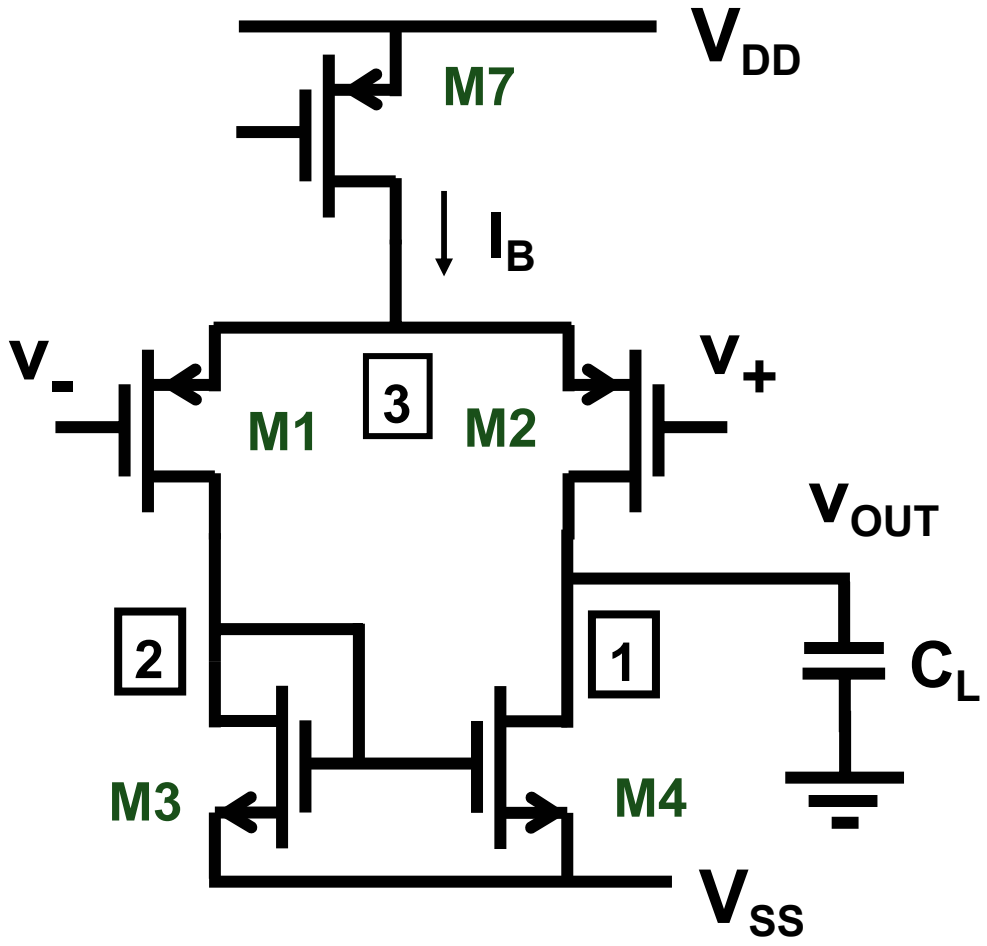
Ref.: Sansen : Analog design essentials, Springer 2006

Single-stage CMOS OTA : GBW



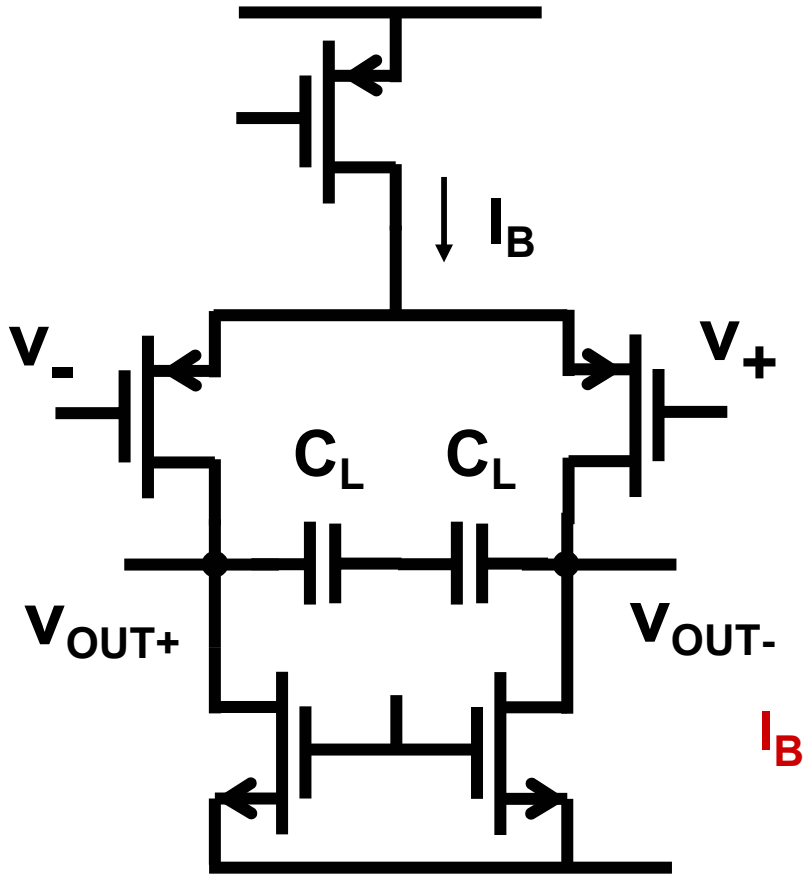
$$A_v = g_{m1} \frac{r_o}{2}$$

if $r_{o2} = r_{o4} = r_o$

$$BW = \frac{1}{2\pi \frac{r_o}{2} (C_L + C_{n1})}$$

$$GBW = \frac{g_{m1}}{2\pi (C_L + C_{n1})}$$

CMOS OTA : Maximum GBW



$$GBW = \frac{g_{m1}}{2\pi C_L} \qquad g_{m1} = \frac{I_B}{V_{GS1}-V_T}$$

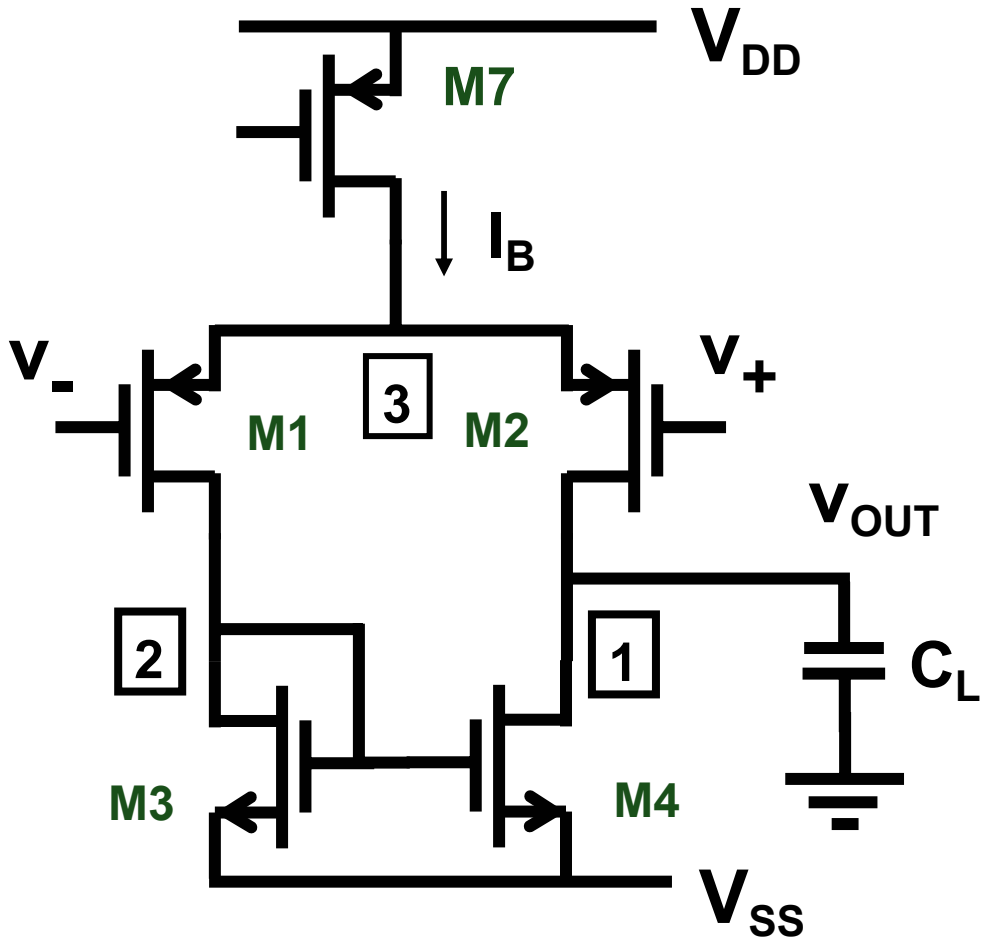
$$GBW_{max} = \frac{I_B}{V_{GS1}-V_T}\,\frac{1}{2\pi C_L}$$

0.2 V

$I_B = 10\ \mu A \quad C_L = 1\ pF \quad GBW_{max} \approx 10\ MHz$ [8]

$$FOM = \frac{GBW.C_L}{I_B} = 1000\ \text{MHzpF/mA} \quad [800]$$

Single stage CMOS OTA : f_{nd}



$$GBW = \frac{g_{m1}}{2\pi\,(C_L + C_{n1})}$$

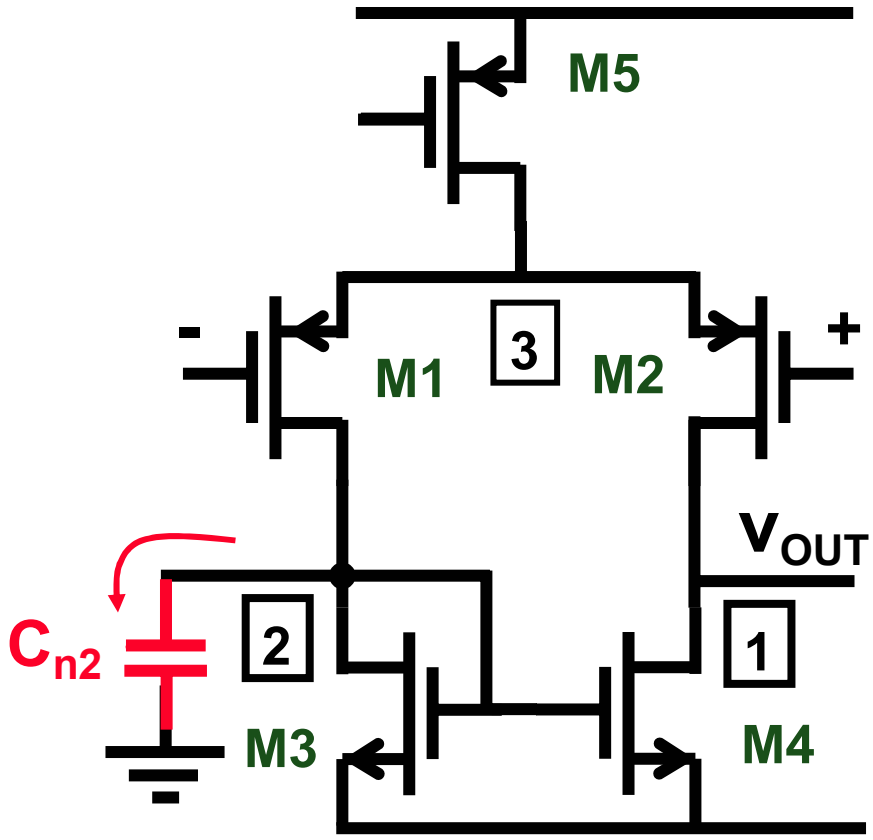
$$f_{nd} = \frac{g_{m3}}{2\pi\,C_{n2}}$$

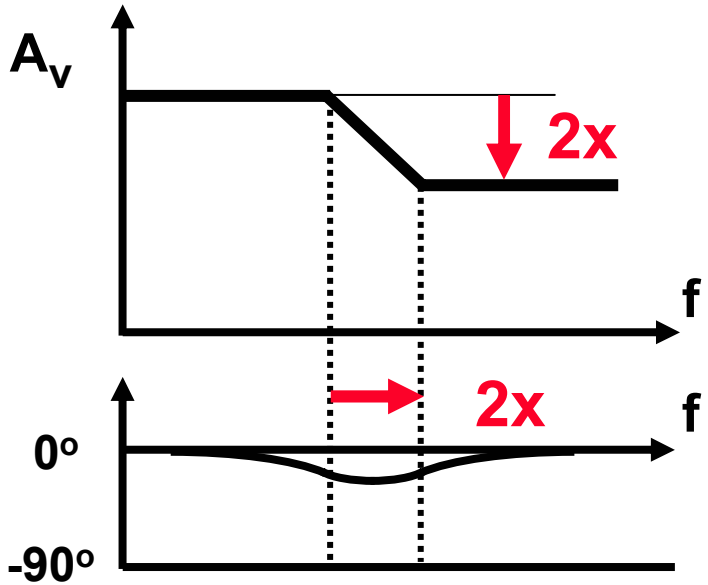
$$C_{n2} \approx 2C_{GS3} + C_{DB3} + C_{DB1}$$

$$\approx 4\,C_{GS3}$$

$$f_{nd} \approx \frac{f_{T3}}{4}$$

Simple CMOS OTA : f_{nd}





$$f_{nd} = \frac{g_{m3}}{2\pi C_{n2}}$$

$$PM = 90^o - \arctan\frac{GBW}{f_{nd}} + \arctan\frac{GBW}{2\,f_{nd}} \approx 85^o$$

Single stage CMOS OTA : Design 1

GBW = 100 MHz for C_L = 2 pF

Techno: L_{min} = 0.35 μm; K'_n = 60 μA/V² & K'_p = 30 μA/V²

I_{DS} ? W ? L ?

$$g_m = GBW\ 2\pi\ C_L = 1.2\ mS$$

$$V_{GS}\text{-}V_T = 0.2\ V \qquad I_{DS} = g_m \frac{V_{GS}\text{-}V_T}{2} = \frac{g_m}{10} = 0.12\ mA$$

$$\frac{W}{L} = \frac{I_{DS}}{K'(V_{GS}\text{-}V_T)^2} = 100$$

$L_p = L_n = 1\ \mu m$ **GAIN !**

$W_p = 100\ \mu m;\ W_n = 50\ \mu m$

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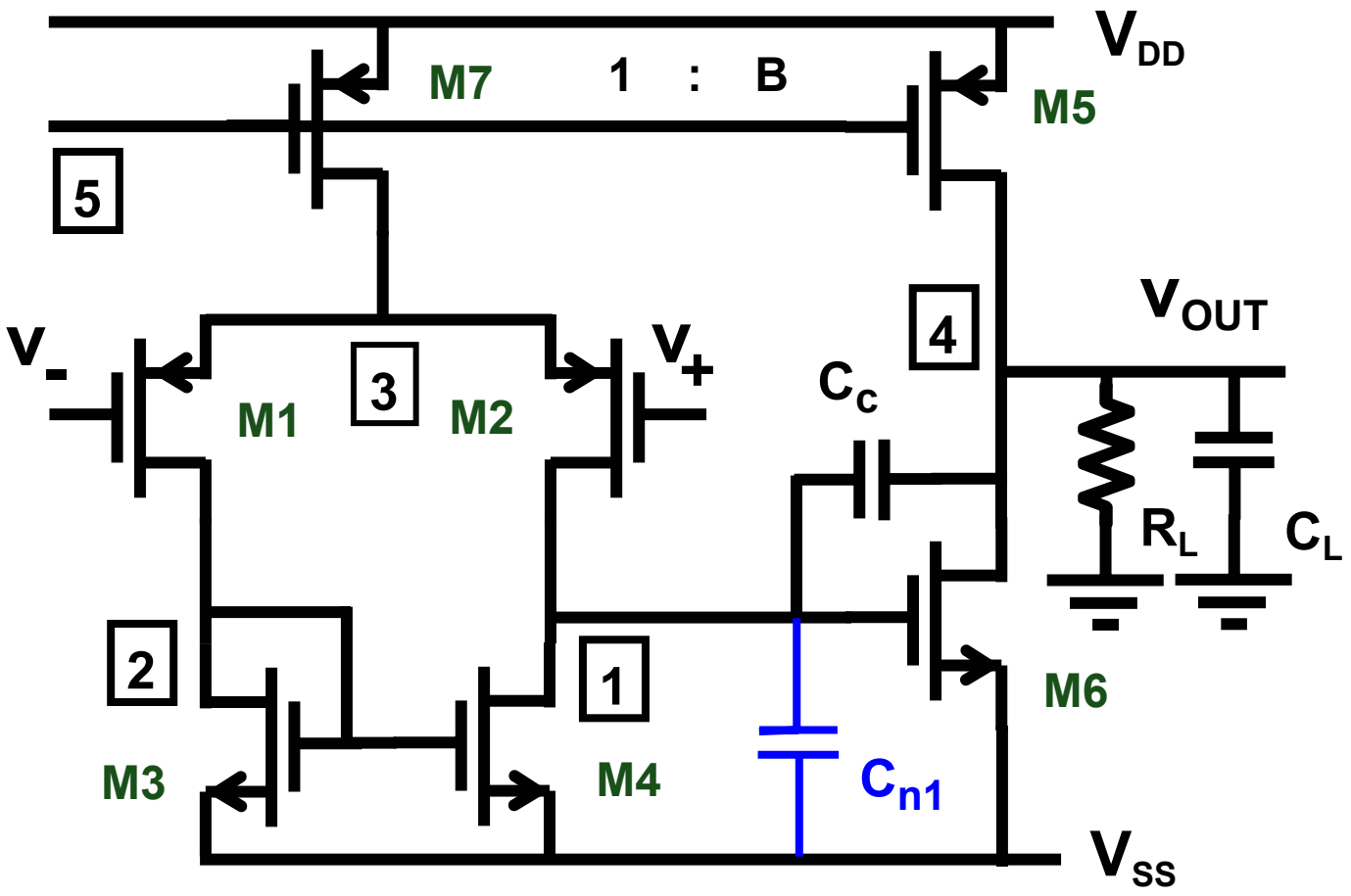
Miller CMOS OTA



Two nodes

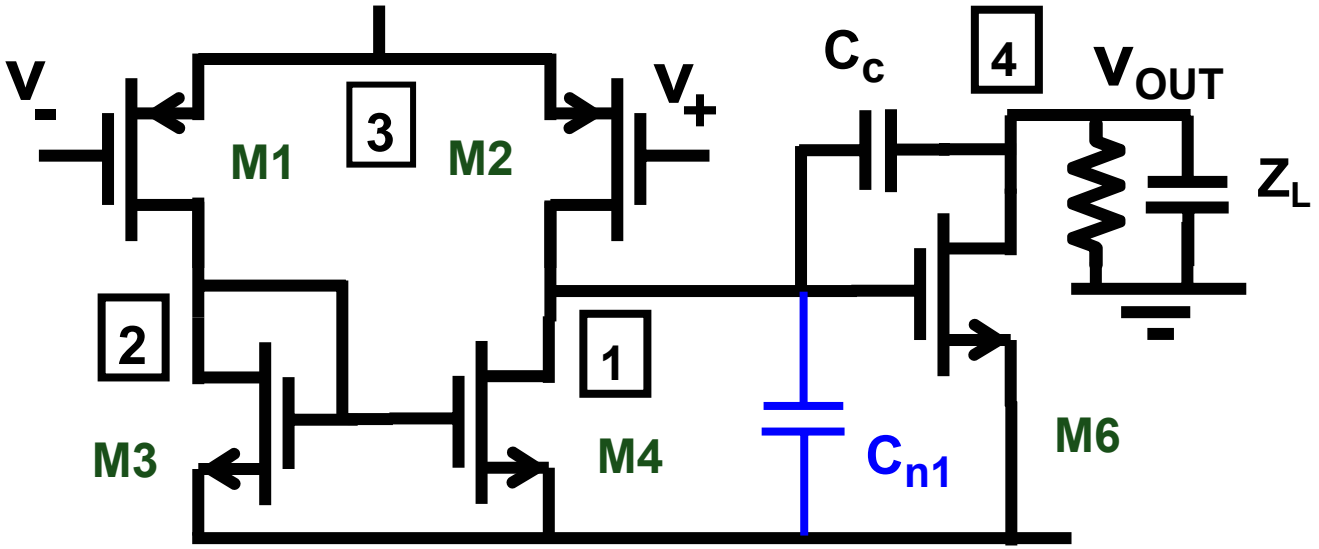
1 4

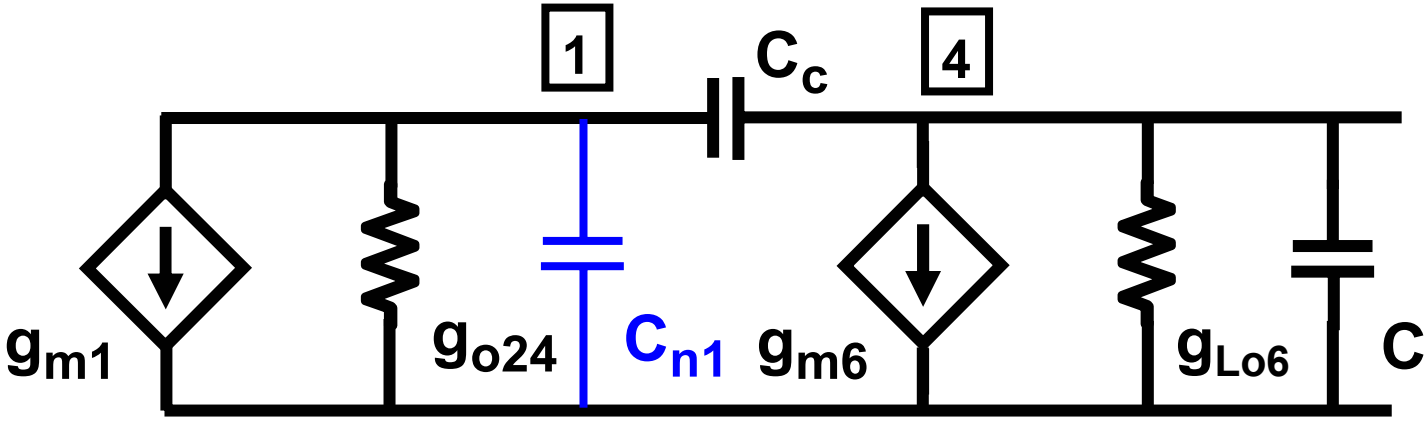
with high Impedance

cause two poles

split by C_c

Miller CMOS OTA : small-signal





GBW= 1MHz

C_L = 10 pF

R_L = 10 kΩ

g_{m1} = 7.5 μS

g_{o24} = 0.03 μS

C_{n1} = 0.37 pF

C_c = 1 pF

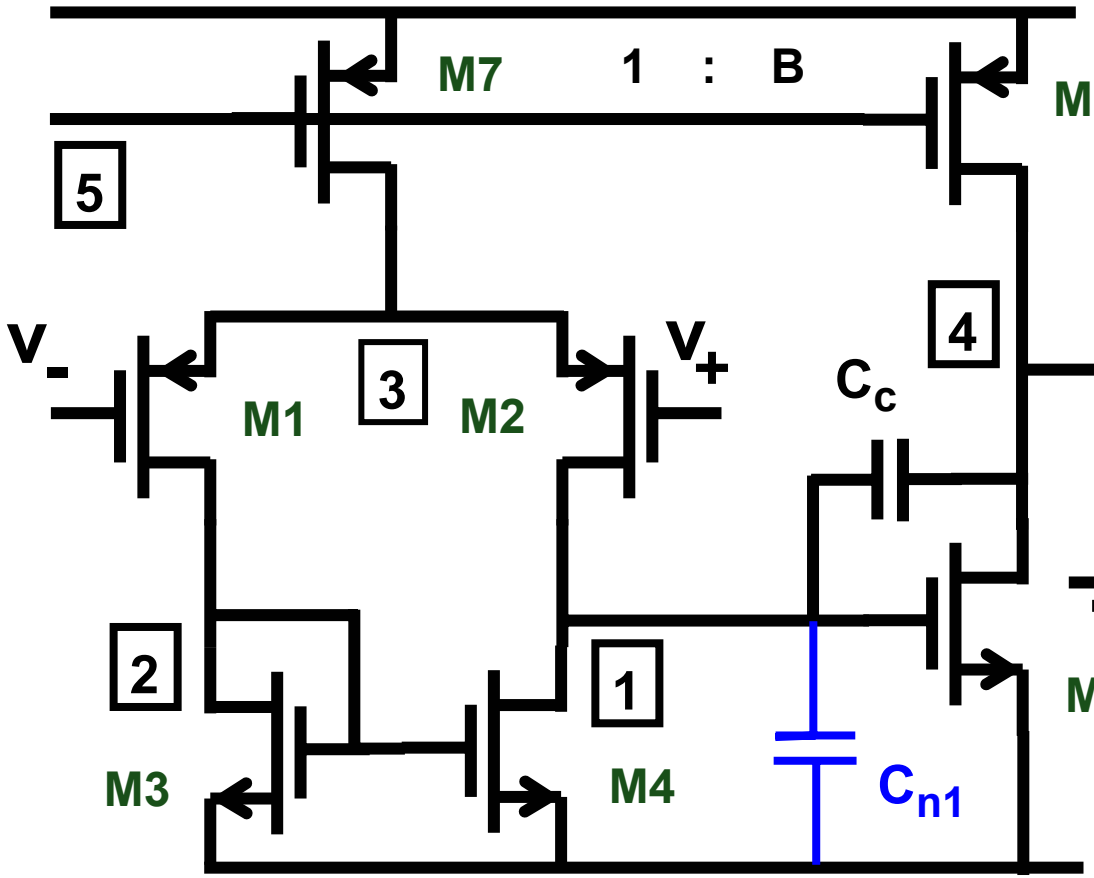
g_{m6} = 246 μS

g_{Lo6} = 120 μS

I_{DS1} = 1.1 μA

I_{DS6} = 25 μA

Miller CMOS OTA : GBW



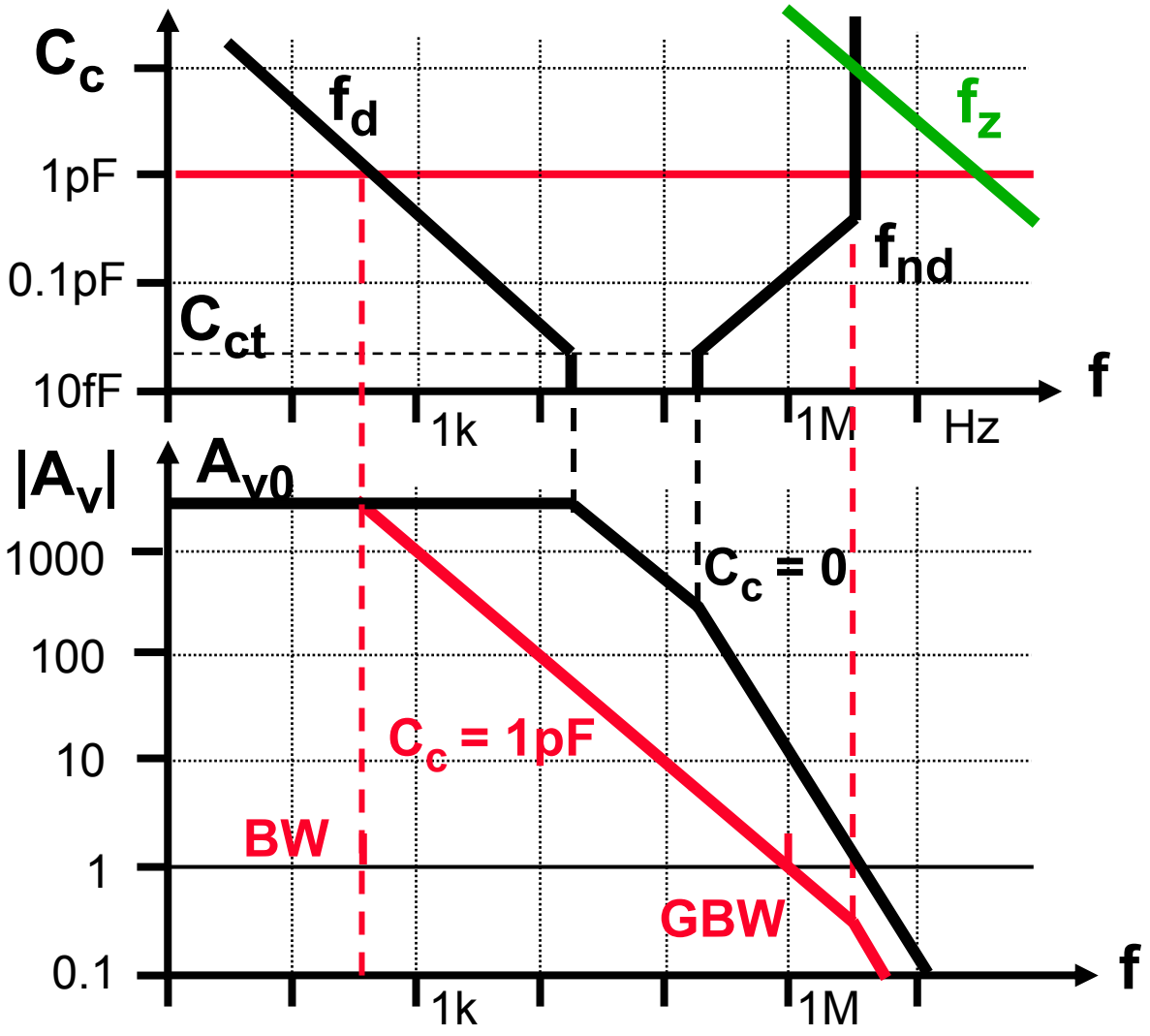
$$A_{v1} = \frac{g_{m1}}{g_{o24}} \qquad A_{v2} = \frac{g_{m6}}{g_{Lo6}}$$

$$BW = \frac{g_{o24}}{2\pi A_{v2} C_c}$$

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} \approx \frac{g_{m6}}{2\pi C_{Ln4}} \frac{1}{1+\frac{C_{n1}}{C_c}}$$

Miller CMOS OTA : poles and zero



Pole splitting starts at

$$C_{ct} \approx \frac{C_{n1}}{A_{v2}} \approx 20\ fF$$

but is sufficient for $C_c = 1pF$

$$f_z = \frac{g_{m6}}{2\pi C_c}$$

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- Other specs: Input range, output range, SR, ...

Miller CMOS OTA: Design plan

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

GBW = 100 MHz and C_L = 2 pF

$$f_{nd} \approx \frac{g_{m6}}{2\pi C_{Ln4}} \frac{1}{1+\frac{C_{n1}}{C_c}}$$

Two equations for

Three variables g_{m1}, g_{m6} and C_c ?!?

Solution : choose g_{m1} or g_{m6} or C_c !!!

What is wrong with

choosing $C_c = 1$ pF ?

Miller CMOS OTA: Design vs C_c

Choose $C_c \approx 3\, C_{n1}$ GBW = $\frac{g_{m1}}{2\pi\, C_c}$

$$3GBW \approx \frac{g_{m6}}{2\pi\, C_{Ln4}} \frac{1}{1.3}$$

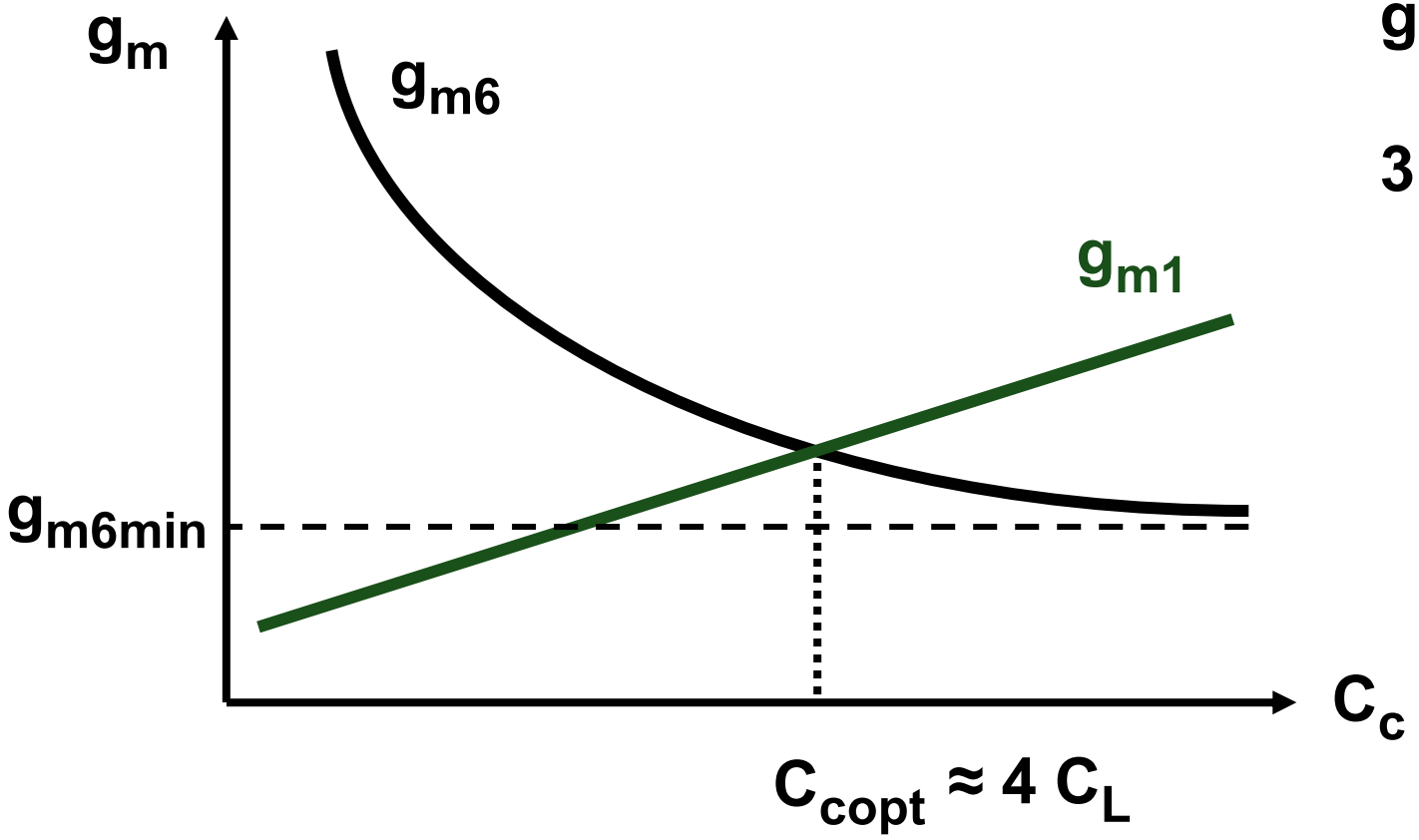
$$\frac{g_{m6}}{g_{m1}} \approx 4 \frac{C_L}{C_c}$$

GBW = 100 MHz and C_L = 2 pF

Choose $C_{n1} < C_c < C_L$

Choice C_c = 1 pF gives g_{m1} = 0.6 mS and g_{m6} = 4.8 mS

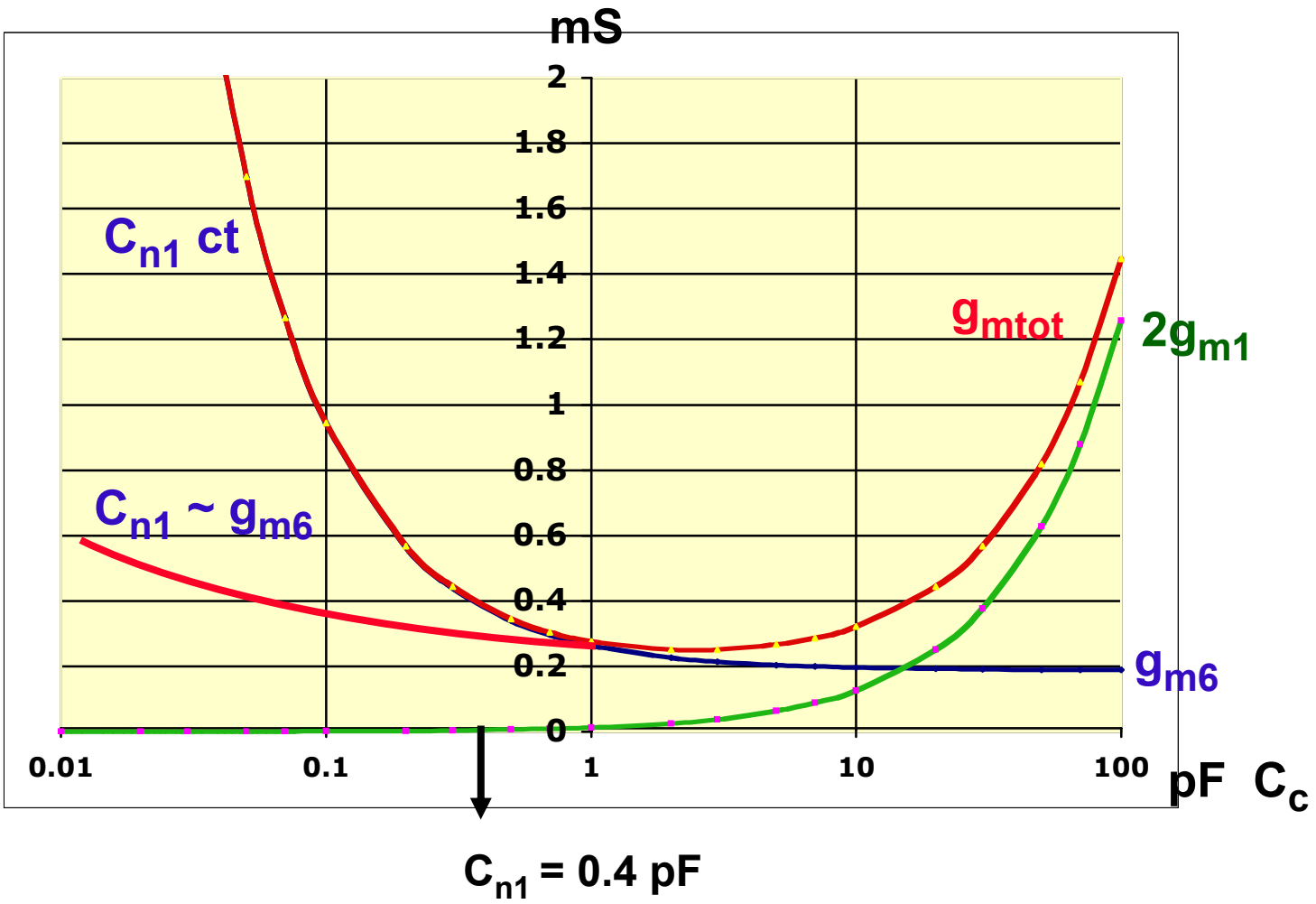
Miller CMOS OTA: Design vs C_c



$g_{m6min} =$

$3\ GBW\ (2\pi\ C_L)$

1 MHz Miller CMOS OTA: Design vs C_c



GBW = 1 MHz

C_L = 10 pF

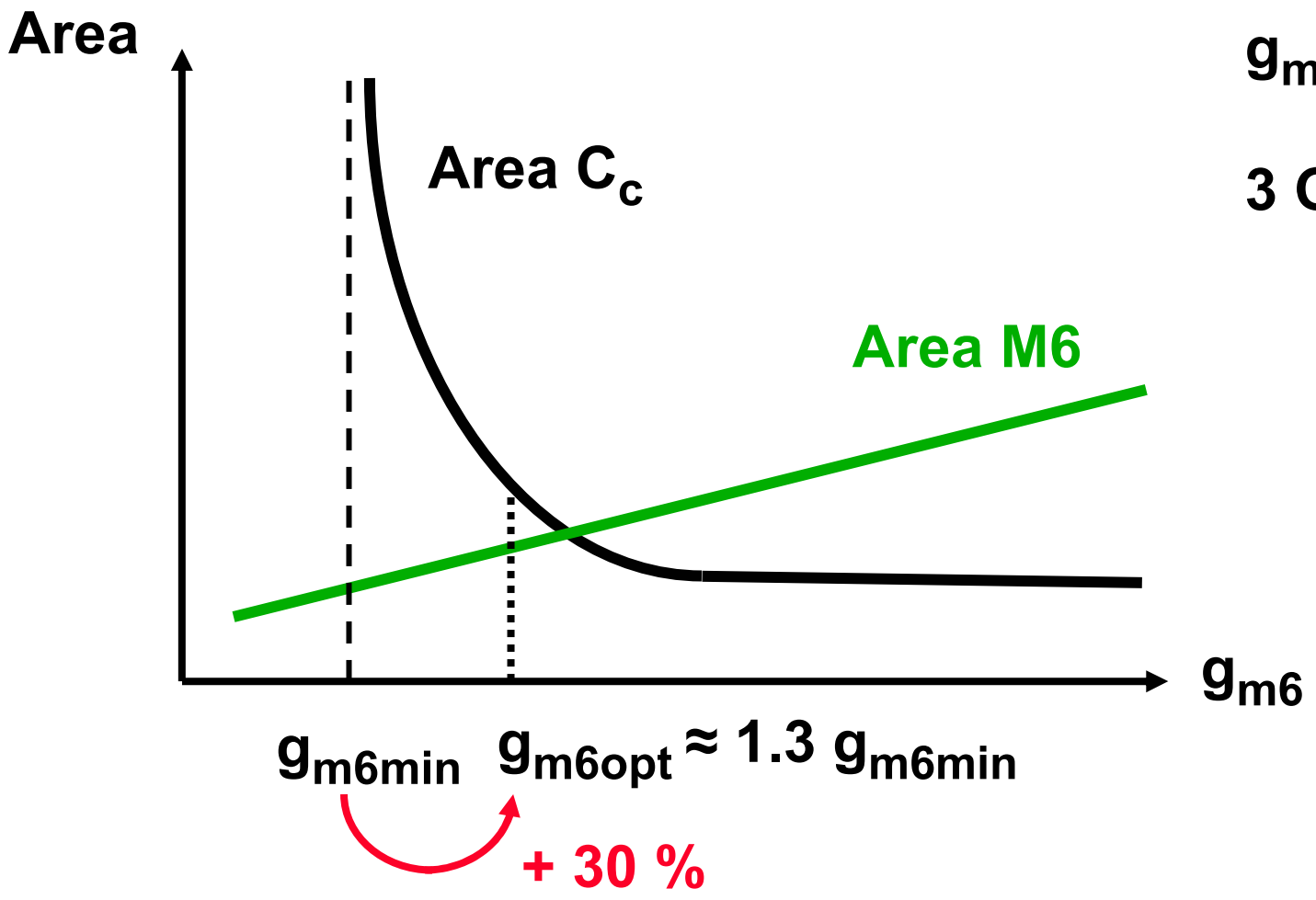
C_{n1} = 0.4 pF

K' = 20 μA/V^2

V_{GS}-V_T = 0.2 V

L = 10 μm

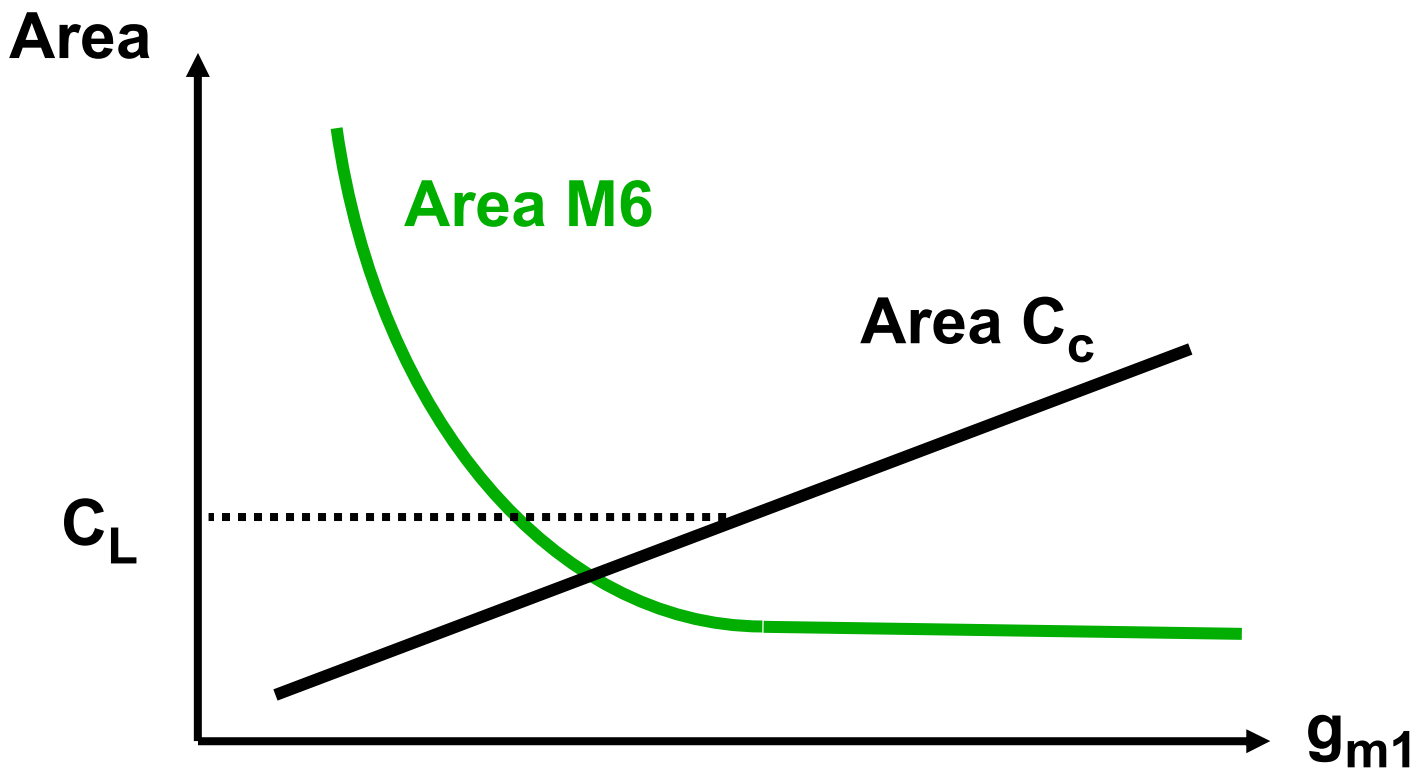
Miller CMOS OTA : Design vs I_{DS6}



g_{m6min} =

3 GBW ($2\pi\ C_L$)

Miller CMOS OTA : Design vs I_{DS1}



Optimum design for high speed Miller OTA - 1

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + C_{n1}/C_c}$$

$$C_L = \alpha C_c \qquad \alpha \approx 2$$

$$C_c = \beta C_{n1} = \beta C_{GS6} \qquad \beta \approx 3$$

$$f_{nd} = \gamma GBW \qquad \gamma \approx 2$$

$$C_{GS} = kW \qquad k = 2\ 10^{-11}\ F/cm$$

$$GBW = \frac{f_{nd}}{\gamma} = \frac{g_{m6}}{2\pi C_L} \frac{1}{\gamma (1 + 1/\beta)}$$

$$C_L = \alpha C_c = \alpha \beta C_{n1} = \alpha \beta C_{GS6} = \alpha \beta kW_6 \qquad W_6 \Uparrow \text{ if } C_L \Uparrow$$

Optimum design Miller for high speed OTA - 2

Elimination of C_L yields

$$GBW = \underbrace{\frac{g_{m6}}{2\pi\, kW_6}}_{f_{T6}} \frac{1}{\alpha\,\beta\,\gamma\,(1 + 1/\beta)} \qquad g_m = \frac{W}{L}\,\frac{17\ 10^{-5}}{1 + 2.8\ 10^4\ L\ /V_{GST}}$$

W, L in cm

$$GBW = \frac{1}{2\pi\, L_6}\,\frac{1}{\alpha\,\beta\,\gamma\,(1 + 1/\beta)}\,\frac{8.5\ 10^6}{1 + 2.8\ 10^4\ L_6\ /\ V_{GST6}} \qquad \text{L in cm}$$

GBW is not determined by C_L, only by L (and V_{GST}) !!

f_T is also determined by L !!!

Optimum design Miller for high speed OTA - 3

Substitution for f_T yields

$$f_T = \frac{g_m}{2\pi C_{GS}}$$

$$GBW = \frac{f_{T6}}{\alpha\,\beta\,\gamma\,(1 + 1/\beta)}$$

$$f_T = \frac{1}{L}\,\frac{1.35}{1 + 2.8\,10^4\,L / V_{GST}}$$

L in cm

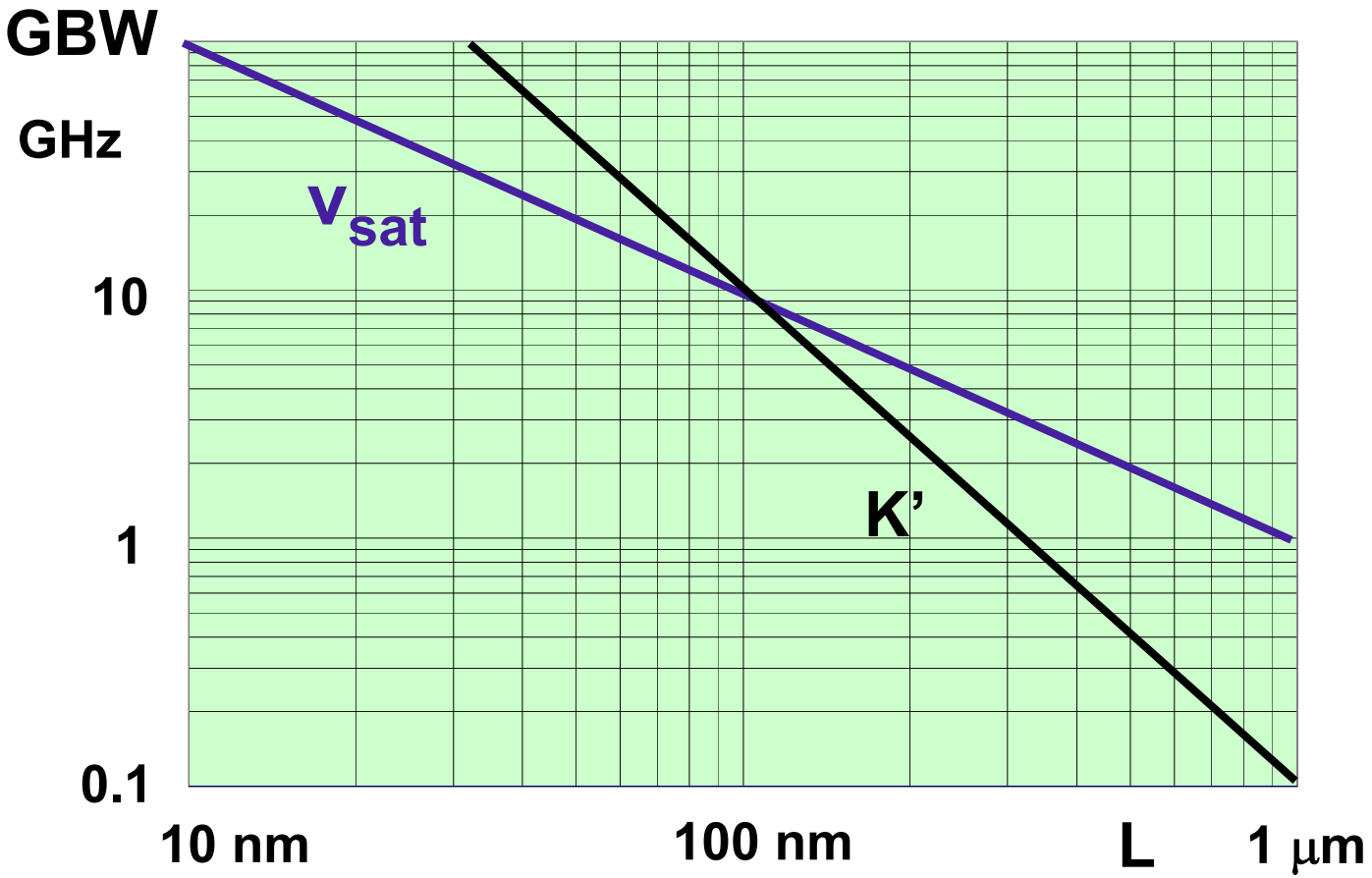
f_T in MHz

GBW is not determined by C_L, only by f_T

f_T is determined by L (and V_{GST}) !!!

If V_{GST} = 0.2 V, v_{sat} takes over for L < 65 nm (If 0.5 V for L < 0.15 μm)

Maximum GBW versus channel length L



$V_{GS}-V_T \approx 0.2$ V

$\alpha \approx 2$

$\beta \approx 3$

$\gamma \approx 2$

or 16 x

$$GBW \approx \frac{f_{T6}}{16}$$

Design optimization for high speed Miller OTA

- Choose α β γ
- Find minimum f_{T6} for specified GBW
- Choose maximum channel length L_6 (max. gain)

  for a chosen V_{GS6}-V_T
- W_6 is calculated from C_L ,

  and determines I_{DS6}
- C_c is calculated from C_L through α
- g_{m1} and I_{DS1} are calculated from C_c
- Noise is determined by g_{m1} or C_c

Design Ex. for GBW = 0.4 GHz & CL = 5 pF

- Choose $\alpha\ \beta\ \gamma$ — **2 3 2**
- Minimum f_{T6} for GBW = 0.4 GHz — f_{T6} = 6.4 GHz
- Maximum channel length L_6 — L_6 = 0.5 μm

  for a chosen V_{GS6}-V_T = 0.2 V
- L_6 is taken to be the minimum L
- W_6 is calculated from C_L, — W_6 = 417 μm

  and determines I_{DS6} (K'_n = 70 $\mu A/V^2$) — I_{DS6} = 2.3 mA

  and determines C_{n1} (k = 2 fF/μm) — C_{n1} = 0.83 pF
- C_c is calculated from C_L through α — C_c = 2.5 pF
- g_{m1} and I_{DS1} are calculated from C_c — I_{DS1} = 0.63 mA

Optimum design Miller for low speed OTA

$$GBW = \frac{f_{T6}}{\alpha\,\beta\,\gamma\,(1 + 1/\beta)}$$

$$\frac{f_I}{f_{TH}} = \sqrt{i}\,(1 - e^{-\sqrt{i}}) \approx i \text{ for small } i$$

$$f_{TH} = \frac{2\,\mu\,kT/q}{2\pi\,L^2}$$

GBW is not determined by C_L, only by f_T

f_T is determined by L and i !!!

Design optimization for low speed Miller OTA

- Choose α β γ
- Find minimum f_{T6} for specified GBW
- Choose channel length L_6 (max. gain), which gives f_{TH6}
- Calculate i_6
- W_6 is calculated from C_L ,

  and determines I_{DST6} and I_{DS6}
- C_c is calculated from C_L through α
- g_{m1} and I_{DS1} are calculated from C_c
- Noise is determined by g_{m1} or C_c

Design Ex. for GBW = 1 MHz & C_L = 5 pF

- Choose $\alpha\ \beta\ \gamma$ — 2 3 2
- Minimum f_{T6} for GBW = 1 MHz — f_{T6} = 16 MHz
- Maximum channel length L_6 — L_6 = 0.5 μm
  - gives f_{TH6} — f_{TH6} = 2 GHz
- Inversion coefficient i is — i = 0.008
- W_6 is calculated from C_L, — W_6 = 417 μm
  - and determines I_{DST6} (K'_n = 70 $\mu A/V^2$) — I_{DST6} = 0.33 mA
  - and determines I_{DS6} — I_{DS6} = 2.7 μA
    - and determines C_{n1} (k = 2 fF/μm) — C_{n1} = 0.83 pF
- C_c is calculated from C_L through α — C_c = 2.5 pF
- g_{m1} and I_{DS1} are calculated from C_c — I_{DS1} = 1.6 μA

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- Design of Miller CMOS OTA
- Design for GBW and Phase Margin
- Other : SR, Output Impedance, Noise, ...

Miller CMOS OTA: Specifications 1

1. Introductory analysis

1.1 DC currents and voltages on all nodes

1.2 Small-signal parameters of all transistors

2. DC analysis

2.1 Common-mode input voltage range vs supply Voltage

2.2 Output voltage range vs supply Voltage

2.3 Maximum output current (sink and source)

Miller CMOS OTA: Specifications 2

3. AC and transient analysis

3.1 AC resistance and capacitance on all nodes

3.2 Gain versus frequency : GBW, …

3.3 Gainbandwidth versus biasing current

3.4 Slew rate versus load capacitance

3.5 Output voltage range versus frequency

3.6 Settling time

3.7 Input impedance vs frequency (open & closed loop)

3.8 Output impedance vs frequency (open & closed loop)

Miller CMOS OTA: Specifications 3

4. Specifications related to offset and noise

4.1 Offset voltage versus common-mode input Voltage

4.2 CMRR versus frequency

4.3 Input bias current and offset

4.4 Equivalent input noise voltage versus frequency

4.5 Equivalent input noise current versus frequency

4.6 Noise optimization for capacitive/inductive sources

4.7 PSRR versus frequency

4.8 Distortion

Miller CMOS OTA: Specifications 4

5. Other second-order effects

5.1 Stability for inductive loads

5.2 Switching the biasing transistors

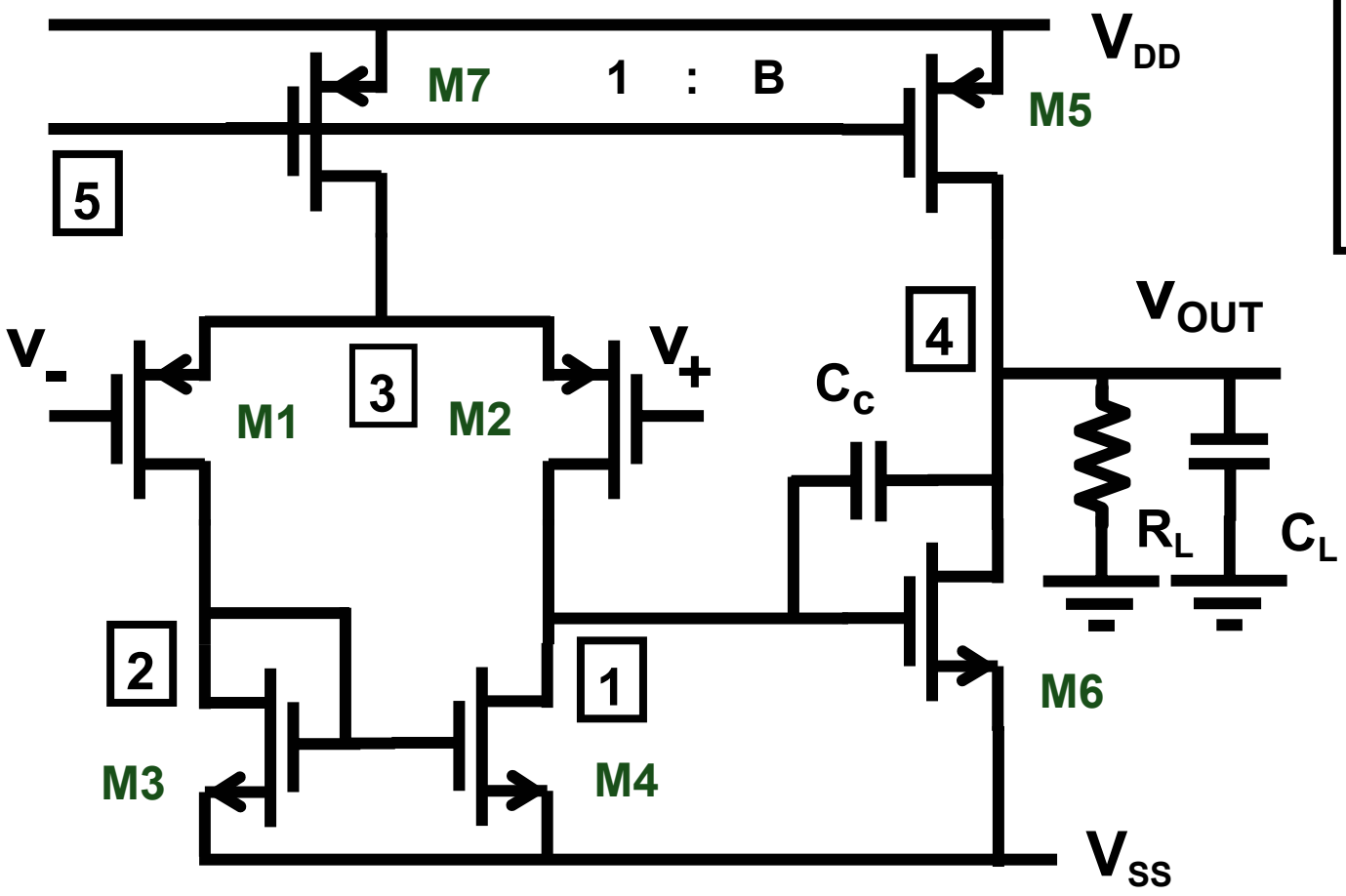
5.3 Switching or ramping the supply voltages

5.4 Different supply voltages, temperatures, ...

M C O : Other specifications

- Common-mode input voltage range
- Output voltage range
- Slew Rate
- Output impedance
- Noise

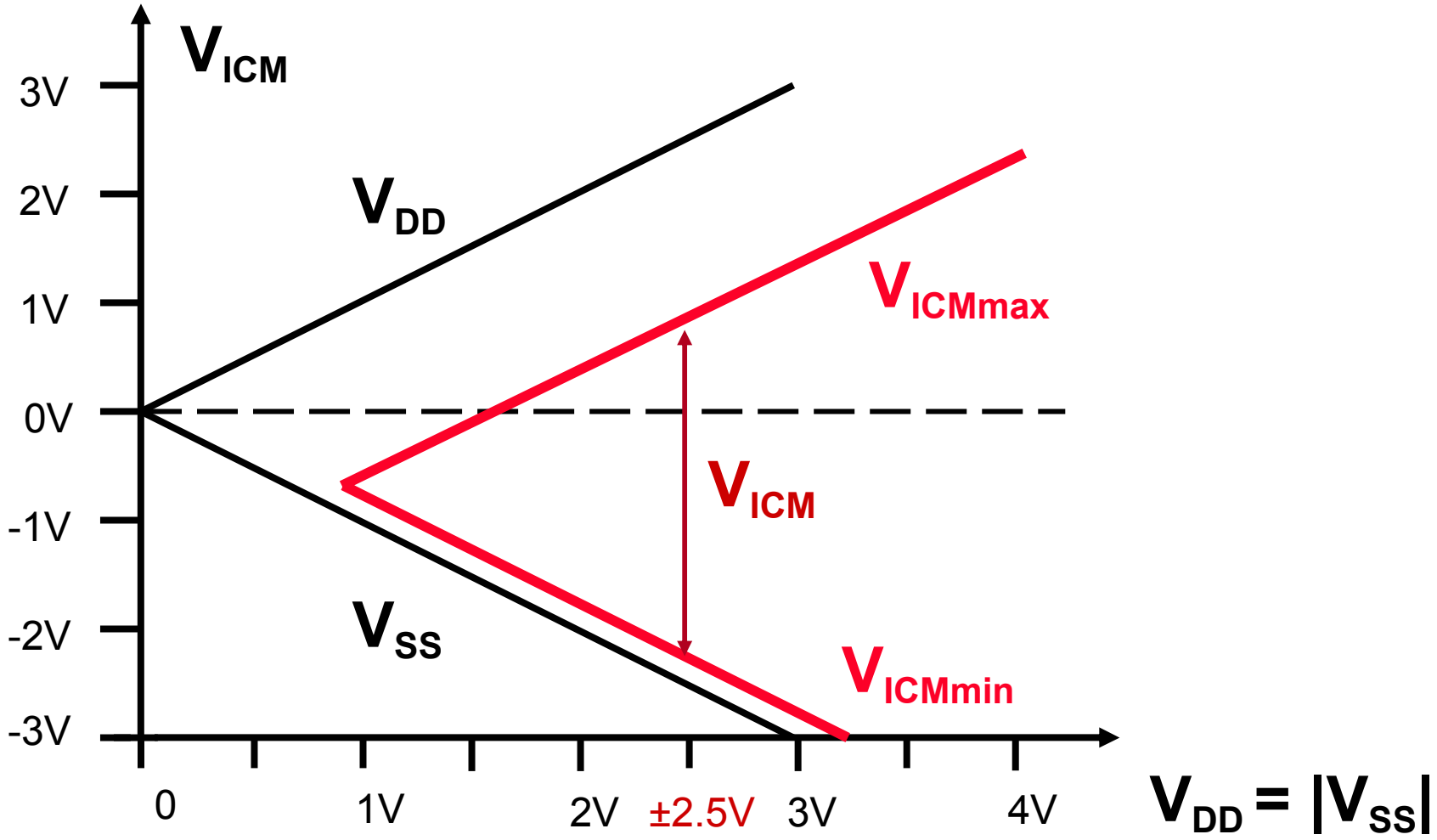
Miller CMOS OTA



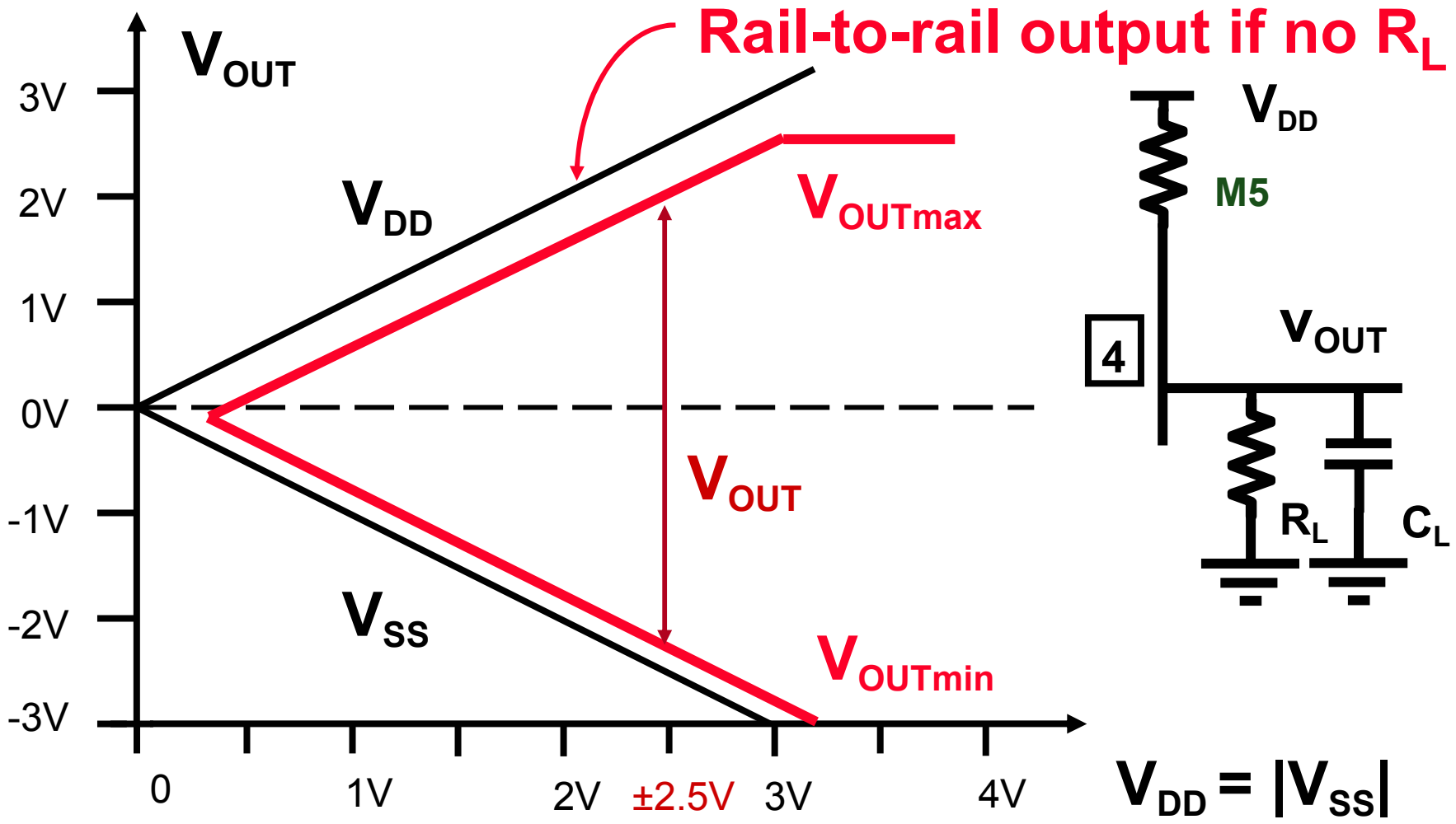
GBW = 1 MHz
C_L = 10 pF
R_L = 10 kΩ

g_{m1} = 7.5 μS
I_{DS1} = 1 μA
g_{o24} = 0.03 μS
g_{m6} = 246 μS
I_{DS6} = 25 μA
C_c = 1 pF

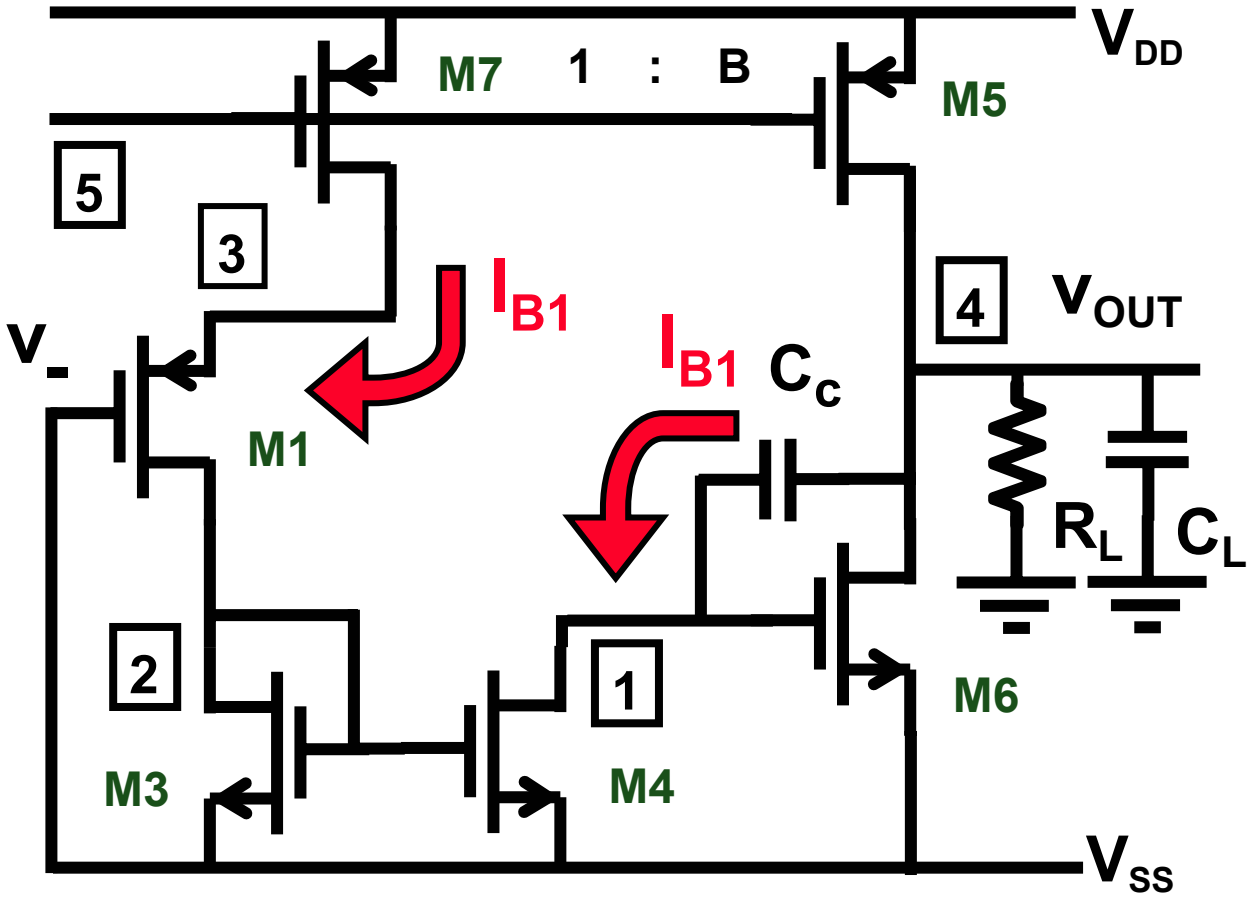
Miller CMOS OTA : CM Input Voltage Range



Miller CMOS OTA : Output Voltage Range



Miller CMOS OTA : Slew Rate - 1



Switch input :

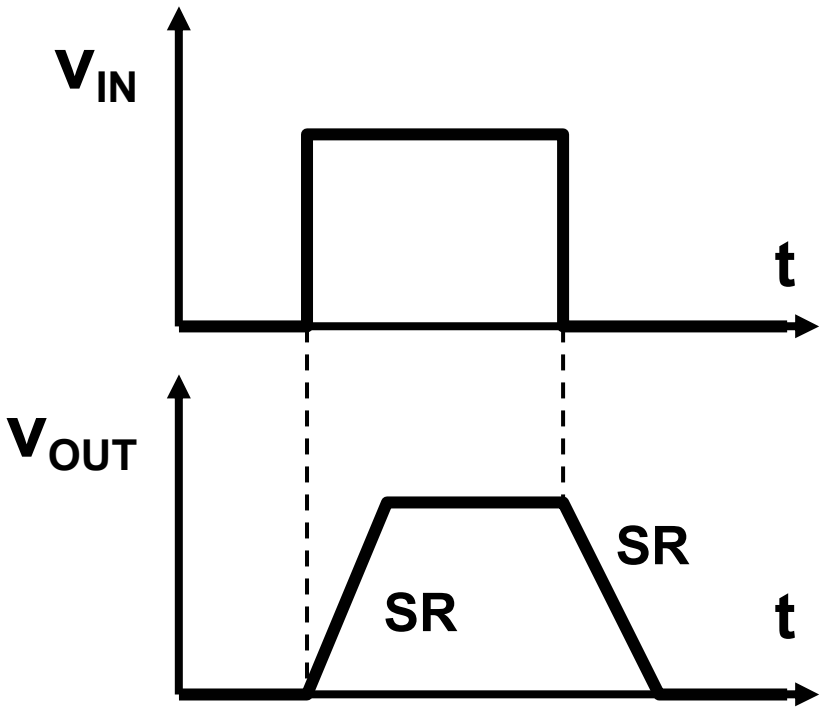
$v_+ > 1$

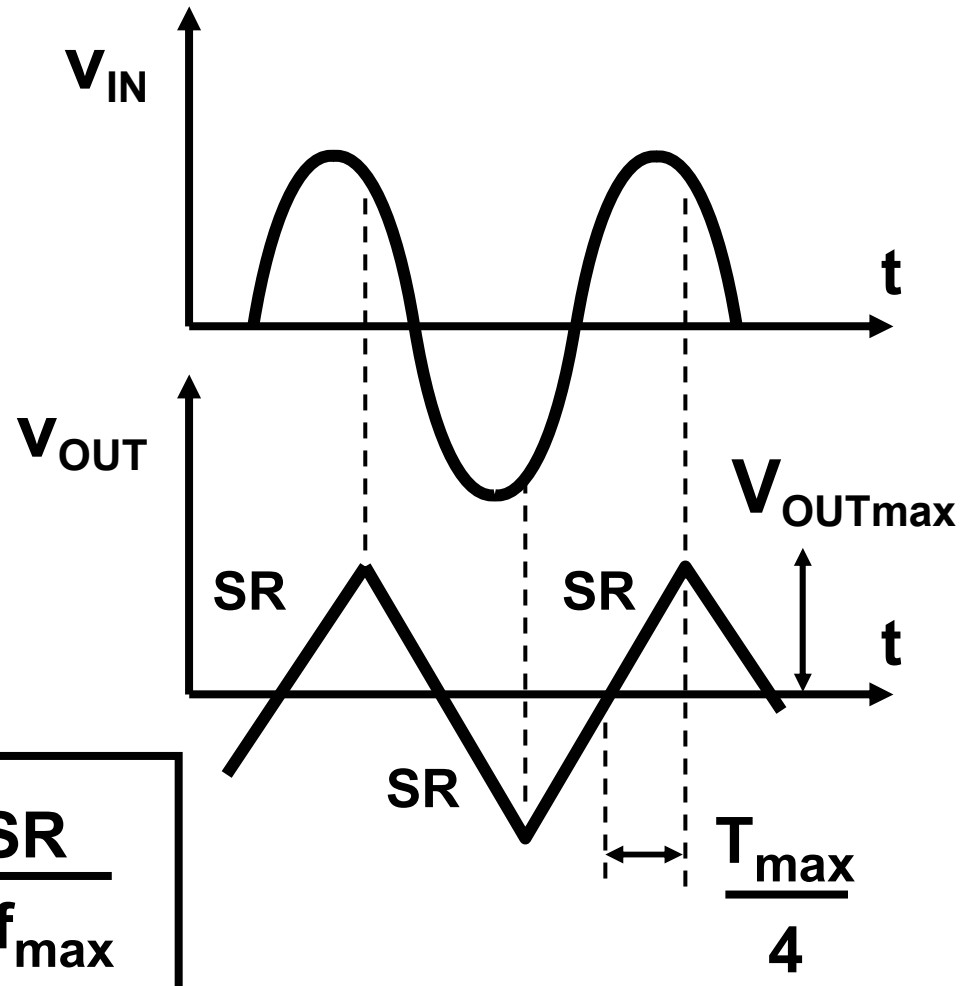
$v_- > 0$

$$SR = \frac{\Delta V_{OUT}}{\Delta t}$$

$$SR = \frac{I_{B1}}{C_c}$$

Miller CMOS OTA : Slew Rate - 2

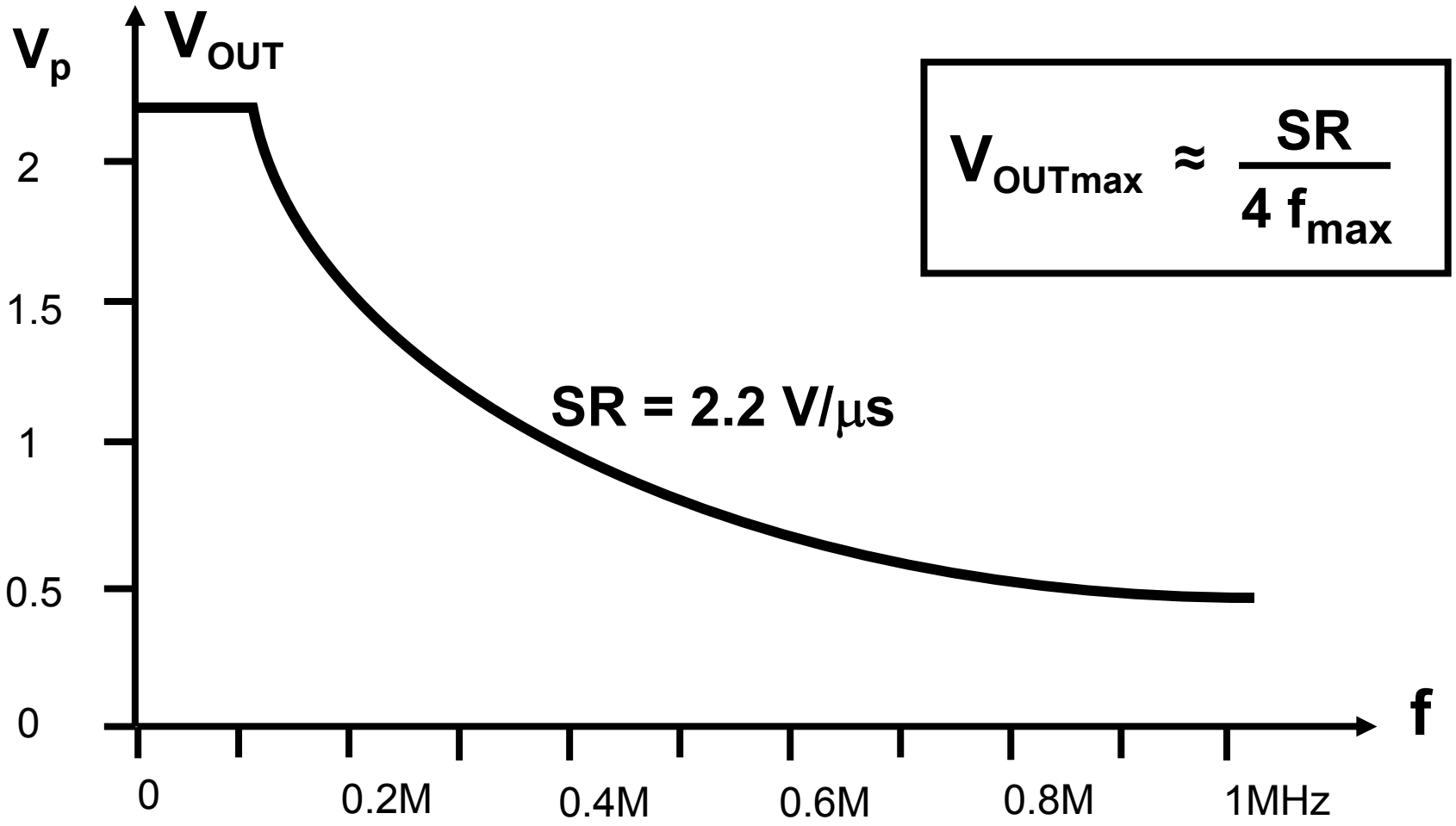




$$\frac{SR}{V_{OUTmax} f_{max}} \approx 4$$

$$V_{OUTmax} \approx \frac{SR}{4 f_{max}}$$

Miller CMOS OTA : Slew Rate - 3



$$V_{OUTmax} \approx \frac{SR}{4\, f_{max}}$$

Design for GBW or SR ?

$$\frac{SR}{GBW} = 4\pi \frac{I_{DS1}}{g_{m1}}$$

$$\frac{I_{DS1}}{g_{m1}} = \frac{V_{GS1}-V_T}{2} \approx 0.1 \ldots 0.3 \text{ V for MOST (si)}$$

x10

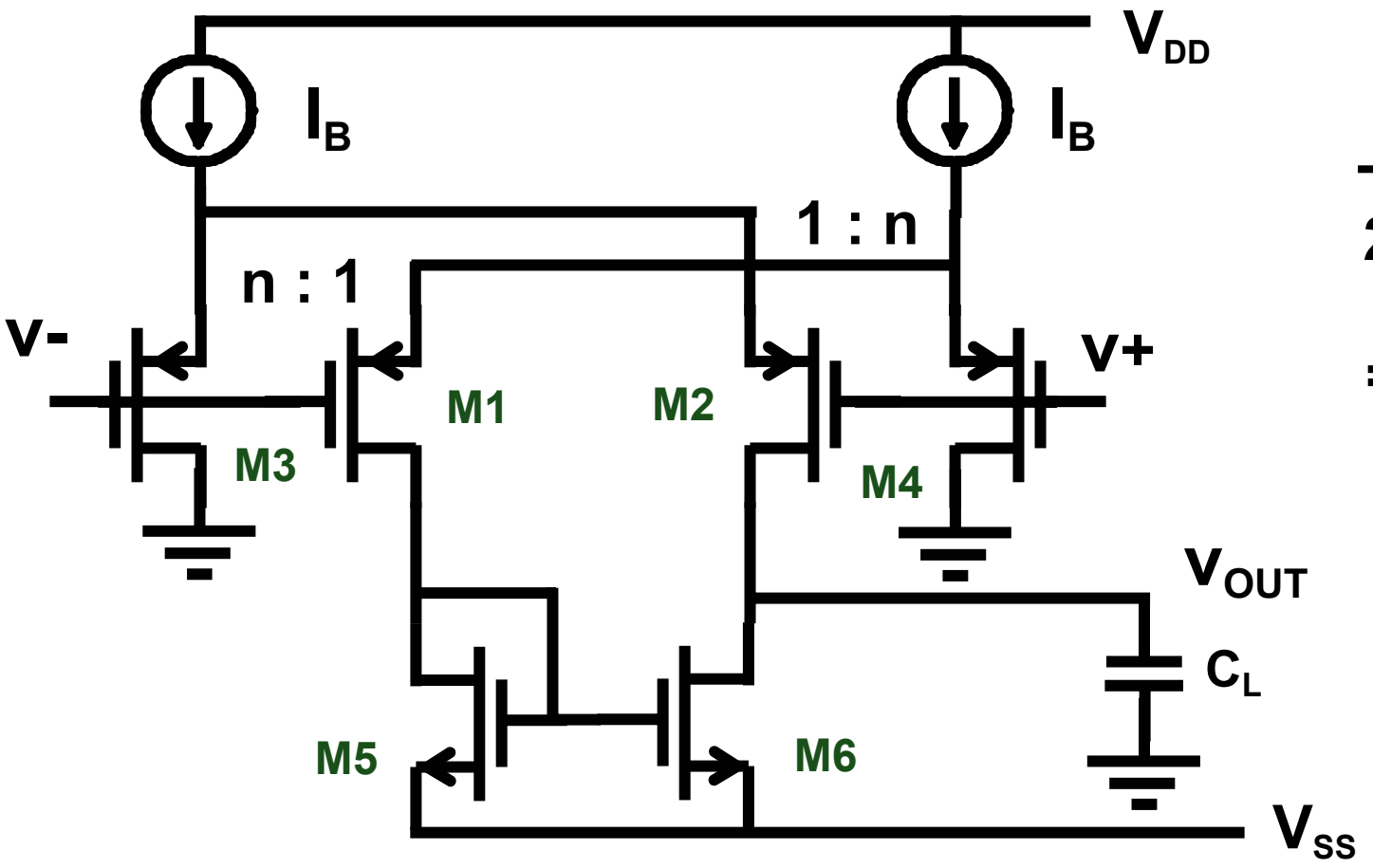
$$\frac{I_{DS1}}{g_{m1}} = \frac{nkT}{q} \approx 30 \ldots 50 \text{ mV for MOST (wi)}$$

$$\frac{I_{CE1}}{g_{m1}} = \frac{kT}{q} \approx 26 \text{ mV for Bipolar trans.}$$

$$\frac{I_{CE1}}{g_{m1}} = (1 + g_{m1}R_E)\frac{kT}{q} \approx \ldots 0.5 \text{ V with } R_E$$

Solomon, JSSC Dec 74, 314-332 □

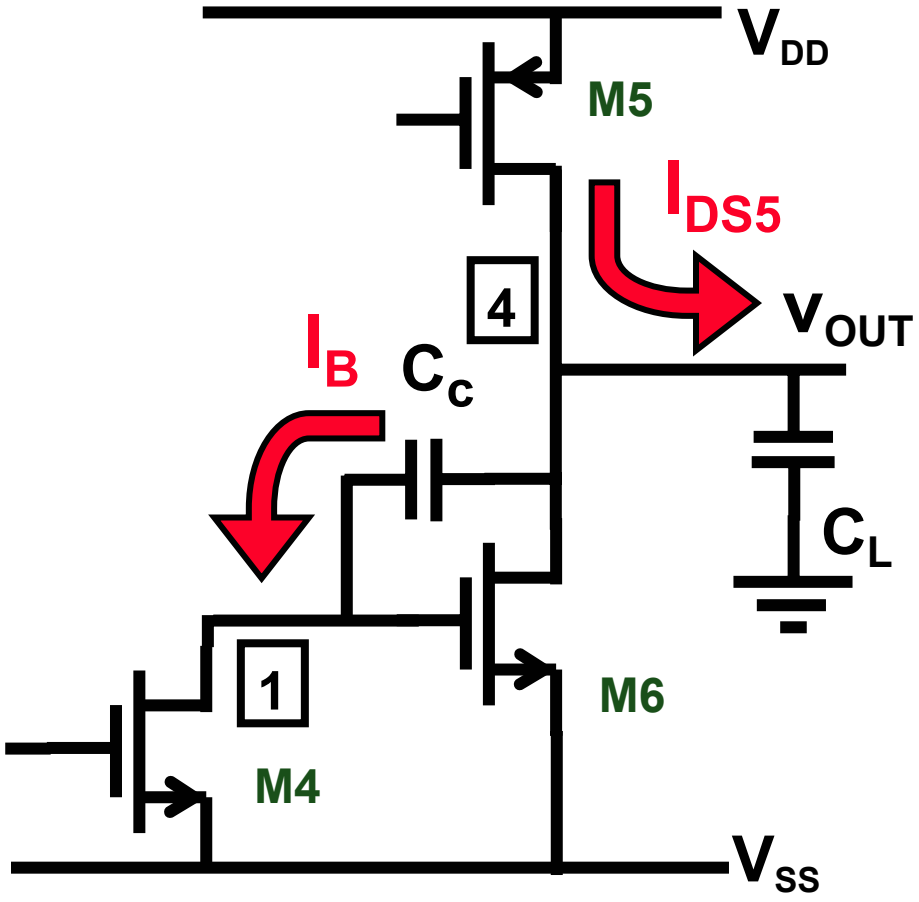
High SR by g_m reduction



$$\frac{SR}{2\pi\ GBW} = x\ (n+1)$$

Ref. Schmoock, JSSC Dec.75, 407-411

External vs internal Slew Rate



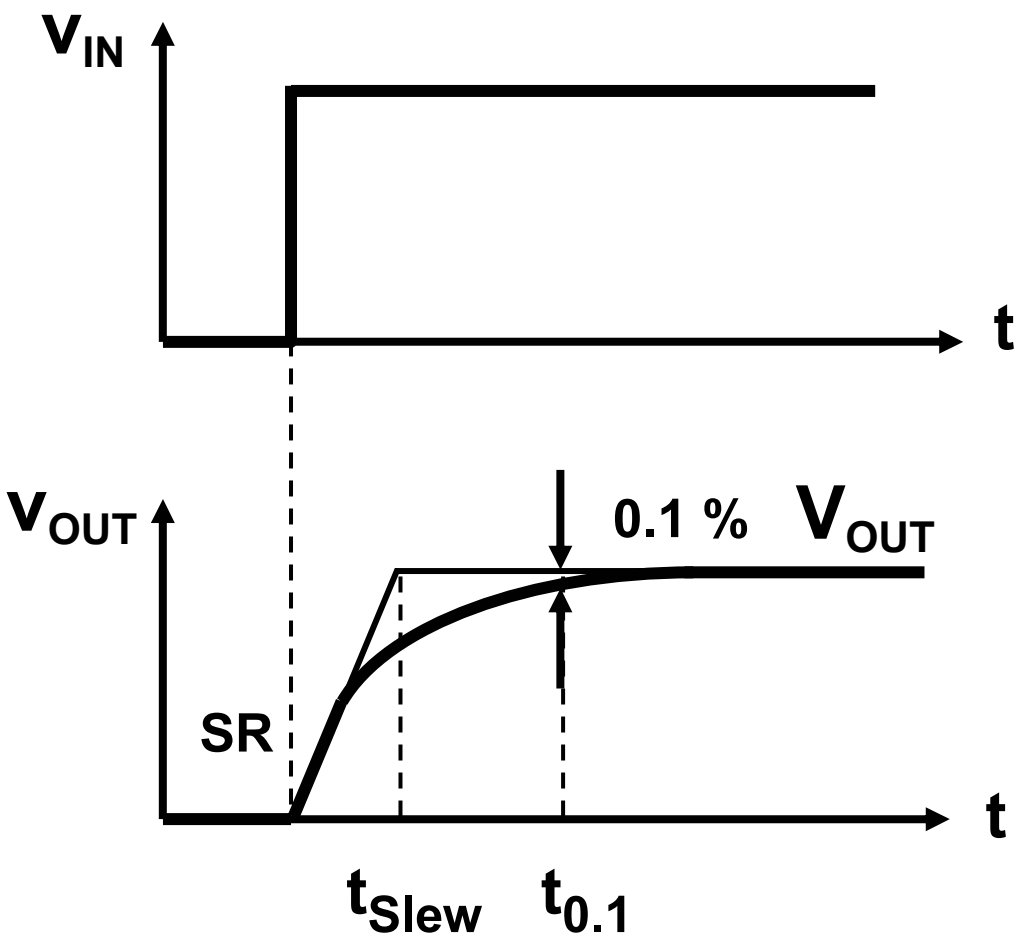
$$SR_{int} = \frac{I_B}{C_c}$$

$$SR_{ext} = \frac{I_{DS5}}{C_L} \quad \text{is larger !}$$

$$\frac{g_{m6}}{g_{m1}} = 4\,\frac{C_L}{C_c} = \frac{I_{DS5}}{I_{DS1}}$$

$$\frac{I_{DS5}}{C_L} \approx 2\,\frac{2I_{DS1}}{C_c}$$

Slew Rate and settling



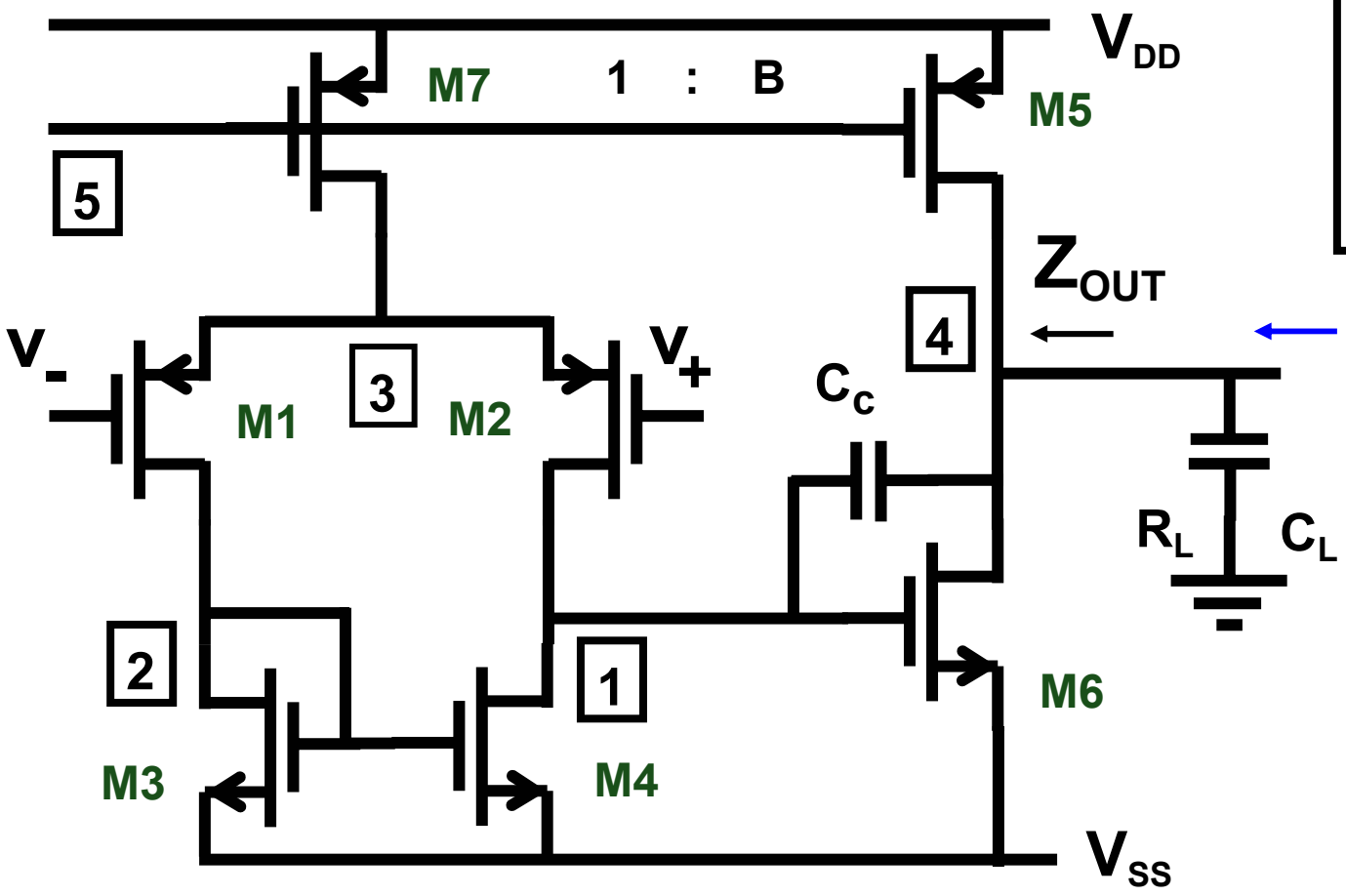
$$t_{TOT} = t_{Slew} + t_{0.1}$$

$$t_{Slew} = \frac{V_{OUT}}{SR}$$

$$t_{0.1} = \frac{7}{2\pi\ BW}$$

$$\ln(1000) \approx 7$$

Miller CMOS OTA Output Impedance



GBW = 1 MHz

C_L = 10 pF

g_{m1} = 7.5 μS

I_{DS1} = 1 μA

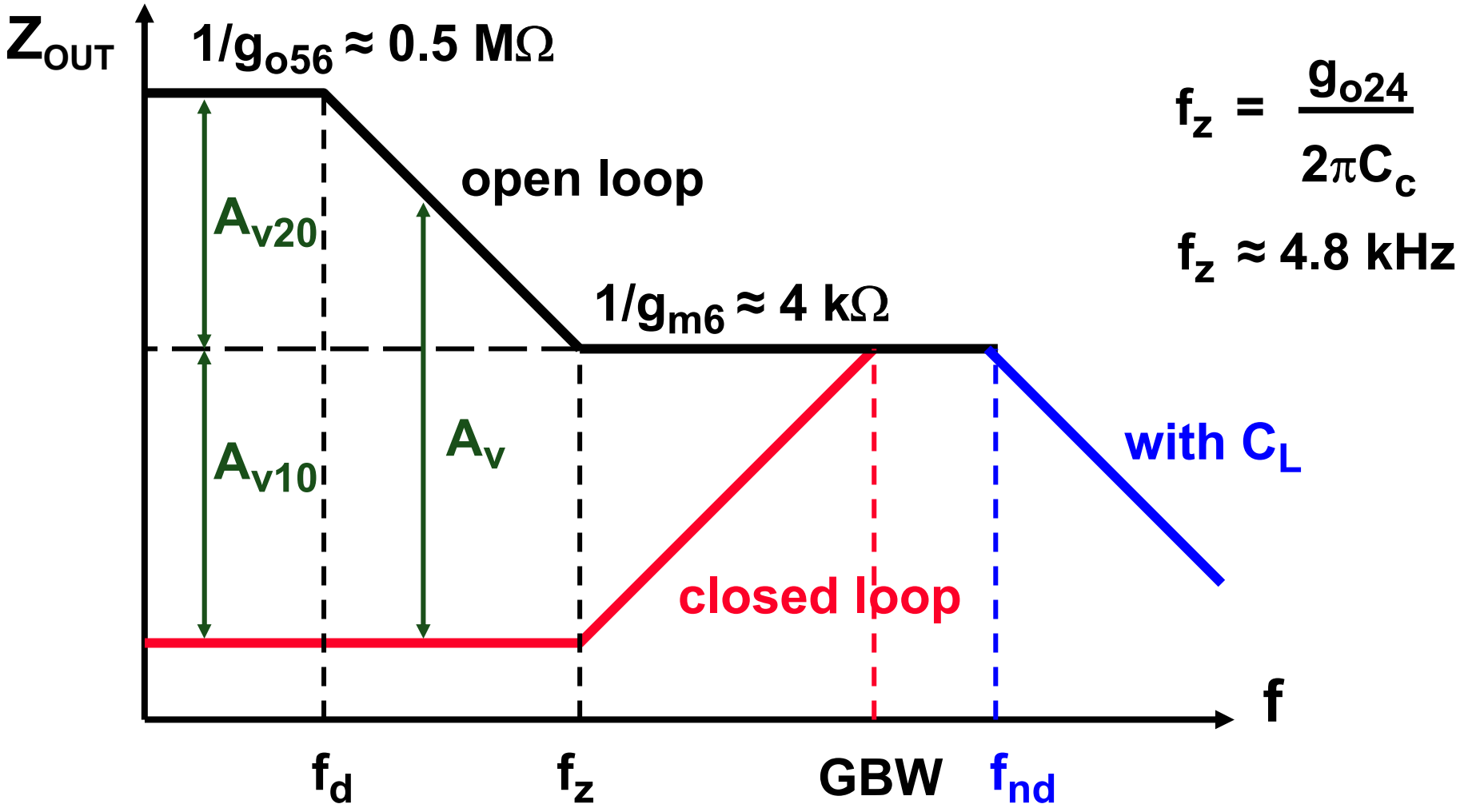
g_{o24} = 0.03 μS

g_{m6} = 246 μS

I_{DS6} = 25 μA

C_c = 1 pF

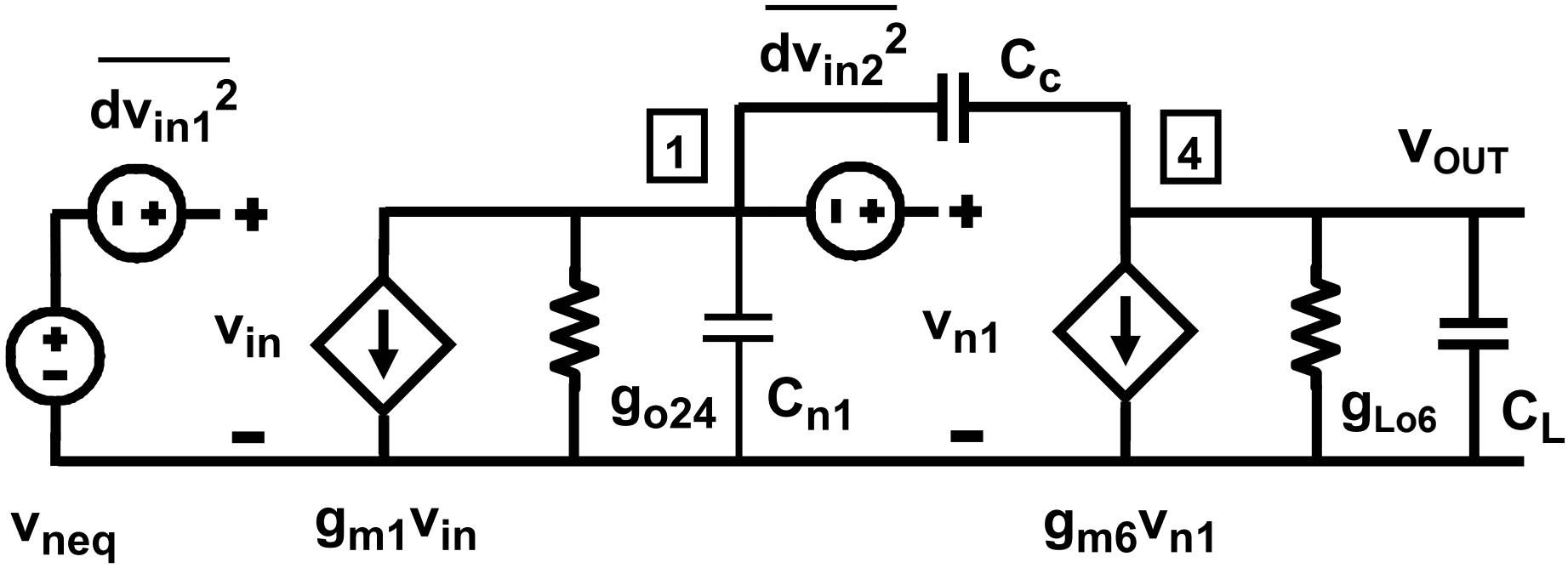
Miller CMOS OTA : Output impedance Z_{OUT}



$$f_z = \frac{g_{o24}}{2\pi C_c}$$

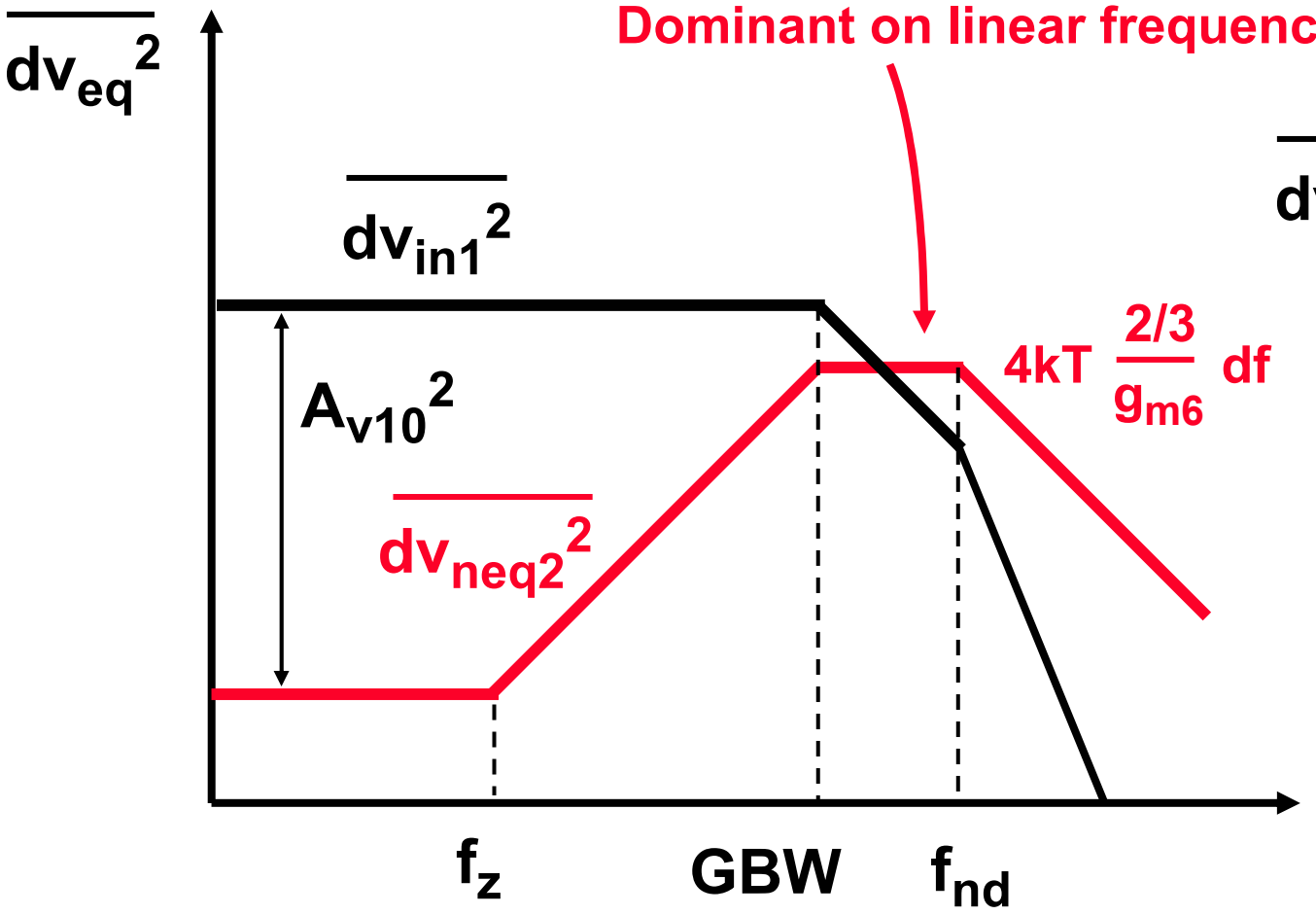
$$f_z \approx 4.8\ kHz$$

Miller CMOS OTA : Noise density 1



$$\overline{dv_{in1}^2} \approx 4kT \frac{4/3}{g_{m1}} df \qquad \overline{dv_{in2}^2} \approx 4kT \frac{2/3}{g_{m6}} df$$

Miller CMOS OTA : Noise density 2

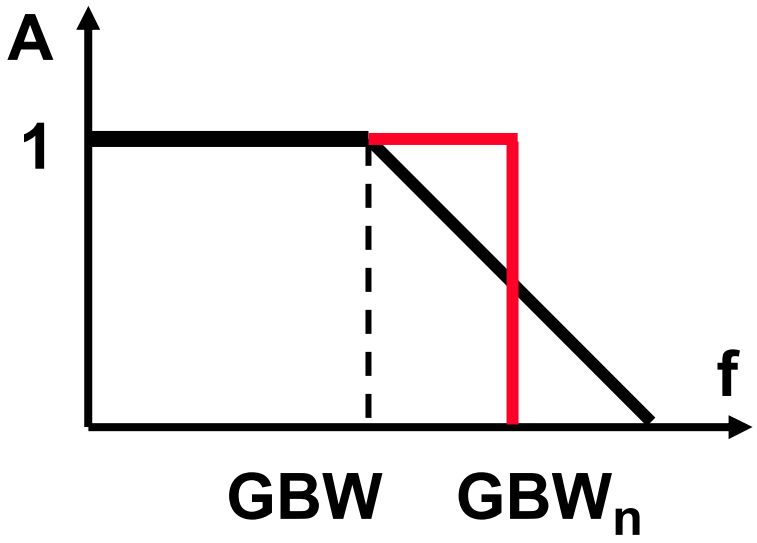


$$\overline{dv_{neq2}^2} = \frac{\overline{dv_{in2}^2}}{|A_{v1}|^2}$$

$$A_{v10} = \frac{g_{m1}}{g_{o24}}$$

$$f_z = \frac{g_{o24}}{2\pi C_c}$$

Miller CMOS OTA : Integrated Noise



$$= \frac{\pi}{2} GBW$$

$$\overline{v_{nieq}^2} = \int_0^\infty \frac{\overline{dv_{nieq}^2}}{1 + (f/GBW)^2}$$

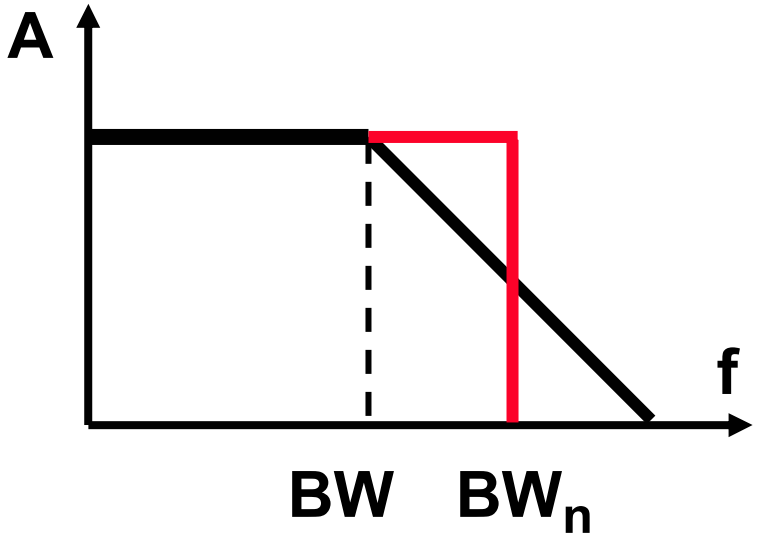
$$\int_0^\infty \frac{dx}{1 + x^2} = \frac{\pi}{2}$$

$$\overline{v_{nieq}^2} = 4kT \frac{4/3}{g_{m1}} GBW \frac{\pi}{2}$$

$$\overline{v_{nieq}^2} = \frac{4}{3} \frac{kT}{C_c}$$

$C_c = 1pF \quad v_{Rs} = 74\ \mu V_{RMS}$

Noise density vs integrated noise



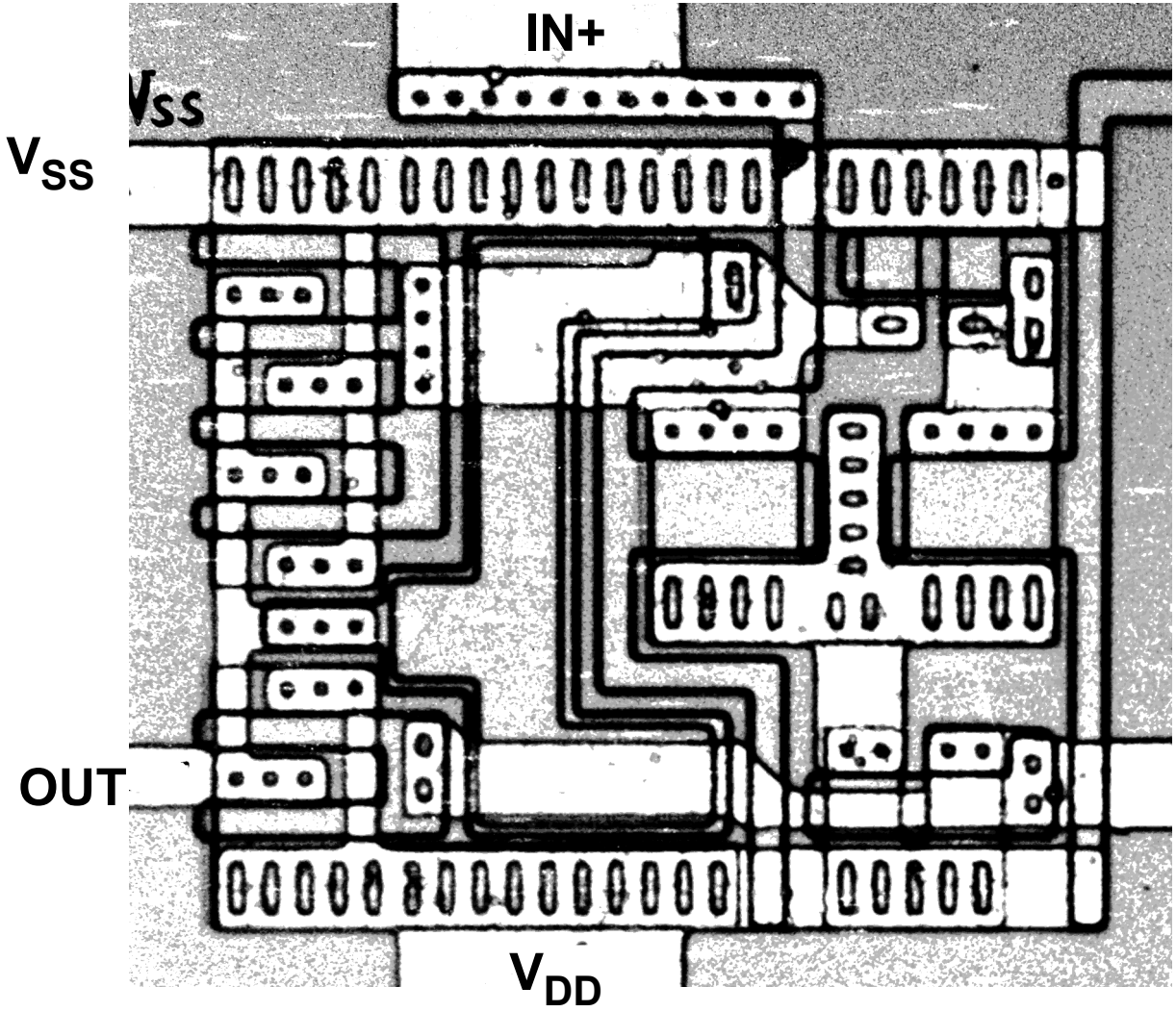
$$\overline{dv_{ni}^2} = 4kT \frac{4/3}{g_m} df$$

$$\overline{v_{ni}^2} = \int_0^\infty \frac{\overline{dv_{ni}^2}}{1 + (f/BW)^2} = \frac{4kT}{3C_c}$$

Noise density (V^2/Hz) ~ $1/g_m$ (or R_S)

Integrated noise (V_{RMS}) ~ $1/C_c$

CMOS Miller OTA layout



GBW = 1 MHz

C_L = 10 pF

SR = 2.2 V/μs

V_{DD} = 5 V

I_{TOT} = 27 μA

370 MHzpF/mA

Miller CMOS OTA : Exercise

GBW = 50 MHz for C_L = 2 pF : use min. I_{DS6} !

Techno: L_{min} = 0.5 μm; K'_n = 50 μA/V² & K'_p = 25 μA/V²

C_{GS} = kW (= C_{ox}WL) and k = 2 fF/ μm

V_{GS} - V_T = 0.2 V

Find

g_{m6} I_{DS6} W_6 $C_{n1} = C_{GS6}$ C_c g_{m1} I_{DS1} $\overline{dv_{ineq}^2}$ v_{inRMS}

Conclusion : Table of contents

- **Design of Single-stage OTA**
- **Design of Miller CMOS OTA**
- **Design for GBW and Phase Margin**
- **Other specs: Input range, output range, SR, ...**