# Coupling effects in Mixed analog-digital ICs


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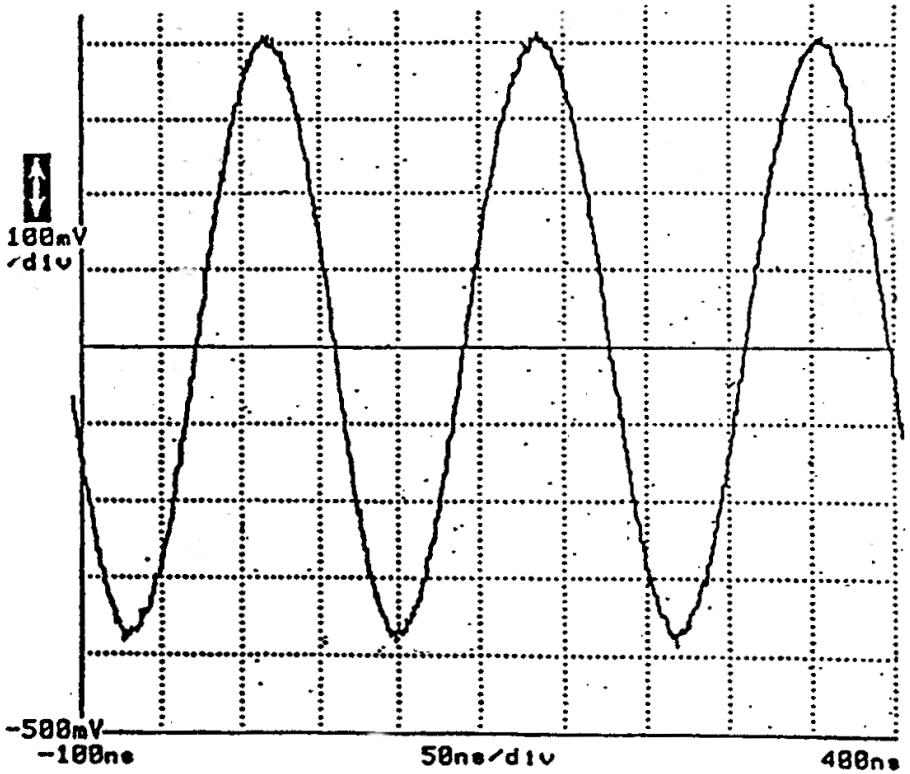
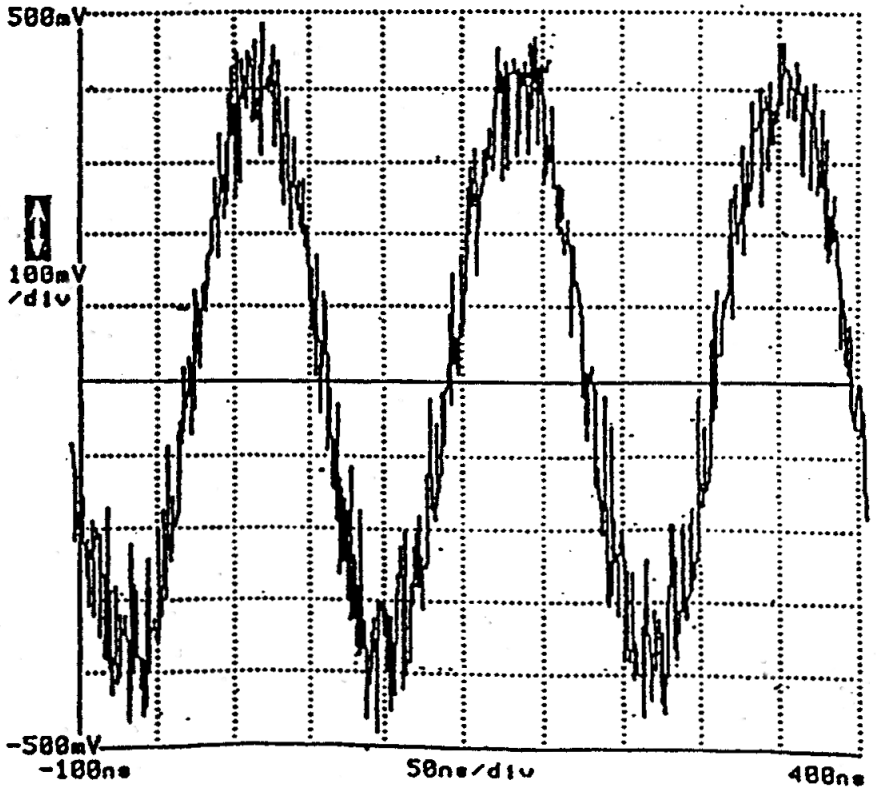
# Switching Noise

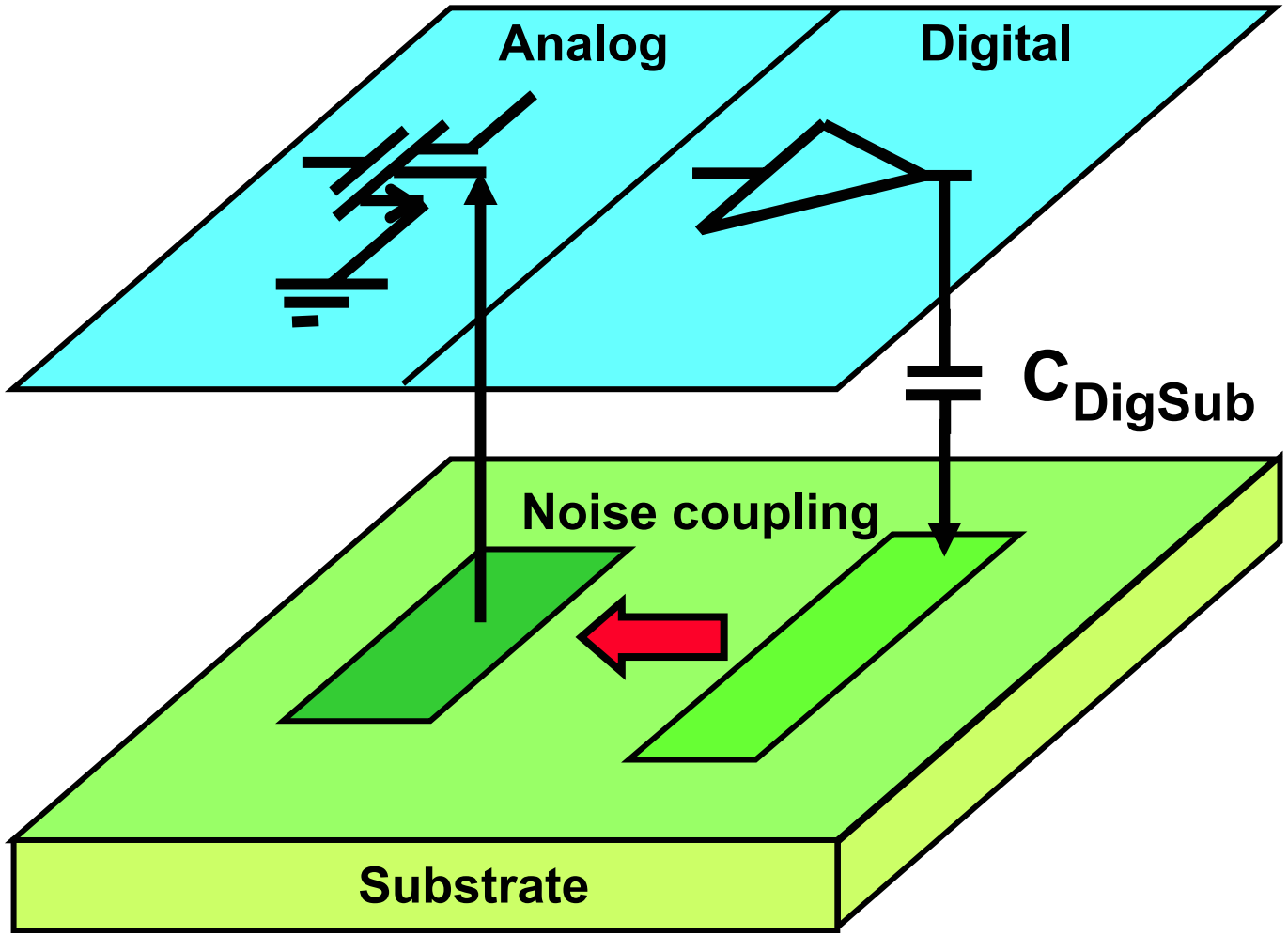



Output without logic switching




Output with logic switching

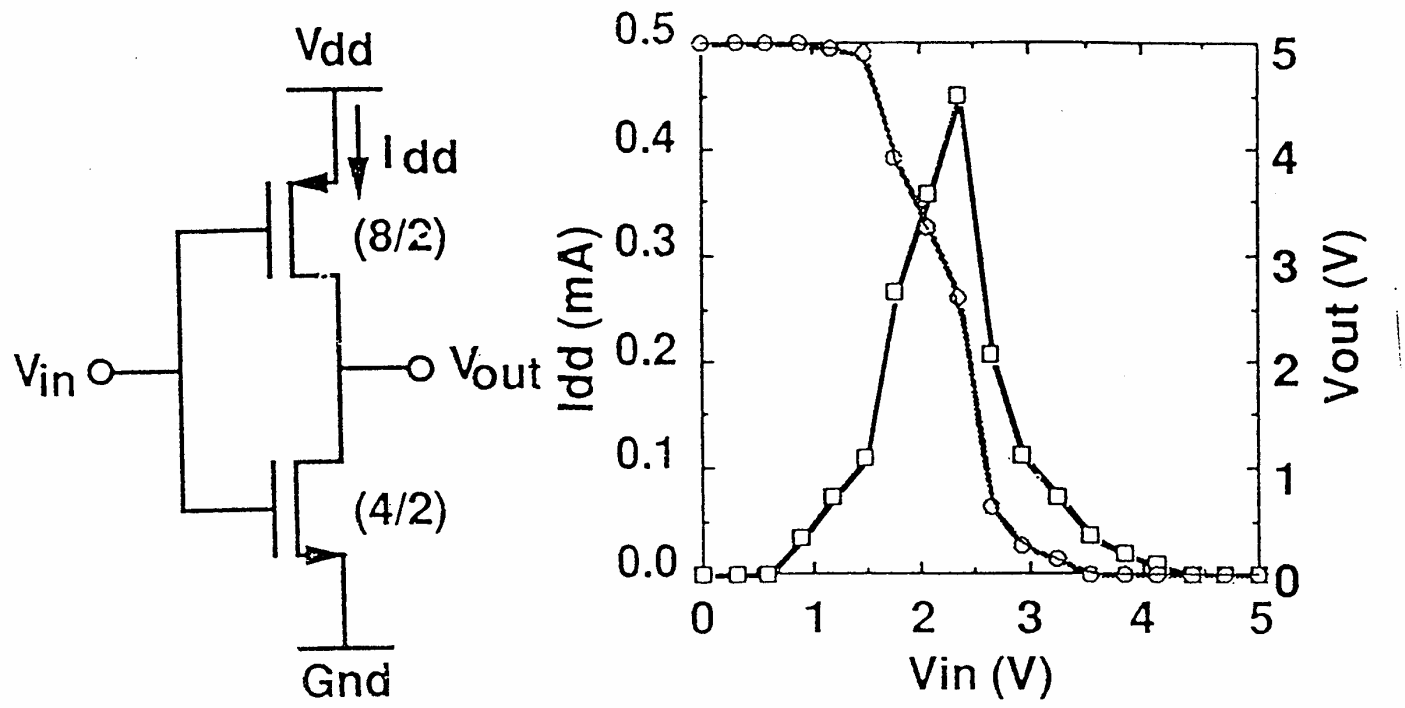
# Noise coupling through the substrate



# Outline

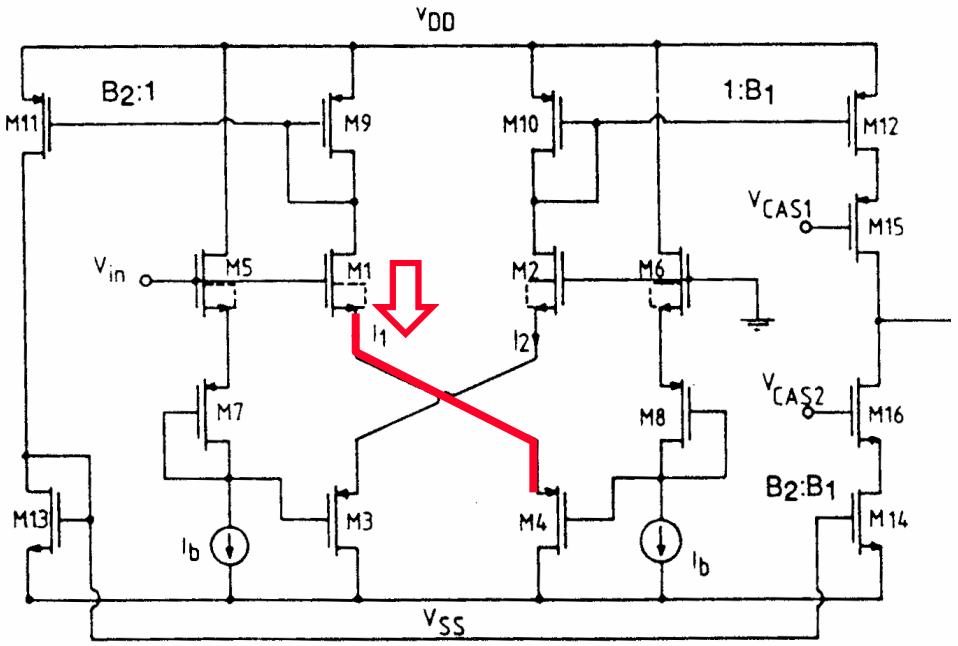
- **Circuit noise generation**
- Circuit noise coupling
  - Power supply pinning
  - Substrate coupling
  - Circuit placement
- Rejection of circuit noise
  - PSRR

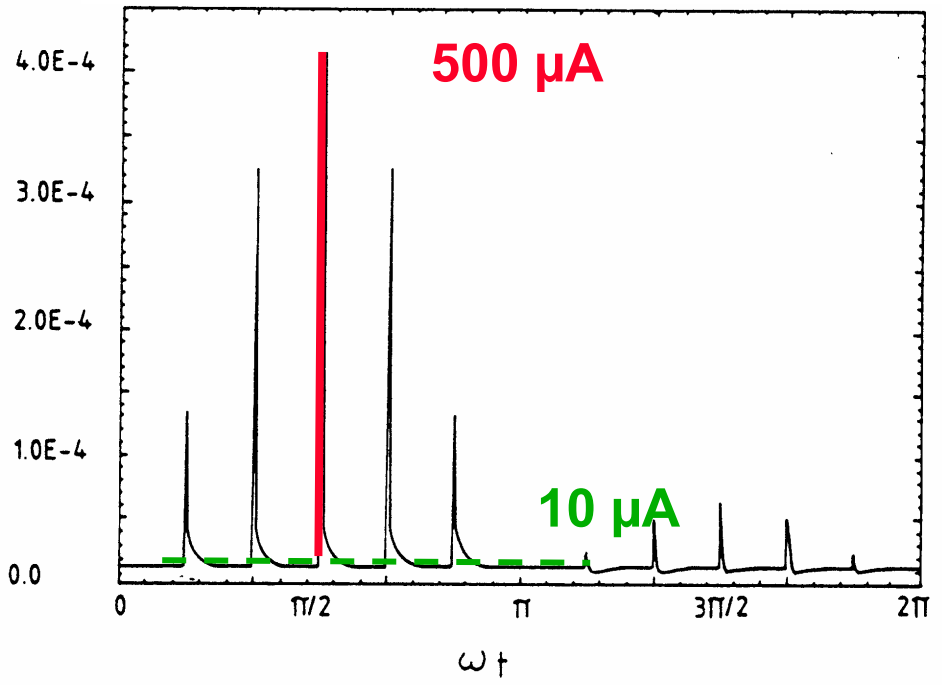
# Circuit Noise Generation




$$I(t) \approx \underbrace{\frac{K}{4}(V_{DD} - V_{SS} - 2|V_T|)^2}_{I_{max}}(1 - \frac{2|t|}{\tau})$$

# Class AB Input structures

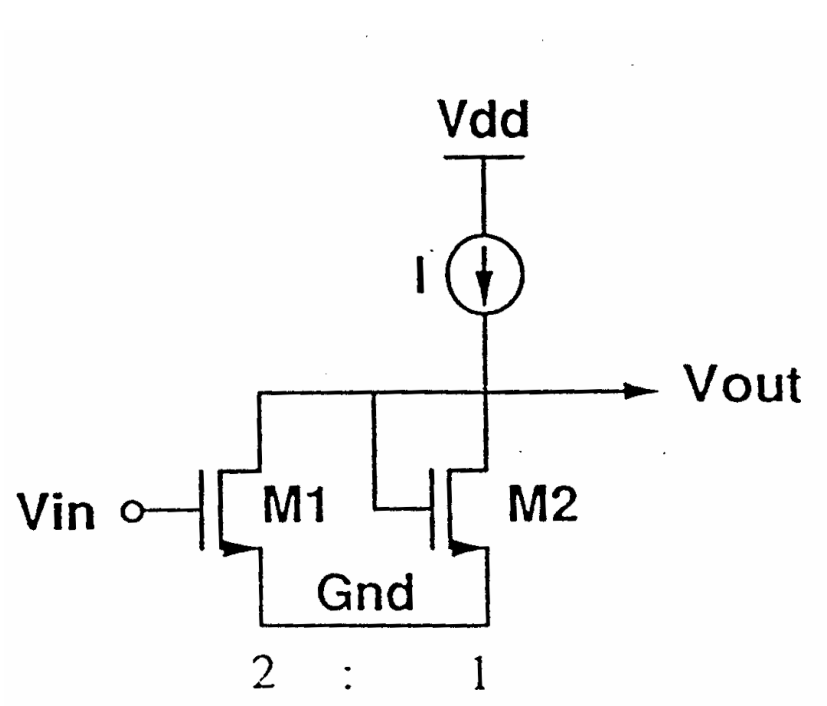


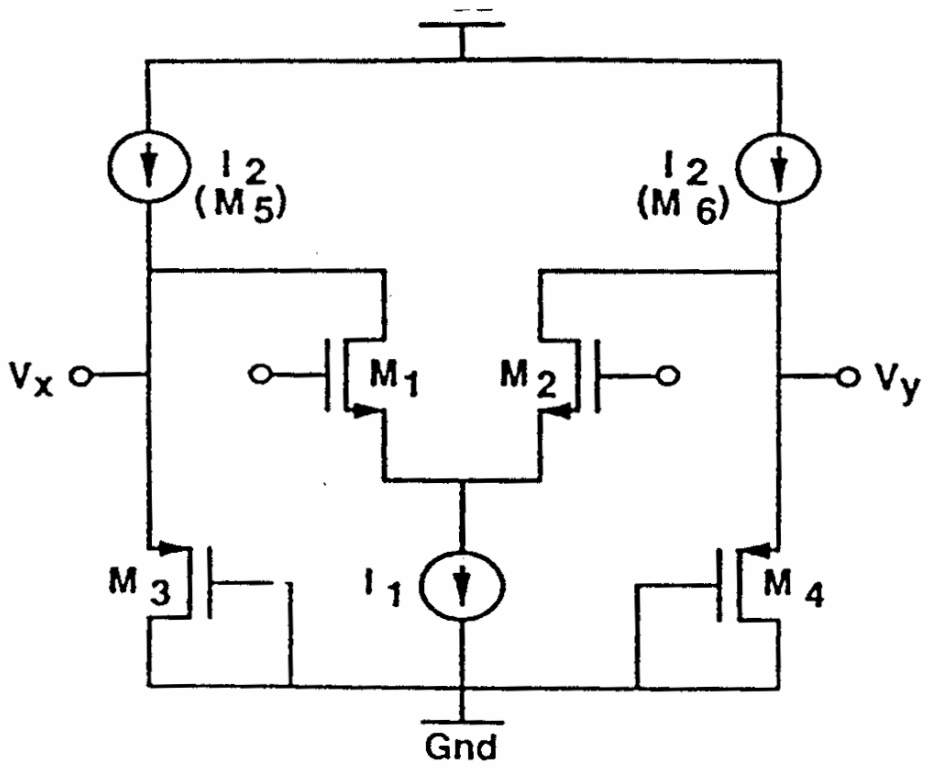

**Over 50 x**

Halonen, CICC

# Current Mode Logic



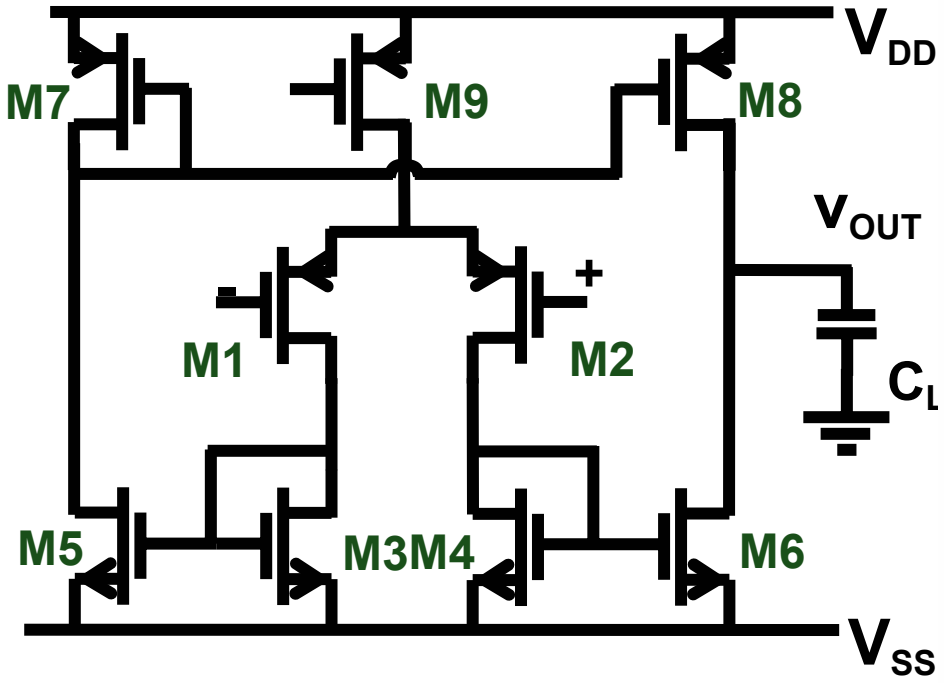

Current Mode Logic

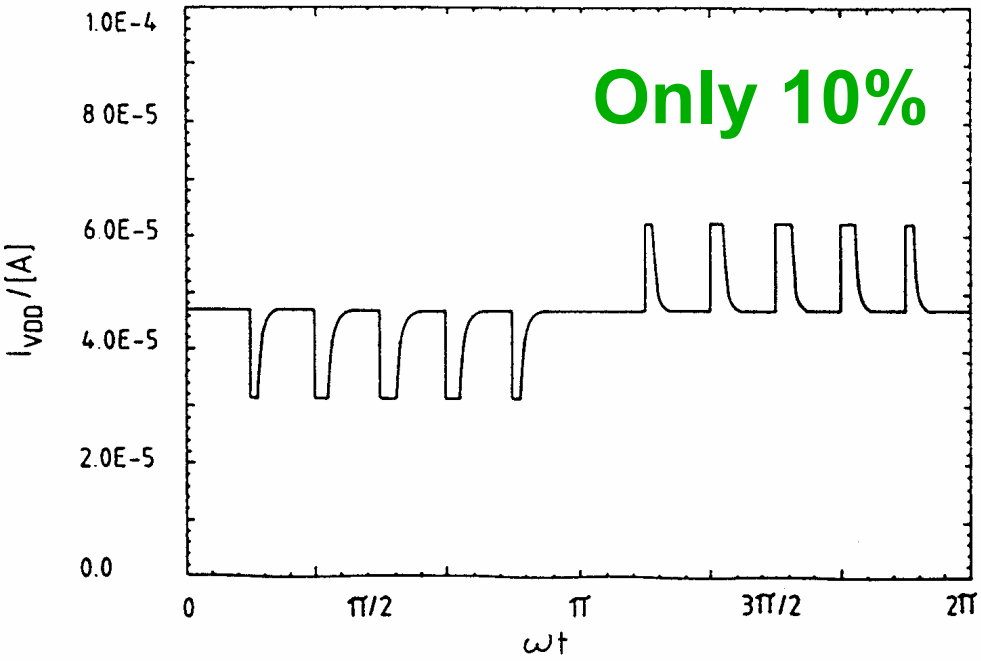



ECL alike CMOS Logic

Allstot, CICC

# Symmetrical OTA's



# Outline

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  - Power supply pinning
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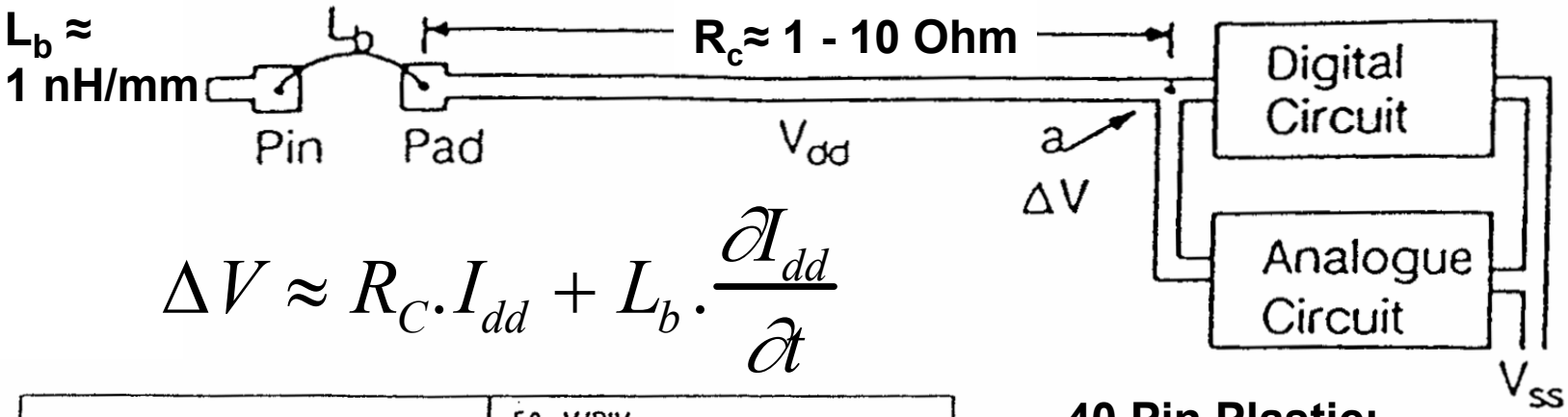
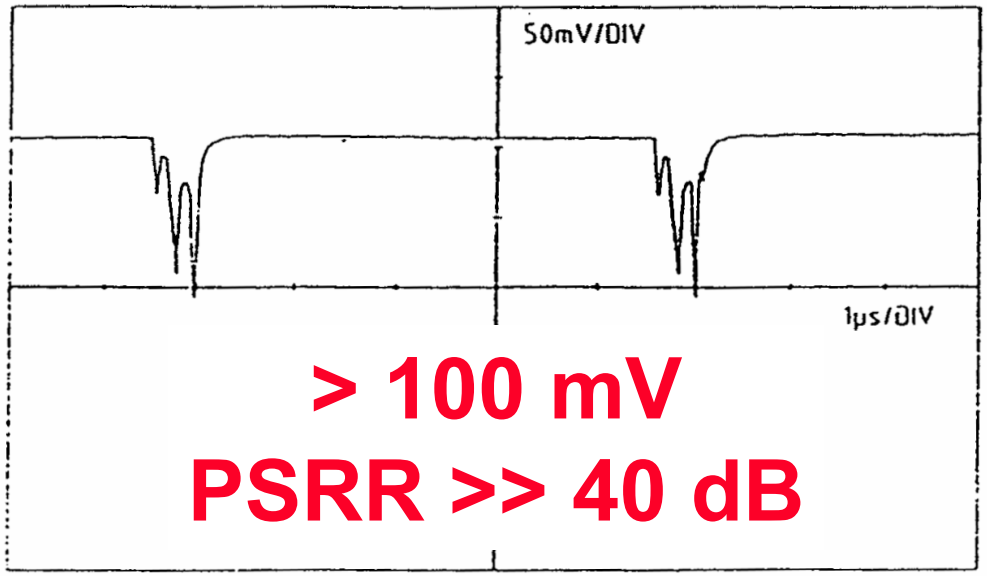
# Power Supply Pinning




$$\Delta V \approx R_C . I_{dd} + L_b . \frac{\partial I_{dd}}{\partial t}$$




**> 100 mV**

**PSRR >> 40 dB**

**40 Pin Plastic:**

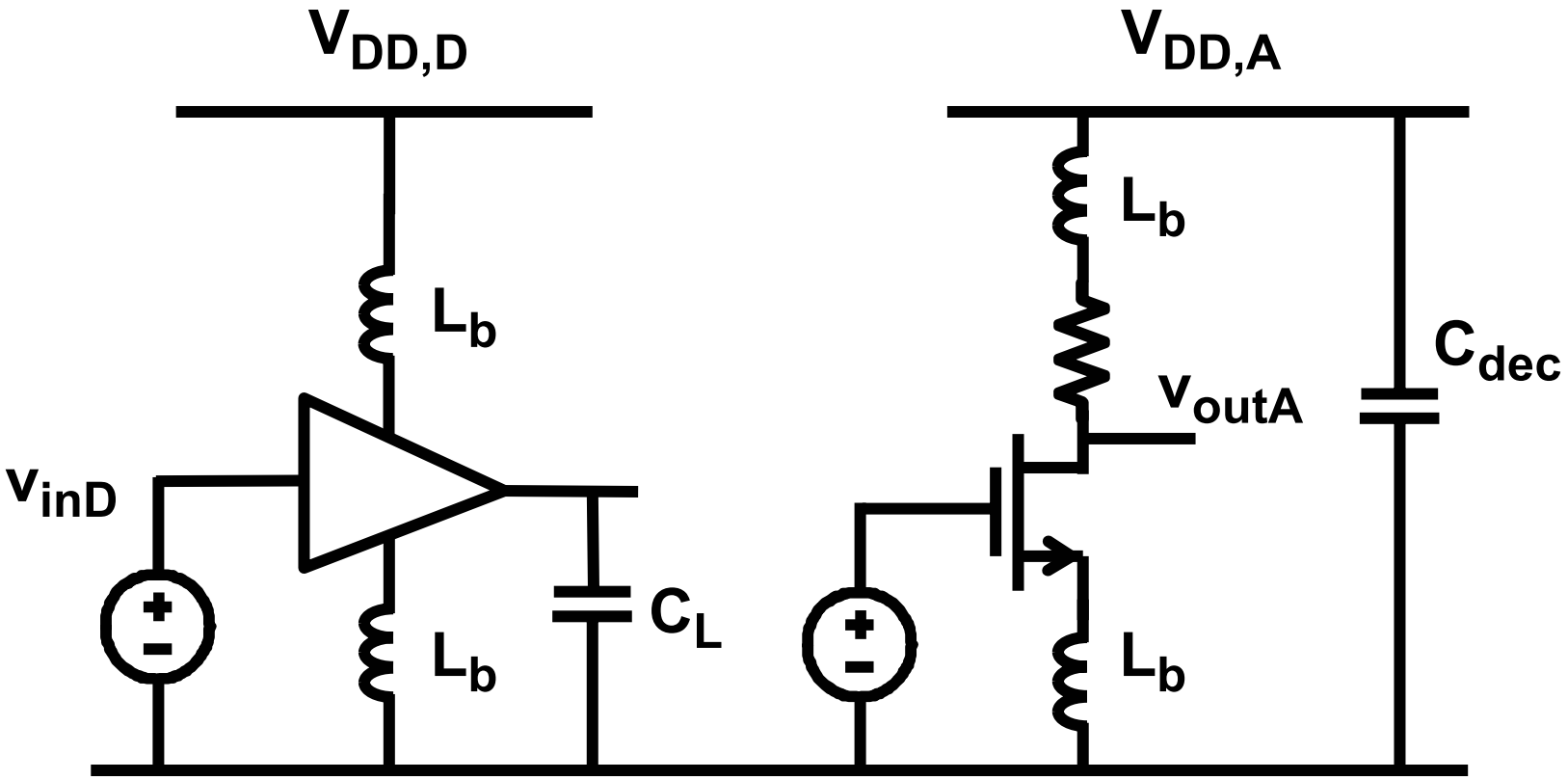
| | |
|---|---|
| 1,2: | 15 nH |
| 10,11: | 4.4nH |

**40 Pin Plastic:**

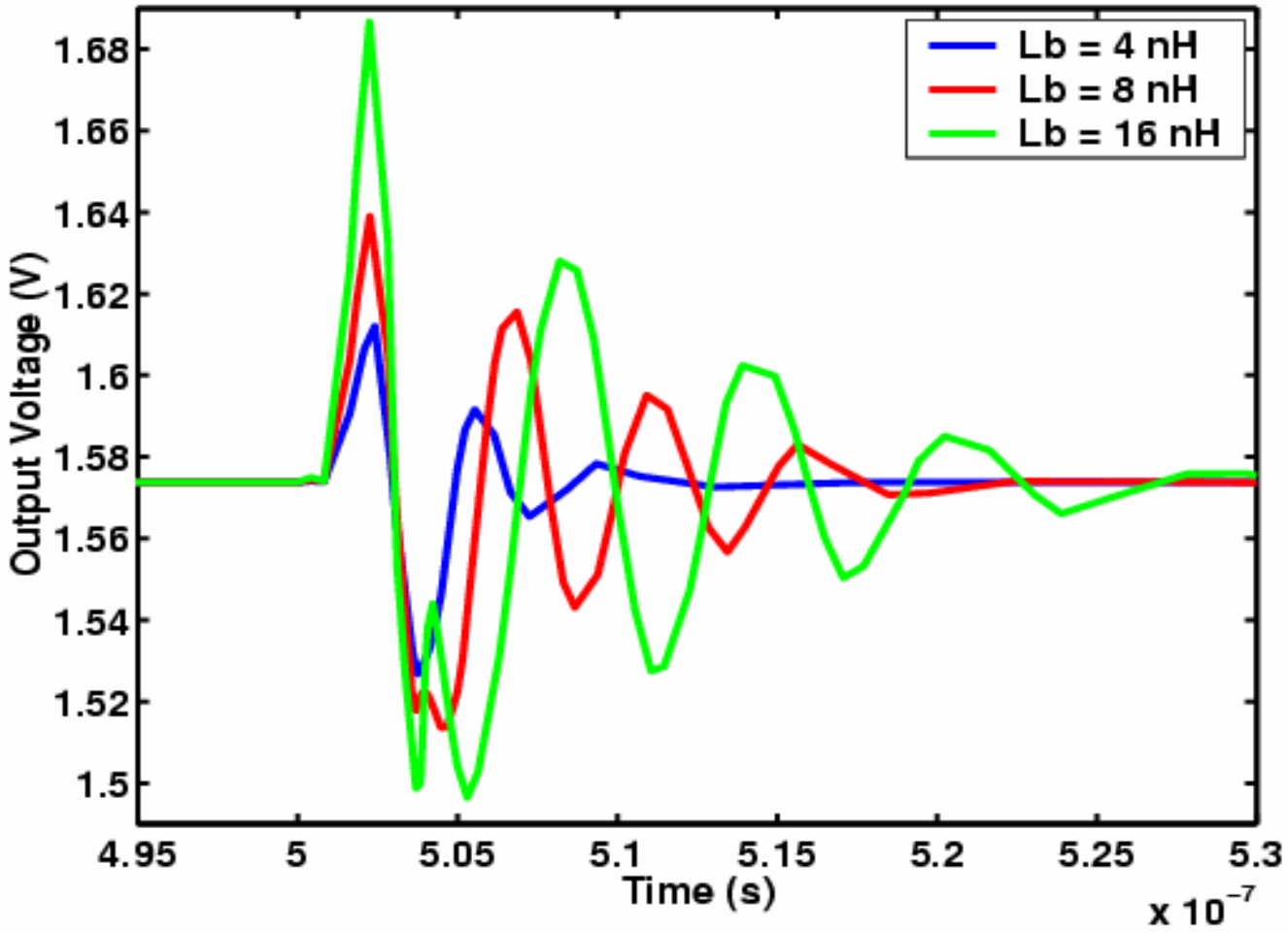
| | |
|---|---|
| 1,2: | 21 nH |
| 10,11: | 9.0nH |

$$\frac{\Delta I}{\Delta t} \approx \frac{10 - 20mA}{1 - 2n\sec} \Rightarrow \Delta V > 500mV$$

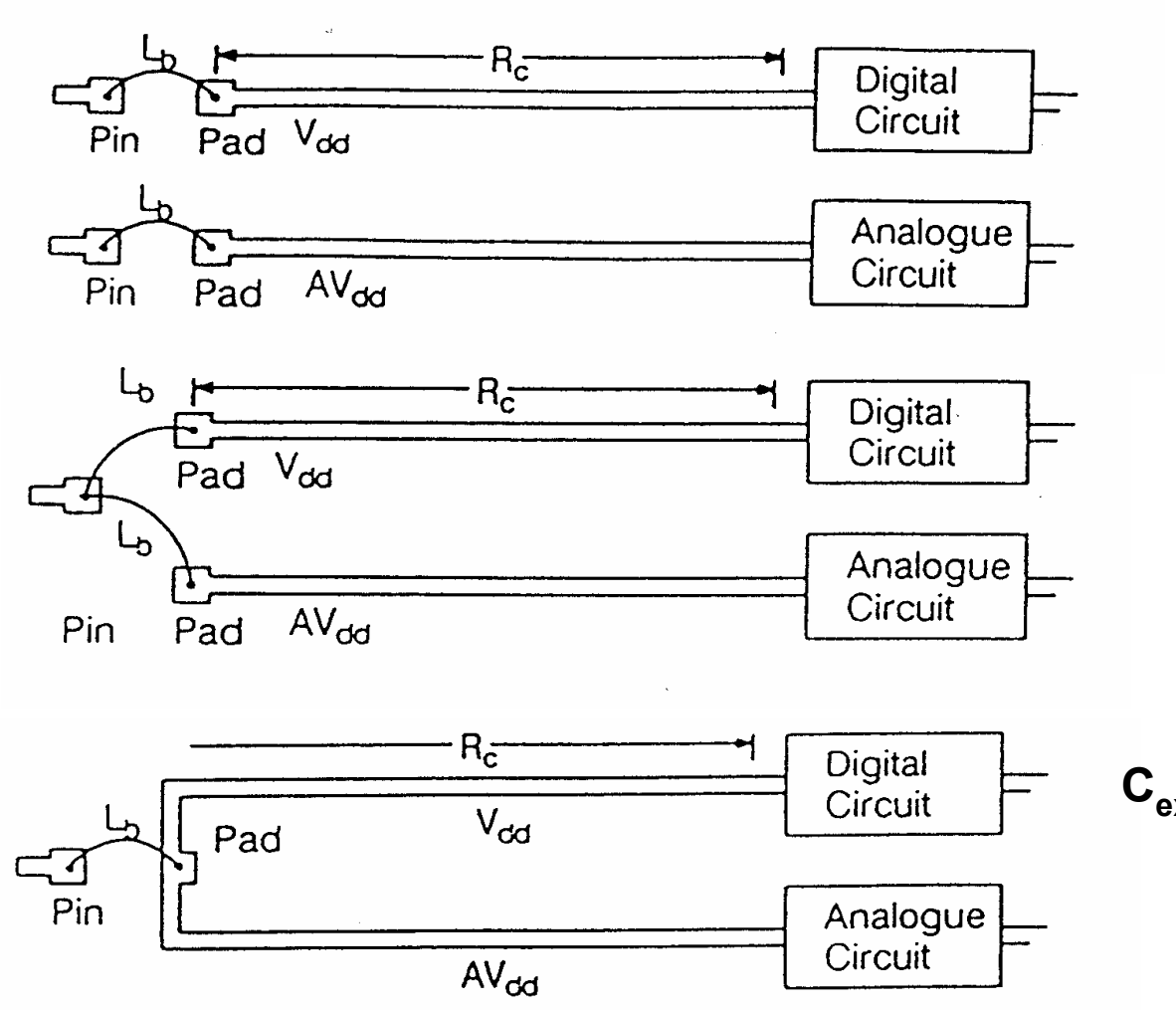
# Supply line bounce (1)



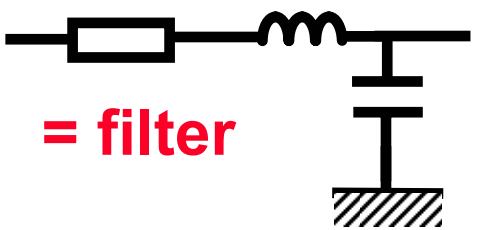
# Supply line bounce (2)

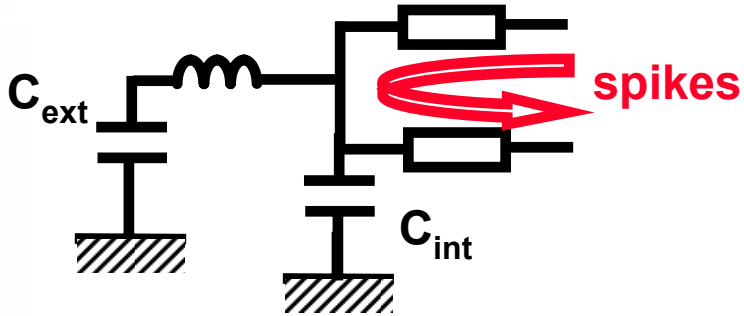


# Pinning Strategy

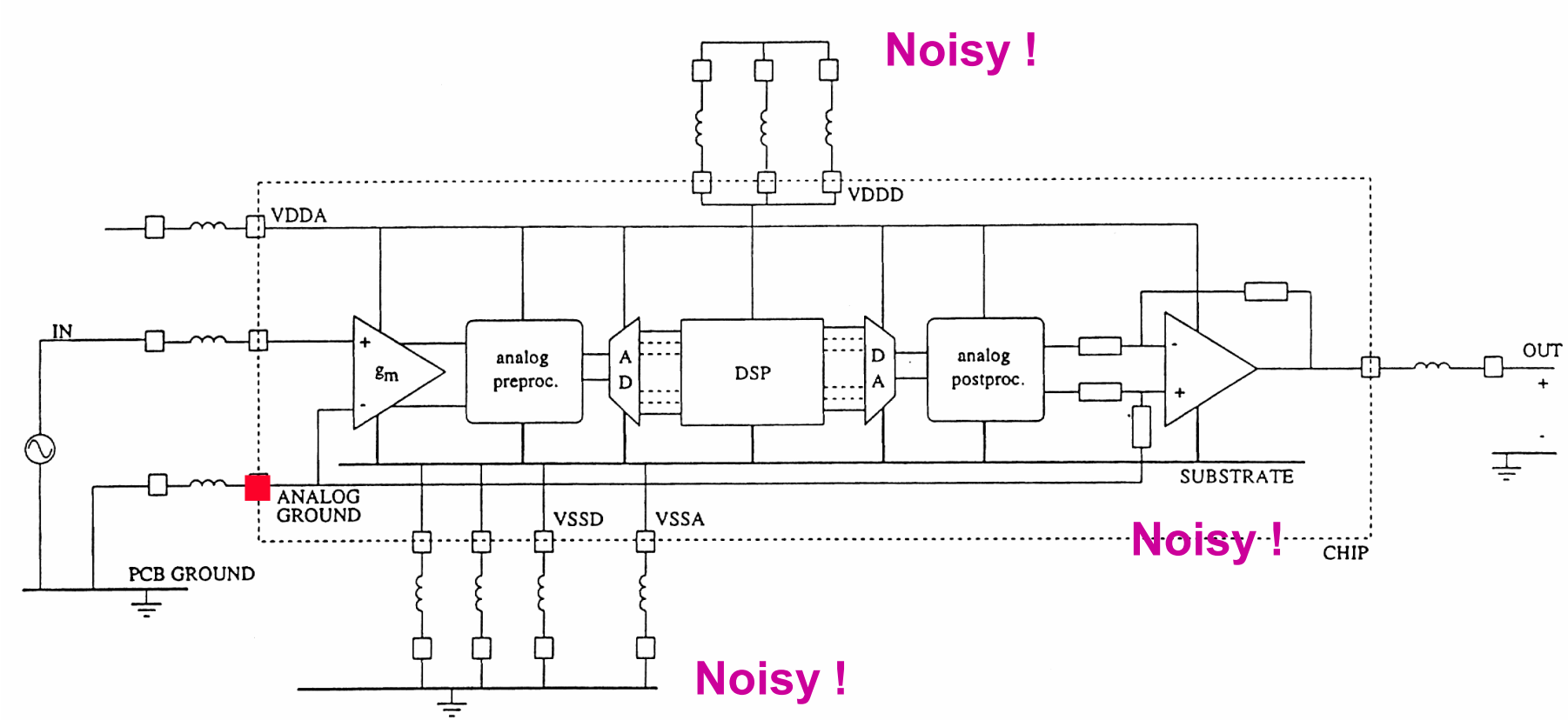



**Best but # pins….**



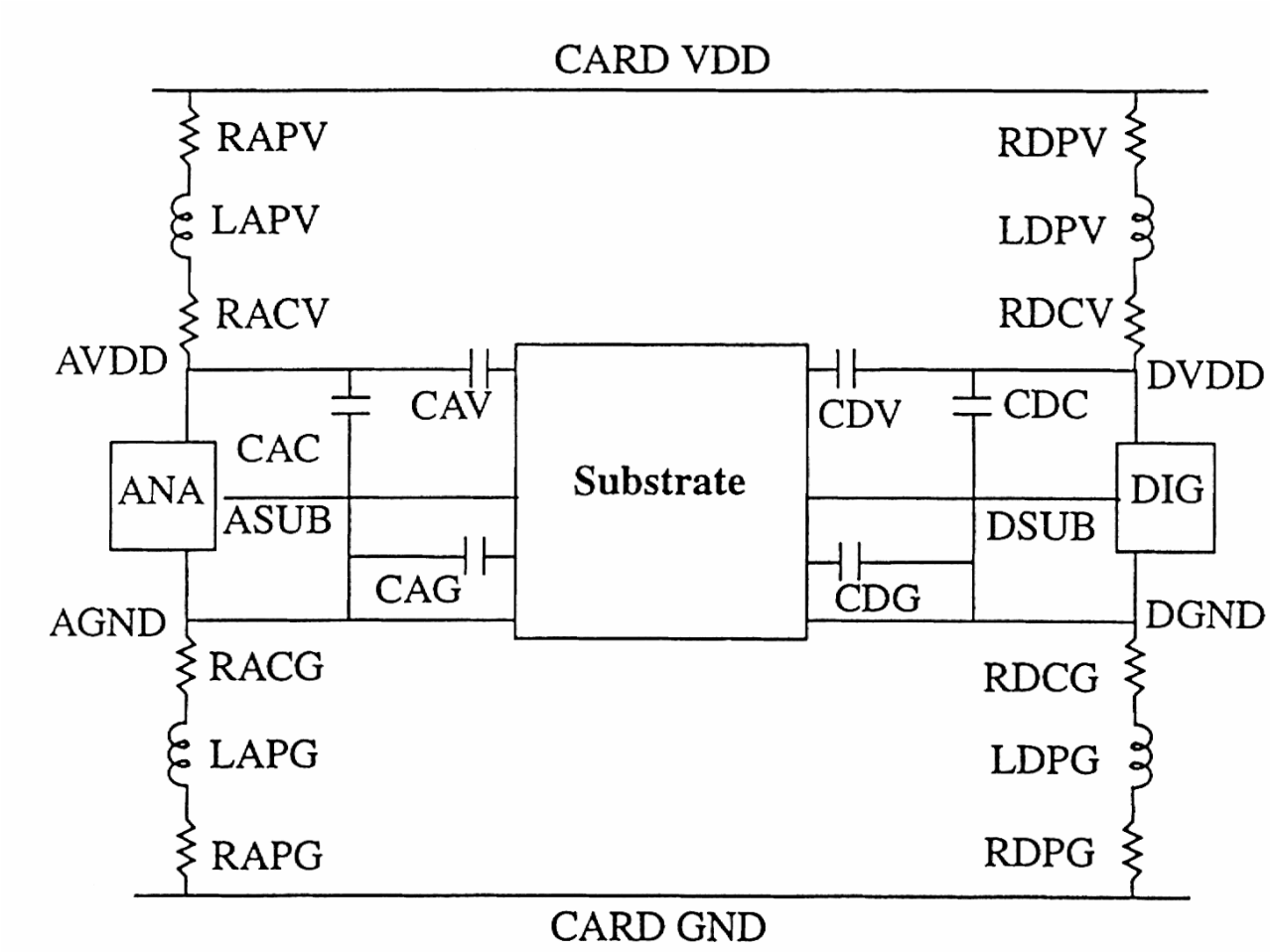
# Supply routing for mixed-signal IC




Clean analog ground

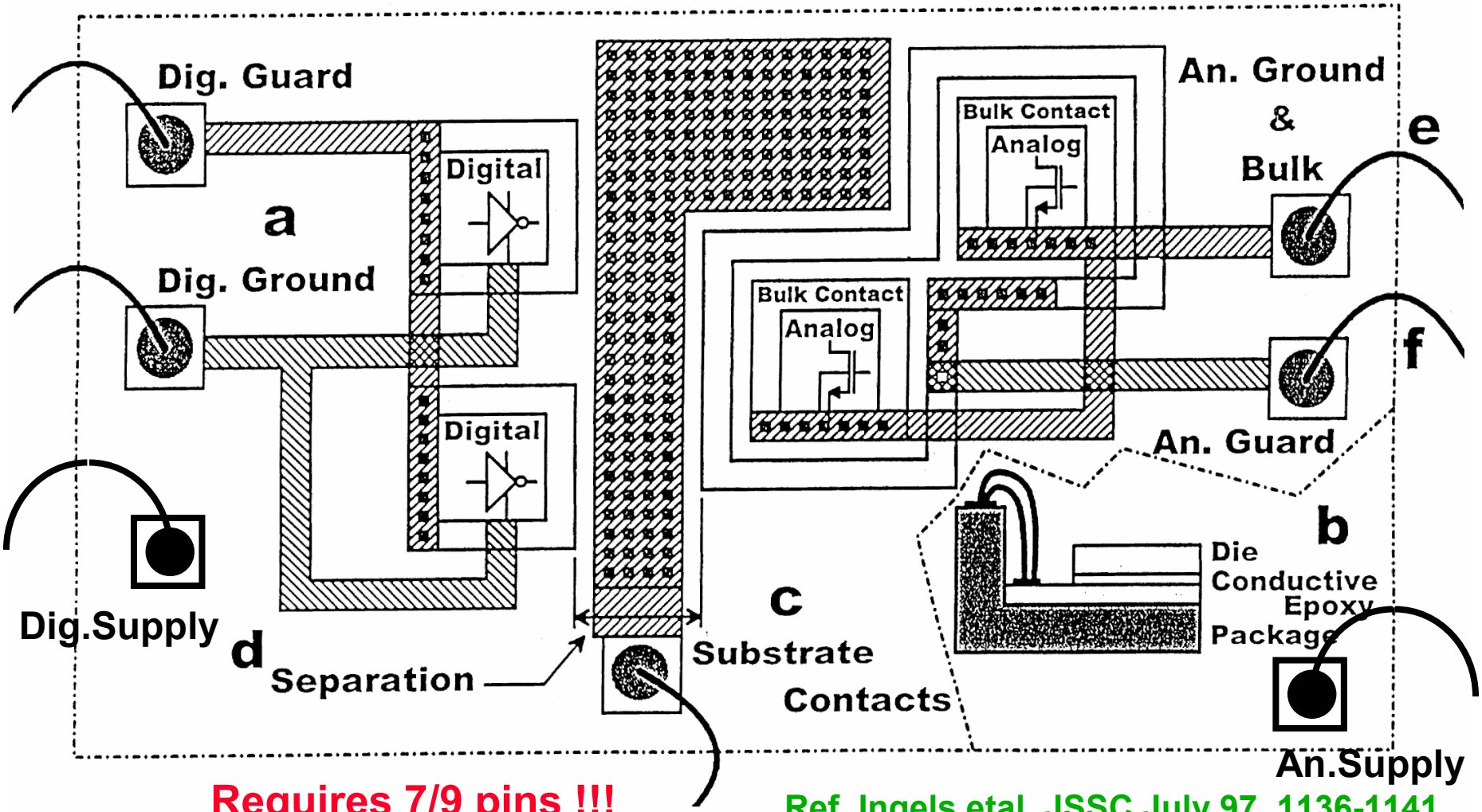
Ref. Nauta, ACD, Huijsing etal,Kluwer 1999, p.165

# Model of parasitics of chip in package




Ref. Verghese, ACD, Huijsing etal, Kluwer 1999, p.246

# Pin connections to A & D




Requires 7/9 pins !!!

Ref. Ingels etal, JSSC July 97, 1136-1141

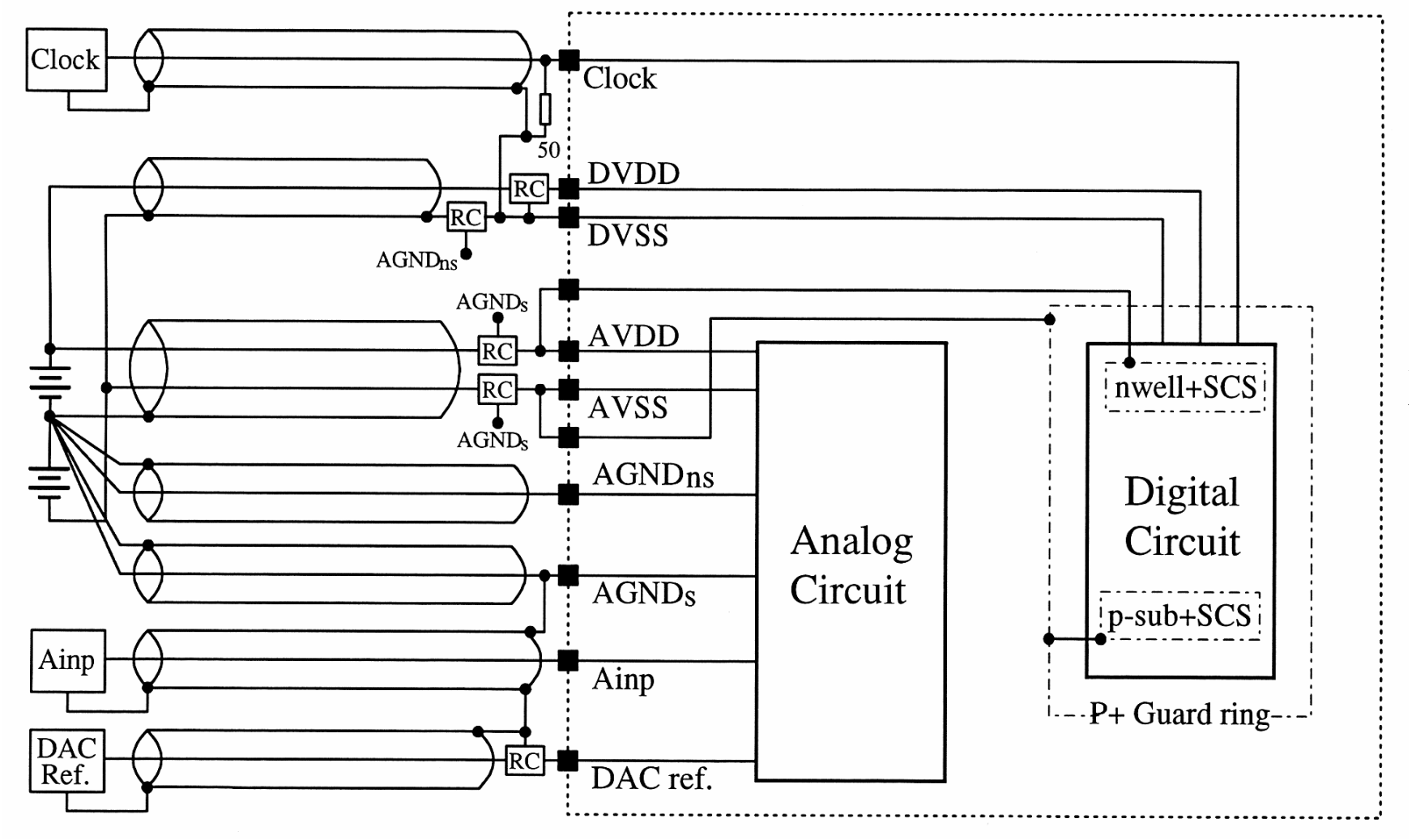
# Rules for pin connections

- The analog and the digital power supply are separated
- The analog ground and the power supply are connected to the outside world with multiple bondwires
- The respective power supplies' bondpads are placed closely to each other to prevent ground loops
- Integrated decoupling capacitors are provided for both the analog and the digital power supplies
- All biasing voltages are internally decoupled to the correct power supply
- The optical input is differential with a dedicated ground bondwire
- The input bondwire is far from the noisy output and power supplies
- A large substrate contact provides a good connection with the heavily doped bulk
- All analog transistors are closely surrounded by substrate contacts that are biased with the analog ground
- All digital transistors are closely surrounded by a guard-ring that is biased with a dedicated clean voltage
- The analog and the digital circuits are separated by a distance that corresponds to approximately 4 times the epi-layer thickness
- A supplemental guard-ring biased with a dedicated voltage is provided between the analog and the digital subcircuits.

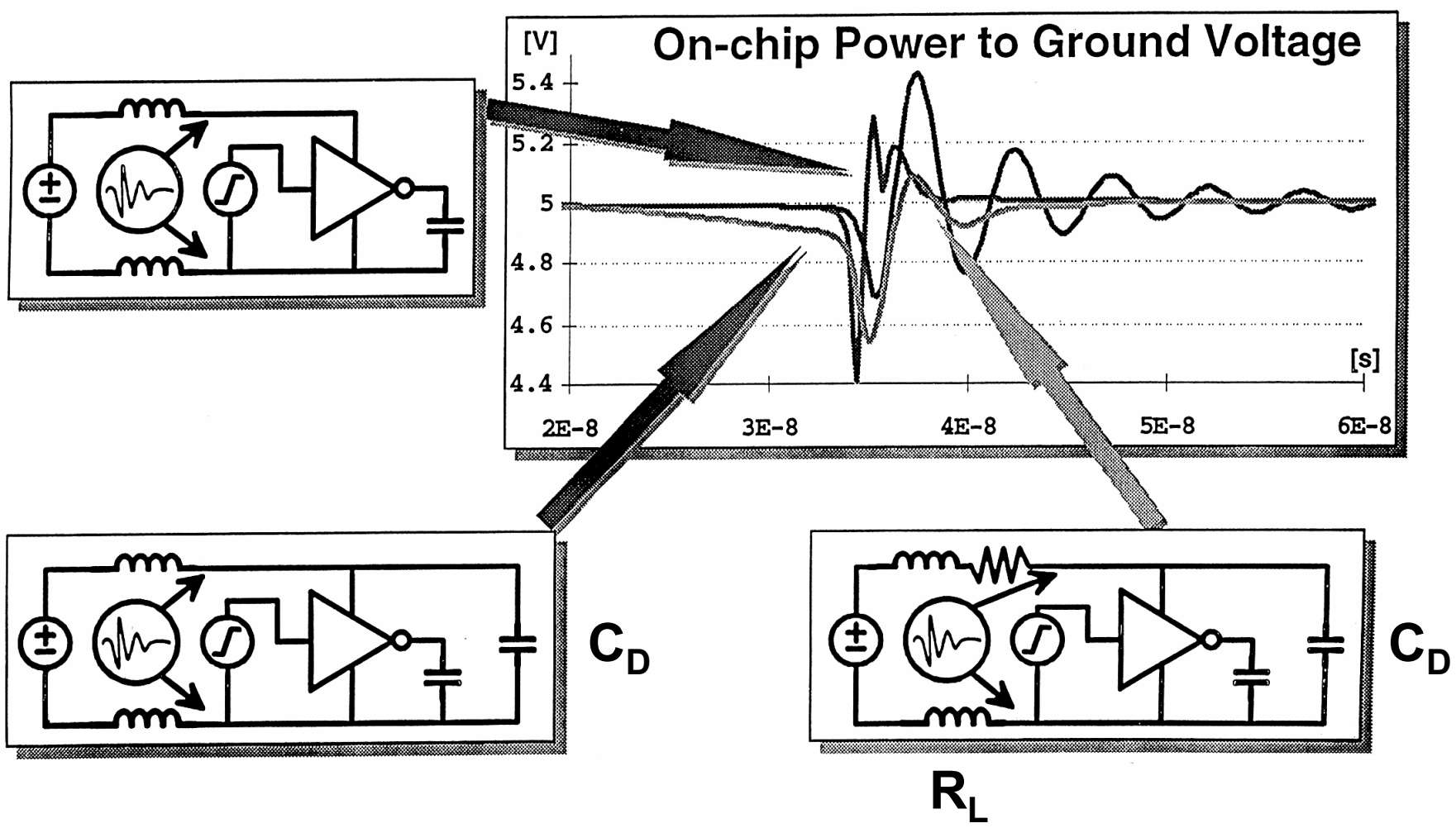
# Noise reduction techniques

- At noise sources side
  - Reduce substrate noise generated by the cells, Switching activity reduction techniques
  - Switching activity spreading techniques
- At noise receiver part
  - Design techniques (fully differential design, etc …)
  - Layout techniques (fully differential implem. …)
  - Separate, and multiple, supply bonding pads
  - Guard ring close to the transistors
  - Buried layers under the transistors
  - On chip decoupling capacitances

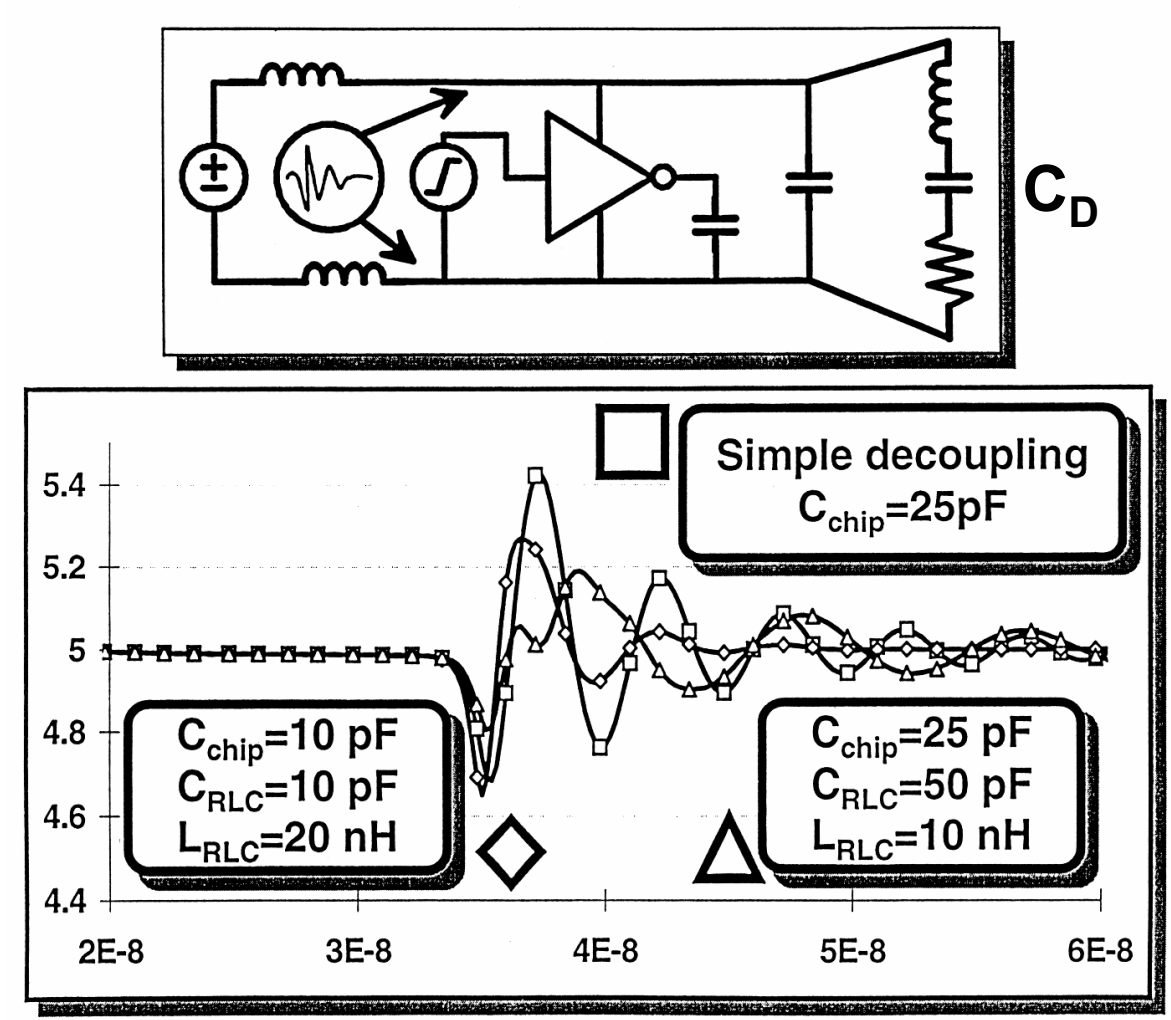
# Measurement set-up for MAD ADC



# On-chip decoupling



# Resonant frequency decoupling




**Tune LC circuit on the clock frequency !**

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

# Outline

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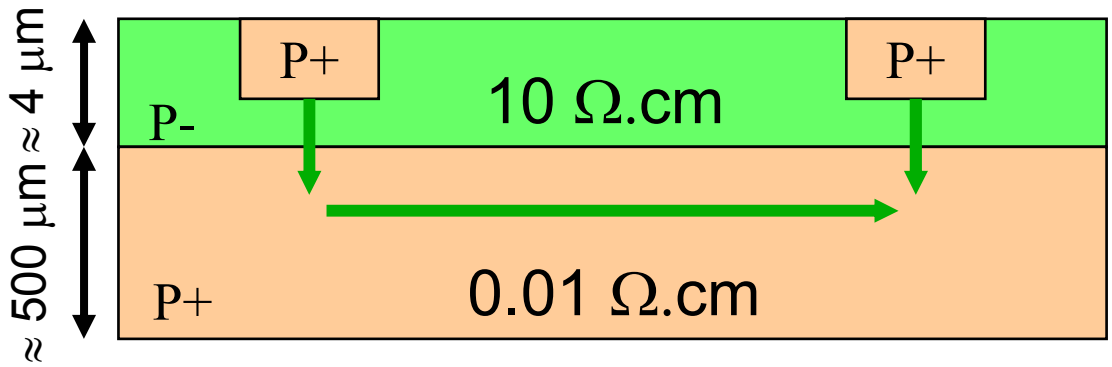
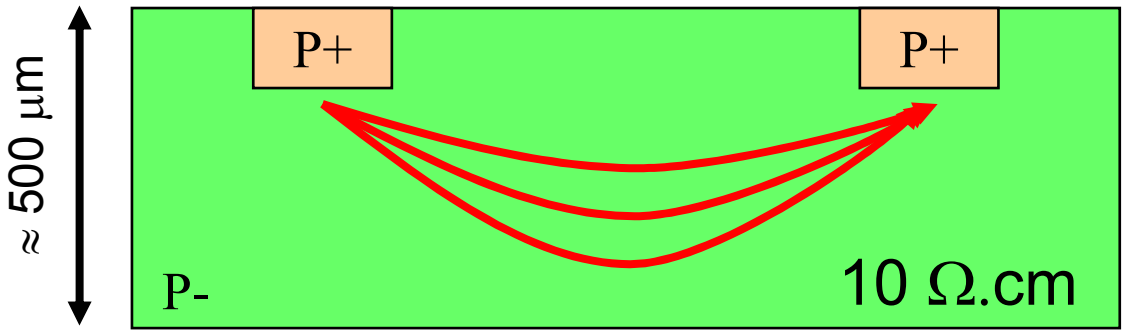
# Substrate Type Influence



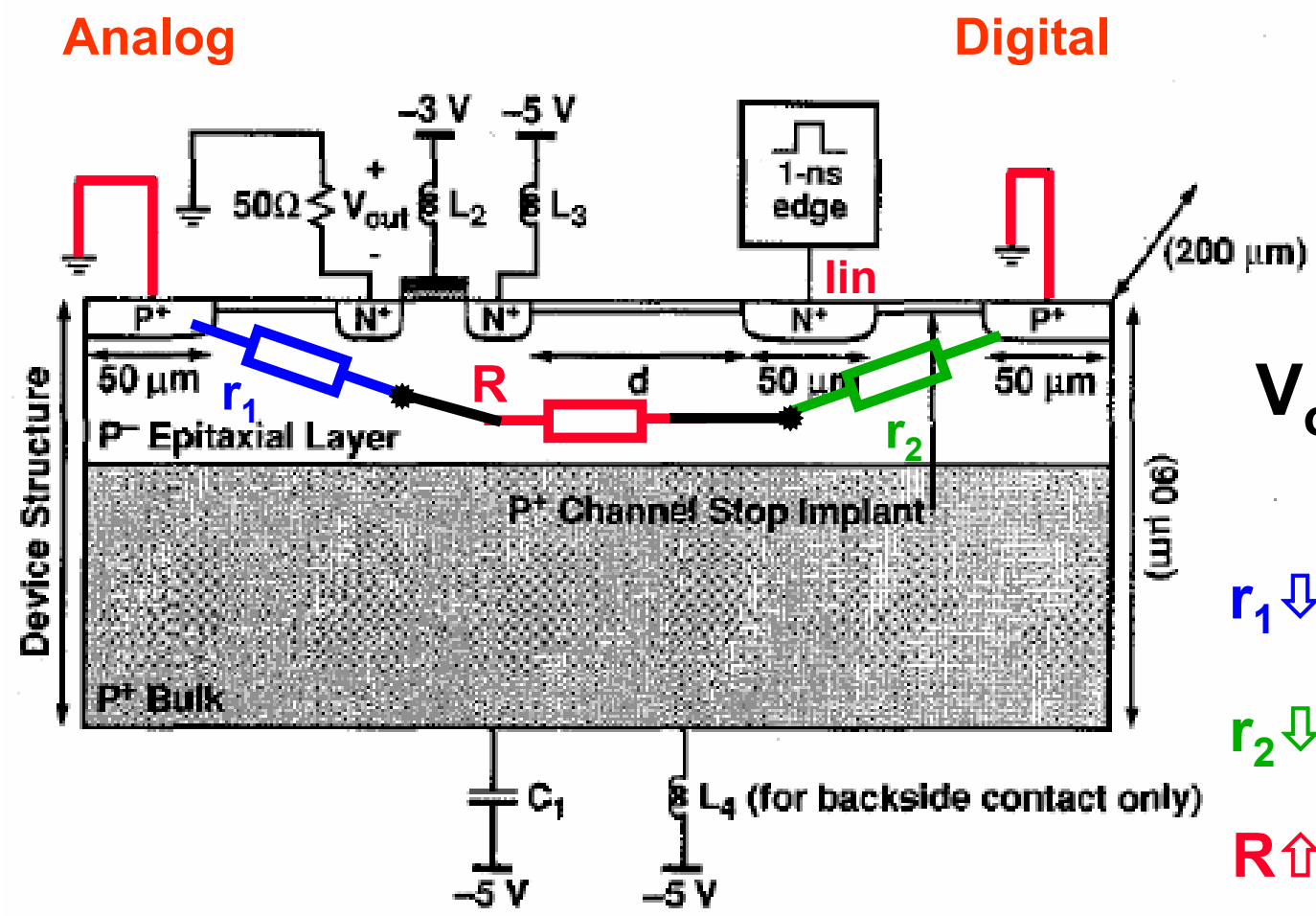




**Heavily doped substrate with epi – layer**

**Distance between p+ islands > 4 x epilayer thickness => coupling independent of distance**

**Lightly doped substrate (high resistivity)**

# Substrate Coupling




$$V_{out} \approx \frac{r_1 r_2}{R} I_{in}$$

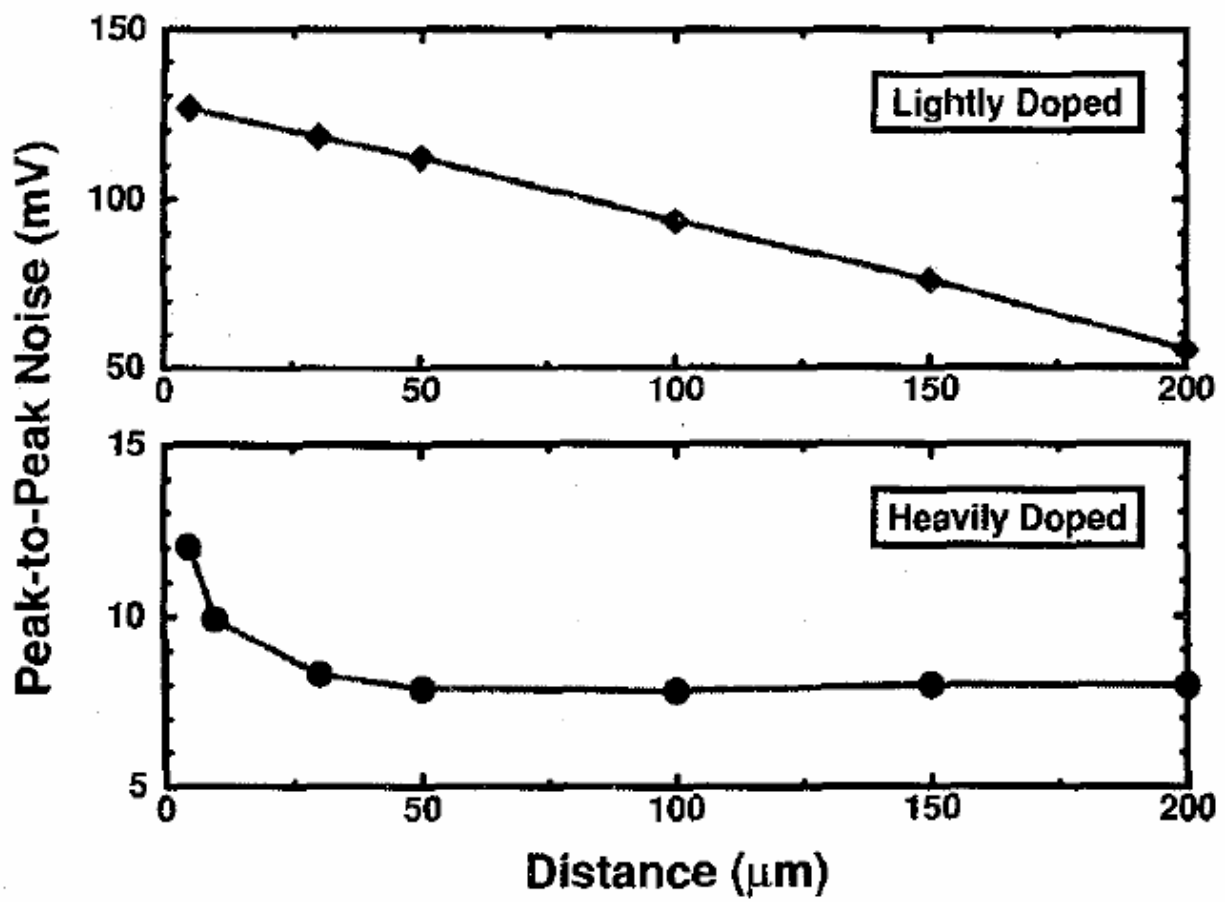
$r_1 \Downarrow$ : Analog Substrate contact

$r_2 \Downarrow$ : Digital Substr. cont.

$R \Uparrow$ : distance $\Uparrow$

Ref.Su , JSSC April 1993, pp.420-430

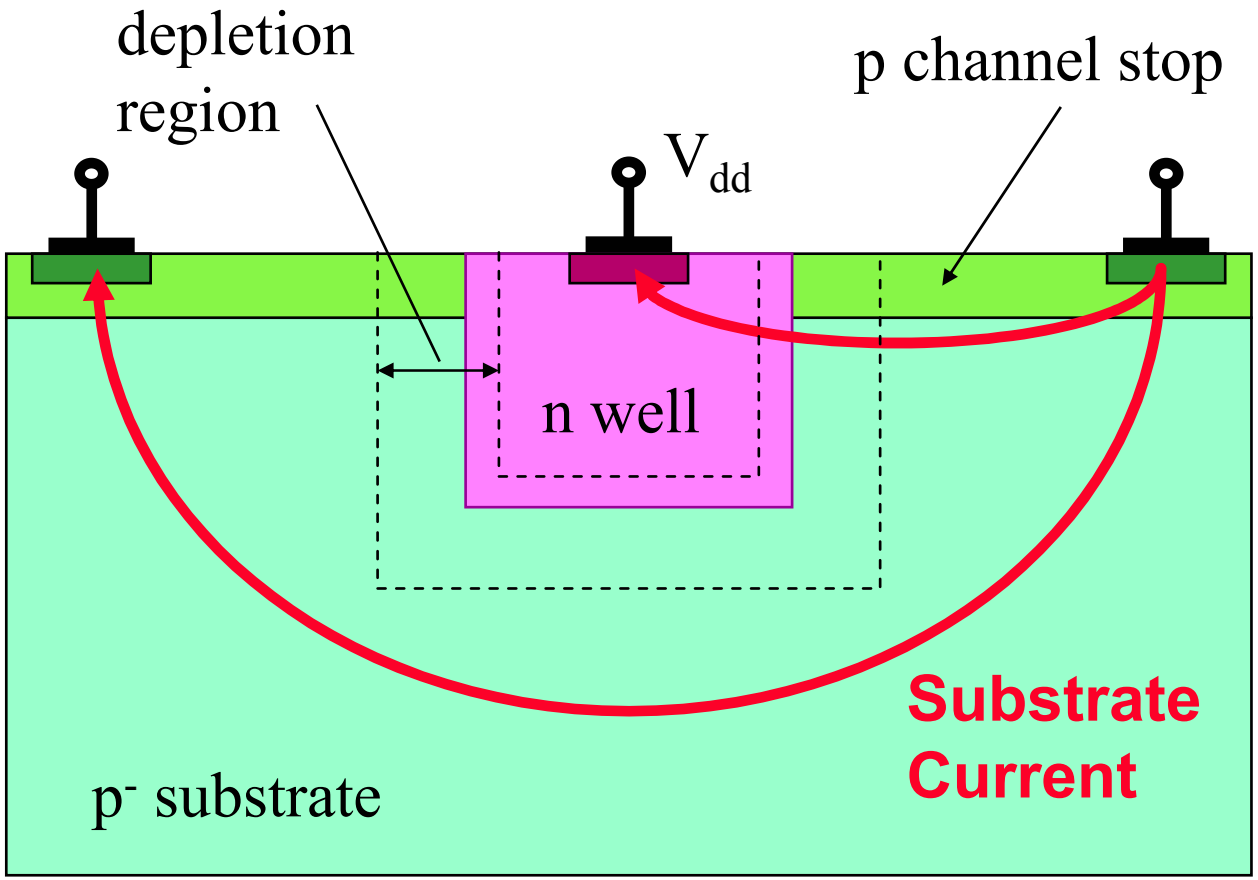
# Distance ?




**Substrate**

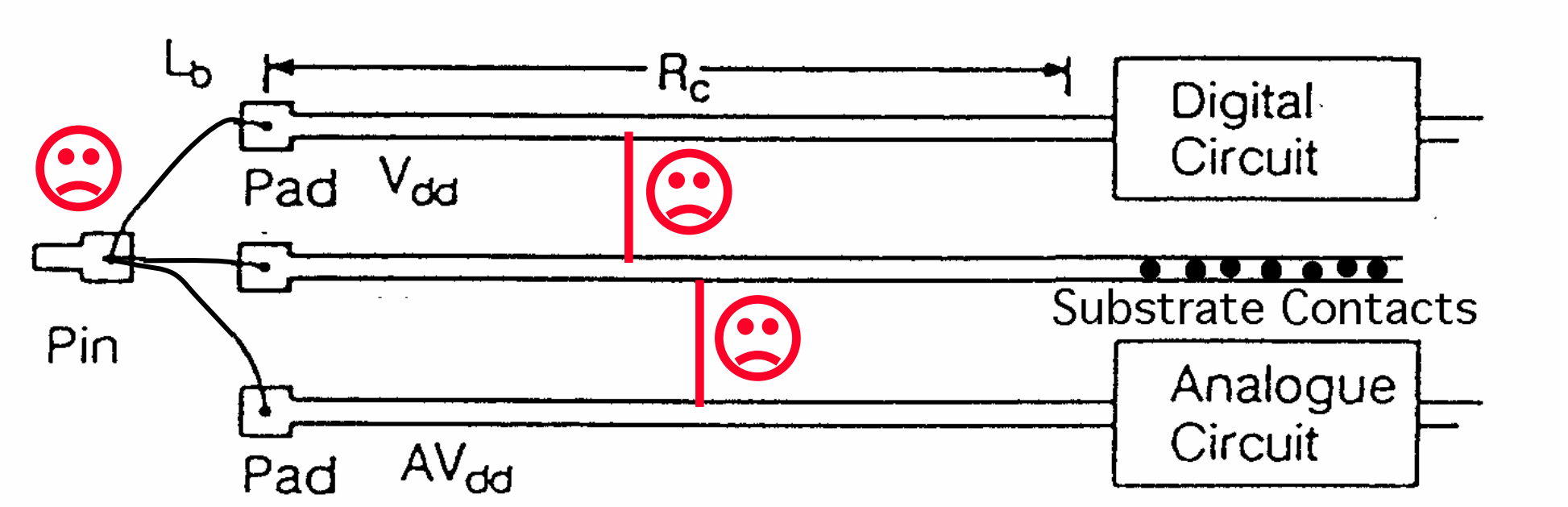
**Distance ≈**
**4 x Epi-thickness**

# Low-n well breaks the surface channel

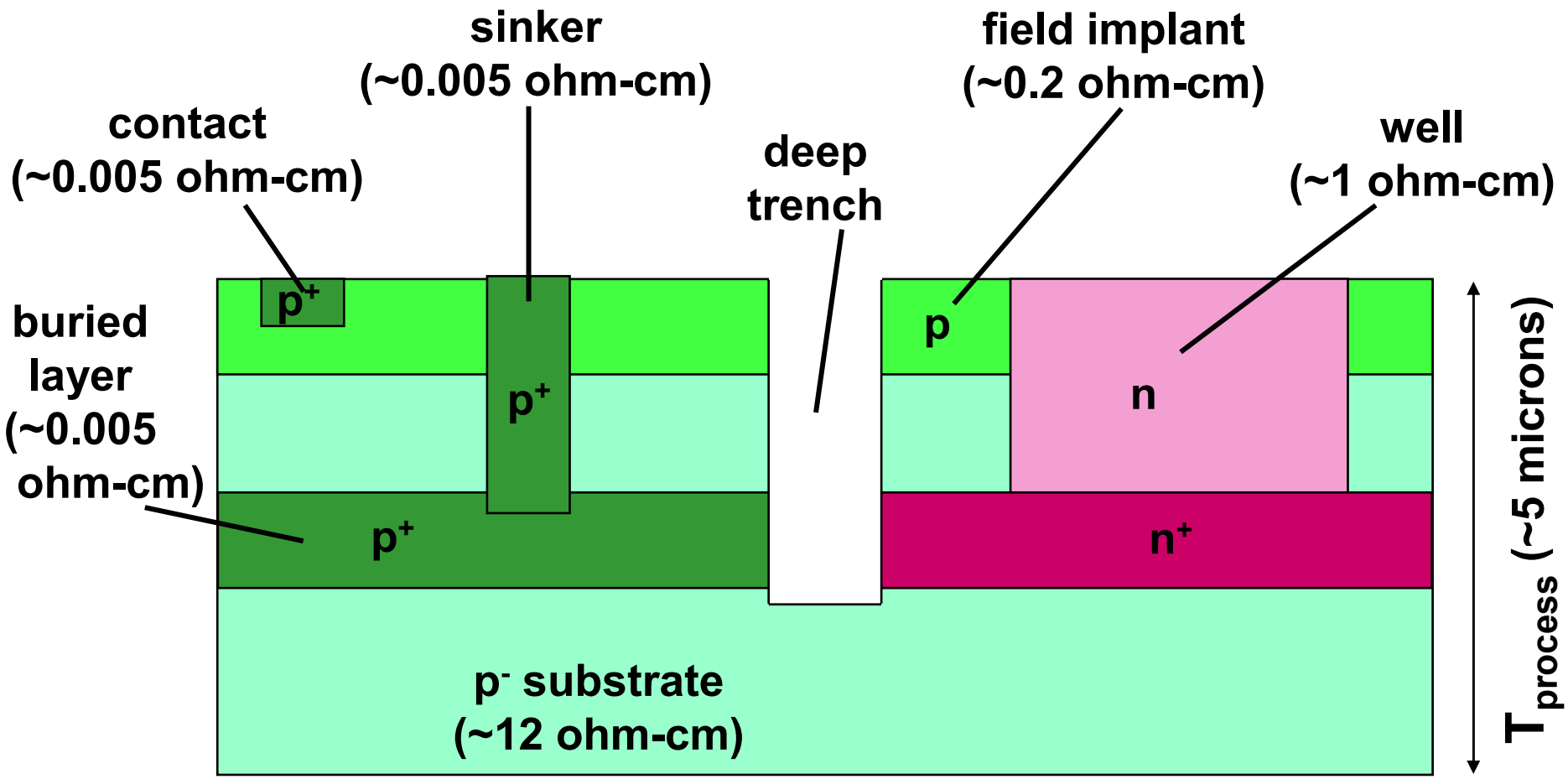



Ref.Clement , ACD Kluwer 1999, p.189; @Simplex

# Separate Bondpads

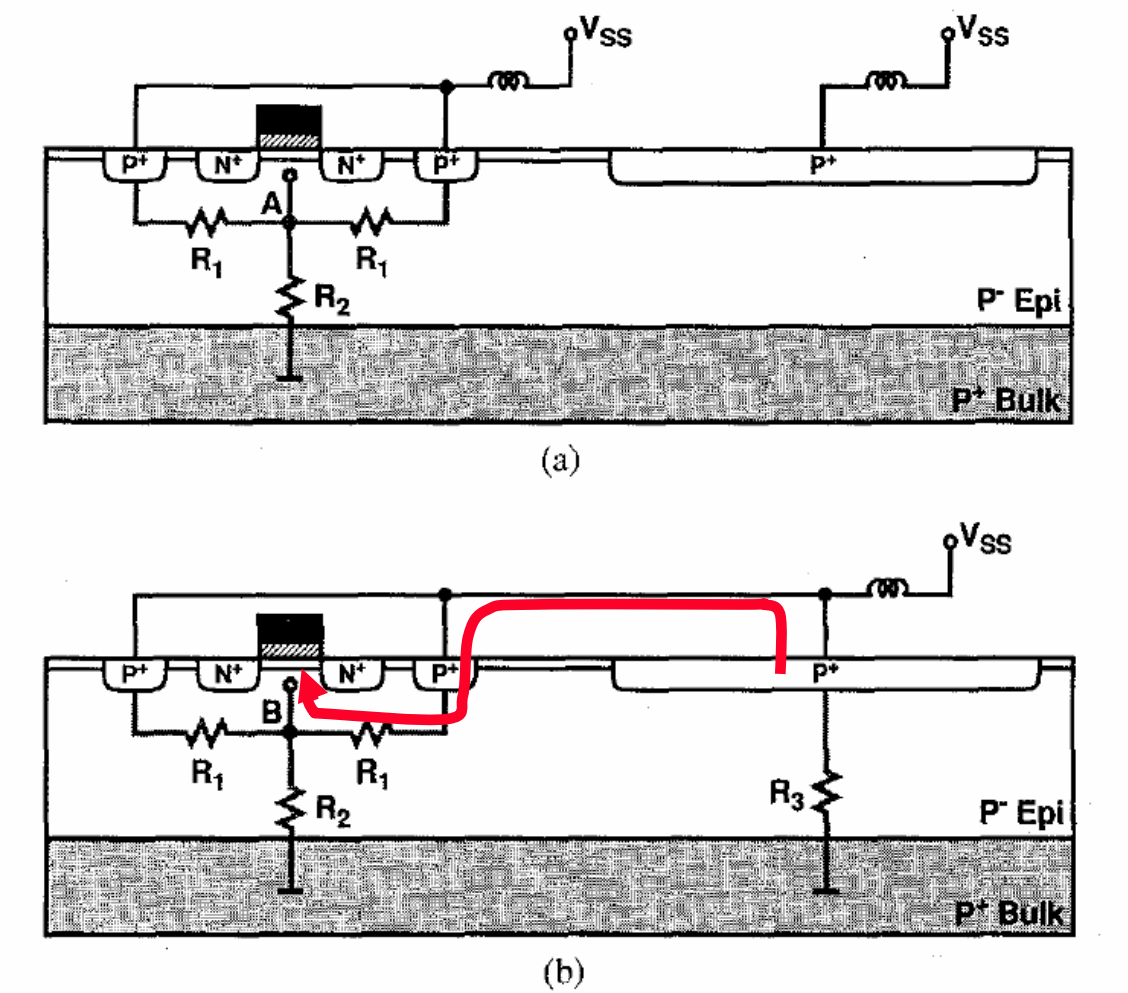


# Process parameters for low coupling



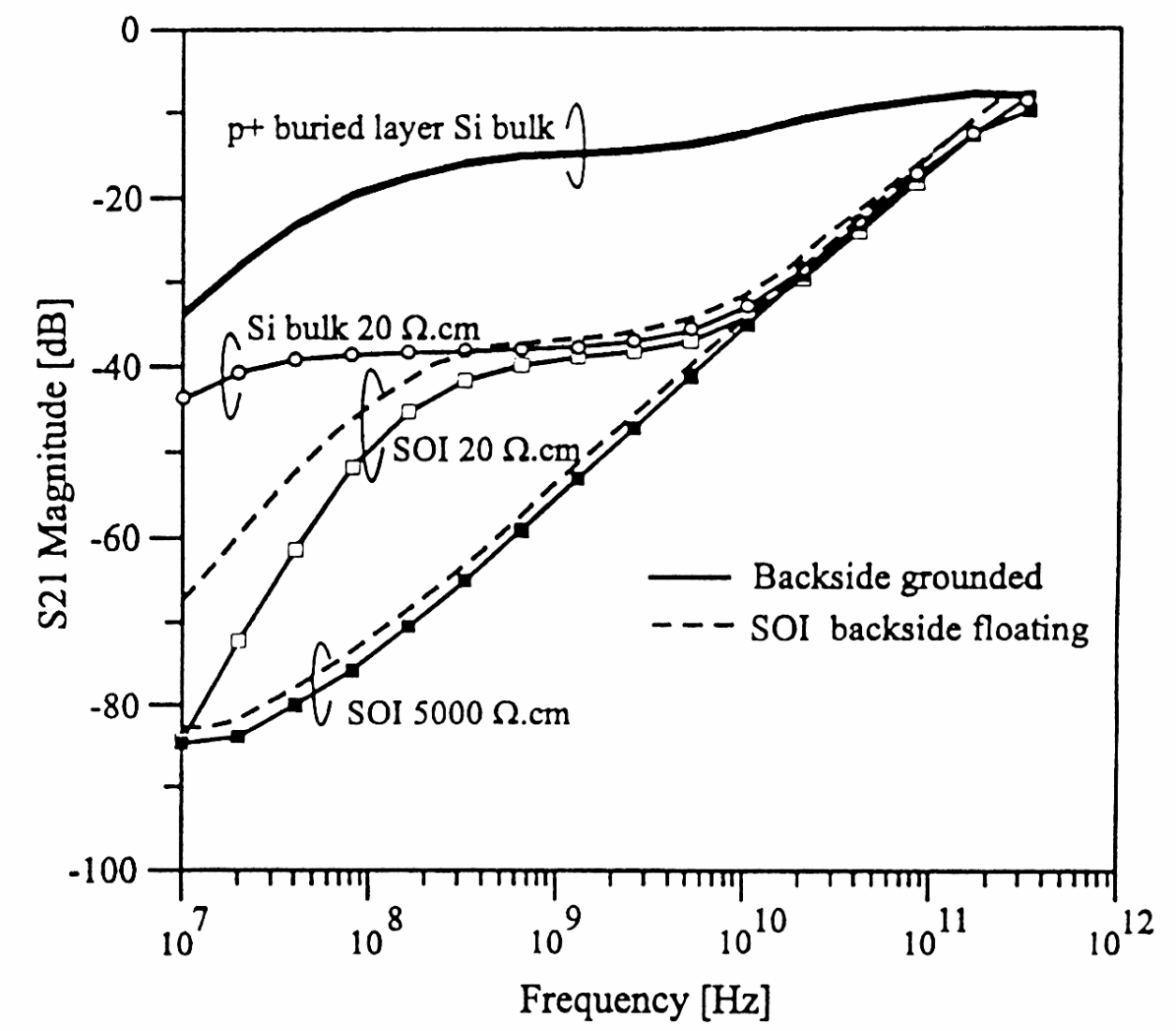

Ref.Clement , ACD Kluwer 1999, p.189; @Simplex

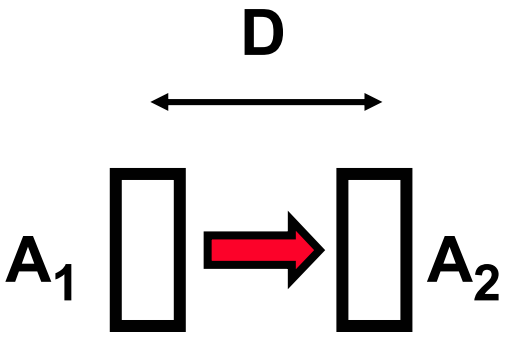
# Different Bondpads for Guard Rings




P+ bulk is single node

# Coupling on SOI substrates




$$C_c \approx \frac{\varepsilon_{ox} A_1 A_2}{2 \pi D^3}$$

UCL, 1999

# Outline

- Circuit noise generation
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  - Power supply pinning
  - Substrate coupling
  - Circuit placement
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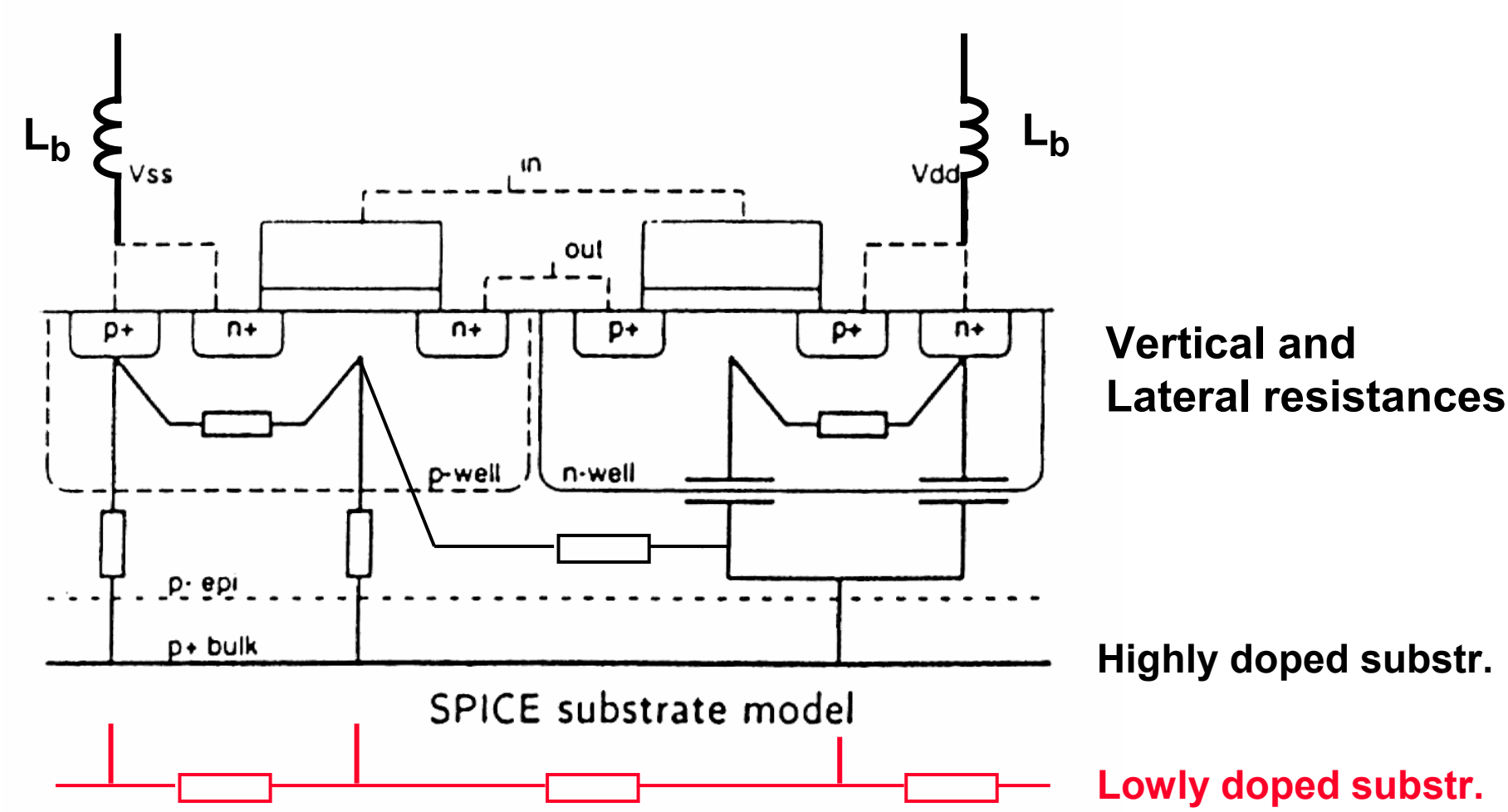
  - PSRR

# Switching noise measurements : model



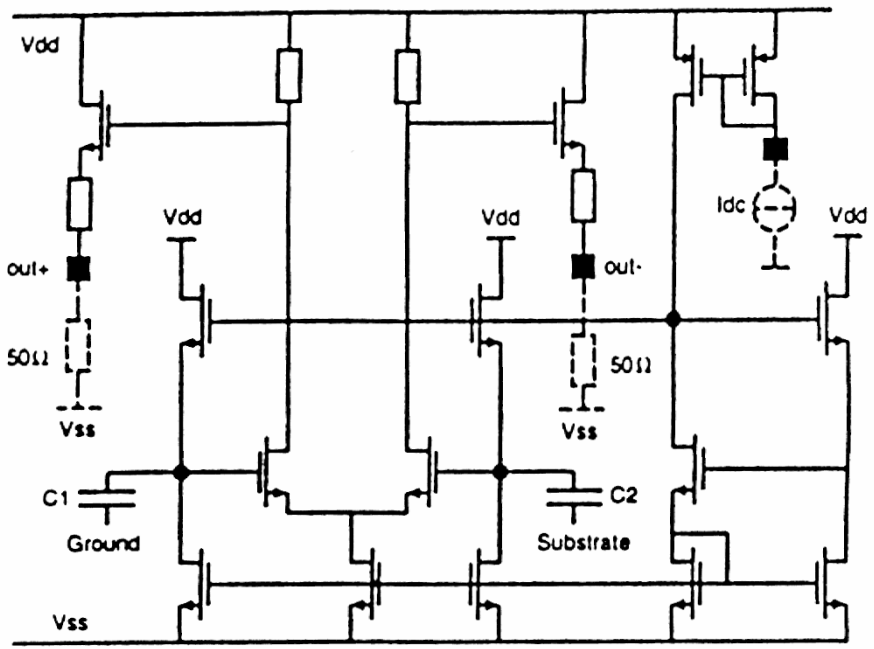

Vertical and
Lateral resistances

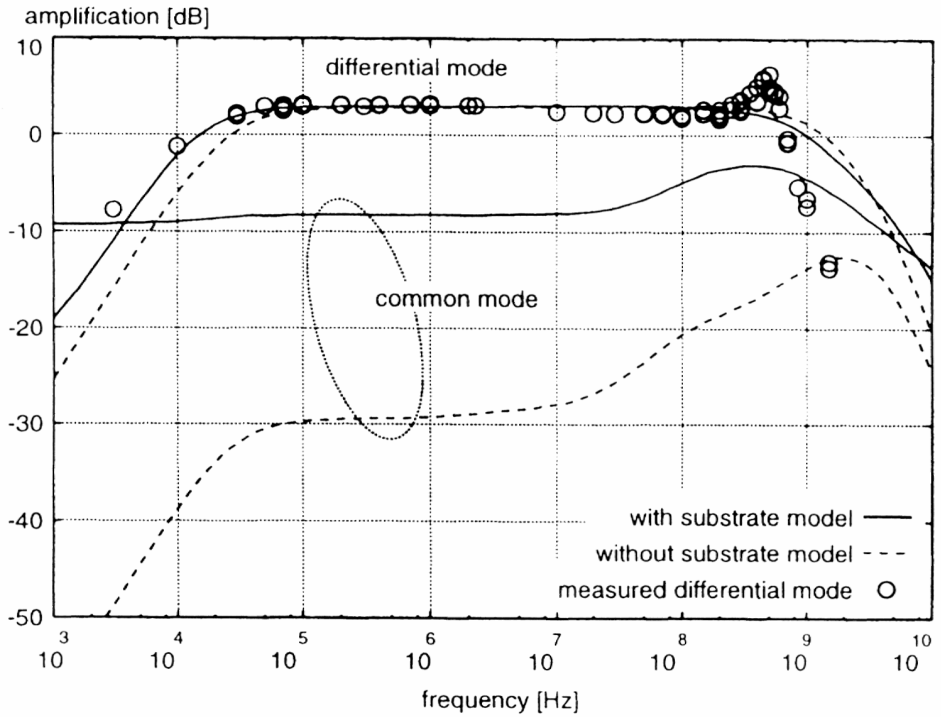
Highly doped substr.

Lowly doped substr.

Van Heijningen,etal. JSSC July 2000, pp.1002-1008

# Switching noise measurements: preamplifier



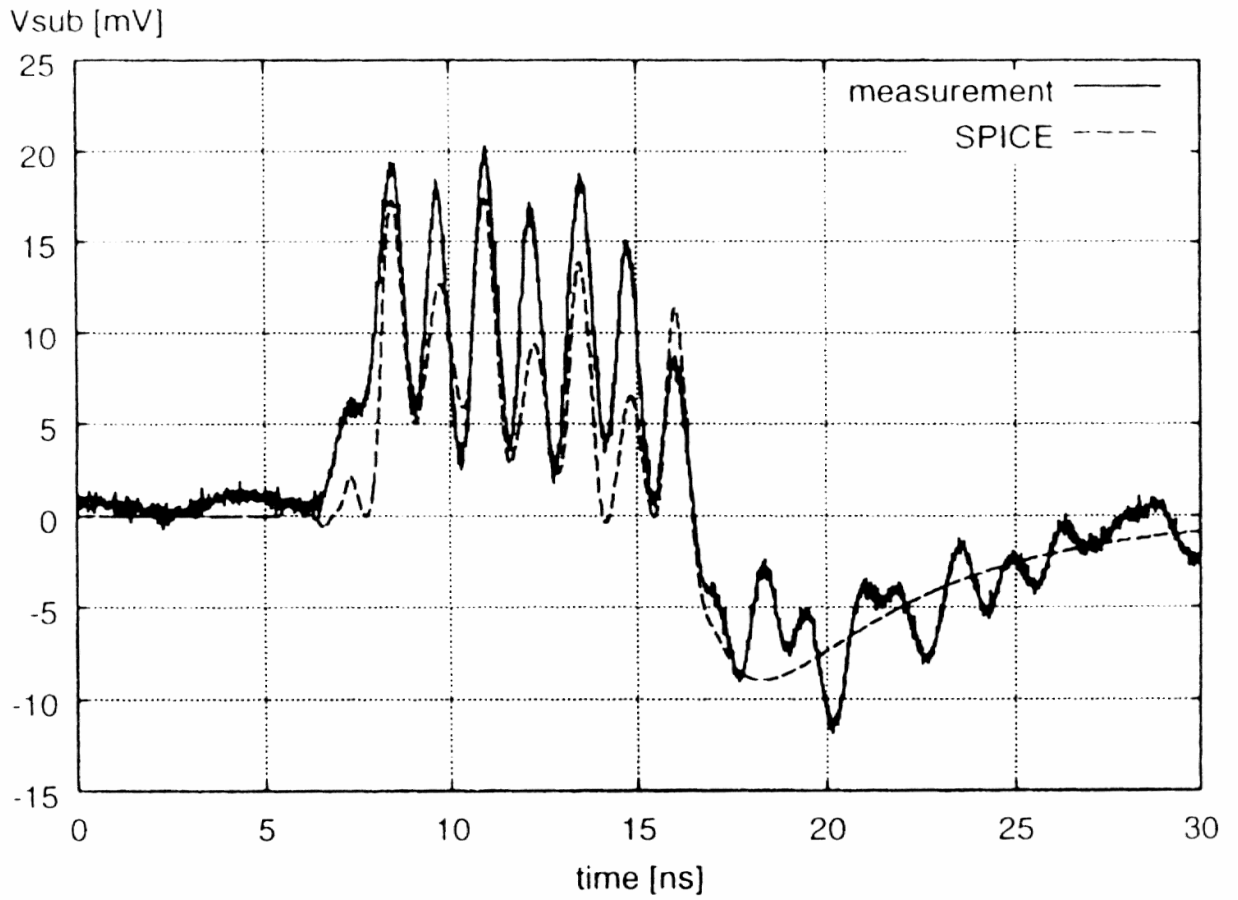




**Input = Substrate**
**3V, 32 mA**
**GBW ≈ 500 MHz**

**Low CMRR**
**because substrate effects**

Van Heijningen,etal. JSSC July 2000, pp.1002-1008

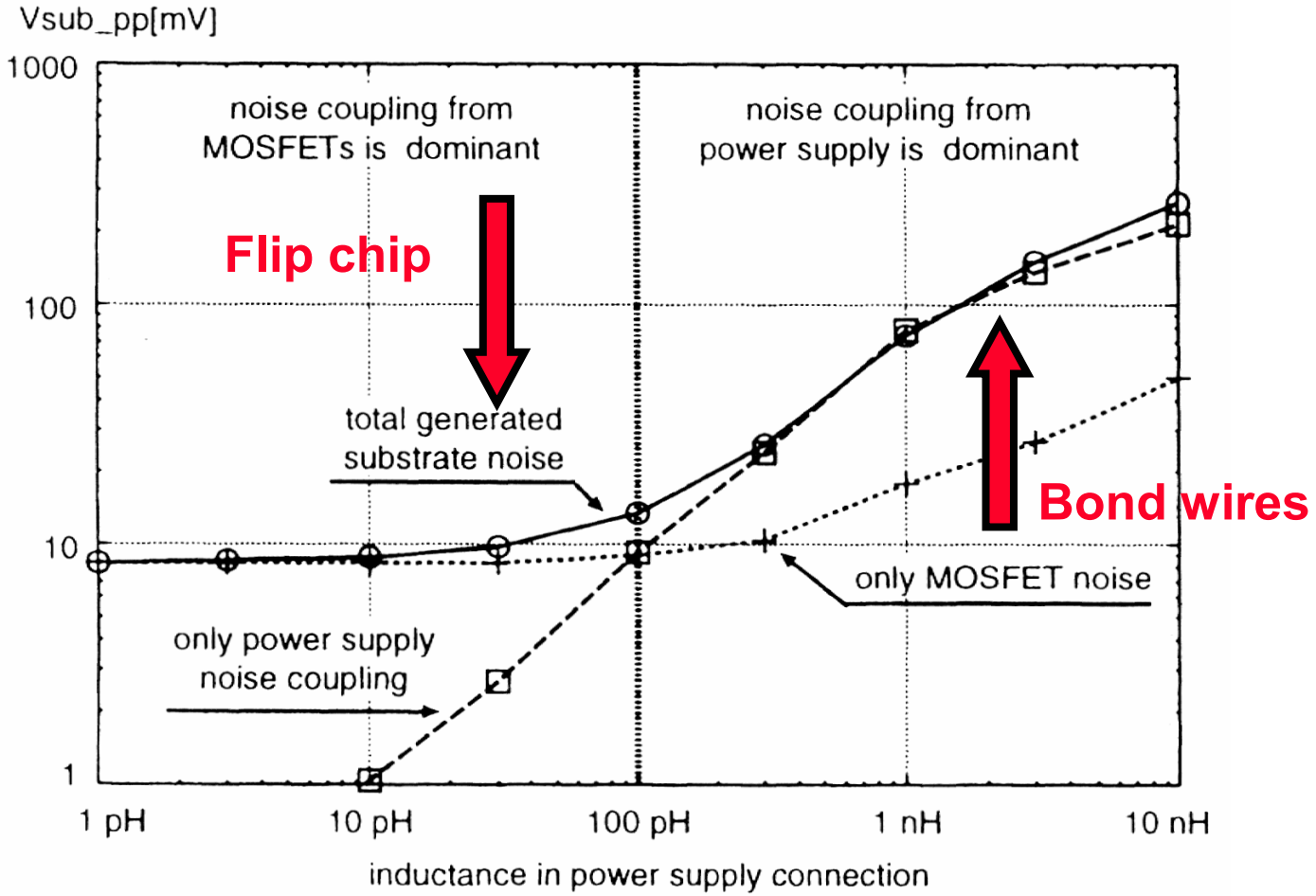
# Switching noise measurements: coupling data




**Caused by 7-stage Ringoscillator : 800 MHz**

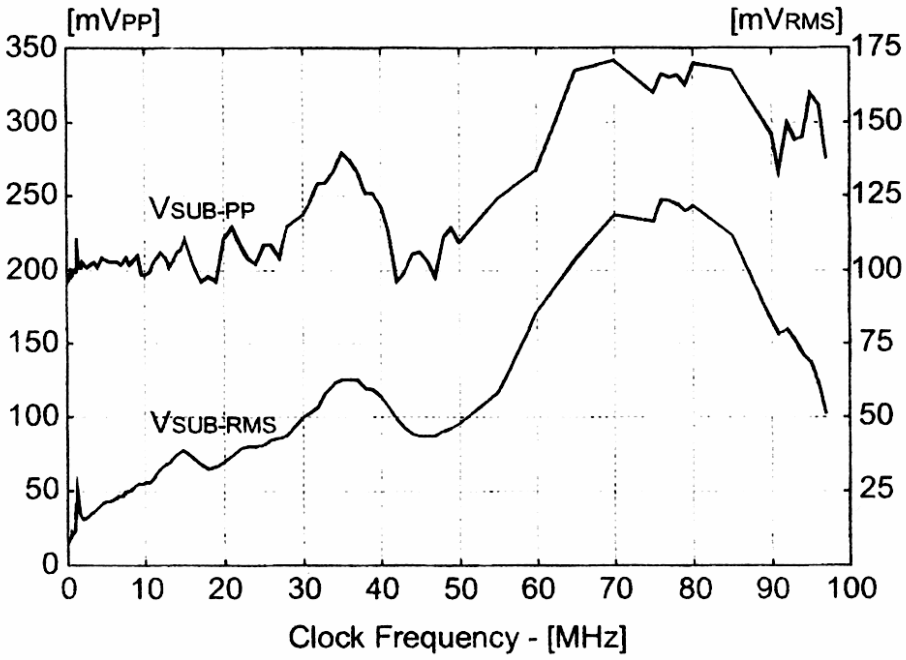
Van Heijningen,etal. JSSC July 2000, pp.1002-1008

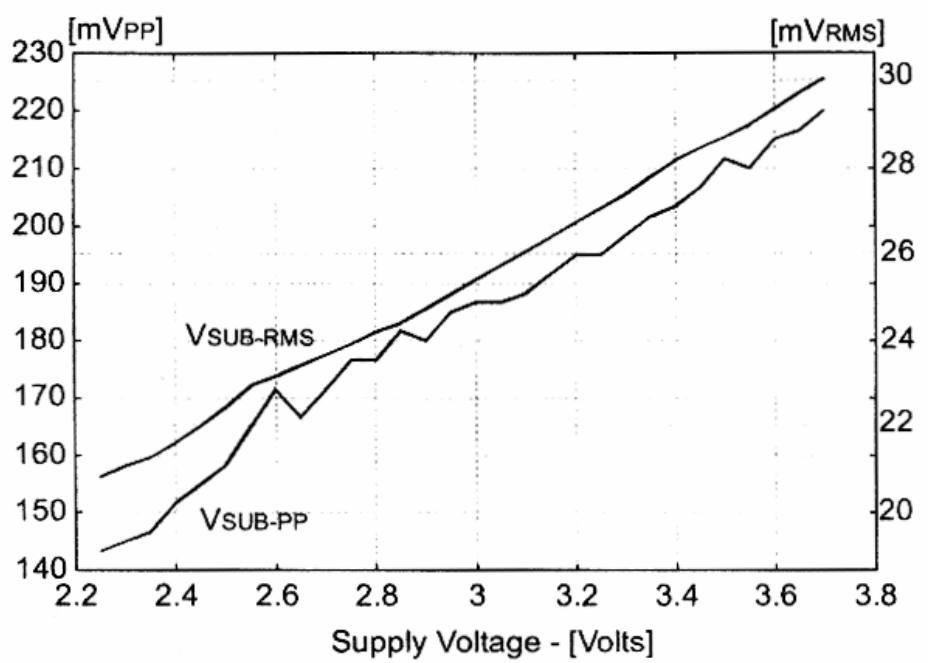
# Switching noise measurements: bonding




Van Heijningen,etal. JSSC July 2000, pp.1002-1008

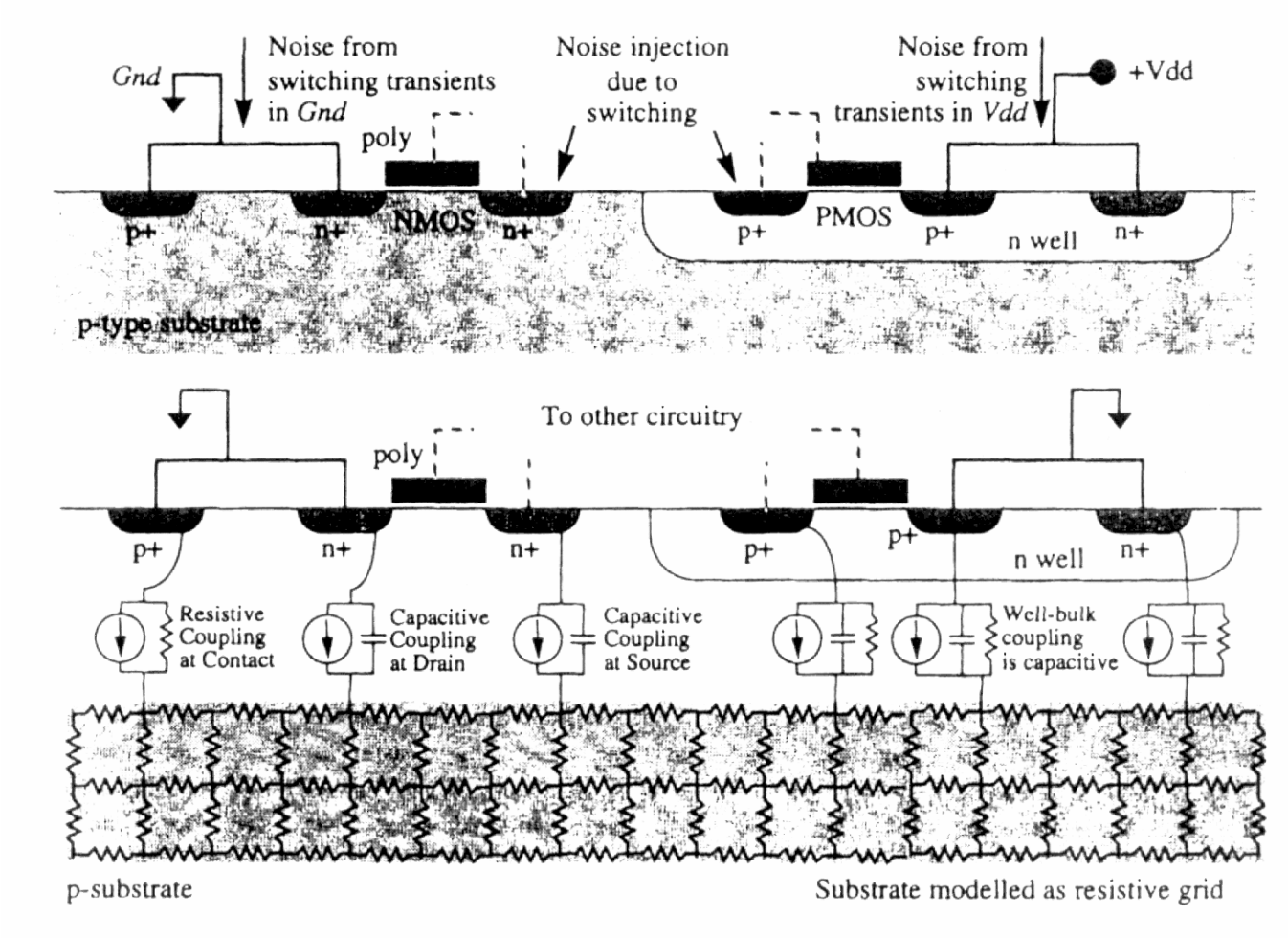
# Generation of substrate noise in SoC




Badaroglu, etal. JSSC July 2003, pp.1250-1260

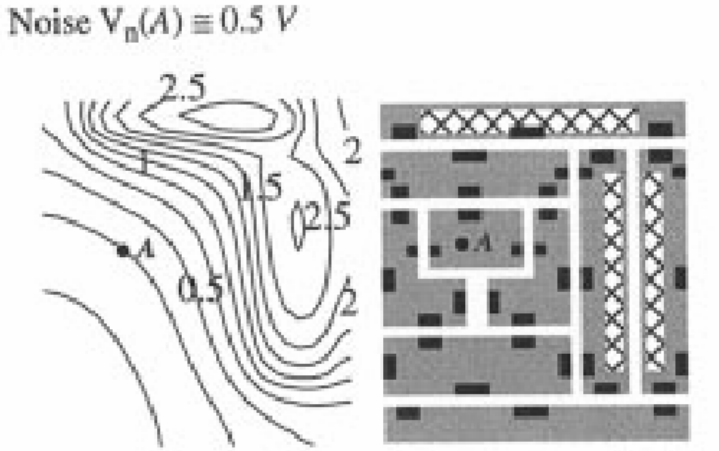
# Substrate model

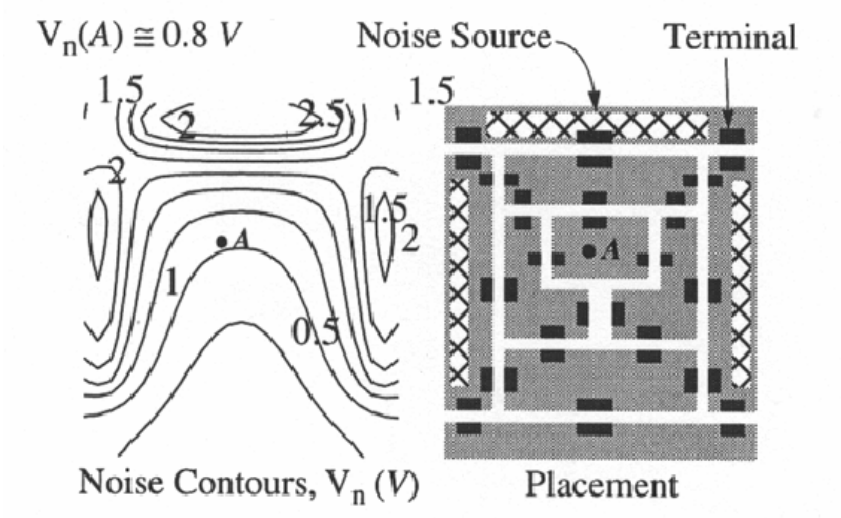


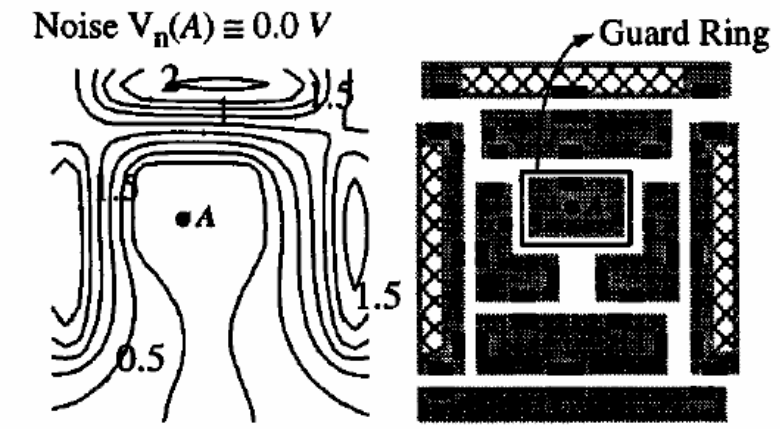

Mitra, JSSC March 1995, pp.269-278

# Placement : iso-noise curves

| Expt. | Constraint (V) | Normalized | | Time (min) |
|---|---|---|---|---|
| | | Area | WireLength | |
| 1 | - | 1 | 1 | 4 |
| 2 | $V_n(A) \leq 0.6$ | 1 | 2.33 | 139 |
| 3 | $V_n(A) \leq 0.1$ | 1.1 | 1.166 | 200 |




Mitra, JSSC March 1995, pp.269-278

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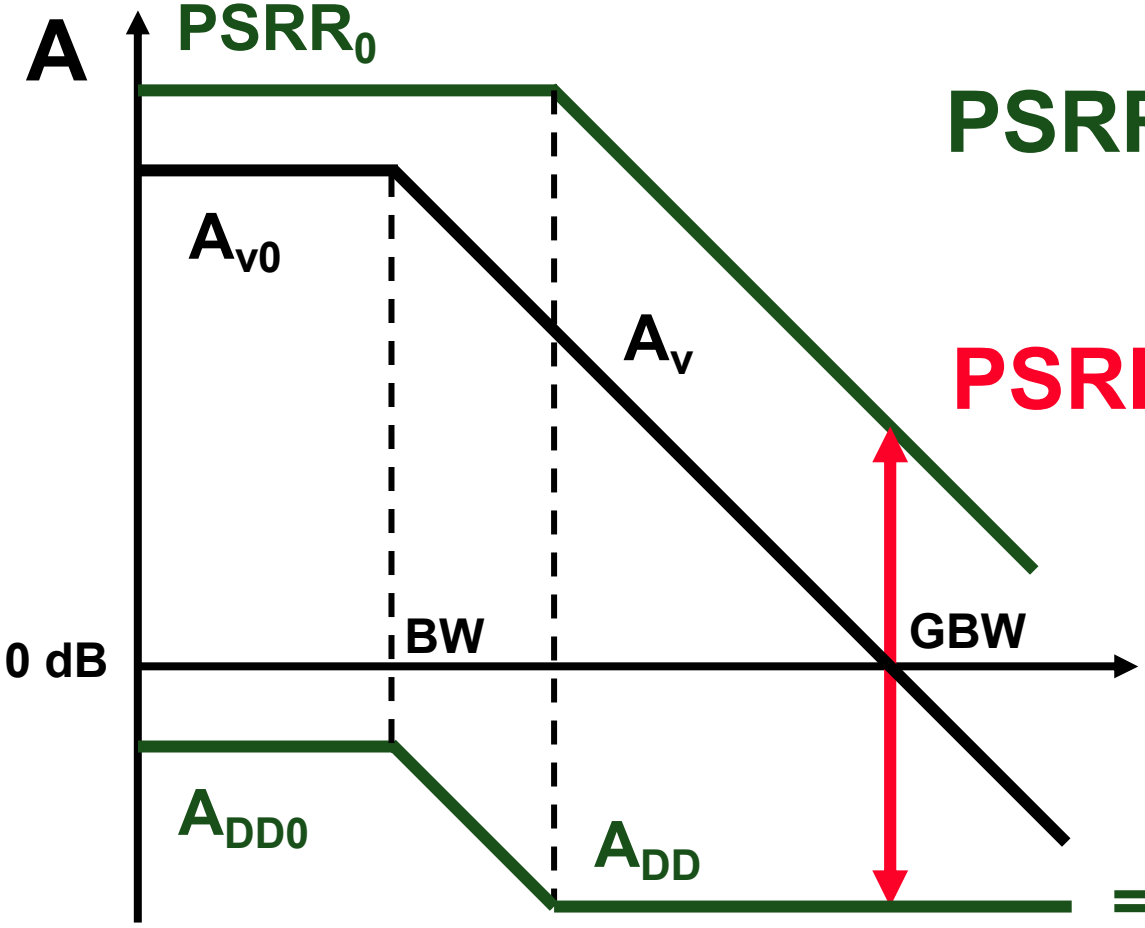
  - PSRR

# PSRR : definitions

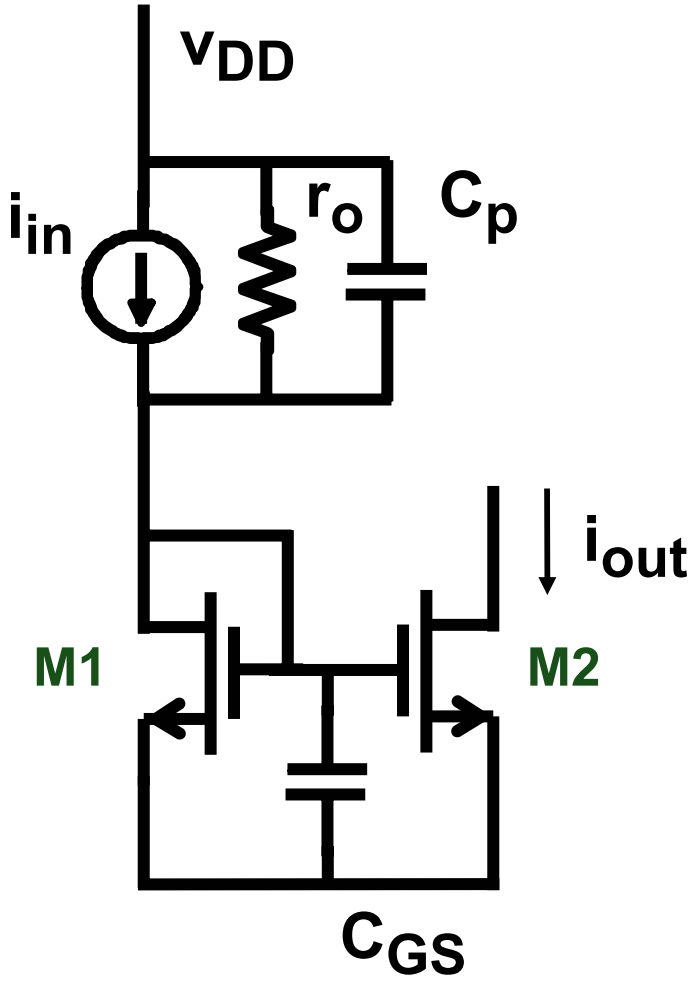



$$PSRR = \frac{A_v}{A_{DD}}$$

$$PSRR\Big|_{GBW} = \frac{1}{A_{DD}\Big|_{GBW}} = \frac{C_L}{C_n}$$

$$= \frac{C_n}{C_L}$$

# Example of PSRR




**LF**

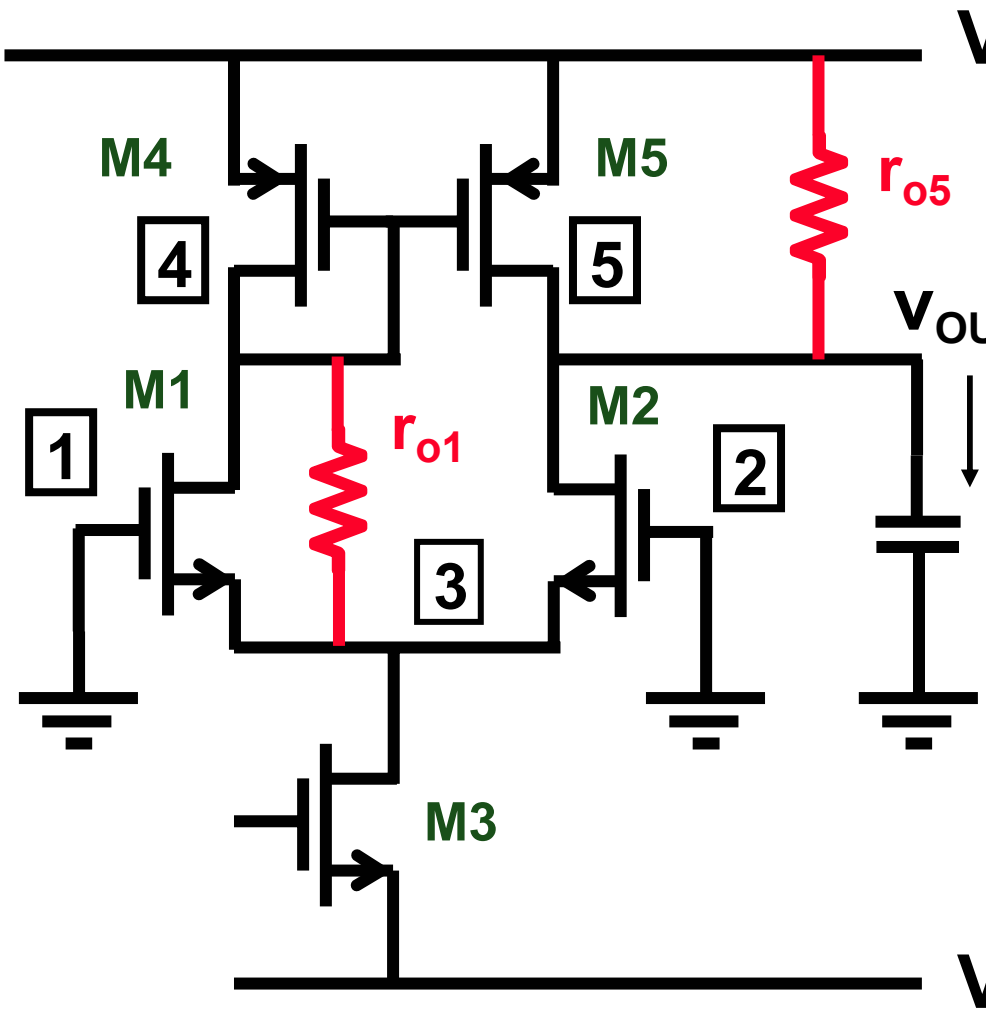
$$\frac{i_{out}}{v_{DD}} \approx g_o \qquad [\, g_o << g_m \,]$$

**HF**

$$\frac{i_{out}}{v_{DD}} \approx C_p s \qquad [\, C_p < C_{GS} \,]$$

$$[\, 1/g_m < C_{GS} s \,]$$

# $PSRR_{DD}$ of Simple CMOS OTA - 1

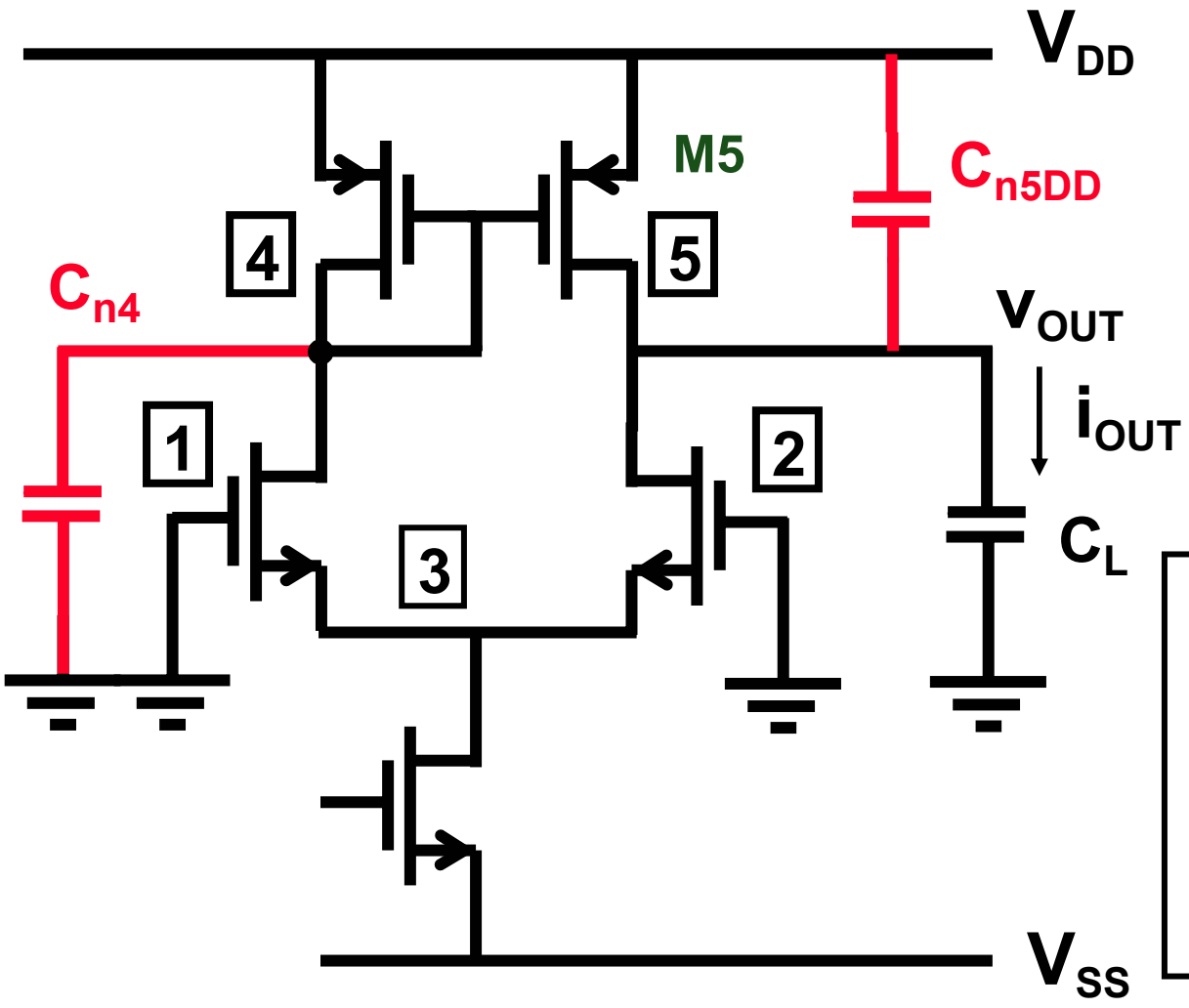



$$\frac{i_{OUT}}{v_{IN}} \approx g_{m1}$$

$$\frac{i_{OUT}}{V_{DD}} \approx g_{o1} + g_{o5}$$

$$PSRR_{DD} \approx \frac{g_{m1}}{g_{o1} + g_{o5}}$$

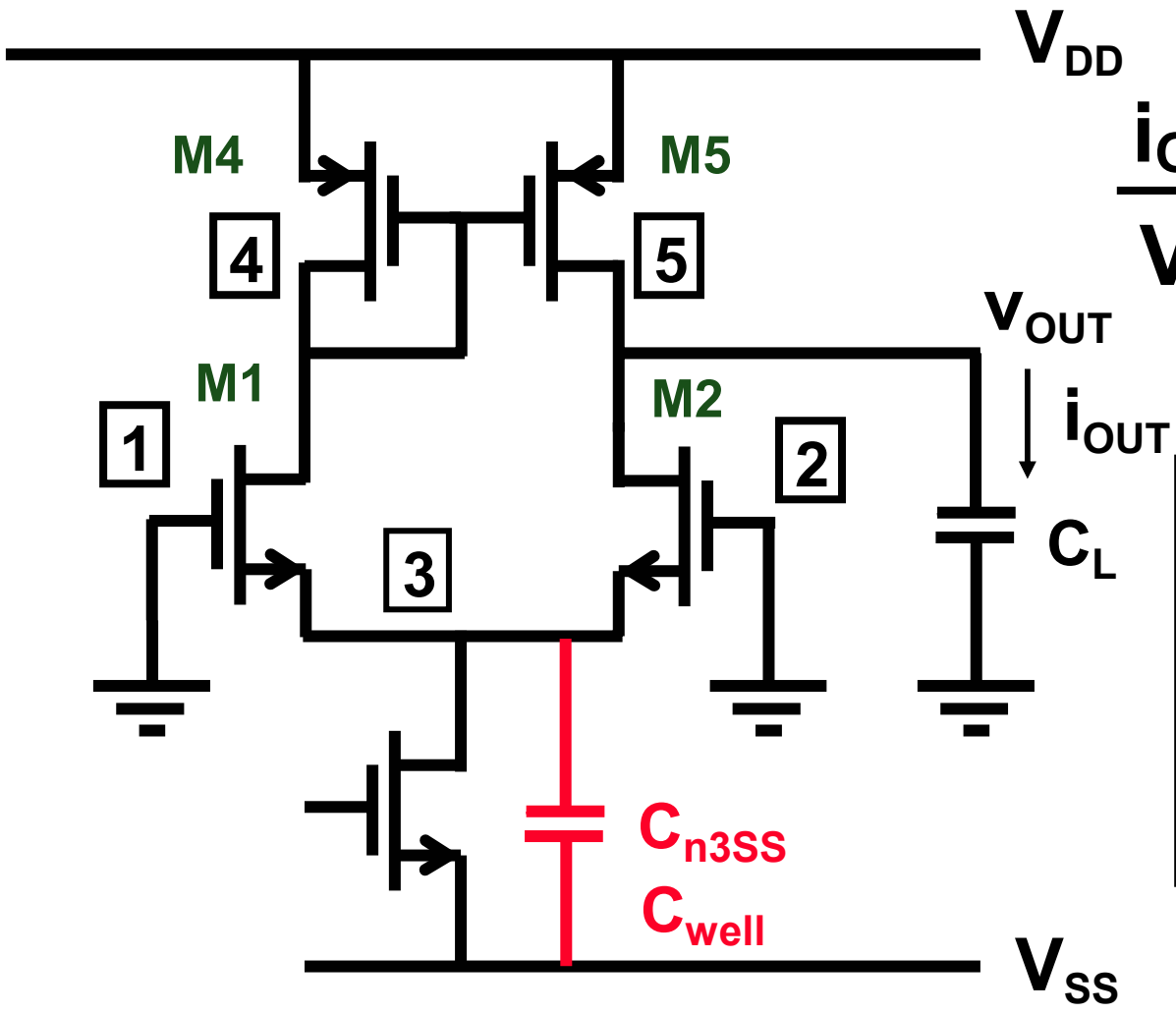
# $PSRR_{DD}$ of Simple CMOS OTA - 2




$$\frac{i_{OUT}}{V_{DD}} \approx (C_{n4} + C_{n5DD})s$$

$$PSRR_{DD}\Big|_{GBW} = \frac{C_L}{C_{n4} + C_{n5DD}}$$

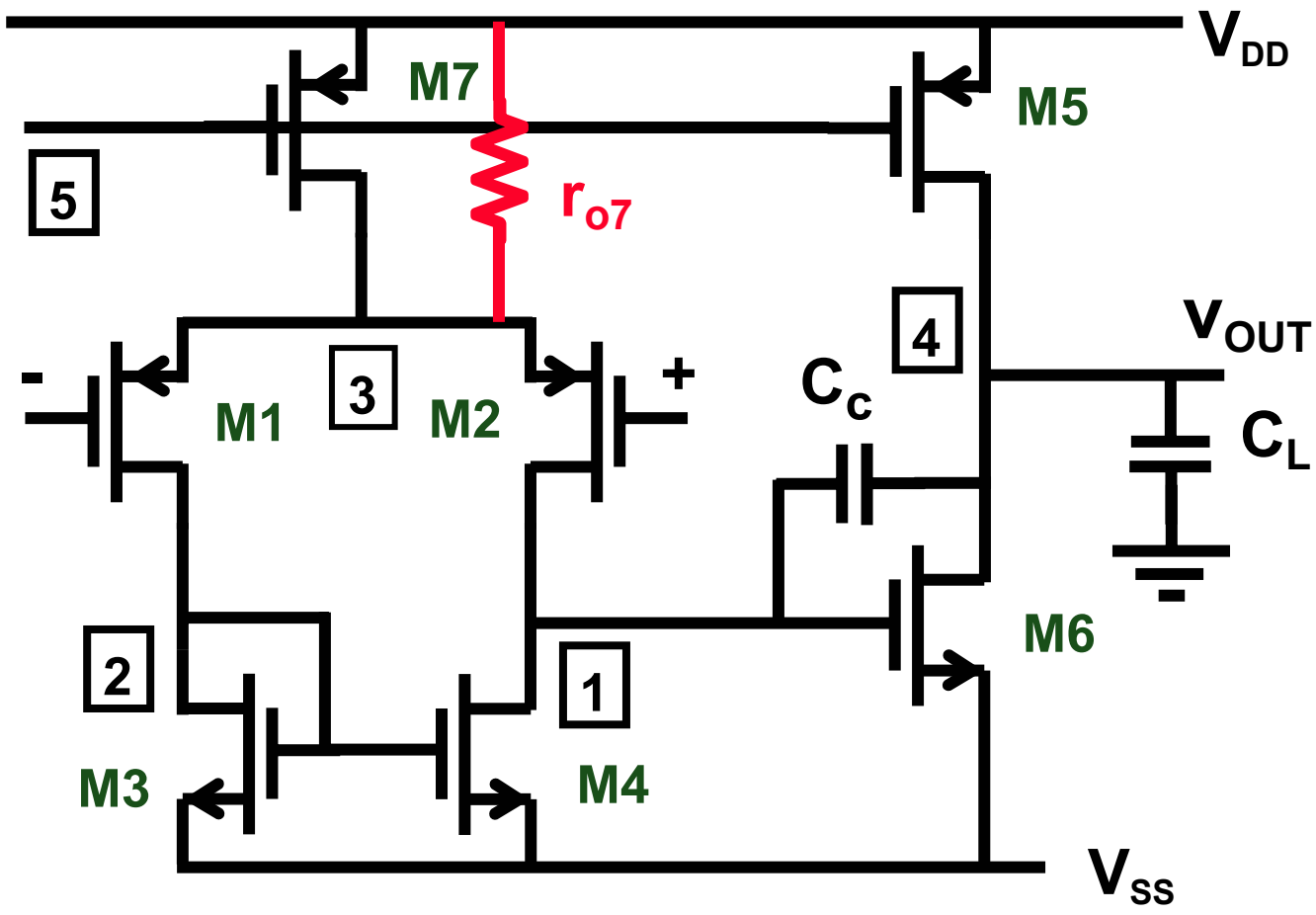
# $PSRR_{SS}$ of Simple CMOS OTA - 3




$$\frac{i_{OUT}}{V_{SS}} = sC_{n3SS}\frac{\Delta g_{m1}}{g_{m1}}$$

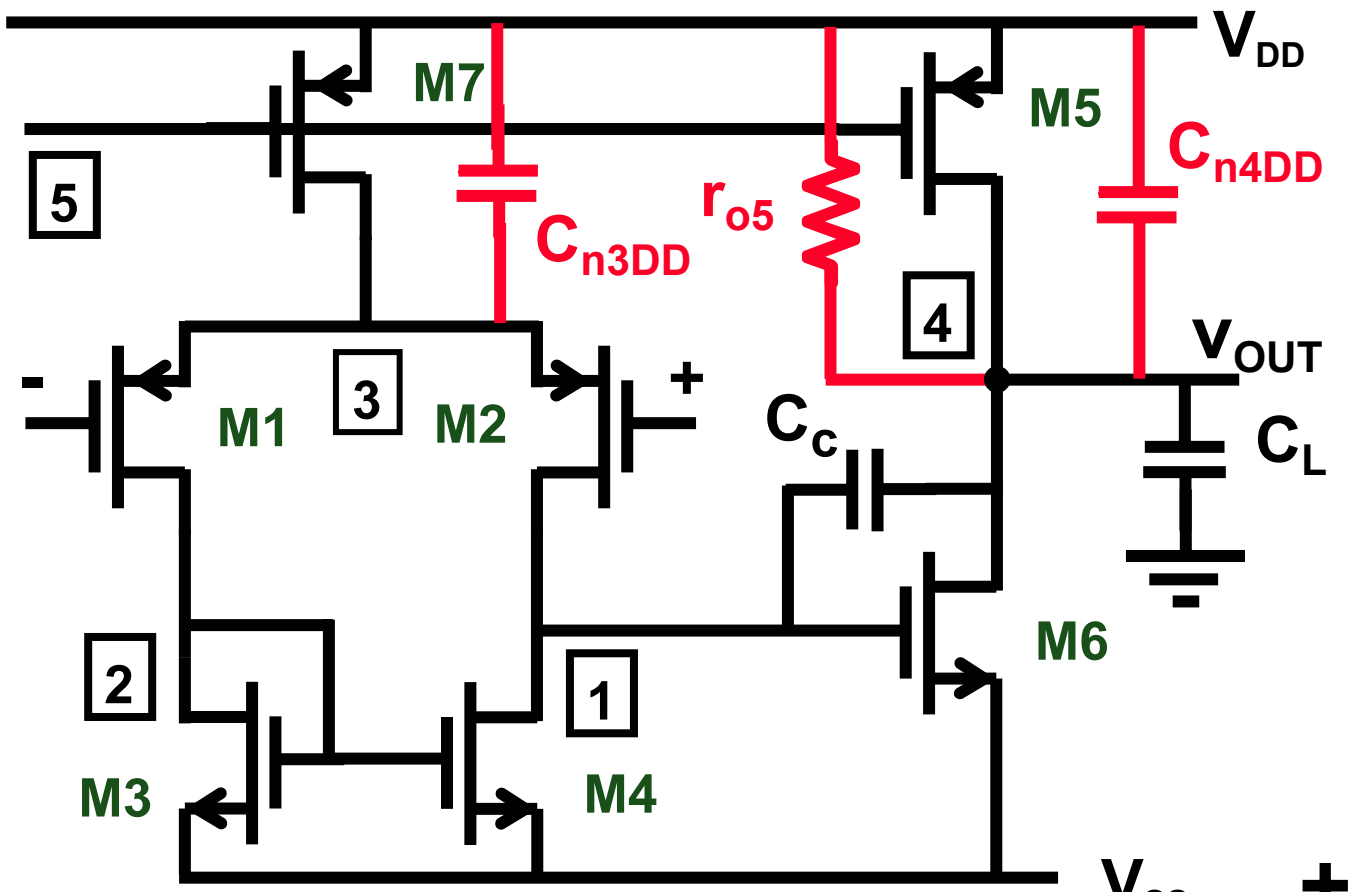
$$PSRR_{SS}\Big|_{GBW} = \frac{C_L}{C_{n3SS}}\frac{g_{m1}}{\Delta g_{m1}}$$

# Miller CMOS OTA - PSRR$_{DD}$



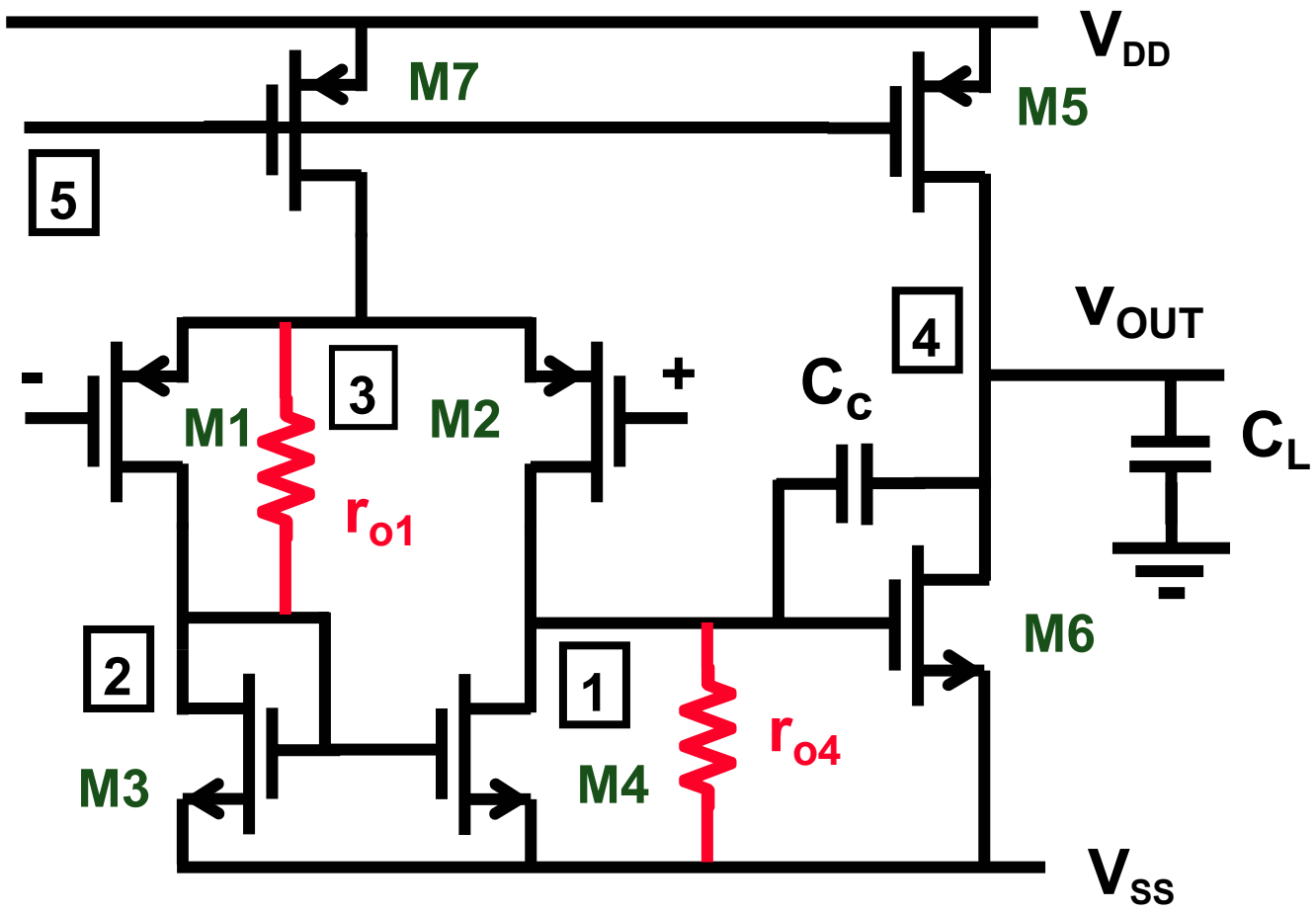

$$PSRR_{DD} = \frac{g_{m1}}{g_{o7}} \frac{g_{m1}}{\Delta g_{m1}}$$

# Miller CMOS OTA - $PSRR_{DD}$



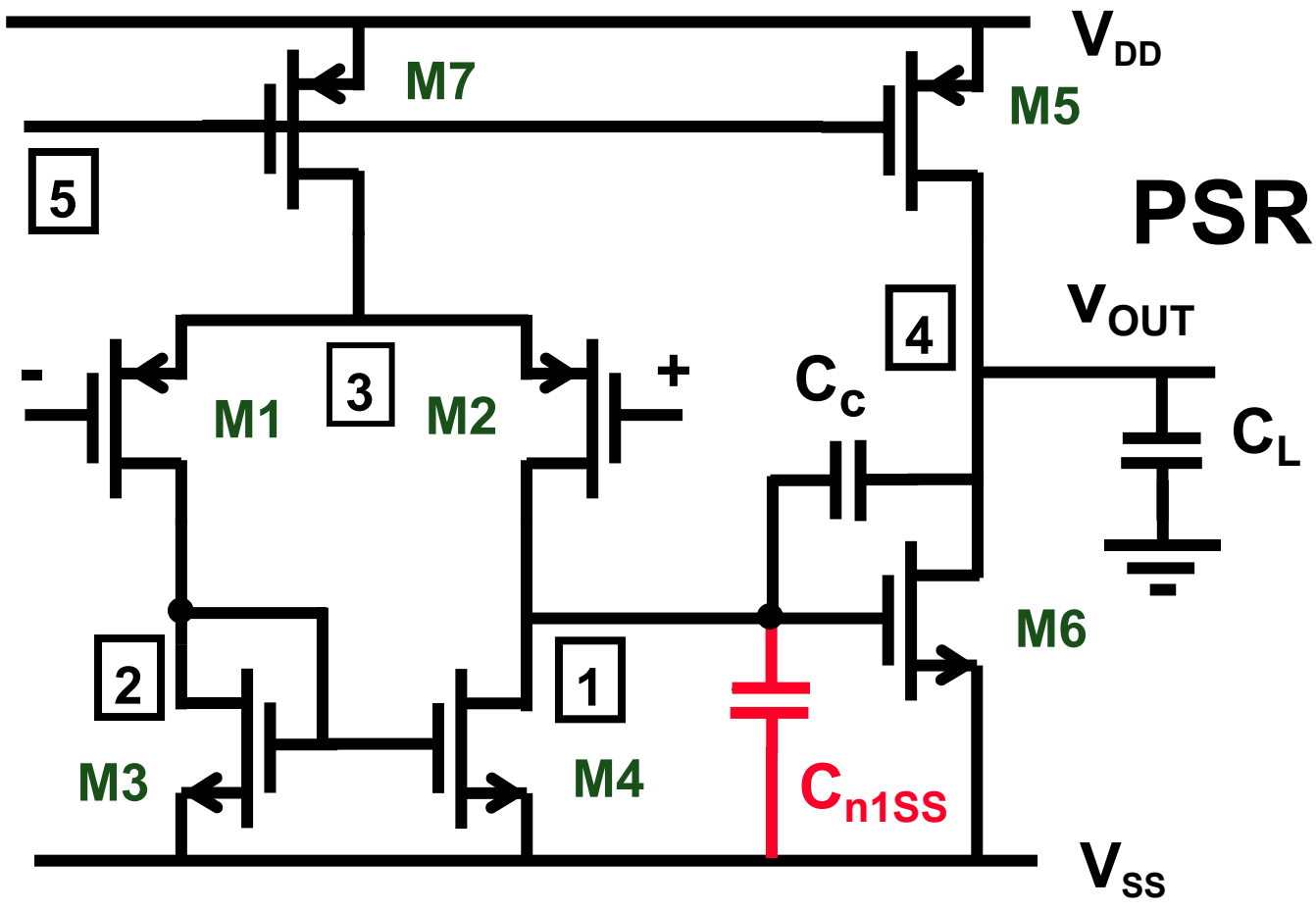

$$\left|\frac{PSRR_{DD}}{GBW}\right| = \frac{1}{\frac{g_{o5}}{g_{m6}} + \frac{C_{n4DD}}{C_L} + \frac{C_{n3DD}}{C_c}\frac{\Delta g_{m1}}{g_{m1}}}$$

# Miller CMOS OTA - PSRRss




$$PSRR_{SS} = \frac{g_{m1}}{g_{o1} + g_{o4}}$$

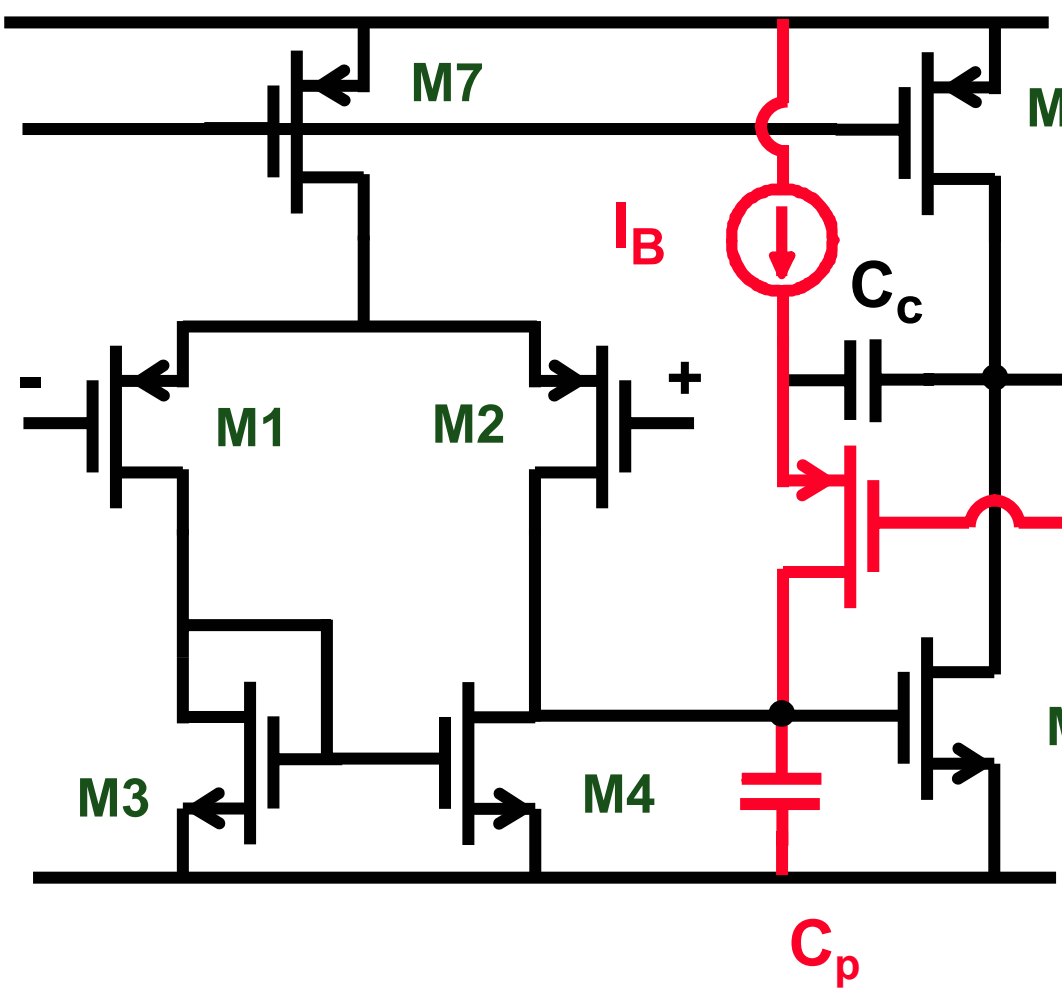
# Miller CMOS OTA - PSRRss




$$PSRR_{SS}\Big|_{GBW} = 1 + \frac{C_{n1SS}}{C_c}$$

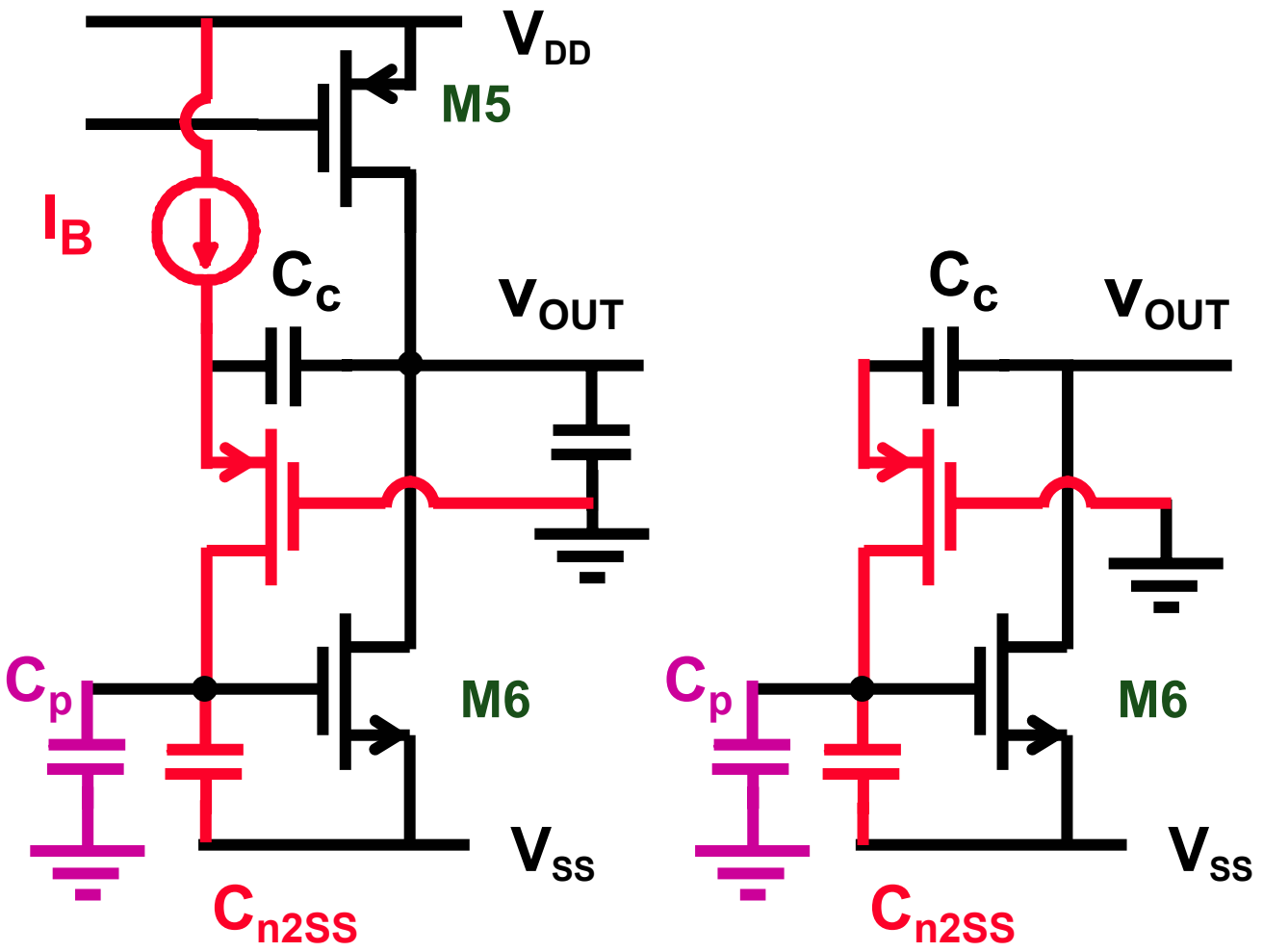
$$\approx 1 \text{ or } 0 \text{ dB}$$

# Improving the Miller CMOS OTA




$$PSRR_{SS}\Big|_{GBW} = \frac{C_c}{C_p} \approx 20\ dB$$

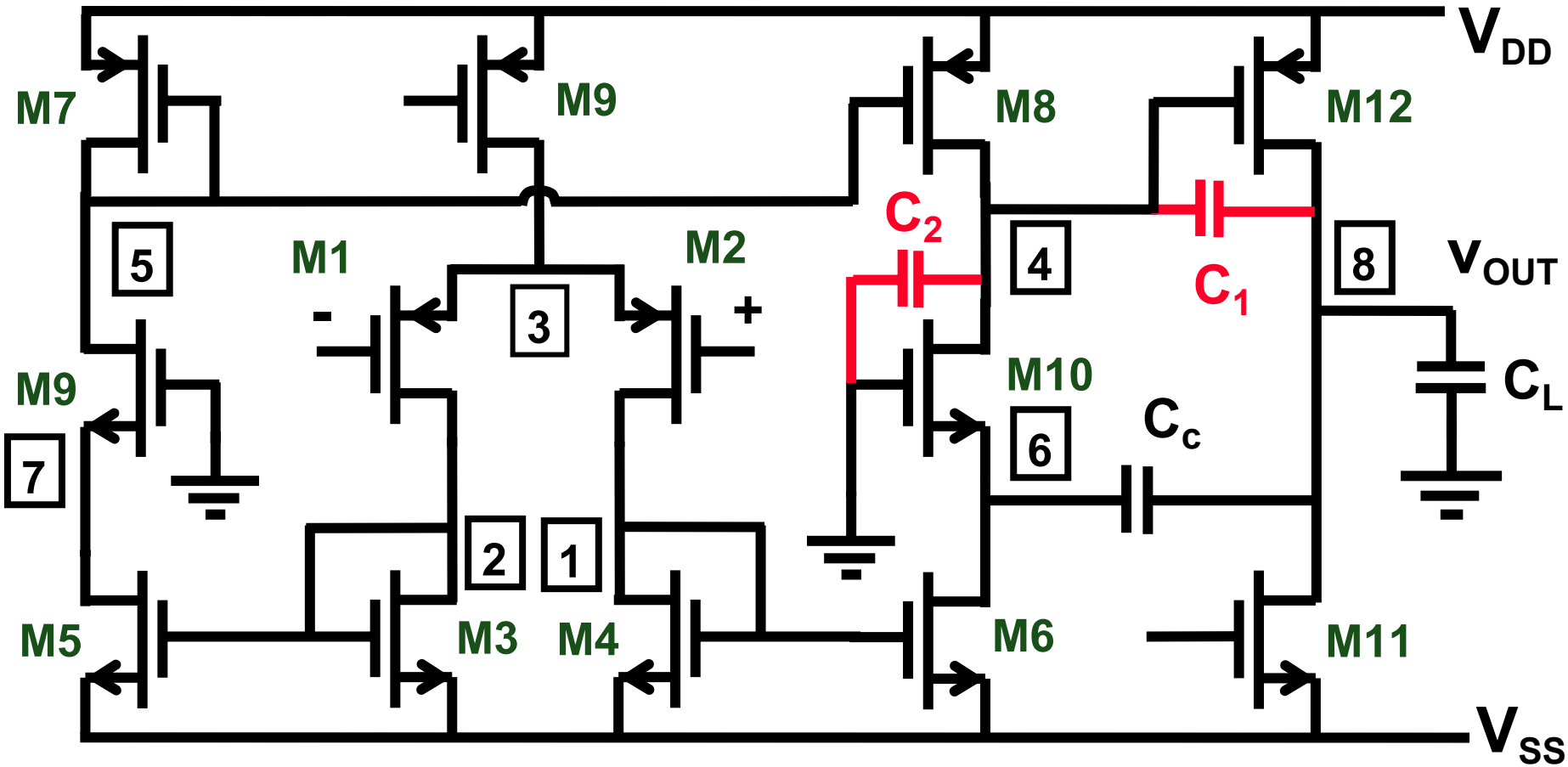
# Improving the Miller CMOS OTA




$$\left|\frac{PSRR_{SS}}{GBW}\right| = \frac{C_c}{C_p^*} \approx 20\ dB$$

$$C_p^* = C_p + C_{n2SS}$$

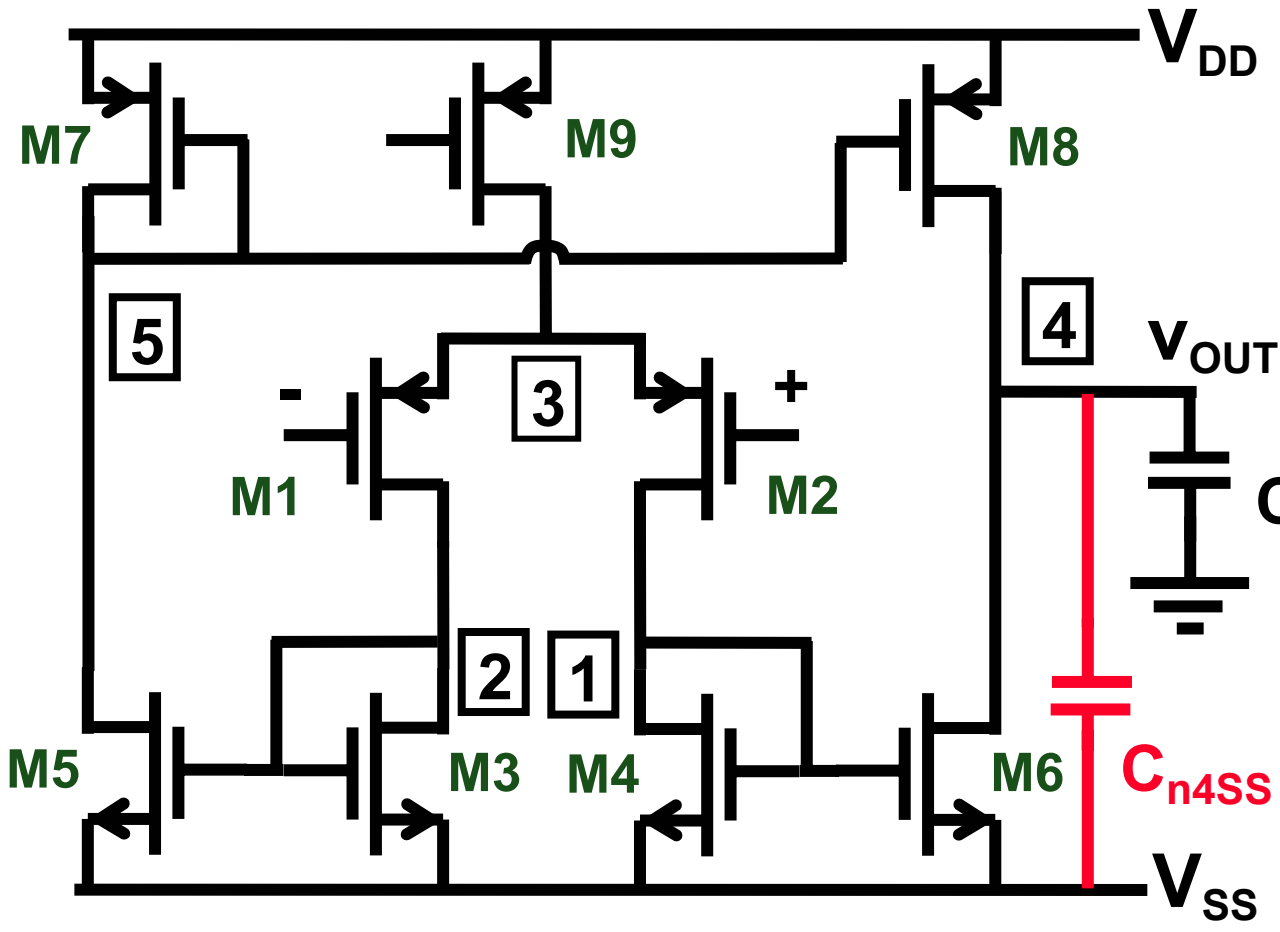
# Miller CMOS OTA - PSRRss




$$PSRR_{SS}\Big|_{GBW} = \frac{C_c}{C_1+C_2}$$

$C_1 = C_{DG12}$ $C_2 = C_{DG10}+C_{DB10}+C_{DB8}$

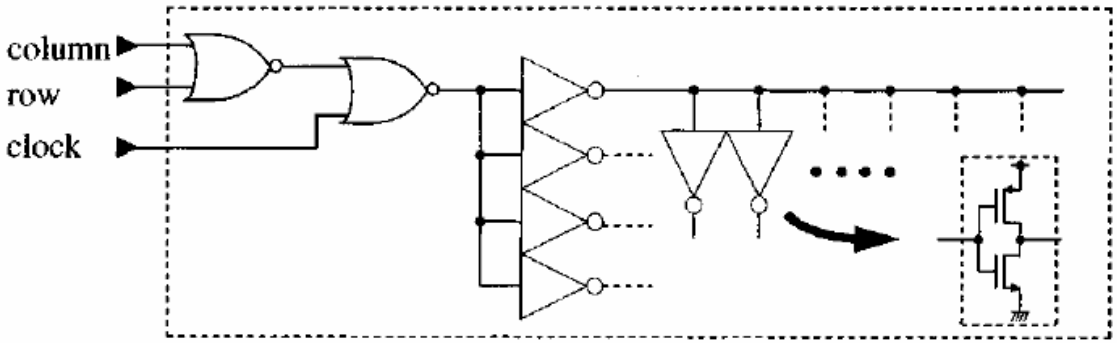
# Symmetrical CMOS OTA - PSRRss

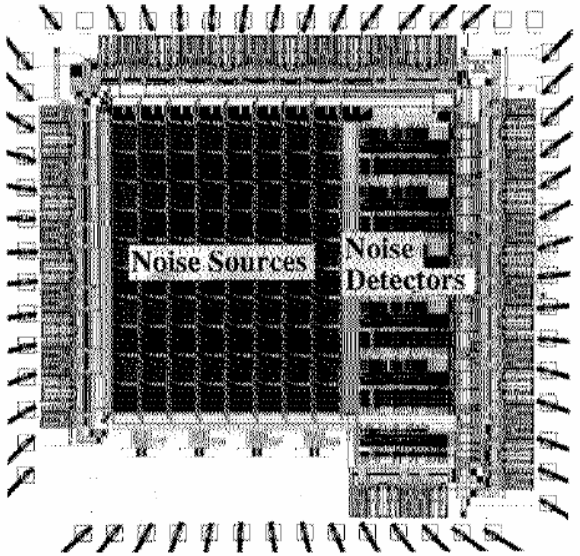


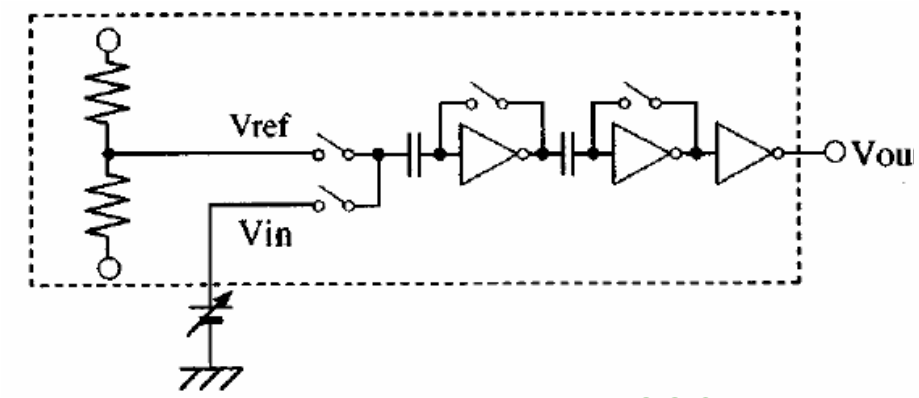

$$PSRR_{SS} \approx \frac{g_{m1}}{g_{o68} + (\Delta C_{n45SS})s}$$

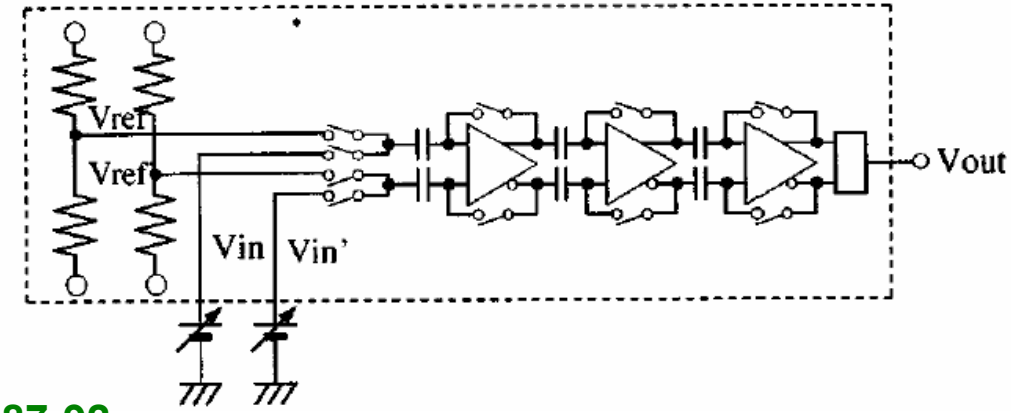
$$PSRR_{SS}\Big|_{GBW} \approx \frac{C_L}{C_{n4SS}}$$

# Differential- versus Single-Ended circuits



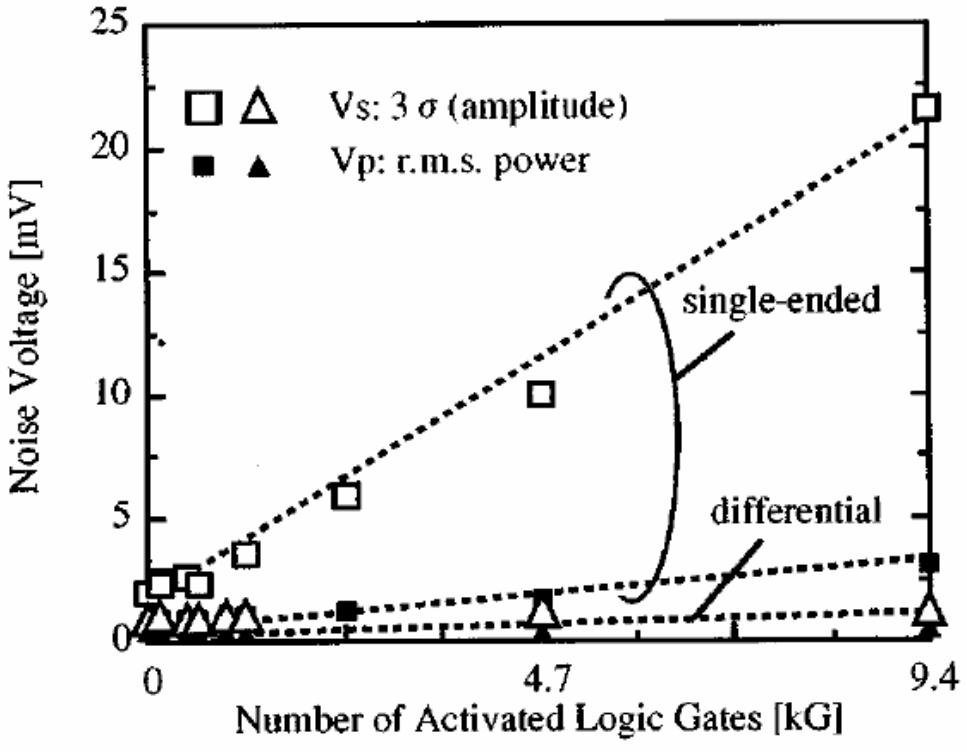



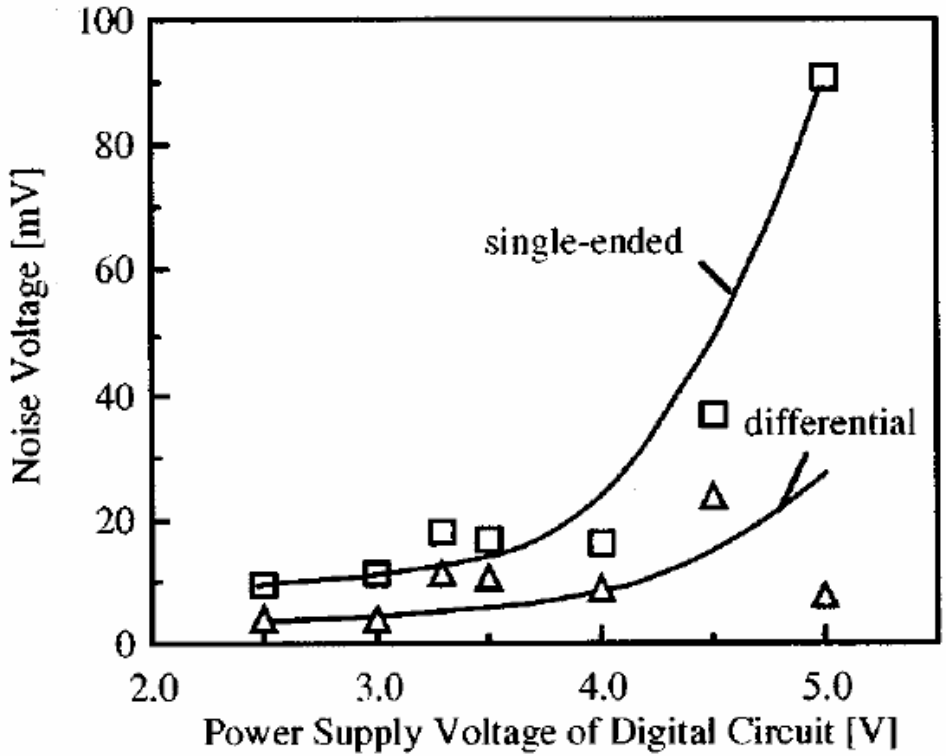




Makie-Fukuda, JSSC, Febr.95, 87-92

# Differential vs Single-Ended data



# Conclusions

- Reduce circuit noise generation
  - Use linear circuits
  - Current mode logic
  - Avoid class AB amplifiers
- Reduce  substrate coupling
  - Use different power supplies for A, D, G and S
  - Reduce drain areas
  - Guard rings close to A with dedicated pin : high-R substr.
  - Buried layers under A : low-R substrate
  - Use decoupling capacitances on A
  - Create distance : high-R substrate
- Improve PSRR by use of differential circuits : matching !!

# Outline

- Circuit noise generation
- Circuit noise coupling
  - Power supply pinning
  - Substrate coupling
  - Circuit placement
- Rejection of circuit noise
  - PSRR