CMOS ADC & DAC Principles

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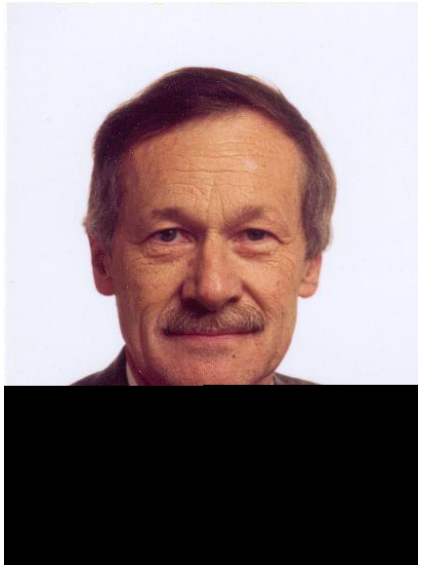

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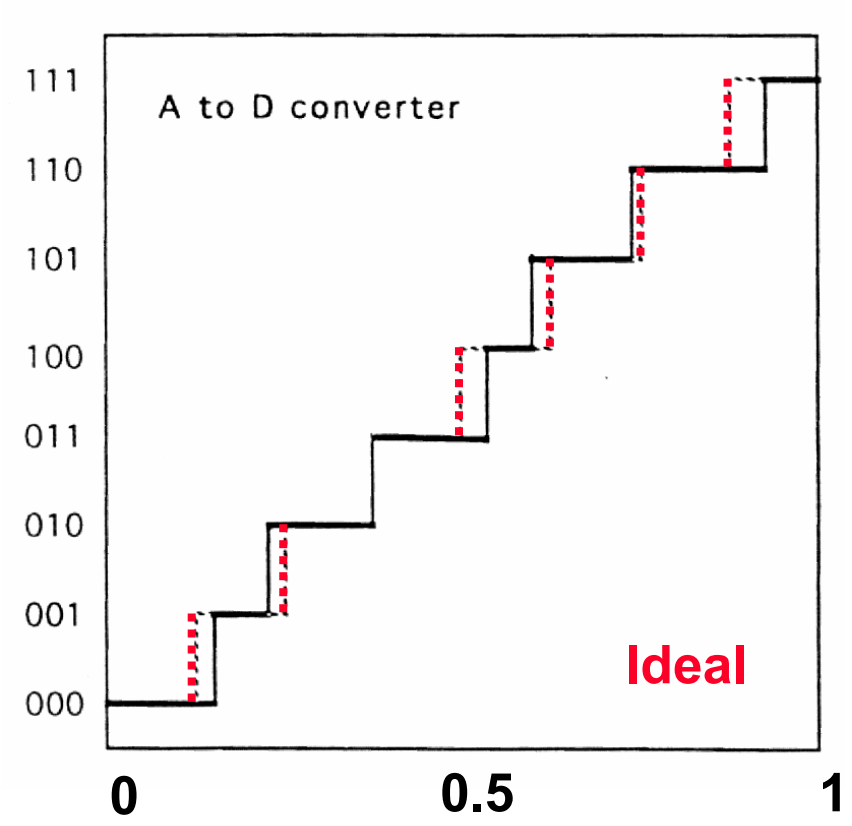
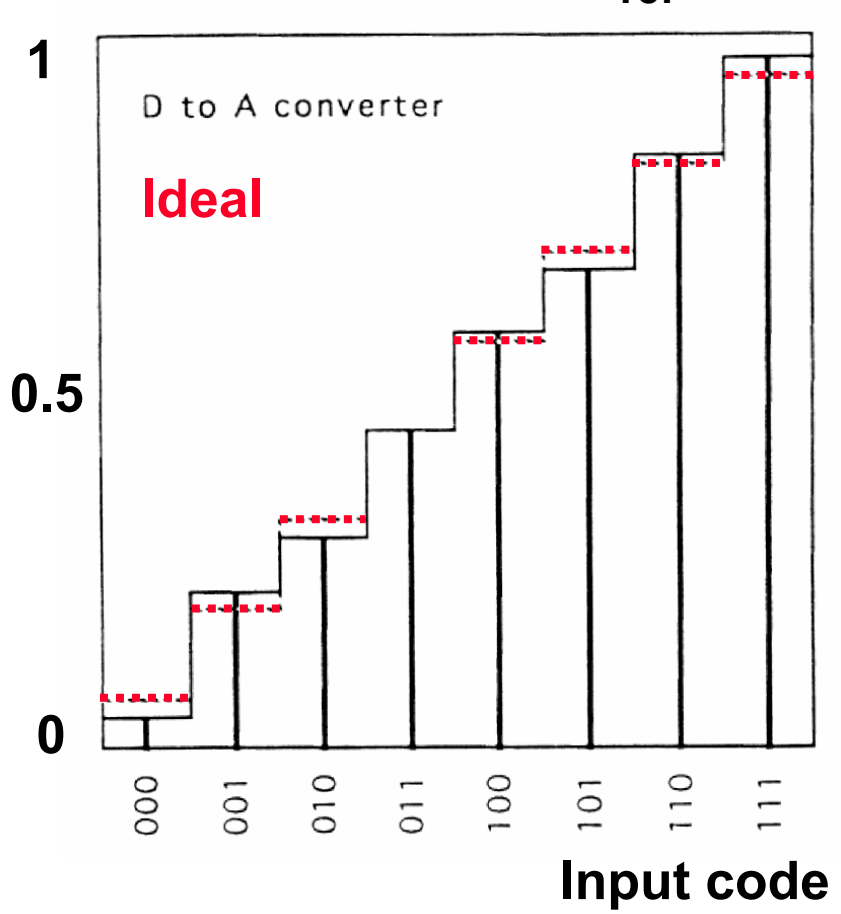
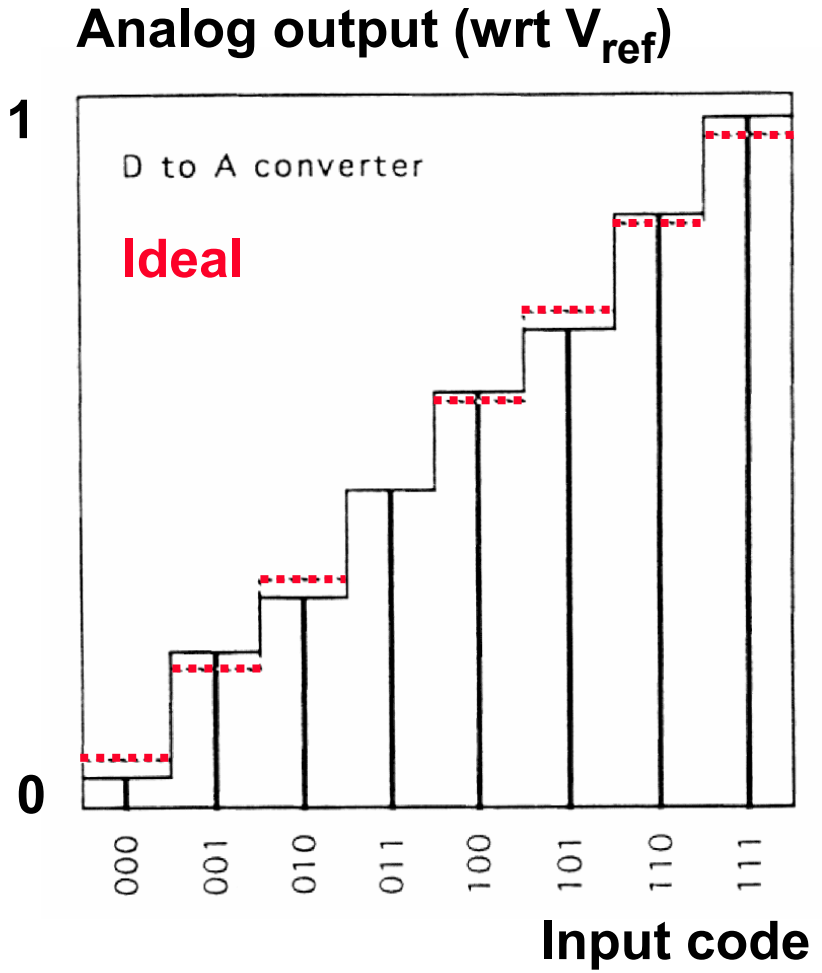
ADC & DAC


Output code
111
110
101
100
011
010
001
000
A to D converter
Ideal
0
0.5
1
Analog input (with respect to V_{ref})


Analog output (wrt V_{ref})
1
0.5
0
D to A converter
Ideal
000
001
010
011
100
101
110
111
Input code

DACs Resolution



$$V_{OUT} = V_{REF}\ B_{IN}$$

$$= V_{REF}\left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \ldots \frac{b_N}{2^N}\right)$$

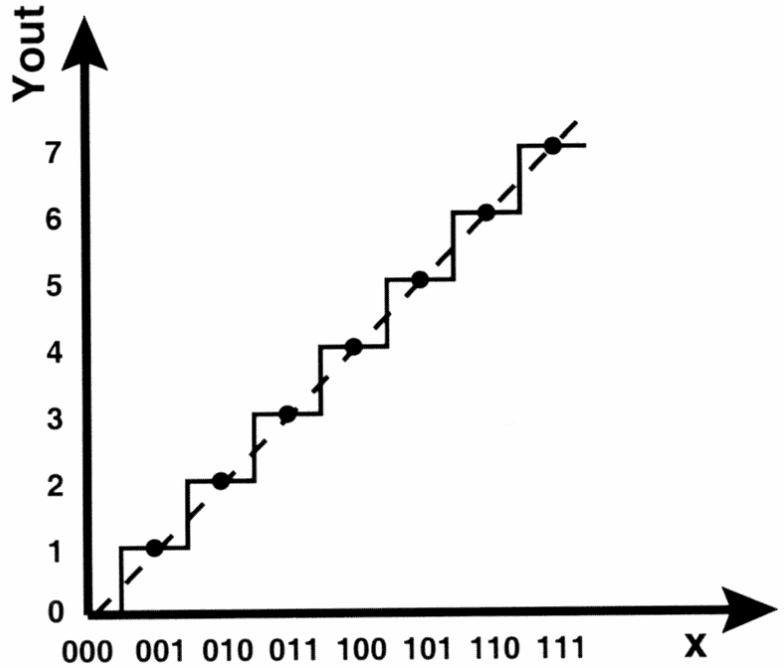
$$V_{LSB} = \frac{V_{REF}}{2^N}$$

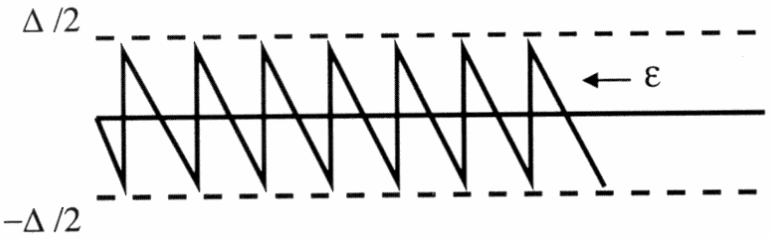
Resolution N

b_1 is Most Significant bit (MSB)

b_N is Least Significant bit (LSB)

The quantisation error of a DAC





$$P_{Noise} = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} \varepsilon^2 \, d\varepsilon = \frac{\Delta^2}{12}$$

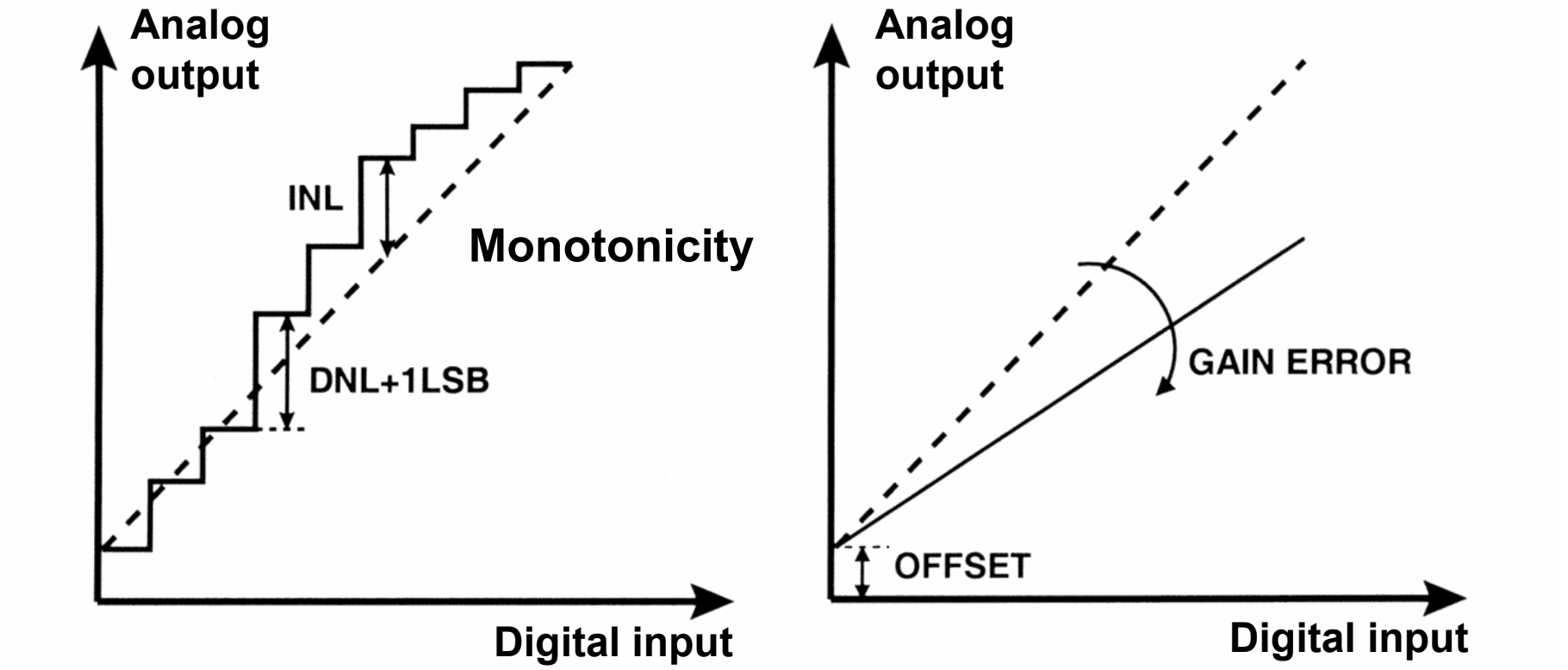
$$V_{ptp} = 2^N \Delta$$

$$P_{Signal} = \frac{V_{ptp}^2}{8}$$

$$SNR = \frac{3}{2} 2^{2N}$$

$$SNR = 6\,N + 1.76 \text{ dB}$$

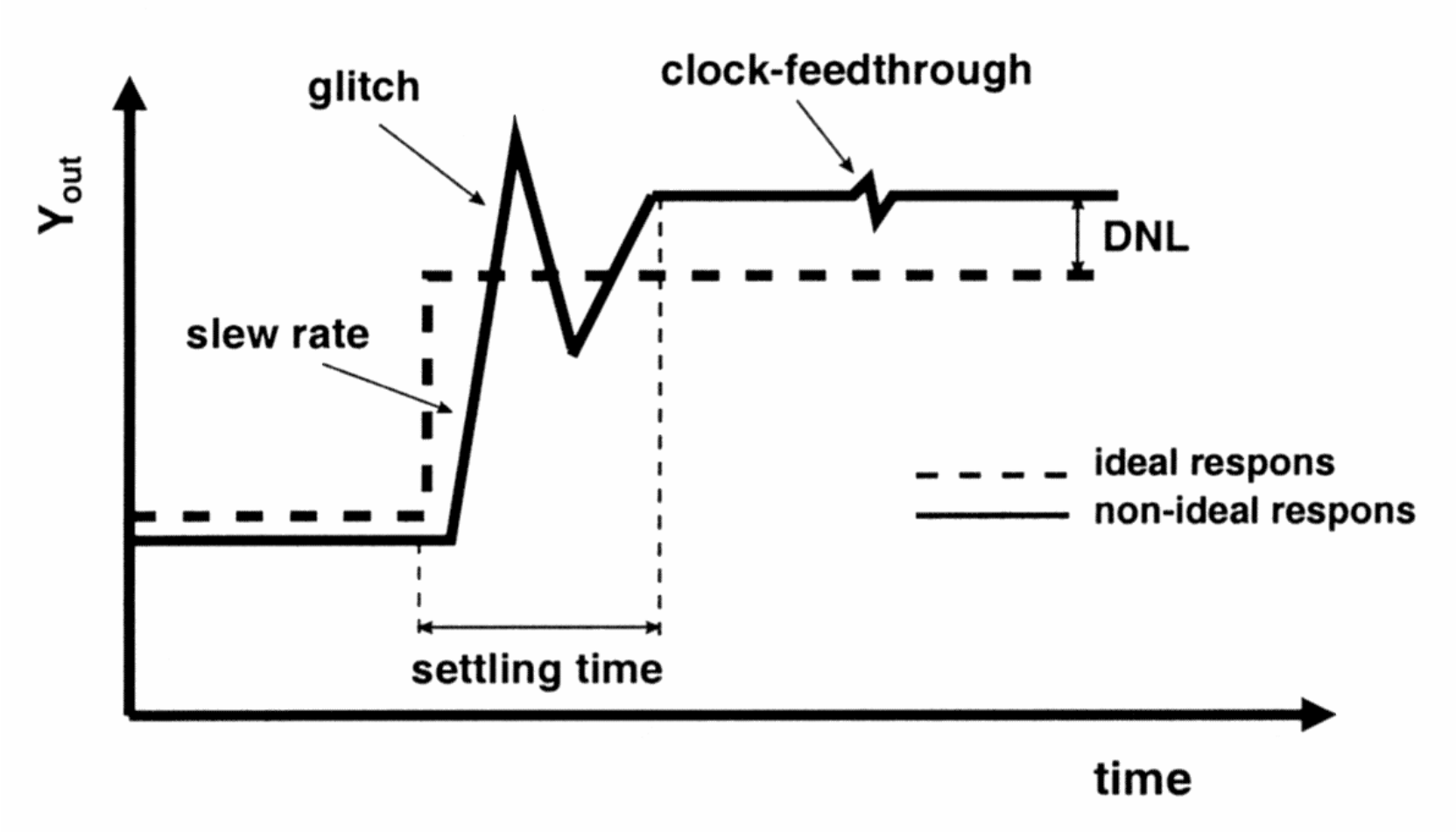
Static specs : INL & DNL



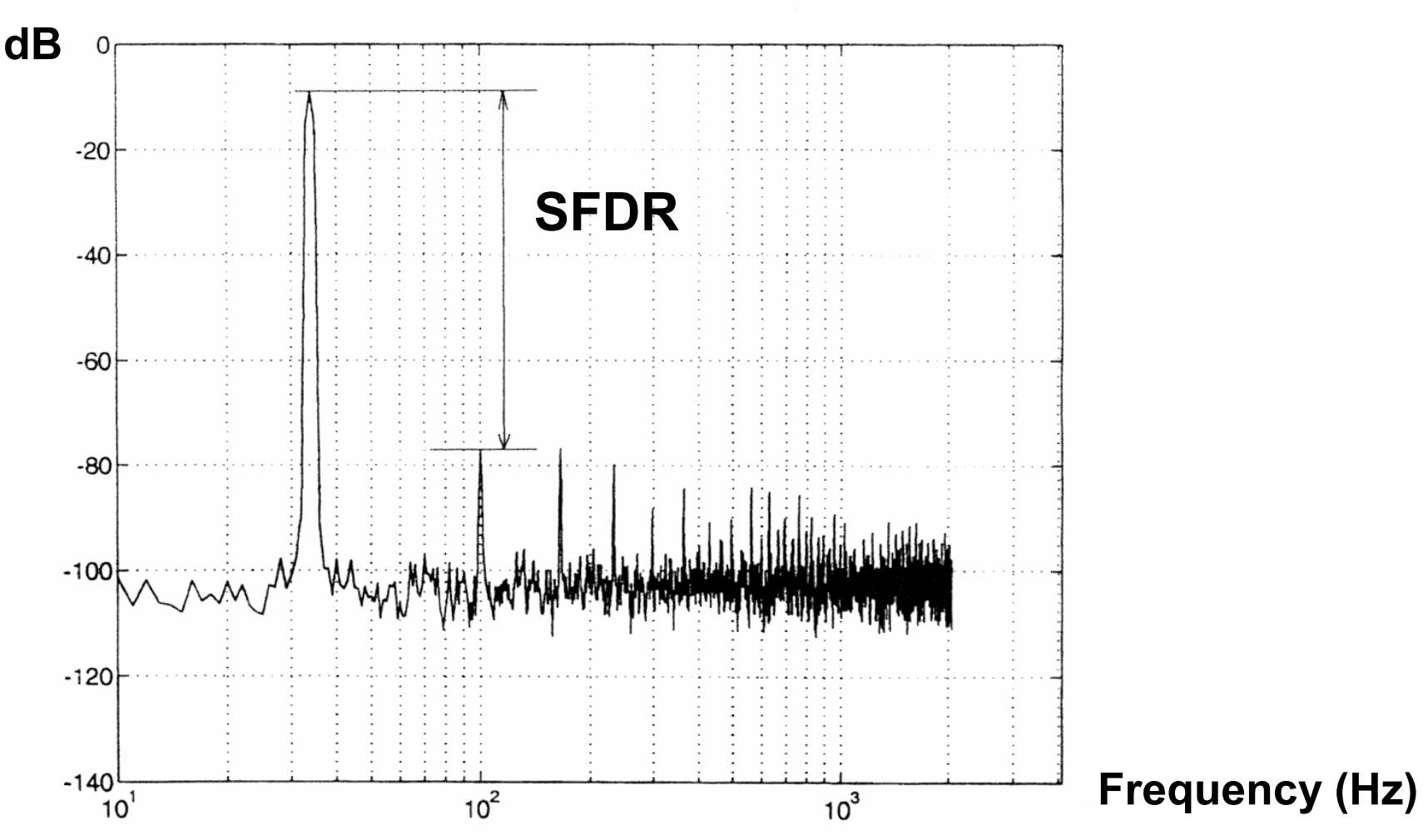
Differential Nonlinearity : DNL = $Y_{OUT}(B) - Y_{OUT}(B-1) - 1$ LSB

Integral Nonlinearity : INL = $Y_{OUT}(B) - Y_{OUT,id}(B)$

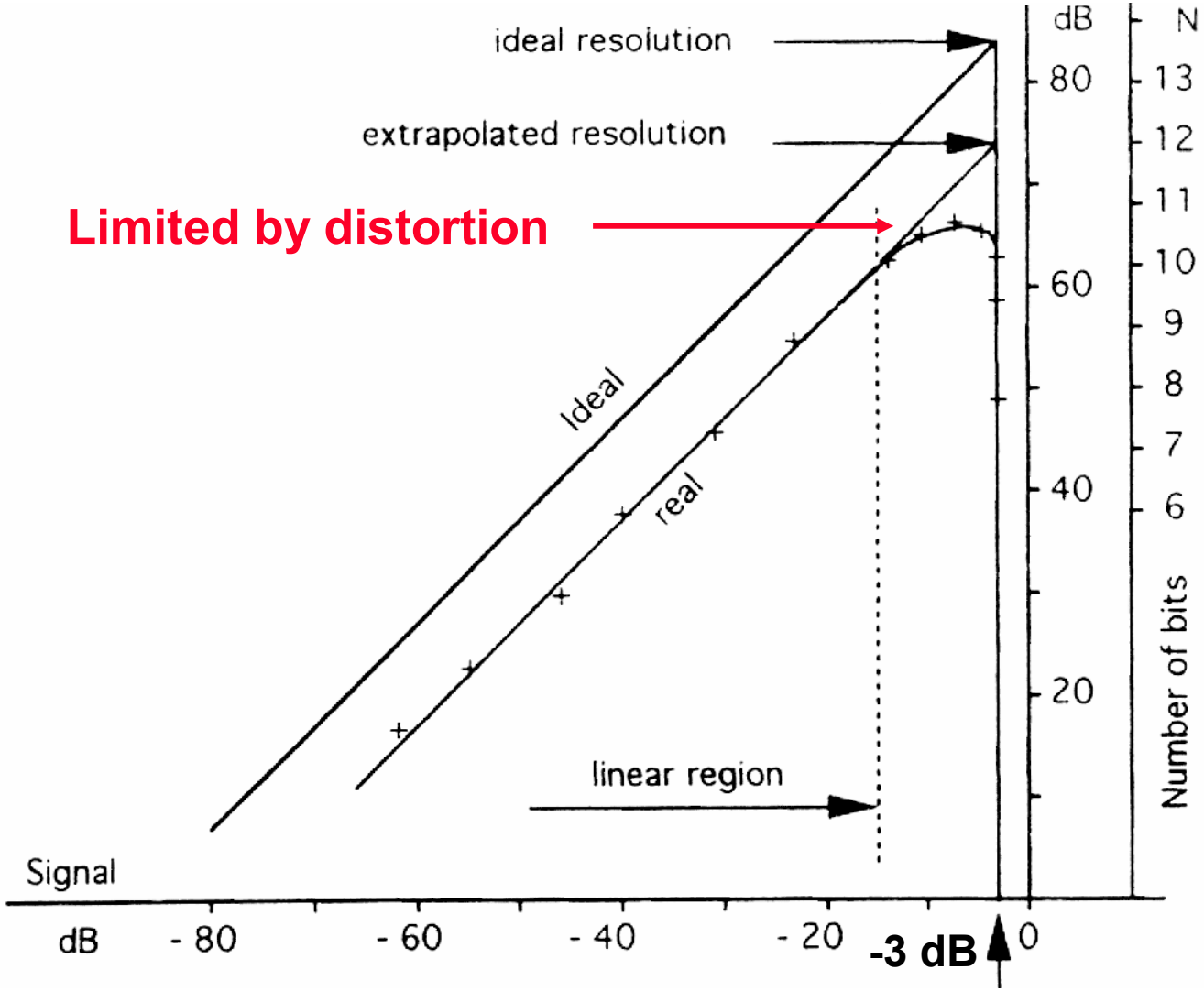
Dynamic specifications



Spectral content : Spurious free dynamic range



Output SNR versus input Signal



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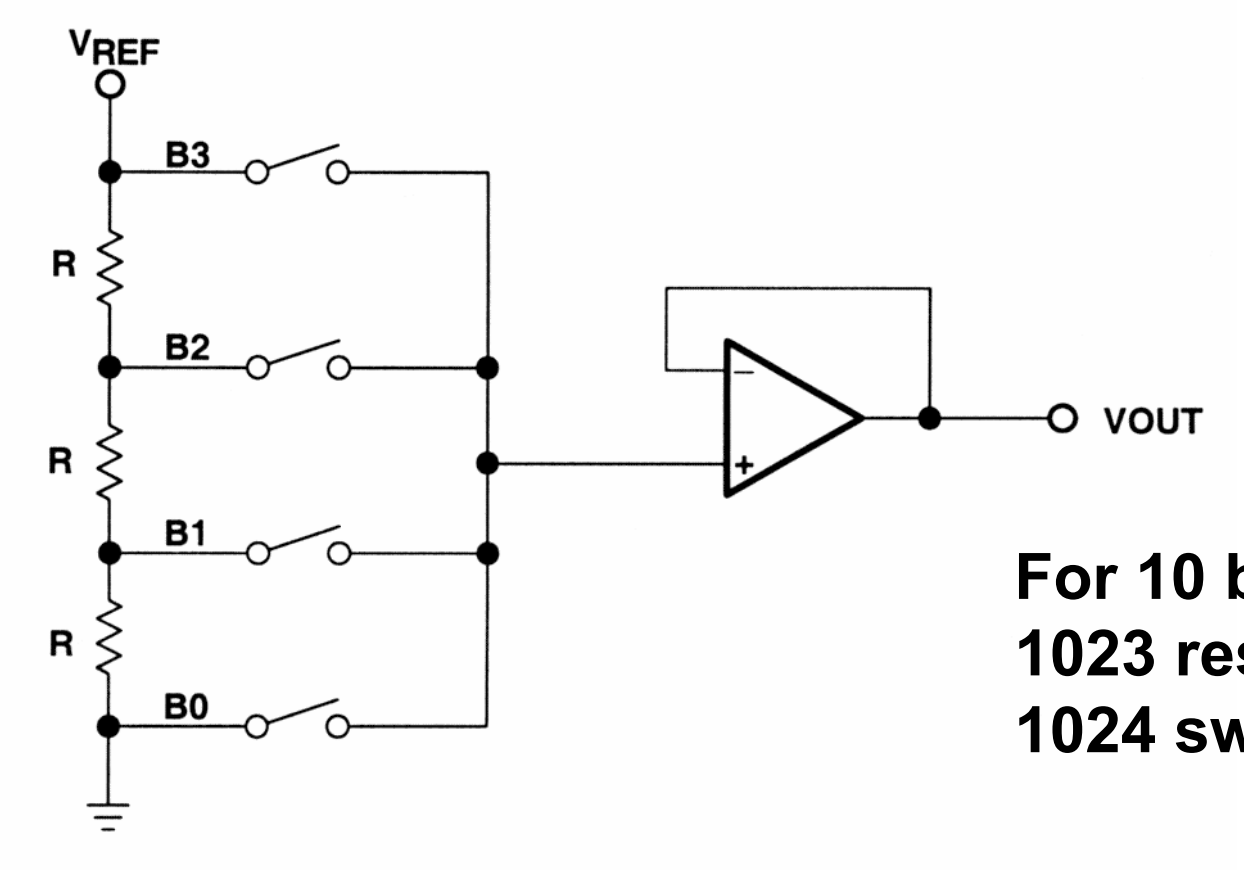
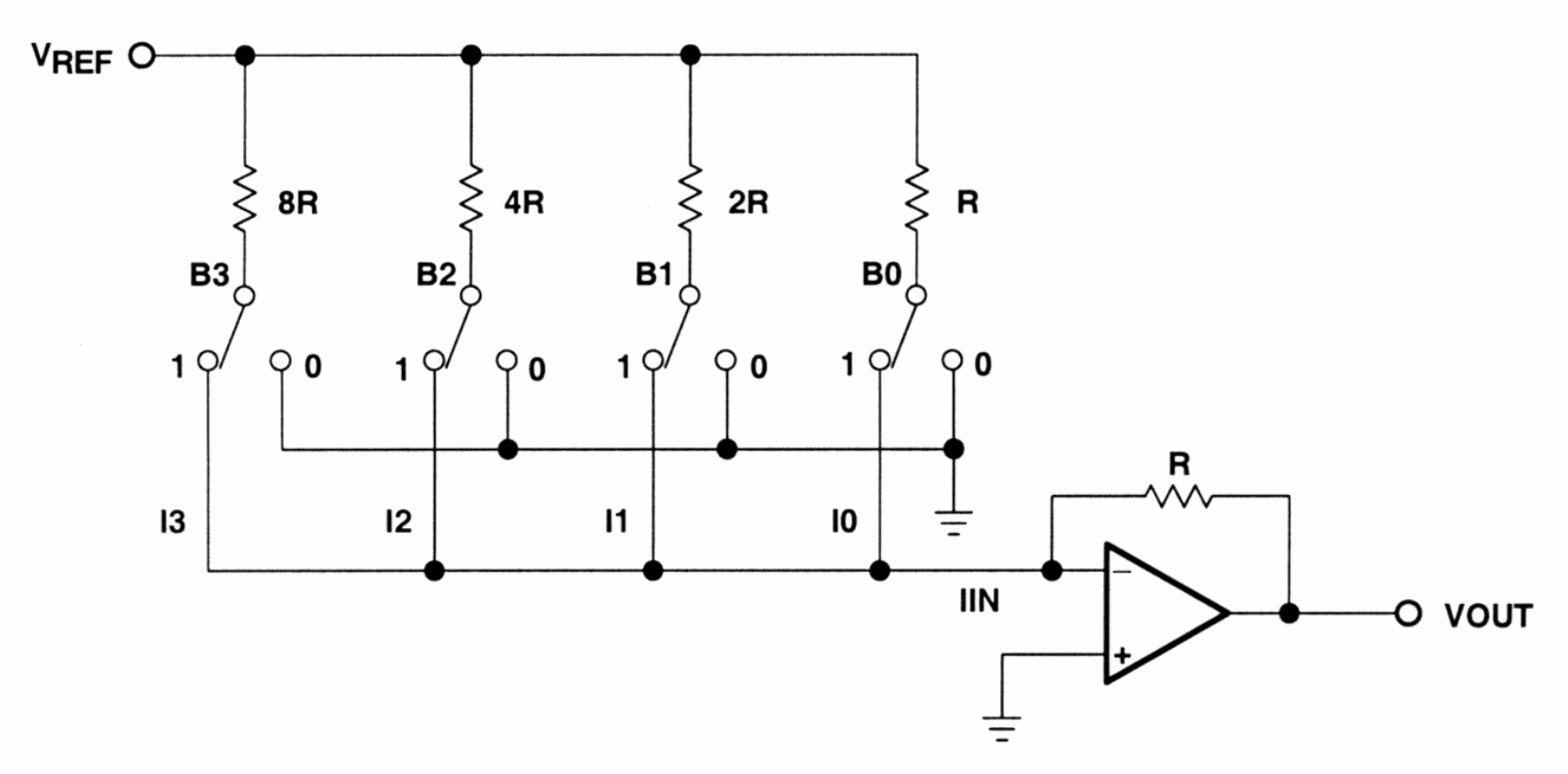
Resistor string DAC



For 10 bit:
1023 resistors and
1024 switches !!

Resistive matching !

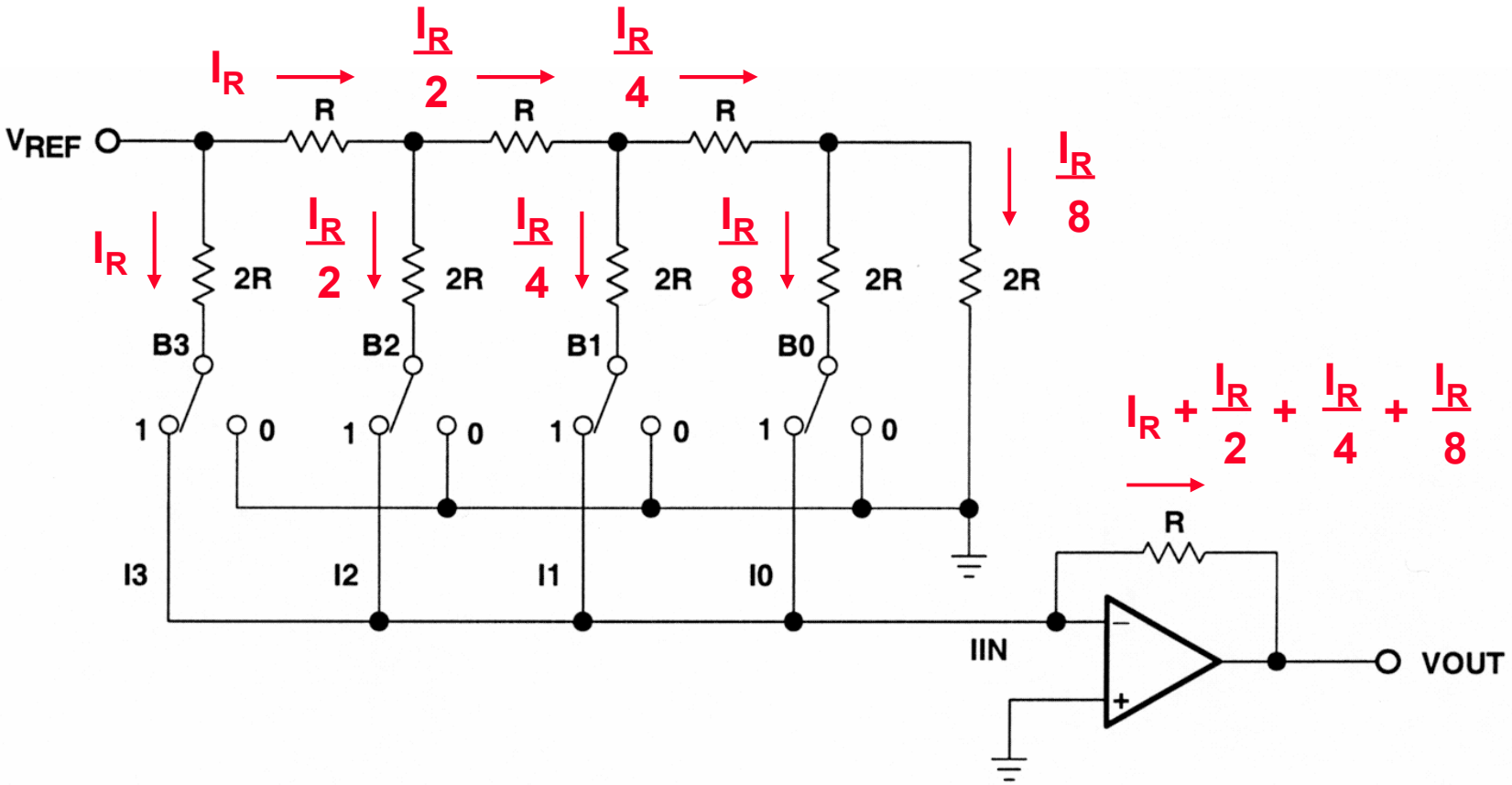
Binary weighted resistor DAC



One Resistor and Switch per bit

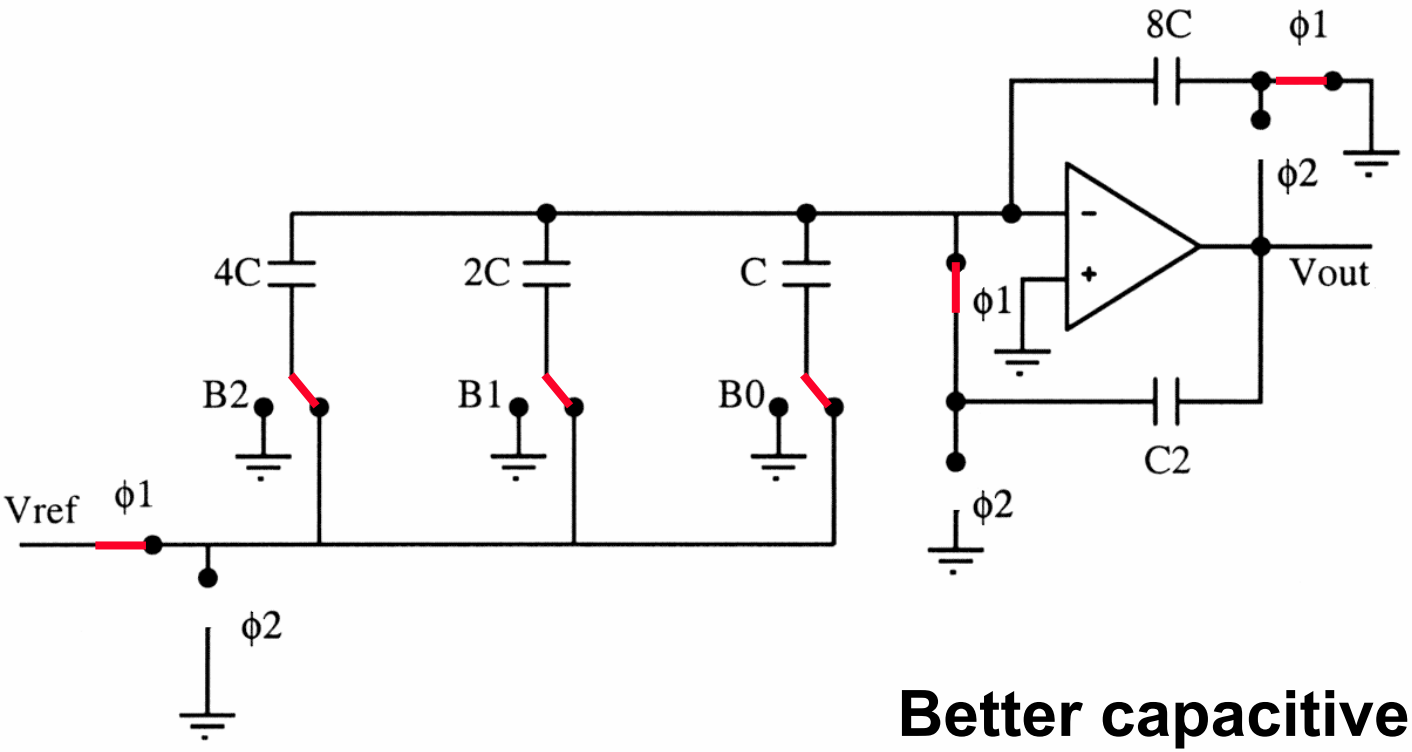
No guaranteed monotonicity (glitches !)

R-2R DAC



Smaller area in Resistors !

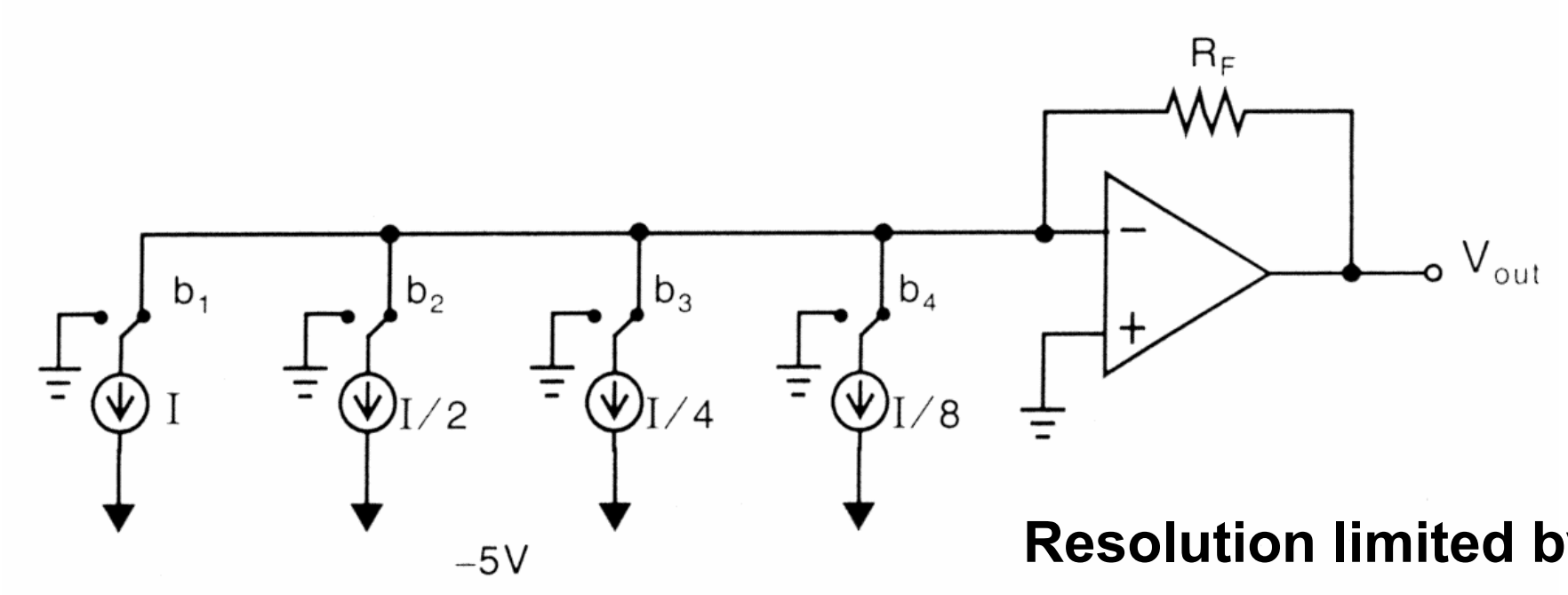
3-bit charge redistribution DAC



Better capacitive matching !

Phase Φ1

4-bit Current steering DAC



Resolution limited by Mismatch in the Current sources !

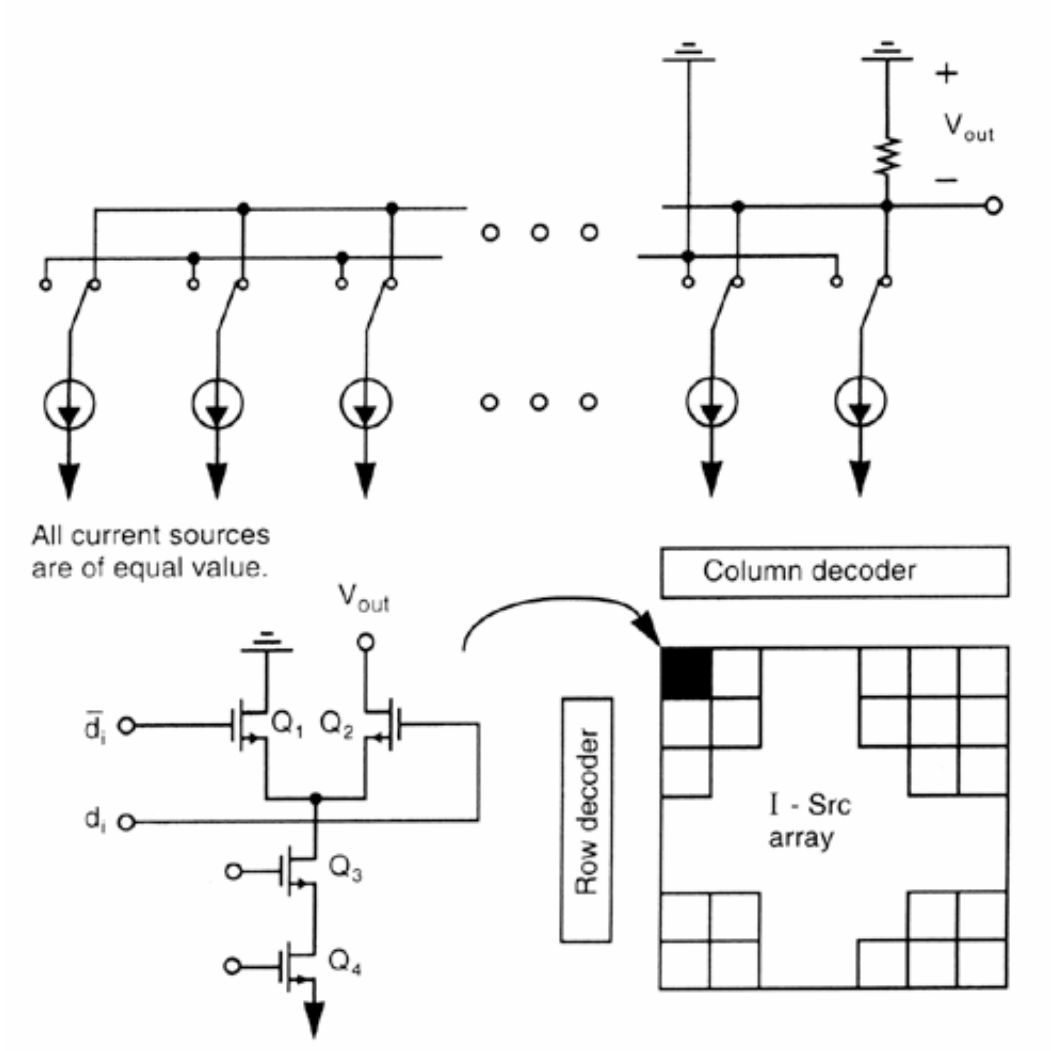
Glitches !

The Binary and thermometer codes

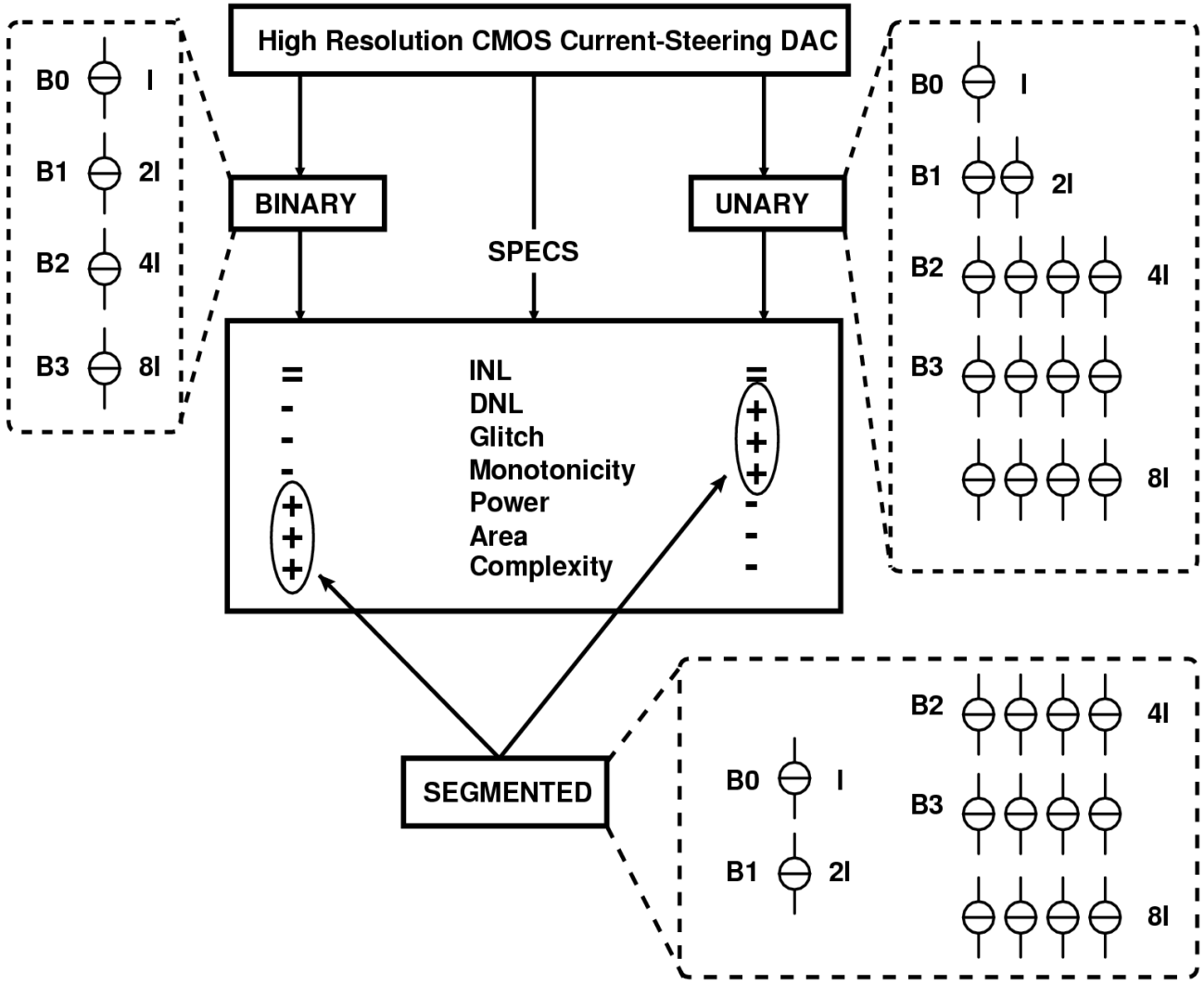
Decimal	Binary			Thermometer Code						
	b_1	b_2	b_3	d_1	d_2	d_3	d_4	d_5	d_6	d_7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

Monotonicity guaranteed !

Thermometer-code Current steering DAC



Binary, unary, segmented DAC



$\sigma(\Delta I) =$

Binary

$$\sqrt{2^N - 1}\ \frac{\sigma(I)}{I}\ \text{LSB}$$

Unary

$$\frac{\sigma(I)}{I}\ \text{LSB}$$

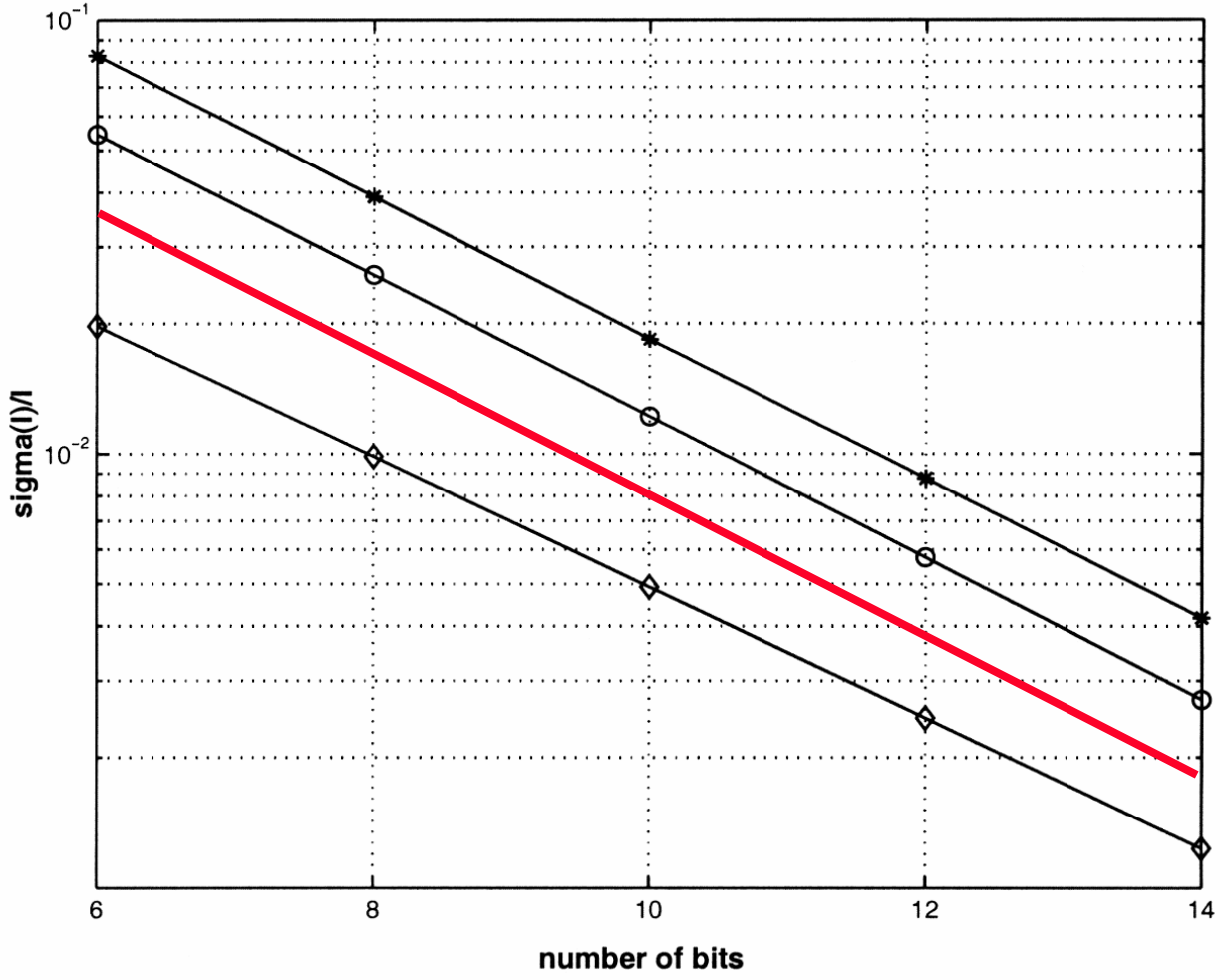
Segmented

B LSBs & N-B MSBs

$$\sqrt{2^{B+1} - 1}\ \frac{\sigma(I)}{I}\ \text{LSB}$$

Van den Bosch, .., Kluwer 2004

σ(I)/I versus resolution



$$\frac{\sigma(I)}{I} = \frac{1}{2\,C\,\sqrt{2^N}}$$

$C \approx 6.2\ 10^{-4}$
for INL_yield = 90%

Yield =

10 %

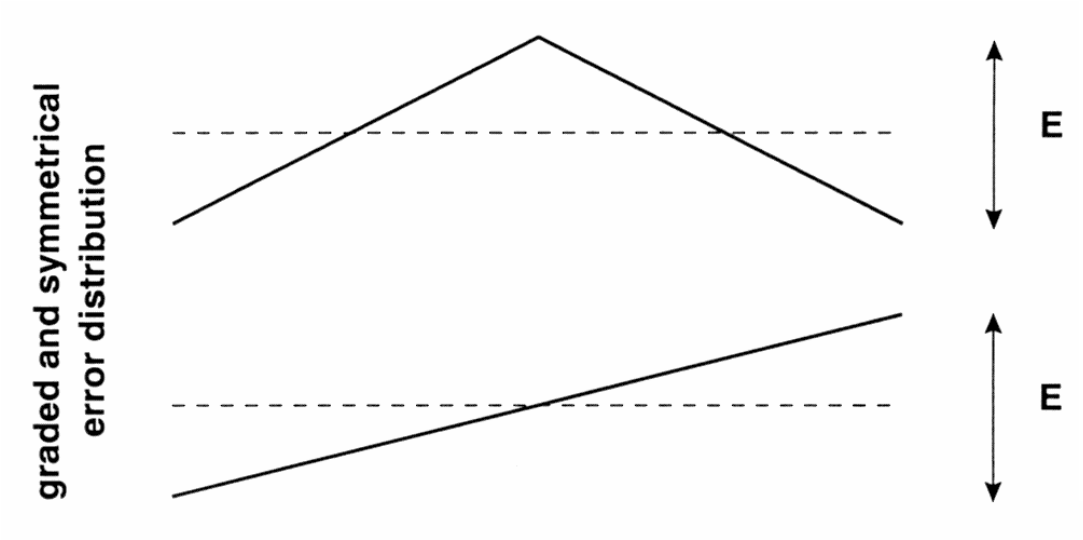
50 %

90 %

99.7 %

Van den Bosch, ..,
Kluwer 2004

Switching schemes

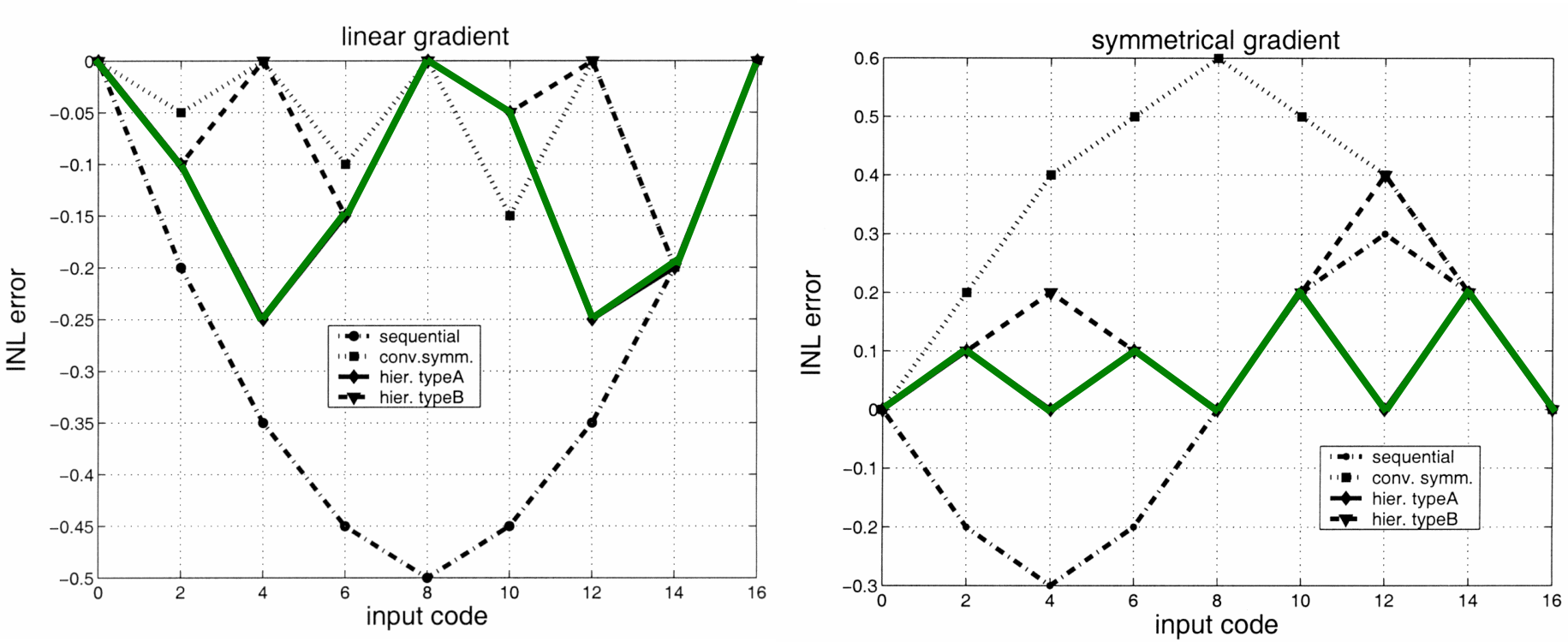


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	sequential scheme
15 13 11 9 7 5 3 1 2 4 6 8 10 12 14 16	conventional symmetrical scheme
14 10 6 2 1 5 9 13 15 11 7 3 4 8 12 16	hierarchical symmetrical scheme (type A)
15 11 7 3 1 5 9 13 14 10 6 2 4 8 12 16	hierarchical symmetrical scheme (type B)

is centroide !

Van den Bosch, .., Kluwer 2004
Miki, JSSC Dec.86, 983-988

INL error for different switching schemes



Hierarchical symmetrical scheme (type A)

DAC Design: Static Accuracy

INL_yield = percentage of functional D/A converters with an INL specification smaller than half an LSB.

$$\text{INL\_yield} = f(\text{mismatch}) = f\left(\frac{\sigma(I)}{I}\right)$$

$$WL = \frac{1}{2\left(\frac{\sigma(I)}{I}\right)^2}\left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)^2}\right]$$

High yield ⇩ **small** $\frac{\sigma(I)}{I}$ ⇩ **Large current source area**

$$\frac{\sigma(I)}{I} \le \frac{1}{2C\sqrt{2^N}} \quad \Rightarrow \quad \boxed{\sigma(I_{unit})/I_{unit} = 0.25\ \%}$$

DAC Design: Calculation W and L

$$\frac{W}{L} = \frac{I_{LSB}}{K' (V_{GS}-V_T)^2}$$

$$WL = \frac{1}{2\left(\frac{\sigma(I)}{I}\right)^2}\left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)^2}\right]$$

$\sigma(I)/I = 0.0025$

$V_{GS}-V_T = 1$ V

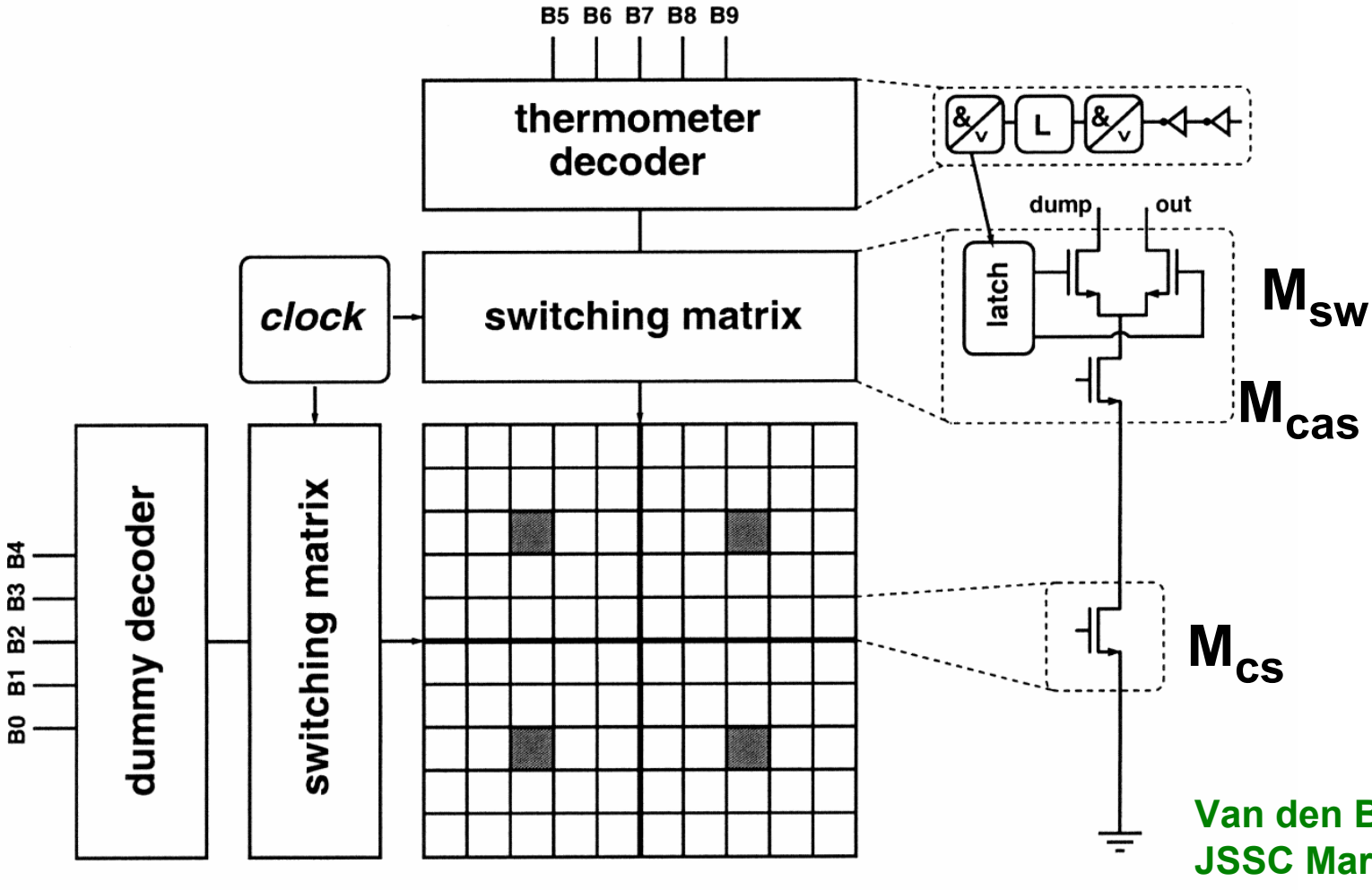
For 0.35 μm CMOS $A_\beta \approx 2$ %μm

$A_{VT} \approx 7$ mVμm

W = 1.8 μm

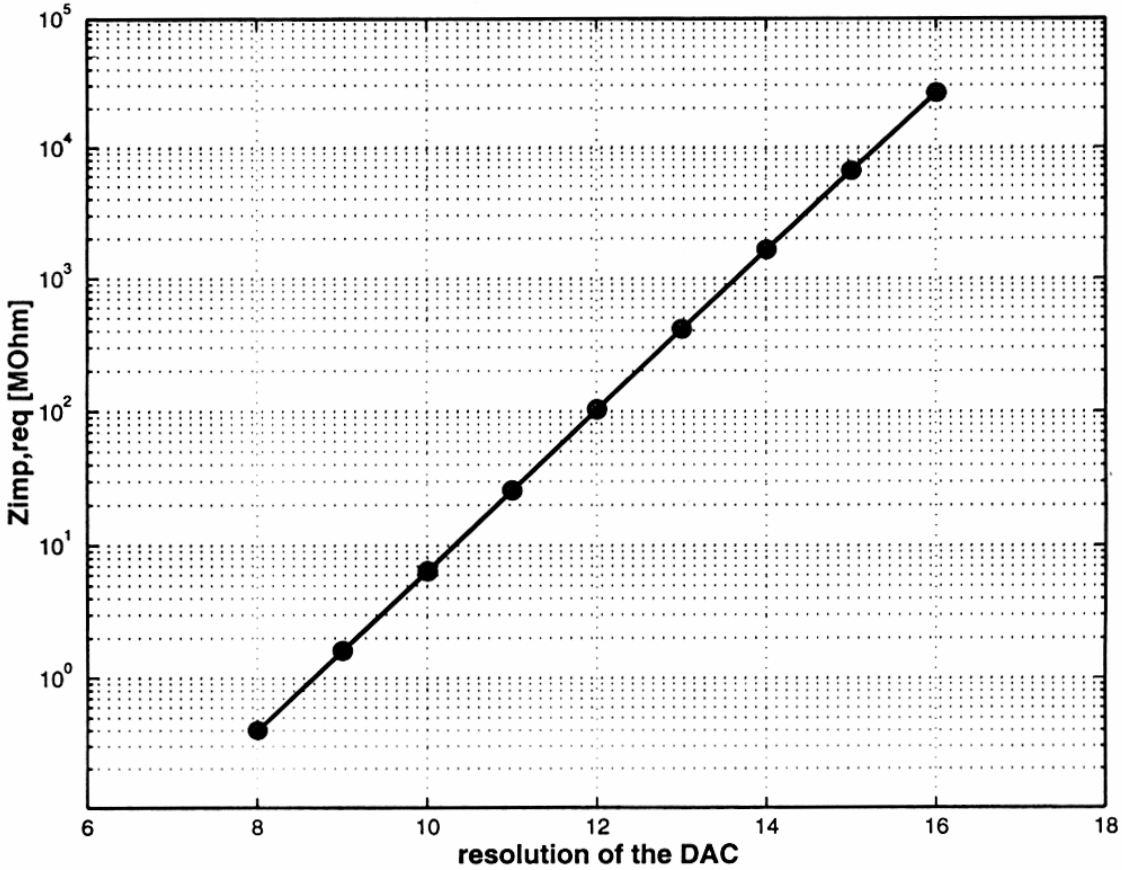
L = 30 μm

Floorplan 10-bit segmented DAC



Van den Bosch, ..,
JSSC March 01, 315-324

Required output impedance versus resolution



A_{VT}	$8.94\ mV\mu m$
A_β	$1.9\ \%\mu m$
$\sigma(I)/I$	0.5 %
$(V_{GS}-V_T)_{cs}$	1 V
I_{FS}	20 mA
segmentation	5-5
$(W/L)_{cs}$	$2\mu m/8\mu m$
$(W/L)_{sw}$	$1\mu m/0.7\mu m$
$(W/L)_{cas}$	$0.5\mu m/0.35\mu m$

10 bit 1GB/s

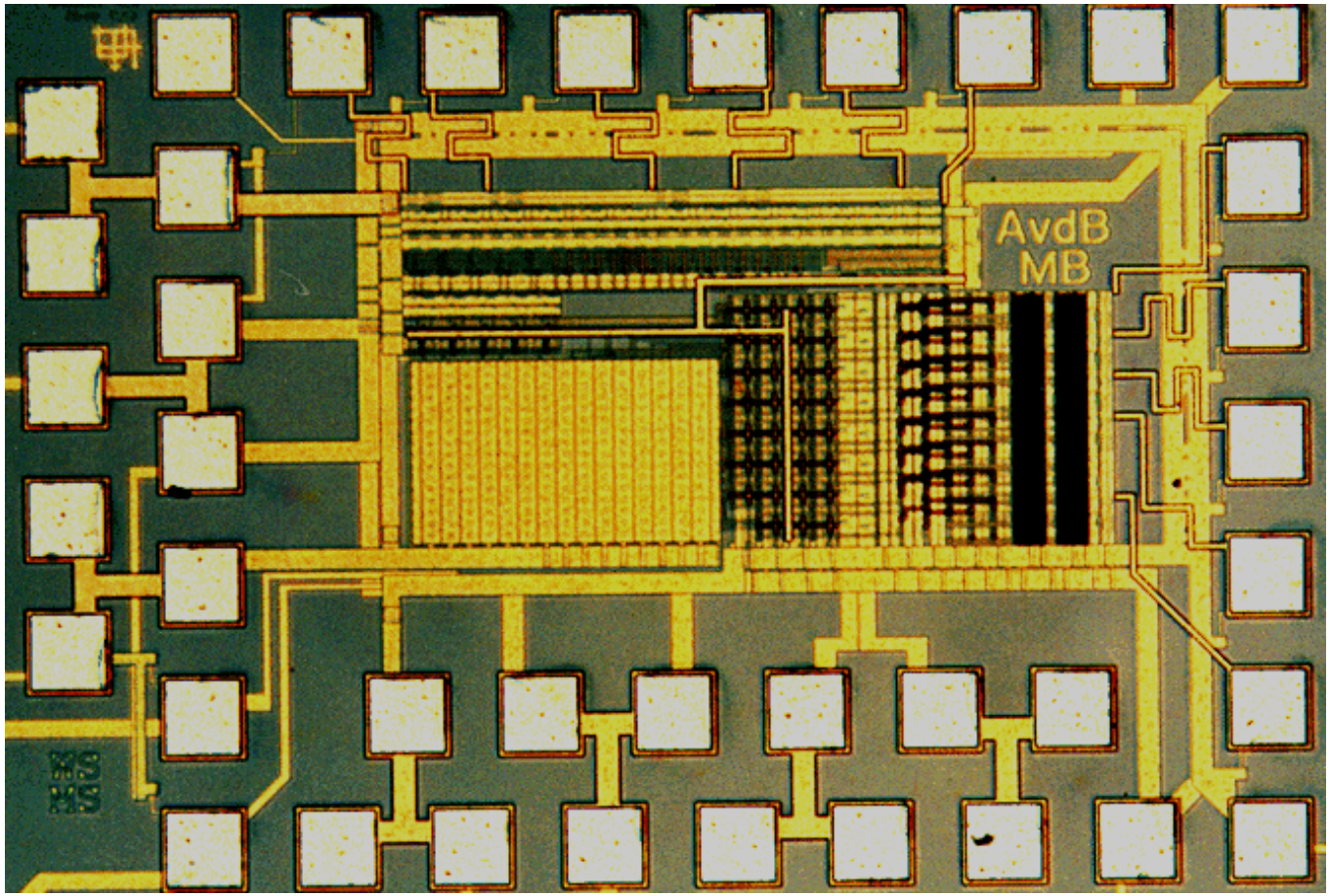
INL = 99.7 %

requires σ(I)/I < 0.5 % :

W = 2 μm & L = 8 μm

Van den Bosch, .., Kluwer 2004
JSSC March 01, 315-324

10-bit 1 GS/s Nyquist Current steering CMOS DAC



Current steering DAC

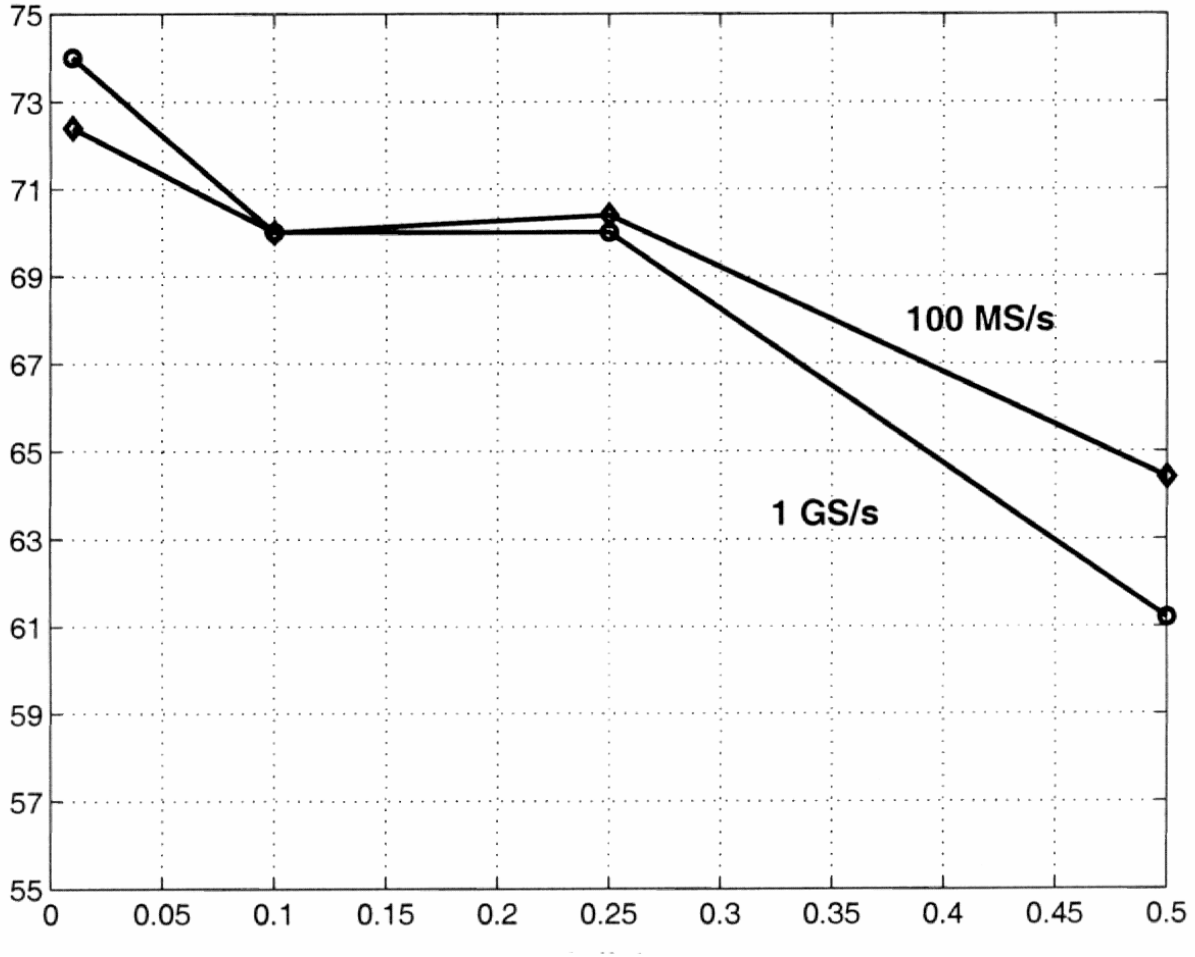
- **10-bit**
- **1 GS/s**

0.35 μm CMOS

- **110 mW**

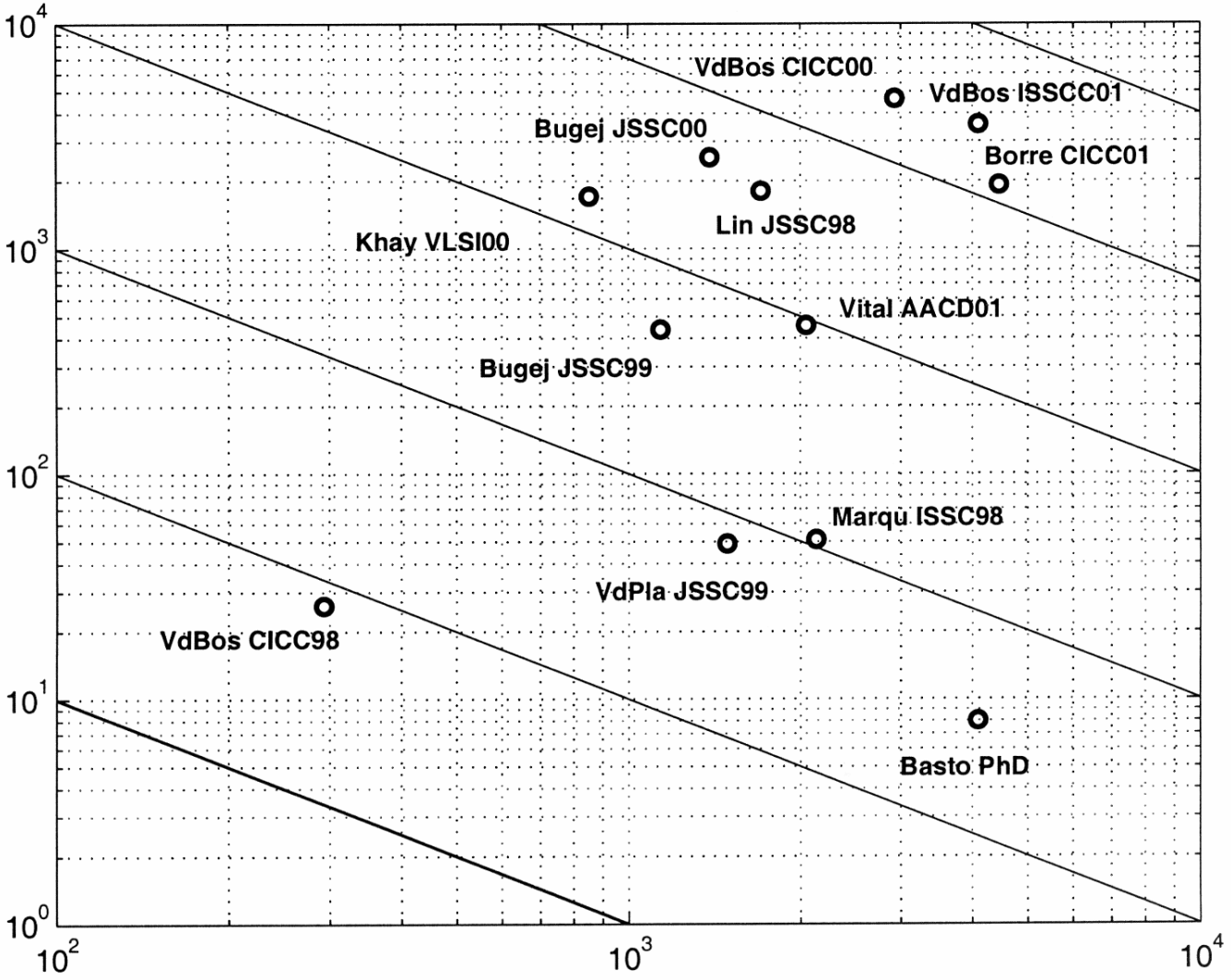
Van den Bosch, .., JSSC, March 01, 315-324

SFDR (dB) versus relative signal frequency



f_{signal} / f_{clock}

FOM (MHz/mW) vs inverse area



$$\text{FOM} = \frac{2^N f_s(-6\text{dB})}{P}$$

2^N/area (mm^2)

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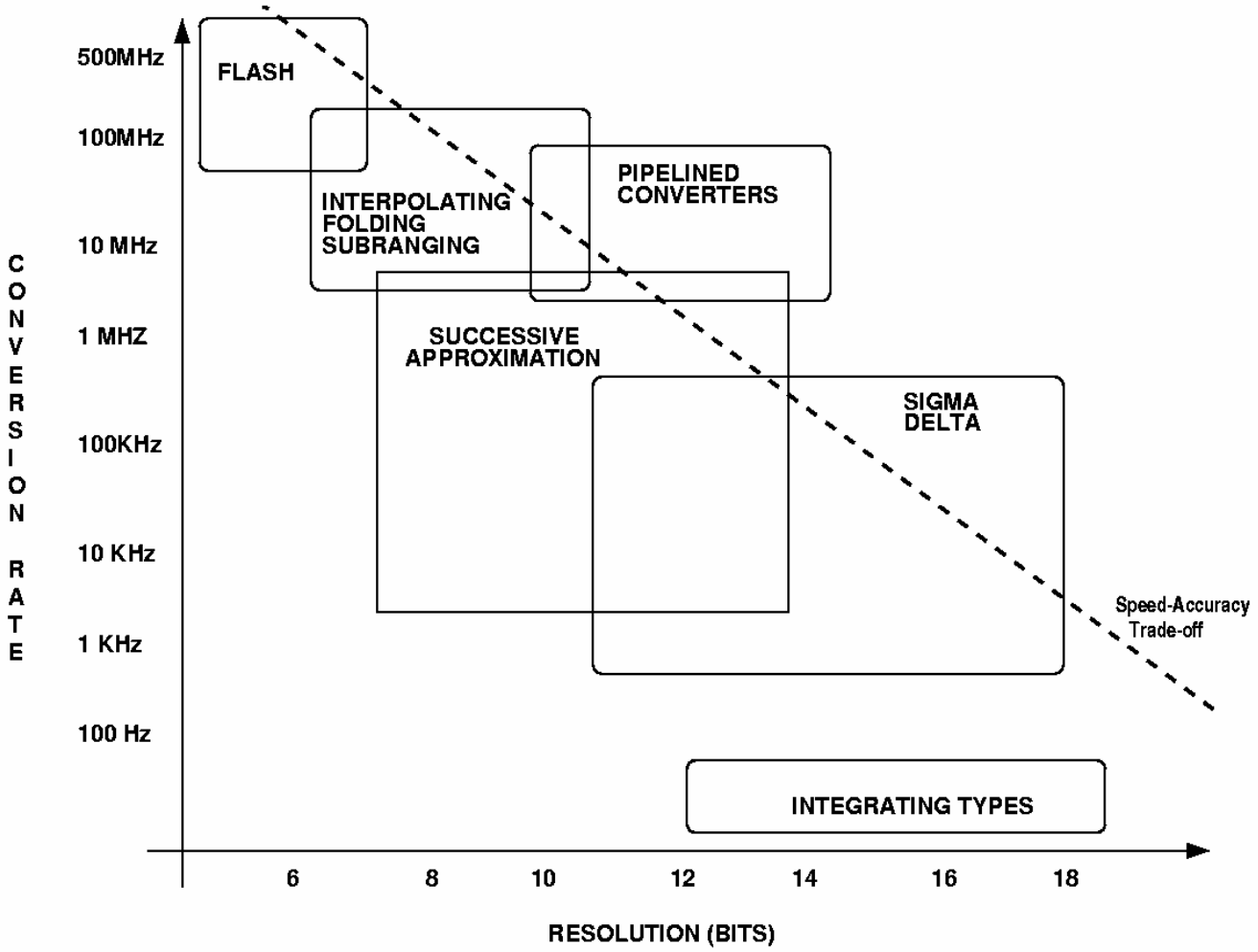
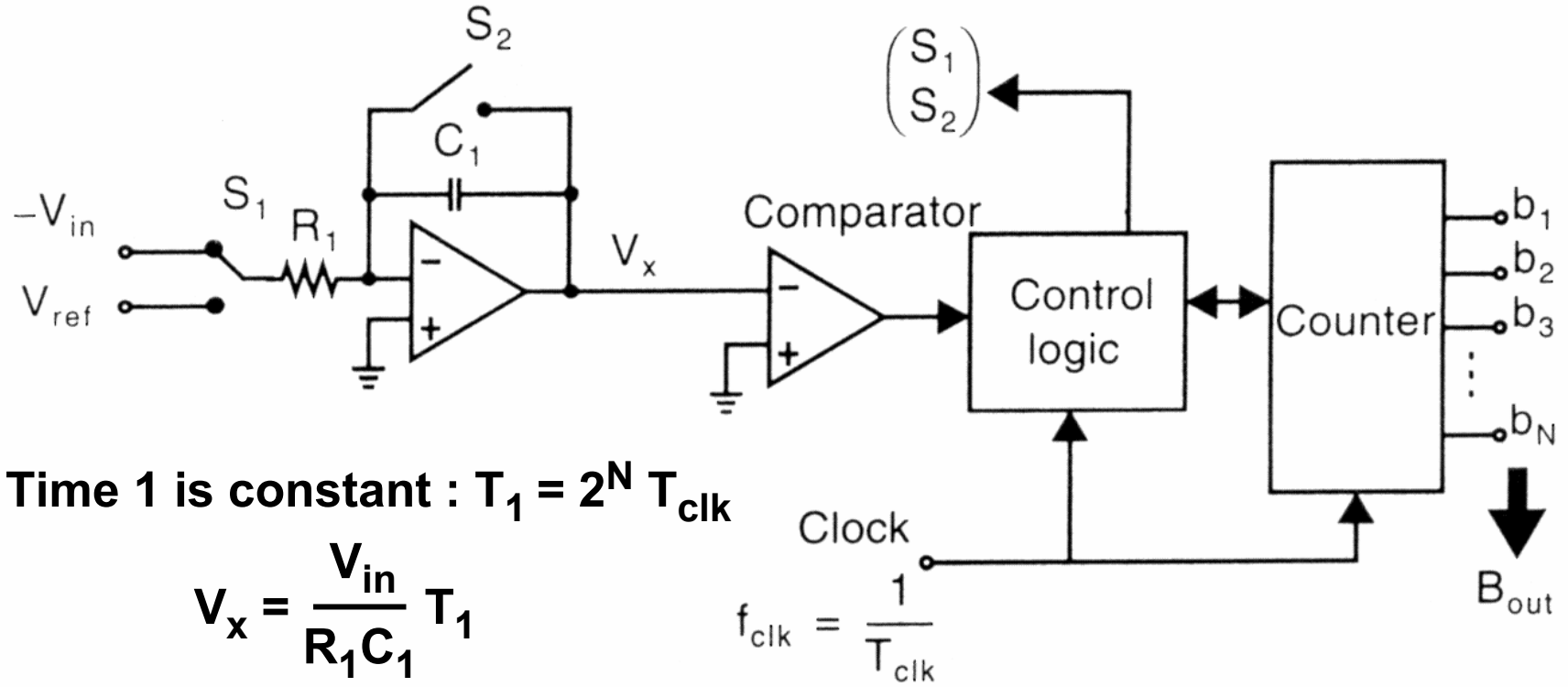
Speed Resolution Limits ADC



$$FOM = \frac{4kT\ BW\ DR}{P}$$

$$\frac{2^N\ 2BW}{P}$$

Dual-slope (integrating) ADC



Time 1 is constant : $T_1 = 2^N T_{clk}$

$$V_x = \frac{V_{in}}{R_1 C_1} T_1$$

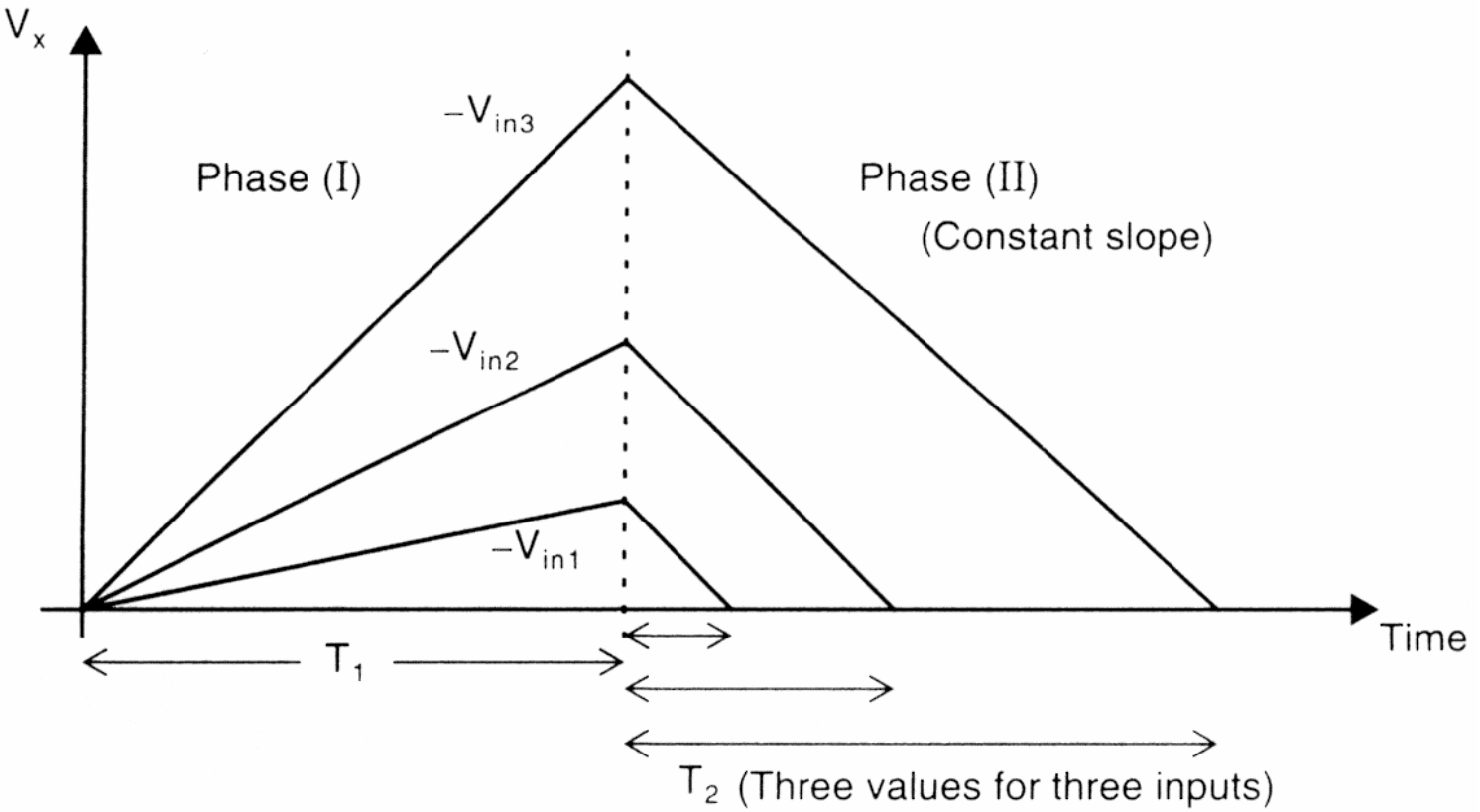
$$f_{clk} = \frac{1}{T_{clk}}$$

Time 2 : V_x decreases with constant slope :

$$V_x = \frac{V_{ref}}{R_1 C_1} T_2 \qquad T_2 = T_1 \frac{V_{in}}{V_{ref}} \Rightarrow B_{out} = \frac{V_{in}}{V_{ref}}$$

Johns, Martin, Wiley 1997

Operation of integrating ADC



Time 1 : $V_x = \frac{V_{in}}{R_1 C_1} T_1$ **Time 2 :** $V_x = \frac{V_{ref}}{R_1 C_1} T_2$ $T_2 = T_1 \frac{V_{in}}{V_{ref}}$

Integrating ADC

Advantages:

High resolution

High linearity

Low circuit complexity

Mainly for voltmeters, …

Eliminates mains supply 50 Hz if T1 is n x 20 ms

Disadvantages:

Very slow :

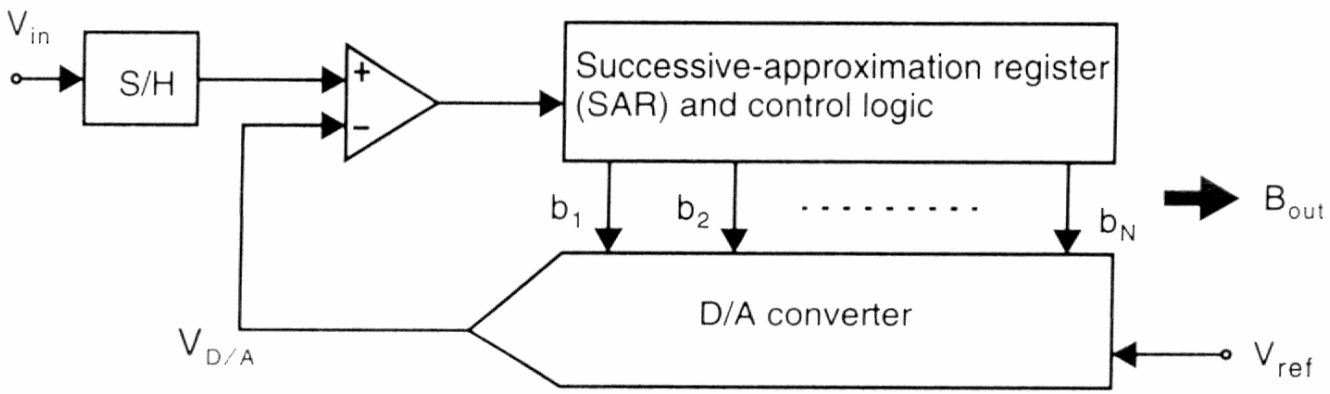
Worst case for $V_{in} = V_{ref}$: 2^{2n+1} clock cycli required !

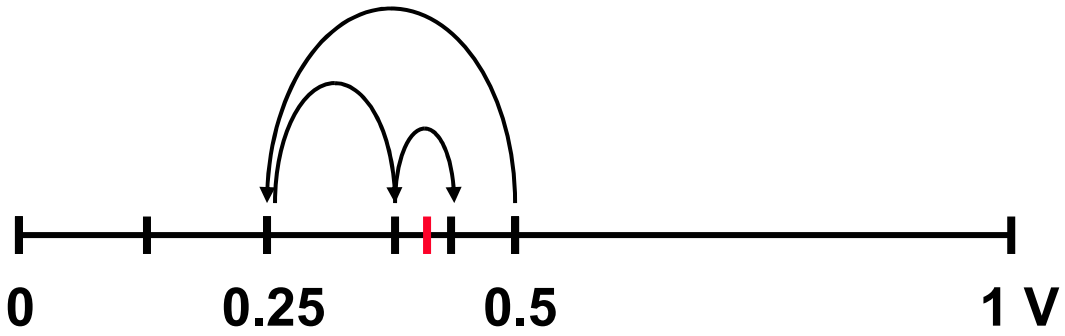
Ex. For n = 16 bit (64000) and F_{clock} = 1 MHz :

7.6 s conversion time

Mainly for voltmeters, …

Successive-approximation ADC





Divide interval by 2 ;

Determine bit :

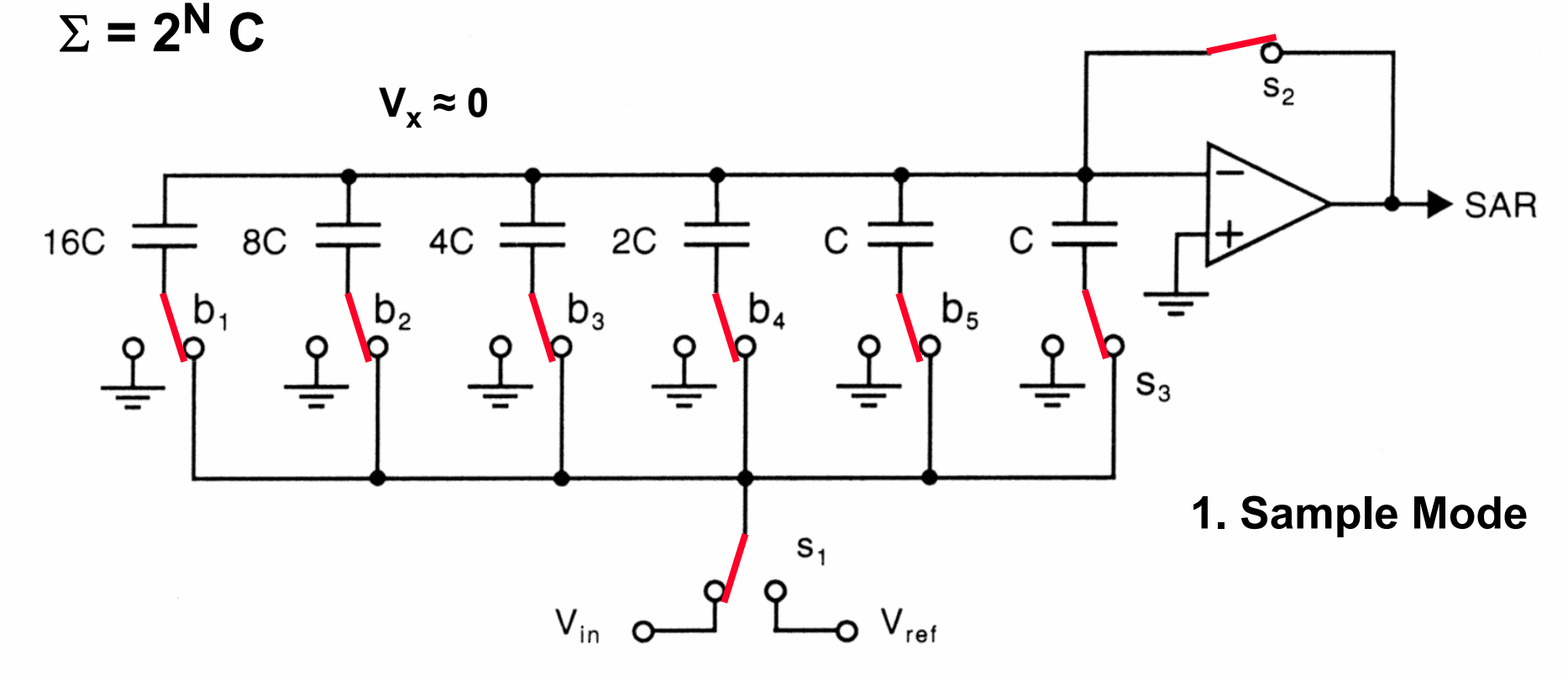
< 1	**: 0**	**b_1 = MSB**
< 0.5	**: 0**	**b_2**
> 0.25	**: 1**	**b_3**
> 0.375	**: 1**	**b_4**
< 0.4375	**: 0**	**b_5**

…..

Johns, Martin, Wiley 1997

5-bit Charge redistribution ADC

$\Sigma = 2^N C$



1. Sample Mode

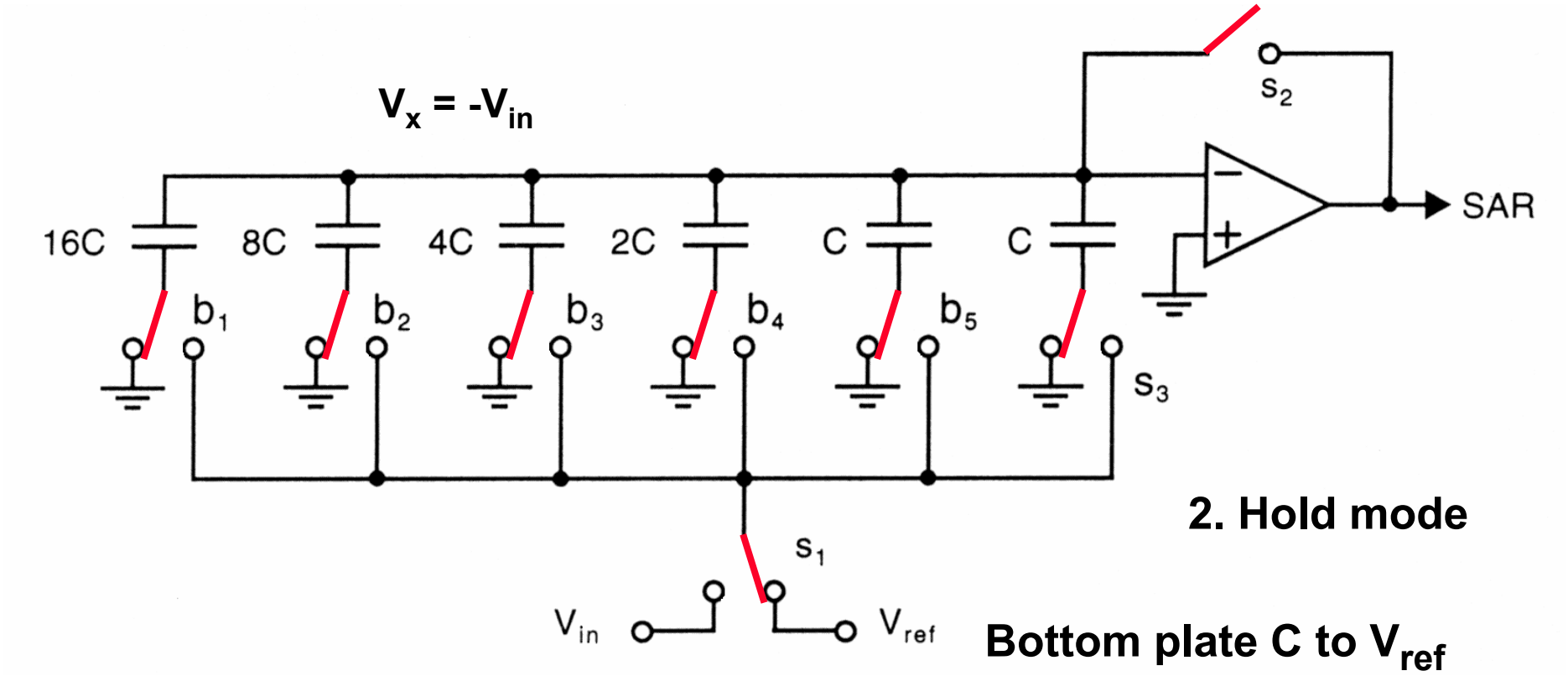
Accuracy limited by capacitive matching to 10-12 bit

Speed limited by $R_{switch}C$ time constants

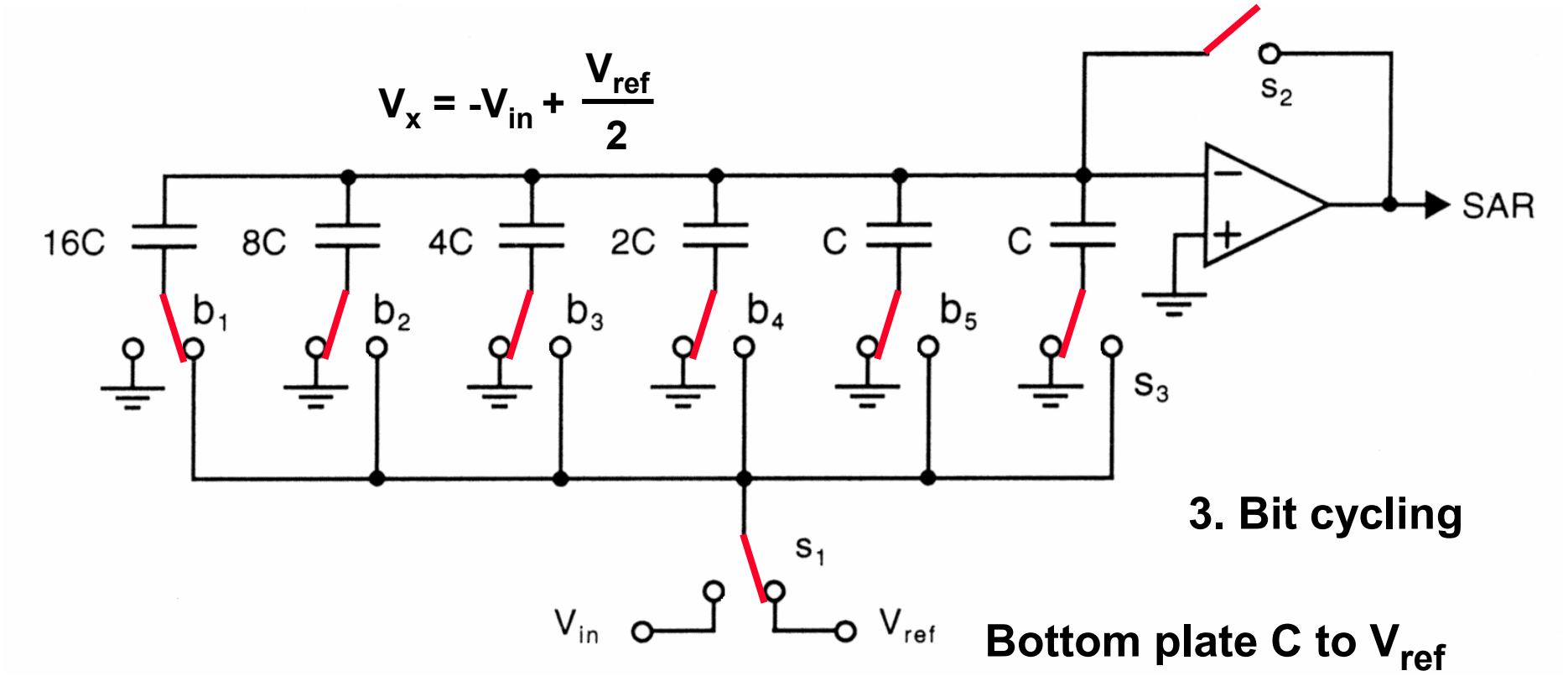
McCreary, JSSC Dec 75, 371-379

Johns, Martin, Wiley 1997

5-bit Charge redistribution ADC



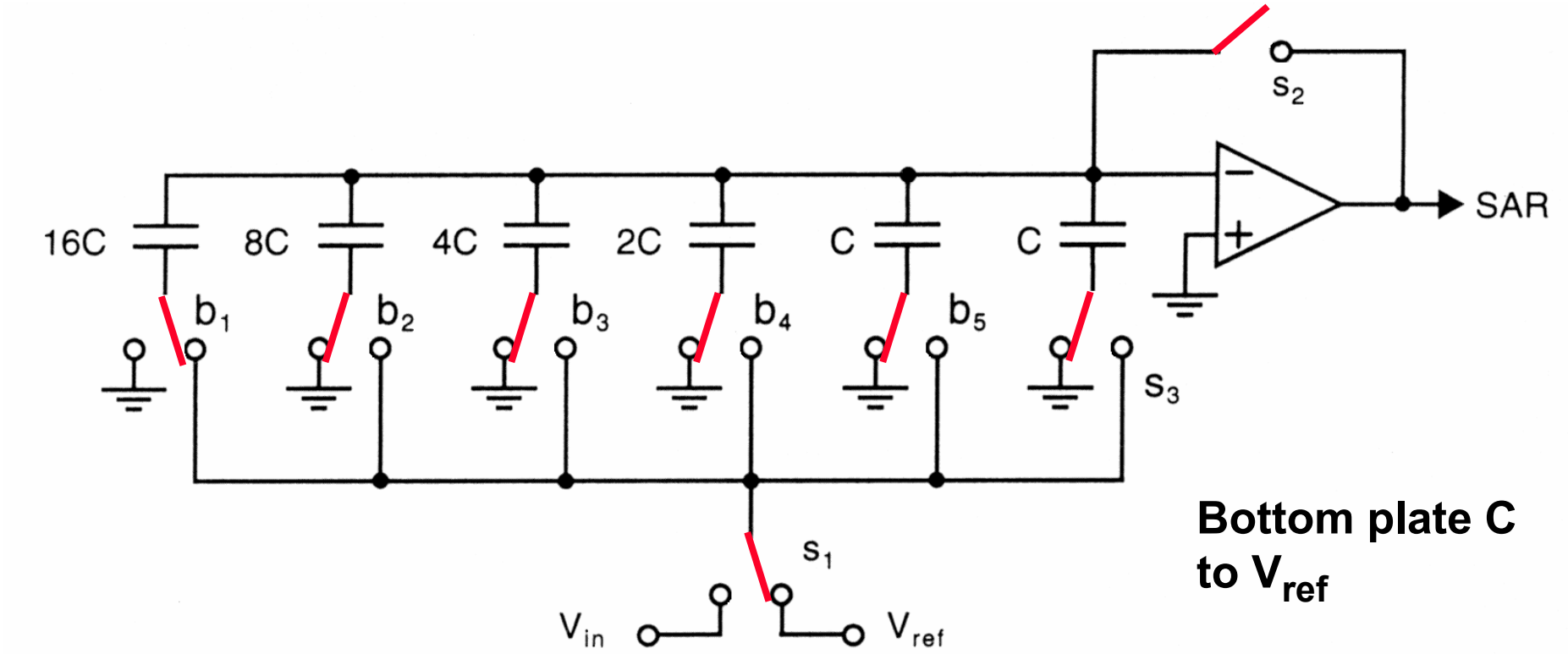
5-bit Charge redistribution ADC



if $V_{in} > V_{ref}/2$ SAR $\Rightarrow$ 1 leave C_{b1} to V_{ref} : try C_{b2}

if $V_{in} < V_{ref}/2$ SAR $\Rightarrow$ 0 leave C_{b1} to Gnd : try C_{b2}

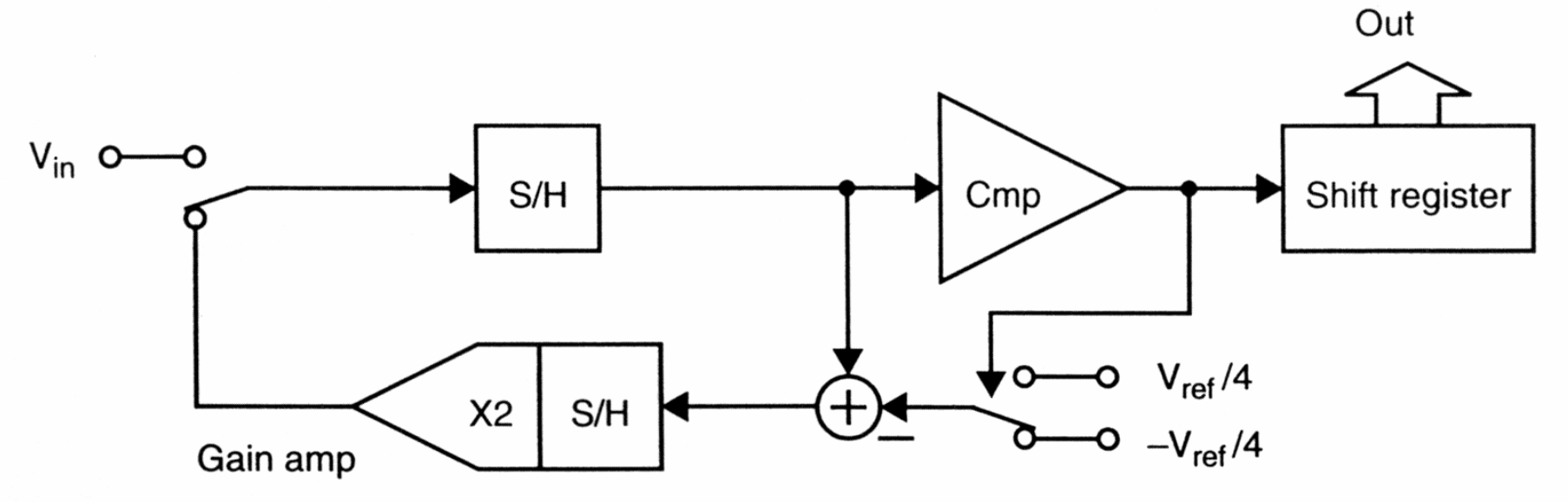
Charge redistribution ADC



Bottom plate C to V_{ref}

Charge redistribution ADC halves V_{ref} in each cycle
Algorithmic ADC doubles V_{error} in each cycle

Algorithmic (or cyclic) ADC



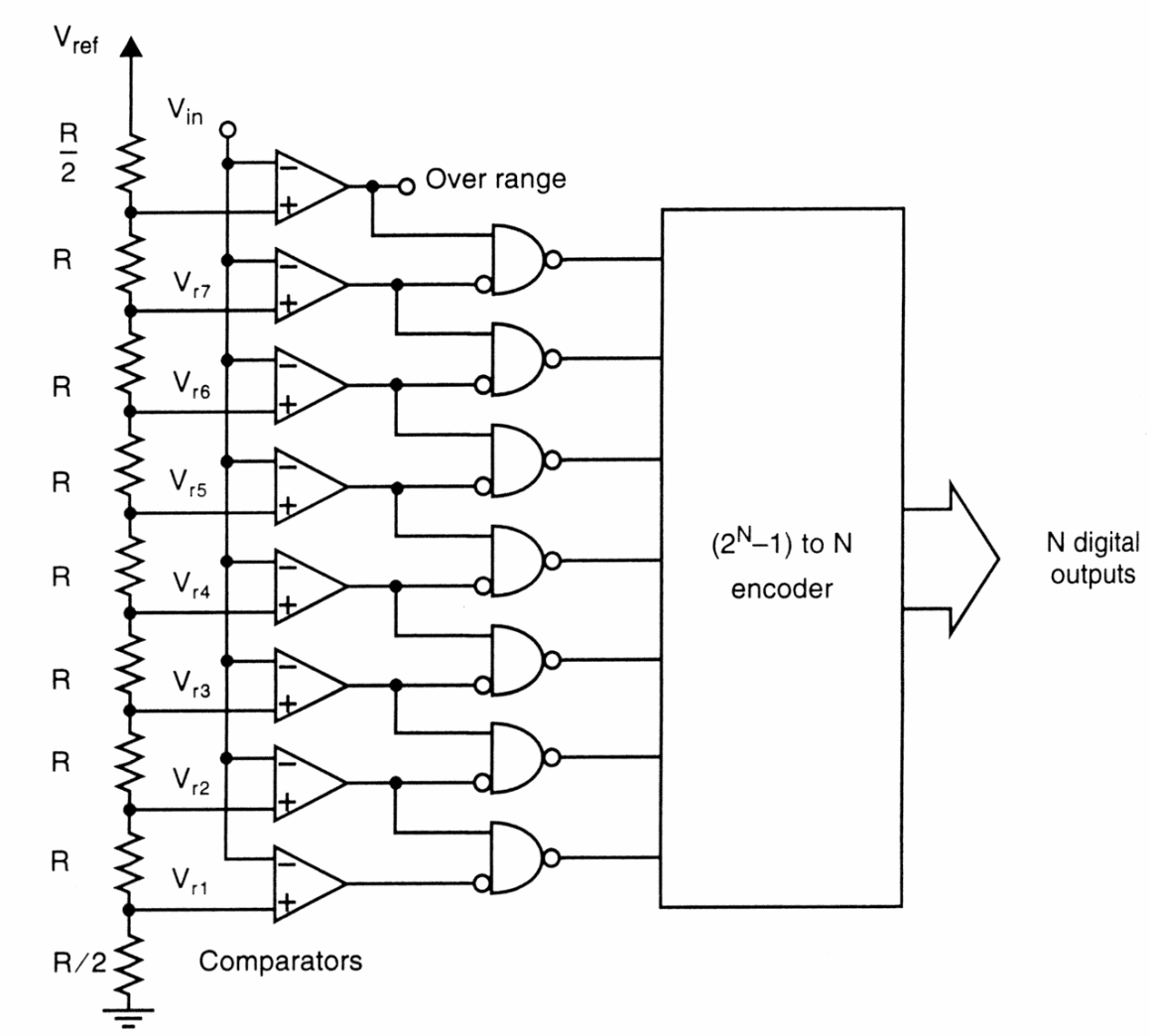
Advantage : small amount of analog circuitry

Difficulty : accuracy x2 Gain amplifier

(fully diff. ; C_{par} insensitive)

Johns, Martin, Wiley, 2003

Flash converter

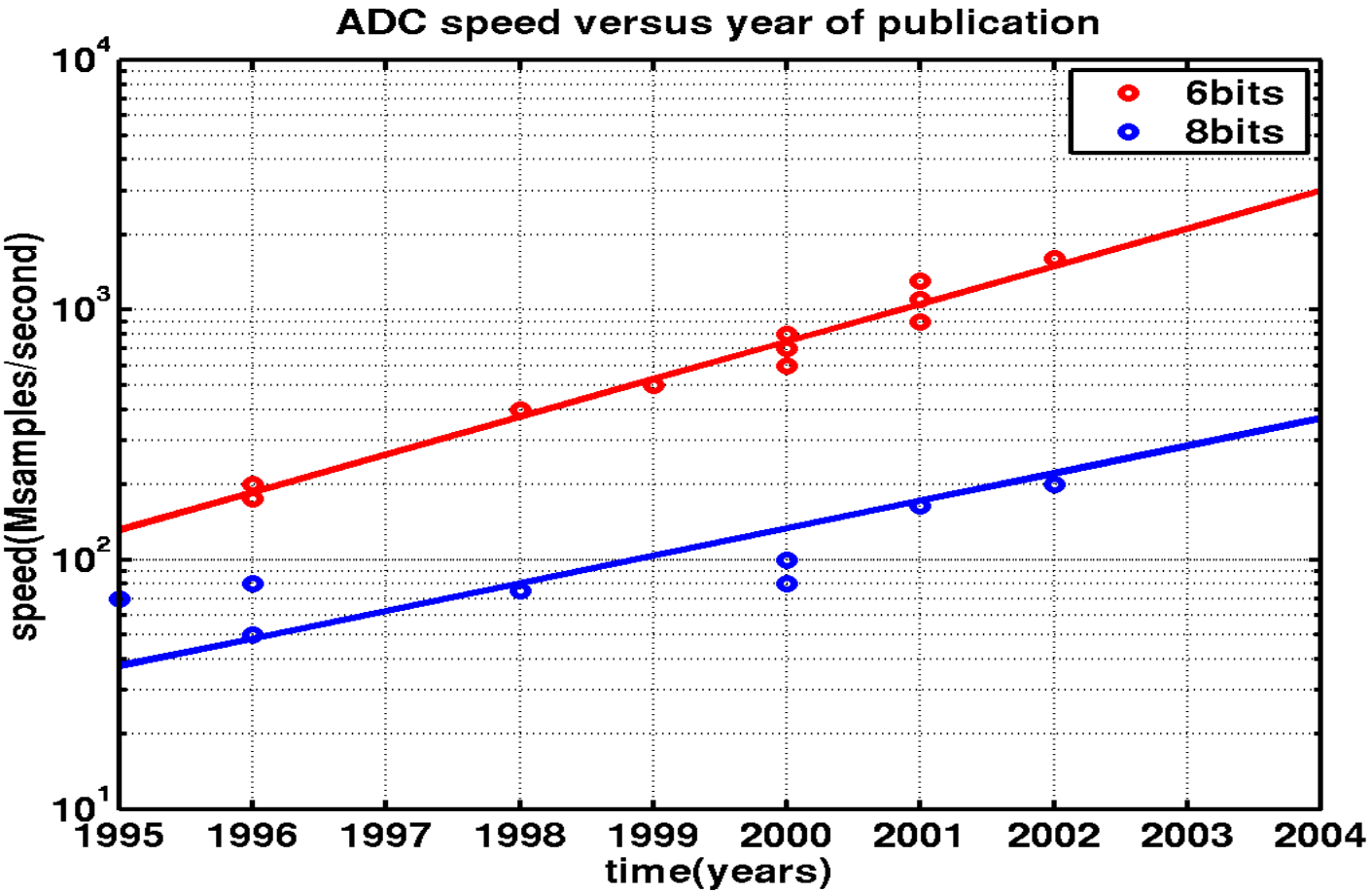


3-bit flash ADC :

fastest
2^3 comparators
input cap. ~ 2^3

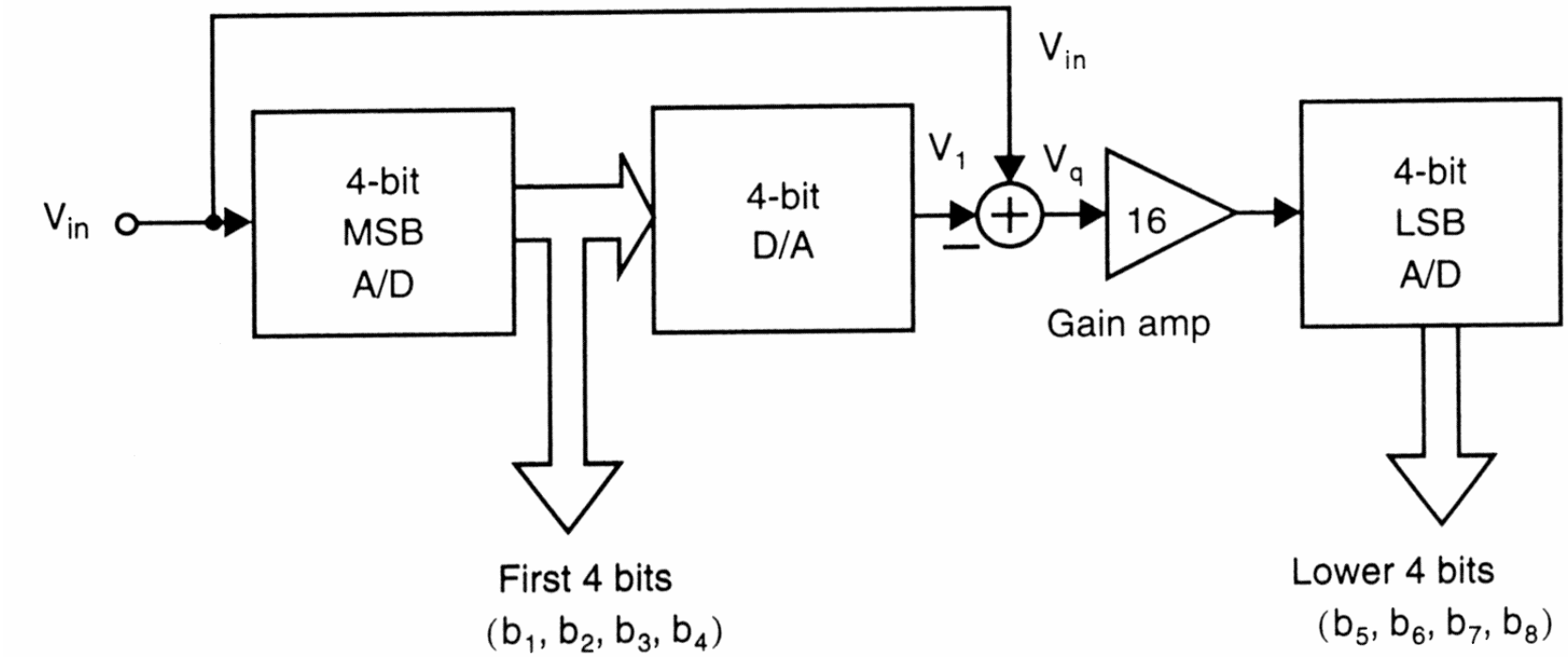
limited to 6 bit
(1 … 2 GS/s)

Evolution in ADC's



Uyttenhove, KULeuven, 2003

Subranging (or two-step) ADC

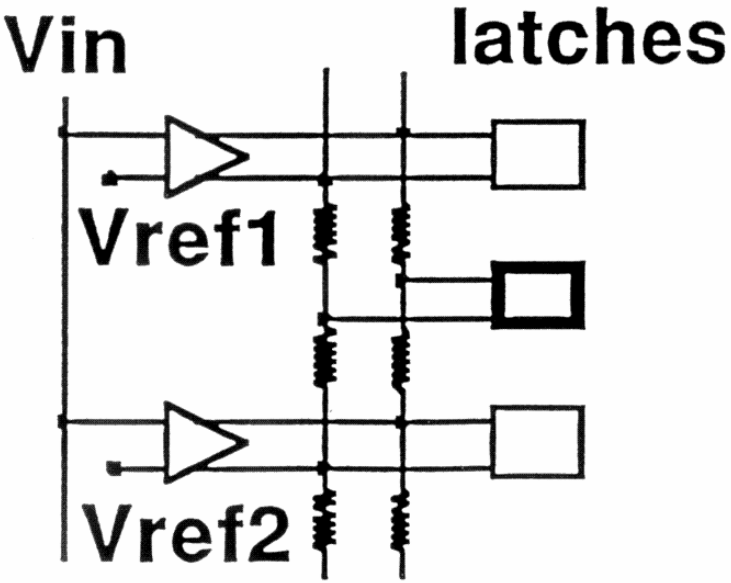


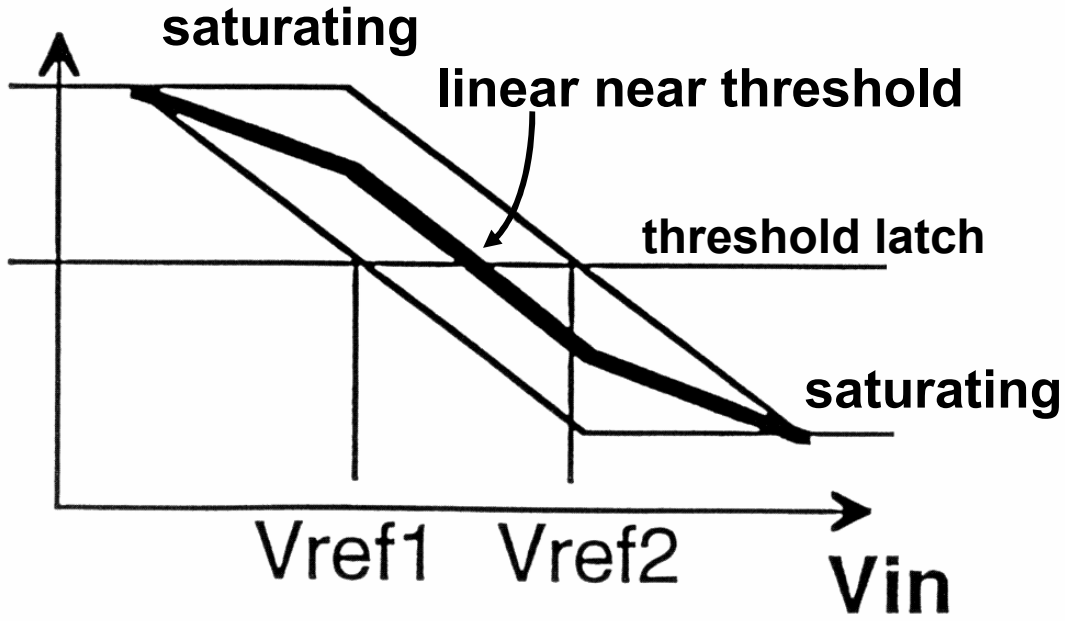
8-bit two-step ADC :
less comparators
introduces latency

2^8 = 256 comp. $\Longrightarrow$ now 32 !
All circuits : 8b accurate
Digital correction required !

Johns, Martin, Wiley 1997

Interpolating saves amplifiers

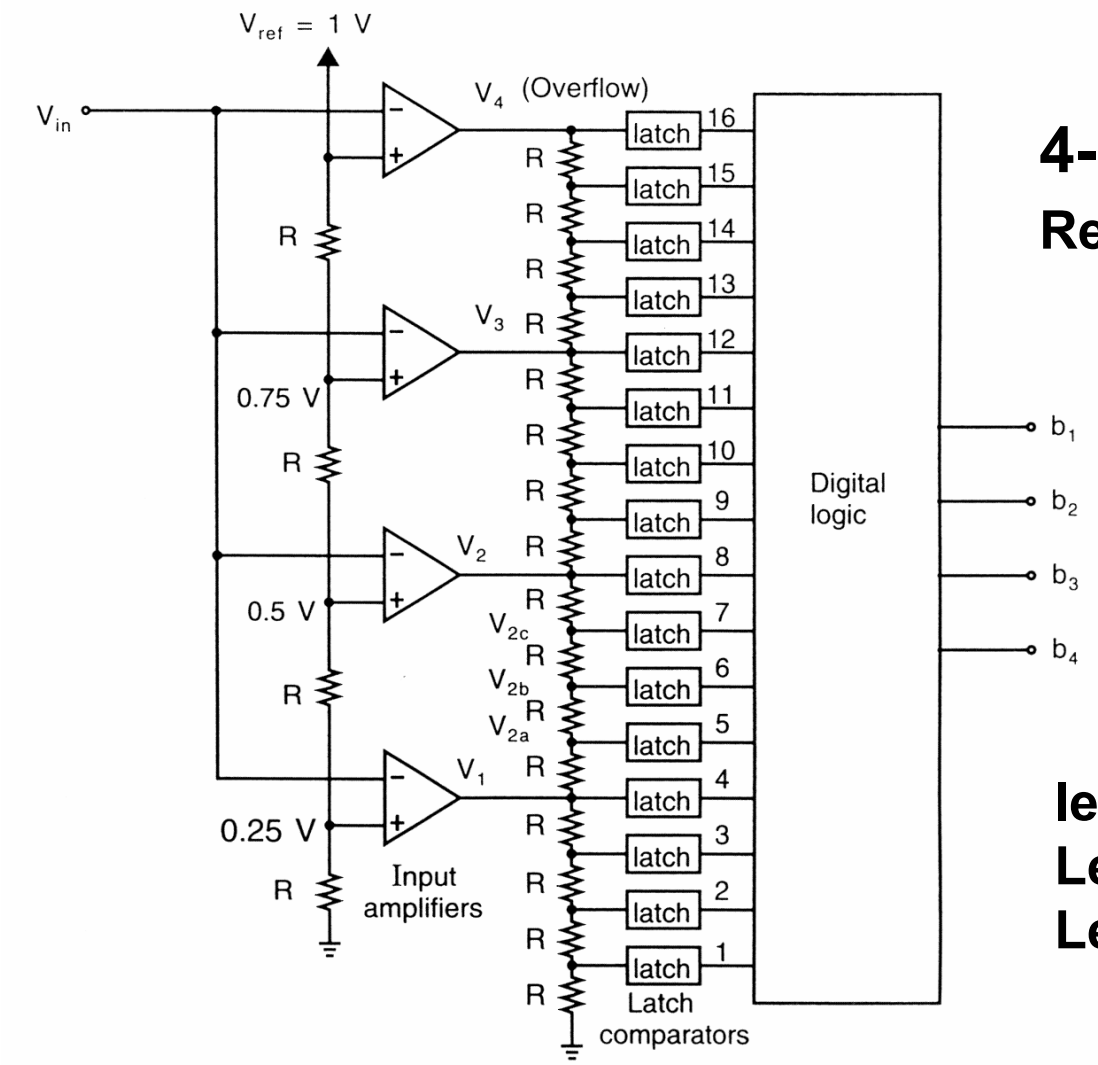




Input amplifiers which saturate

Van de Grift, JSSC Dec. 87, 944-953; Steyaert CICC 1993

Interpolating ADC



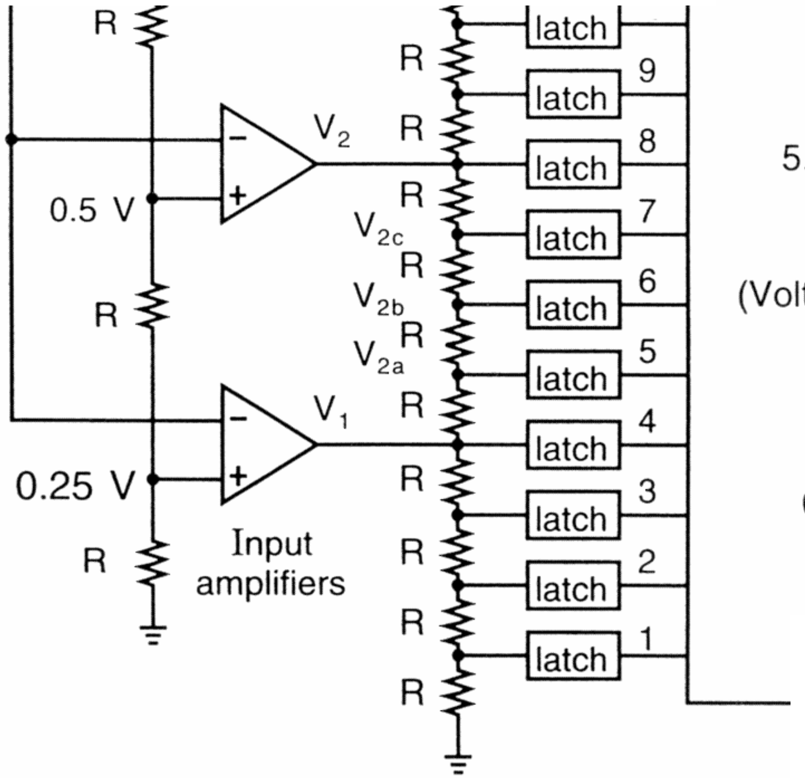
4-bit interpolating ADC

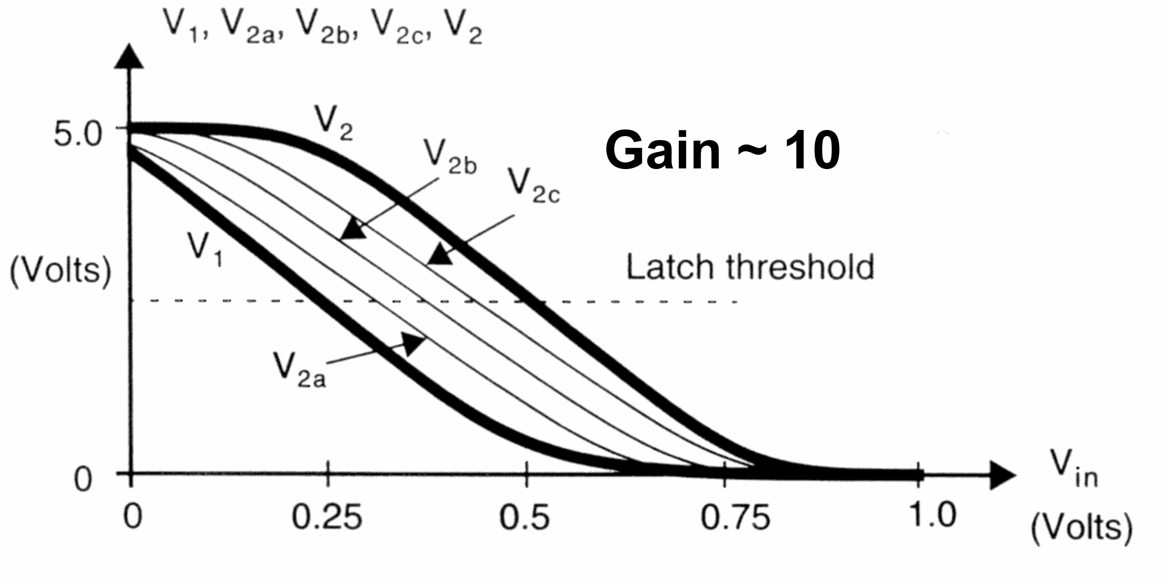
Resistive interpolation

leave out 3 out of 4 amps
Less power consumption
Less input capacitance

Johns, Martin, Wiley 1997

Transfer curves





Gain ~ 10

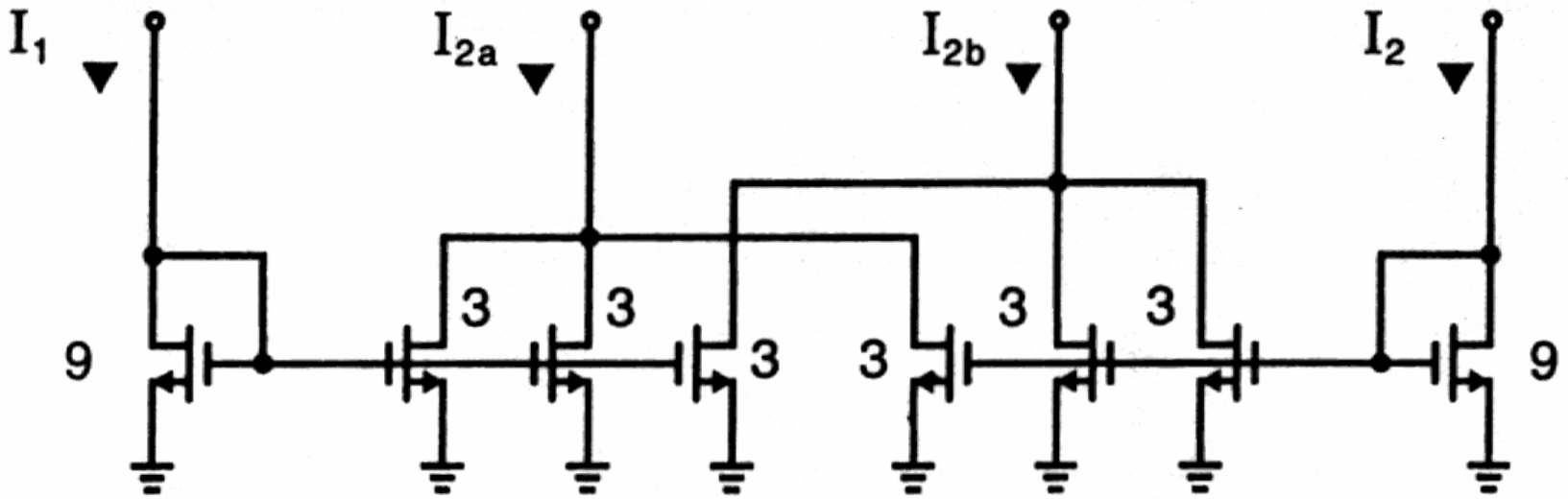
Only the zero crossings carry info

Resistors generate the intermediate outputs

Resistors average out offsets, etc.

Add series resistors to latch inputs to equalize delay times

Averaging with output currents



$$I_{2a} = \frac{2}{3} I_1 + \frac{1}{3} I_2$$

$$I_{2b} = \frac{1}{3} I_1 + \frac{2}{3} I_2$$

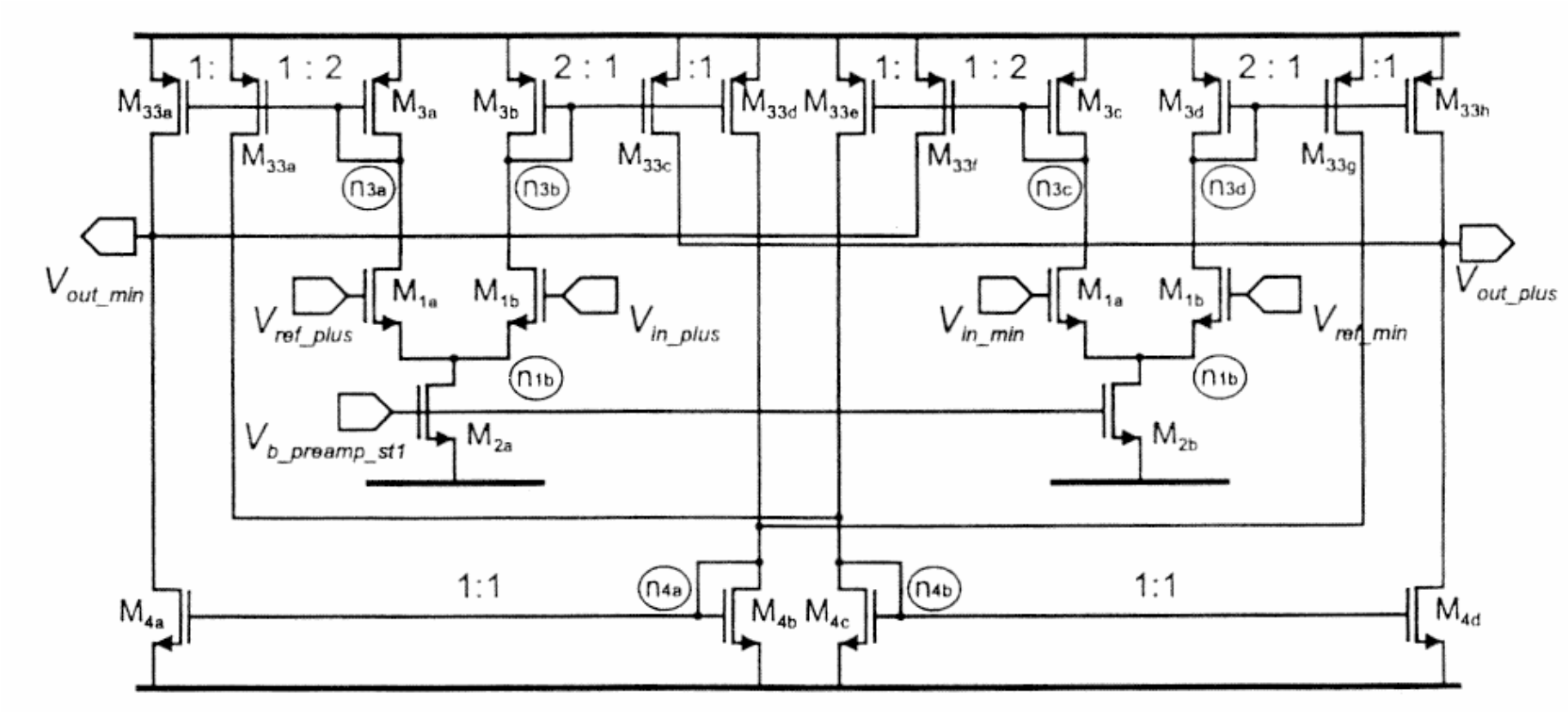
Interpolating by 3

between output currents I_1 & I_2

Requires 1/3 input amps.: $C_{in}/3$

Steyaert CICC 93

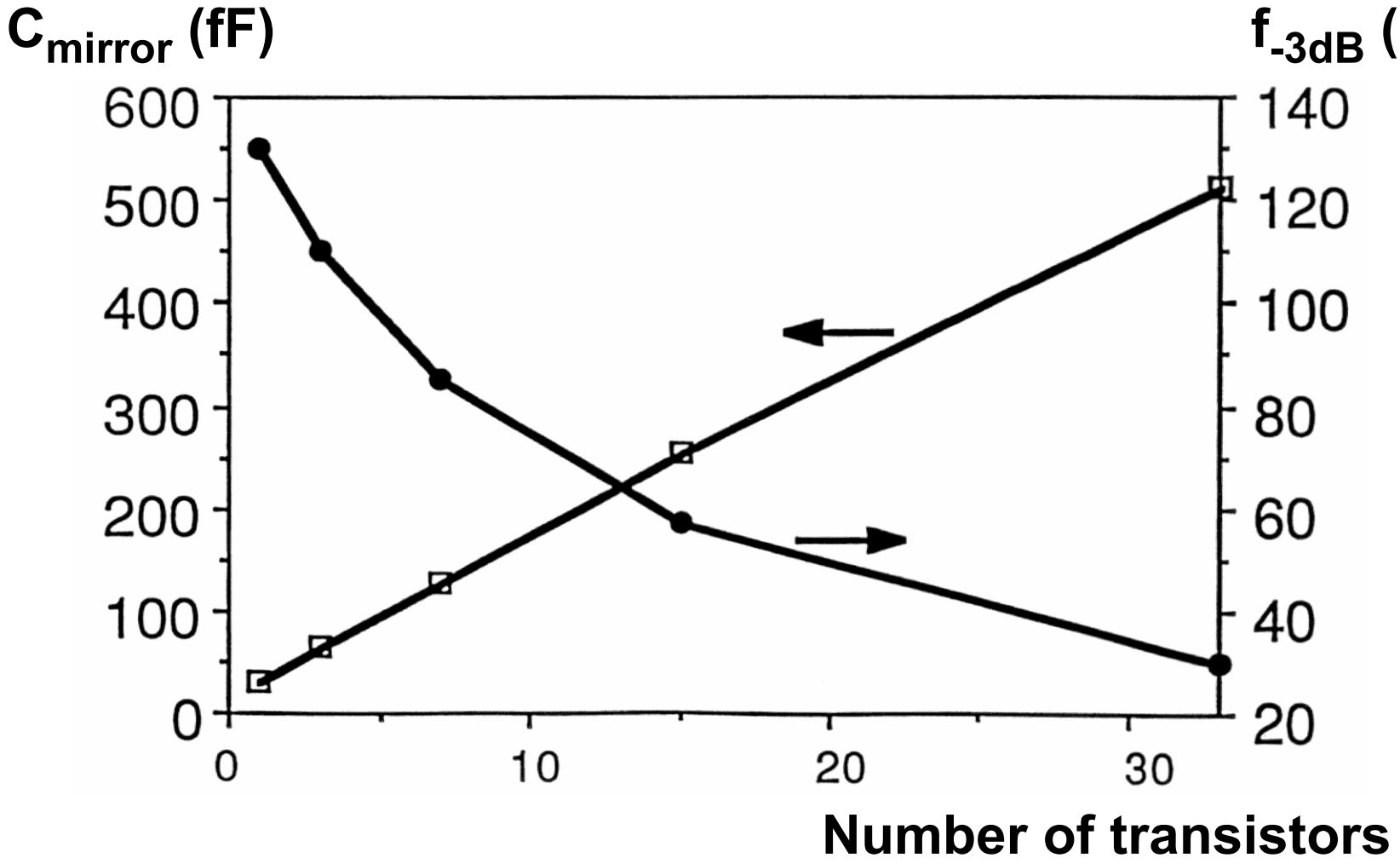
Interpolating/Averaging ADC - 1st amp



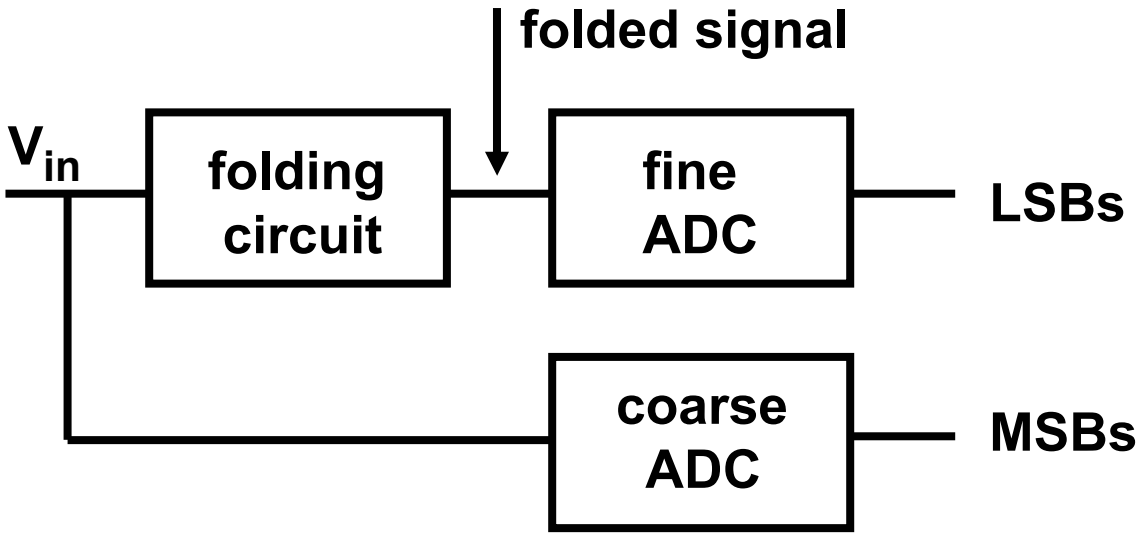
Current mirror interpolator

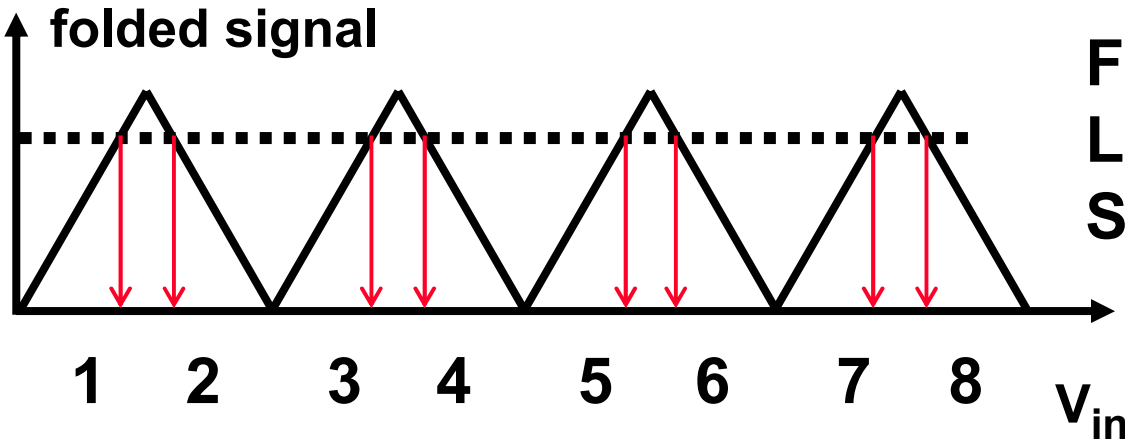
Steyaert CICC 93
Roovers JSSC July 96, 938-944

Interpolating : limitations



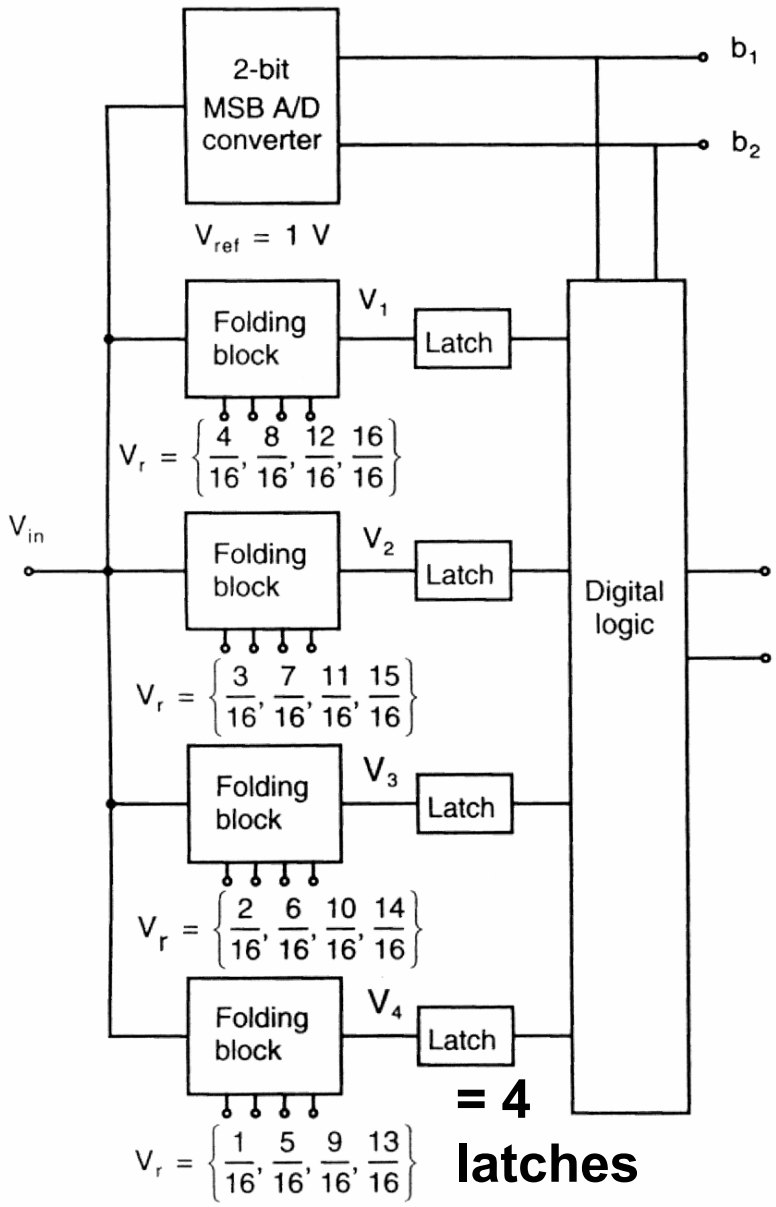
Folding ADC Analog preprocessing



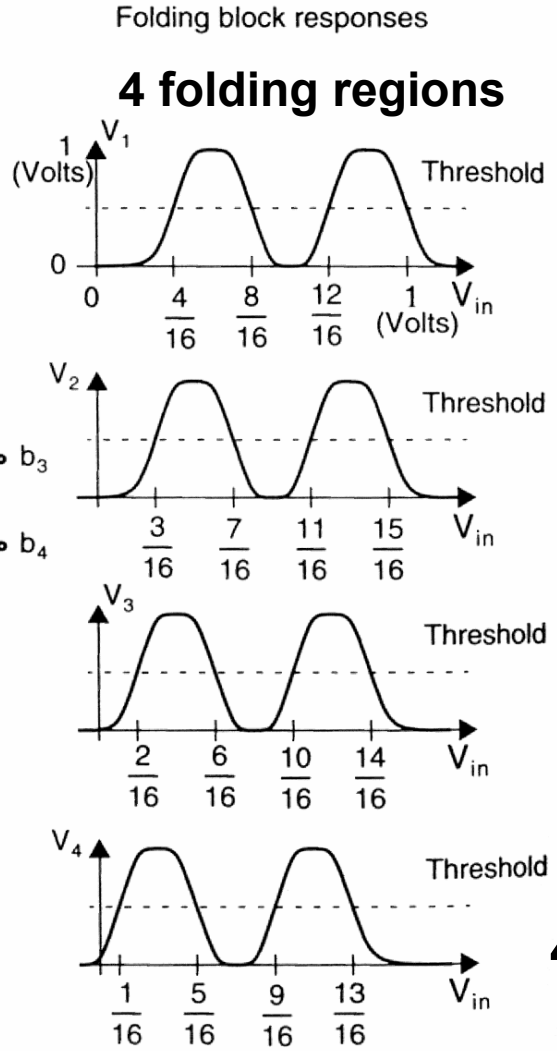


Folding rate 8
Less comparators
Same input capacitance

4-bit Folding ADC



= 4 latches



V_{in} starts

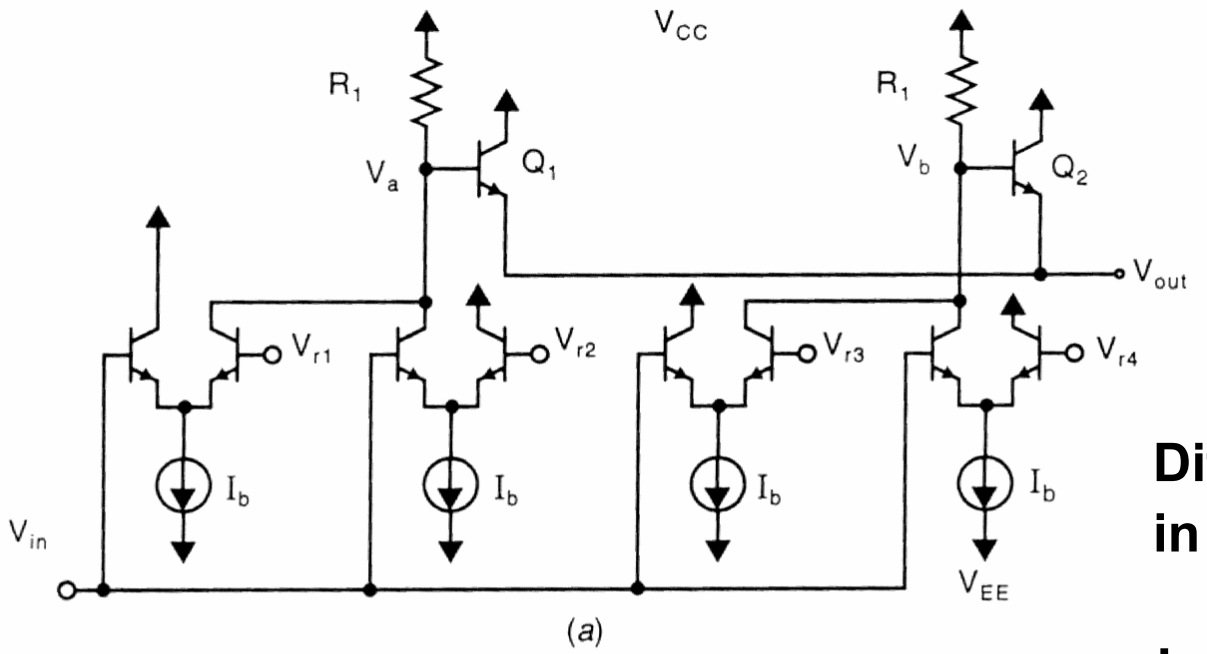
from 0 to 1/4 :
0001
0011
0111
1111

from 1/4 to 1/2 :
1110
1100
1000
0000

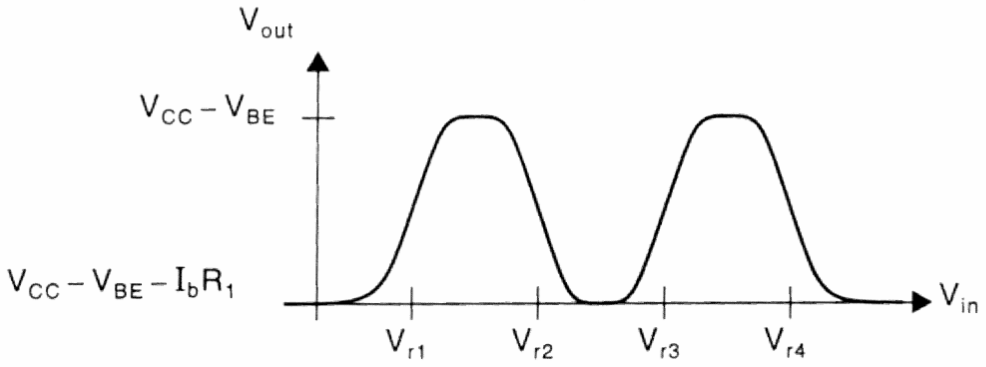
4-bit flash: 16 comp.
folding: 8 comp.

Johns, Martin, Wiley 1997

Folding block realization



(a)



Folding rate of 4

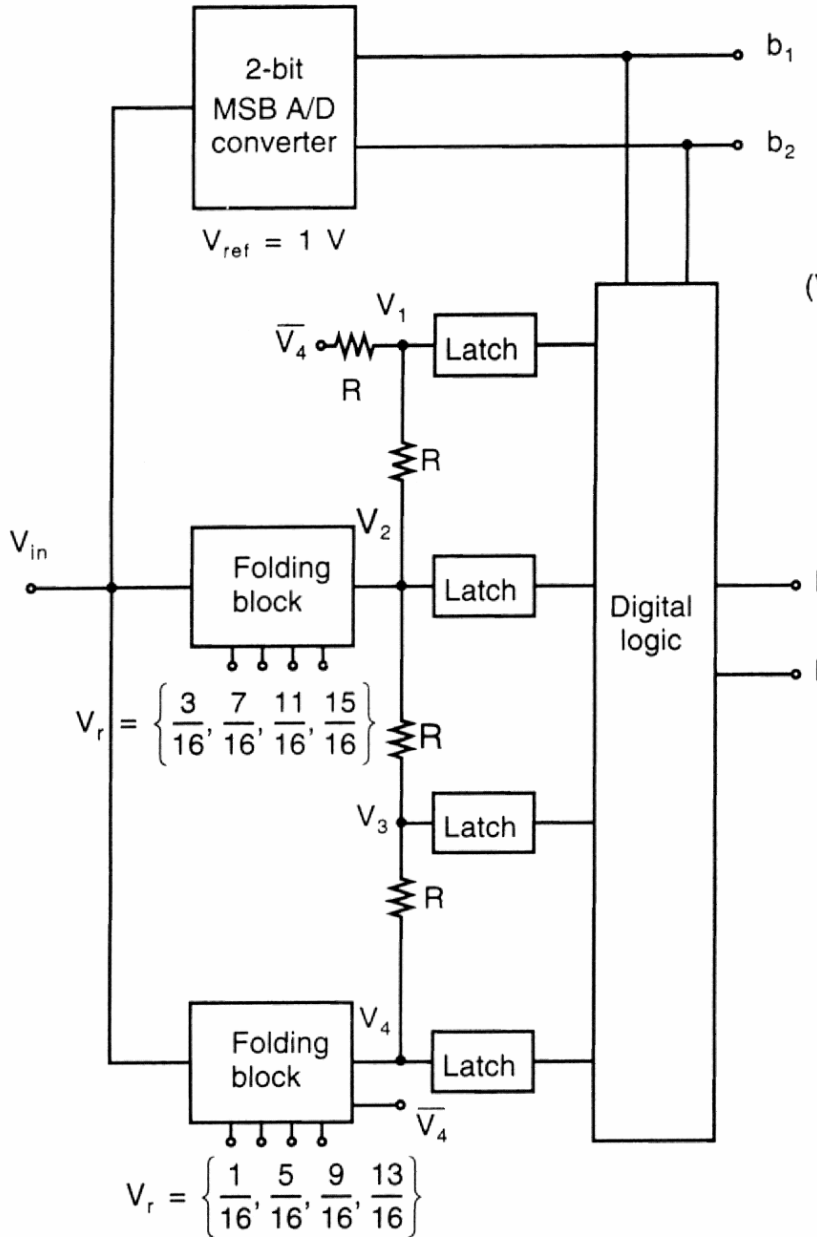
Differential pairs in parallel !

Large C_{in} !

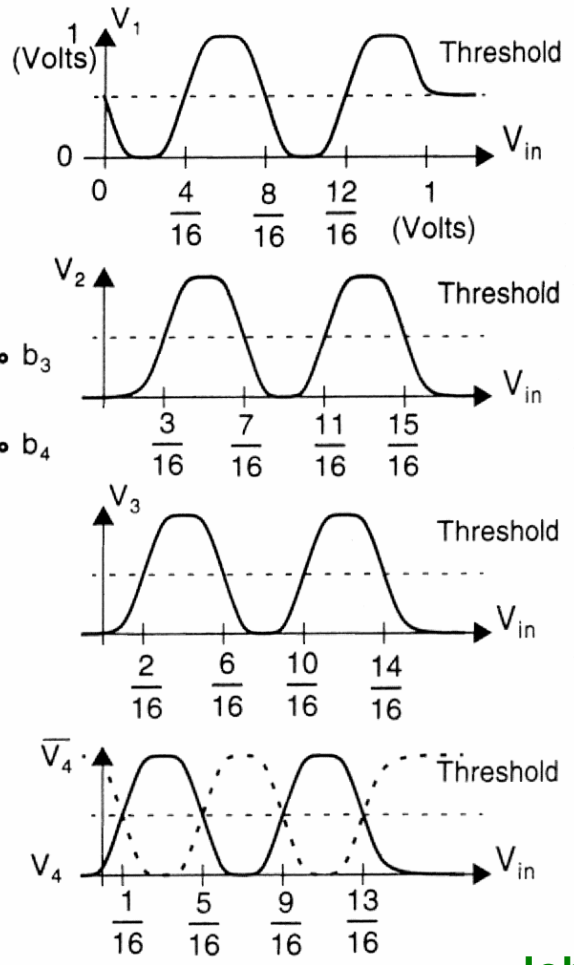
Output at higher freq. = f_{in} x folding rate

Johns, Martin, Wiley 1997

Folding + interpolation



Folding-block responses



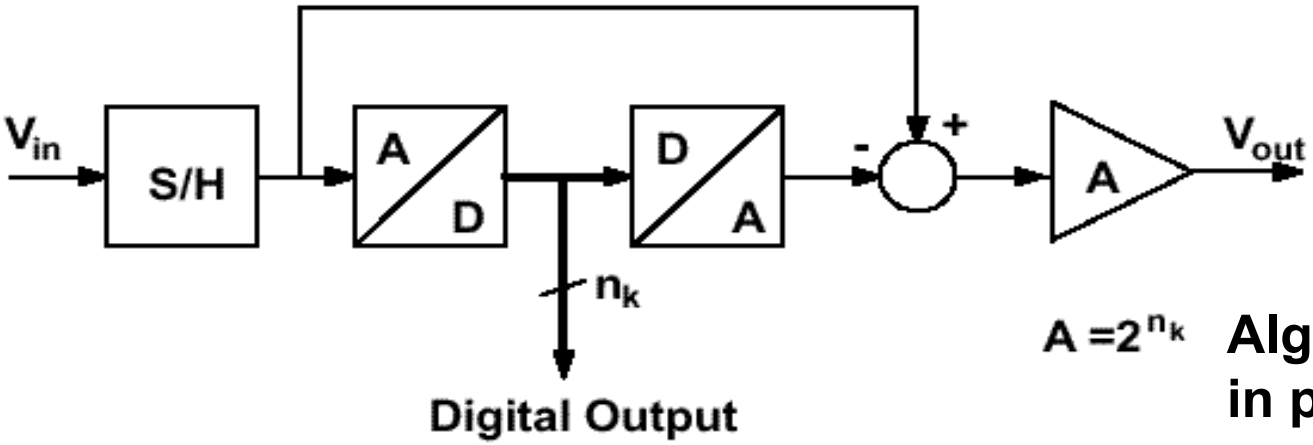
Folding rate of 4
Interpolate by 2

Lower C_{in} !

Van Valburg JSSC
Dec. 92, 1662-1666

Johns, Martin, Wiley 1997

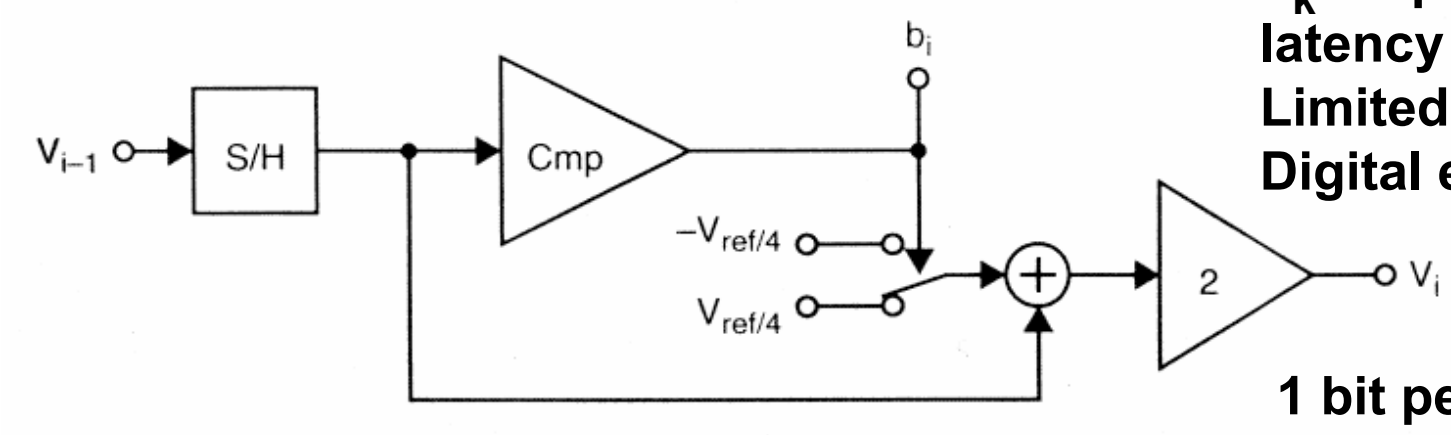
Pipelined ADC : n_k and single bit per stage



$A = 2^{n_k}$

Algorithmic conversion in pipeline !

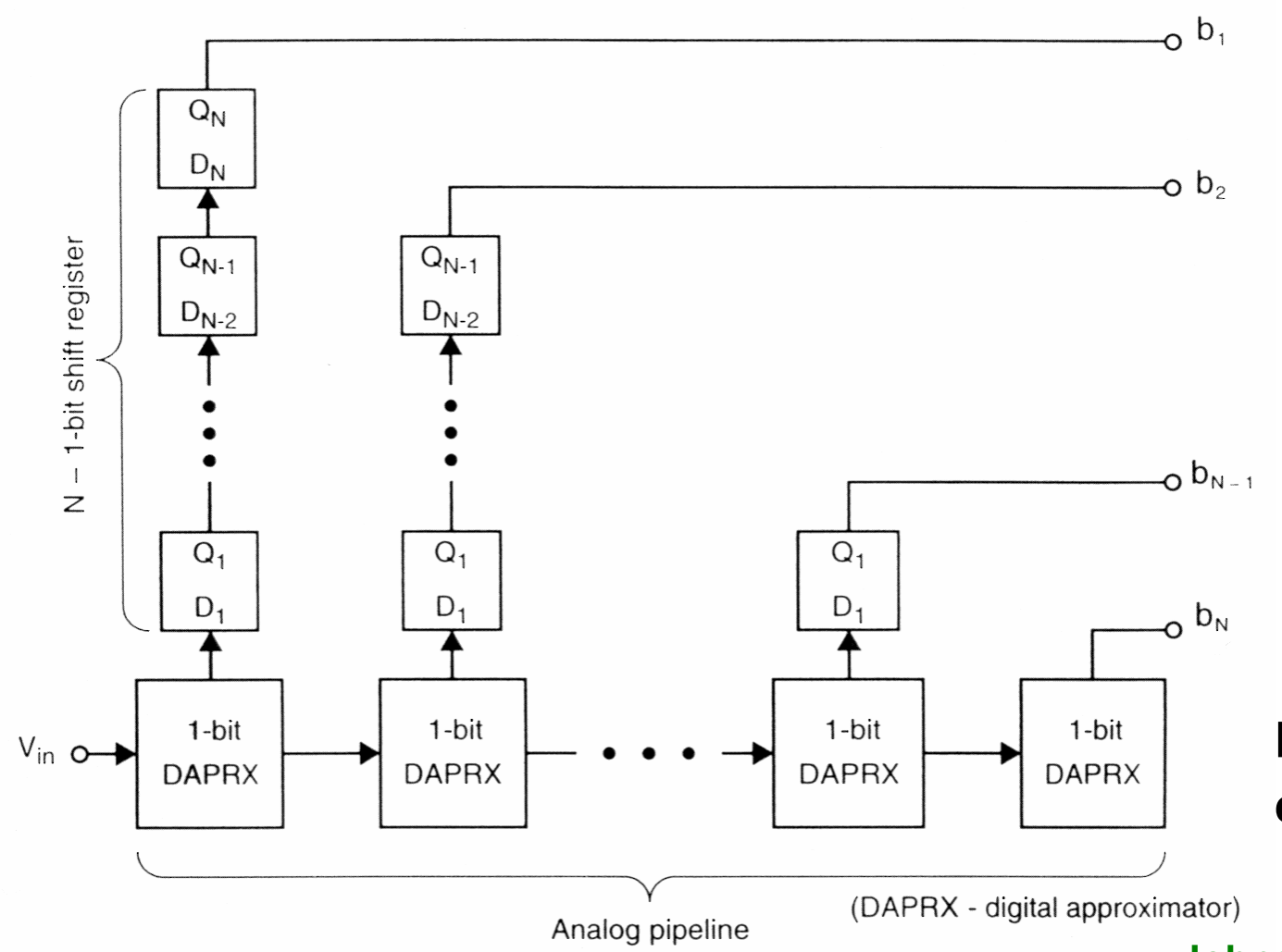
n_k bit per stage
latency of N clock periods
Limited to 12 bit by amp.
Digital error correction



1 bit per stage

Johns, Martin, Wiley 1997

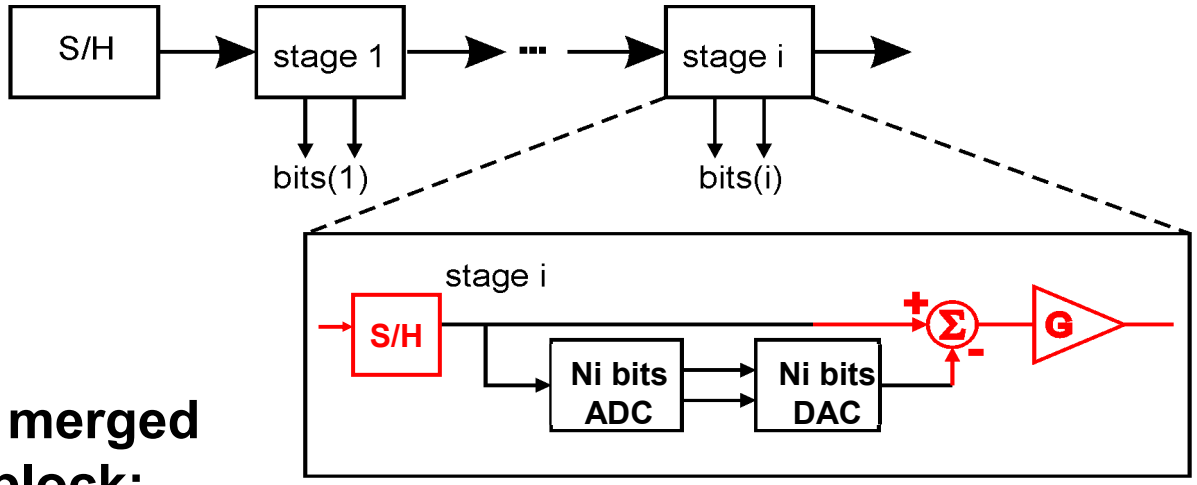
Pipelined ADC block diagram



New sample each clock cycle

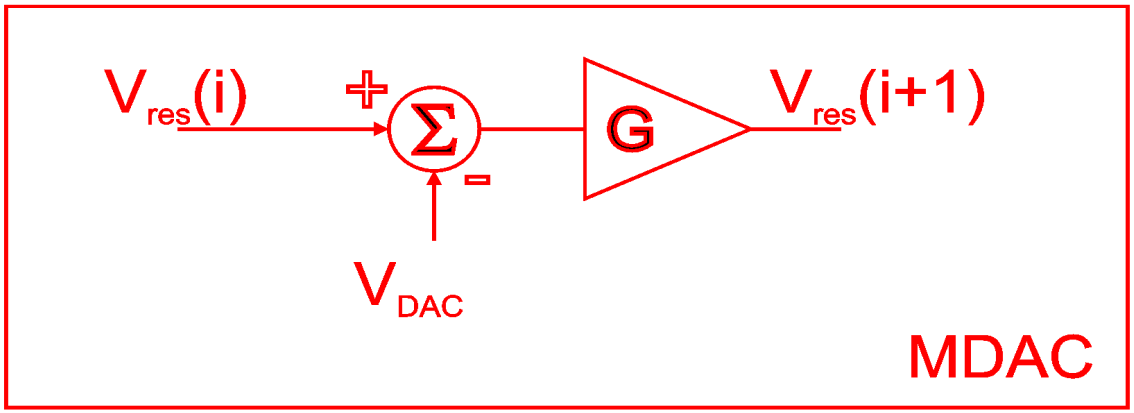
Johns, Martin, Wiley 1997

Multiplying DAC

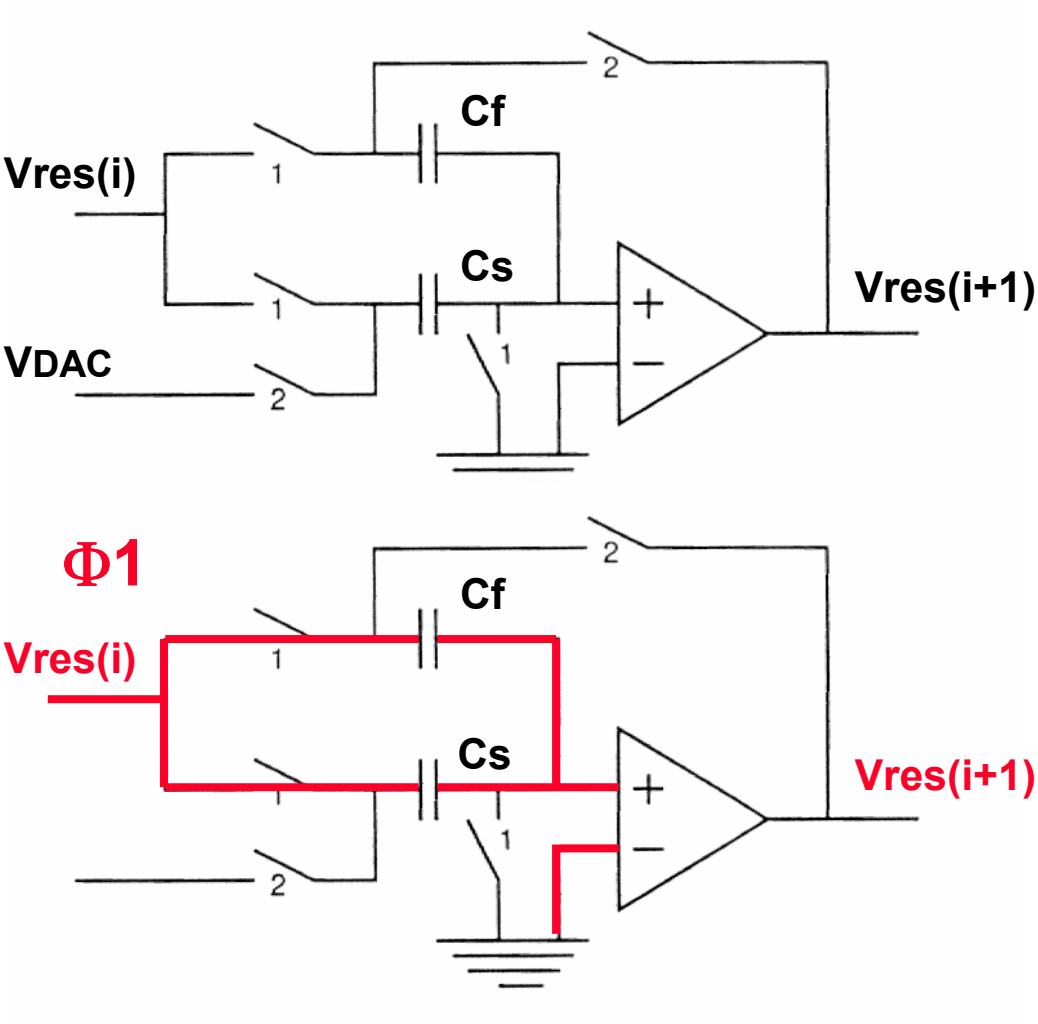


DAC + Gain Are merged In one building block:

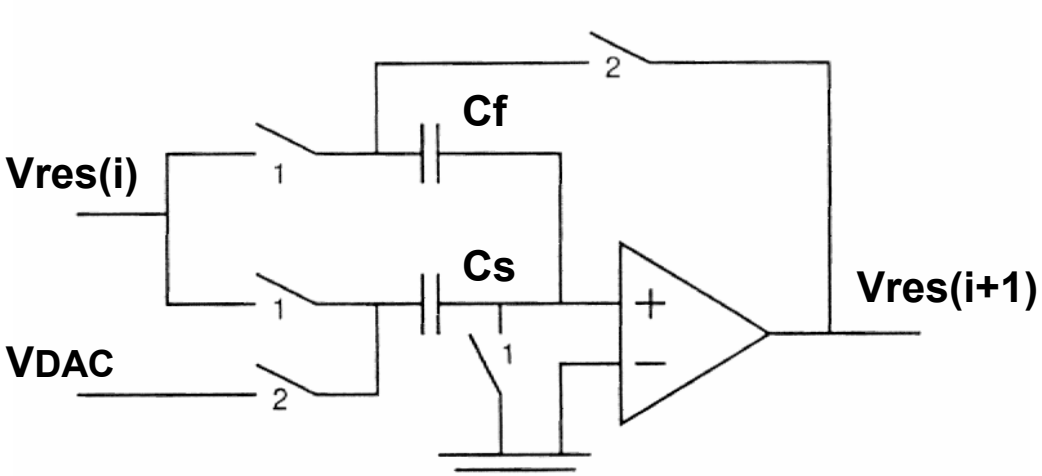
Multiplying DAC

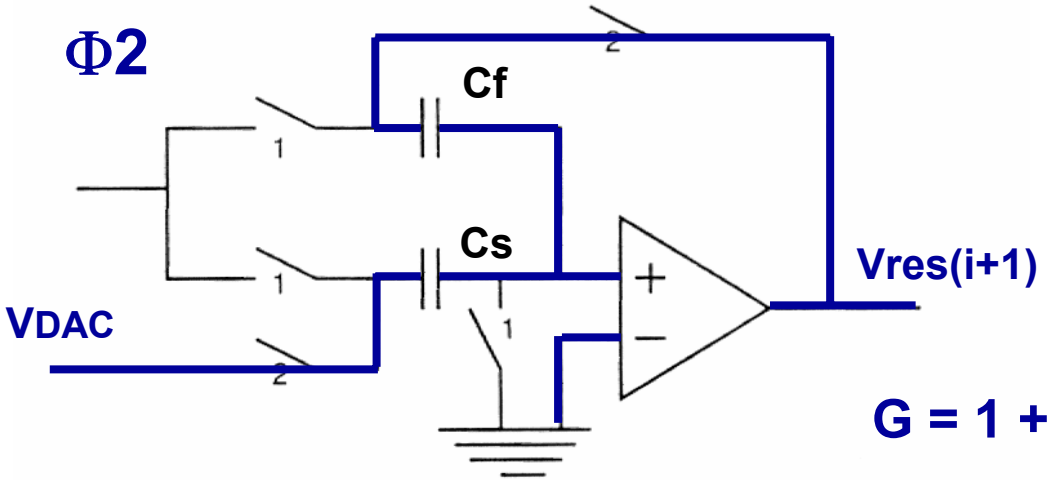


Multiplying DAC : Phase 1



Multiplying DAC : Phase 2

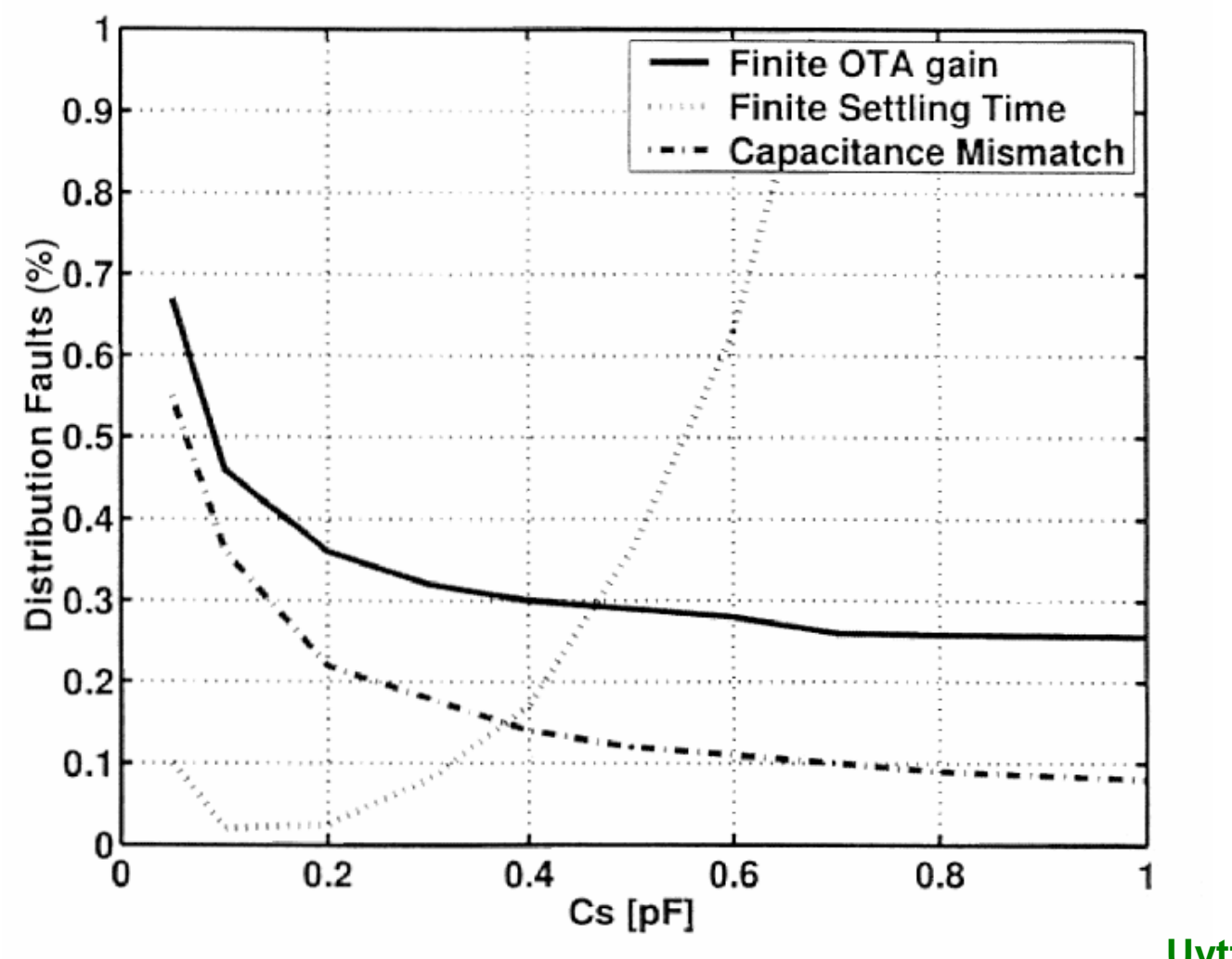




$$Vres(i+1) = Vres(i) + \frac{Cs}{Cf}(Vres(i) - VDAC)$$

$$G = 1 + \frac{Cs}{Cf} = 2 \quad \text{if} \quad Cs = Cf$$

Non-idealities versus Cs

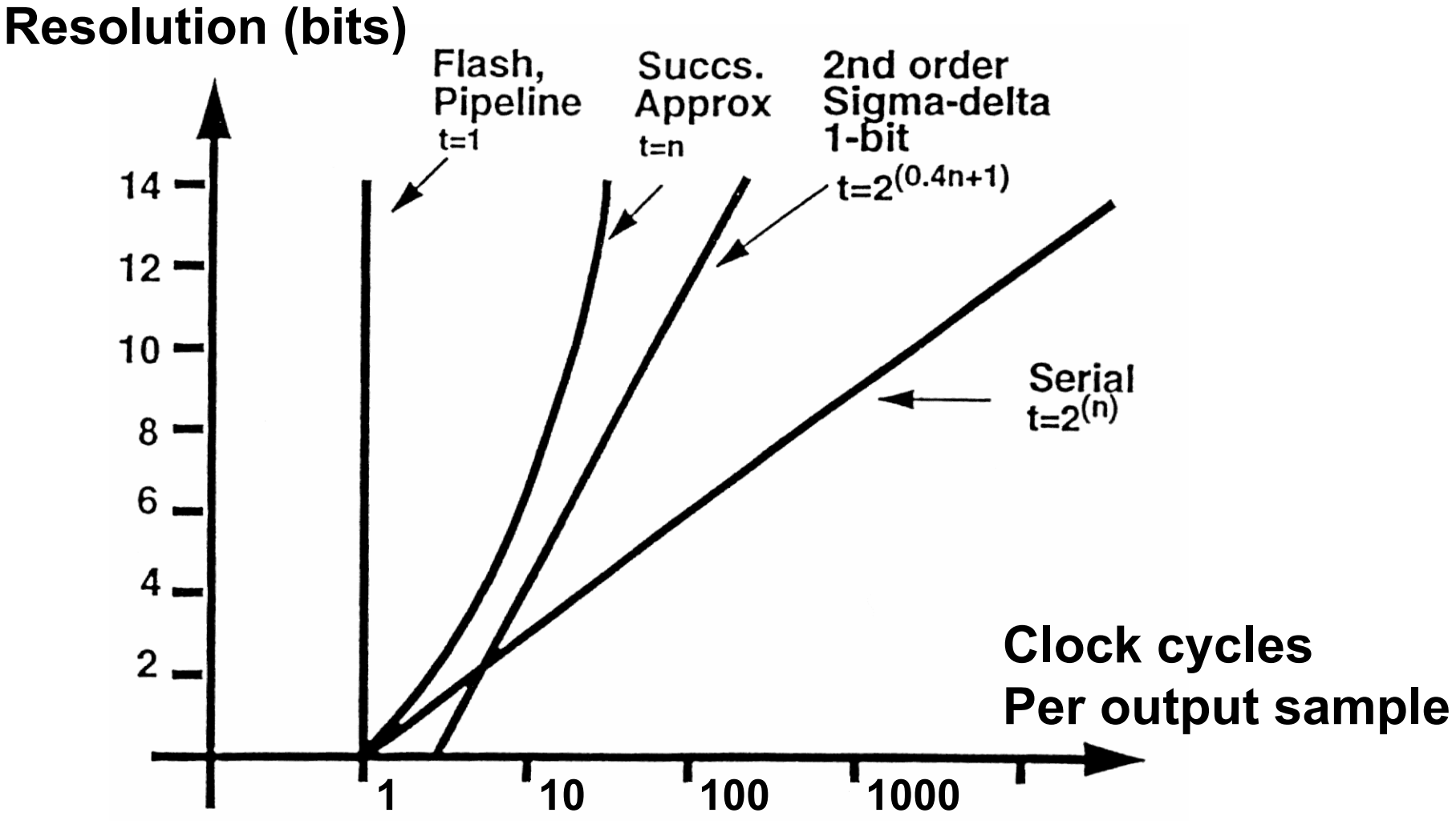


0.25 μm CMOS

f_s = 400 MHz

Uyttenhove, Kuleuven, 2003

Comparison ADCs



Impact of device mismatch on resolution/power

Two transistors : $\sigma^2(\text{Error}) \sim \frac{1}{WL}$

$$\sigma_{VT} = \frac{A_{VT}}{\sqrt{WL}}$$

$(\text{Accuracy})^2 \sim WL$

By design : increasing W increases I_{DS} and Power

decreasing L increases the speed

$$\frac{\text{Speed x (Accuracy)}}{\text{Power}} = \text{Technol. constant}$$

Ref. Kinget, ..."Analog VLSI .."
pp 67, Kluwer 1997.

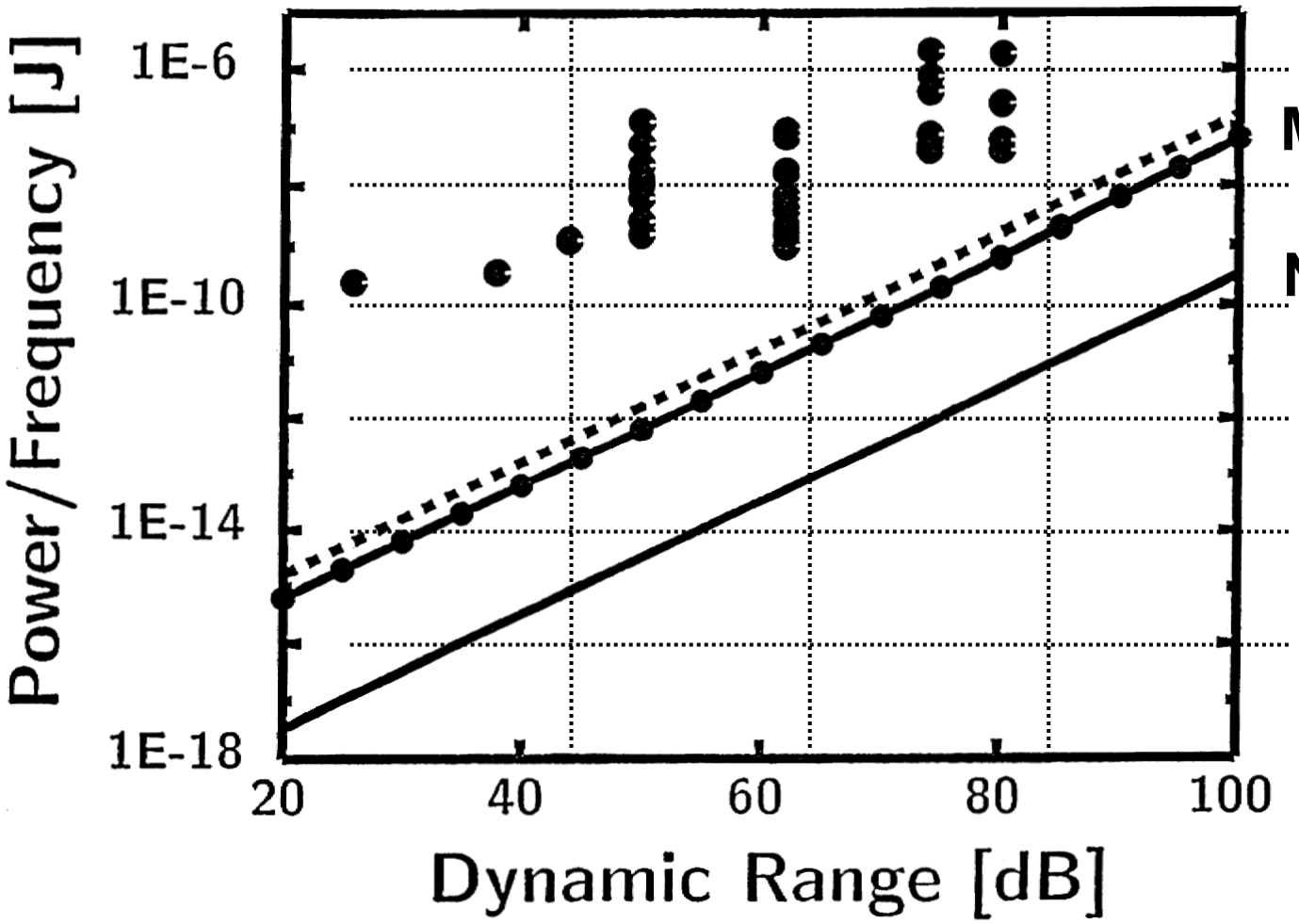
Power and mismatch/noise

Accuracy	$1/\sigma^2(V_{os}) \sim \text{Area} / A_{VT}$
Dynamic range	$DR = V_{sRMS} / (3\,\sigma\,(V_{os}))$
Capacitance	$C \sim C_{ox}\,\text{Area}$
Power	$P = 8\,f\,C\,V_{sRMS}^2$

Mismatch : $P = 24\ C_{ox}\ A_{VT}^2\ f\ DR^2$

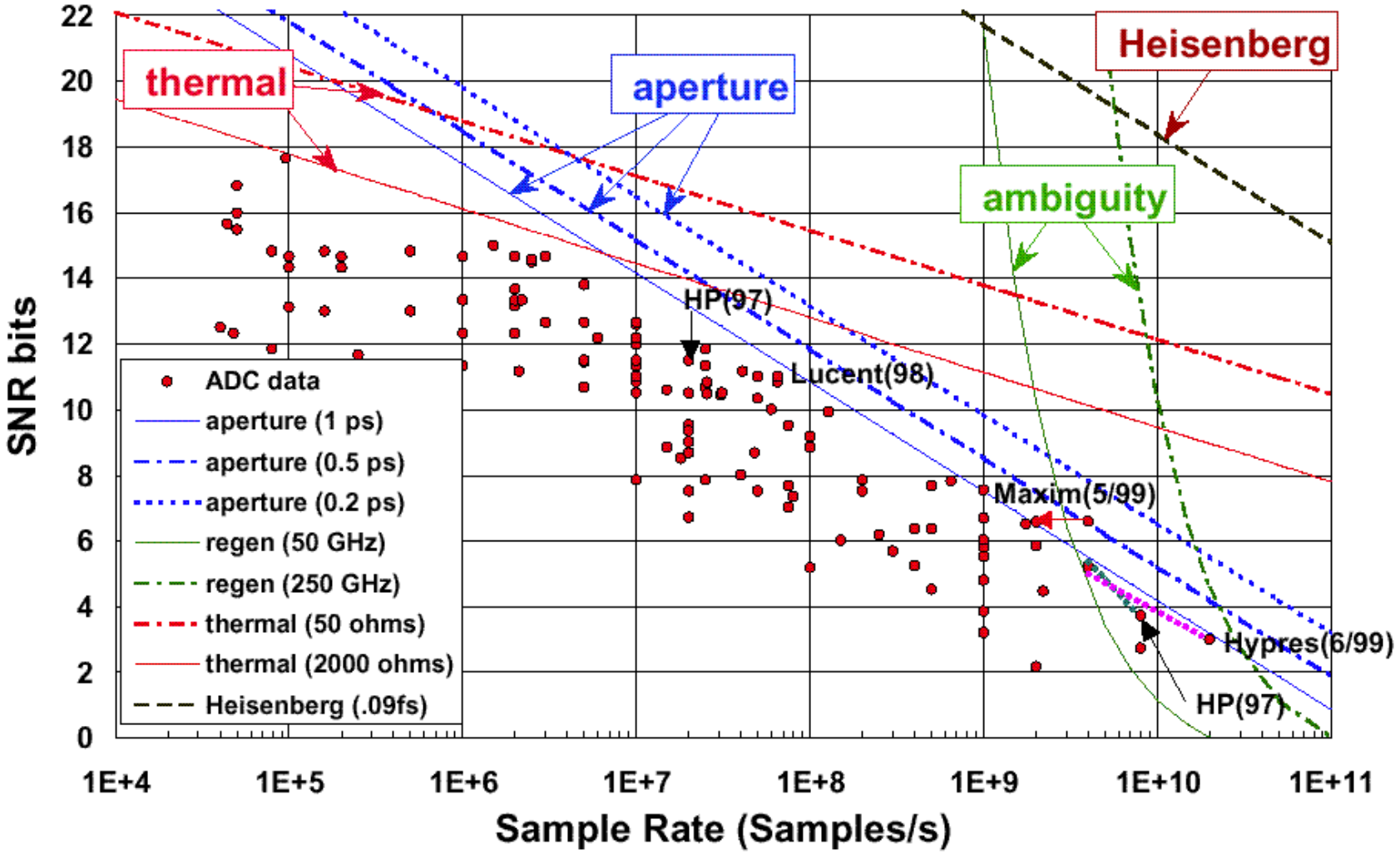
Noise : $P = 8\ kT\ f\ DR^2$

Noise vs mismatch for DR



Ref. P.Kinget, ...
"Analog VLSI .."
page 67,
Kluwer 1997.

ADC limitations



Ref Walden IEEE Selected Areas Comm. April 1999, 539-550; Uyttenhove 2003

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- P. Jespers, “Integrated Converters”, Oxford Univ. Press, 2001
- B. Razavi, “Principles of Data Conversion System Design”, IEEE Press 1995
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- R. Van de Plassche, “Integrated Analog-to-digital and Digital-to-Analog converters”, Kluwer Ac. Press, 1994

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