

北京航空航天大學  
BEIHANG UNIVERSITY

新型存储器技术

(ReRAM, PCRAM, MRAM, 赛道存储器)

2020年11月17日星期二



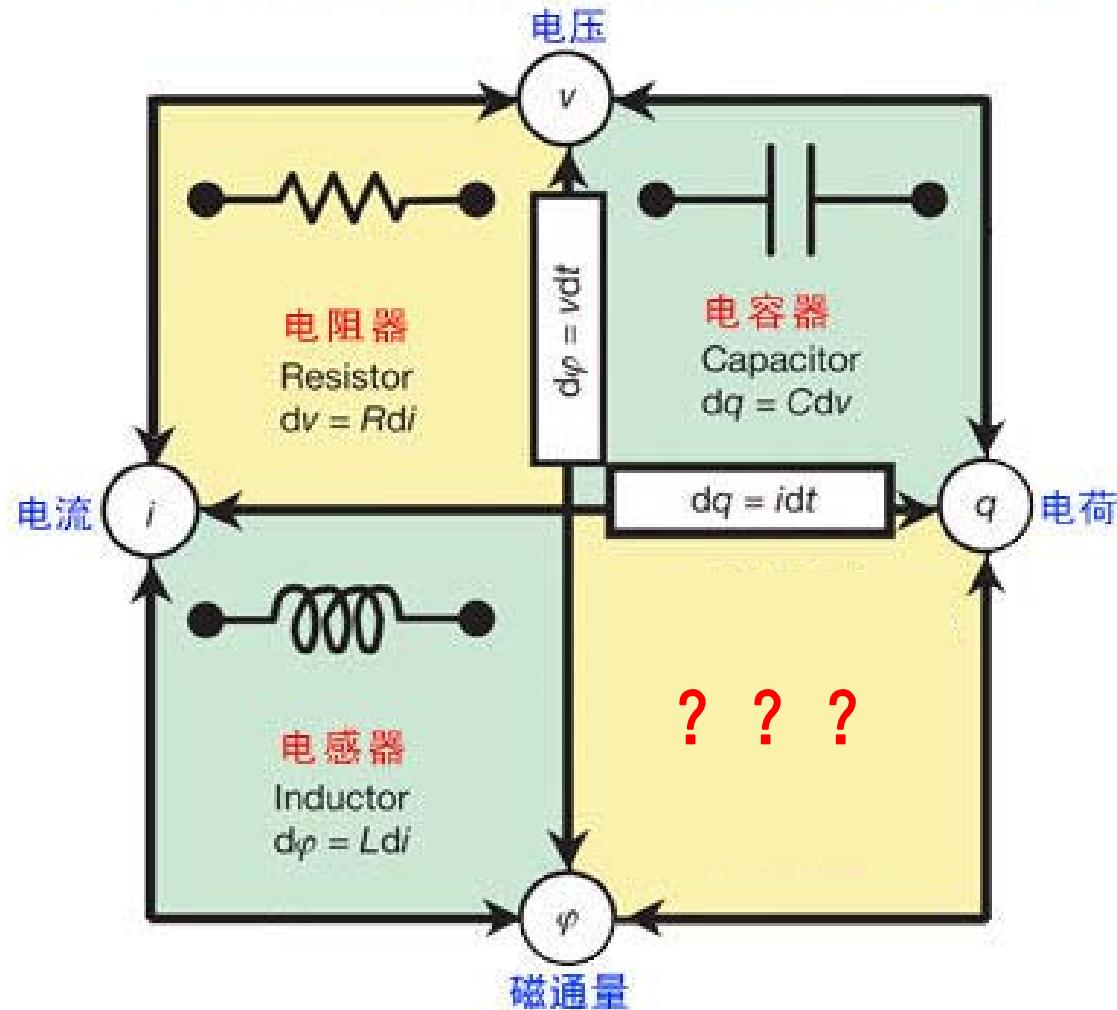
# 后摩尔时代新型存储器

- **ReRAM: Resistive RAM**  
阻变存储器（忆阻器）
- **PCRAM: Phase change RAM**  
相变存储器
- **MRAM: Magnetic RAM**  
磁存储器
- **Racetrack Memory: 赛道存储器**



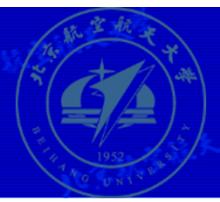
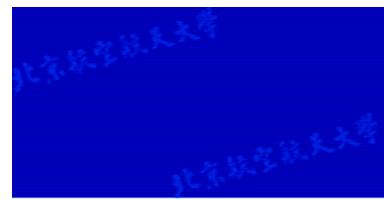
# 复习一下高中物理

## 四种基本元件之间的关系



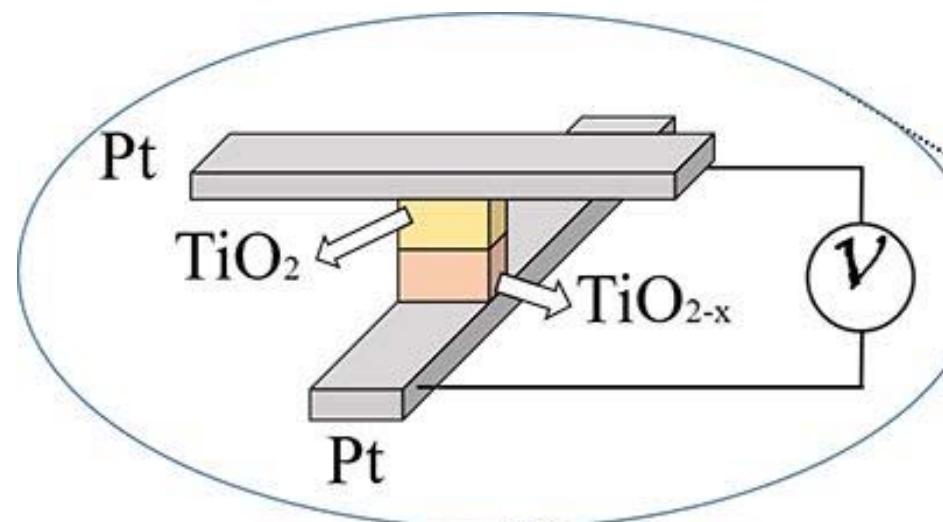
1971年，蔡少棠  
忆阻器之父

忆阻器，即记忆电阻器 (Memristor)，表示磁通与电荷关系的电路器件。

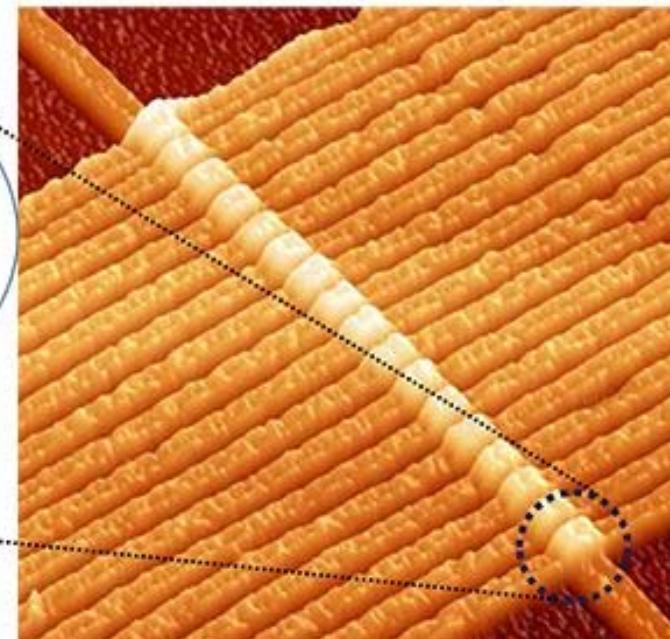


# 新型存储器技术：忆阻器

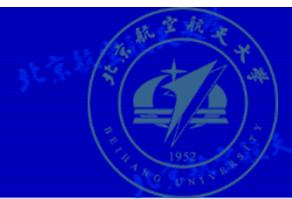
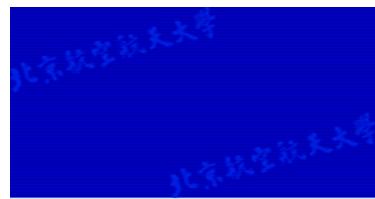
2008年，忆阻器被**惠普实验室**证实，同年，忆阻器的物理实现被美国《时代》（Time）周刊评为年度50项最佳发明者之一，入选美国《连线》（Wired）年度十大科技突破。  
未来在存储器与处理器（类脑计算）芯片中具有巨大应用前景



金属氧化物



From baidu



# 新型存储器技术：忆阻器

## The Periodic Table of the Elements

corresponding binary oxide that exhibits bistable resistance switching

**metal that is used for electrode**

<b>H</b>	<b>exhibits bistable resistance switching</b>												<b>H</b>	<b>He</b>	
<b>Li</b>	<b>Be</b>												<b>B</b>	<b>C</b>	
<b>Na</b>	<b>Mg</b>												<b>Al</b>	<b>Si</b>	
<b>K</b>	<b>Ca</b>	<b>Sc</b>	<b>Ti</b>	<b>V</b>	<b>Cr</b>	<b>Mn</b>	<b>Fe</b>	<b>Co</b>	<b>Ni</b>	<b>Cu</b>	<b>Zn</b>	<b>Ga</b>	<b>Ge</b>	<b>As</b>	<b>Se</b>
<b>Rb</b>	<b>Sr</b>	<b>Y</b>	<b>Zr</b>	<b>Nb</b>	<b>Mo</b>	<b>Tc</b>	<b>Ru</b>	<b>Rh</b>	<b>Pd</b>	<b>Ag</b>	<b>Cd</b>	<b>In</b>	<b>Sn</b>	<b>Sb</b>	<b>Te</b>
<b>Cs</b>	<b>Ba</b>	<b>La</b>	<b>Hf</b>	<b>Ta</b>	<b>W</b>	<b>Re</b>	<b>Os</b>	<b>Ir</b>	<b>Pt</b>	<b>Au</b>	<b>Hg</b>	<b>Tl</b>	<b>Pb</b>	<b>Bi</b>	<b>Po</b>
<b>Fr</b>	<b>Ra</b>	<b>Ac</b>	<b>Rf</b>	<b>Db</b>	<b>Sg</b>	<b>Bh</b>	<b>Hs</b>	<b>Mt</b>							

58	59	60	61	62	63	64	65	66	67	68	69	70	71
Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
90	91	92	93	94	95	96	97	98	99	100	101	102	103
Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

From baidu

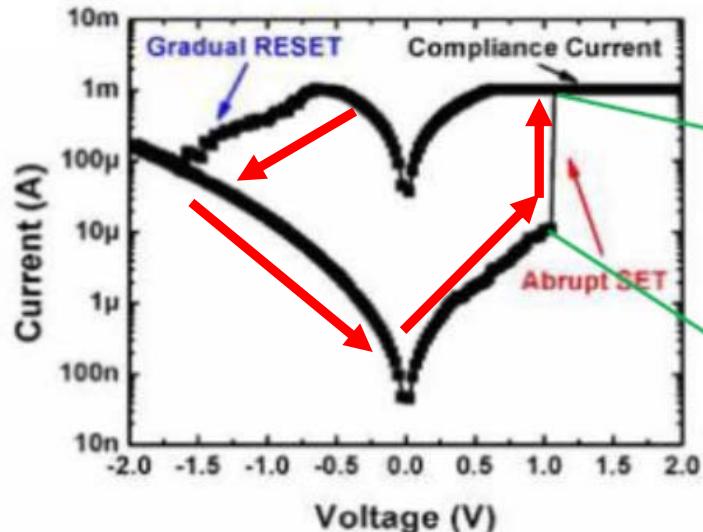


# 新型存储器技术：忆阻器

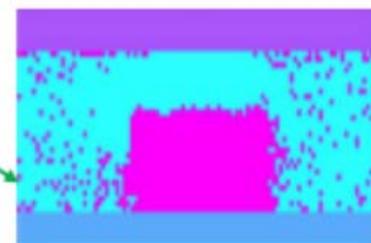
顶电极



氧化物  
HfO<sub>x</sub>, TiO等



Filament connect

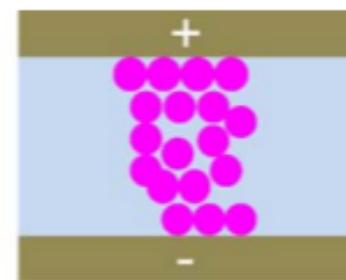
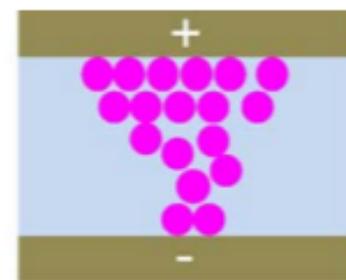
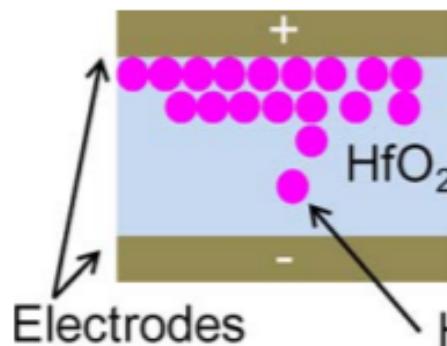


Filament rupture

底电极

高阻态

低阻态

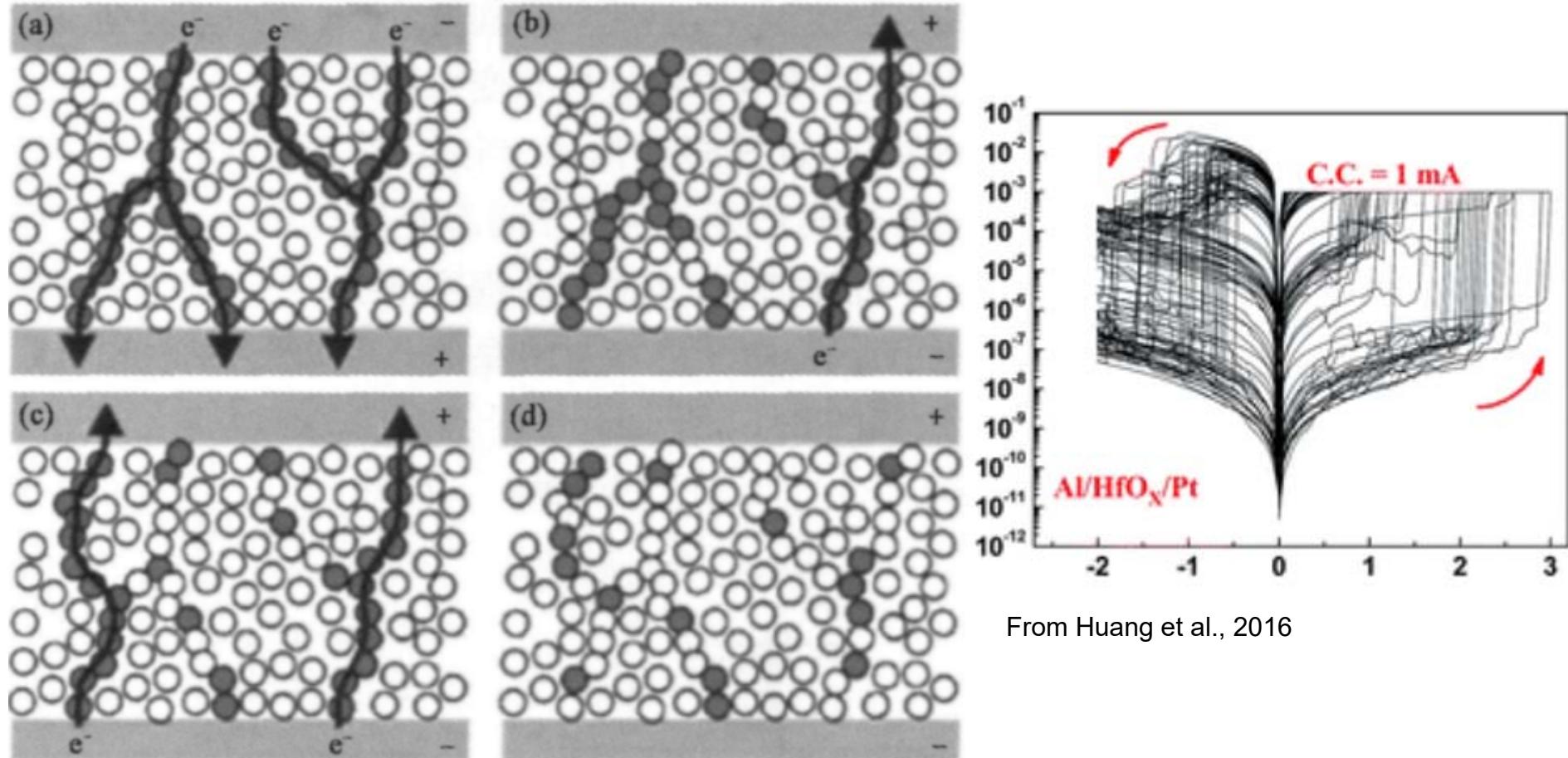


Hf or V<sub>O</sub>

From Huang et al., 2018



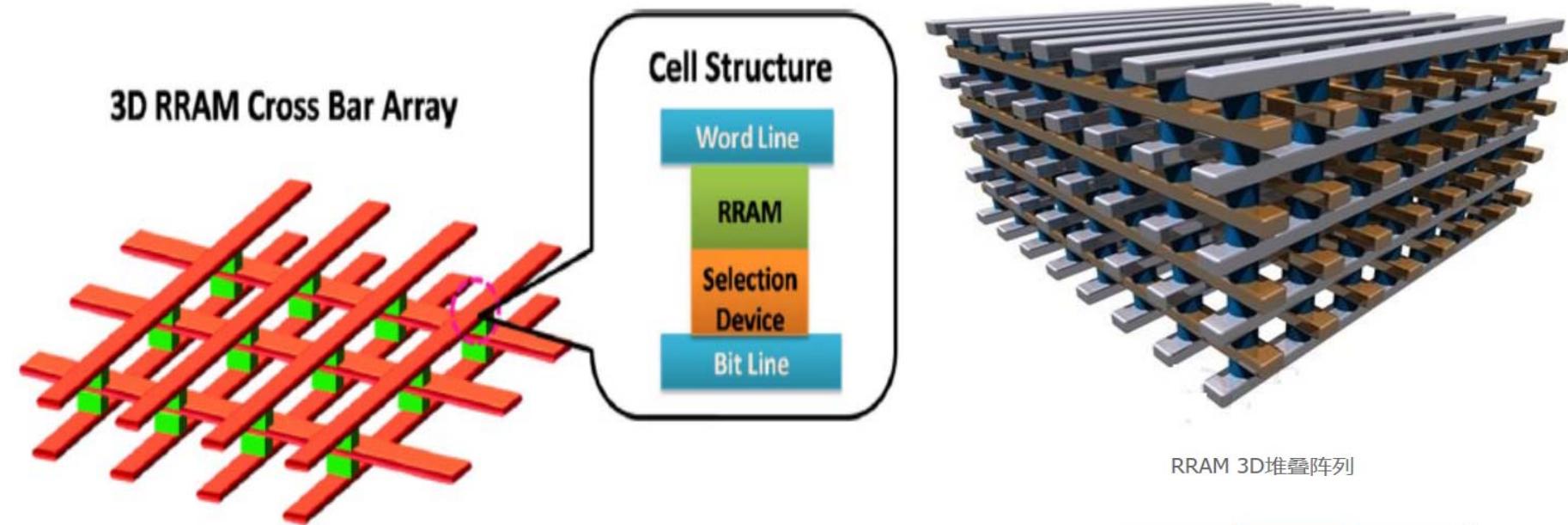
# 新型存储器技术：忆阻器



From Huang et al., 2016

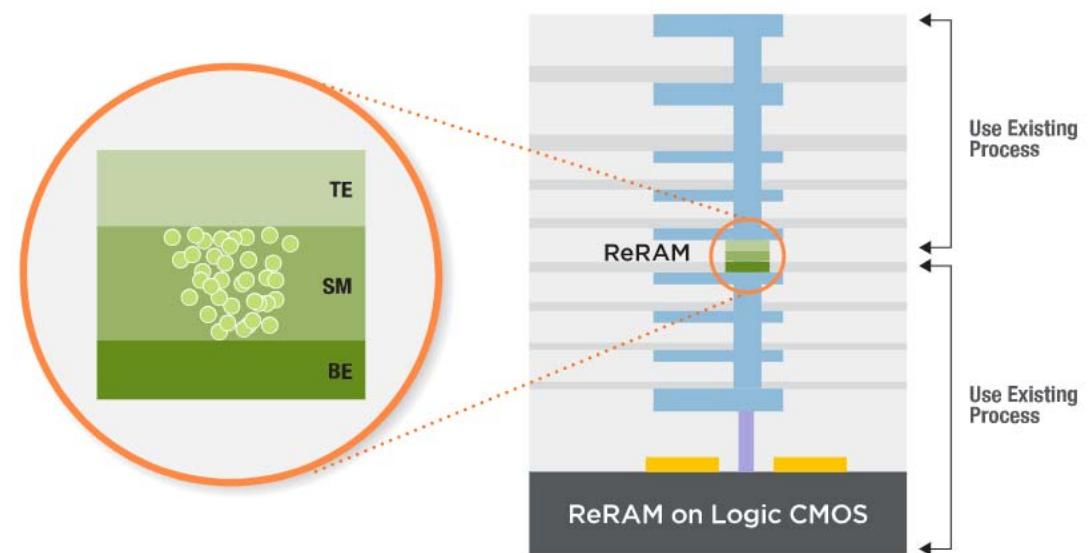
产业化问题：导电丝形成的位置、粗细、数量都不尽相同，不同单元之间，甚至同一个单元不同时刻的翻转行为特征都不一样

# 忆阻器应用：大容量、高速度、低功耗存储

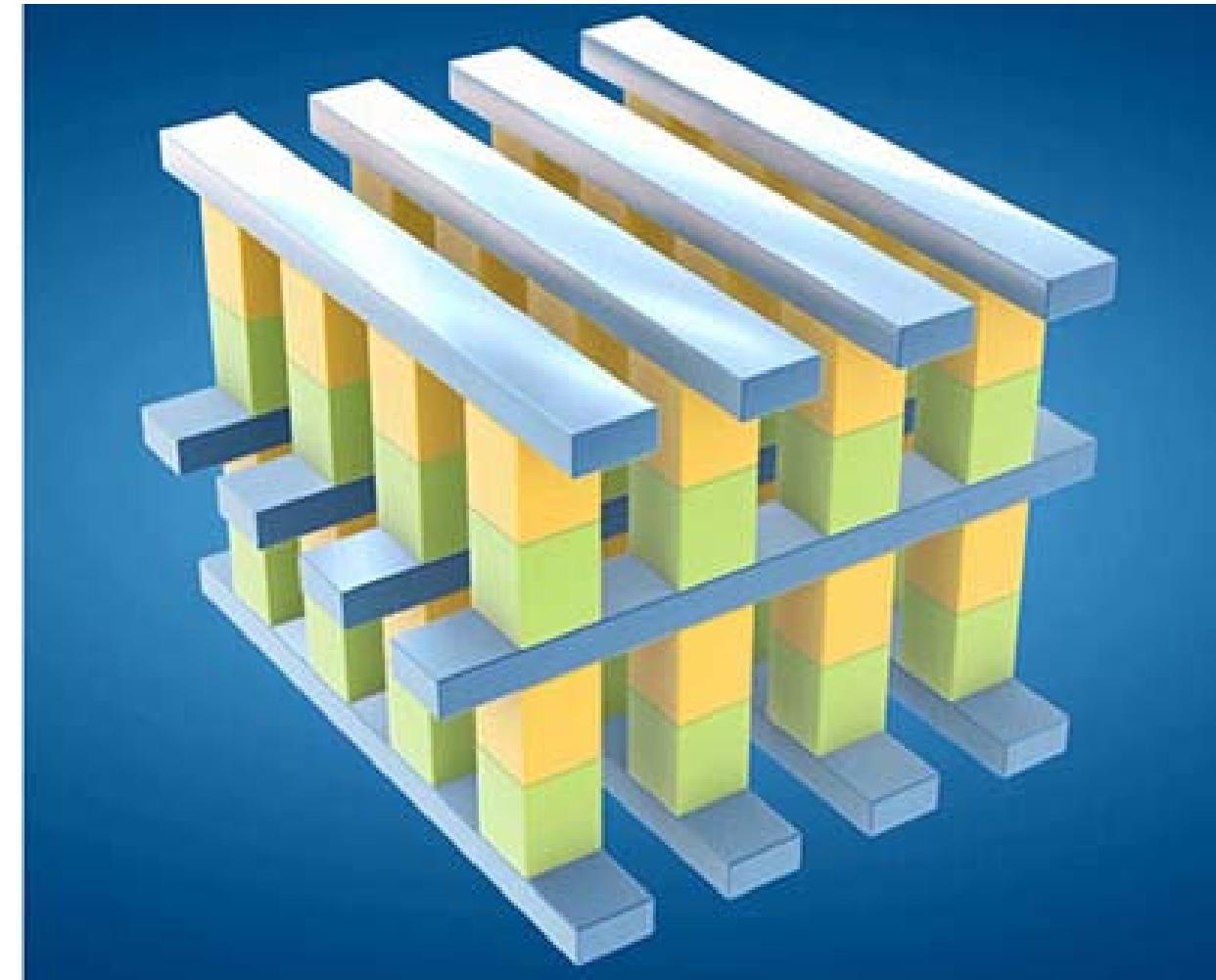


跟NAND Flash相比，

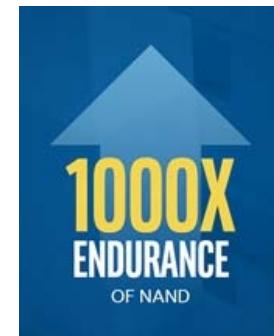
- 高2倍的存储密度
- 低100倍的读延迟
- 快1000倍写性能



# 忆阻器应用：大容量、高速度、低功耗存储



3D XPoint™ Technology



# 忆阻器应用：大容量、高速度、低功耗存储



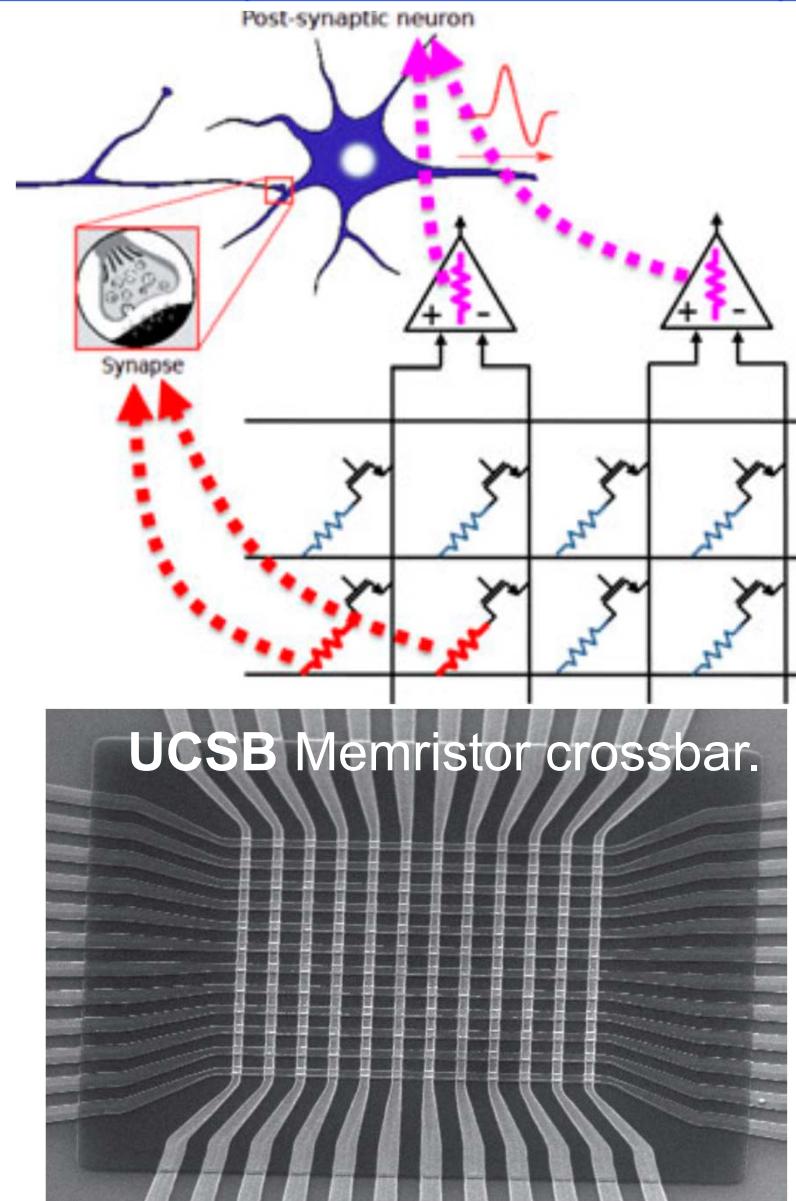
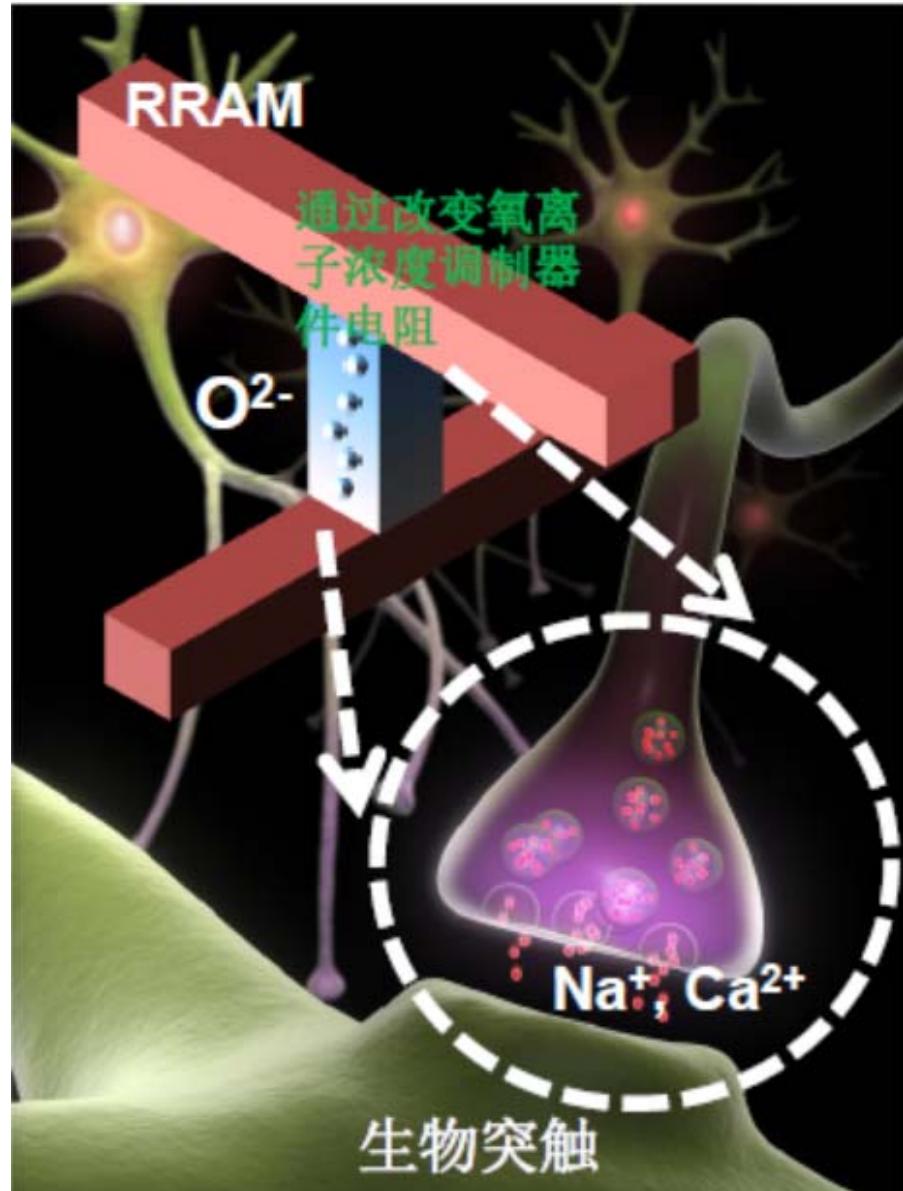
替换NAND  
用于SSD



替换DRAM  
用于内存

非易失性

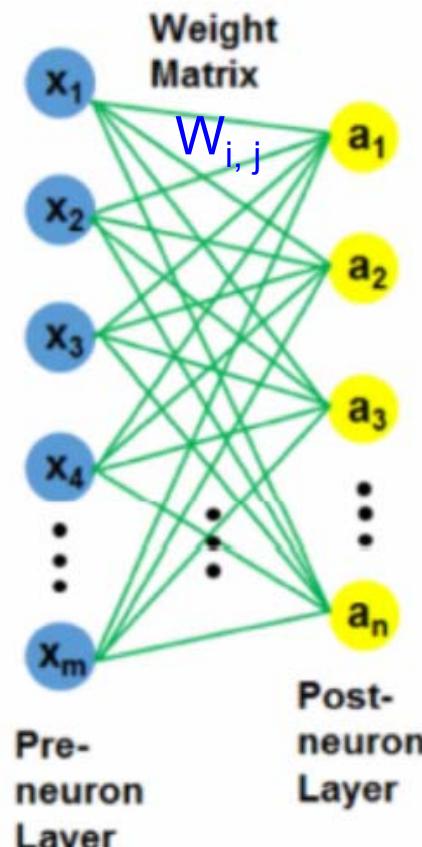
# 新应用：类脑计算/深度学习



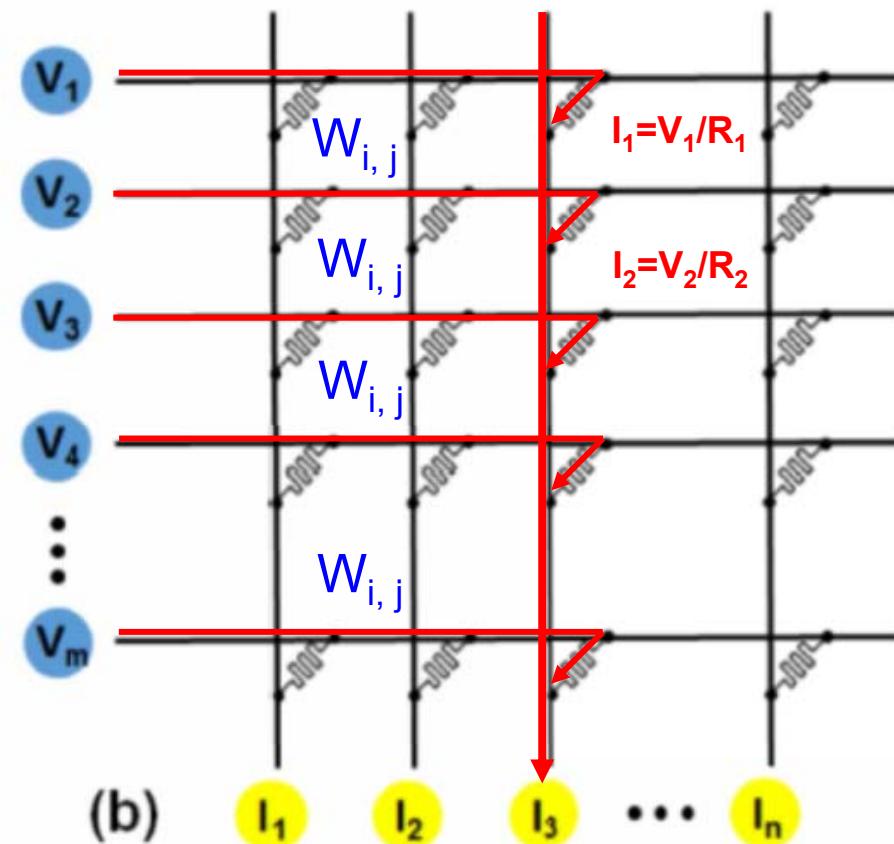
# 新应用：类脑计算/深度学习

$$a_i = \sum_1^m x_j w_{i,j}$$

欧姆定律+基尔霍夫定律



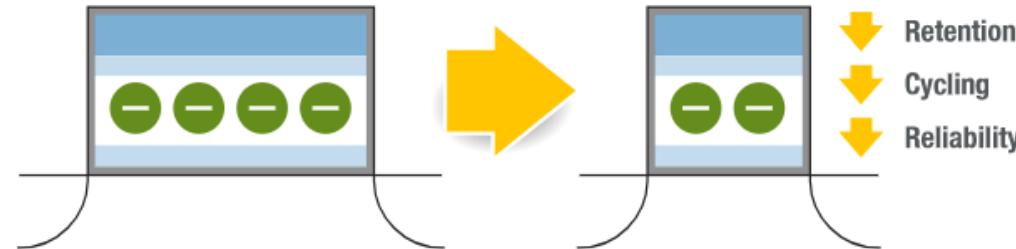
Conductance of crossbar array  
represents weight matrix



# 尺寸微缩：忆阻器 VS Flash

## How flash technology scales:

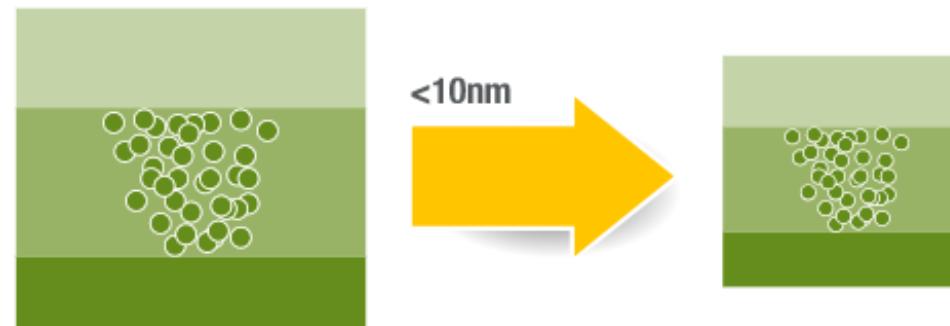
scaling > less electrons > performance degrade



>28nm

## How Crossbar ReRAM scales:

scaling > same nanofilament > better performance



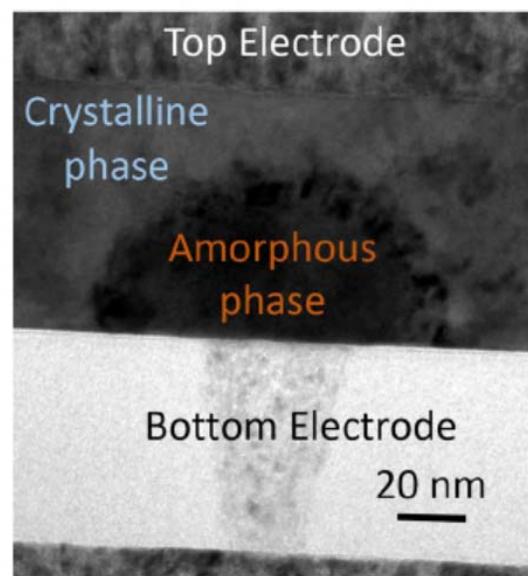
<10nm

# 新型存储器技术：相变存储器

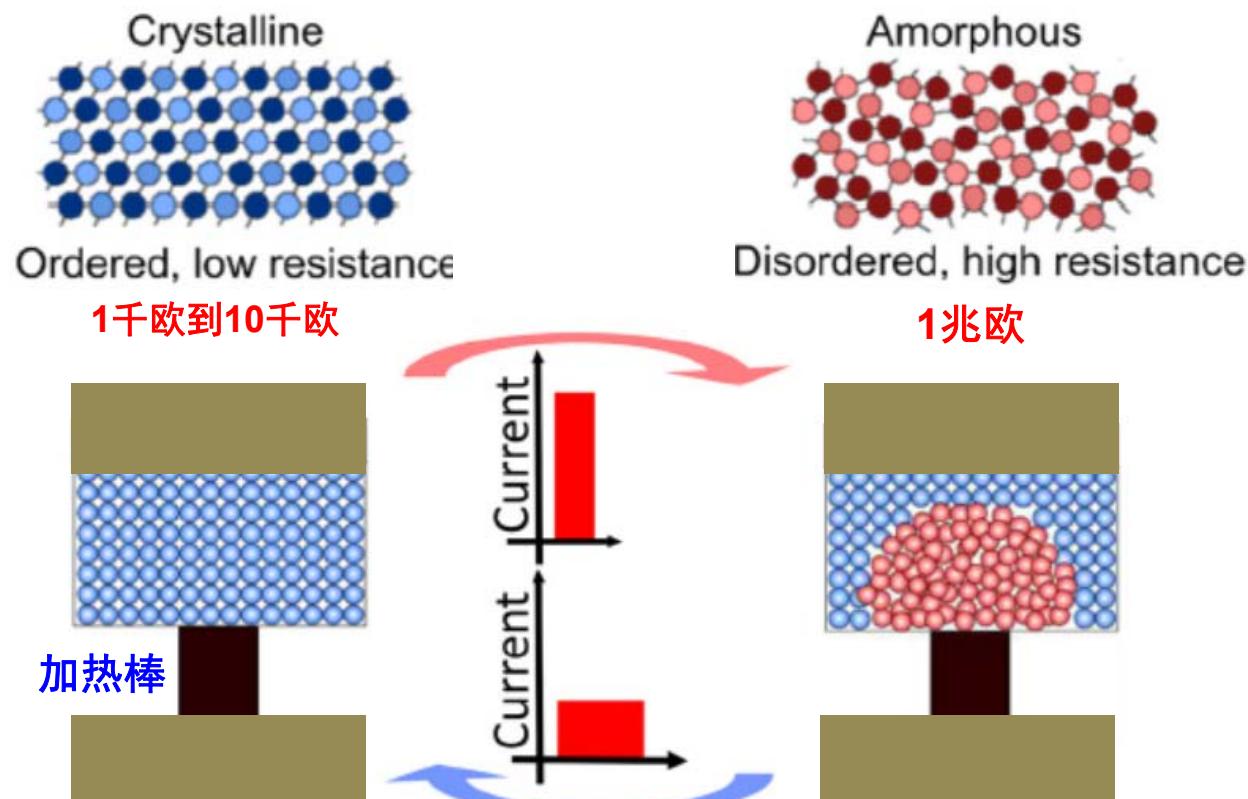
顶电极



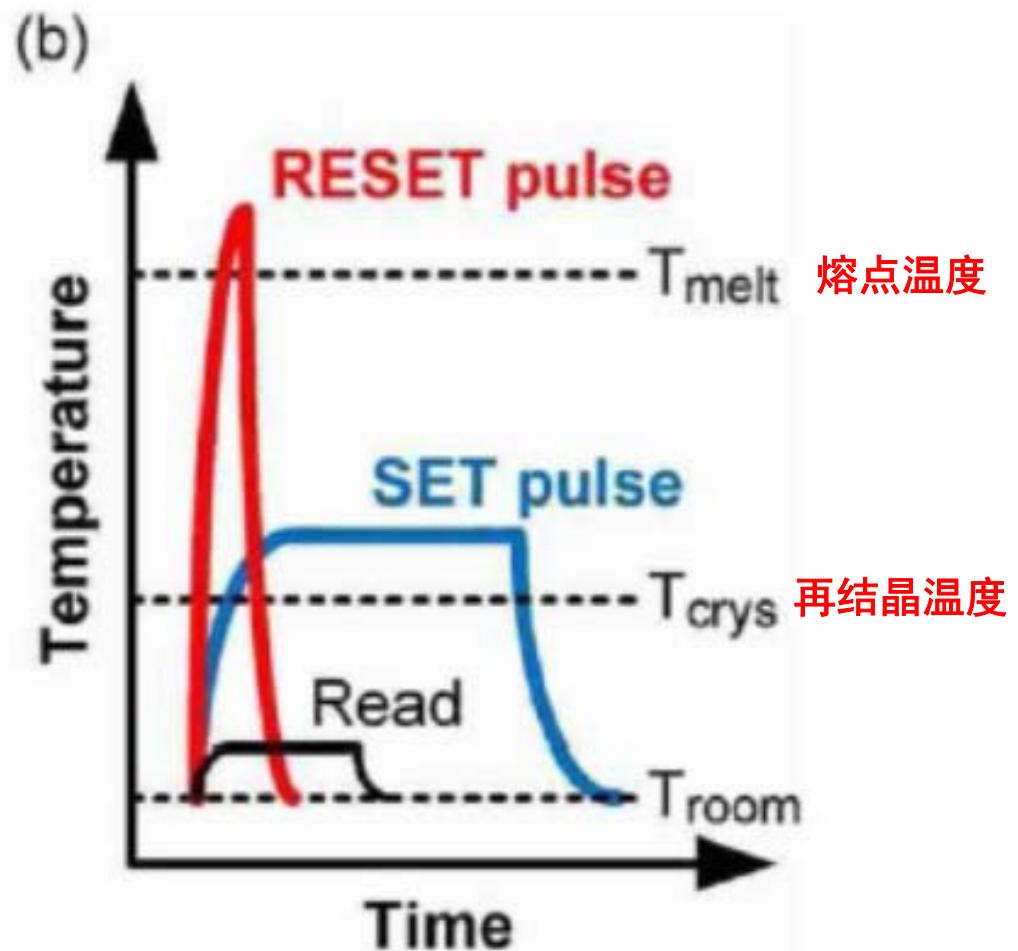
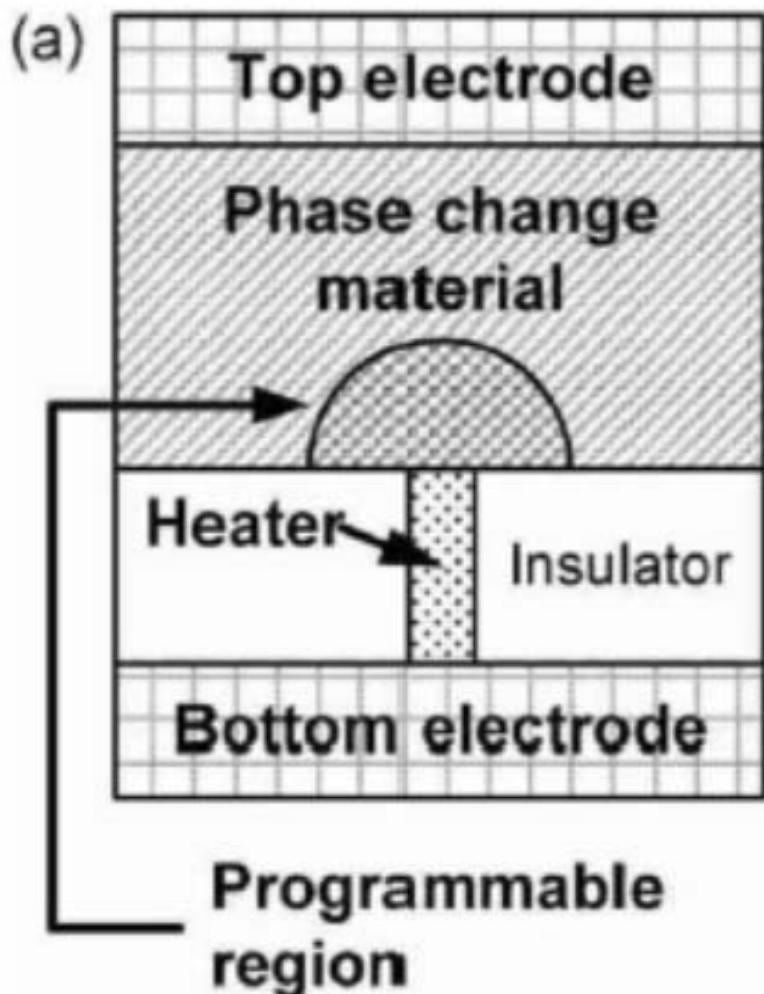
底电极



利用硫族化合物在晶态（低电阻态）和非晶态（高电阻态）巨大的导电性差异来存储数据，两种状态之间的转变通常通过加热来实现



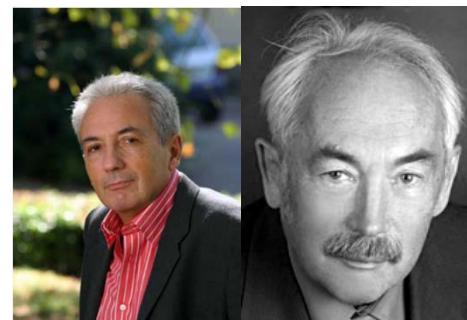
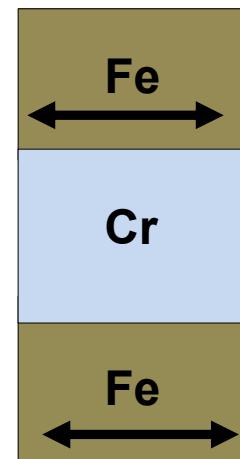
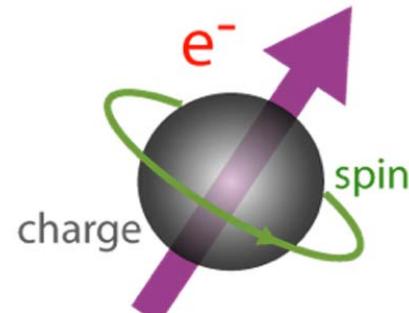
# 新型存储器技术：相变存储器



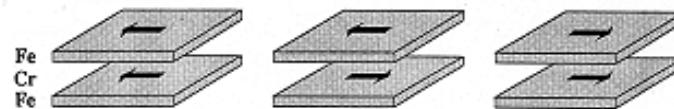
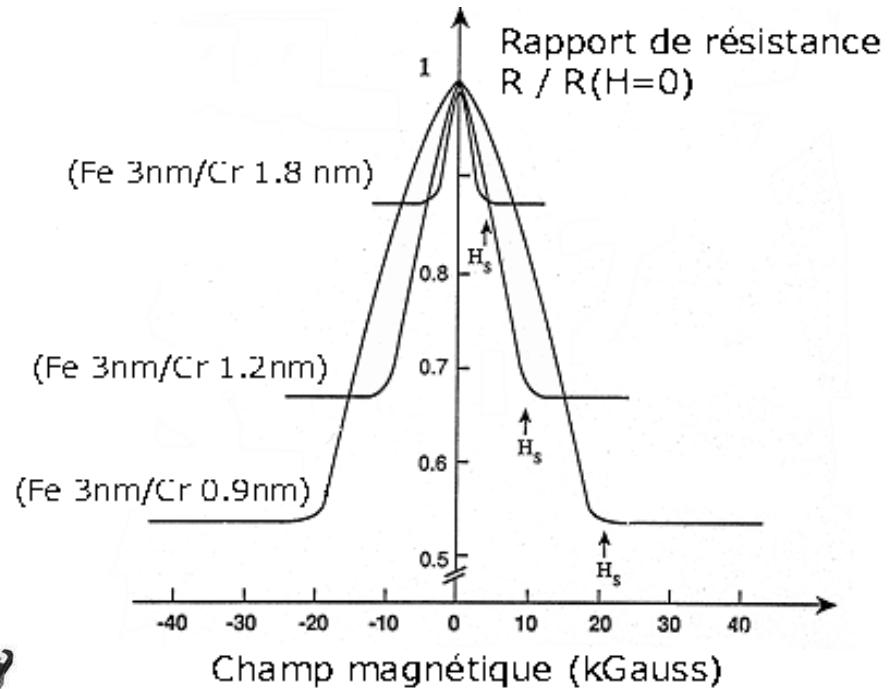


# 新型存储器技术：自旋电子

**自旋电子学：**电子的**自旋、电荷、质量属性**，现在大部分半导体都是用电子的电荷属性来存储或者处理信息，今后的电子器件将使用电子的自旋属性！

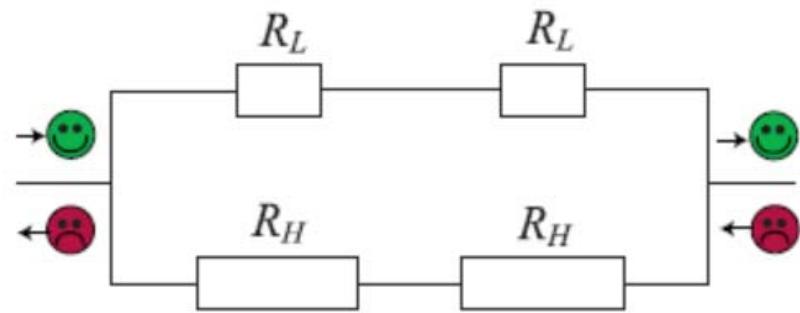
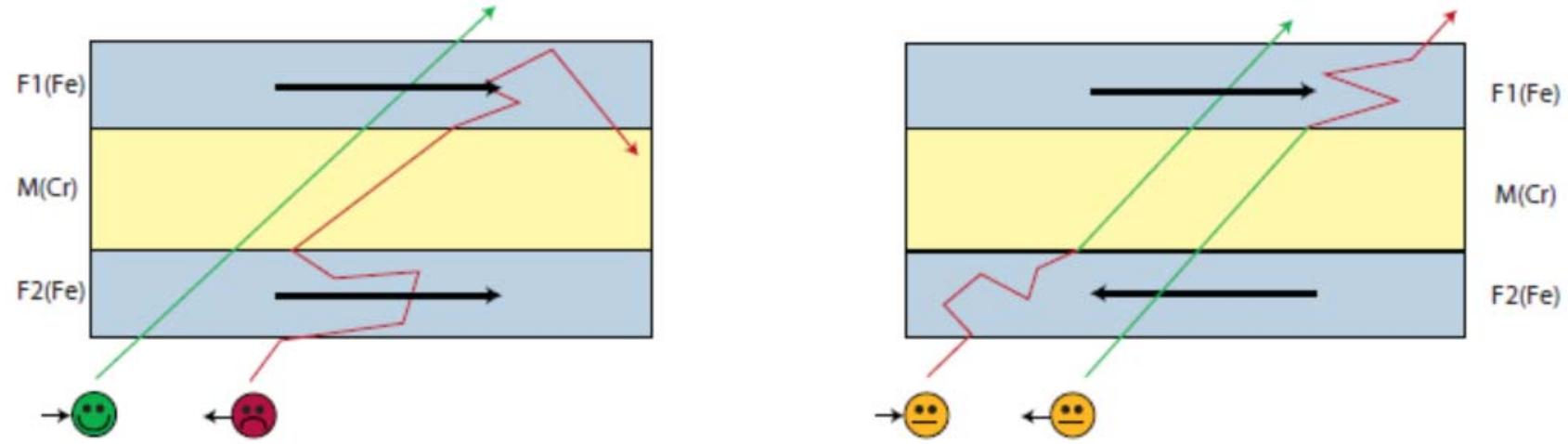


2007年诺贝尔物理学奖

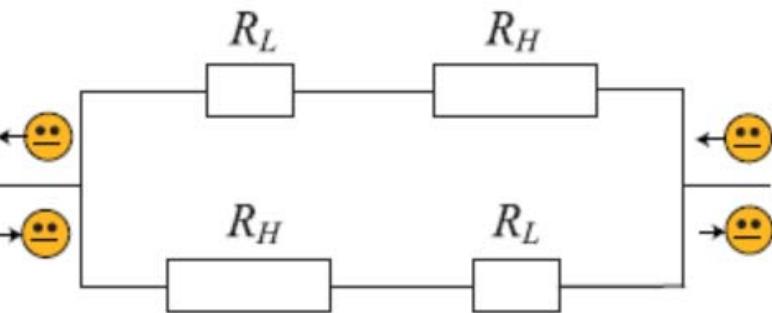


1988年，费尔团队发现巨磁阻效应

# 新型存储器技术：MRAM



(a)



(b)

## 巨磁阻效应：双通道模型

在GMR实验中，为什么GMR只有在Cr厚度降低到一定尺寸才行？

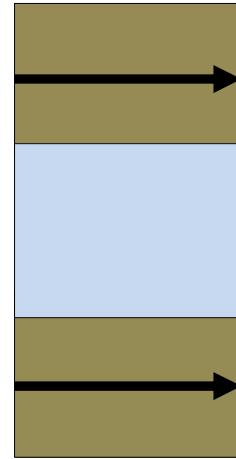


# 新型存储器技术：MRAM

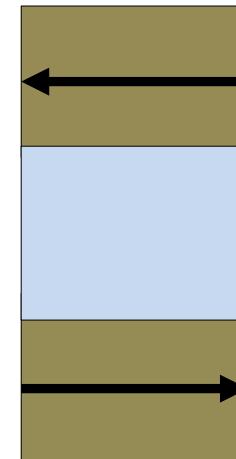
铁磁材料  
(CoFeB)



低阻态



高阻态



磁场  
电流  
电压  
光等

磁隧道结

隧穿磁阻

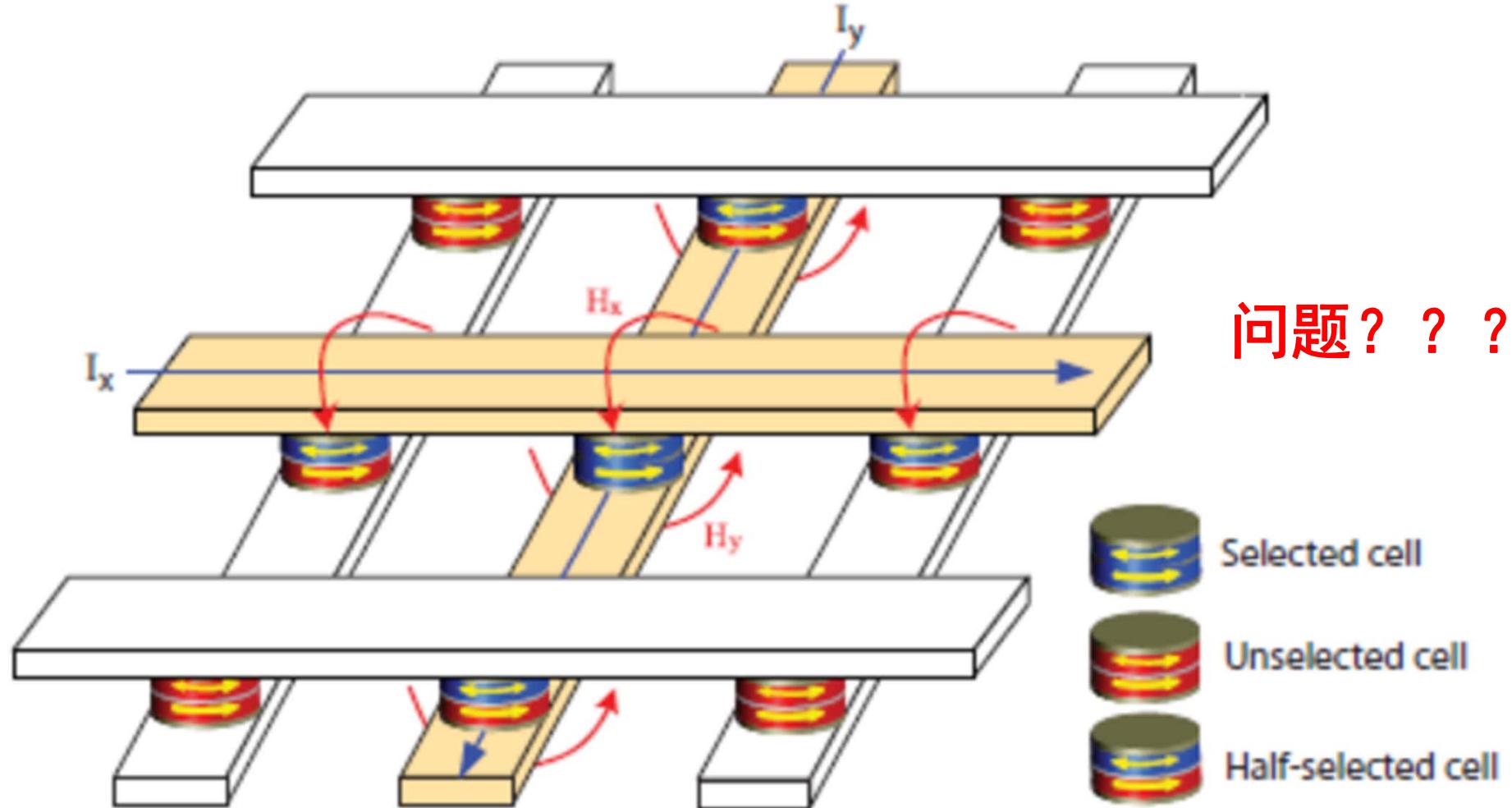
面内磁化

垂直磁化

$$\frac{R_{AP} - R_P}{R_P} \times 100\%$$

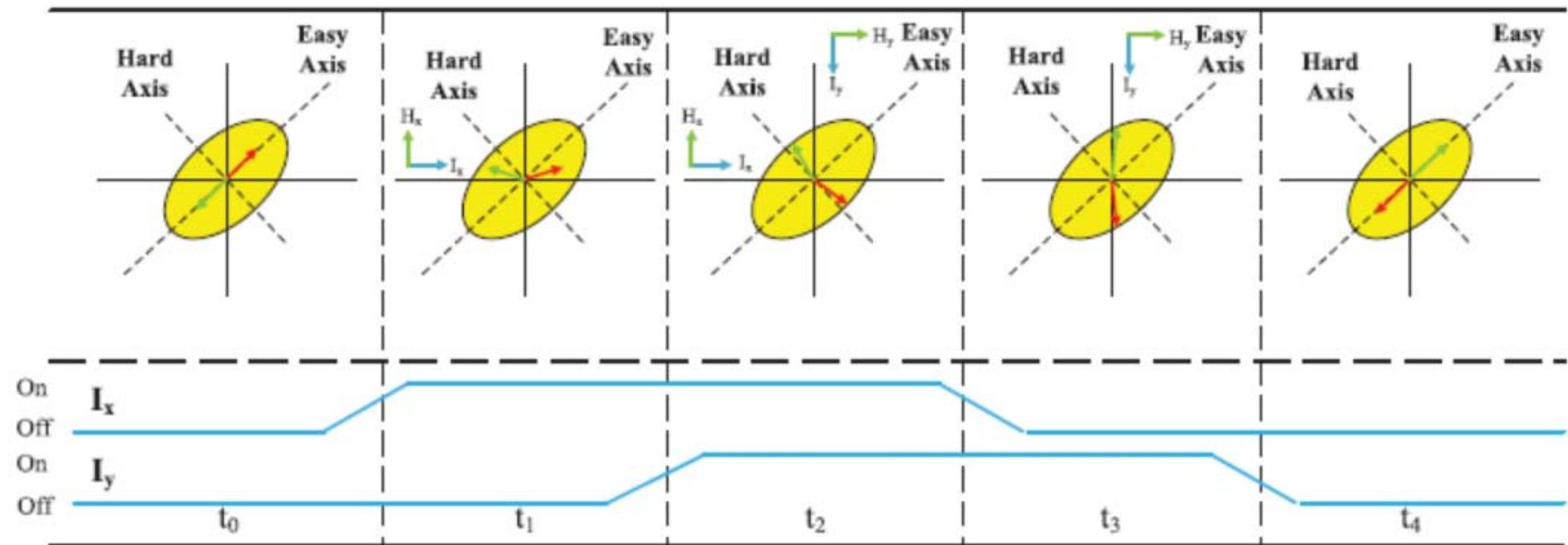


# 第1代MRAM：磁场驱动



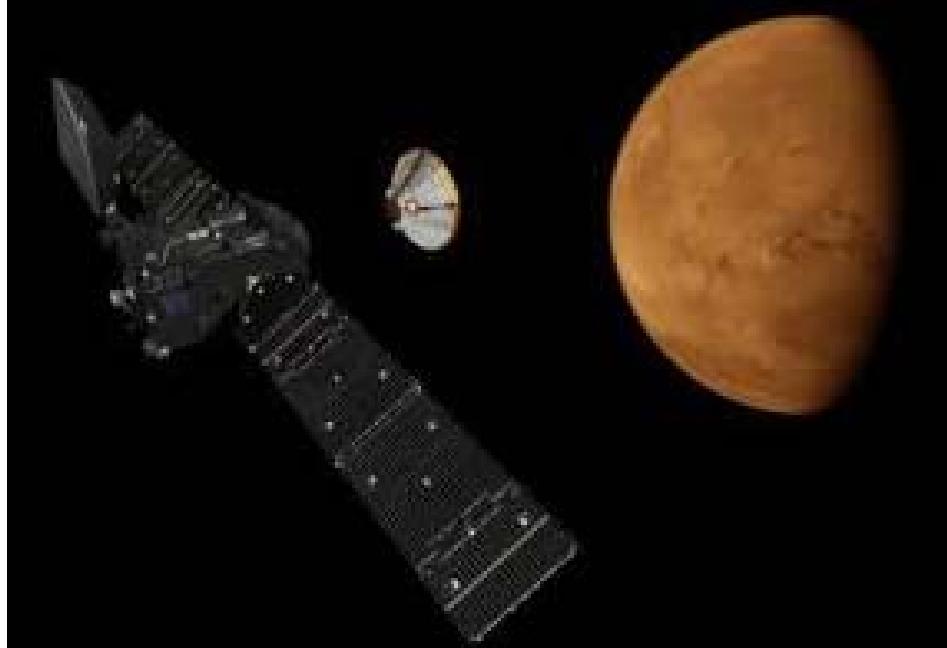


# 第1.5代MRAM：磁场驱动



**Toggle-MRAM**, 飞思卡尔于2006年量产，容量4Mb  
需要用电流（mA级）产生磁场，功耗比较大

# 第1.5代MRAM：磁场驱动



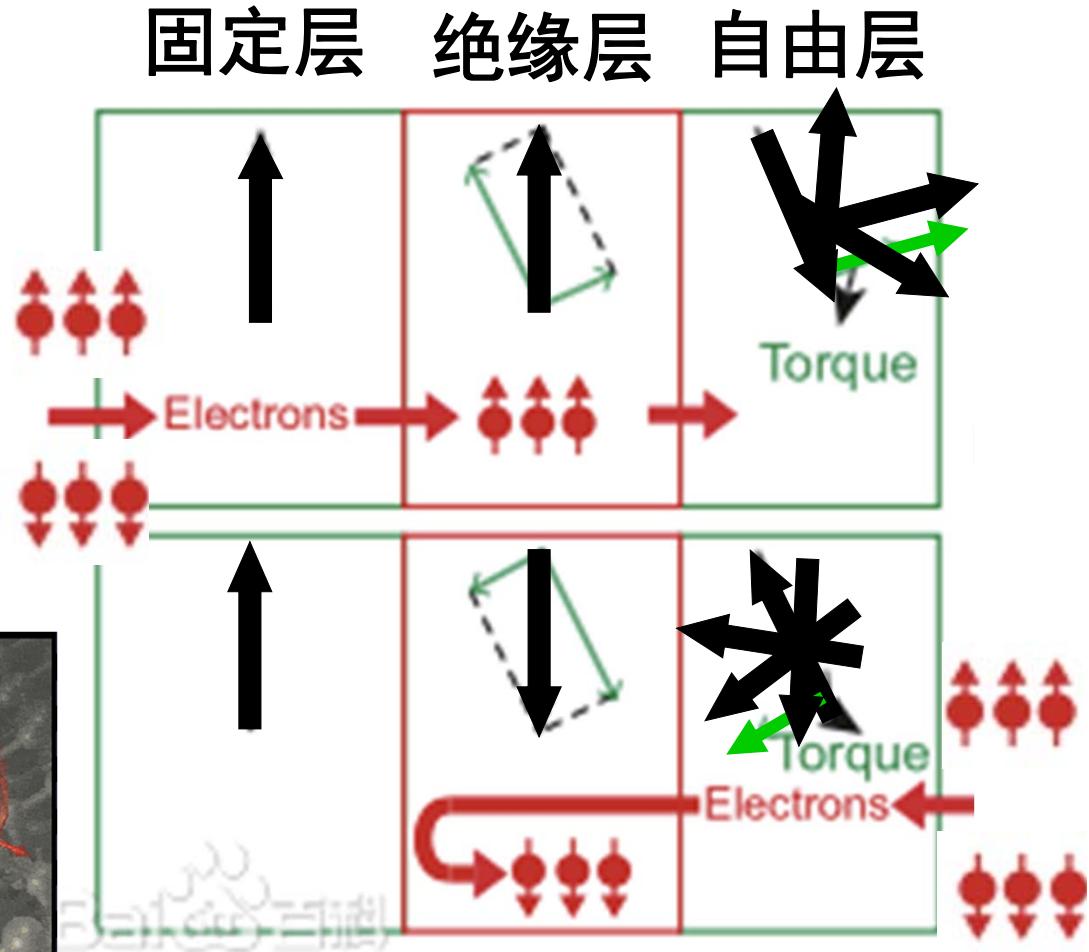
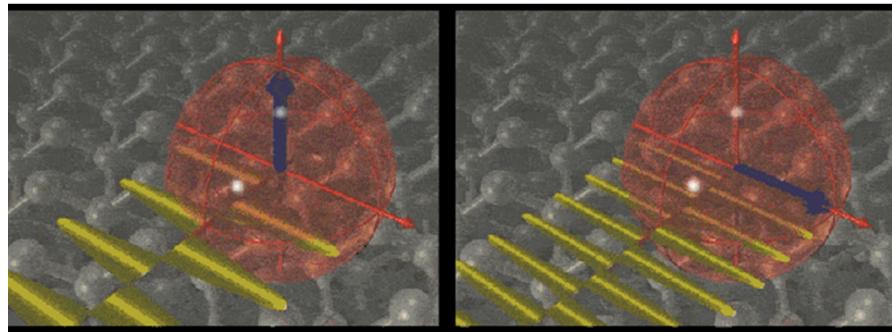
**非易失性  
天然抗辐射**

# 第2代MRAM：电流驱动STT

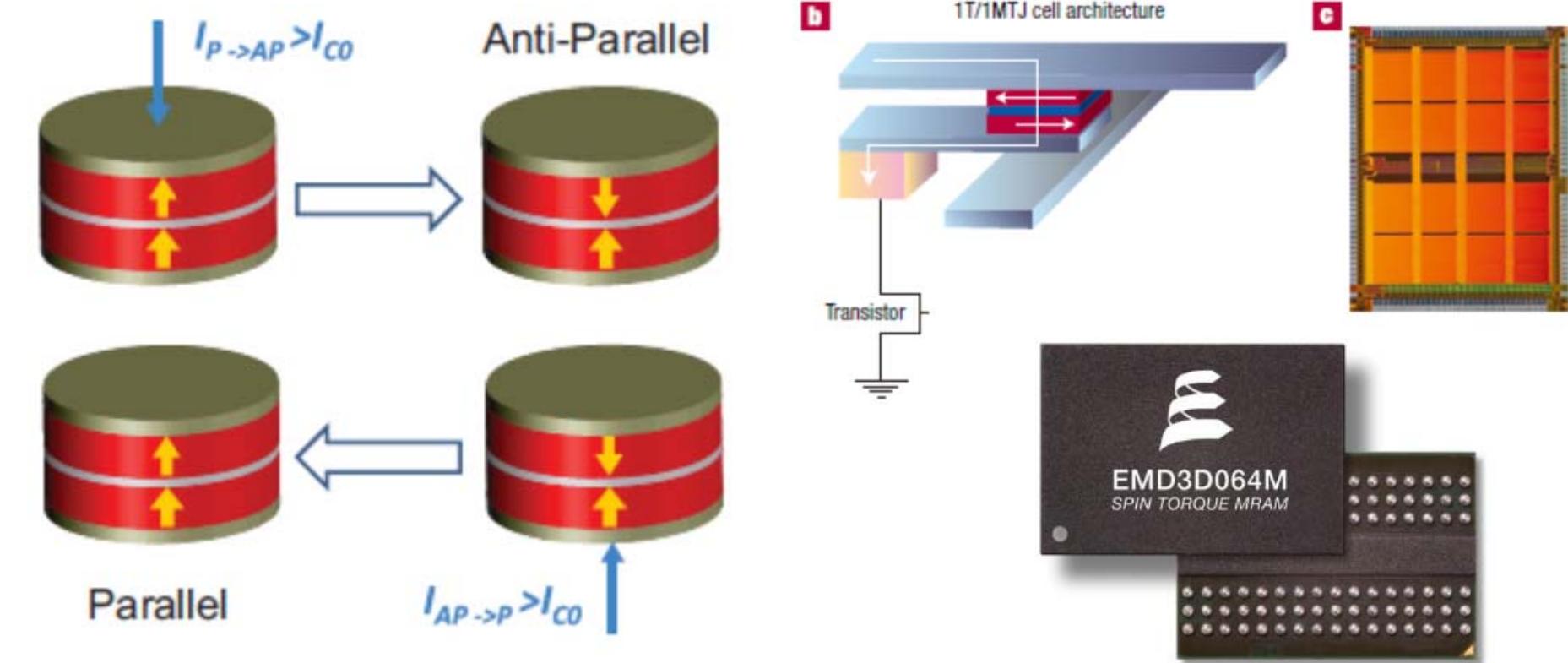


IBM.

1996年自旋转移矩(STT)  
理论模型，2000年验证



# 第2代MRAM：平面电流驱动STT



STT-MRAM, 飞思卡尔于2014年量产，容量256Mb

# 第2代MRAM: 2018年大规模产业化



TSMC to start eMRAM production in 2018



According to reports, Taiwan Semiconductor Manufacturing Company (TSMC) is aiming to start producing embedded MRAM chips in 2018 using a 22nm process. This will be initial "risk production" to gauge market reception.



TSMC also aims to start embedded RRAM chip production in 2019.

Global Foundries to offer Everspin's PMTJ STT-MRAM as an embedded memory solution



Everspin announced that it has licensed its PMTJ STT-MRAM technology to Global Foundries as an embedded 22nm memory. Everspin licensed its technology global foundries which will offer this as part of its 22FDX platform.



The 22FDX platform targets emerging applications such as battery powered consumer devices, IoT, Advanced Driver Assistance Systems (ADAS) and Vision Processing. Customers of Global Foundries will now be able to embed MRAM memory in next-generation SoC and MCU based producers.

Everspin recently filed for an IPO, aiming to raise around \$45 million. Everspin says that the company shipped more than 60 million MRAM discrete and embedded products - into data centers, cloud storage, energy,

Toshiba and Hynix to co-develop and produce MRAM products

Toshiba and Hynix announced an agreement to jointly develop MRAM products. Once the development is complete, the companies intend to establish an MRAM production plant together. We believe the companies intend to develop STT-MRAM technology.

Toshiba has been developing STT-MRAM for quite some time, and just a few days ago reported a breakthrough MT device that could pave the way towards Gigabit MRAM devices. They expect such chips within 3-4 years, so that's probably the time frame for the JV with Hynix. Hynix have already announced 1Gb eMRAM in 2009 using STT-MRAM technology a year earlier.



## Spin Memory announces an MRAM IP licensing agreement with Arm

2018-11-13 01:32:21-05



Spin Memory (previously Spin Transfer Technologies) announced that it has signed a licensing agreement with Arm. The license includes Spin Memory's Endurance Engine technology and IP - and as part of the agreement, Spin Memory will also work together to create SRAM-class MRAM design solutions.



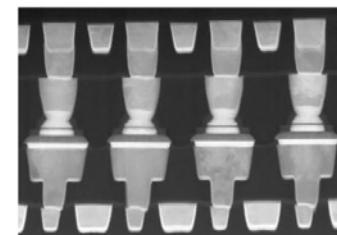
Spin Memory's Endurance Engine is a design architecture that is used to develop embedded MRAM solutions.

[Read more](#)

## Intel is developing embedded MRAM technologies



Intel says it will present a new paper detailing its MRAM research at the International Electron Devices Meeting (IEDM) in early December 2018. This is the first time we've seen anything R&D at Intel which is great news, even if it just a research paper.



Intel has apparently successfully integrated embedded MRAM into the company's 22nm FinFET CMOS technology on full 300mm wafers. The magnetic tunnel junction-based memory cells are built from dual MgO magnetic tunnel junctions (MTJs) separated by a CoFeB-based layer in a 1-transistor-1-resistor (1T-1R) configuration in the interconnect stack. Intel has manufactured a 7.2Mbit array with reported data retention figures in excess of 10 years and write endurance of greater than 10<sup>16</sup> cycles.

## Samsung to soon start mass producing 28nm embedded MRAM



Digitimes reports that Samsung Foundry will soon start mass producing MRAM chips using Samsung's 28nm fully depleted silicon-on-insulator (FD-SOI) process technology.

Digitimes says that Samsung has already completed the tape-out of its embedded MRAM which will be utilized in the lower power I.MX-series chipset targeted at automotive, multimedia and display panel applications.

## Avalanche sign an agreement with UMC for 28nm embedded STT-MRAM technology



pMTJ STT-MRAM developer Avalanche Technology announced that it has entered into a joint development and production agreement with Taiwan's United Microelectronics Corporation (UMC), a global semiconductor foundry.

UMC will provide embedded non-volatile STT-MRAM based on UMC's 28nm CMOS manufacturing process, which will enable customers to integrate low-latency, very high performance and low power embedded MRAM memory blocks into MCUs and SoCs, targeting the Internet of Things, wearable, consumer, industrial and automotive electronics markets.

UMC and Avalanche Technology are also considering to expand the cooperation beyond 28nm.

In February 2016 Avalanche Technology raised \$23 million and announced it has a substantial debt facility in place with Horizon Technology Finance. In 2016 the company also entered into a manufacturing agreement with Sony Semiconductor Manufacturing Corporation (SSMC) for volume production of its STT-MRAM on 300 mm wafers. The production of 4Mb to 64Mb discrete chips was planned to begin in early 2017. Avalanche started to sample 32Mb and 64Mb STT-MRAM chips in 2015.

## Toshiba developed STT-MRAM based microprocessor cache memory



Toshiba developed new STT-MRAM technology that can be used to enable MRAM based cache memory for microprocessors. The L2 cache alone uses about 80% of the power consumed by the CPU, so reducing the power consumption of the cache is very important - and STT-MRAM may reduce this consumption by about 60%. It's not clear how close is this technology to actually being commercialized.

Toshiba's new STT-MRAM uses a dual-cell (2T-2MTJ) circuit in which the two MTJs have complementary resistive states (high and low resistive states). This creates the low power and also increases the readout signal intensity - and so improves access speed. In fact, the access time is 1 ns - very close to that of SRAM, while the write time (2.1ns) is similar to SRAM. Toshiba also implemented error correction mechanisms into the cache STT-MRAM chip.

In December 2013, Toshiba announced a new computing architecture that uses only STT-MRAM to perform both operations and storage. The idea support computing capability, register file, primary cache and secondary cache all on the same perpendicular STT-MRAM, and Toshiba says it could lead to CPUs that are drastically faster and more efficient.

Source: Nikkei Technology

## Mentor to support eVaderis eMRAM technology on its FastSPICE platform



eVaderis announced that it is collaborating with Mentor to build advanced design solutions for embedded MRAM (eMRAM) technologies, based on Mentor's Analog FastSPICE (AFS) platform.

Earlier this month GlobalFoundries and eVaderis announced that the two companies are co-developing an ultra-low power microcontroller (MCU) reference design using GF's embedded MRAM on the 22nm FD-SOI (22FDX) platform.

Tags: [Embedded MRAM](#)

Posted: Mar 28, 2018 by Ron Mertens



# 第2代MRAM：2020年典型应用

September 29, 2020

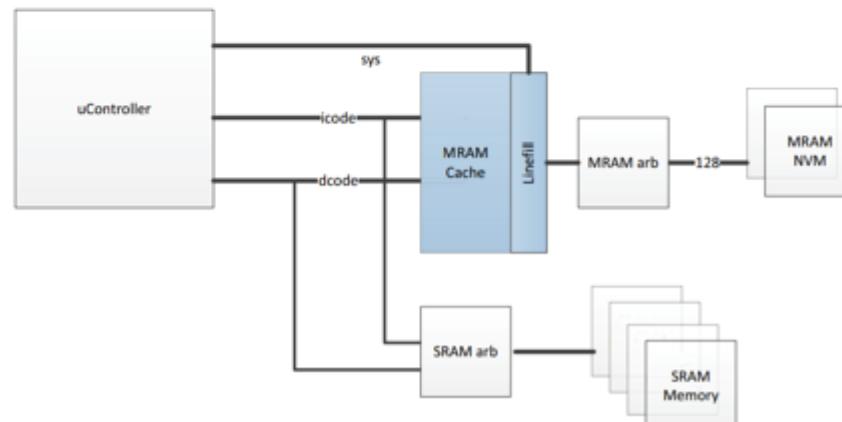
## Ambiq Apollo4 Undercuts IoT Power

Unique Subthreshold Voltage Drops MCU into Microwatt Range

by Jim Turley

Apollo4 has **2MB of MRAM** (magnetoresistive RAM) and another 1 MB of SRAM.

Ambiq says that Apollo4 consumes just **3  $\mu$ A per MHz (10  $\mu$ W/MHz at 3.3V)**, which works out to about 2mW at top speed.



1:51 31 •

86%



Jeongdong Choe · 2 度

Senior Technical Fellow at TechInsights, Ph. D.

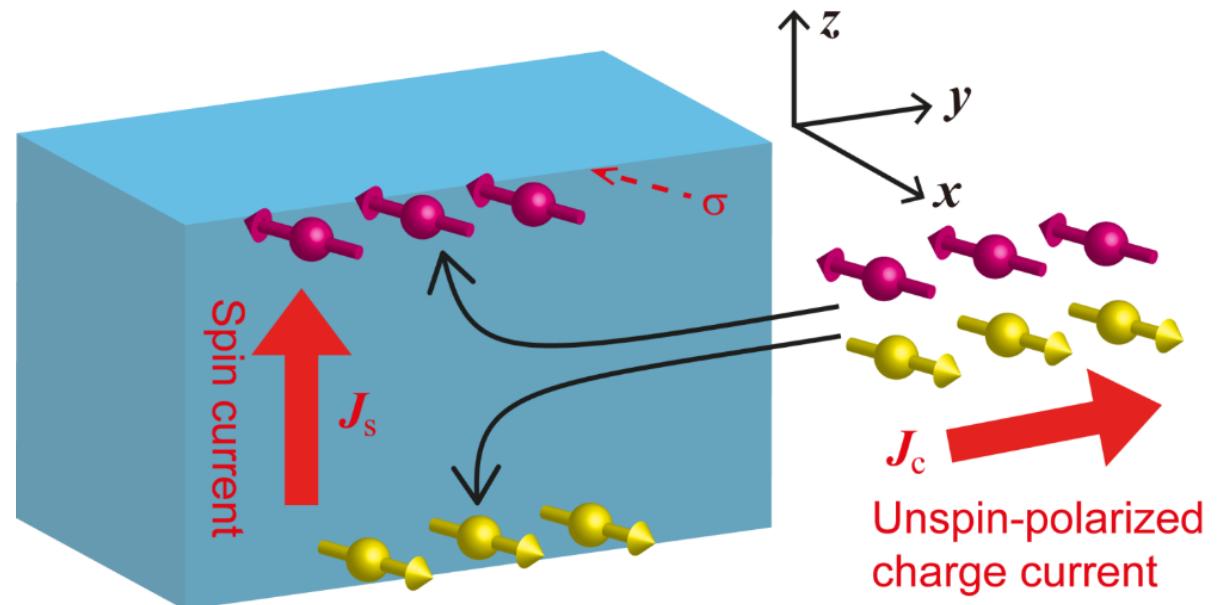
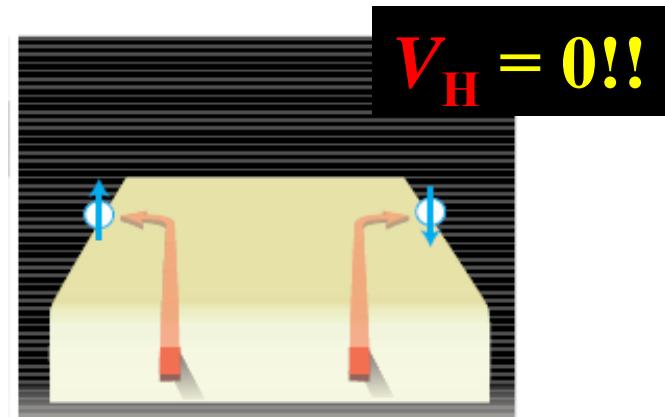
15 小时前 ·

#Samsung #28FDS #eMRAM found.

Last year, Samsung announced commercial production of its first **#embedded** MRAM (eMRAM) product based on its 28-nm FD-SOI process. We, TechInsights, finally specified the foundry customer for the product. We found **#Sony** GNSS transceiver and controller die with Samsung 28 FDS eMRAM (eSTT-MRAM, 8 Mb) removed from **#Huawei** GT 2 Smartwatch. The eMRAM cell size 190 nm x 190 nm (0.0364  $\mu$ m<sup>2</sup>) on M6 with FD SOI-transistors, and embedded memory array area portion 4.3 % of the die. For more information, please visit/contact **#TechInsights** (<https://lnkd.in/gZHaw9E>).

[查看译文](#)

# 第2.5代MRAM: 垂直电流驱动, 自旋霍尔效应(SOT)



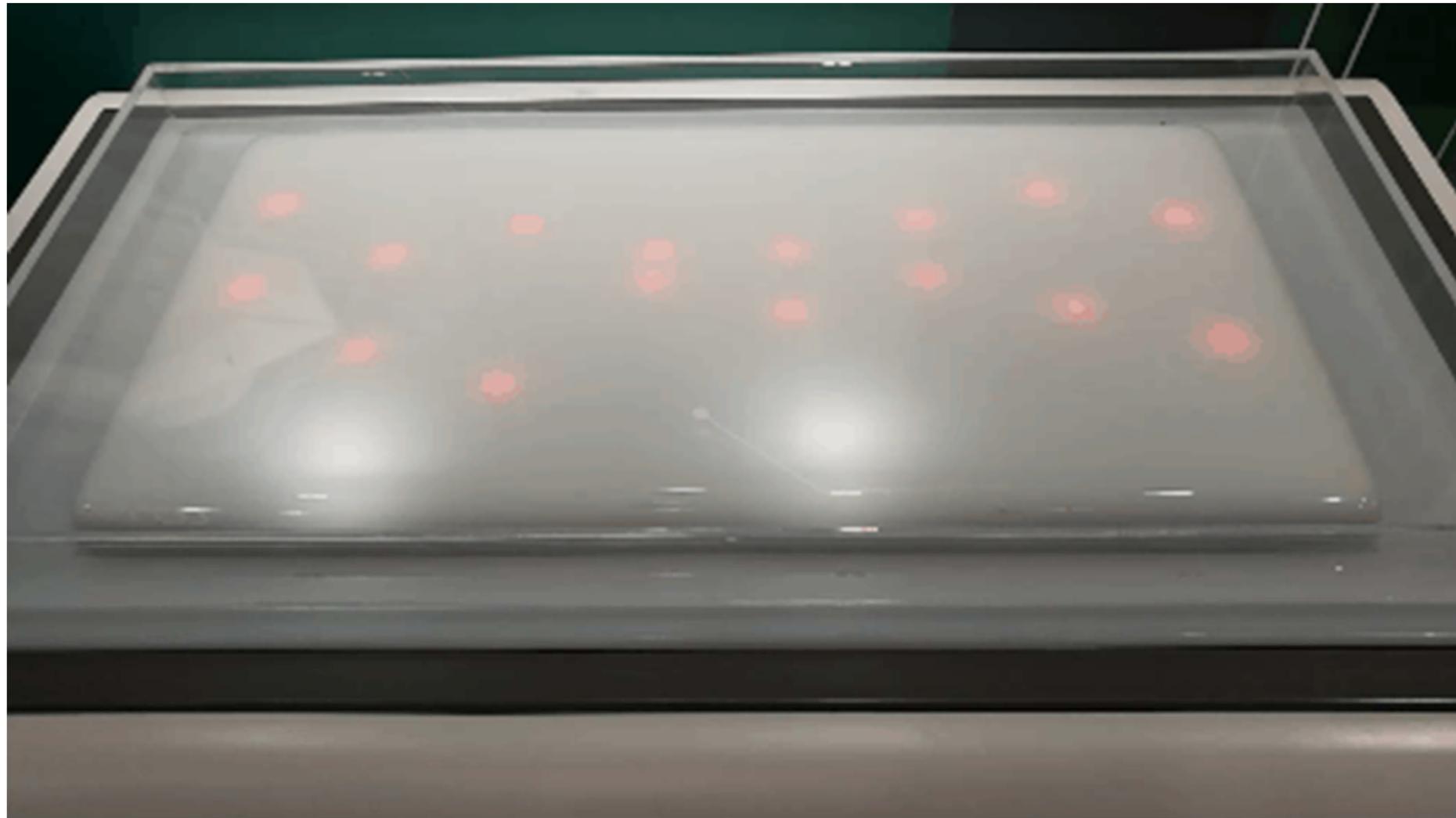
自旋电流



为什么霍尔电阻为0?  
为什么自旋电流中总电流为0?



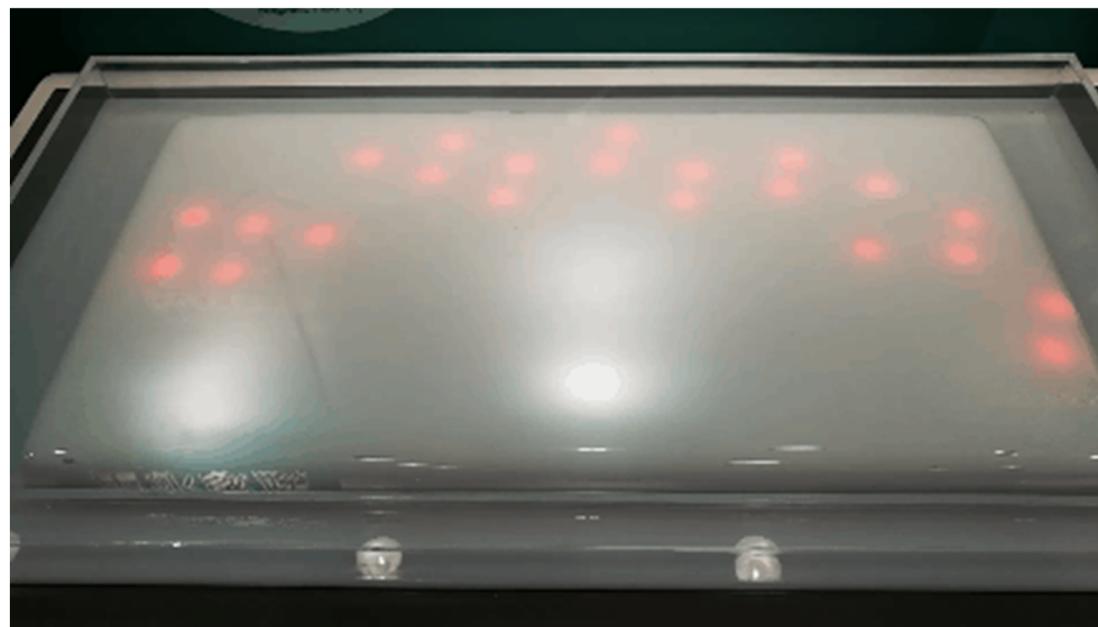
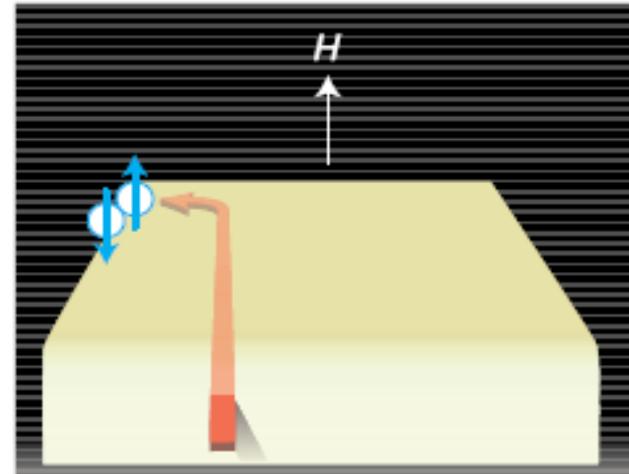
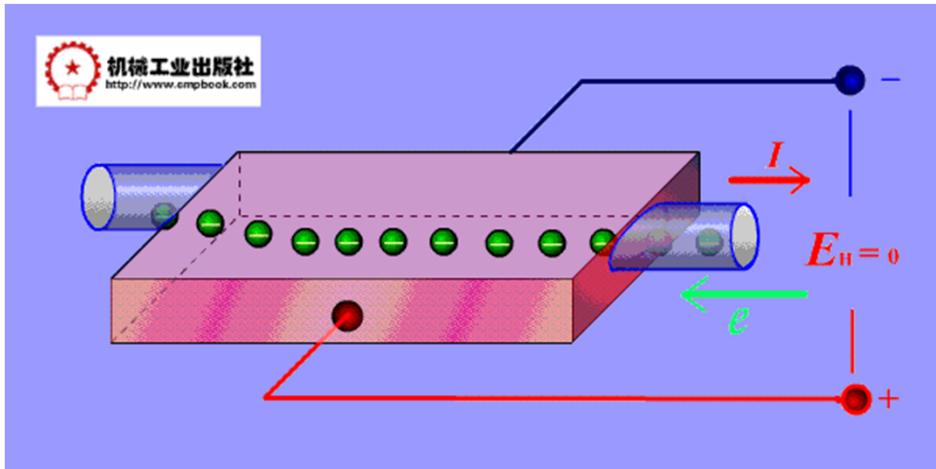
# 电子->电流



[https://www.cdstm.cn/subjects/ggkf40/zxzx/201808/t20180803\\_840125.html](https://www.cdstm.cn/subjects/ggkf40/zxzx/201808/t20180803_840125.html)



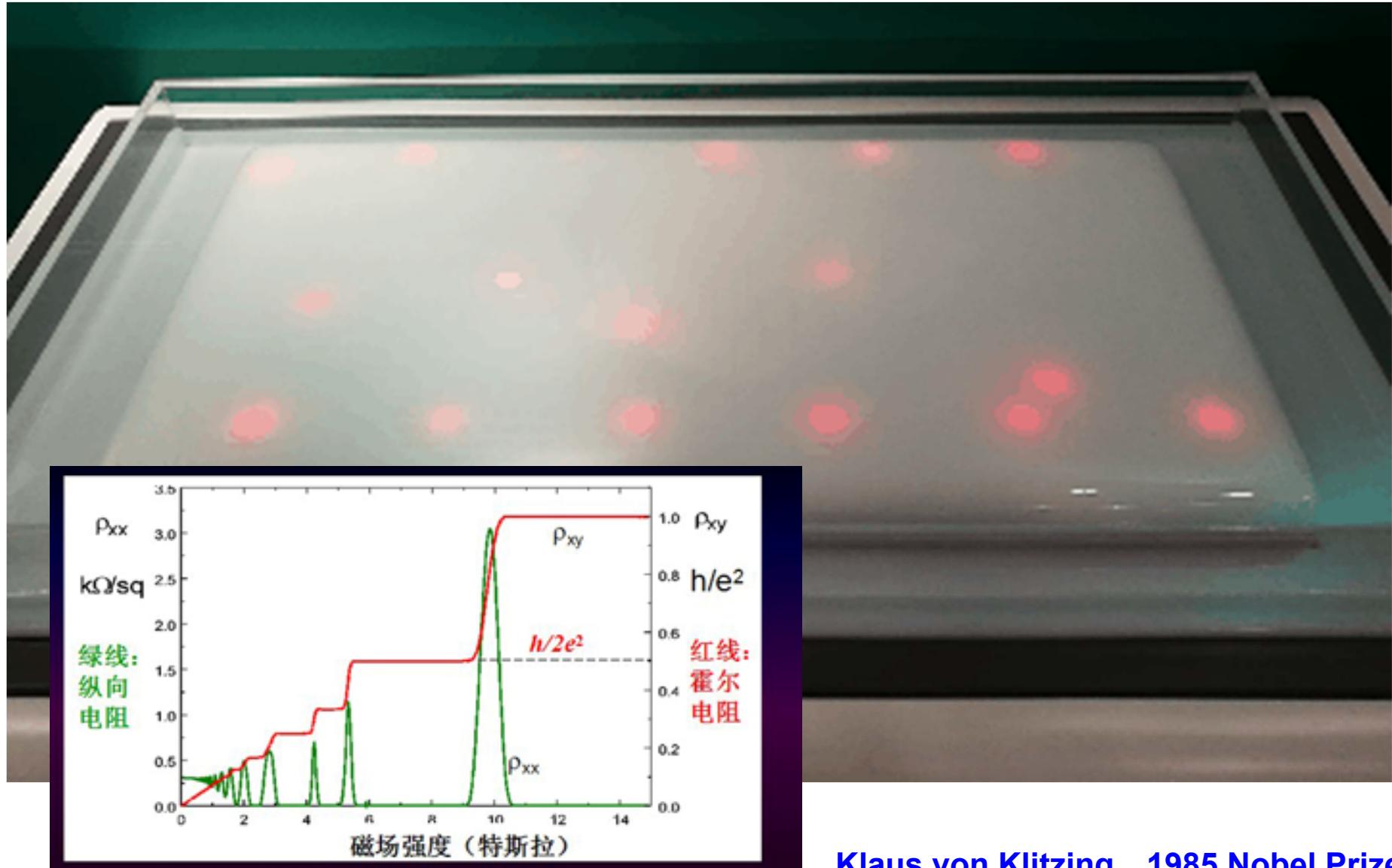
# 霍尔效应, 1879



霍尔传感器

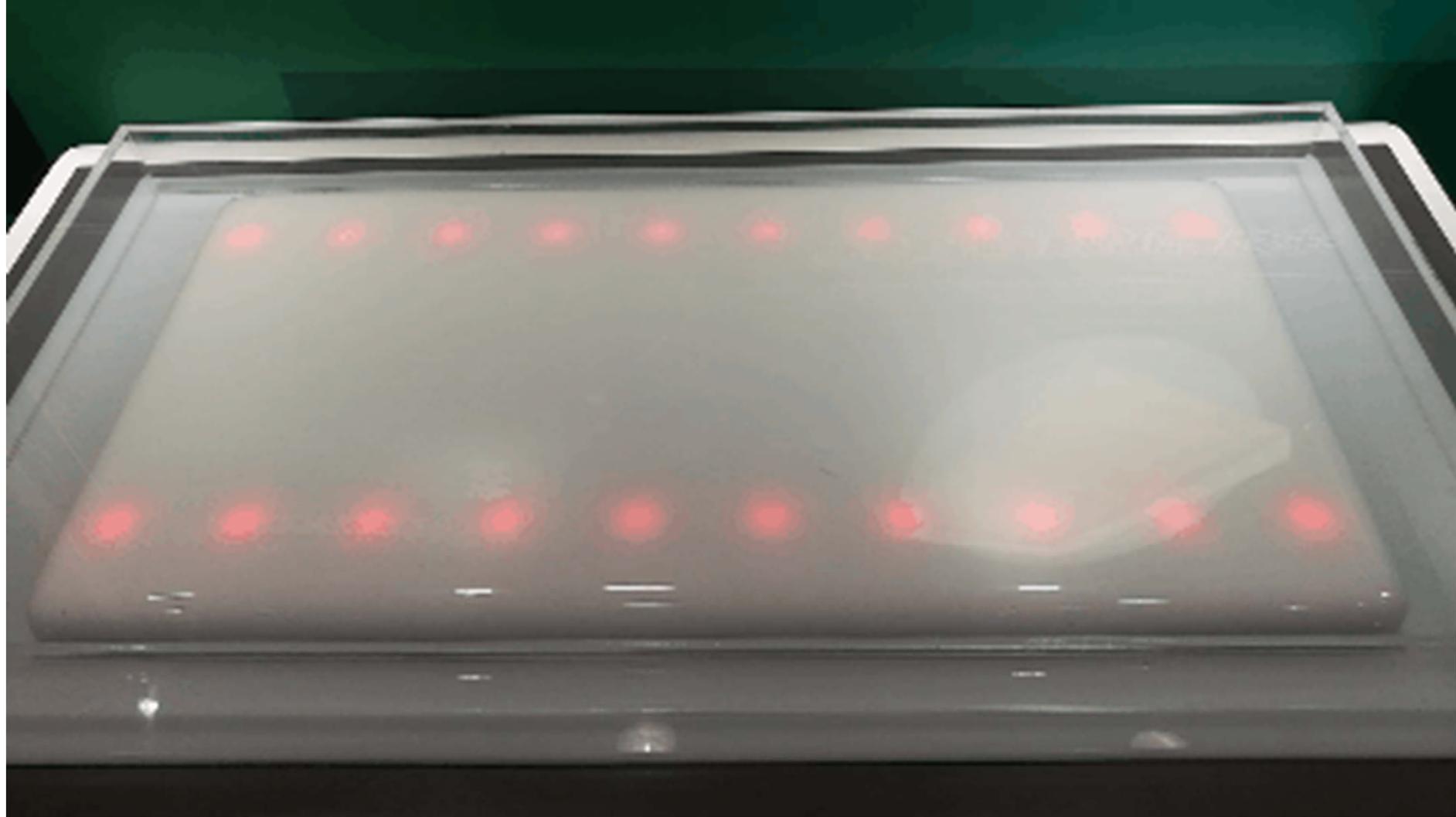


# 量子霍尔效应, 1980



Klaus von Klitzing, 1985 Nobel Prize

# 量子反常霍尔效应, 2006, 2013

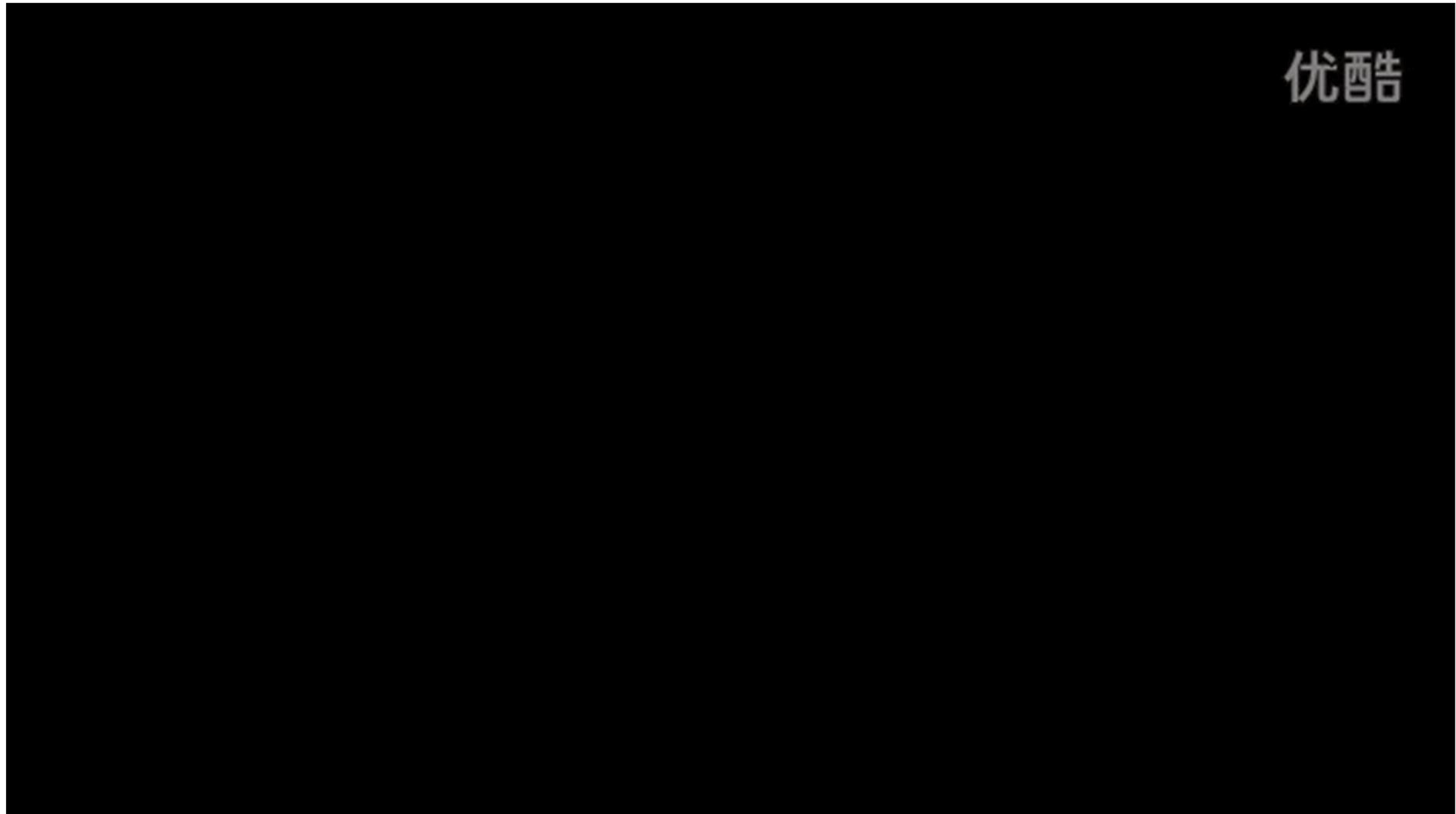


斯坦福张守晟教授理论预测, 清华大学校长薛其坤院士实验证实



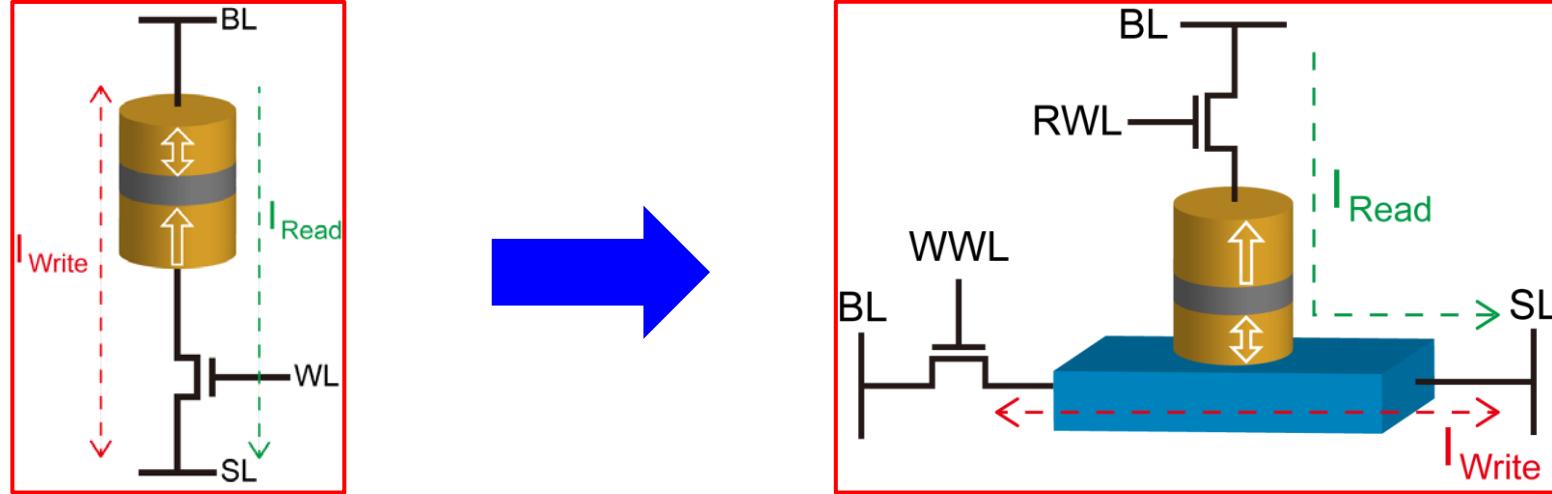
# 霍尔效应家族

优酷





# 第2.5代，SOT-MRAM



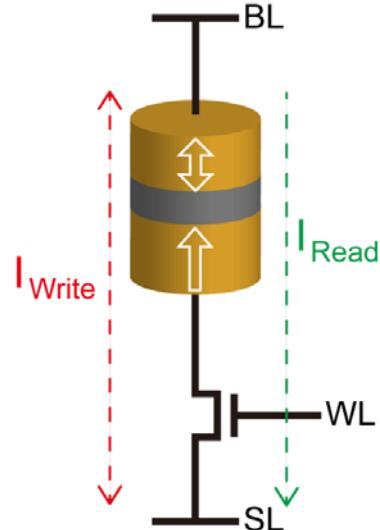
## 第二代：自旋转移矩

- ✓ 1996 理论提出
- ✓ 2004 实验验证
- ✓ 2012 产品商用
- ✓ 主要面向民用消费品

## 第三代：自旋轨道矩

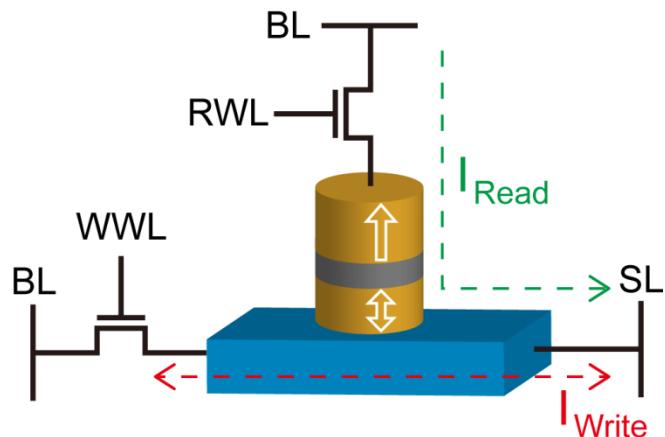
- ✓ 2011 实验验证
- ✓ 近期 IMEC在12寸晶圆上首次制出单元阵列

# SOT-MRAM VS STT-MRAM



## □自旋转移矩

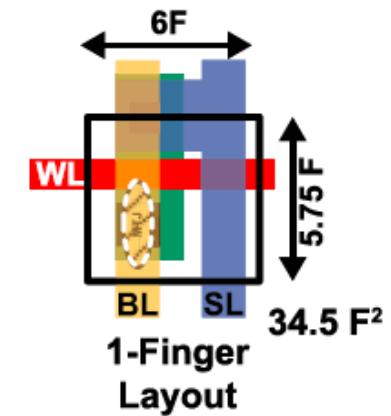
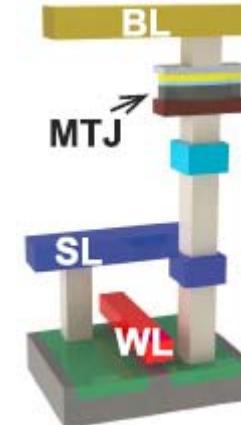
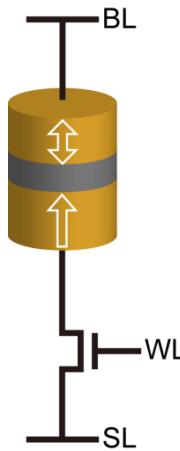
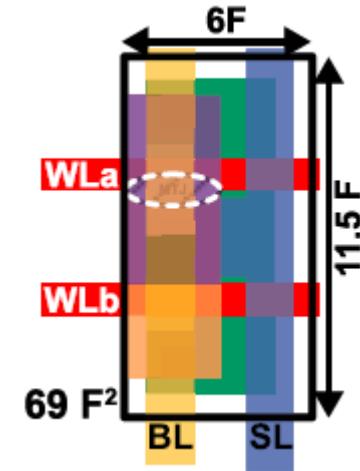
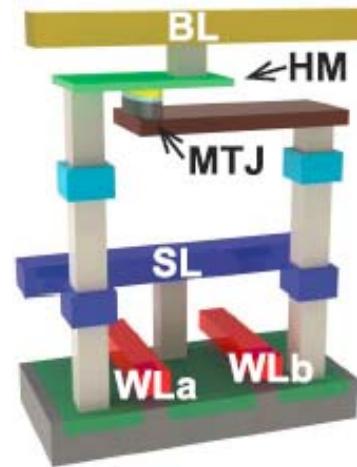
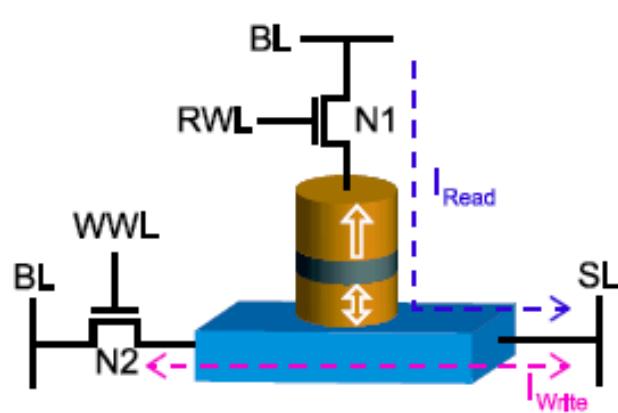
- ✓ 结构简洁
- ✗ 有孵化延迟，限制写入速度。
- ✗ 写入电流经过势垒，易引起器件击穿
- ✗ 写入具有非对称性



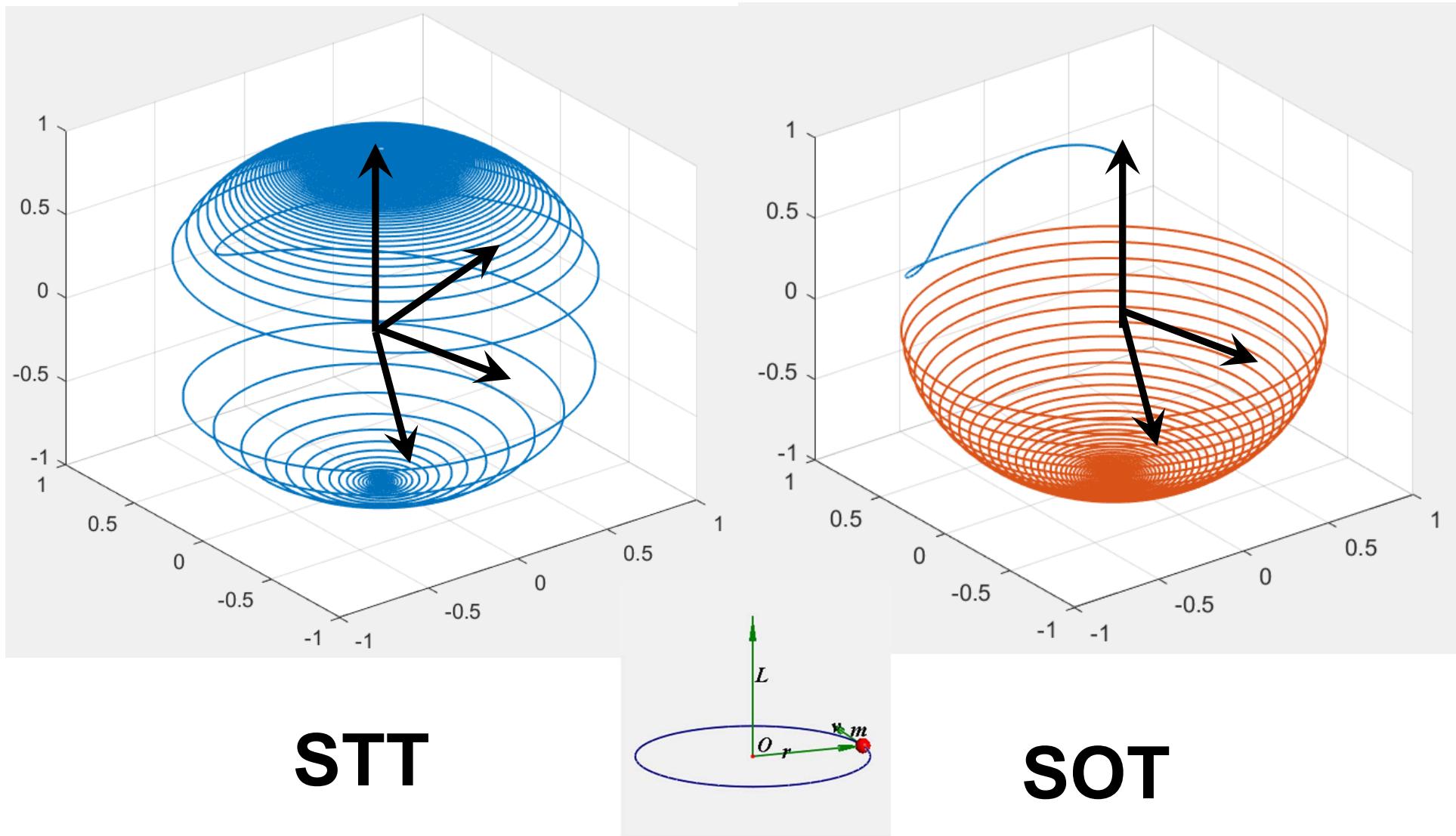
## □ 自旋轨道矩

- ✓ 速度极快，读写支路分离。
- ✗ 三端口器件，导致较大的面积开销。

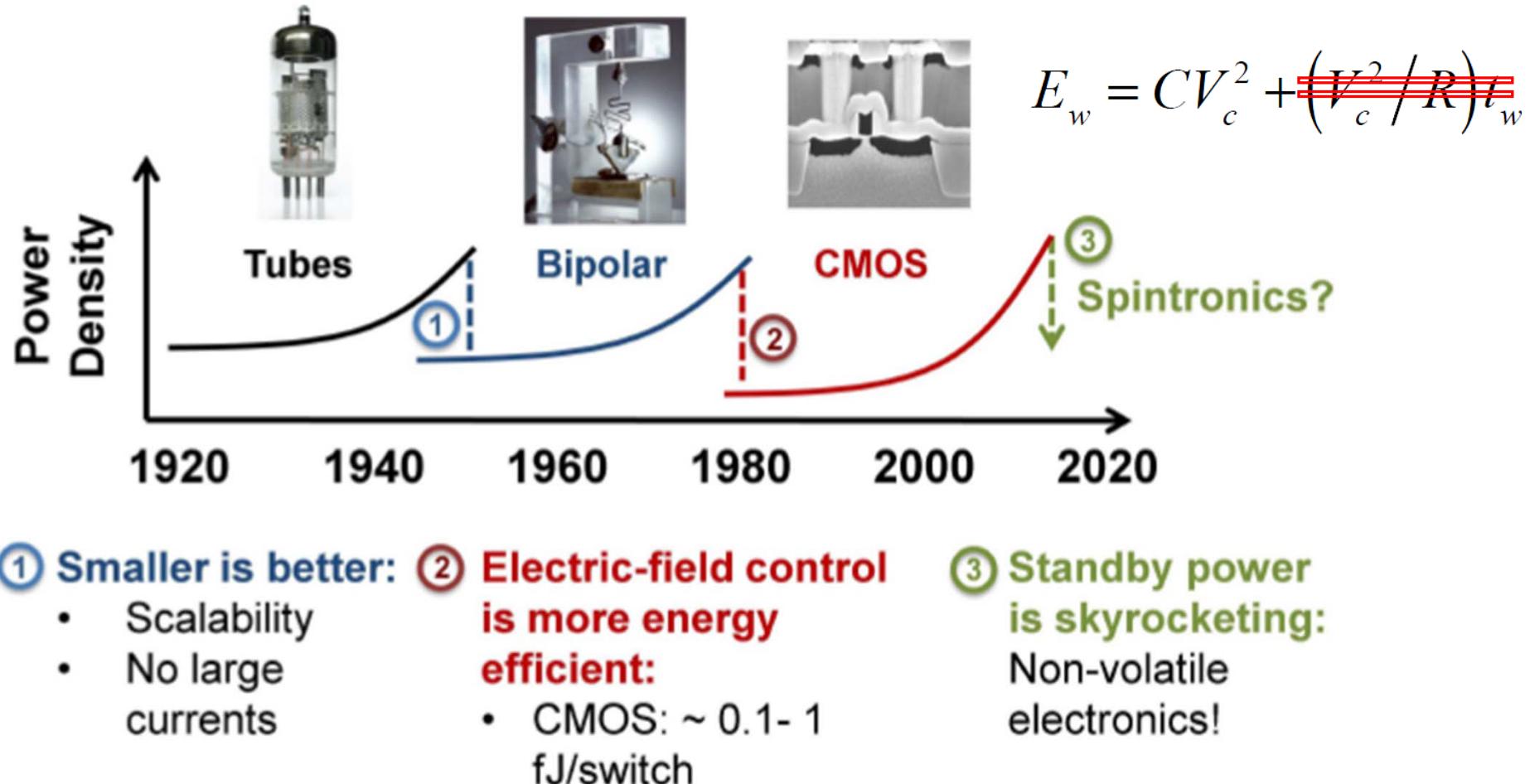
# SOT-MRAM VS STT-MRAM (面积)



# SOT-MRAM VS STT-MRAM (速度)

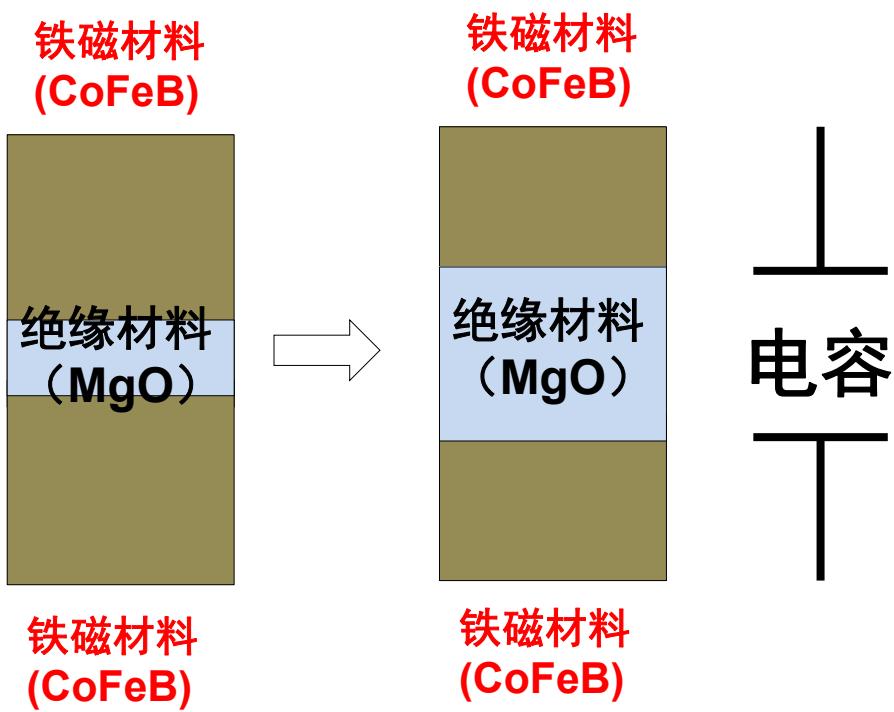


# 从半导体发展历程学到的经验

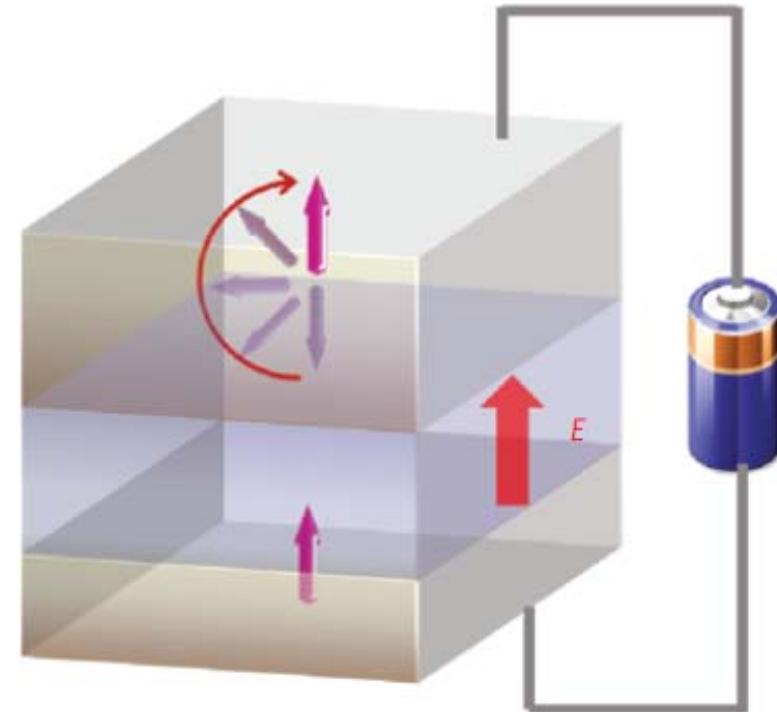


电场控制的器件通常比电流控制的器件更低功耗

# 第3代，电场驱动（MeRAM，研发早期）



STT-MRAM    MeRAM



弱效应，目前产业化  
的难点是电压降不下来

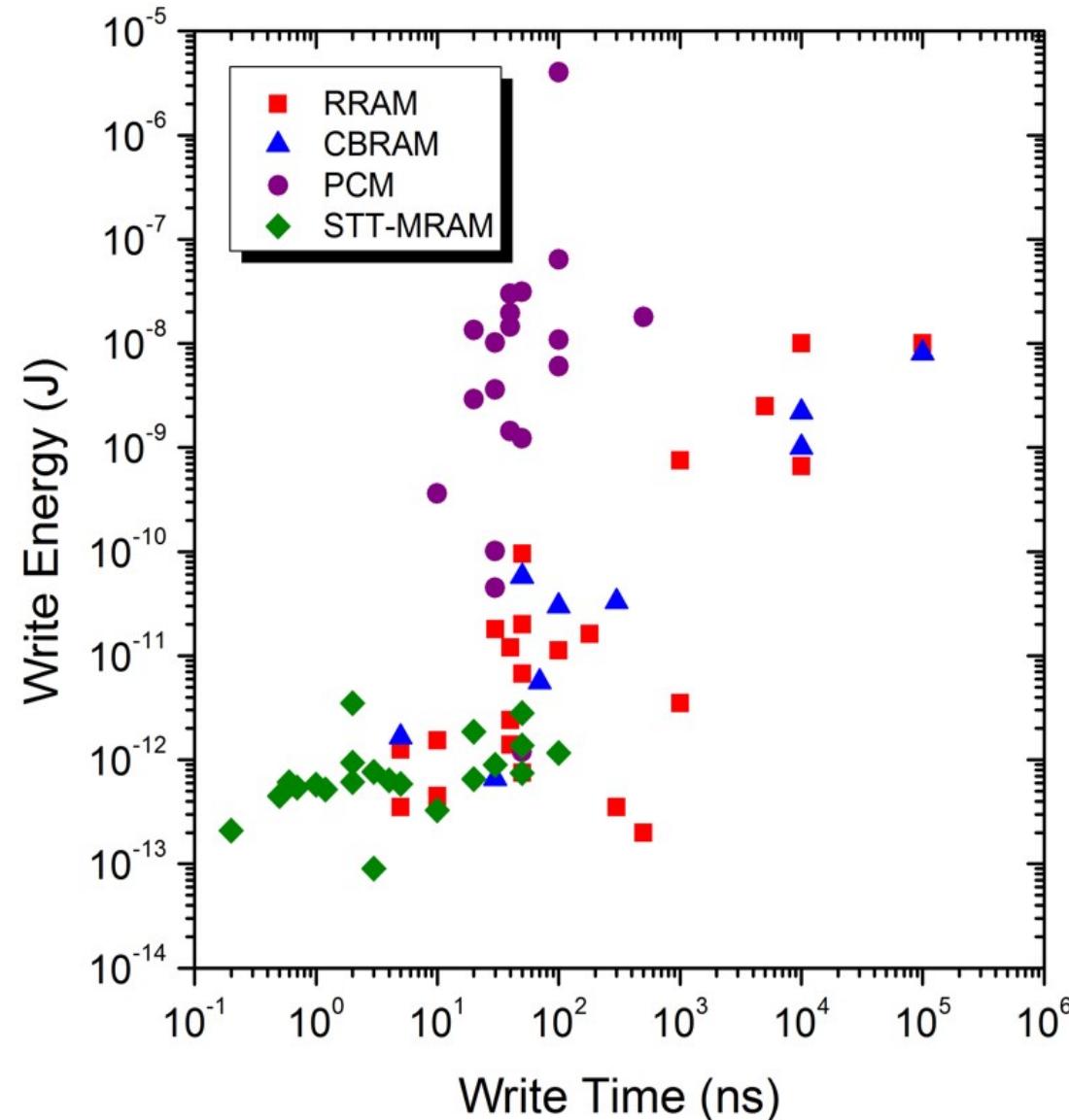


# 三代MRAM性能对比

	Existing	Emerging	Existing	Prototype	Emerging	Emerging	Existing
Technology	eFlash	eReRAM	eDRAM	STT-MRAM	SOT-MRAM	MeRAM	SRAM
Endurance (Cycles)	$10^5$	$10^5$	$10^{15}$	$10^{15}$	$10^{15}$	$10^{15}$	$10^{15}$
Read Time (ns)	10	3–10	1–2	1–5	1–5	1–5	1
Write/Erase Time (ns)	25 μs/2 ms	500 /100 μs	1–2	5–10	<1	<1	1
Cell Size (area in $F^2$ )	40–100	15–30	40–100	40–50	50–70	20–30	>150
Bit Density (Gb/cm <sup>2</sup> )	0.5–1	1.5–3	0.5–1	1	0.75	2	<0.3
Read Energy/Bit (fJ)*	$10^6$	1000	100	10–20	10–20	1–5	1–5
Write/Erase Energy/Bit (fJ)*	$10^6$	1000 / $10^6$	1000	100–200	<10	<5	1
Nonvolatile	Yes	Yes	No	Yes	Yes	Yes	No
Standby Power	None	None	Refresh	None	None	None	Leakage

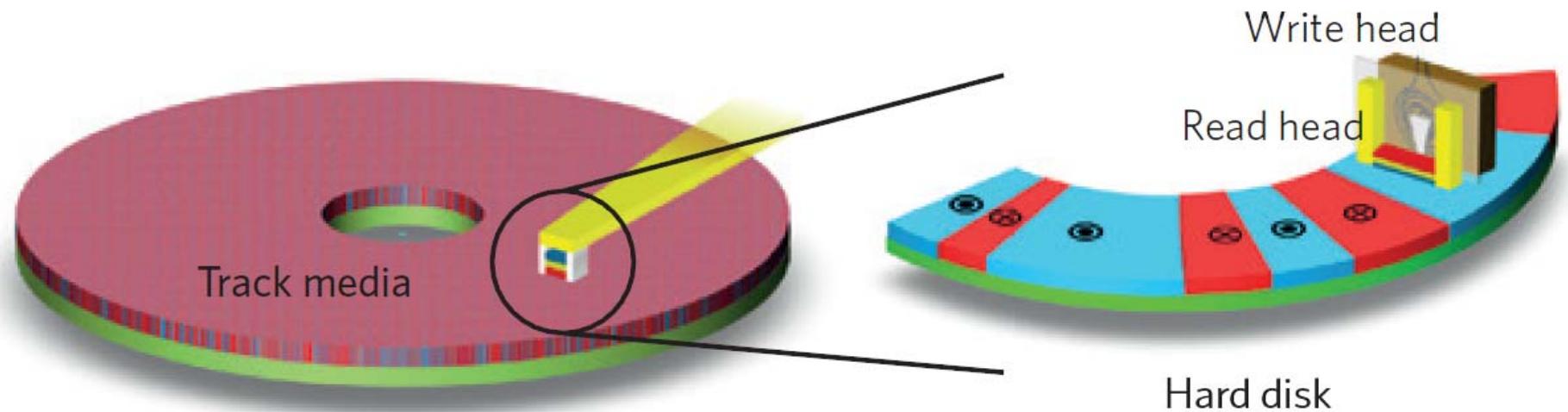


# 新型存储器对比



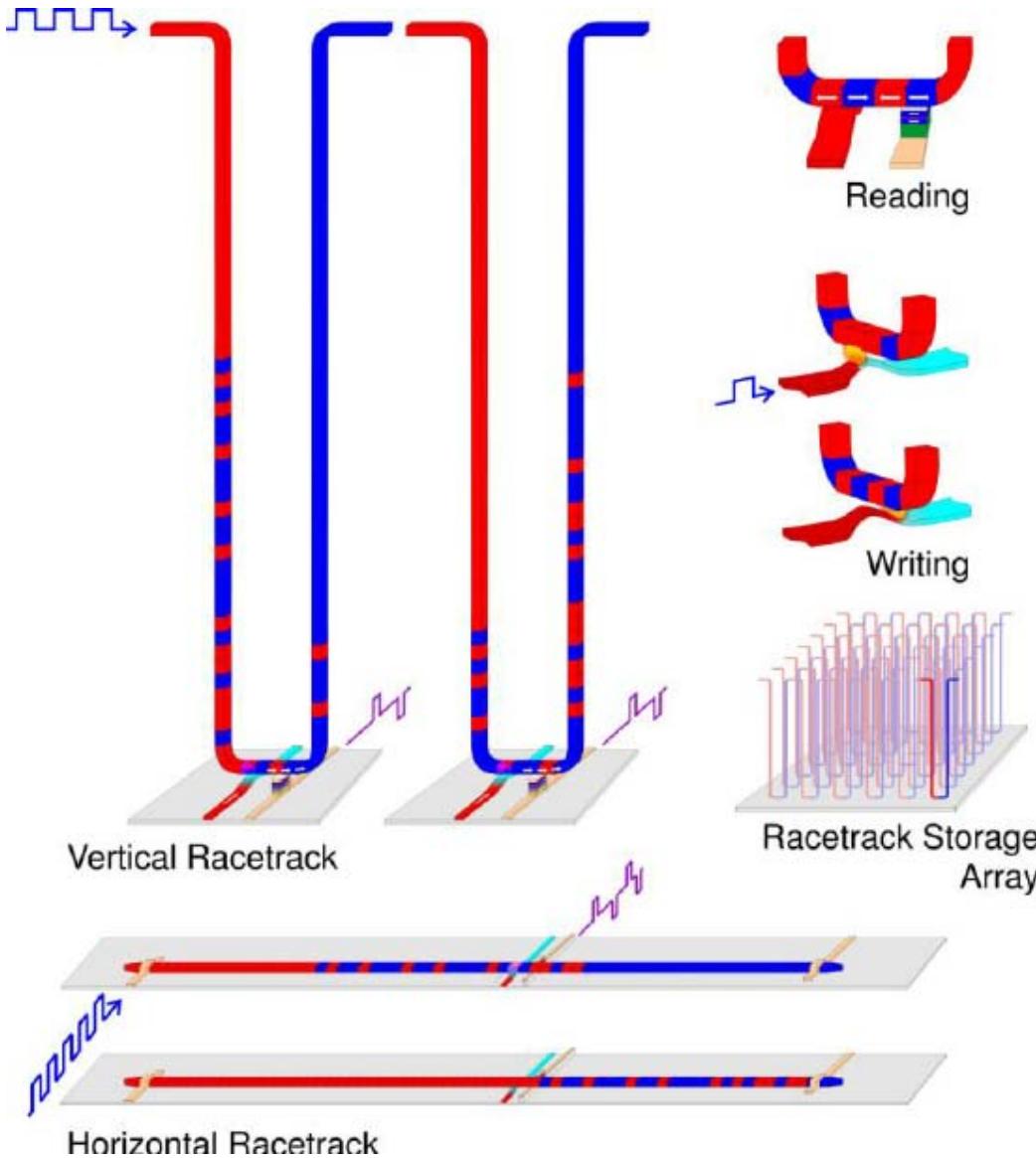


# 回顾：机械硬盘



- 1、面内存储，存储密度受限
- 2、机械传动，可靠性、功耗、速度等问题

# 赛道存储器, 2008



诺贝尔奖?



Stuart Parkin, 1955  
Science, 2008



SherWen



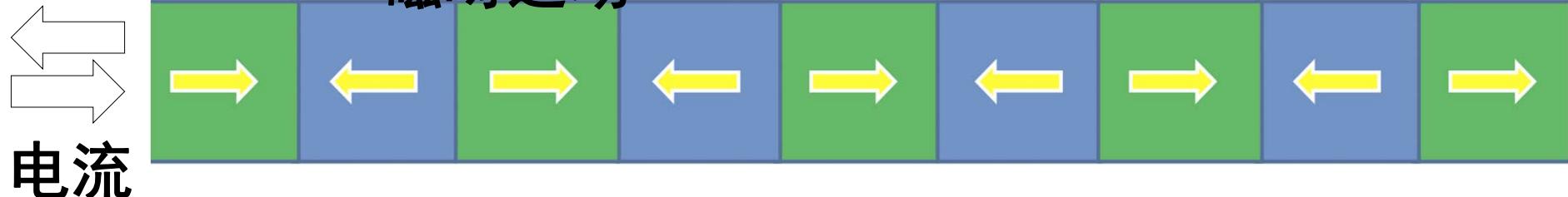
# 赛道存储器



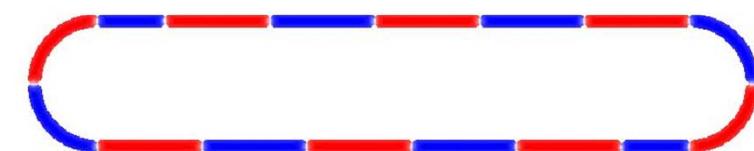
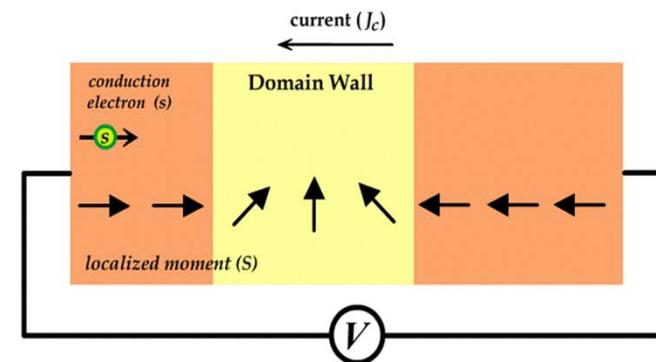


# 赛道存储器

磁畴运动

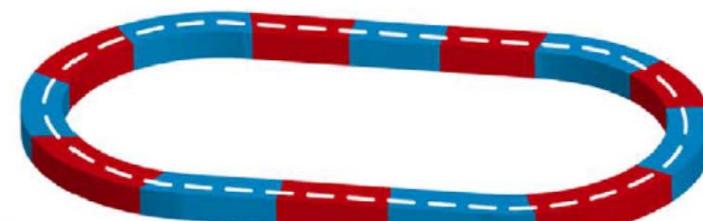


写入 读取



$t = 0.0 \text{ ns}$

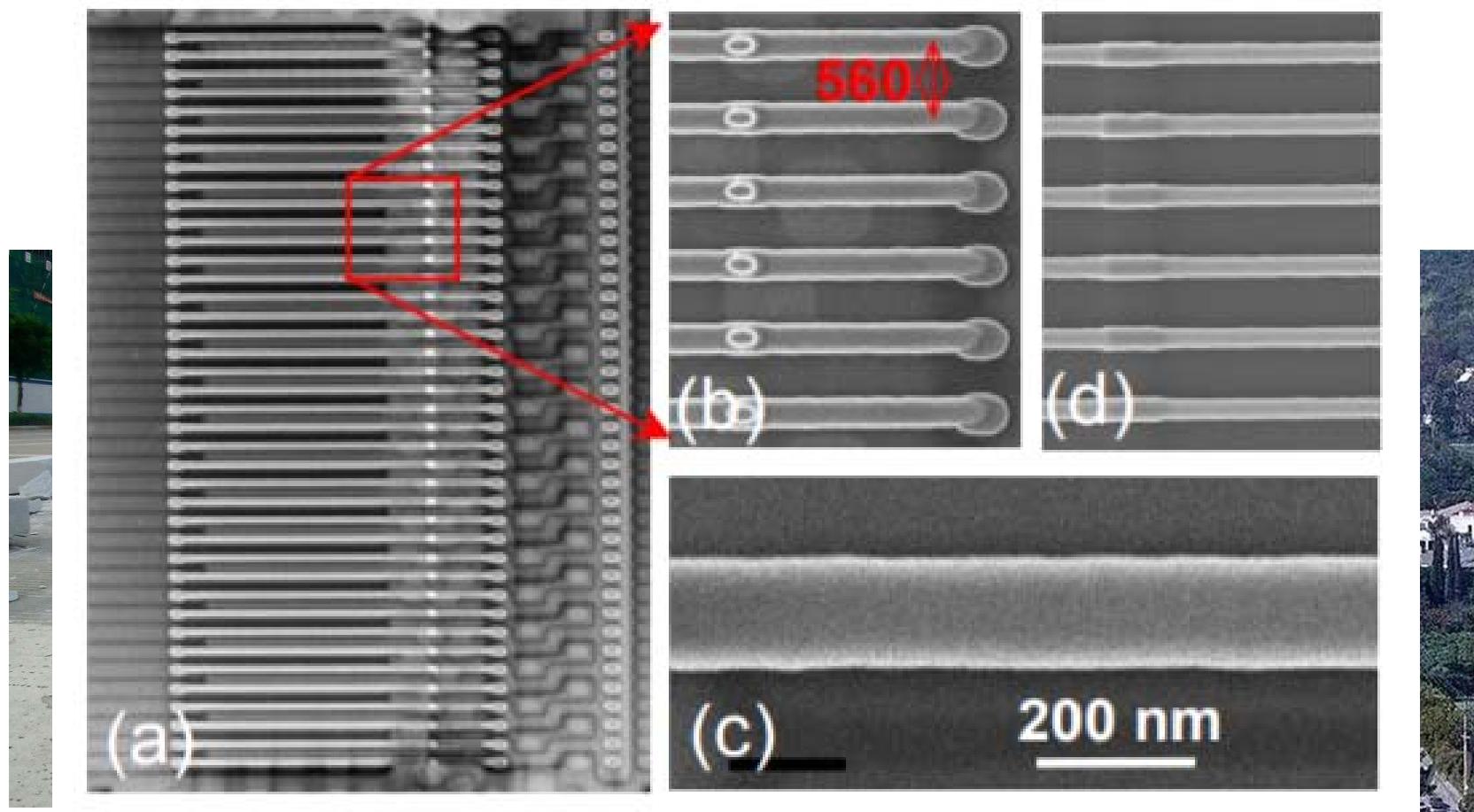
问题?



# 赛道存储器的产业化难点

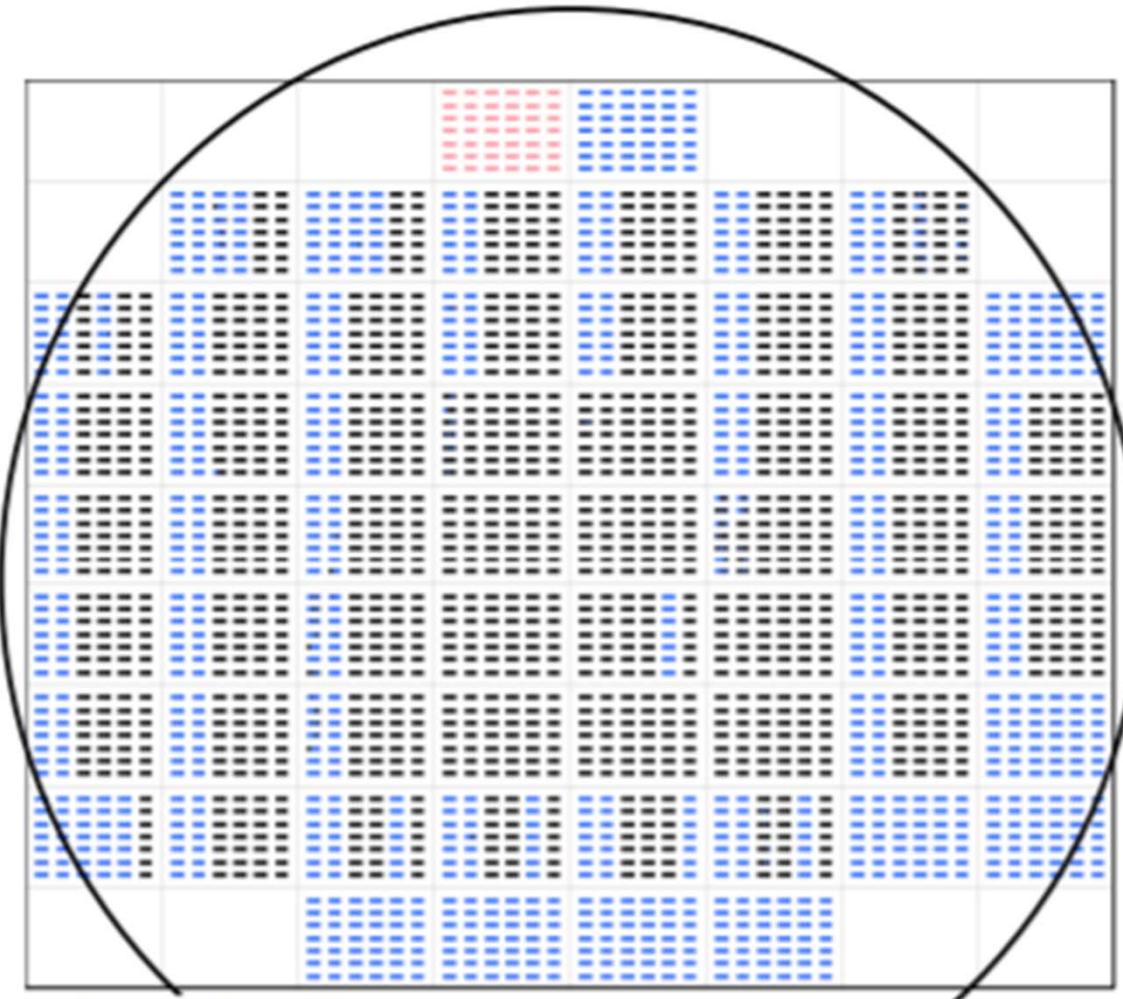
对材料纯净度、制备工艺要求非常高

**40 nanowires (32 active) IBM. 2011**



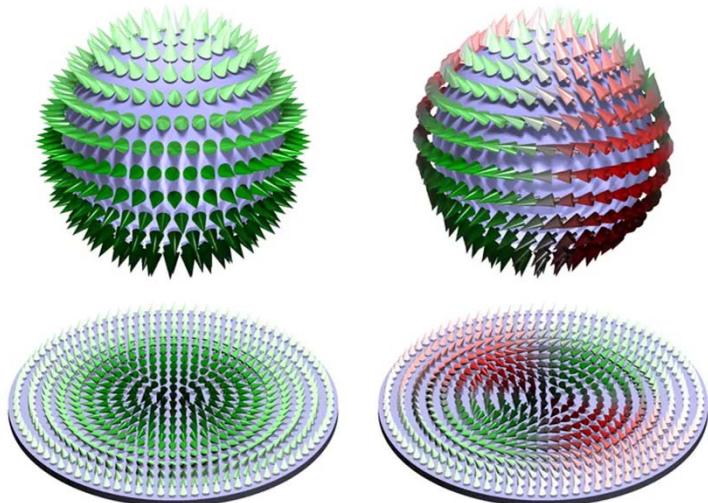


# 赛道存储器的产业化难点



short circuit  
**good device**  
open circuit

# 斯格明子 (Skyrmion)



3D view



2D view

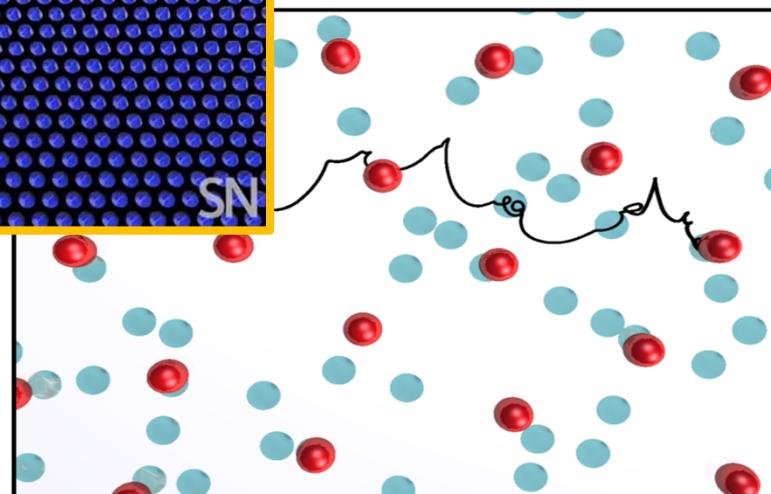
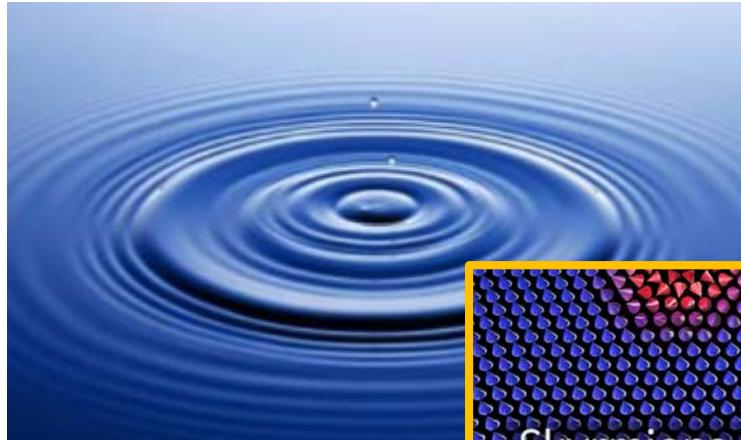
Science, 2009



T. H. R. Skyrme  
1962理论预测

类粒子的涡旋磁化结构  
尺寸可以微缩到3nm  
运动速度可以到1000m/s  
驱动电流可以 $10^6 \text{ A/cm}^2$

# 斯格明子 (Skyrmion)

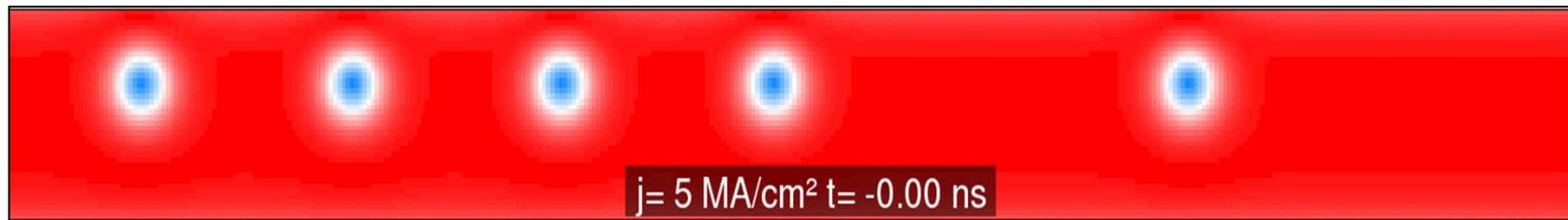


Skyrmion-like patterns can be found everywhere in world

问题：粒子还是波？  
答：具有粒子特性的一种磁化状态



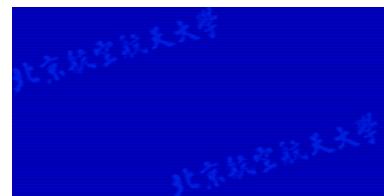
# 斯格明子 (Skyrmion)



Fert et al, Nature Nanotech.8, 152, 2013



斯格明子的粒子特性使  
它具有更高的可靠性，  
能够绕过杂质或者缺陷



# 斯格明子 (Skyrmion)

拓扑自旋电子学 = 自旋电子学 + 拓扑学

2007 年诺贝尔物理学奖：  
自旋电子学 (Spintronics)



2016 年诺贝尔物理学奖：  
拓扑学 (Topology)



Photo: U. Montan  
Albert Fert  
Prize share: 1/2

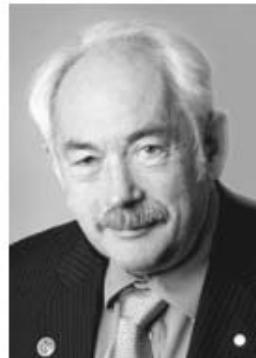


Photo: U. Montan  
Peter Grünberg  
Prize share: 1/2



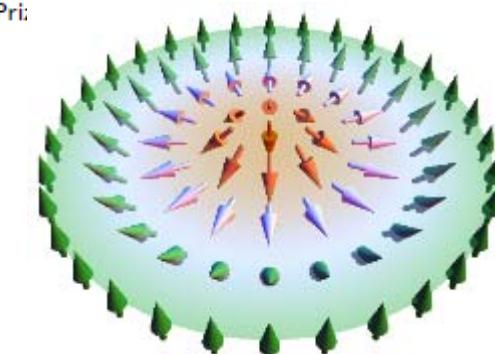
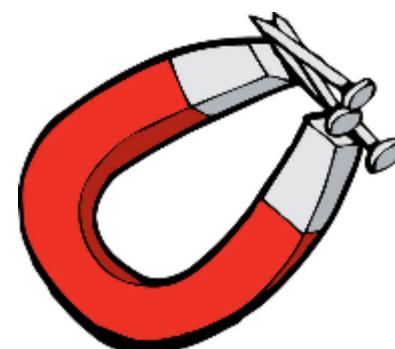
Photo: A. Mahmoud  
David J. Thouless  
Prize share: 1/2



Photo: A. Mahmoud  
F. Duncan M.  
Haldane  
Pr:



Photo: A. Mahmoud  
J. Michael Kosterlitz  
Pr:



# 斯格明子 vs 磁畴



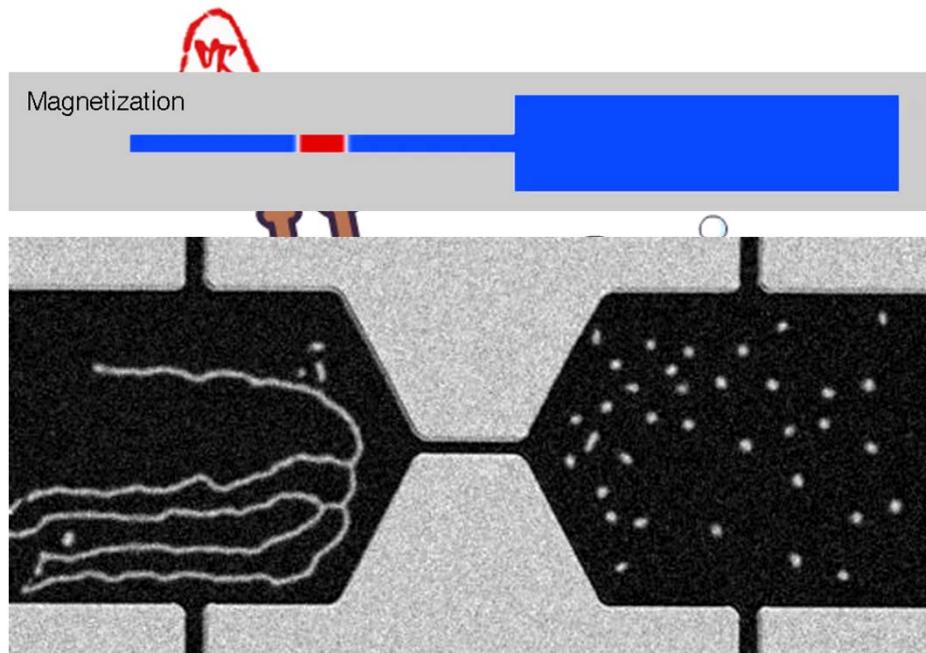
RESEARCH ARTICLE

MAGNETISM

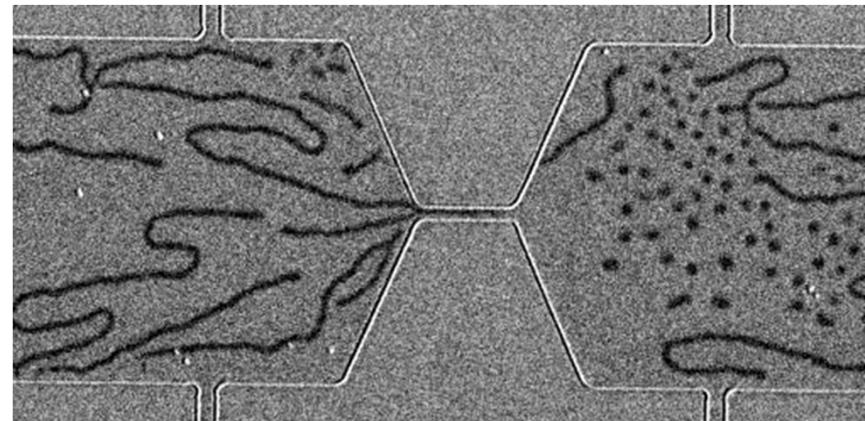
Science, 2005

## Blowing magnetic skyrmion bubbles

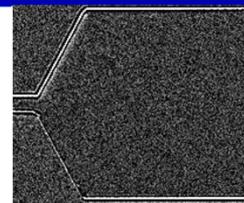
Wanjun Jiang,<sup>1</sup> Pramey Upadhyaya,<sup>2</sup> Wei Zhang,<sup>1</sup> Guoqiang Yu,<sup>2</sup>  
M. Benjamin Jungfleisch,<sup>1</sup> Frank Y. Fradin,<sup>1</sup> John E. Pearson,<sup>1</sup> Yaroslav Tserkovnyak,<sup>3</sup>  
Kang L. Wang,<sup>2</sup> Olle Heinonen,<sup>1,4,5,6</sup> Suzanne G. E. te Velthuis,<sup>1</sup> Axel Hoffmann<sup>1\*</sup>



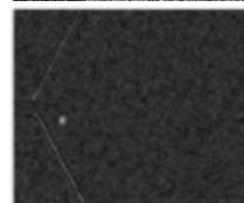
吹出来的斯格明子



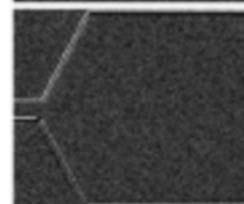
# 单个斯格明子的可控产生与驱动



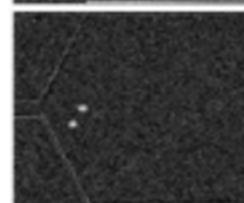
单个斯格明子



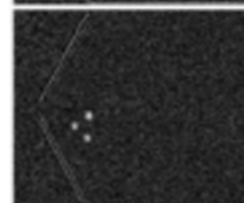
Correct



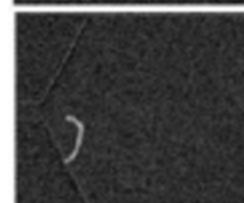
Error I



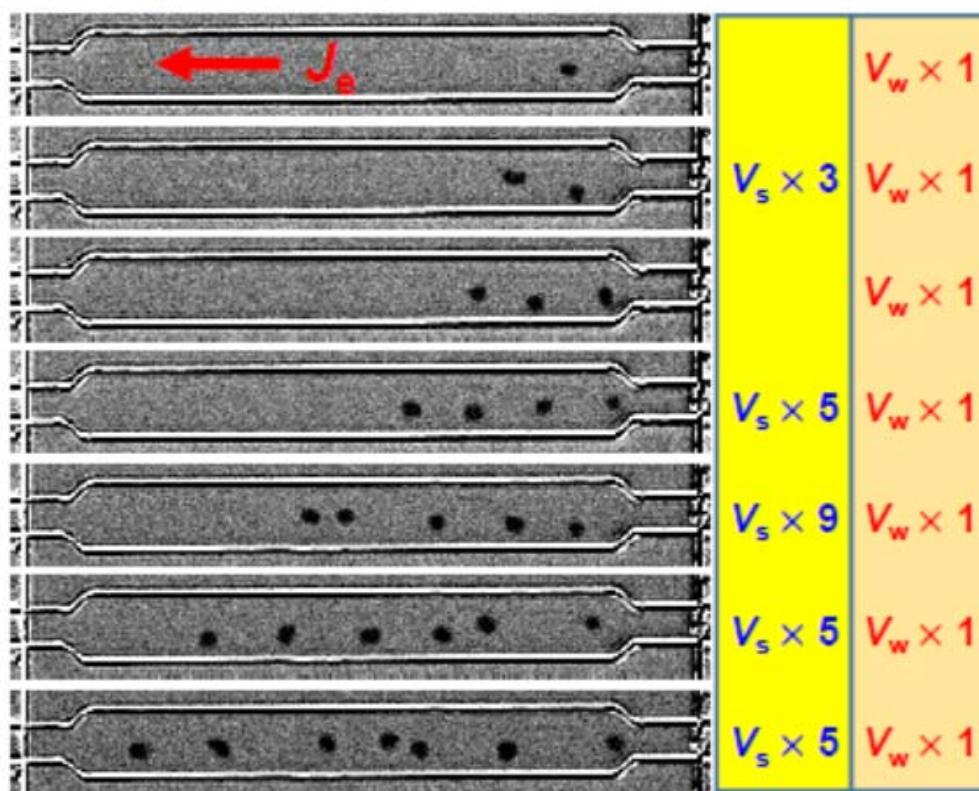
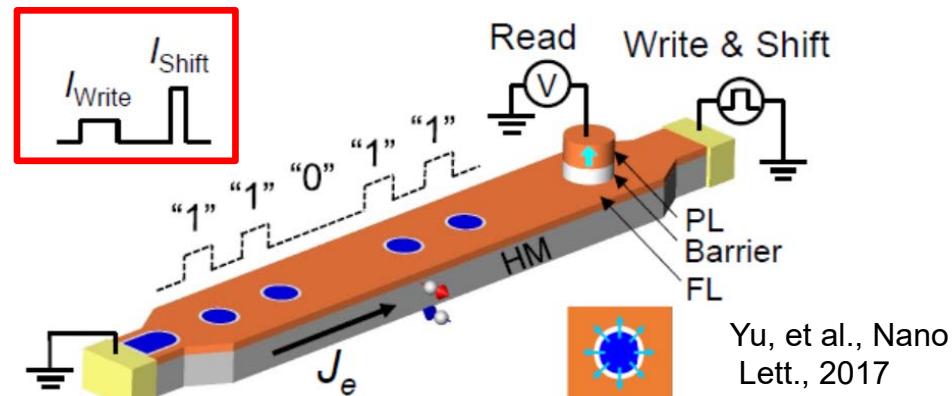
Error II



Error III



Error IV





# 斯格明子运动 VS 香蕉球





# 香蕉球



J罗 拜仁

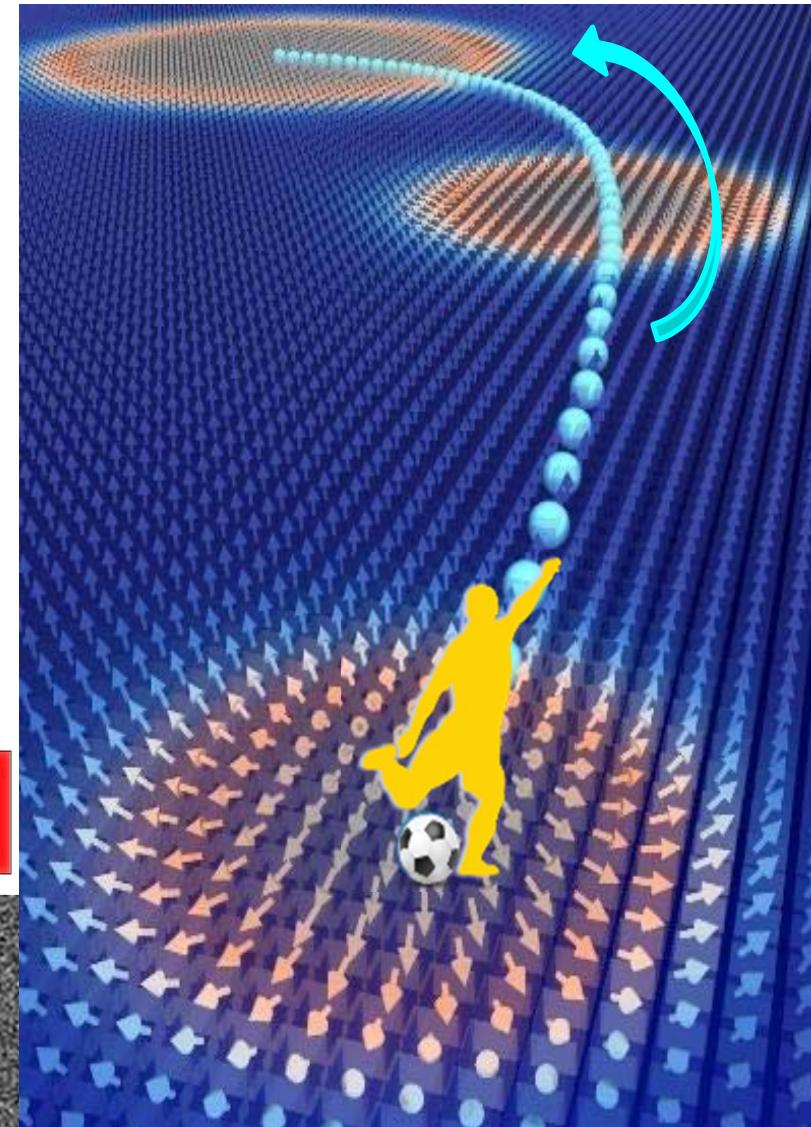
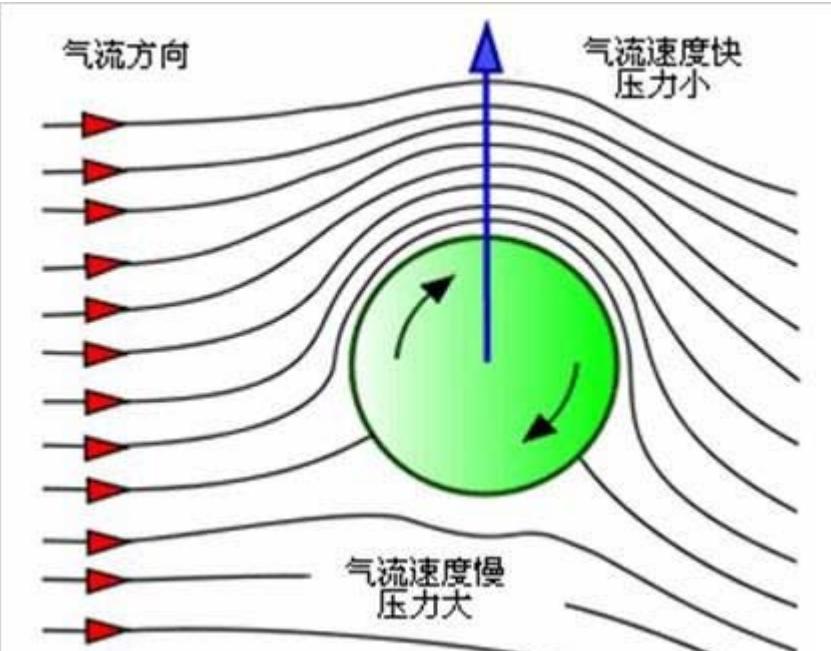


中国男孩 雷科巴 乌拉圭



巴西后卫卡洛斯

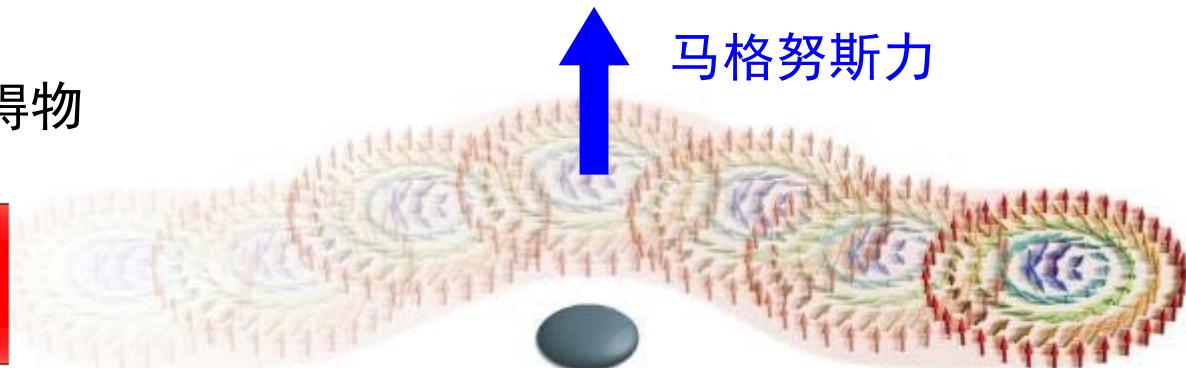
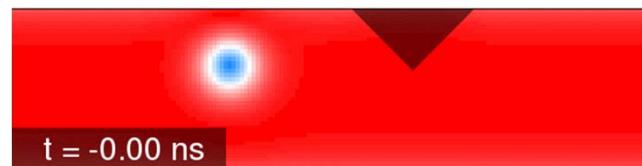
# 斯格明子的马格努斯效应



# 斯格明子的马格努斯效应

## 好处

使得斯格明子运动偏移障碍物



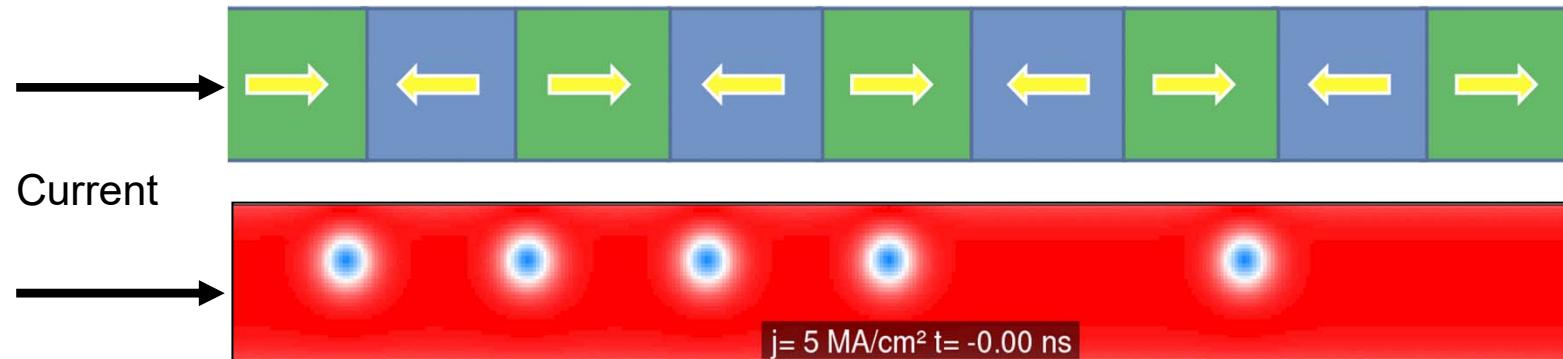
缺陷或者障碍

## 坏处

- 1、限制了斯格明子运动速度，和存储密度
- 2、可能导致斯格明子碰到边缘而产生湮灭



# 斯格明子赛道存储器 vs 磁畴赛道存储器



Fert et al, Nature Nanotech.8, 152, 2013

作为信息载体，磁畴必须首尾相连，而斯格明子是独立的个体  
我们可以更方便的对信息进行更新



# 课后思考

新型存储器相比传统存储器的优势与劣势？