数字电路基础　第七周作业

范云潜 18373486

微电子学院 184111 班

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作业内容：5.14，5.15，5.16，5.26

Problem 5.14

只需考虑上升沿的状态，由于这系列时间内 R'_D 为高，只考虑 D 。如 **图 1** 。

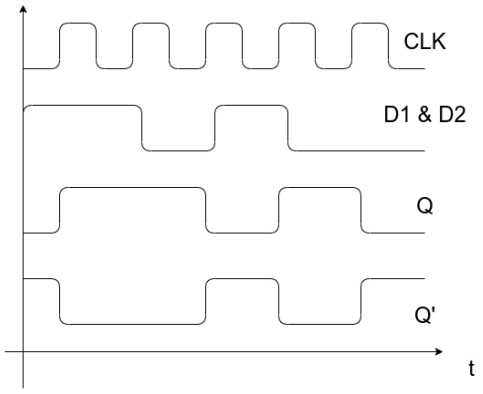

图 1

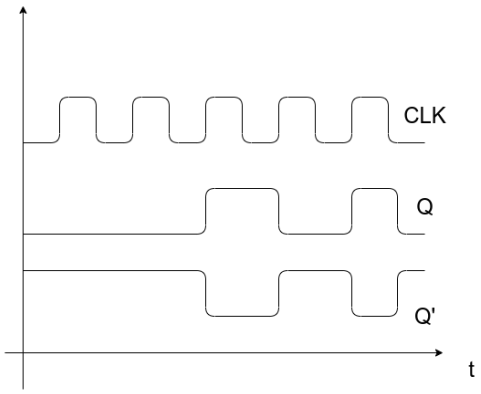

图 2

Problem 5.15

JK 触发器规则为 $Q^{n+1} = JQ^{n\prime} + K'Q^n$ ，那么在每个上升沿有：

$$init : Q = 0$$

$$clk0 : Q = 0 + 1\&0 = 0$$

$$clk1 : Q = 0 + 0 = 0$$

$$clk2 : Q = 1\&1 + x = 1$$

$$clk3 : Q = 0 + 0 = 0$$

$$clk4 : Q = 1$$

绘制如 **图 2**

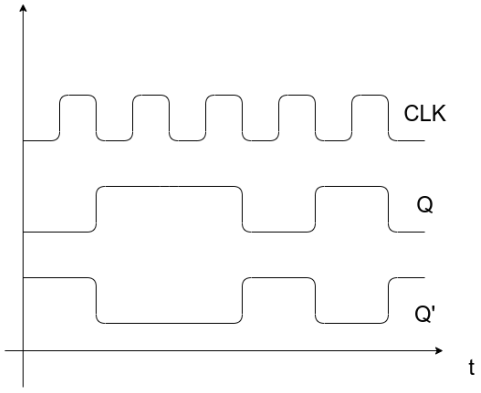

图 3

Problem 5.16

T 触发器观察下降沿采样即可。设初值 Q 为 0 。绘制如 **图 3**

Problem 5.26

JK 端子均接高，那么 $Q^{n+1} = JQ^{n\prime} + K'Q^n = Q^{n\prime}$ ，均接 Q_2 为 $Q_3^{n+1} = Q_2Q_3^{n\prime} + Q_2'Q_3^n = Q_2 \otimes Q_3^n$ 。但是需要注意到，实际上时钟有的来自之前信号的下降沿。

在每个 CLK 下降沿：

$init: Q_1 = 0, Q_2 = 0, Q_3 = 0$

$clk0: Q_1 = 1(Q_1' \downarrow), Q_2 = 1, Q_3 = 0$

$clk1: Q_1 = 0(Q_1 \downarrow), Q_2 = 1, Q_3 = 1$

$clk2: Q_1 = 1(Q_1' \downarrow), Q_2 = 0, Q_3 = 1$

$clk3: Q_1 = 0(Q_1 \downarrow), Q_2 = 0, Q_3 = 1$

$clk4: Q_1 = 1(Q_1' \downarrow), Q_2 = 1, Q_3 = 1$

$clk5: Q_1 = 0(Q_1 \downarrow), Q_2 = 1, Q_3 = 0$

$clk6: Q_1 = 1(Q_1' \downarrow), Q_2 = 0, Q_3 = 0$

$clk7: Q_1 = 0(Q_1 \downarrow), Q_2 = 0, Q_3 = 0$

Return to the init

绘制如 **图 4**

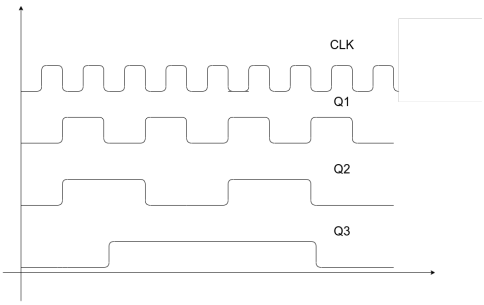

图 4