Papaya Pi Hardware Introduction

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Version	Author	Date	Change
1.0	Nikola Manolov	25/04/2019	Document created
1.1	Nikola Manolov Ivo Ivanov	23/05/2019	Added features table Added mechanical specifications Introduction changes.

Contents

1. Introduction

The Papaya Pi is an open source development kit for the Allwinner V3S SoC. All of the V3S interfaces are routed to connectors, headers and sockets for easy use and development.

The Allwinner V3s features a single ARM Cortex-A7 CPU that operates at speed up to 1.2GHz with integrated 512Mbit (64MB) of DDR2 RAM memory, with support for numerous peripherals. The processor targets the need of the growing Car Digital Video Record (DVR) and IP Camera (IPC) Monitor System.

For further information about the Allwinner V3S SoC, please refer to the Allwinner V3S Datasheet.

CPU	32 bit 1.2 Ghz Single-Core ARM Cortex A7
SDRAM	512Mbit (64MB) of integrated DDR2 RAM
Power Inputs	1x USB Micro 5V DC Power Only input. A minimum of 0.5A is requiered.
	1x 9 to 24V DC Barrel jack input.
	Power over Ethernet Capability
RTC	1x RTC battery connecter
GPIO	43 GPIOs on 3 GPIO Headers. Some of those can be used for peripherals souch as UART, I2C, SPI and other.
Networking	10/100Mbps Ethernet with PoE support
USB	1x USB A Port
Storage	1x SD Card Slot for Booting
	1x SD Card Slot for Data (Shares pins with GPIOs of PORT G)
Display	24-bit Parallel RGB Interface on a standard 40 pin FFC (Shares pins with GPIOs of PORT E)
Camera	MIPI-CSI2 interface compliant with MIPI-DPHY v1.0 and MIPI-CSI2 v1.0
	Supports 8 bit parallel camera. (Shares pins with GPIOs of PORT E)
Video Encoding	Please refer to the Allwinner V3S datahssed for the video encoding capabilities.
Audio Output	3.5mm Audio Jack
Audio Input	Optional Microphone Input.
	Mic. input integrated in to the 3.5mm Audio Jack (currently unsupported by the kernel)

Table 1 Papaya Pi Features
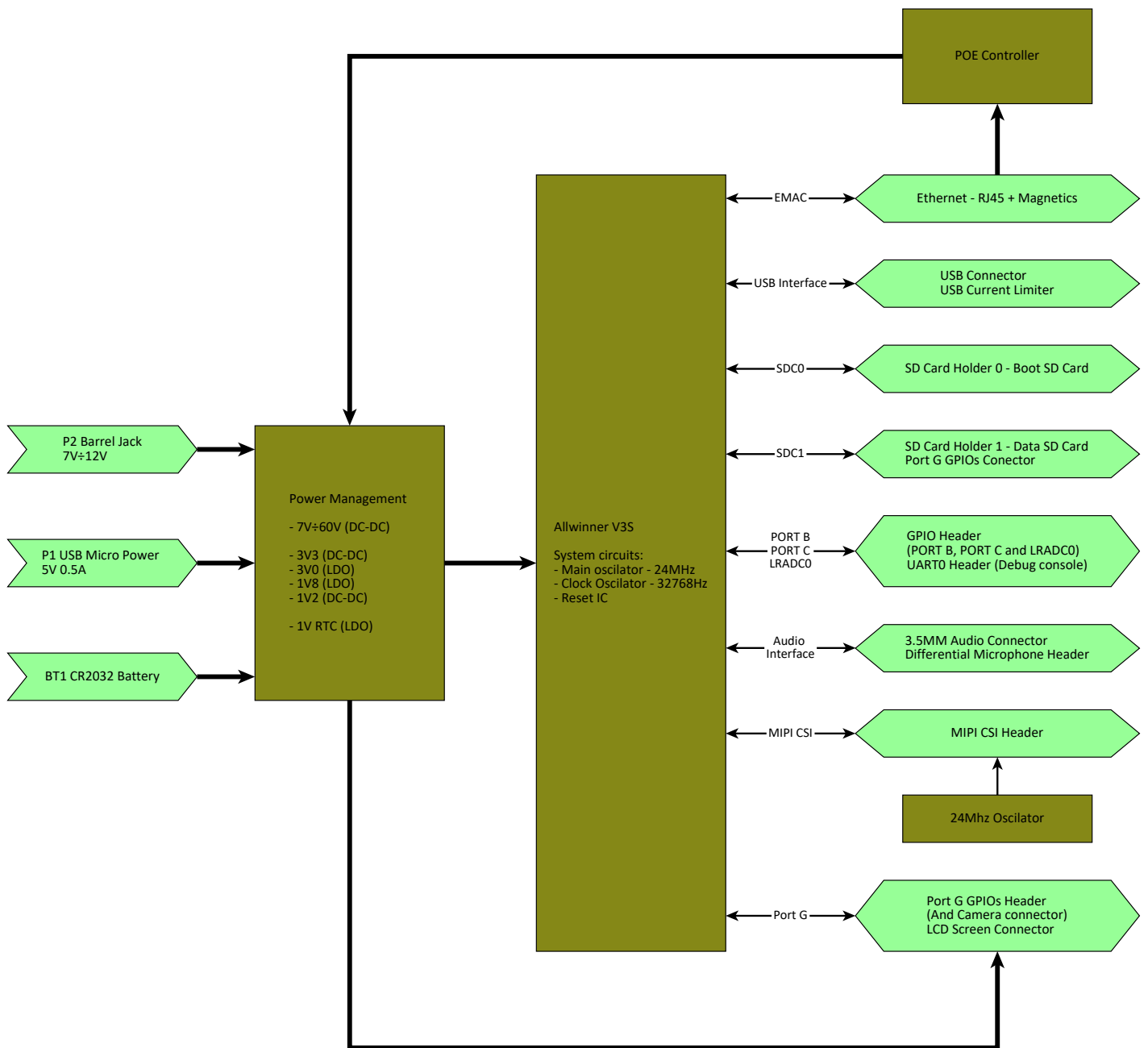
2. Block Diagram

Figure 1 Papaya Pi Block Diagram
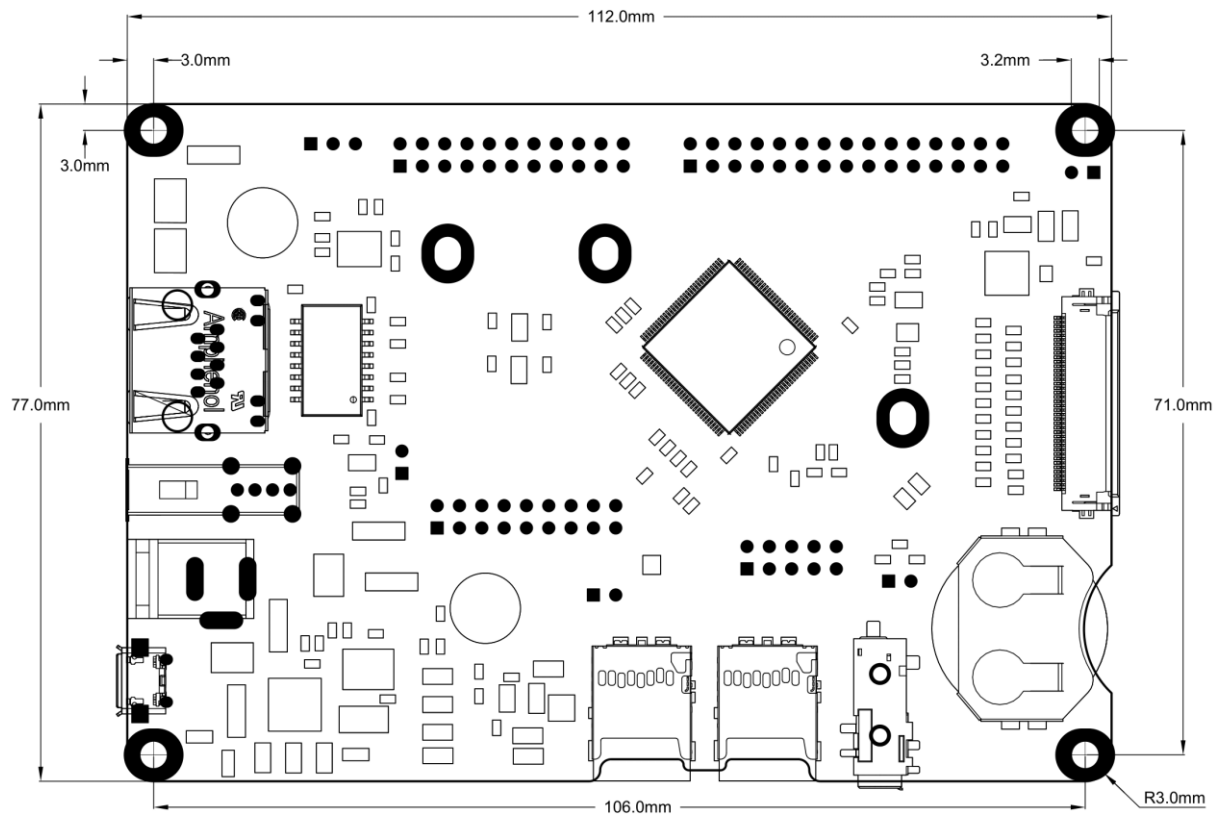
3. Mechanical Specifications

Figure 2 Mechanical Dimensions

PCB Thickness – 1.6mm

Recommended mounting screws – 3mm
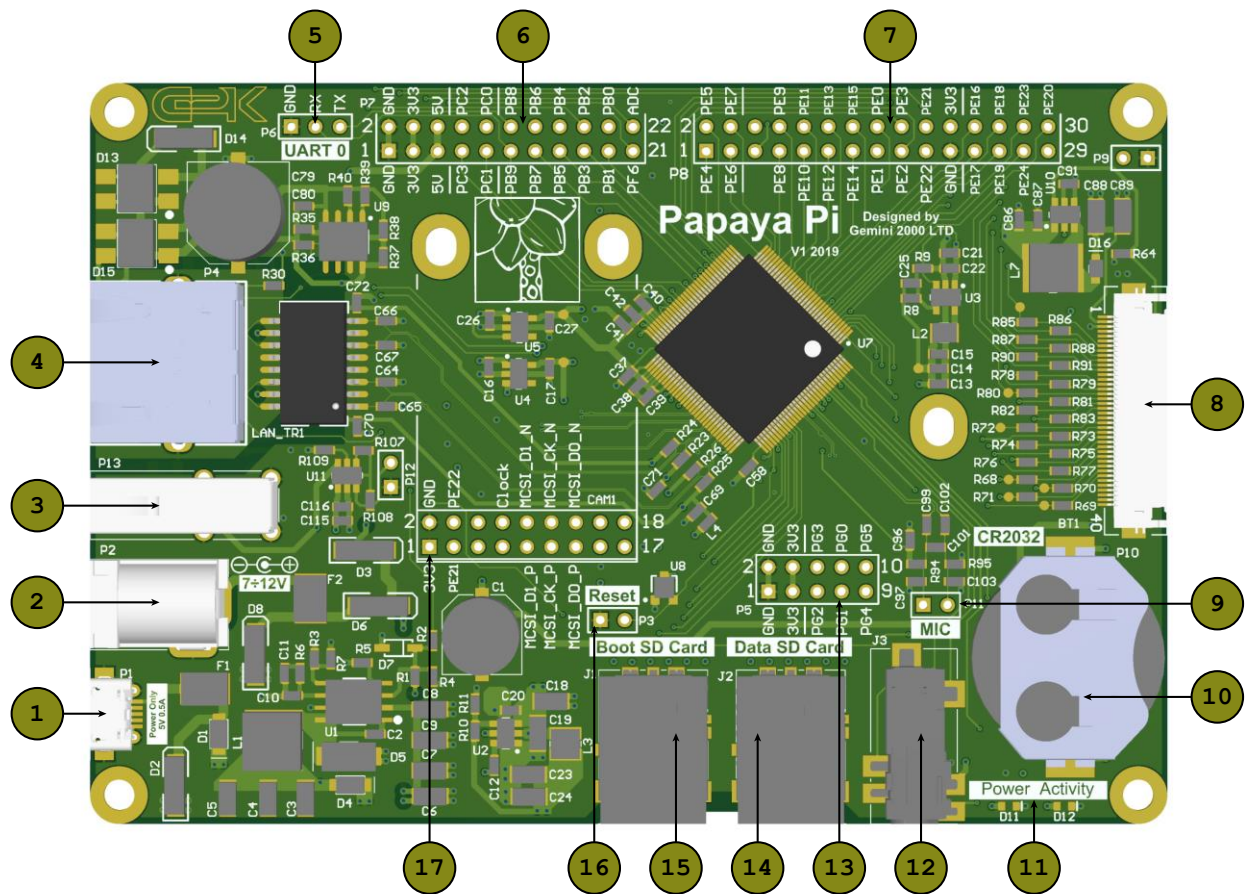
4. Papaya Pi Layout and Connectors

Figure 3 Connector Placement

1. USB Micro Jack (Power only - 5V, 0.5A)
2. Barrel Jack 9V to 24V
3. USB A - USB Host Connector
4. Ethernet Connector with PoE
5. P6 - UART0 Header (By default it is the debug console)
6. P7 - GPIO Header for Port B and Port C
7. P8 - GPIO Header for Port E (also used for OV5640 camera module)
8. Parallel LCD Connector
9. Battery Connector for CR2032 Battery
10. Activity and Power LEDs
11. Differential Microphone Header
12. 3.5mm Connector for audio
13. P6 - GPIO Header for Port G (Shared with Data SD Card)
14. Data SD Card (SDC 1 - SD Card 1)
15. Boot SD Card (SDC 0 - SD Card 0)
16. Reset Header
17. MIPI CSI Connector - For OV5640 camera module. MIPI CSI is currently not supported by the kernel

4.1. Papaya Pi Header Pinouts

4.1.1. P6 - UART0 Header Pinout.

This header is designed to provide easy access to UART0, without needing to change the cabling on P7.

Pin	Name	Alternative Functions	Notes
1	GND		
2	PB9	TWI1_SDA/UART0_RX/PB_EINT9	By default - debuging UART0.
3	PB8	TWI1_SCK/UART0_TX/PB_EINT8	

Table 2 P6 Pinout

4.1.2. P5 - GPIO Header for Port G (Shared with Data SD Card)

Pin	Name	Alternative Functions	Notes
1	GND		
2	GND		
3	3V3		
4	3V3		
5	PG2	SDC1_D0/PG_EINT2	By default used for SD Card 1 (SDC1)
6	PG3	SDC1_D1/PG_EINT3	
7	PG1	SDC1_CMD/PG_EINT1	
8	PG0	SDC1_CLK/PG_EINT0	
9	PG4	SDC1_D2/PG_EINT4	
10	PG5	SDC1_D3/PG_EINT5	

Table 3 P5 Pinout

4.1.3. P7 - GPIO Header for Port B and Port C Pinout

Pin	Name	Alternative Functions	Notes
1	GND		
2	GND		
3	5V		
4	5V		
5	3V3		
6	3V3		
7	PC3	SDC2_D0/SPI0_MOSI	
8	PC2	SDC2_RST/SPI0_CS	
9	PC1	SDC2_CMD/SPI0_CLK	
10	PC0	SDC2_CLK/SPI0_MISO	
11	PB9	TWI1_SDA/UART0_RX/PB_EINT9	By default - debuging UART0.
12	PB8	TWI1_SCK/UART0_TX/PB_EINT8	
13	PB7	TWI0_SDA/PB_EINT7	
14	PB6	TWI0_SCK/PB_EINT6	
15	PB5	PWM1/PB_EINT5	
16	PB4	PWM0/PB_EINT4	
17	PB3	UART2_CTS//PB_EINT3	
18	PB2	UART2_RTS/PB_EINT2	By default used for activity LED.
19	PB1	UART2_RX/PB_EINT1	
20	PB0	UART2_TX/PB_EINT0	
21	PF6		By default - USB ID Pin for OTG.
22	LRADC0		

Table 4 P7 Pinout

4.1.4. P8 - GPIO Header for Port E (also used for OV5640 camera module)

Pin	Name	Alternative Functions	Notes
1	PE4	CSI_D0/LCD_D2	
2	PE5	CSI_D1/LCD_D3	
3	PE6	CSI_D2/LCD_D4	
4	PE7	CSI_D3/LCD_D5	
5	Reset for OV5640 camera module (not fitted)		OV5640 Can be mounted here (in parallel mode)
6	Power Down OV5640 camera module (not fitted)		
7	PE8	CSI_D4/LCD_D6	
8	PE9	CSI_D5/LCD_D7	
9	PE10	CSI_D6/LCD_D10	
10	PE11	CSI_D7/LCD_D11	
11	PE12	CSI_D8/LCD_D12	
12	PE13	CSI_D9/LCD_D13	
13	PE14	CSI_D10/LCD_D14	
14	PE15	CSI_D11/LCD_D15	
15	PE1	CSI_MCLK/LCD_DE	
16	PE0	CSI_PCLK/LCD_CLK	
17	PE2	CSI_HSYNC/LCD_HSYNC	
18	PE3	CSI_VSYNC/LCD_VSYNC	
19	PE22	CSI_SDA/TWI1_SDA/UART1_RX	
20	PE21	CSI_SCK/TWI1_SCK/UART1_TX	
21	GND		
22	3V3		
23	PE17	CSI_D13/LCD_D19	
24	PE16	CSI_D12/LCD_D18	
25	PE19	CSI_D15/LCD_D21	
26	PE18	CSI_D14/LCD_D20	
27	PE24	LCD_D23/UART1_CTS	
28	PE23	LCD_D22/UART1_RTS	
29	Empty		
30	PE20	CSI_FIELD/CSI_MIPI_M CLK	

Table 5 P8 Pinout

5. Powering the Papaya Pi

The Papaya Pi can be powered from:
1. USB Micro Jack (power only - 5V/1A)
2. Barrel Jack 9V to 24V
3. Power over Ethernet (PoE)

It's not recommended to use more than one power source at a time. Using more than one power source at a time will not damage the Papaya Pi.

Battery for RTC:

In order to power the RTC of the V3S, a battery connector for a CR2032 battery is provided on the Papaya PI. The RTC battery is optional and not needed for the normal operation of the device.

6. Booting the Papaya Pi

The Allwinner V3S SoC can boot from SDC0 (SD Card 0) by default. The boot SD Card is located on (15) on the Papaya Pi. For more information about the booting process and the OS for the V3S, please refer to the Allwinner V3S Datasheet and to the README file in the software folder of the Papaya Pi Github.