

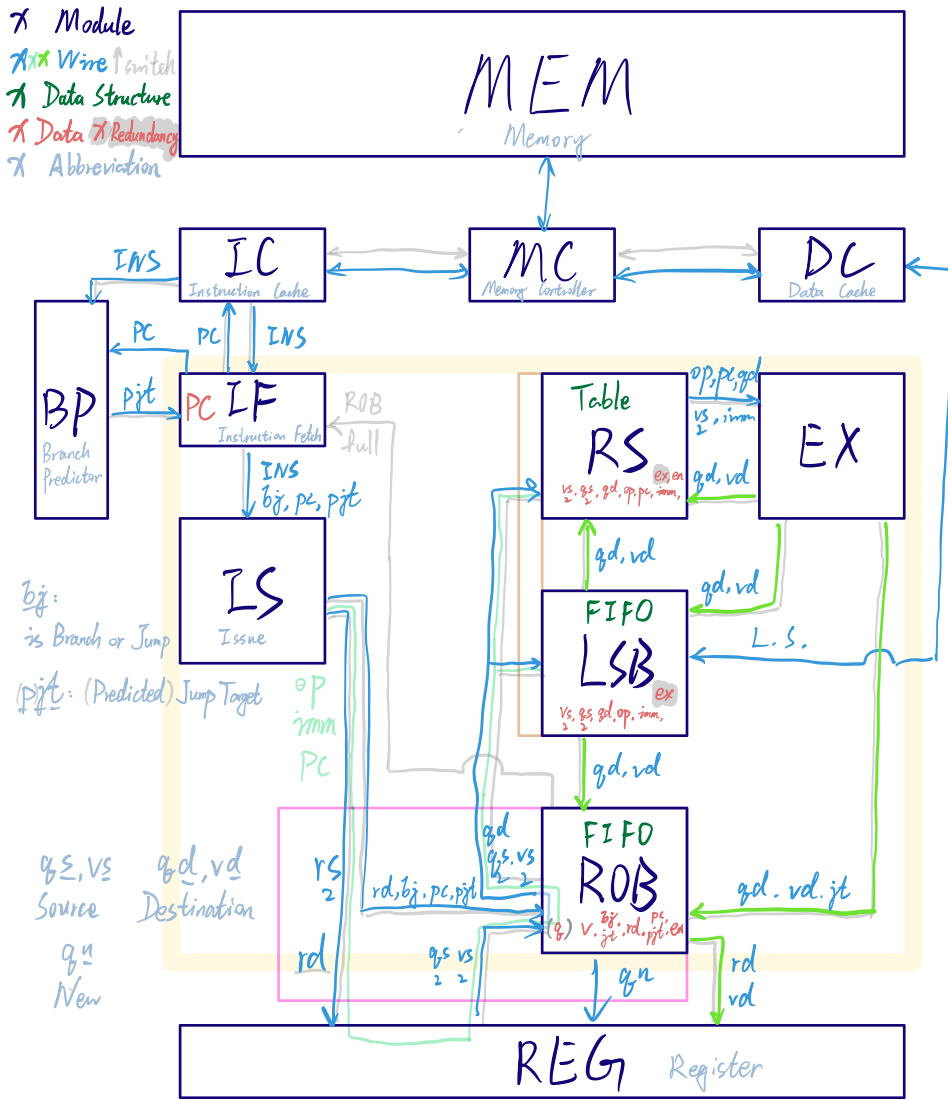
Module

Wire

Data Structure

Data Redundancy

Abbreviation



RS: Reserve Station

ROB: Reordered Buffer

LSB: Load-Store Buffer

EX: Execution

PC from ROB
RS & LSB input:
op, imm, vs, rs, qd

LSB & EX output:
qd, vd
jt to ROB, RS, LSB

bj: is Branch or Jump

pjt: (Predicted) Jump Target

qs, vs
Source
qn
New

IS. vs & rd → REG

REG[rd].q = qn

REG[rs].vs & qs

ROB[qn].PC & rd ← IS.pc & rd

ROB.qs = REG.qs

ROB.vs = (ROB[qs].en) ? (ROB[qs].v) : (REG.vs)

LSB为依次执行

ROB为依次 Commit

ROB为 Branch/Jump指令精确中断:

1. Store指令完成后对应 entry in ROB 才能 Commit

2. 预测失败则清空

IF, IS, ROB, RS, EX, LSB