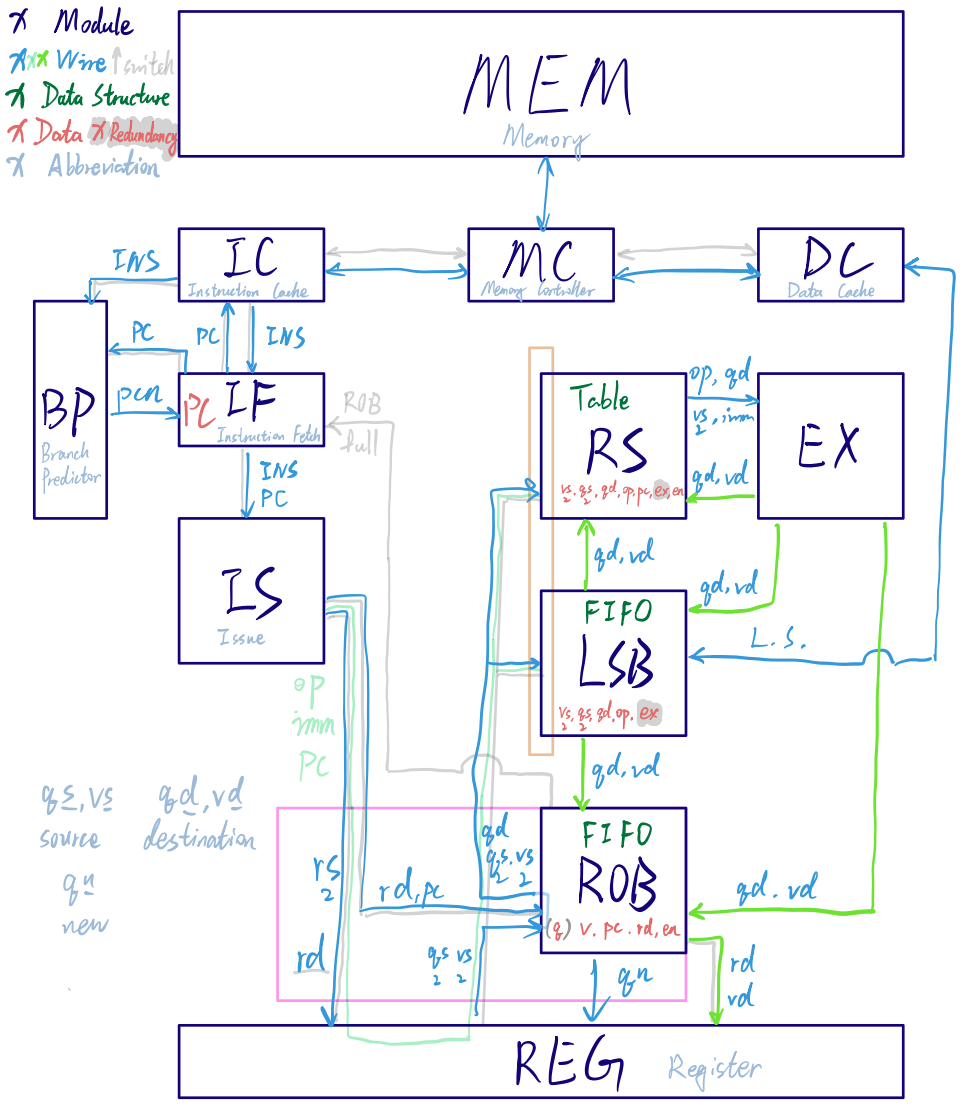

R.S. Reserve Station
ROB: Reordered Buffer
LSB: Load-Store Buffer
EX: EXecution

RS & LSB input:
op, imm, v_s, q_s, qd
output: qd, vd

IS. r_s & rd → REG
REG[rd].q = qn
REG[r_s].v_s & q_s
ROB[qn].PC&rd ← IS.pc & rd
ROB.q_s = REG.q_s
ROB.v_s = (ROB[q_s].en)?(ROB[q_s].v):(REG.v_s)