Legend:
- Module
- Wire / switch
- Data Structure
- Data / Redundancy
- Abbreviation
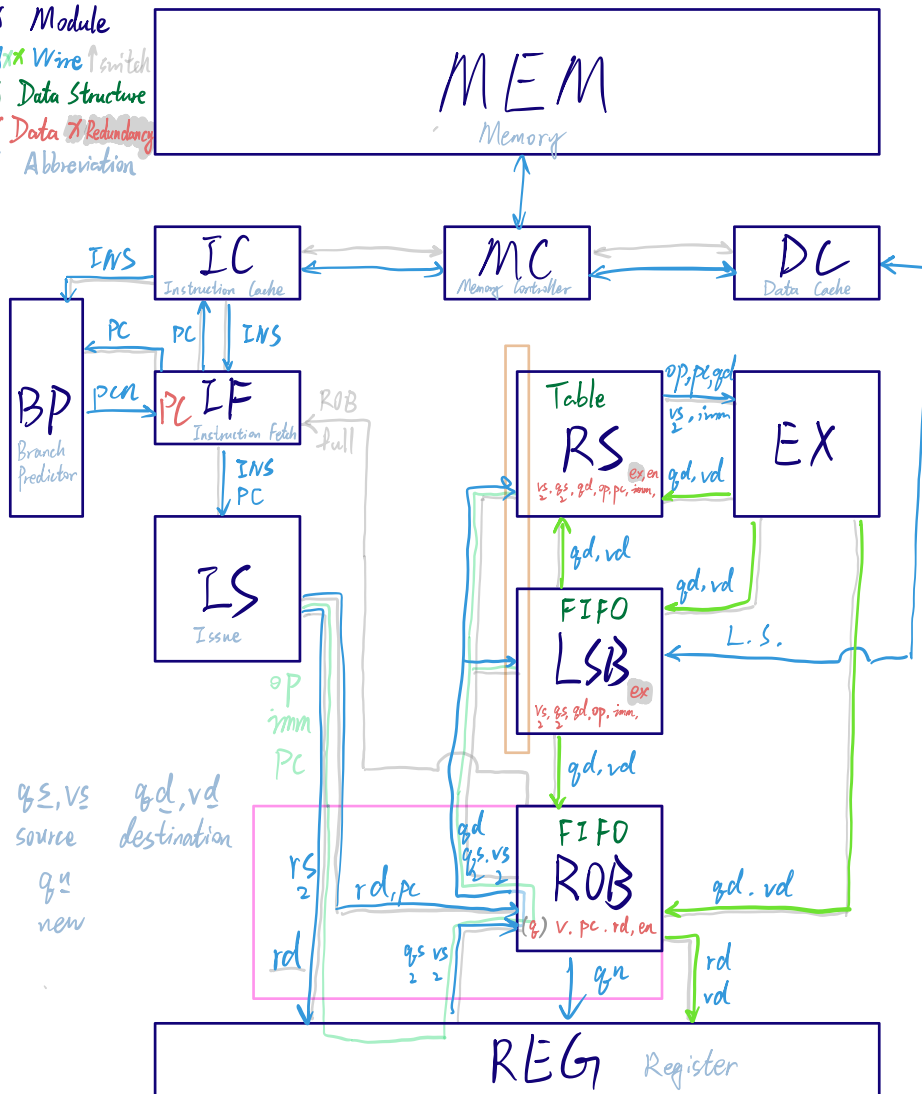
MEM — Memory

IC — Instruction Cache
MC — Memory Controller
DC — Data Cache

BP — Branch Predictor
LF — Instruction Fetch
IS — Issue

Table — RS
$v_s, q_s, q_d, op, pc, imm,$ ex, en
EX
op, pc, q_d
v_s, imm
q_d, v_d

FIFO — LSB
$v_s, q_s, q_d, op, imm,$ ex

FIFO — ROB
$(q)\, v, pc, rd, en$

REG — Register

q_s, v_s source
q_d, v_d destination
q_n new

RS & LSB input:
op, imm, v_s, q_s, q_d
output: q_d, v_d

q_d, v_d

$op\ imm\ PC$

rs
rd, pc
rd
$q_s\ v_s$
q_d
q_s, v_s
q_n
rd
v_d

L.S.

IS. rs & $rd \rightarrow$ REG

REG$[rd].q = q_n$

REG$[rs].v_s$ & q_s

ROB$[q_n].pc$ & $rd \leftarrow$ IS. pc & rd

ROB.q_s = REG.q_s

ROB.v_s = (ROB$[q_s].en$) ? (ROB$[q_s].v$) : (REG.v_s)