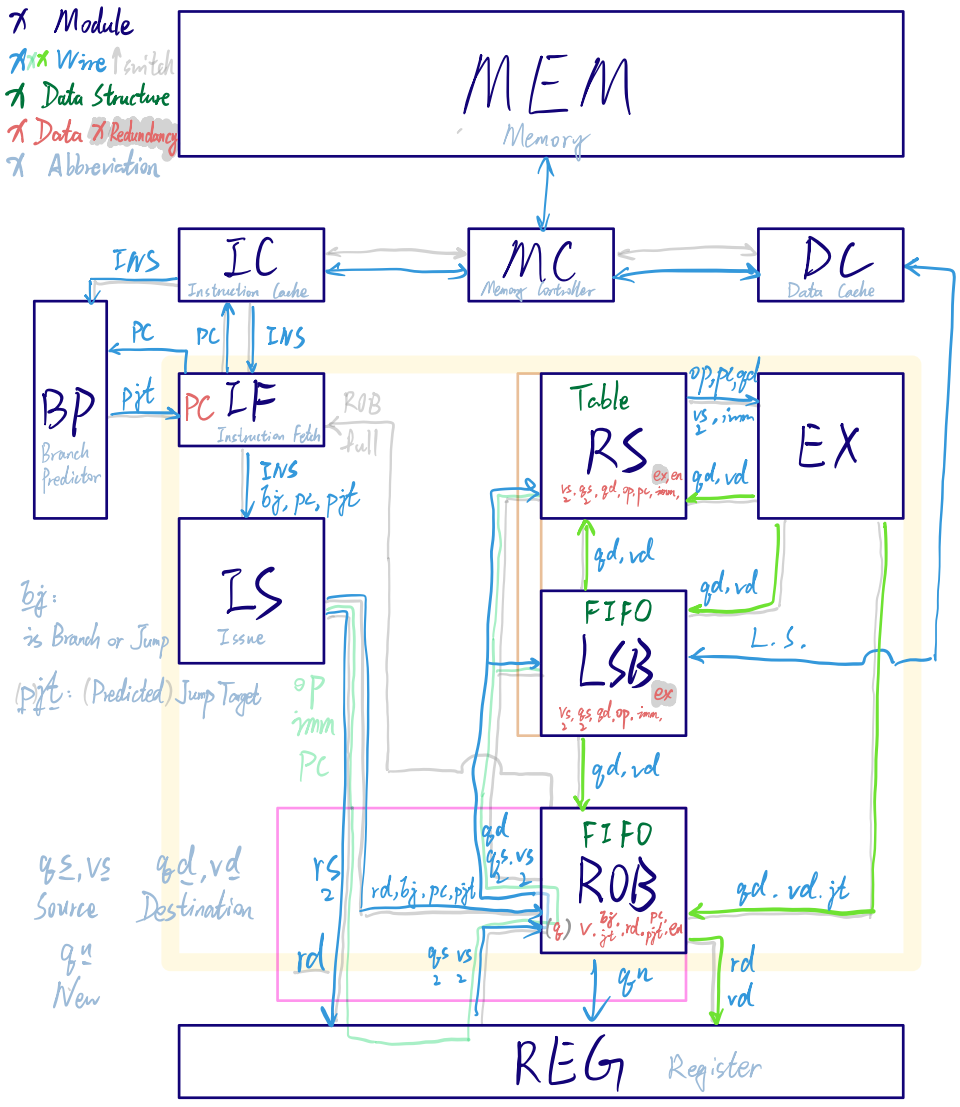

R.S.: Reserve Station
ROB: Reordered Buffer
LSB: Load-Store Buffer
EX: EXecution

from ROB
PC
RS & LSB input:
op, imm, vs, qs, qd

LSB & EX output:
qd, vd
jt
to ROB, RS, LSB

IS. vs & rd → REG
REG[rd].q = qn
REG[rs].vs & qs
ROB[qn].pc & rd ← IS.pc & rd
ROB.qs = REG.qs
ROB.vs = (ROB[qs].en)? (ROB[qs].v) : (REG.vs)

LSB内依次执行
ROB内依次Commit
ROB为Branch/Jump指令精确中断:
1. Store指令完成后对应entry in ROB才能Commit
2. 预测失败则清空
IF, IS, ROB, RS, EX, LSB