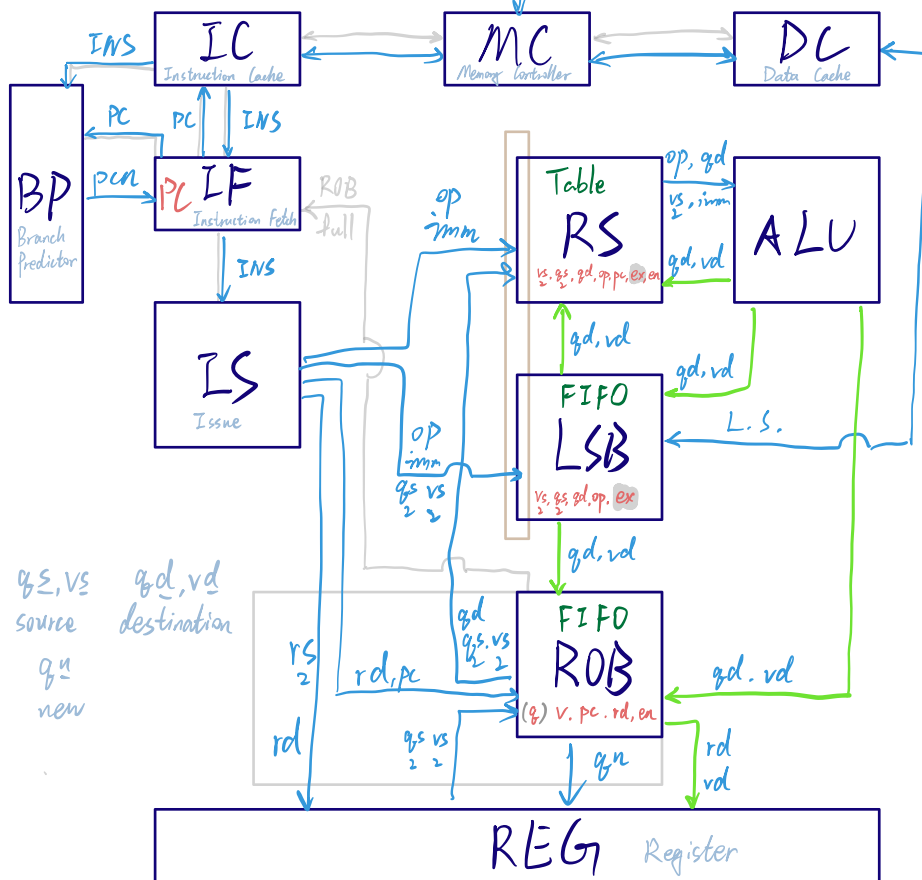


- Module
- Wire
- Data Structure
- Data Redundancy
- Abbreviation

RS: Reserve Station  
ROB: Reordered Buffer  
LSB: Load-Store Buffer  
ALU: Arithmetic Logic Unit



RS & LSB input:  
op, imm,  $vs_2$ ,  $qs_2$ , qd  
output: qd, vd

IS.  $vs_2$  & rd  $\rightarrow$  REG

REG[rd].q =  $qn$

REG[ $rs_2$ ]. $vs_2$  &  $qs_2$

ROB[ $qn$ ].PC & rd  $\leftarrow$  IS.pc & rd

ROB. $qs_2$  = REG. $qs_2$

ROB. $vs_2$  = (ROB[ $qs_2$ ].en) ? (ROB[ $qs_2$ ].v) : (REG. $vs_2$ )