

Module

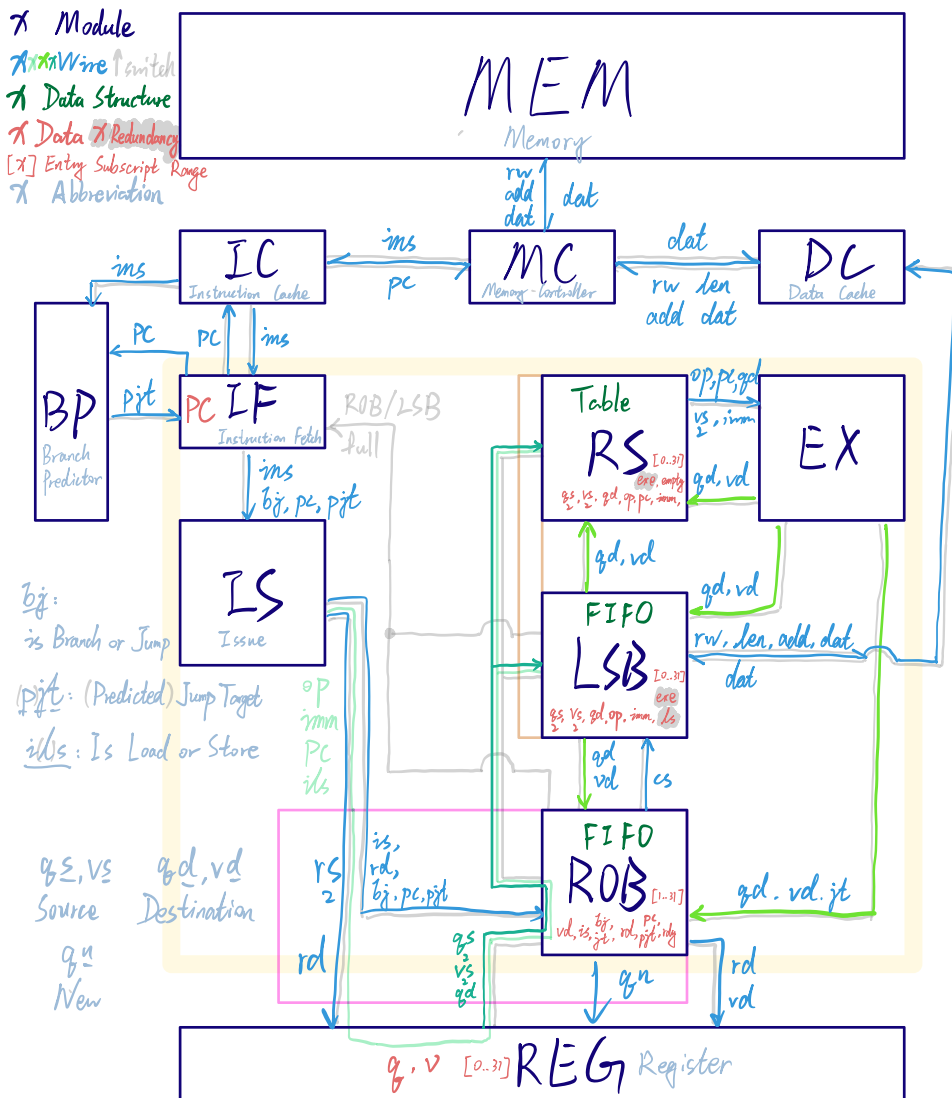
Wire

Data Structure

Data Redundancy

Entry Subscript Range

Abbreviation



bj : is Branch or Jump
 pjt : (Predicted) Jump Target
 ils : Is Load or Store
 gs, vs : Source
 gd, vd : Destination
 gn : New

RS: Reserve Station
 ROB: Reordered Buffer
 LSB: Load-Store Buffer
 EX: Execution

PC from ROB
 RS & LSB input:
 op, imm, vs, gs, gd
 LSB & EX output:
 gd, vd
 to ROB, RS, LSB

RS: exe: EXEcutible
 LSB: ls : Load or Store
 ROB: rdy : READY to be committed
 rw : Read or Write
 LSB: len : LENGTH
 DC: add : ADDRESS
 dat : DATA
 ROB: cs : Commit Store
 LSB

$IS. vs \& rd \rightarrow REG$
 $REG[rd].g = gn$
 $REG[rs].vs \& gs$
 $ROB[gn].PC \& rd \leftarrow IS.pc \& rd$
 $ROB.gs = REG.gs$
 $ROB.vs = (ROB[gs].en) ? (ROB[gs].v) : (REG.vs)$

LSB 内依次执行
 ROB 内依次 Commit
 ROB 为 Branch/Jump 指令精确中断:
 1. Store 指令完成后对应 entry in ROB 才能 Commit
 2. 预测失败则清空
 IF, IS, ROB, RS, EX, LSB
 以及 REG 中的 Q
 保留前缀
 Committed STORE