# OPENCL调试与性能优化

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#### **Outline**

- OpenCL调试
  - CPU调试
  - GPU调试
- OpenCL性能优化
  - 线程映射
  - 设备占用
  - 向量化
- · N-body仿真实例

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### OpenCL调试技术

- Compiling for x86 CPU
  - Debugging with GDB
- GPU printf
- Live debuggers
  - gDEBugger

### CPU端程序调试

- OpenCL allows the same code to run on different types of devices
  - Compiling to run on a CPU provides some extra facilities for debugging
  - Additional forms of IO (such as writing to disk) are still not available from the kernel
- AMD's OpenCL implementation recognizes any x86 processor as a target device
  - Simply select the CPU as the target device when executing the program
- NVIDIA's OpenCL implementation can support compiling to x86 CPUs if AMD's installable client driver is installed

#### CPU端程序调试——GDB

- Setting up for GDB
  - Pass the compiler the "-g" flag
    - Pass "-g" to clBuildProgram()
    - Set an environment variable CPU\_COMPILER\_OPTIONS="-g"
  - Avoid non-deterministic execution by setting an environment variable CPU MAX COMPUTE UNITS=1

#### CPU端程序调试——GDB

Run gdb with the OpenCL executable

```
> gdb a.out
```

- Breakpoints can be set by line number, function name, or kernel name
- To break at the kernel hello within gdb, enter:

```
(gdb) b __OpenCL_hello_kernel
```

- The prefix and suffix are required for kernel names
- OpenCL kernel symbols are not known until the kernel is loaded, so setting a breakpoint at

```
clEnqueueNDRangeKernel() is helpful
```

```
(gdb) b clEnqueueNDRangeKernel
```

#### CPU端程序调试——GDB

- To break on a certain thread, introduce a conditional statement in the kernel and set the breakpoint inside the conditional body
  - Can use gdb commands to view thread state at this point

```
if(get_global_id(1) == 20 &&
  get_global_id(0) == 34) {
  ; // Set breakpoint on this line
}
```

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#### GPU程序调试——GPU Printf

- AMD GPUs support printing during execution using printf()
  - NVIDIA does not currently support printing for OpenCL kernels (though they do with CUDA/C)
- AMD requires the OpenCL extension cl\_amd\_printf to be enabled in the kernel
- printf() closely matches the definition found in the C99 standard

#### GPU程序调试—— GPU Printf

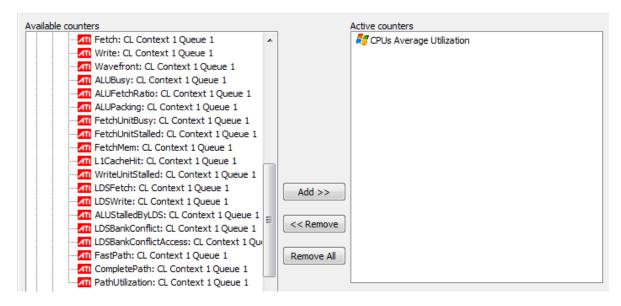
- printf() can be used to print information about threads or check help track down bugs
- The following example prints information about threads trying to perform an improper memory access

```
int myIdx = ... // index for addressing a matrix
if(myIdx < 0 || myIdx >= rows || myIdx >= cols) {
    printf("Thread %d,%d: bad index (%d)\n",
        get_global_id(1), get_global_id(0), myIdx));
}
```

#### GPU程序调试—— GPU Printf

- printf() works by buffering output until the end of execution and transferring the output back to the host
  - It is important that a kernel completes in order to retrieve printed information
  - Commenting out code following printf() is a good technique if the kernel is crashing

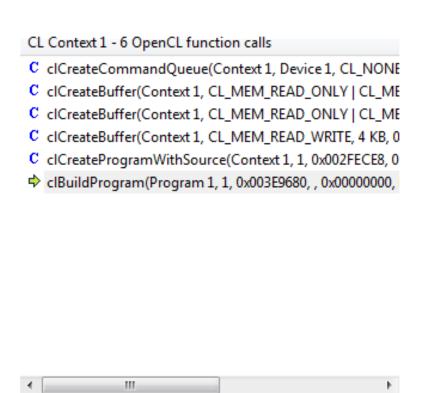
- Developed by Graphic Remedy
  - Cost: not free
- Debugger, profiler, memory analyzer
- Integrated with AMD/ATI and NVIDIA performance counters



 Displays information about OpenCL platforms and devices present in the system

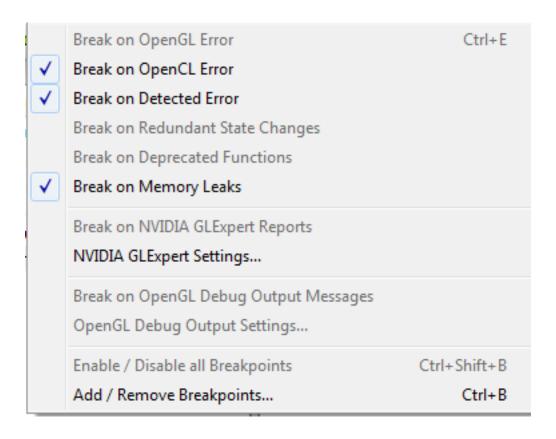
ystem Display OpenGL Rende	erer OpenGL Pixel Formats OpenGL Ex	xtensions OpenCL Platforms OpenCL Devices	
Parameter	Device 1 (CPU)	Device 2 (GPU)	,
Platform ID	1	1	
Device Type	CPU	GPU	
Device Name	Intel(R) Core(TM) i7 CPU 920	Cypress	ı
/endor	GenuineIntel	Advanced Micro Devices, Inc.	ı
Command Queue Properties	Queue profiling	Queue profiling	
Address Bits	32	32	
s Available	Yes	Yes	
s Compiler Available	Yes	Yes	
Single FP Config	Denorms, INF and NaNs, Round to	INF and NaNs, Round to nearest, Round to zero, Round to +ve and	
Double FP Config	Unknown / unsupported	Unknown / unsupported	
Half FP Config	Unknown / unsupported	Unknown / unsupported	
s Little Endian	Yes	Yes	
Error Correction Support	No	No	
Execution Capabilities	Kernel Execution, Native Kernel Exe	Kernel Execution	
Global Memory Cache Size	32 KB	0 bytes	
Memory Cache Type	Read Write	None	
Global Memory Cache Line Size	64 bytes	0 bytes	
Global Memory Size	1,024 MB	512 MB	
Arg Impage Cupperted	Ma III	Von	

- Can step through OpenCL calls, and view arguments
  - Links to programs, kernels, etc. when possible in the function call view

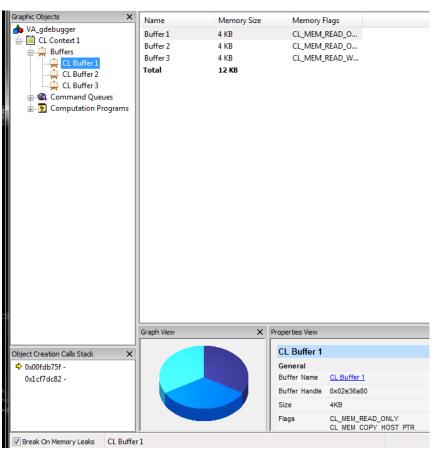




Automatically detects OpenCL errors and memory leaks



- Displays contents of buffers and images present on OpenCL devices
  - View live
  - Export to disk



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- Thread mapping determines which threads will access which data
  - Proper mappings can align with hardware and provide large performance benefits
  - Improper mappings can be disastrous to performance

- By using different mappings, the same thread can be assigned to access different data elements
  - The examples below show three different possible mappings of threads to data (assuming the thread id is used to access an

11

15

element)

```
int tid =
                                         int tid =
  Mapping
              get global id(1) *
                                         get global id(0) *
                                         get global size(1) +
              get global size(0) +
                                         get global id(1);
              get global id(0);
                                                       12
Thread IDs
                        6
                                                      13
                8
                        10
                                                  10
                                                      14
                            11
```

13

14

int group size = get local size(0) \* get local size(1); int tid = get group id(1) \* get num groups(0) \* group size + get group id(0) \* group size + get local id(1) \* get local size(0) + get local id(0) 3 7 6 13 15

\*assuming 2x2 groups

Consider a serial matrix multiplication algorithm

```
for(i1=0; i1 < M; i1++)
  for(i2=0; i2 < N; i2++)
    for(i3=0; i3 < P; i3++)
        C[i1][i2] += A[i1][i3]*B[i3][i2];</pre>
```

- This algorithm is suited for output data decomposition
  - We will create NM threads
    - Effectively removing the outer two loops
  - Each thread will perform P calculations
    - The inner loop will remain as part of the kernel
- Should the index space be MxN or NxM?

 Thread mapping 1: with an MxN index space, the kernel would be:

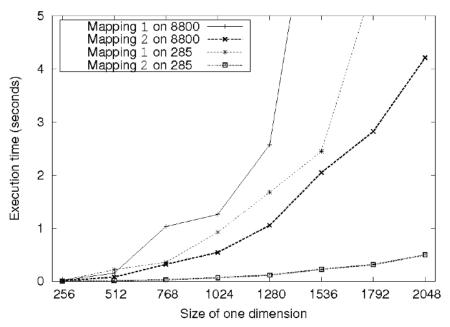
```
int tx = get_global_id(0);
int ty = get_global_id(1);
for(i3=0; i3<P; i3++)
    C[tx][ty] += A[tx][i3]*B[i3][ty];</pre>
```

 Thread mapping 2: with an NxM index space, the kernel would be:

```
int tx = get_global_id (0);
int ty = get_global_id (1);
for(i3=0; i3<P; i3++)
    C[ty][tx] += A[ty][i3]*B[i3][tx];</pre>
```

 Both mappings produce functionally equivalent versions of the program

 This figure shows the execution of the two thread mappings on NVIDIA GeForce 285 and 8800 GPUs



 Notice that mapping 2 is far superior in performance for both GPUs

- The discrepancy in execution times between the mappings is due to data accesses on the global memory bus
  - Assuming row-major data, data in a row (i.e., elements in adjacent columns) are stored sequentially in memory
  - To ensure coalesced accesses, consecutive threads in the same wavefront should be mapped to columns (the second dimension) of the matrices
    - This will give coalesced accesses in Matrices B and C
    - For Matrix A, the iterator i3 determines the access pattern for row-major data, so thread mapping does not affect it

- In mapping 1, consecutive threads (tx) are mapped to different rows of Matrix C, and non-consecutive threads (ty) are mapped to columns of Matrix B
  - The mapping causes inefficient memory accesses

```
int tx = get_global_id(0);
int ty = get_global_id(1);
for(i3=0; i3<P; i3++)
    C[tx][ty] += A[tx][i3]*B[i3][ty];</pre>
```

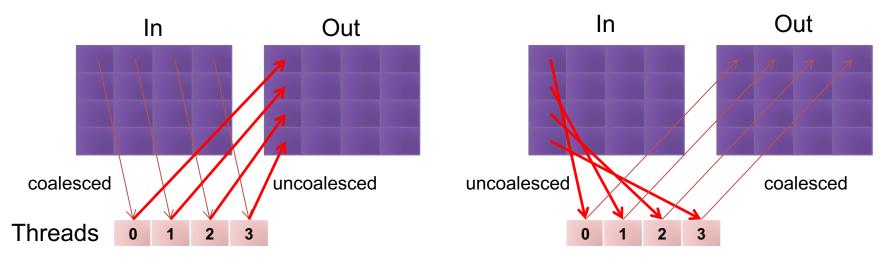
- In mapping 2, consecutive threads (tx) are mapped to consecutive elements in Matrices B and C
  - Accesses to both of these matrices will be coalesced
    - Degree of coalescence depends on the workgroup and data sizes

```
int tx = get_global_id (0);
int ty = get_global_id (1);
for(i3=0; i3<P; i3++)
    C[ty][tx] += A[ty][i3]*B[i3][tx];</pre>
```

- In general, threads can be created and mapped to any data element by manipulating the values returned by the thread identifier functions
- The following matrix transpose example will show how thread IDs can be modified to achieve efficient memory accesses

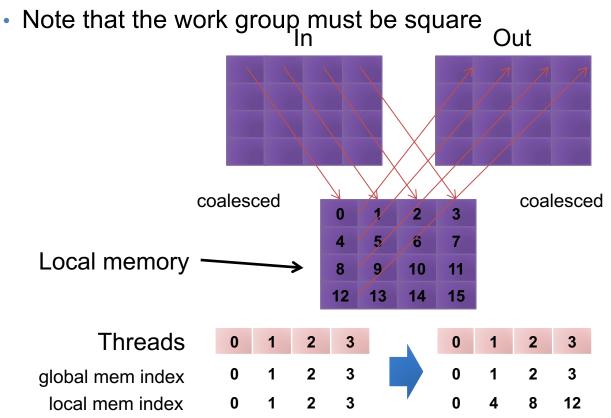
### Matrix Transpose

- A matrix transpose is a straightforward technique
  - Out(x,y) = In(y,x)
- No matter which thread mapping is chosen, one operation (read/write) will produce coalesced accesses while the other (write/read) produces uncoalesced accesses
  - Note that data must be read to a temporary location (such as a register) before being written to a new location



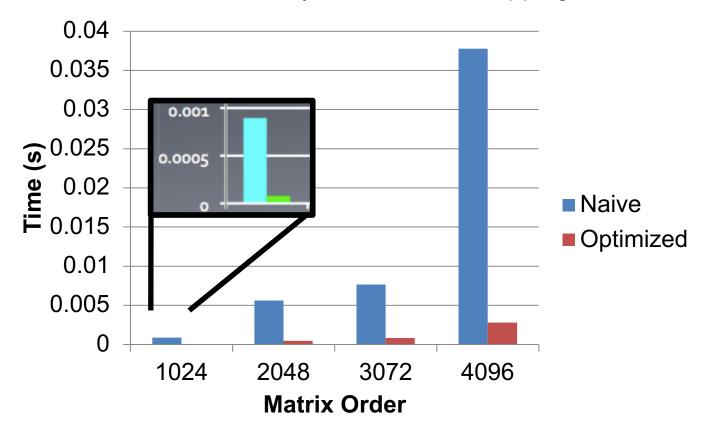
#### Matrix Transpose

 If local memory is used to buffer the data between reading and writing, we can rearrange the thread mapping to provide coalesced accesses in both directions



### Matrix Transpose

- The following figure shows a performance comparison of the two transpose kernels for matrices of size NxM on an AMD 5870 GPU
  - "Optimized" uses local memory and thread remapping



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#### 设备占用

- On current GPUs, work groups get mapped to compute units
  - When a work group is mapped to a compute unit, it cannot be swapped off until all of its threads complete their execution
- If there are enough resources available, multiple work groups can be mapped to the same compute unit at the same time
  - Wavefronts from another work group can be swapped in to hide latency
- Resources are fixed per compute unit (number of registers, local memory size, maximum number of threads)
  - Any one of these resource constraints may limit the number of work groups on a compute unit
- The term occupancy is used to describe how well the resources of the compute unit are being utilized

### 设备占用——寄存器

- The availability of registers is one of the major limiting factor for larger kernels
- The maximum number of registers required by a kernel must be available for all threads of a workgroup
  - Example: Consider a GPU with 16384 registers per compute unit running a kernel that requires 35 registers per thread
    - Each compute unit can execute at most 468 threads
    - This affects the choice of workgroup size
      - A workgroup of 512 is not possible
      - Only 1 workgroup of 256 threads is allowed at a time, even though 212 more threads could be running
      - 3 workgroups of 128 threads are allowed, providing 384 threads to be scheduled, etc.

### 设备占用——寄存器

- Consider another example:
  - A GPU has 16384 registers per compute unit
  - The work group size of a kernel is fixed at 256 threads
  - The kernel currently requires 17 registers per thread
- Given the information, each work group requires 4352 registers
  - This allows for 3 active work groups if registers are the only limiting factor
- If the code can be restructured to only use 16 registers,
   then 4 active work groups would be possible

#### 设备占用——本地内存

- GPUs have a limited amount of local memory on each compute unit
  - 32KB of local memory on AMD GPUs
  - 32-48KB of local memory on NVIDIA GPUs
- Local memory limits the number of active work groups per compute unit
- Depending on the kernel, the data per workgroup may be fixed regardless of number of threads (e.g., histograms), or may vary based on the number of threads (e.g., matrix multiplication, convolution)

#### 设备占用——线程资源

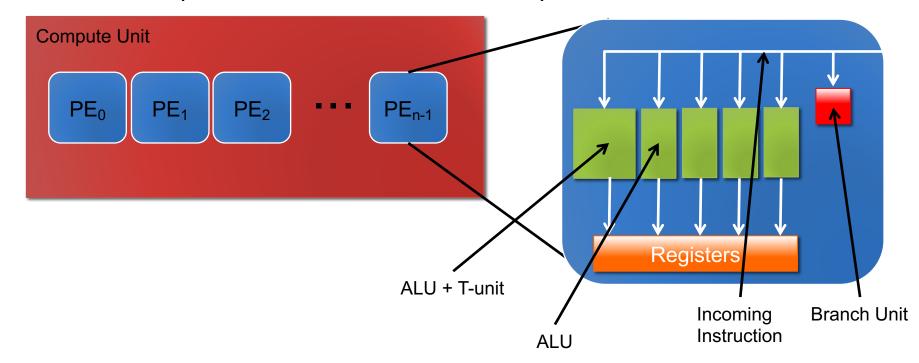
- GPUs have hardware limitations on the maximum number of threads per work group
  - 256 threads per WG on AMD GPUs
  - 512 threads per WG on NVIDIA GPUs
- NVIDIA GPUs have per-compute-unit limits on the number of active threads and work groups (depending on the GPU model)
  - 768 or 1024 threads per compute unit
  - 8 or 16 warps per compute unit
- AMD GPUs have GPU-wide limits on the number of wavefronts
  - 496 wavefronts on the AMD 5870 GPU (~25 wavefronts or ~1600 threads per compute unit)

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#### 向量化

- On AMD GPUs, each processing element executes a 5way VLIW instruction
  - 5 scalar operations or
  - 4 scalar operations + 1 transcendental operation

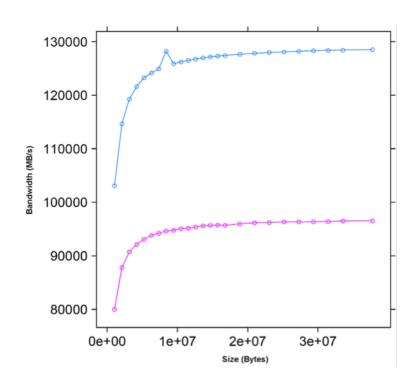


#### 向量化

- Vectorization allows a single thread to perform multiple operations at once
- Explicit vectorization is achieved by using vector datatypes (such as float4) in the source program
  - When a number is appended to a datatype, the datatype becomes an array of that length
  - Operations can be performed on vector datatypes just like regular datatypes
    - Each ALU will operate on different element of the float4 data

#### 向量化

- Vectorization improves memory performance on AMD GPUs
  - The AMD Accelerated Parallel Processing OpenCL Programming Guide compares float to float4 memory bandwidth

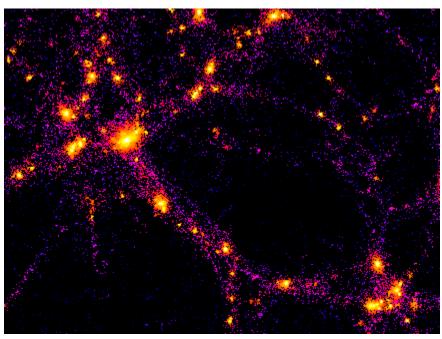


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# N-body 仿真

- An n-body simulation is a simulation of a system of particles under the influence of physical forces like gravity
  - E.g.: An astrophysical system where a particle represents a galaxy or an individual star
- N<sup>2</sup> particle-particle interactions
  - Simple, highly data parallel algorithm
- Allows us to explore optimizations of both the algorithm and its implementation on a platform



Source: THE GALAXY-CLUSTER-SUPERCLUSTER CONNECTION <a href="http://www.casca.ca/ecass/issues/1997-DS/West/west-bil.html">http://www.casca.ca/ecass/issues/1997-DS/West/west-bil.html</a>

## Algorithm

- The gravitational attraction between two bodies in space is an example of an N-body problem
  - Each body represents a galaxy or an individual star, and bodies attract each other through gravitational force
- Any two bodies attract each other through gravitational forces (F)

$$F = G * \left( \frac{m_i * m_j}{\parallel r_{ij} \parallel^2} \right) * \frac{r_{ij}}{\parallel r_{ij} \parallel}$$

F = Resultant Force Vector between particles i and j

G = Gravitational Constant

 $m_i = Mass of particle i$ 

 $m_i = \text{Mass of particle j}$ 

 $r_{ii}$  = Distance of particle i and j

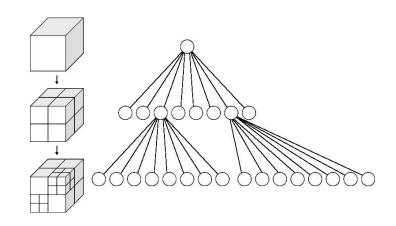
For each particle this becomes

$$F_i = (G * m_i) * \sum_{j=1 \to N} \left( \frac{m_j}{\mid\mid r_{ij}\mid\mid^2} * \left( \frac{r_{ij}}{\mid\mid r_{ij}\mid\mid} \right) \right)$$

- An O(N<sup>2</sup>) algorithm since N\*N interactions need to be calculated
- This method is known as an all-pairs N-body simulation

## N-body Algorithms

- For large counts, the previous method calculates of force contribution of distant particles
  - Distant particles hardly affect resultant force
- Algorithms like Barnes Hut reduce number of particle interactions calculated
  - Volume divided into cubic cells in an octree
  - Only particles from nearby cells need to be treated individually
  - Particles in distant cells treated as a single large particle
- In this lecture we restrict ourselves to a simple all pair simulation of particles with gravitational forces



- A octree is a tree where a node has exactly 8 children
- Used to subdivide a 3D space

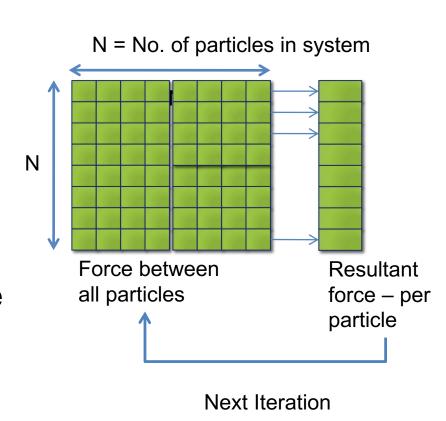
## Basic Implementation – All pairs

- All-pairs technique is used to calculate close-field forces
- Why bother, if infeasible for large particle counts?
  - Algorithms like Barnes Hut calculate far field forces using near-field results
  - Near field still uses all pairs
  - So, implementing all pairs improves performance of both near and far field calculations
- Easy serial algorithm
  - Calculate force by each particle
  - Accumulate of force and displacement in result vector

```
for(i=0; i<n; i++)
   ax = ay = az = 0;
  // Loop over all particles "j"
  for (j=0; j< n; j++) {
     //Calculate Displacement
            dx=x[j]-x[i];
            dy=y[j]-y[i];
            dz=z[i]-z[i];
            // small eps is delta added for
dx,dy,dz = 0
            invr = 1.0/sqrt(dx*dx+dy*dy+dz*dz
+eps);
            invr3 = invr*invr*invr;
            f=m[ j ]*invr3;
            // Accumulate acceleration
            ax += f*dx:
            ay += f*dy;
            az += f*dx;
  // Use ax, ay, az to update particle
positions
```

### Parallel Implementation

- Forces of each particle can be computed independently
  - Accumulate results in local memory
  - Add accumulated results to previous position of particles
- New position used as input to the next time step to calculate new forces acting between particles



## Naïve Parallel Implementation

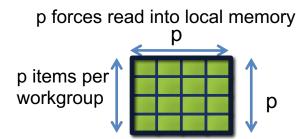
- Disadvantages of implementation where each work item reads data independently
  - No reuse since redundant reads of parameters for multiple work-items
  - Memory access= N reads\*N threads= N<sup>2</sup>

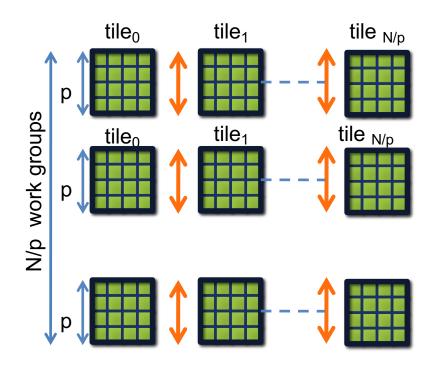
```
N = No. of particles
All N particles read in by each
work item
```

```
kernel void nbody(
            global float4 * initial pos,
            global float4 * final pos,
          Int N, local float4 * result) {
int localid = get local id(0);
int globalid = get global id(0);
result [localid] = 0;
for( int i=0 ; i<N;i++) {
         //! Calculate interaction between
   //! particle globalid and particle i
          GetForce( globalid, i,
                       initial pos, final pos,
                       &result [localid]);
          finalpos[ globalid] = result[ localid];
```

### **Local Memory Optimizations**

- Data Reuse
  - Any particle read into compute unit can be used by all p bodies
- Computational tile:
  - Square region of the grid of forces consisting of size p
  - 2p descriptions required to evaluate all p<sup>2</sup> interactions in tile
  - p work items (in vertical direction) read in p forces
- Interactions on p bodies captured as an update to p acceleration vectors
- Intra-work group synchronization shown in orange required since all work items use data read by each work item





## OpenCL Implementation

- Data reuse using local memory
  - Without reuse N\*p items read per work group
  - With reuse p\*(N/p) = N items read per work group
  - All work items use data read in by each work item
- SIGNIFICANT improvement: p is work group size (at least 128 in OpenCL, discussed in occupancy)
- Loop nest shows how a work item traverses all tiles
- Inner loop accumulates contribution of all particles within tile

#### Kernel Code

```
for (int i = 0; i < numTiles; ++i)
     // load one tile into local memory
     int idx = i * localSize + tid:
     localPos[tid] = pos[idx];
    barrier(CLK LOCAL MEM FENCE);
    // calculate acceleration effect due to each body
   for( int j = 0; j < localSize; ++j ) {
        // Calculate acceleration caused by particle i on i
       float4 r = localPos[i] - myPos;
        float distSqr = r.x * r.x + r.y * r.y + r.z * r.z;
       float invDist = 1.0f / sqrt(distSqr + epsSqr);
              float s = localPos[i].w * invDistCube;
        // accumulate effect of all particles
       acc += s * r;
     // Synchronize so that next tile can be loaded
     barrier(CLK LOCAL MEM FENCE);
```

#### Thread Mapping and Vectorization

- As discussed previously,
  - Vectorization allows a single thread to perform multiple operations in one instruction
  - Explicit vectorization is achieved by using vector data-types (such as float4) in the source
- Vectorization using float4 enables efficient usage of memory bus for AMD GPUs
  - Easy in this case due to the vector nature of the data which are simply spatial coordinates
- Vectorization of memory accesses implemented using float4 to store coordinates

```
// Loop Nest Calculating per tile interaction
// Same loop nest as in previous slide
for (int i=0 ; i< numTiles; i++)
{
    for( int j=0; j<localsize; j ++)
    }
}</pre>
```

## Performance - Loop Unrolling

- We also attempt loop unrolling of the reuse local memory implementation
  - We unroll the innermost loop within the thread
- Loop unrolling can be used to improve performance by removing overhead of branching
  - However this is very beneficial only for tight loops where the branching overhead is comparable to the size of the loop body
  - Experiment on optimized local memory implementation
  - Executable size is not a concern for GPU kernels
- We implement unrolling by factors of 2 and 4 and we see substantial performance gains across platforms
  - Decreasing returns for larger unrolling factors seen

#### Effect of Unroll on Kernel Performance

#### Execution Time – Unrolled Kernels – with data reuse

