CLASS: S.E. E &TC **SUBJECT: DC**

EXPT. NO.: 6 **DATE: 05/12/2020**

ROLL NO:22119

TITLE : Study of Counter ICs (74LS90/74LS93)

PRE-REQUISITES FOR EXPT. : Definition of Asynchronous Counter, Implementation and operation of Asynchronous Counter using 74LS90/74LS93
(Refer Data-Sheet)

OBJECTIVE :

1. Design and Implement MOD-2 / MOD-5 / MOD-10 / MOD-N / MOD-NN using IC-74LS90. Draw the Timing Diagram.

2. Design and Implement MOD-2 / MOD-8 / MOD-16 / MOD-N / MOD-NN using IC-74LS93. Draw the Timing Diagram.

APPARATUS :

Digital-Board, GP-4Patch-Cords, IC-74LS32,IC-74LS00 / IC-74LS04/IC-74LS08, IC-74LS90,74LS93

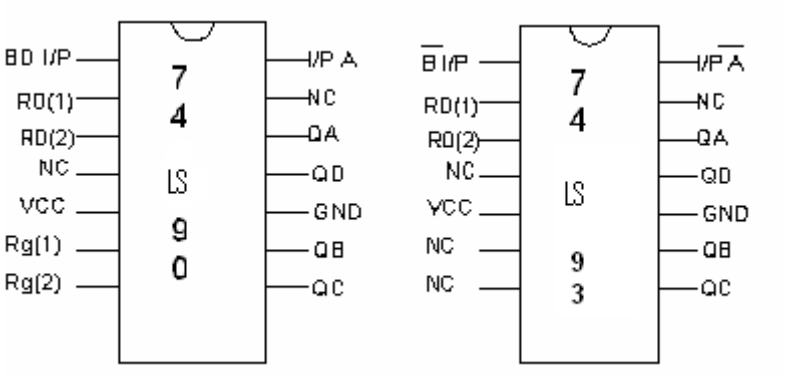
THEORY :

IC 74LS90 is 4-bit Ripple MOD-10 (Decade) Counter. Internal Structures of IC-74LS90 contained 4 MS-JK Flip-Flop.IC-74LS90 contained MOD-2 and MOD-5.IC-74HC90 contains two set & reset pin (R0 (1) & R0 (2) are reset pins which are active high and R9 (1) and R9 (2) are set pins which are active high). IC-74LS90 output will set to 1001 when R9 (1) and R9(2) are given with VCC logic, And IC-74LS90 output will reset when R0(1) and R0(2) are given with VCC logic. To implement Decade counter

cascade MOD-2 and MOD-5 Counter available in IC-7490.Connect set & reset pins to ground.

IC-74LS93 is a 4-bit ripple Up-Counter (4-bit binary Up-Counter), IC-74LS93 has MOD-2 and MOD-8 counter. To implement MOD-16, make a cascading of MOD-2 and MOD8.

PIN Diagram:

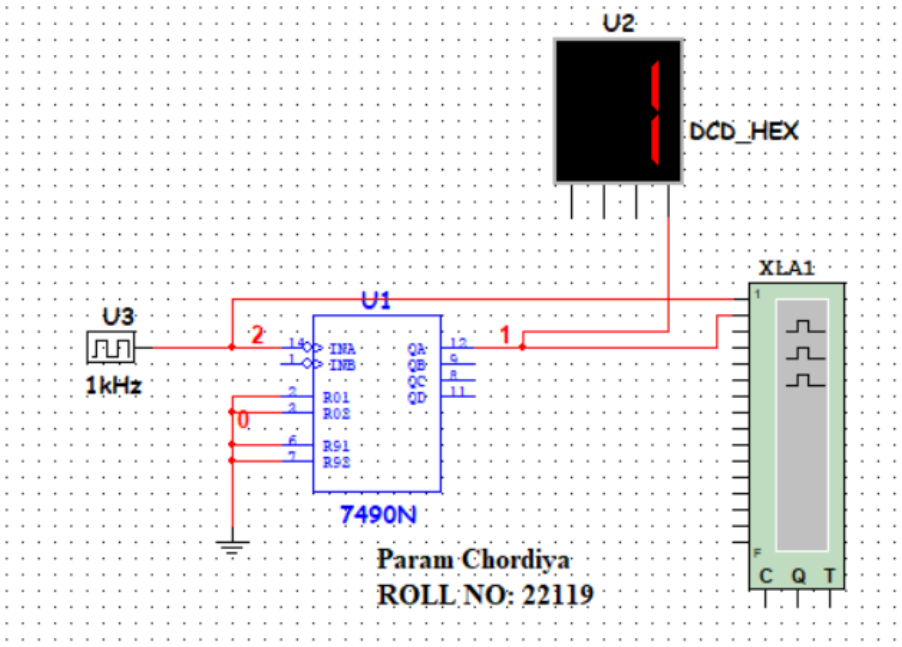


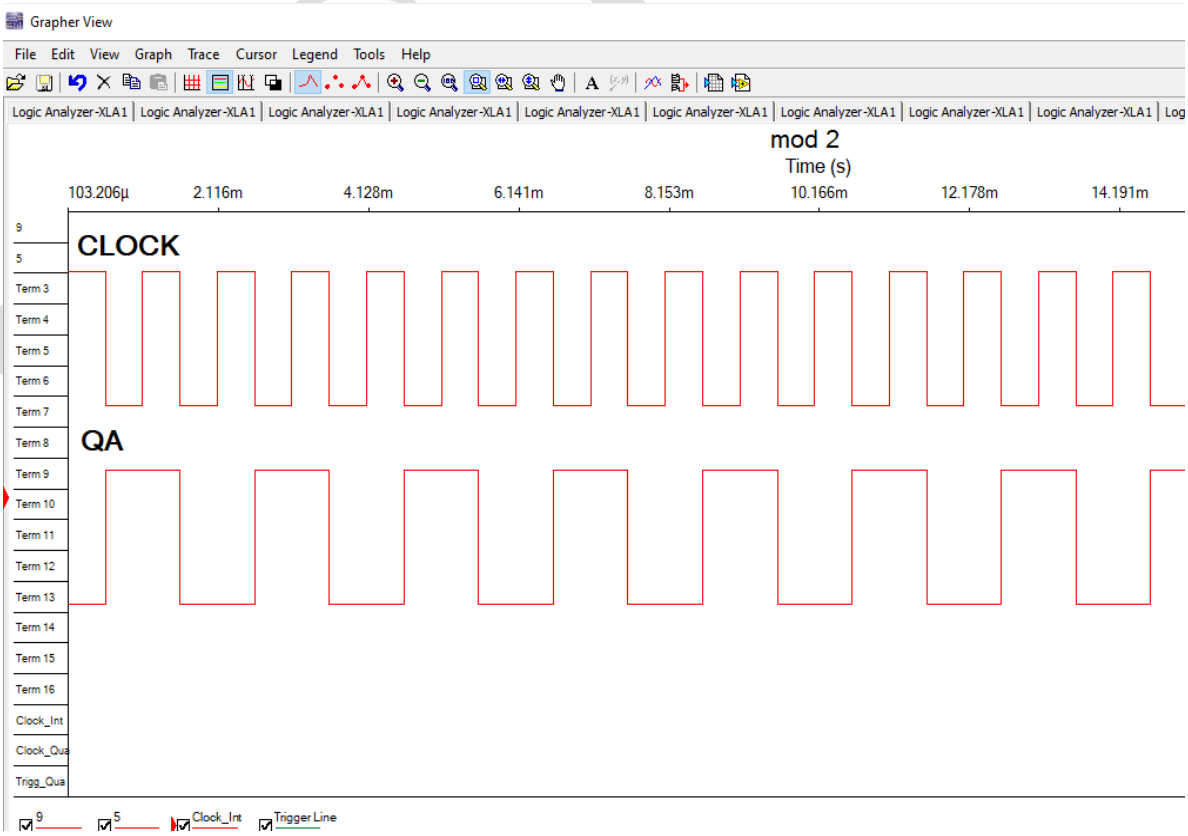
PROCEDURE :

1. Make the connections as per the Logic circuit of MOD-2 / MOD-5 / MOD-10 / MOD-N /MOD-NN using IC74LS90 and verify its state Table.
2. Make the connections as per the Logic circuit of MOD-2 / MOD-8 / MOD-16 /MOD-N / MOD-NN using IC74LS93 and verify its state Table.

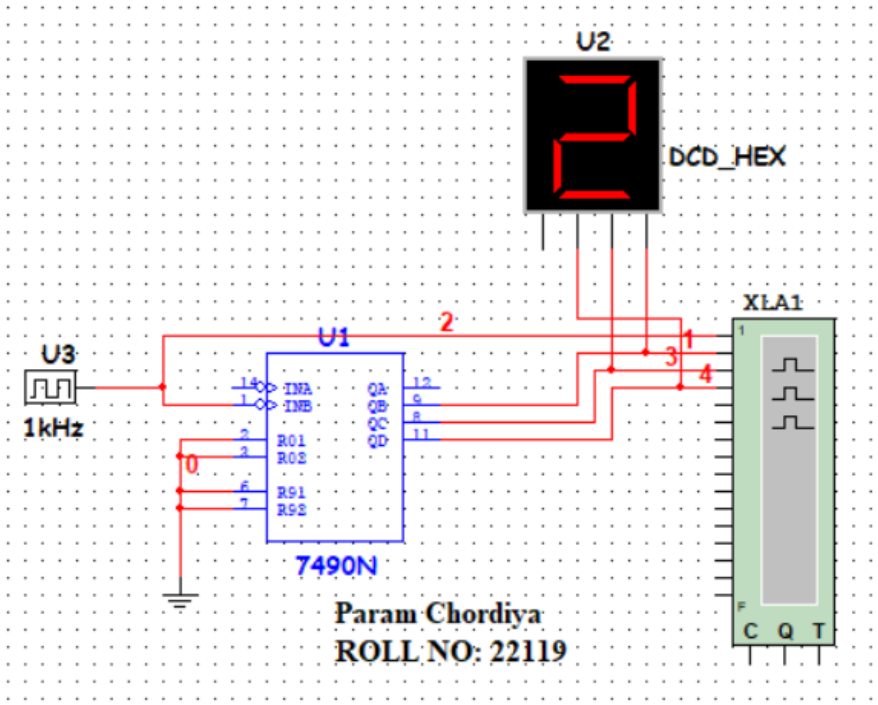
Logic Diagram: (MOD-2 /MOD-5 and MOD-10 using IC-74LS90)

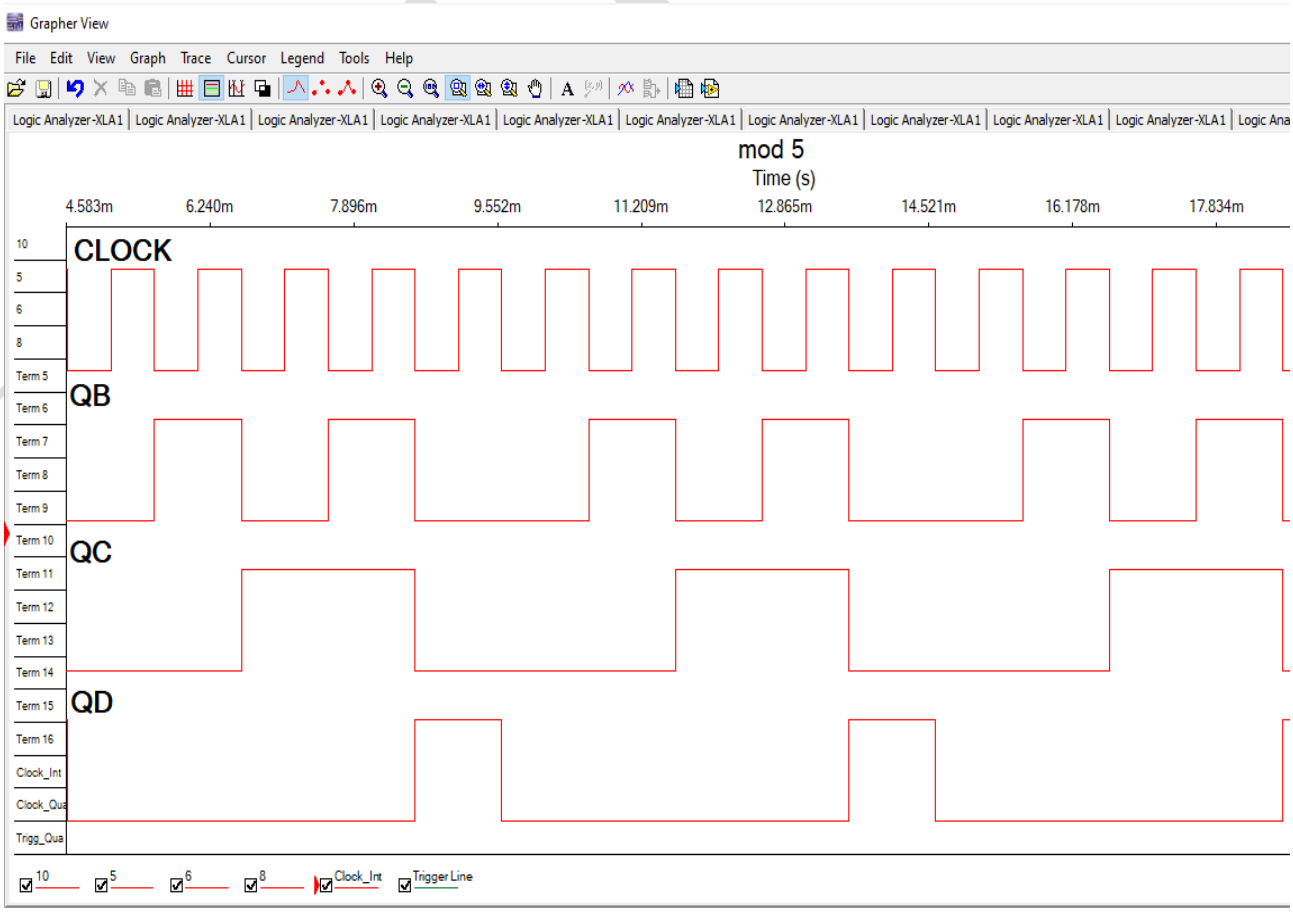
MOD2:



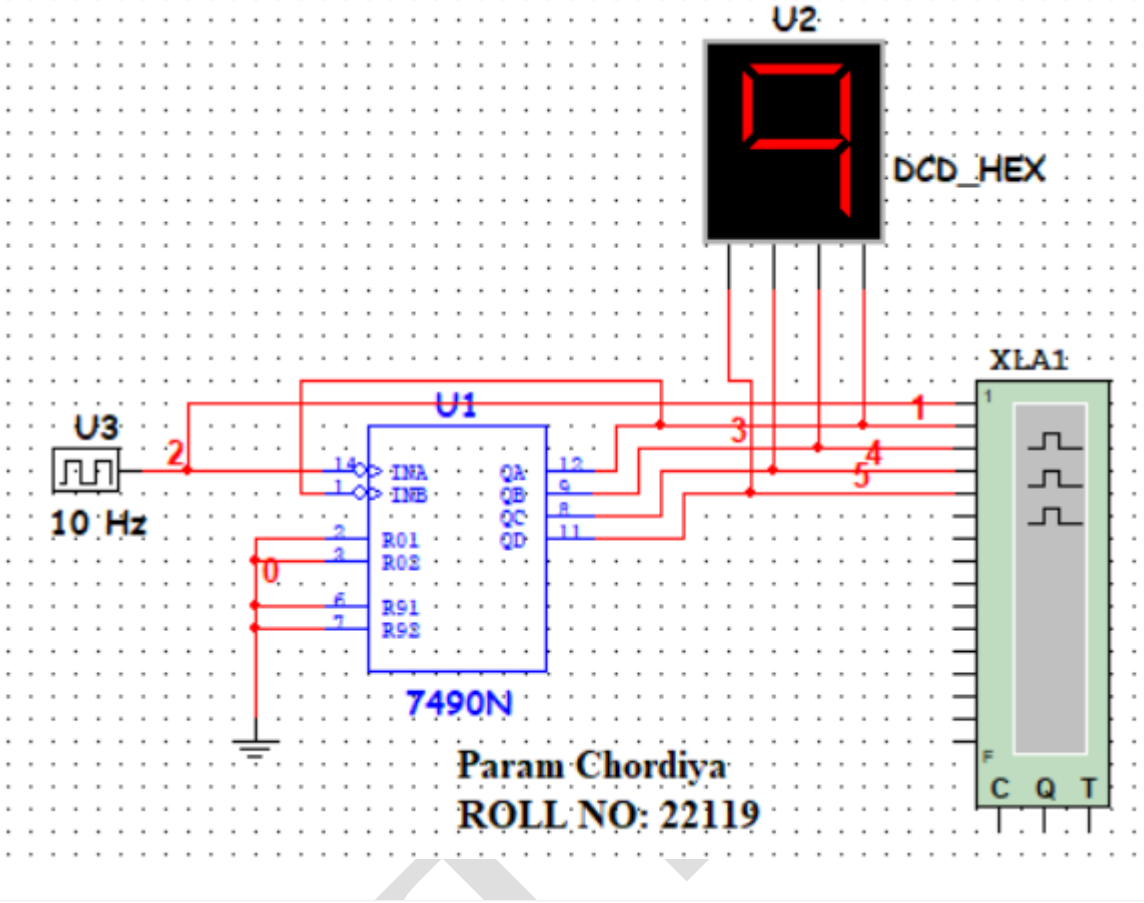


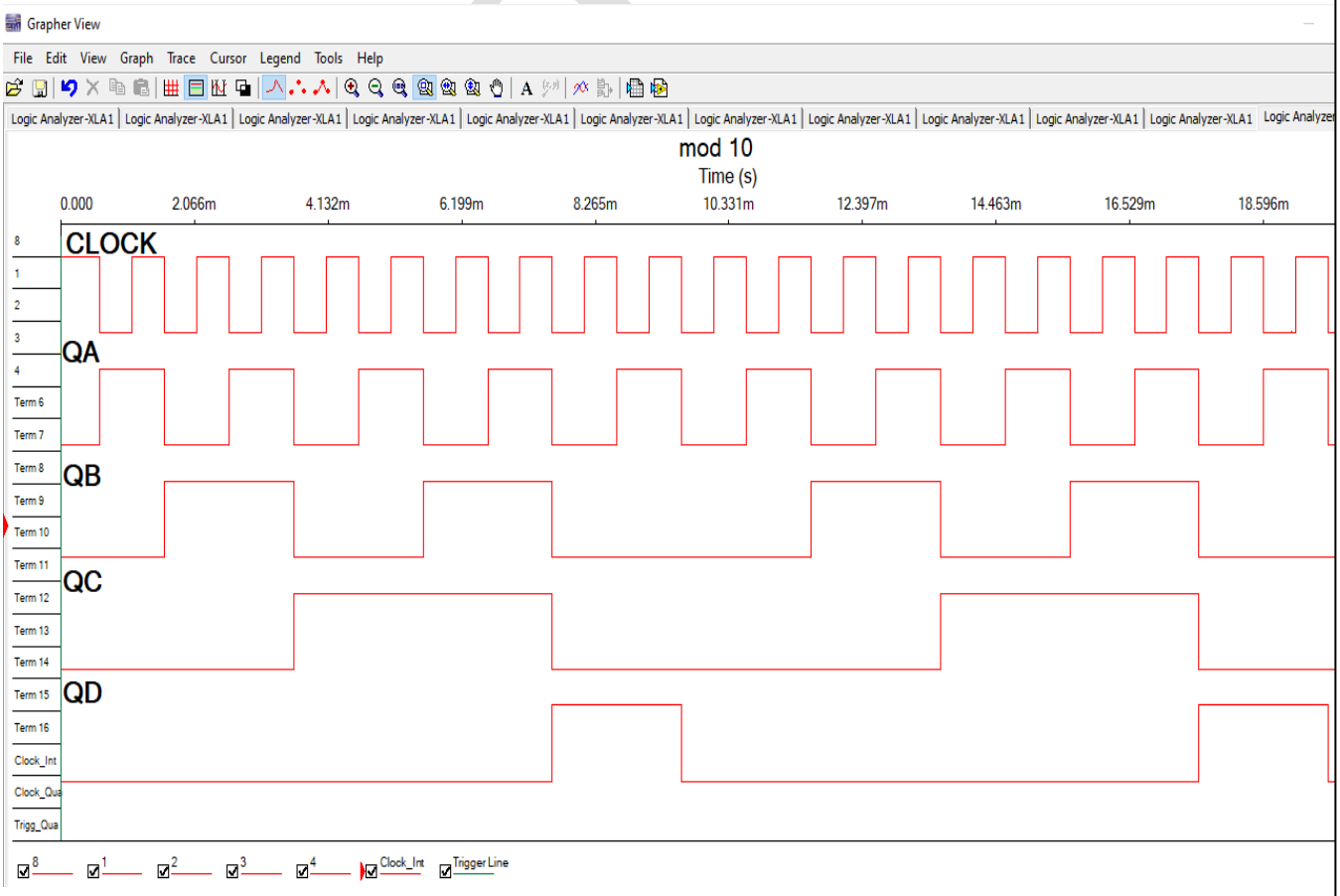
MOD5:


U2
DCD_HEX
XLA1
U3
1kHz
U1
7490N
Param Chordiya
ROLL NO: 22119
C Q T


Grapher View
File Edit View Graph Trace Cursor Legend Tools Help
mod 5
Time (s)
4.583m
6.240m
7.896m
9.552m
11.209m
12.865m
14.521m
16.178m
17.834m
CLOCK
QB
QC
QD
Clock_Int
Trigger Line

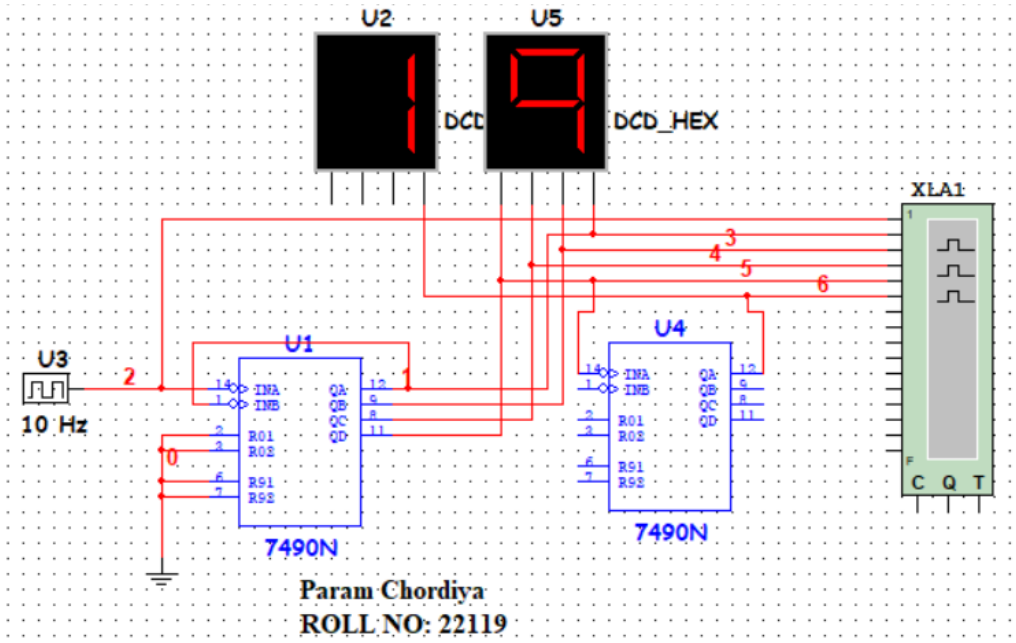
MOD10:

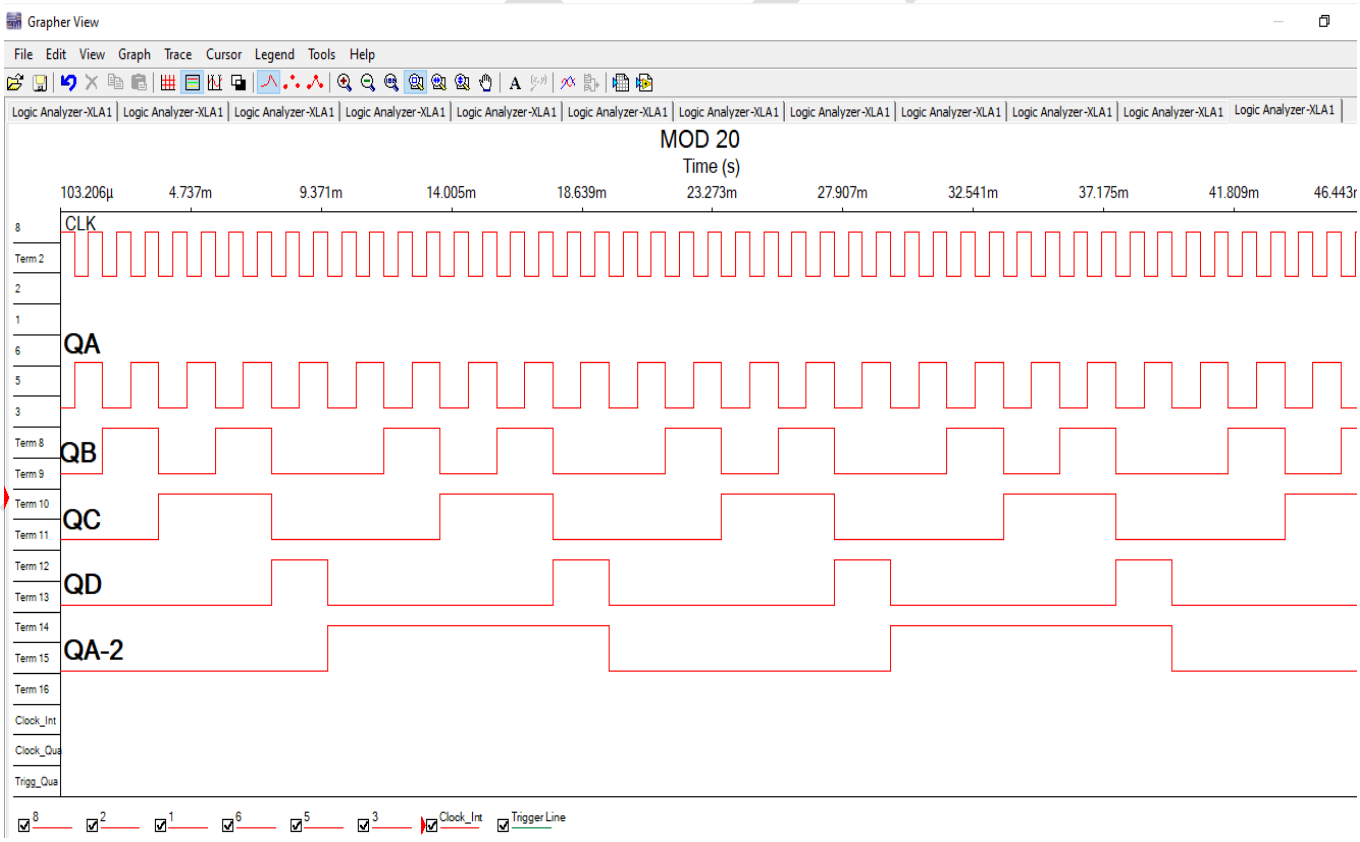

U2
DCD_HEX
XLA1
U1
U3
10 Hz
7490N
Param Chordiya
ROLL NO: 22119
C Q T


Grapher View
File Edit View Graph Trace Cursor Legend Tools Help
mod 10
Time (s)
0.000
2.066m
4.132m
6.199m
8.265m
10.331m
12.397m
14.463m
16.529m
18.596m
CLOCK
QA
QB
QC
QD
Clock_Int
Trigger Line

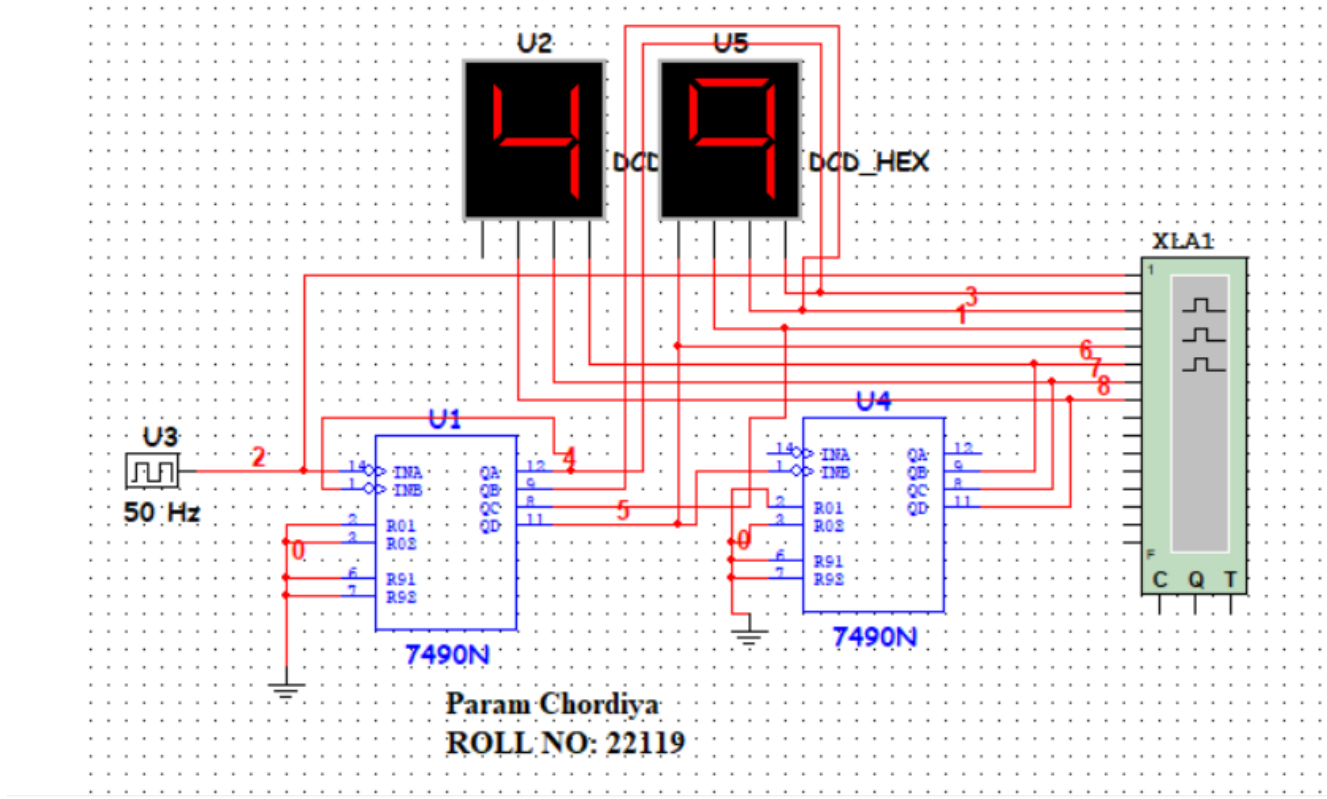
MOD 20 & MOD 50 :

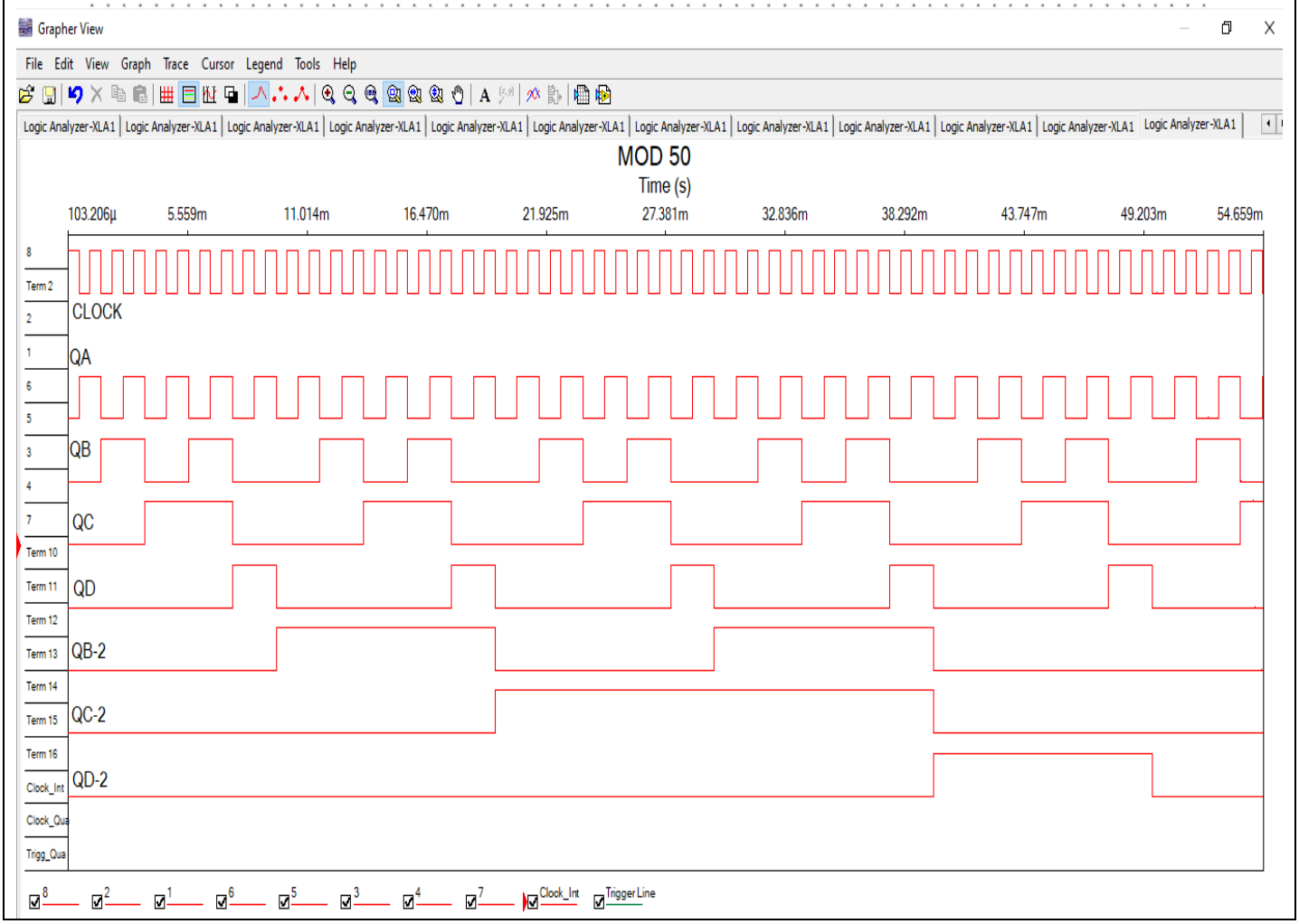
MOD20:



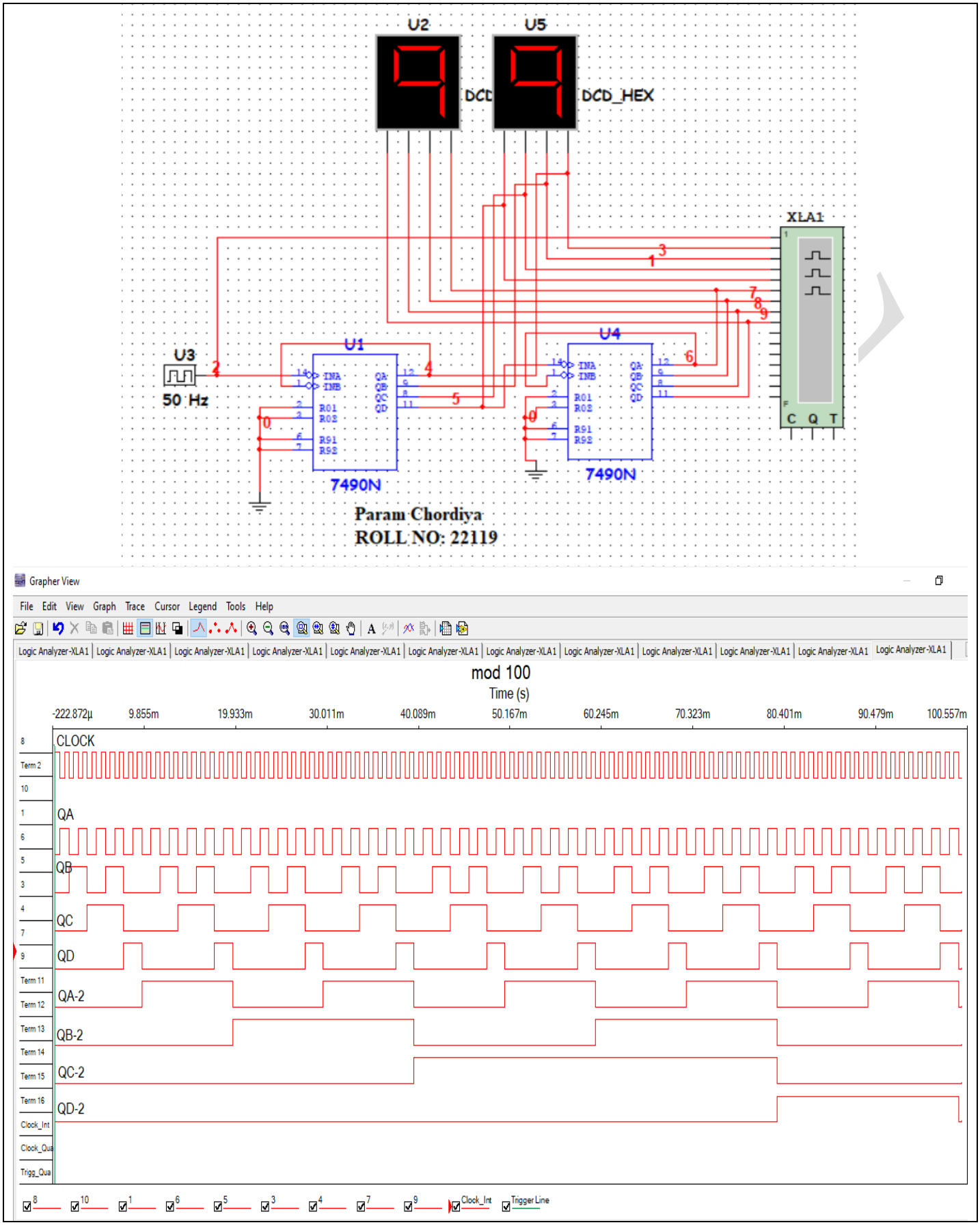


MOD50:


U2
U5
DCD
DCD_HEX
XLA1
U3
50 Hz
U1
U4
7490N
7490N
Param Chordiya
ROLL NO: 22119

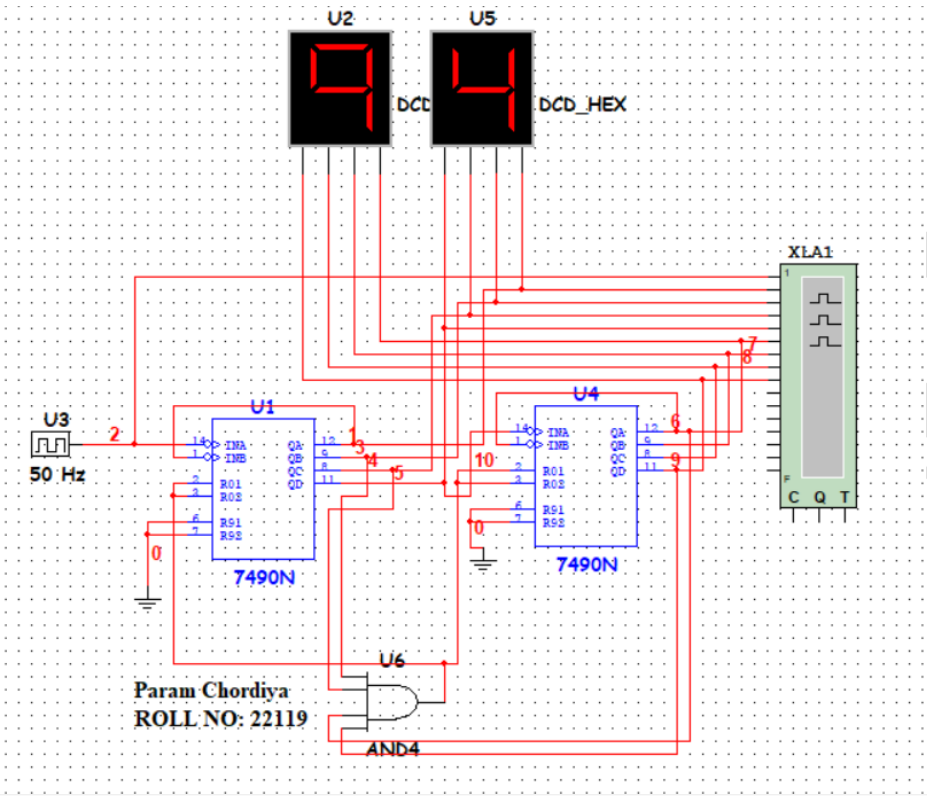

Grapher View
File Edit View Graph Trace Cursor Legend Tools Help
MOD 50
Time (s)
103.206µ
5.559m
11.014m
16.470m
21.925m
27.381m
32.836m
38.292m
43.747m
49.203m
54.659m
CLOCK
QA
QB
QC
QD
QB-2
QC-2
QD-2
Clock_Int
Trigger Line

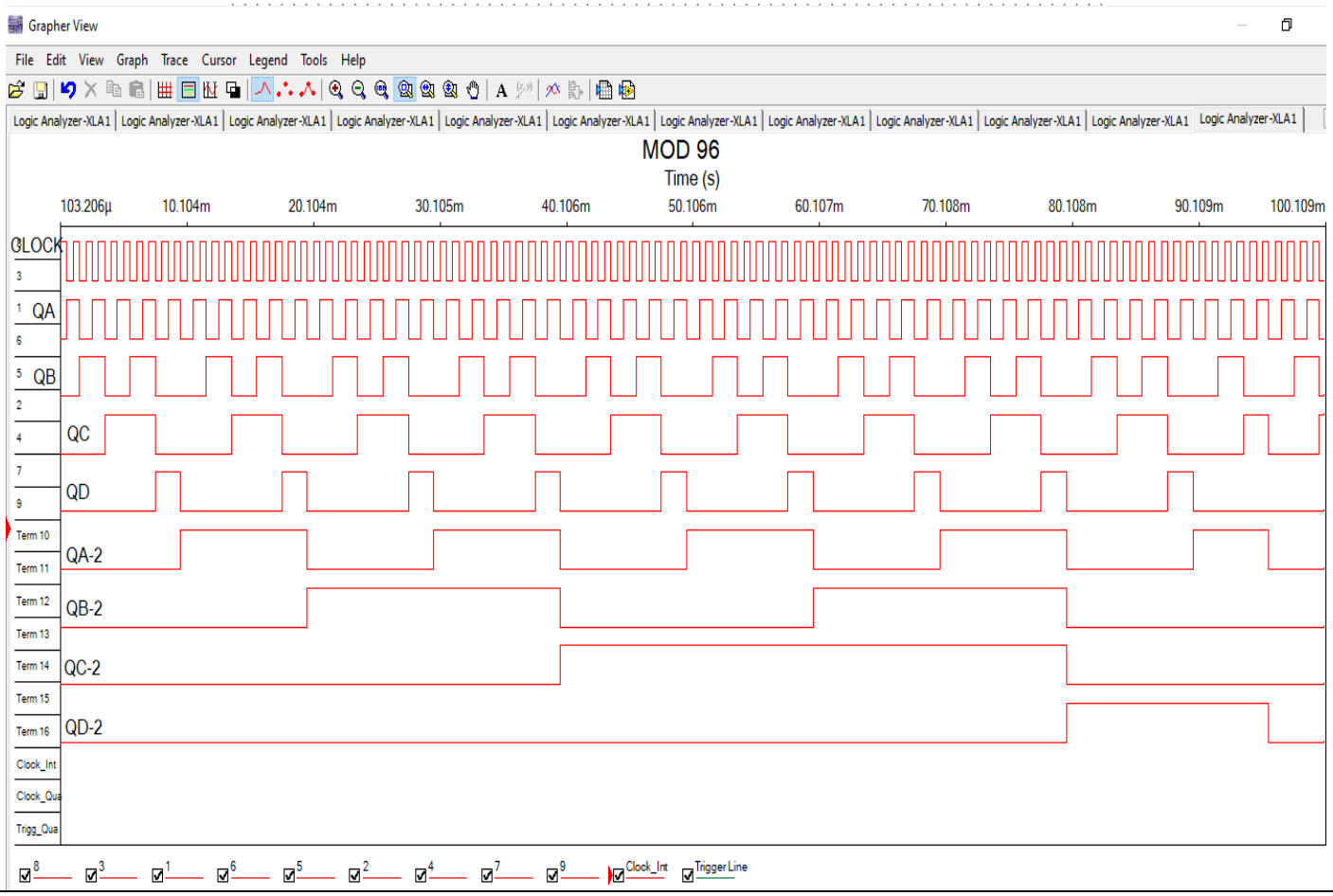
MOD: 100


U2
U5
DCD
DCD_HEX
XLA1
U3
50 Hz
U1
U4
7490N
7490N
Param Chordiya
ROLL NO: 22119
Grapher View
File Edit View Graph Trace Cursor Legend Tools Help
mod 100
Time (s)
-222.872µ
9.855m
19.933m
30.011m
40.089m
50.167m
60.245m
70.323m
80.401m
90.479m
100.557m
CLOCK
QA
QB
QC
QD
QA-2
QB-2
QC-2
QD-2
Clock_Int
Trigger Line

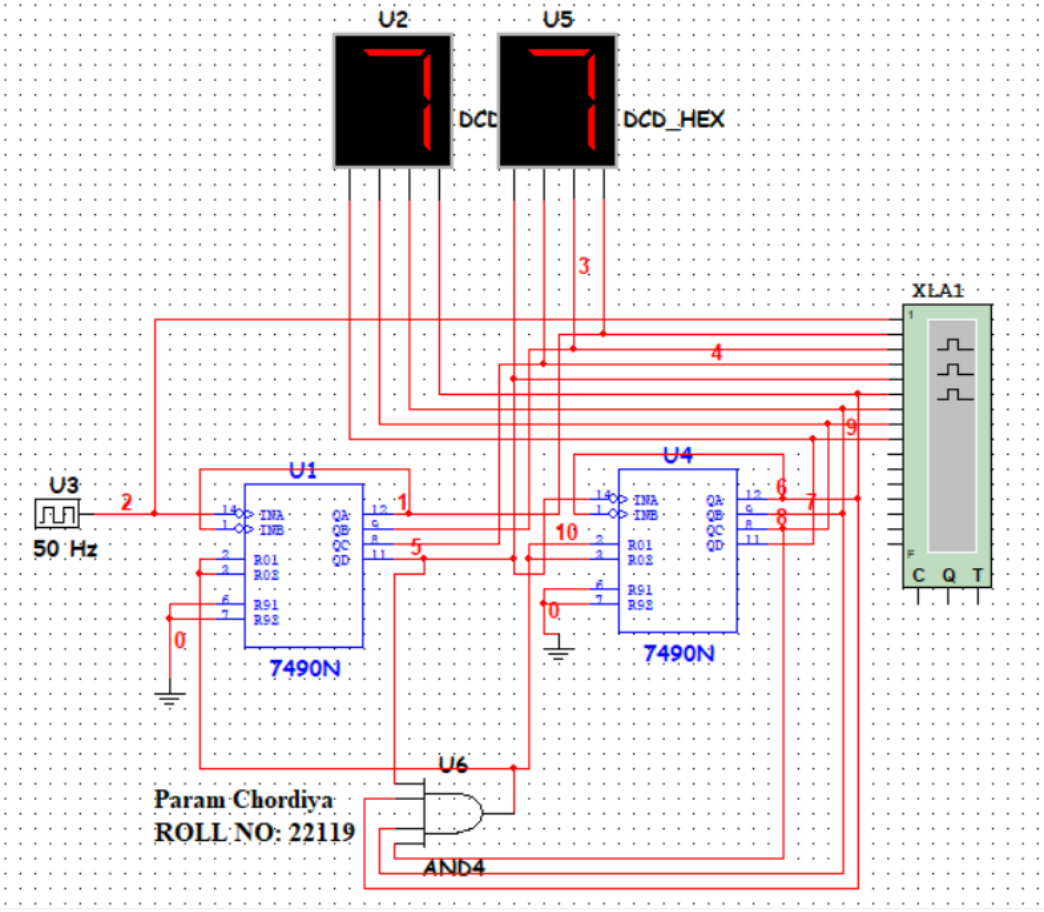
MOD 96 & MOD 78 :

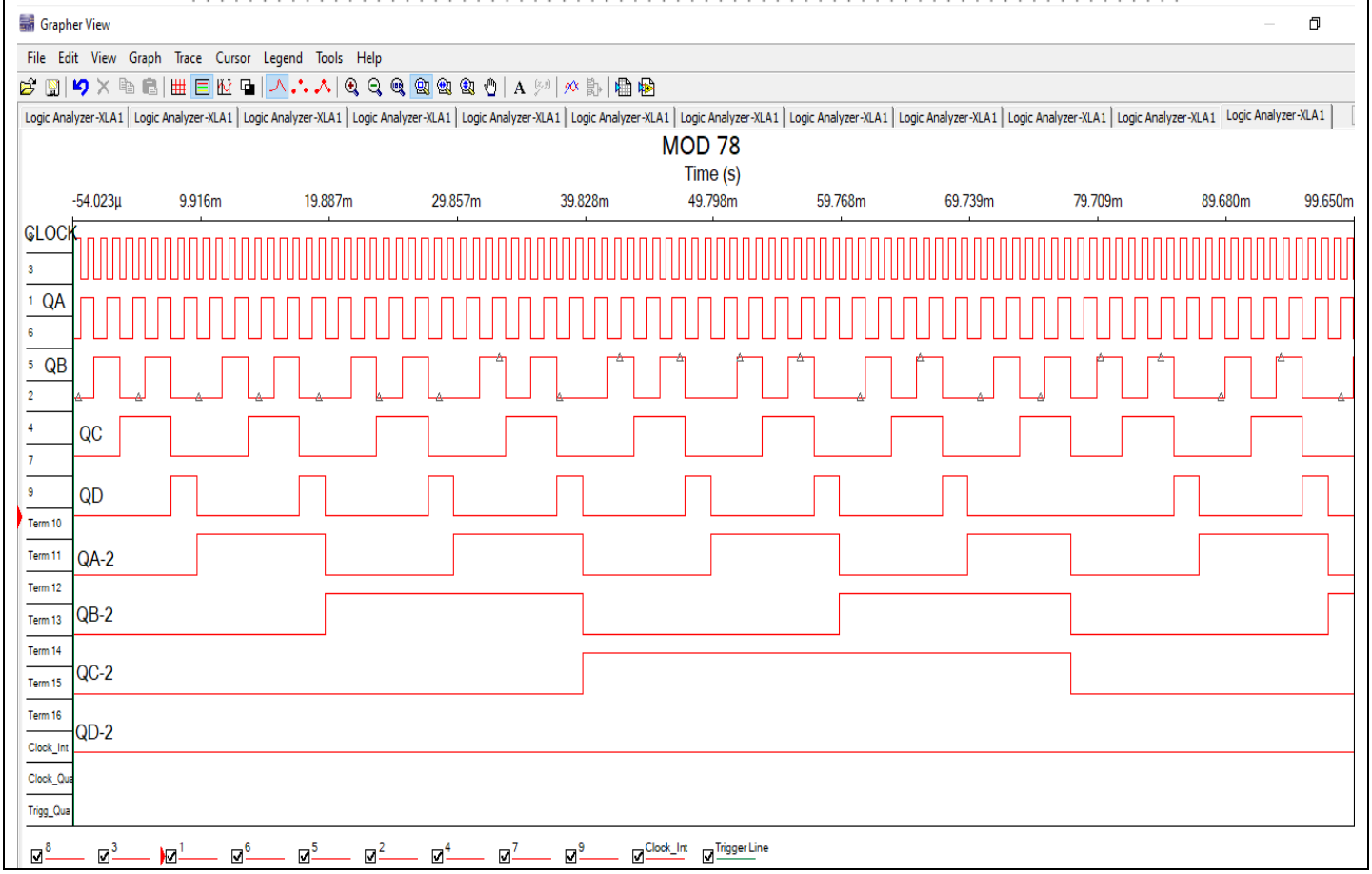
MOD96:





MOD78:

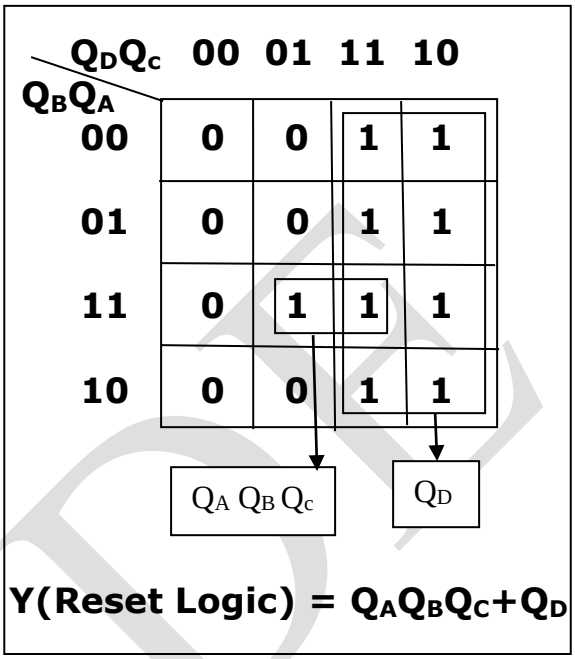

U2
U5
DCD
DCD_HEX
XLA1
U3
50 Hz
U1
U4
7490N
7490N
U6
AND4
Param Chordiya
ROLL NO: 22119


Grapher View
File Edit View Graph Trace Cursor Legend Tools Help
MOD 78
Time (s)
-54.023µ
9.916m
19.887m
29.857m
39.828m
49.798m
59.768m
69.739m
79.709m
89.680m
99.650m
CLOCK
QA
QB
QC
QD
QA-2
QB-2
QC-2
QD-2
Clock_Int
Trigger Line

Design of MOD-7 Ripple Counter:

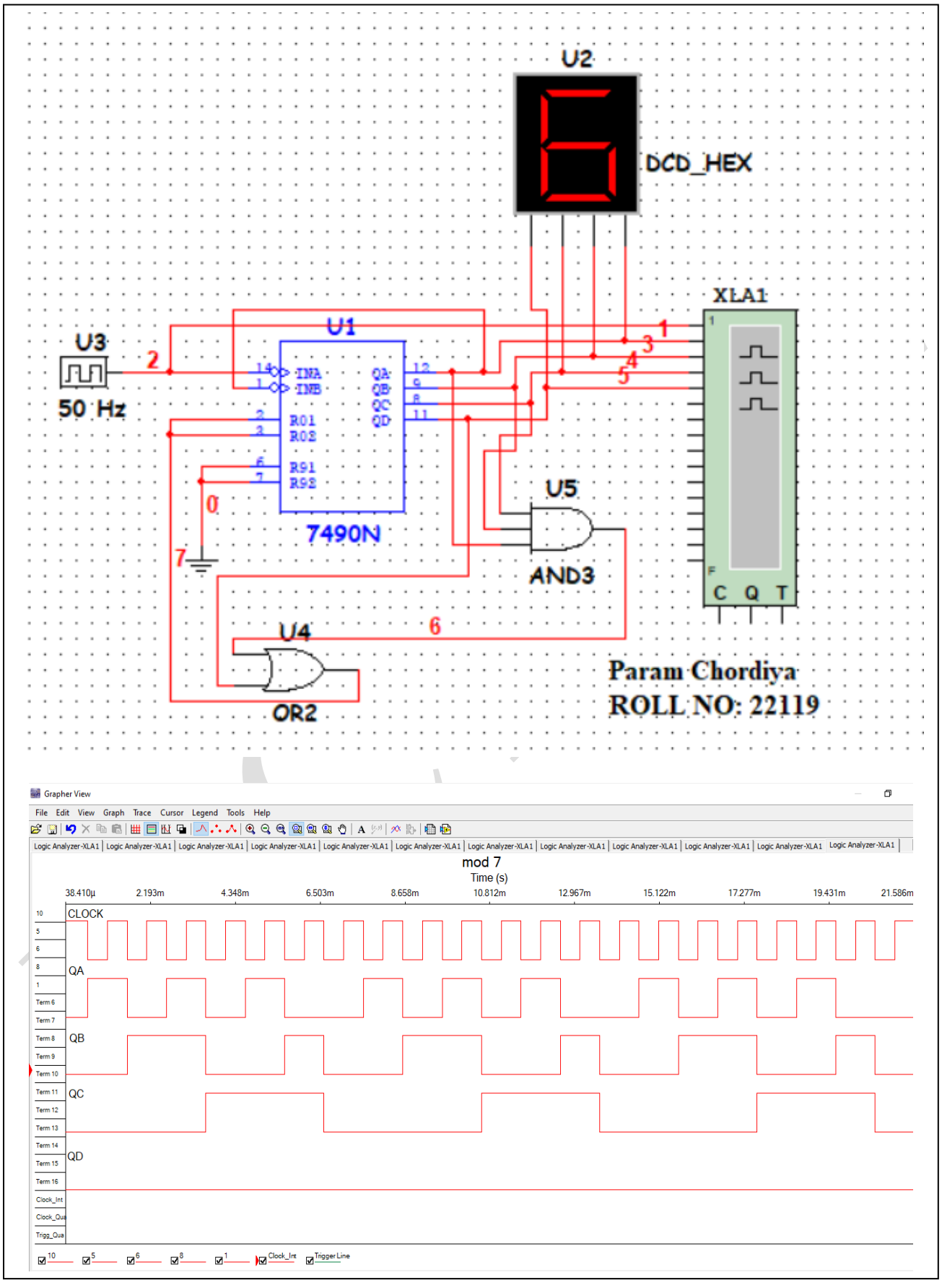
OUTPUT				RESET LOGIC
Q_D	Q_c	Q_B	Q_A	
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

K-Map for RESET Logic

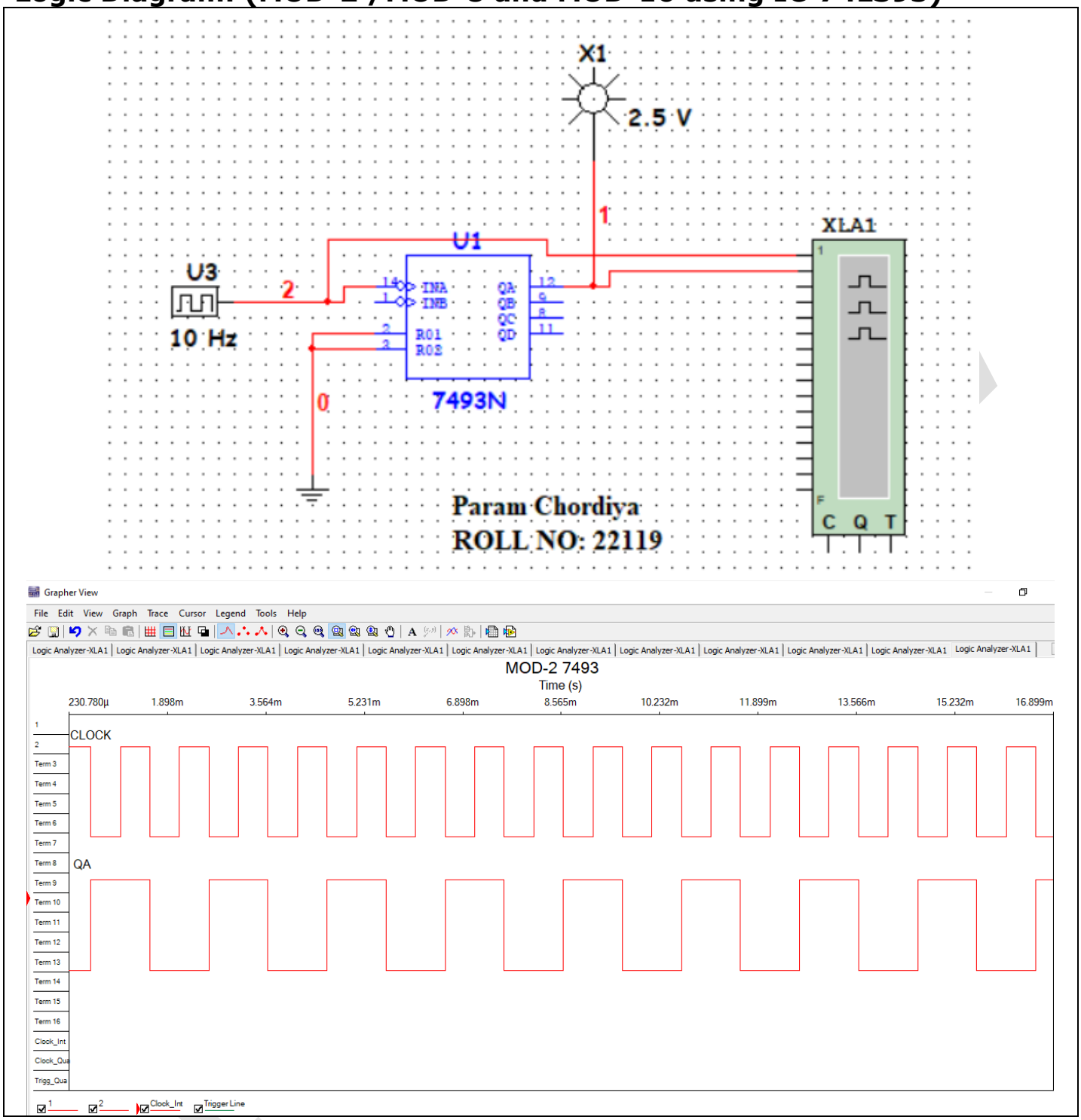


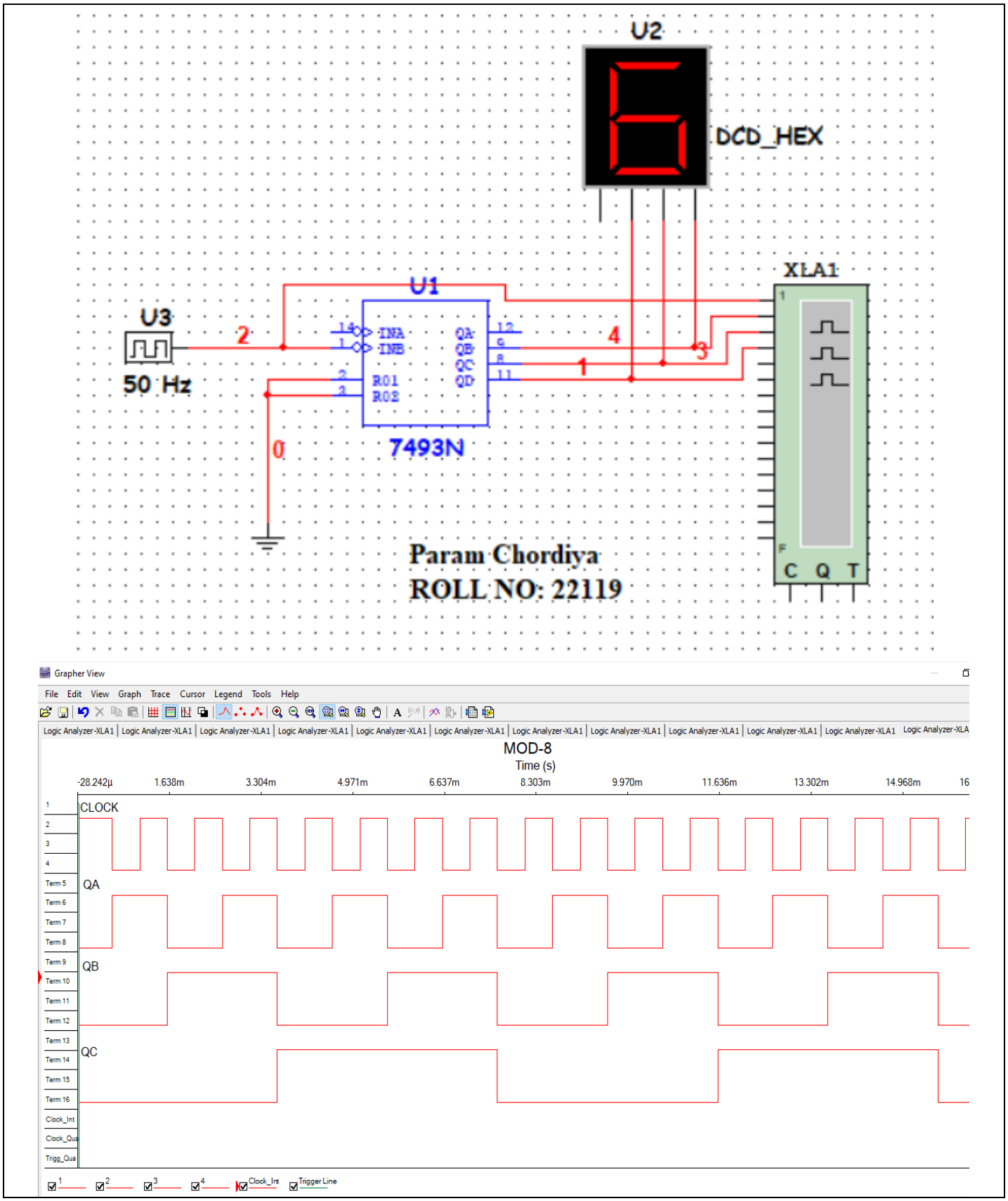
Y(Reset Logic) = $Q_AQ_BQ_C+Q_D$

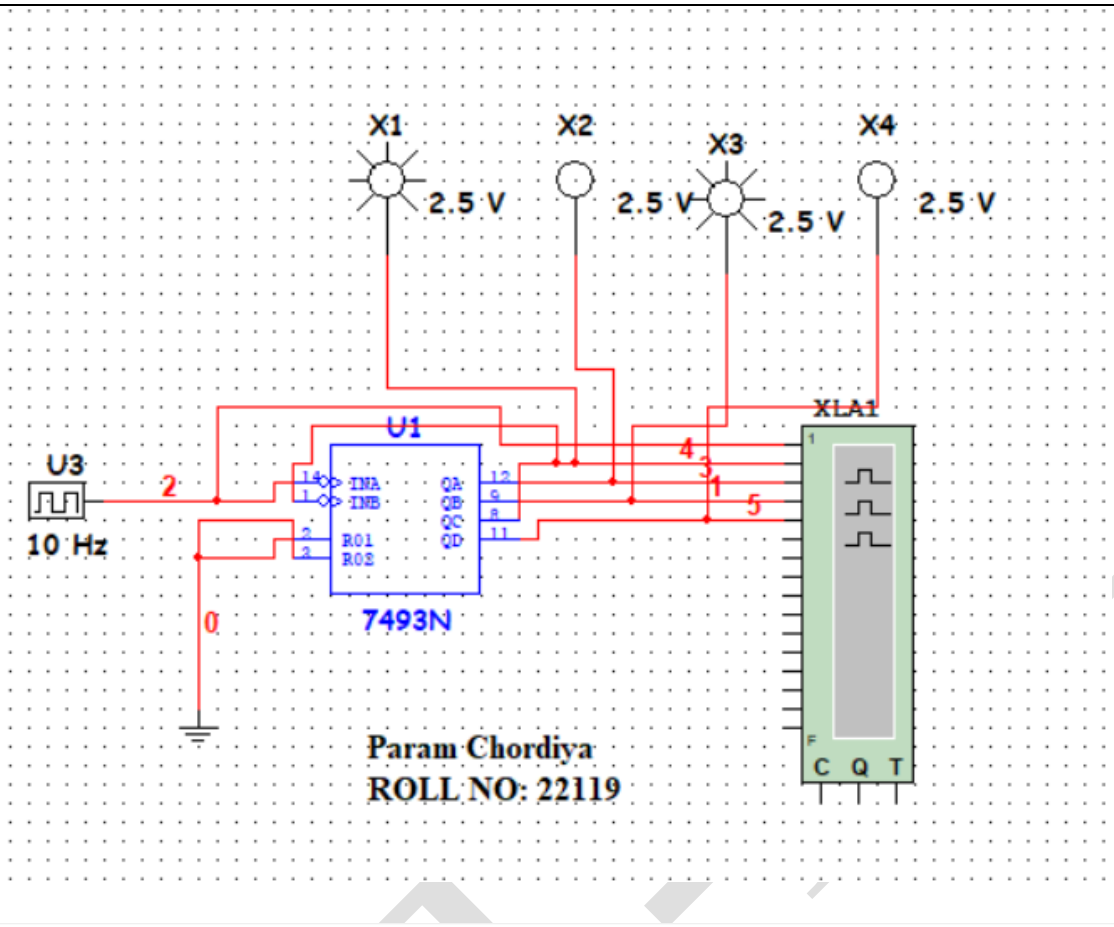
Logic Diagram: (MOD-N Counter using IC-74LS90)

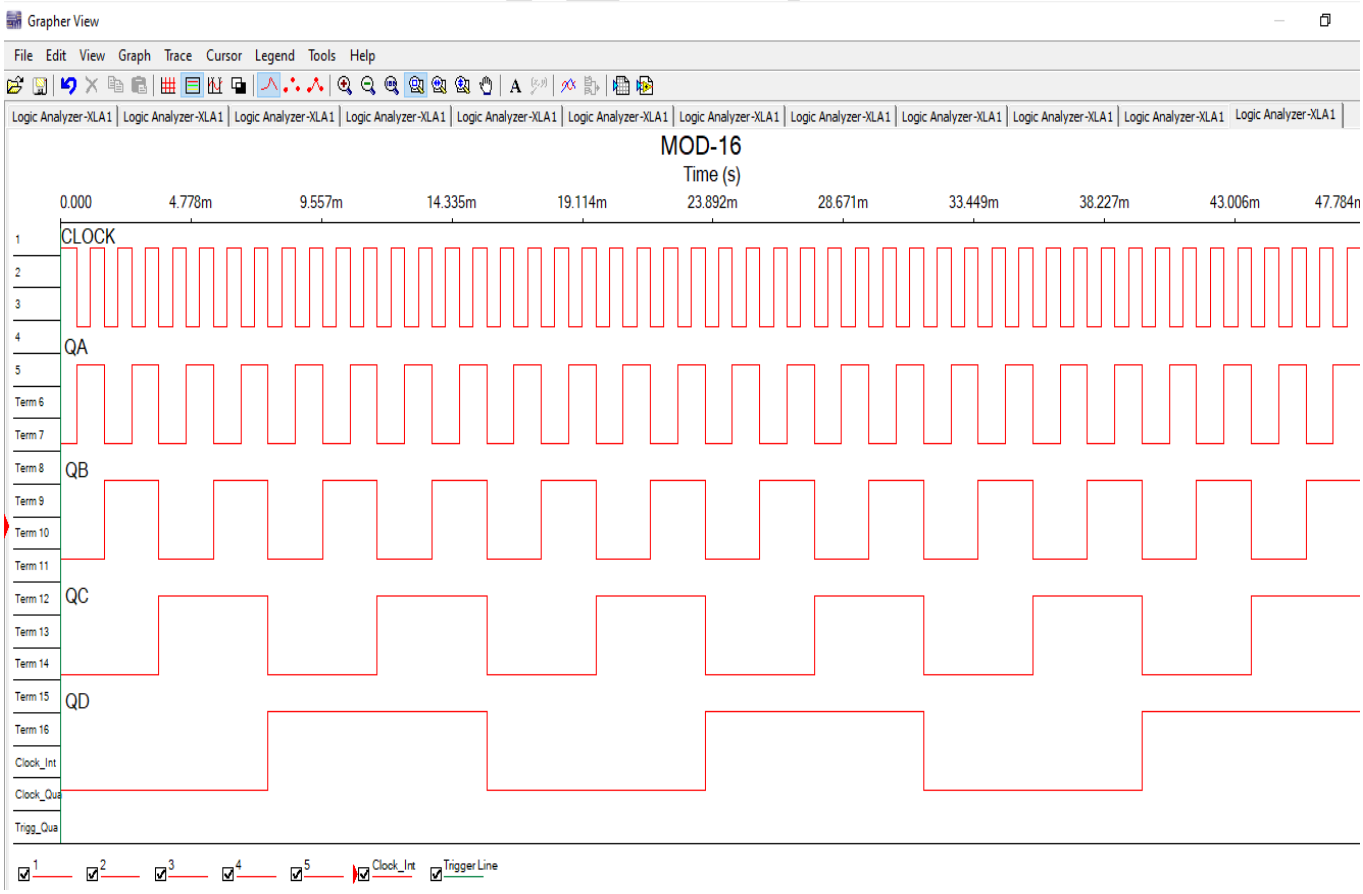


Logic Diagram: (MOD-2 /MOD-8 and MOD-16 using IC-74LS93)




U2
DCD_HEX
U1
U3
50 Hz
2
4
1
3
0
7493N
XLA1
INA
INB
R01
R02
QA
QB
QC
QD
C Q T
Param Chordiya
ROLL NO: 22119
Grapher View
File Edit View Graph Trace Cursor Legend Tools Help
MOD-8
Time (s)
-28.242µ
1.638m
3.304m
4.971m
6.637m
8.303m
9.970m
11.636m
13.302m
14.968m
CLOCK
QA
QB
QC
Clock_Int
Trigger Line

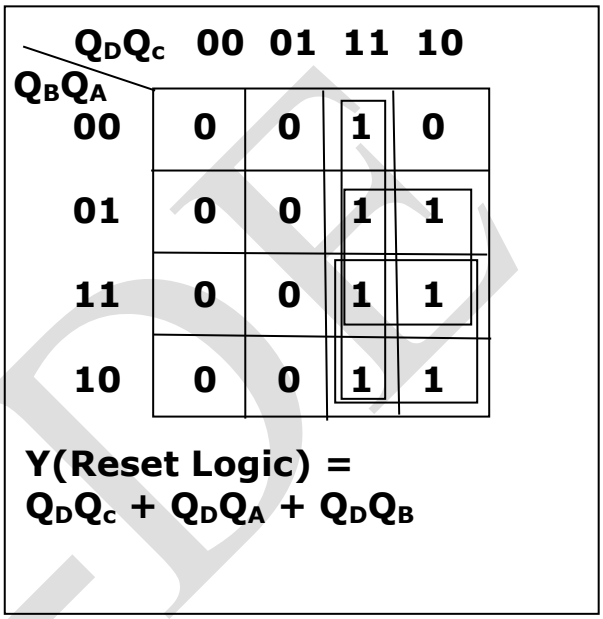

X1
X2
X3
X4
2.5 V
2.5 V
2.5 V
2.5 V
U1
U3
10 Hz
7493N
XLA1
Param Chordiya
ROLL NO: 22119
C Q T


Grapher View
File Edit View Graph Trace Cursor Legend Tools Help
MOD-16
Time (s)
0.000
4.778m
9.557m
14.335m
19.114m
23.892m
28.671m
33.449m
38.227m
43.006m
47.784m
CLOCK
QA
QB
QC
QD
Clock_Int
Trigger Line

Design of MOD-N using IC-74LS93

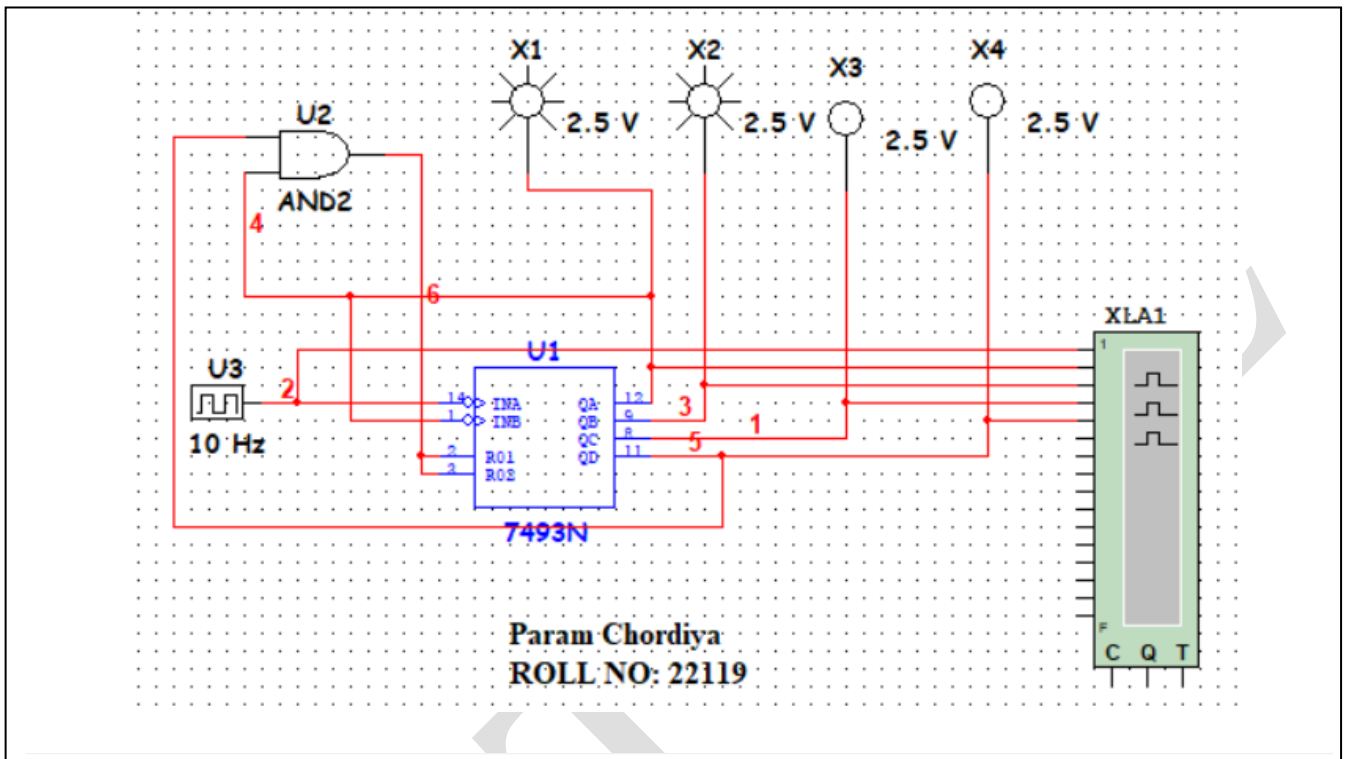
OUTPUT				RESET LOGIC
Q_D	Q_C	Q_B	Q_A	
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

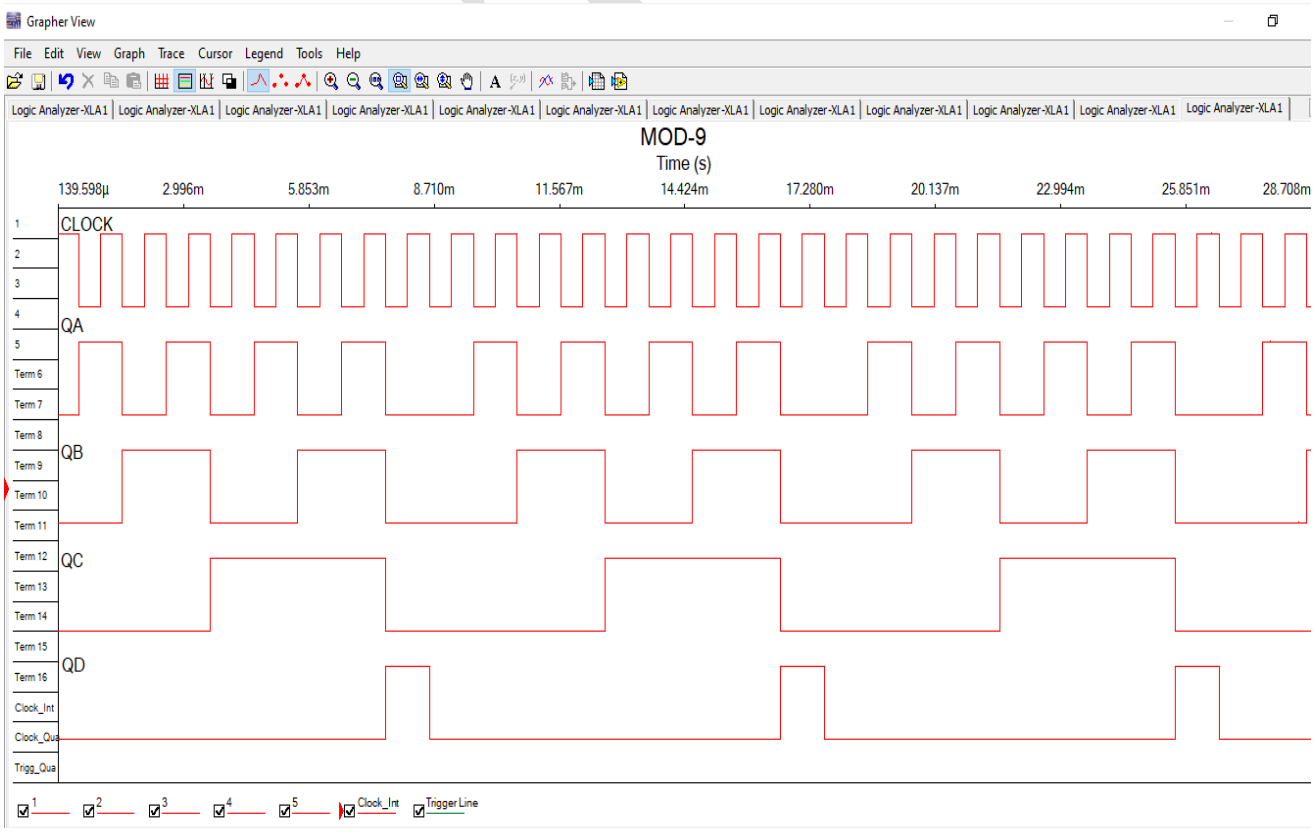
K-Map for RESET Logic



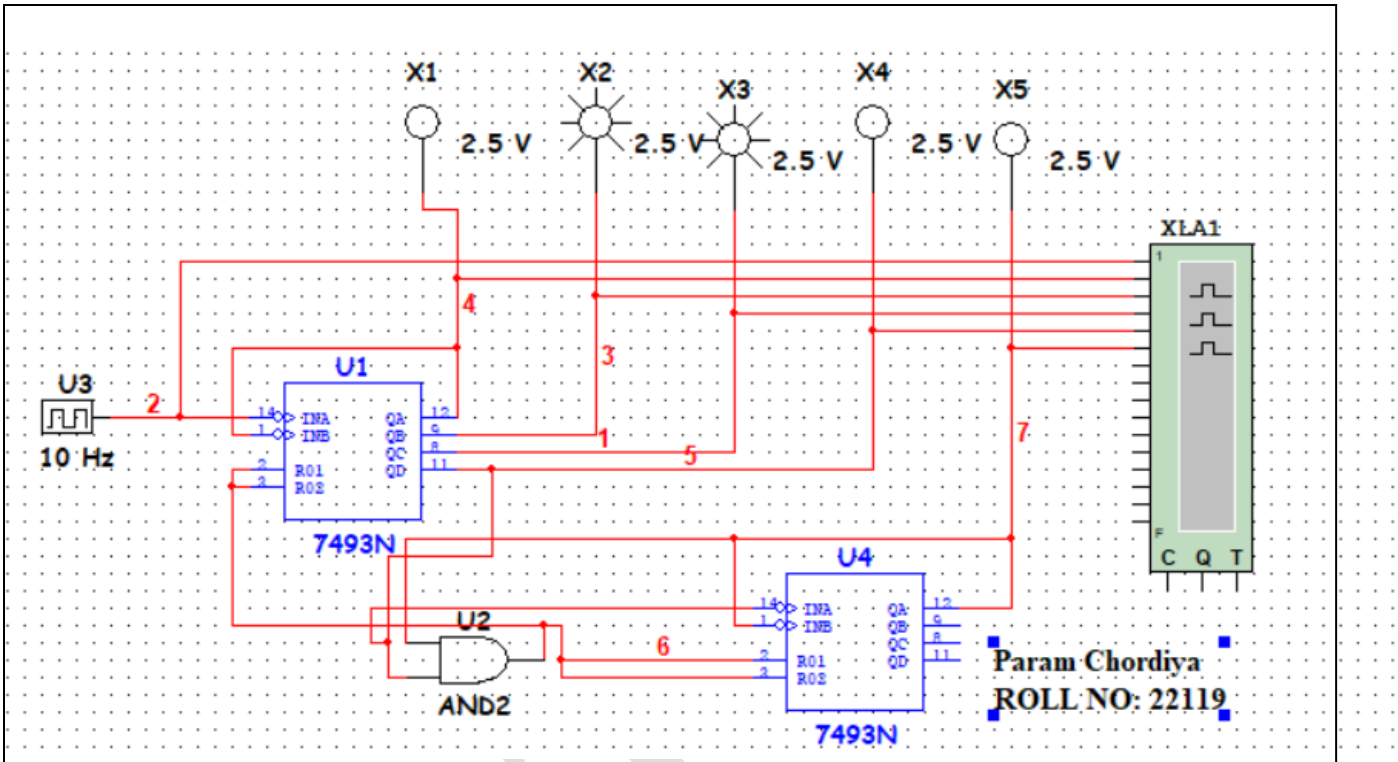
Y(Reset Logic) =
$Q_DQ_c + Q_DQ_A + Q_DQ_B$

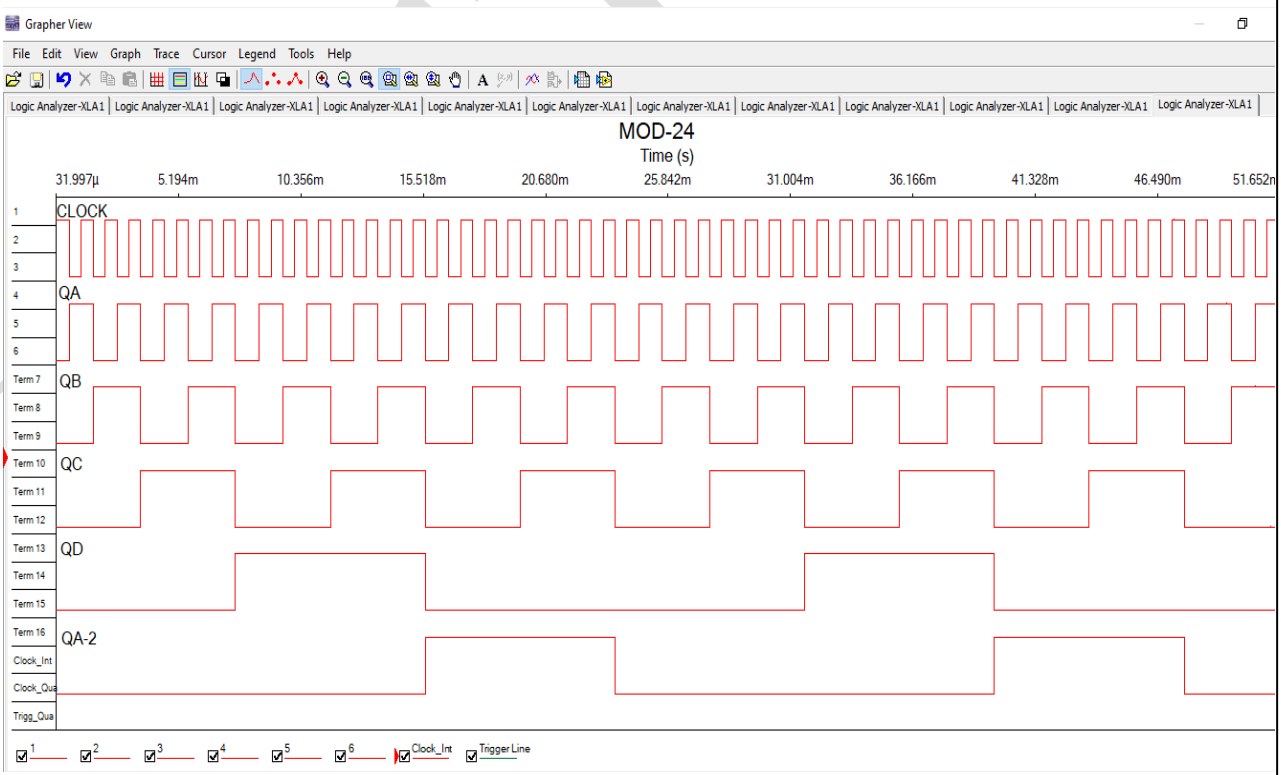
Logic Diagram: (MOD-9 using IC-74LS93)



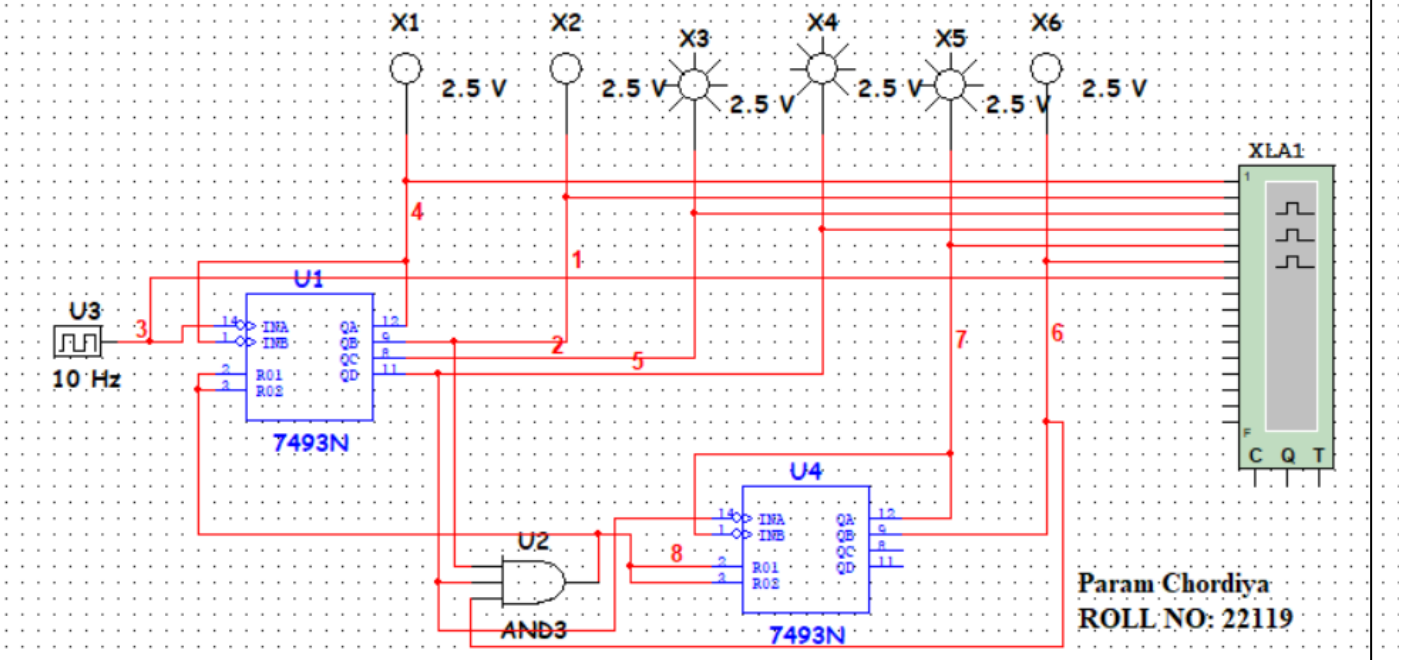


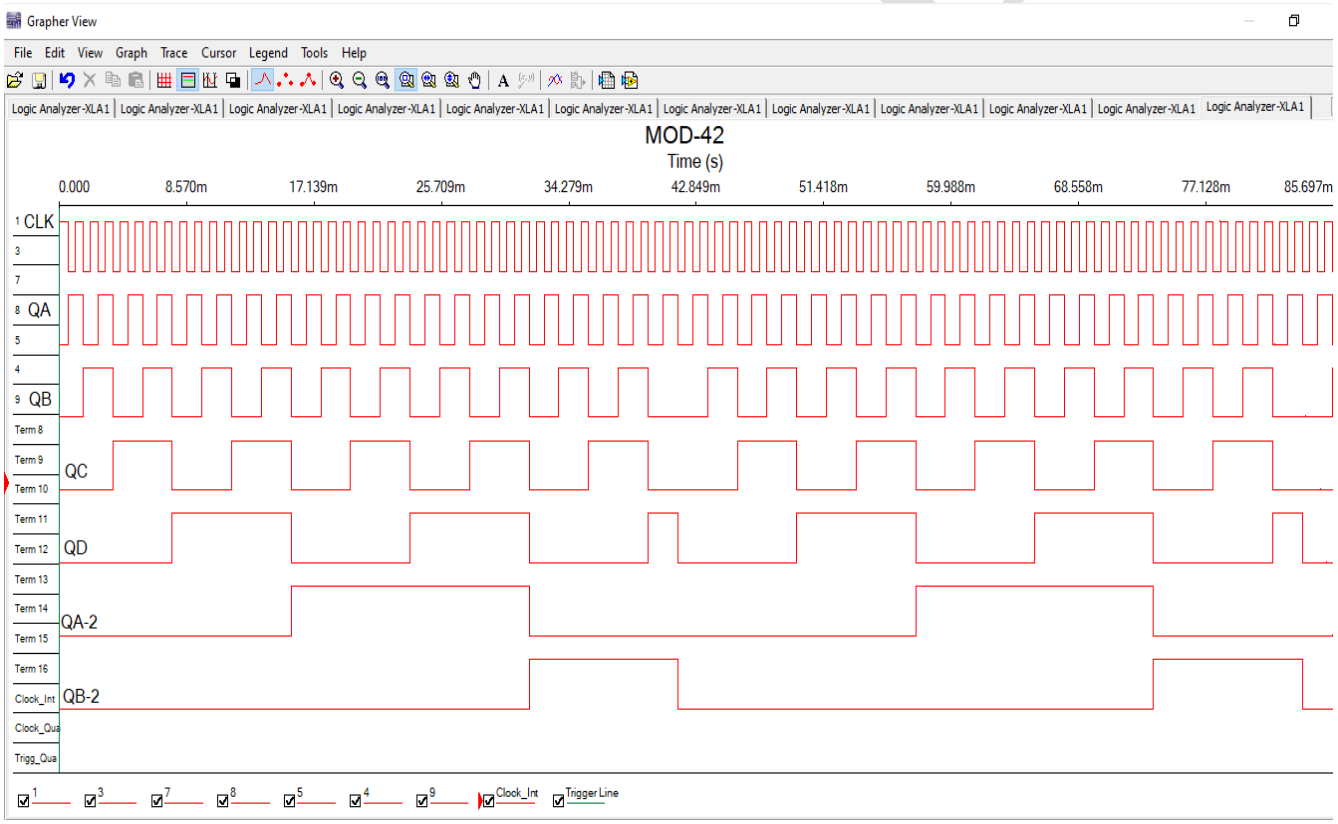
Logic Diagram: (MOD-24 using IC-74LS93)





Logic Diagram: (MOD-42 using IC-74LS93)





CONCLUSION:

Designed and Implemented MOD-2, MOD-5, MOD-10 using IC-74LS90. Drawn the Timing Diagram.

Designed and Implemented MOD-N - MOD-7 using IC-74LS90

Designed and Implemented MOD-NN - MOD-20, MOD-50, MOD-100, MOD-96, MOD-78 using IC-74LS90

Design and Implement MOD-2, MOD-8, MOD-16 using IC-74LS93. Drawn the Timing Diagram.

Design and Implement MOD-N - MOD-9 using IC-74LS93.

Designed and Implemented MOD-NN - MOD-24, MOD-42 using IC-74LS93

REFFRENCE:

1) : **R.P. Jain , "Modern digital electronics" , 3rd edition**
2) : **A. Anand Kumar, "Fundamentals of digital circuits" 1st edition**

Subject teacher Sign with Date Remark