PUNE INSTITUTE OF COMPUTER TECHNOLOGY, PUNE - 411043

Department of Electronics & Telecommunication

CLASS: S.E. E &TC **SUBJECT: DC**

EXPT. NO.: 6 **DATE :05/12/2020**

Roll No:22119

PRE-REQUISITES FOR EXPT. :

Definition of Synchronous Counter

Implementation and operation of Synchronous Counter Using IC74LS90 or IC74LS93

OBJECTIVE :

1. Design & Implement Mod-2 Counter using IC-74HC190
2. Design & Implement Mod-5 Counter using IC-74HC190
3. Design & Implement Decade Counter using IC-74HC190
4. Design & Implement Mod-20 Counter using IC-74HC190
5. Design & Implement Mod-50 Counter using IC-74HC190
6. Design & Implement Mod-100 Counter using IC-74HC190

APPARATUS :

Digital-Board, Multisim

THEORY :

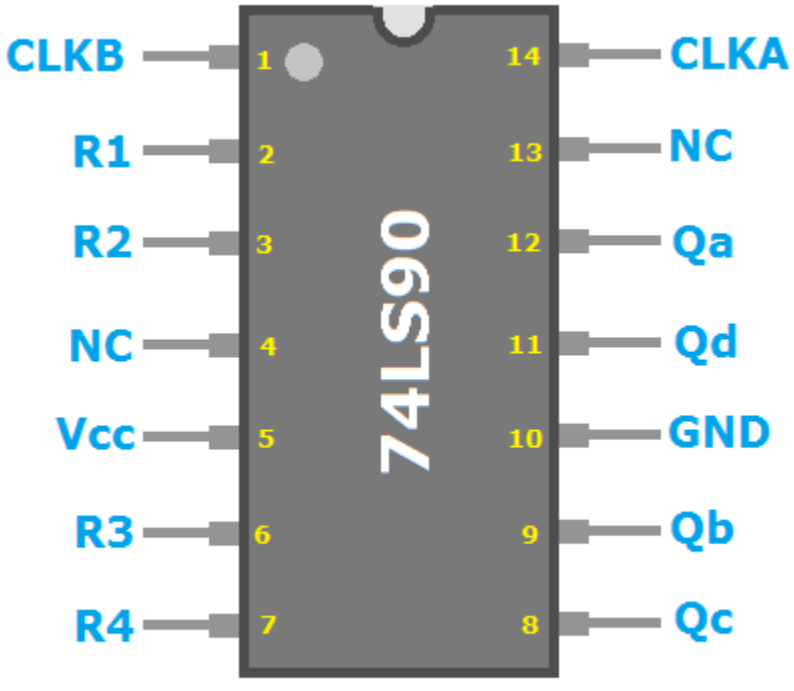
IC 74LS90 BCD counter.

Each of these monolithic counters contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-five for the DM74LS90.

All of these counters have a gated zero reset and the DM74LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade or four bit binary), the B input is connected to the QA output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the DM74LS90 counters by connecting the QD output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output QA.

PIN DIAGRAM



IC 7490 Pin Diagram

Truth Table:

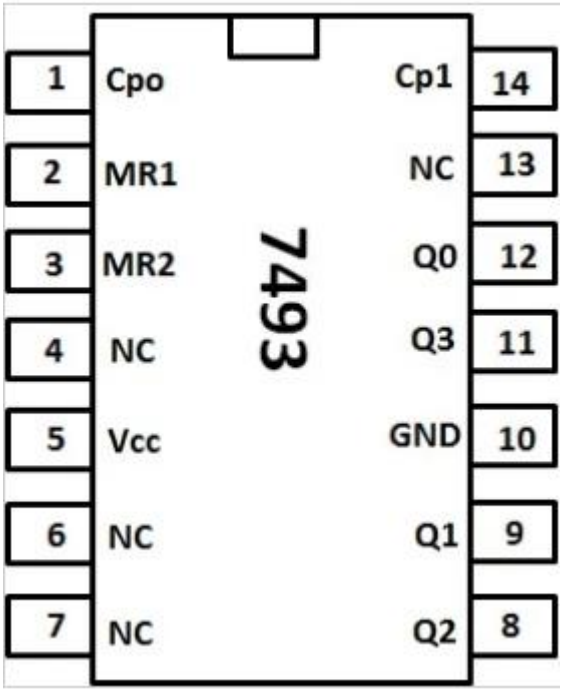
Count	Qd	Qc	Qb	Qa
(Start) 0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
(New Cycle) 10	0	0	0	0

IC 7490 Truth Table

IC 74LS93 – 4 Bit Binary Counter

The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to CP) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

PIN DIAGRAM



TRUTH Table :

LS93
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

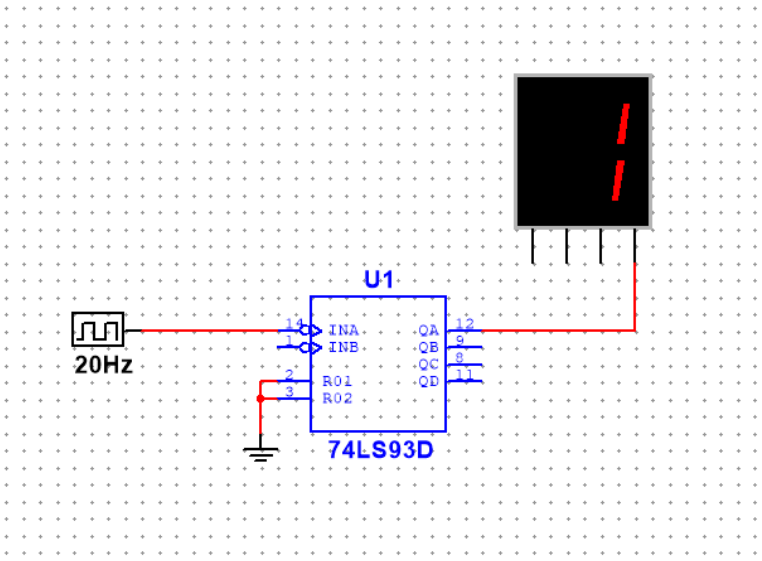
PROCEDURE :

1. Make the connections as per the logic circuit of Mod-2 Counter, Mod-5 Counter, Mod-20 Counter, Mod-50 Counter, Mod-100 Counter

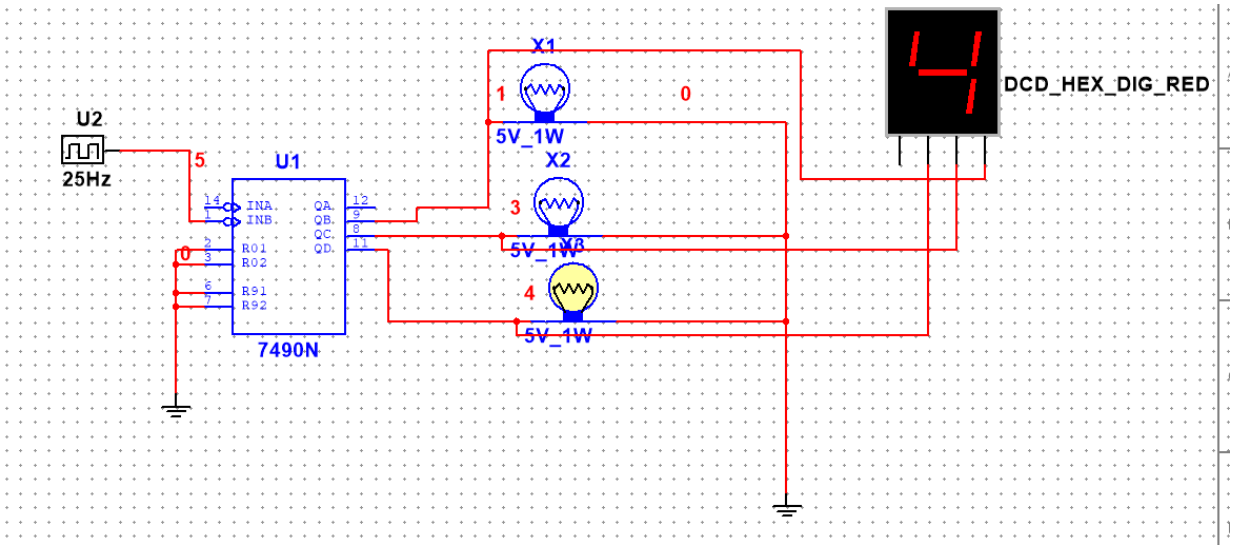
2.Make the connections as per the logic circuit of Decade Counter &

Verify the truth table of IC7490.

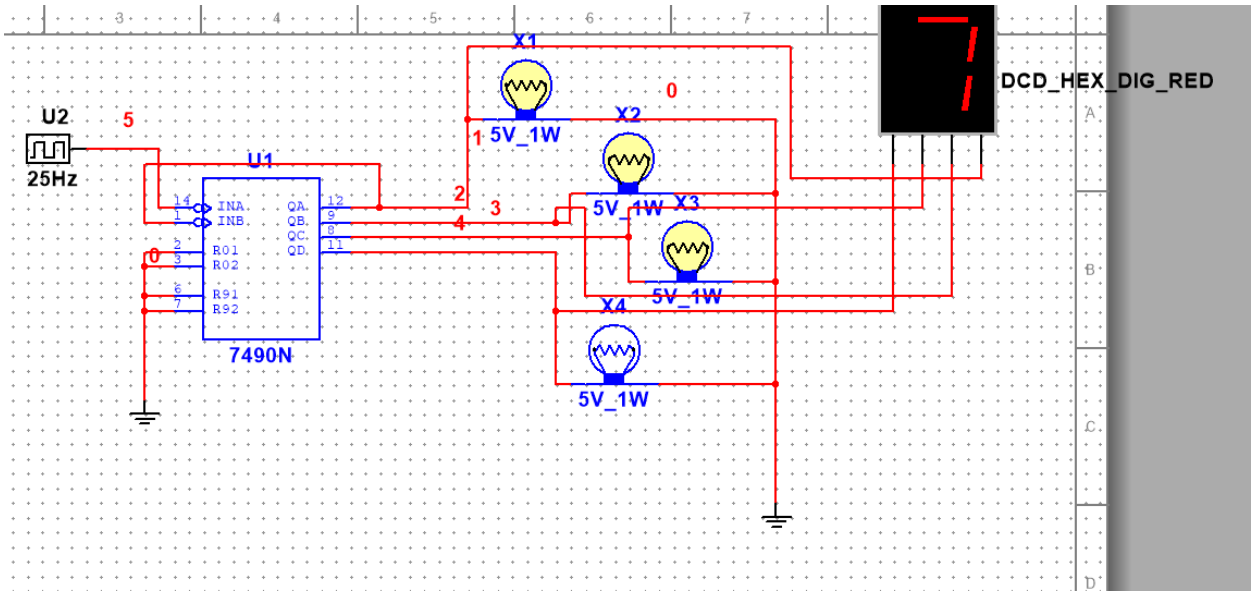
Design & implement of Mod-2 counter



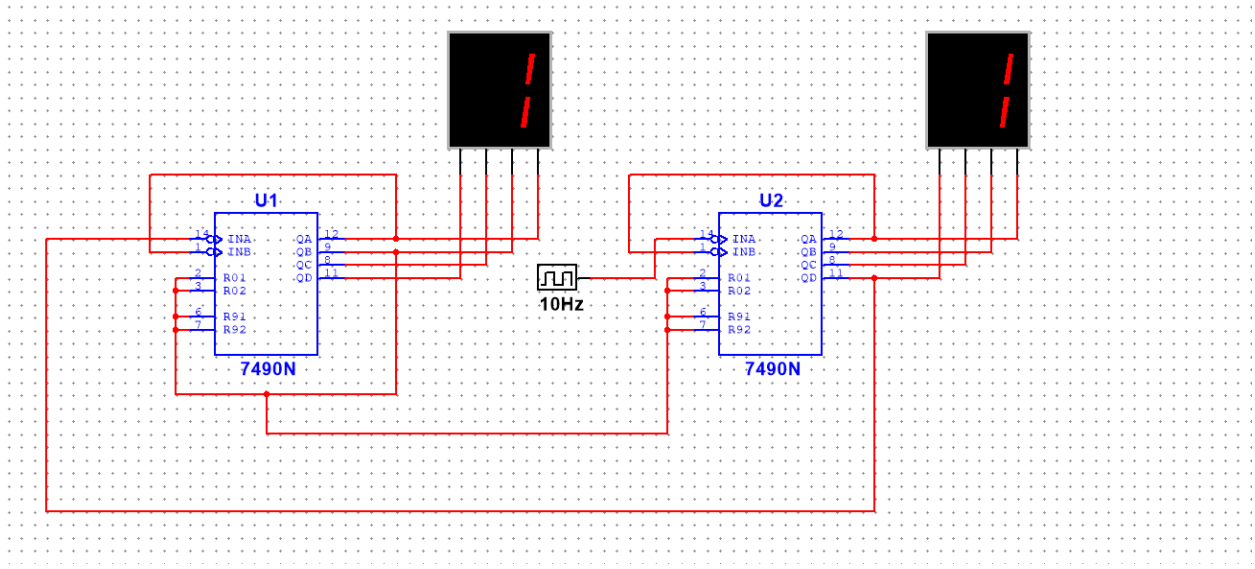
Design & implement of Mod-5 counter



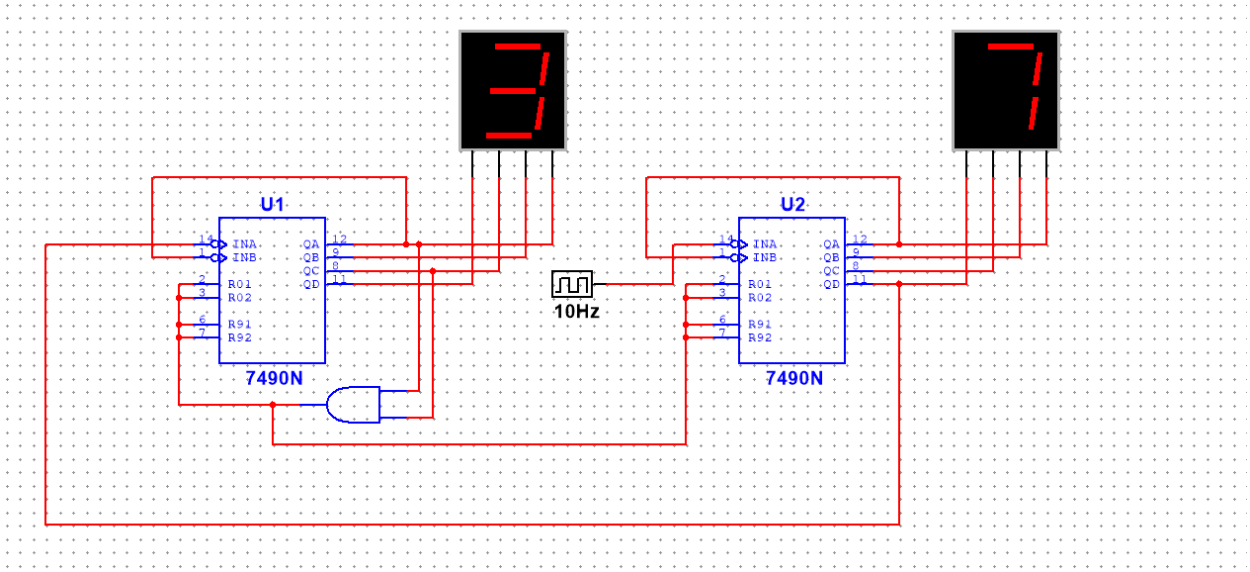
Design & implement of Decade counter



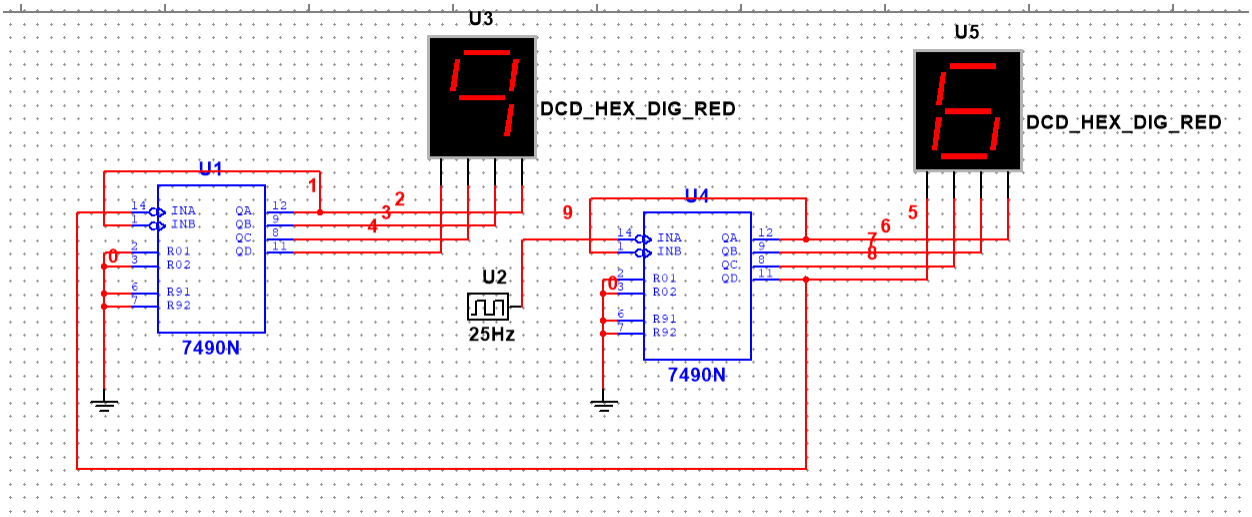
Design & implement of Mod-20 counter



Design & implement of Mod-50 counter



Design & implement of Mod-100 counter



CONCLUSION:

1. We learnt pin configuration & Truth table of IC 74LS90 & IC74LS93.
2. We implement Mod-n counters.
3. We also verified the truth table of IC 74LS90

REFFRENCE:

1) : R.P. Jain, "Modern digital electronics", 3rd edition

2) : A. Anand Kumar, "Fundamentals of digital circuits" 1st edition

Subject teacher Sign with Date Remark