CLASS: S.E. E &TC **SUBJECT: DC**

EXPT. NO.: 5 **DATE: 05/12/2020**

ROLL NO: 22119

TITLE : Study of Counter using J-K Flip-flop

PRE-REQUISITES FOR EXPT. :

Definition of Synchronous Counter

Implementation and operation of Counter Using J-K Flip-Flop

(Refer Data-Sheet)

OBJECTIVE :

1. Design & Implement 4-bit Up-Counter using J-K Flip-Flop
2. Design & Implement 4-bit Down Counter using J-K Flip-Flop
3. Design & Implement 4-bit UP/Down Counter using J-K Flip-Flop
4. MOD-N Up Counter and MOD N down counter using J-K Flip-Flop Draw the Timing Diagram.

APPARATUS :

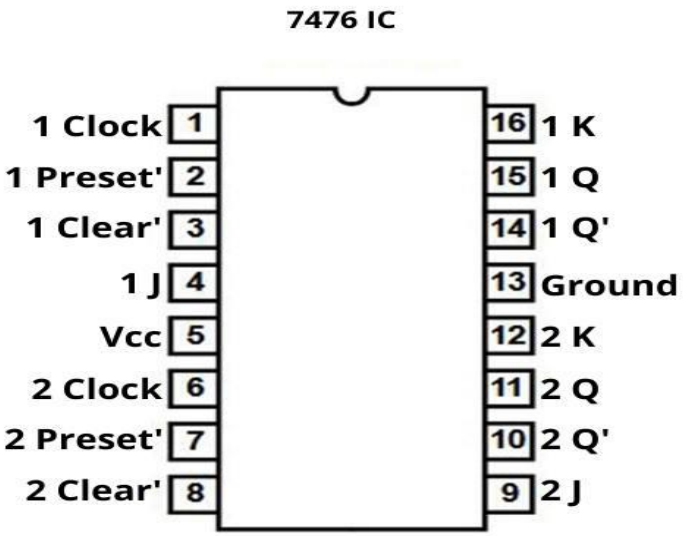
Digital-Board, GP-4Patch-Cords, IC-74LS86,IC-7476N.

THEORY :

The **SN7476** is a **dual in-line JK flip flop IC**, i.e. it has two JK flip flops inside it and each can be used individually based on our application. The JK flip flops are considered to be the most efficient flip-flop and can be used for certain applications on its own. The flip-flops are also called as latching devices meaning it can remember one single bit

of data and latch the output based on it, due to this property they are commonly used as shift registers, control registers, storage registers or where ever a small memory is required.

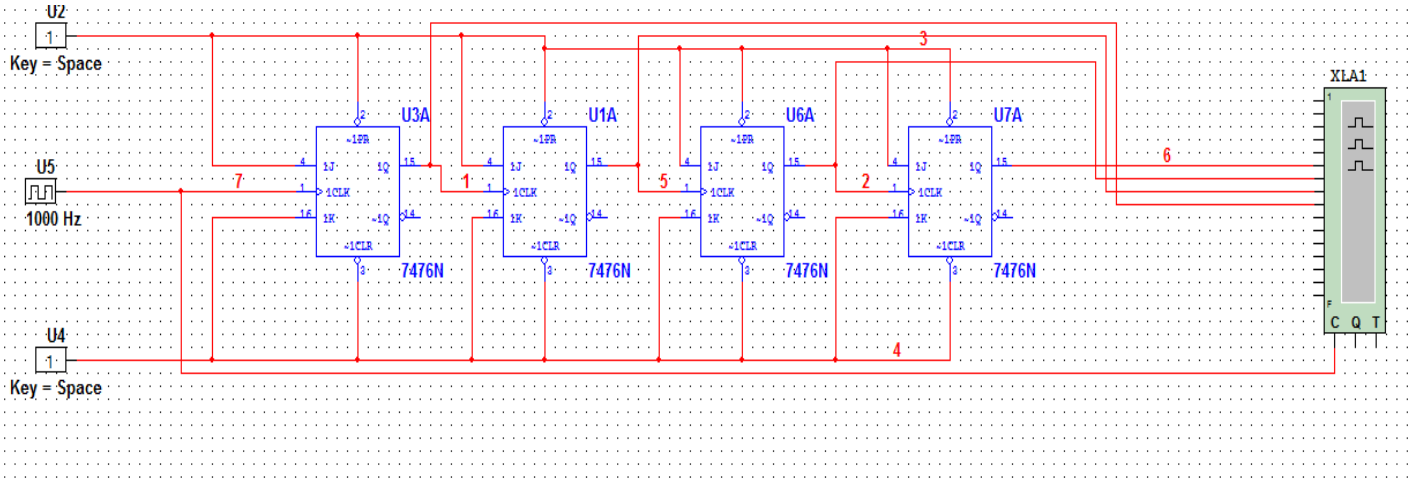
PIN Diagram:



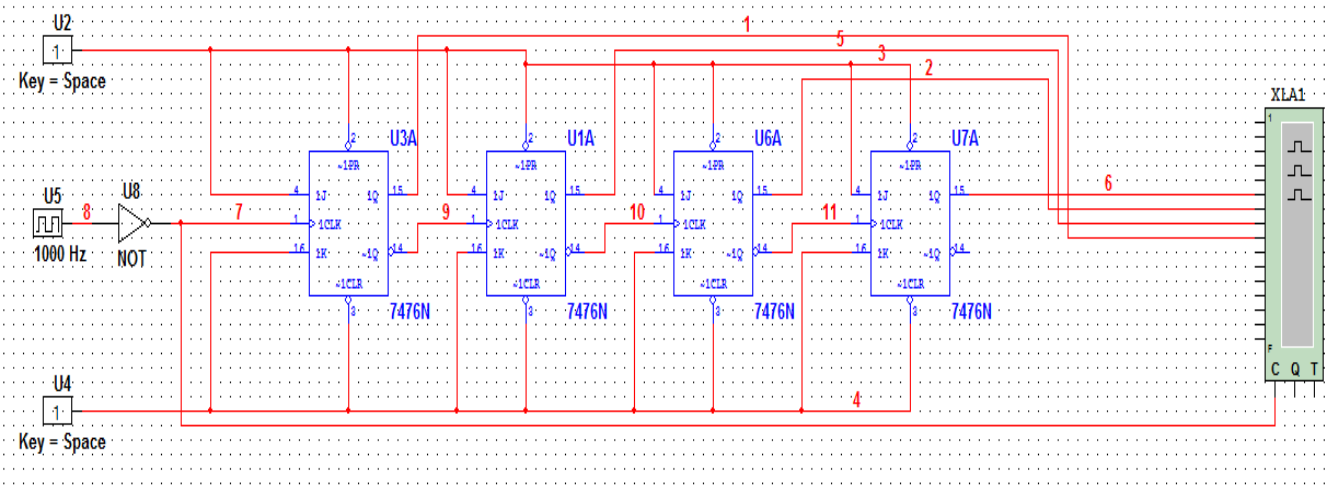
PROCEDURE :

1. Make the connections as per the Logic circuit of 4-bit Up-Counter, 4-bit Down-Counter, MOD- N up counter and MOD-N down counter using J-K Flip-flop and Verify its state Table.

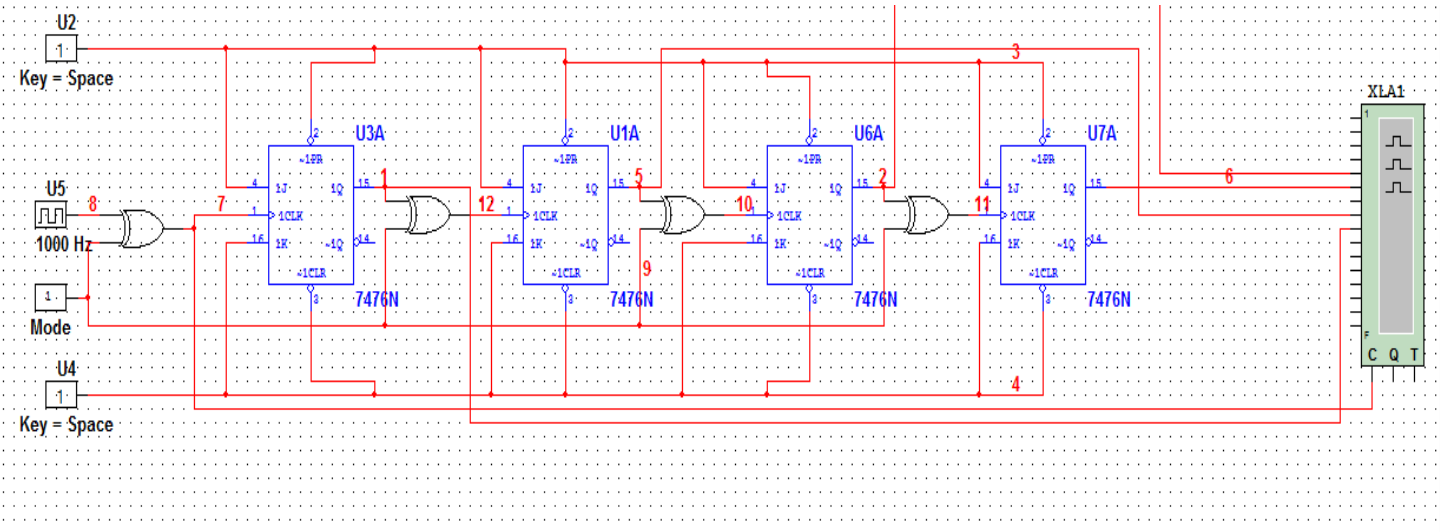
Logic Diagram: (4-bit Up-Counter using J-K Flip-flop):



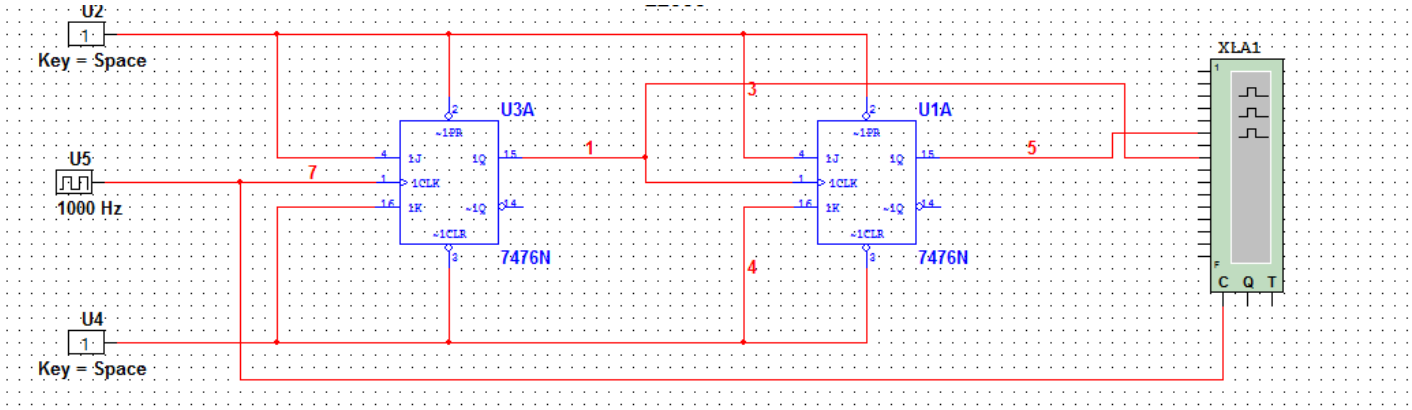
Logic Diagram: (4-bit Down-Counter using J-K Flip-flop):



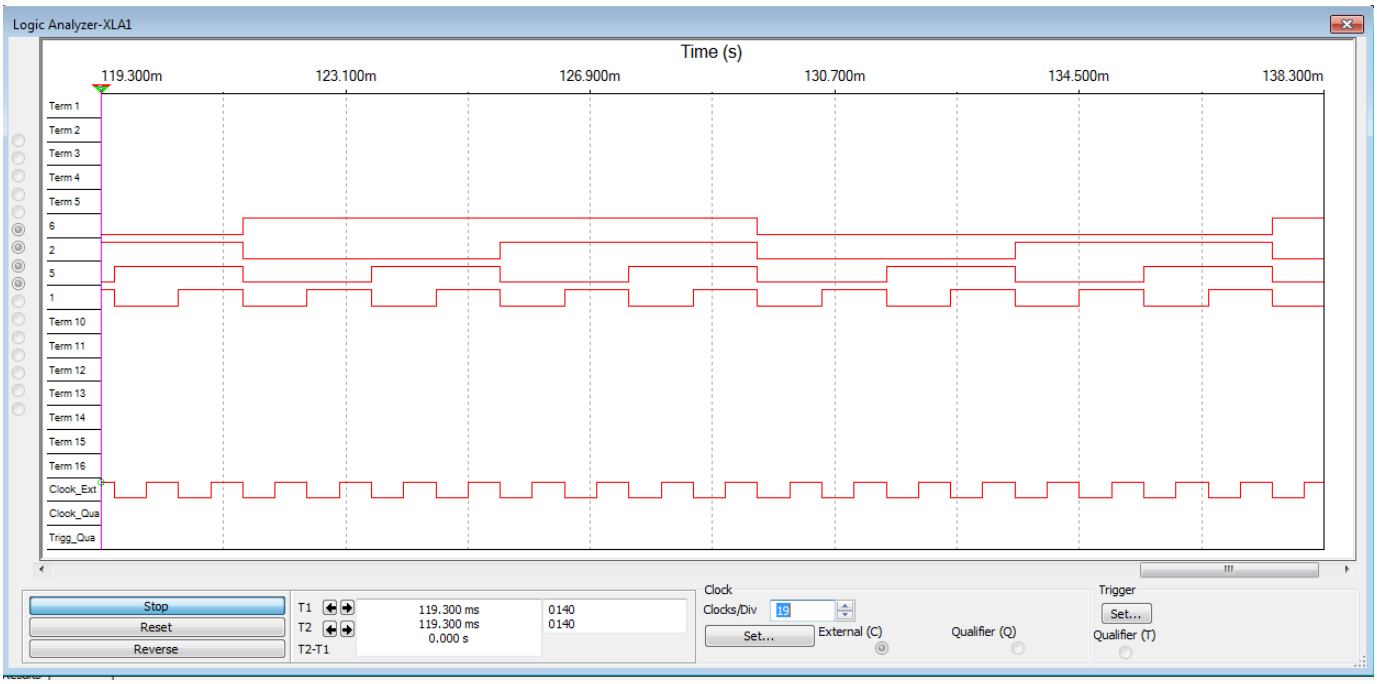
Design & Implement UP/DOWN counter using J-K Flip-flop:



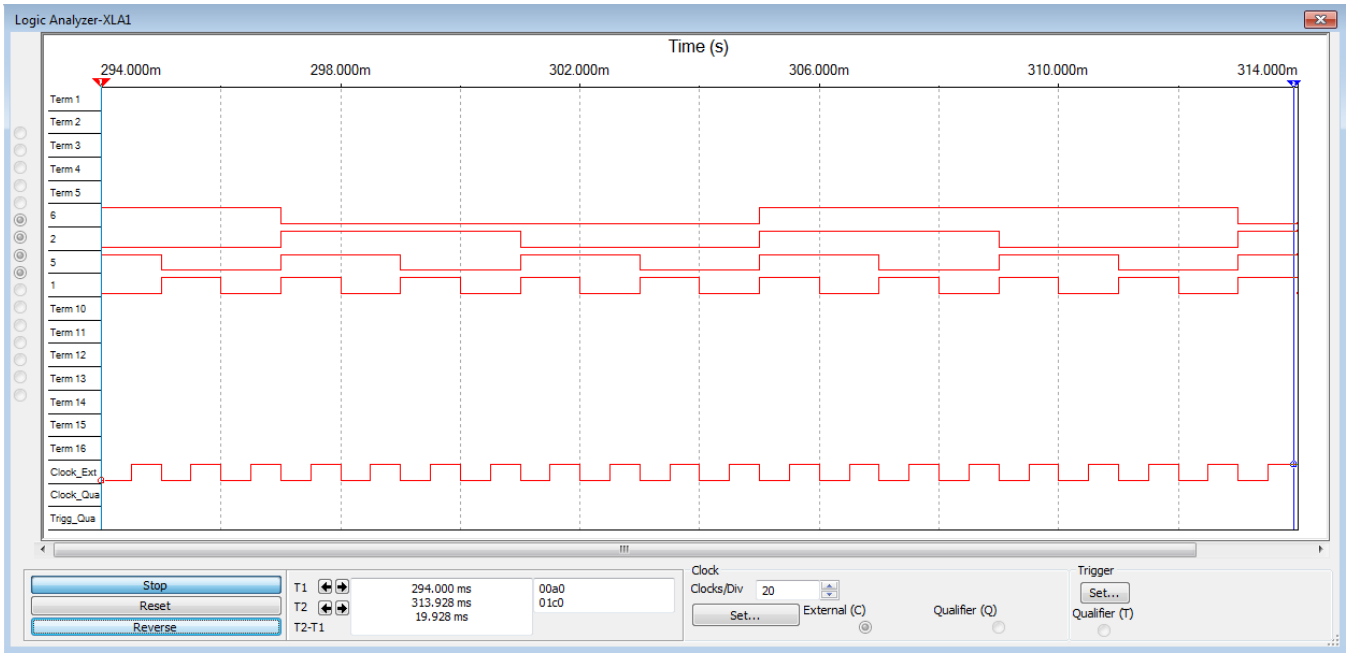
Logic Diagram: (N-bit Up-Counter using J-K Flip-flop):
(2-bit Up-Counter using J-K Flip-flop):



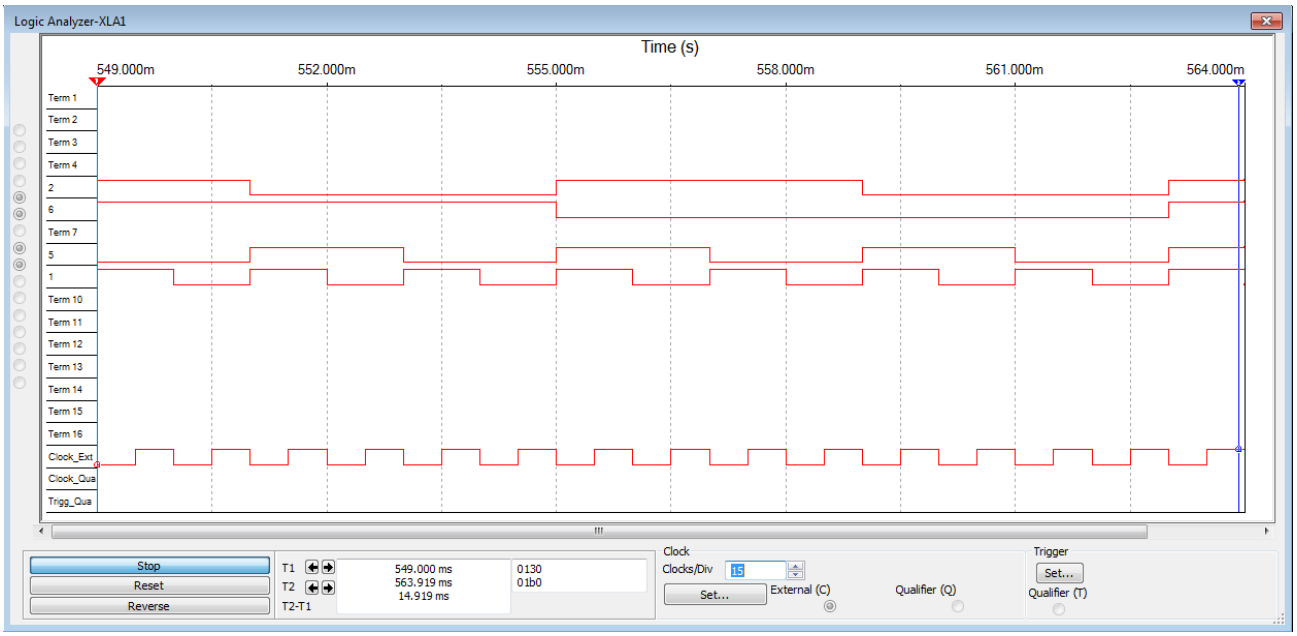
GRAPHS: Draw all timing diagrams on graph paper



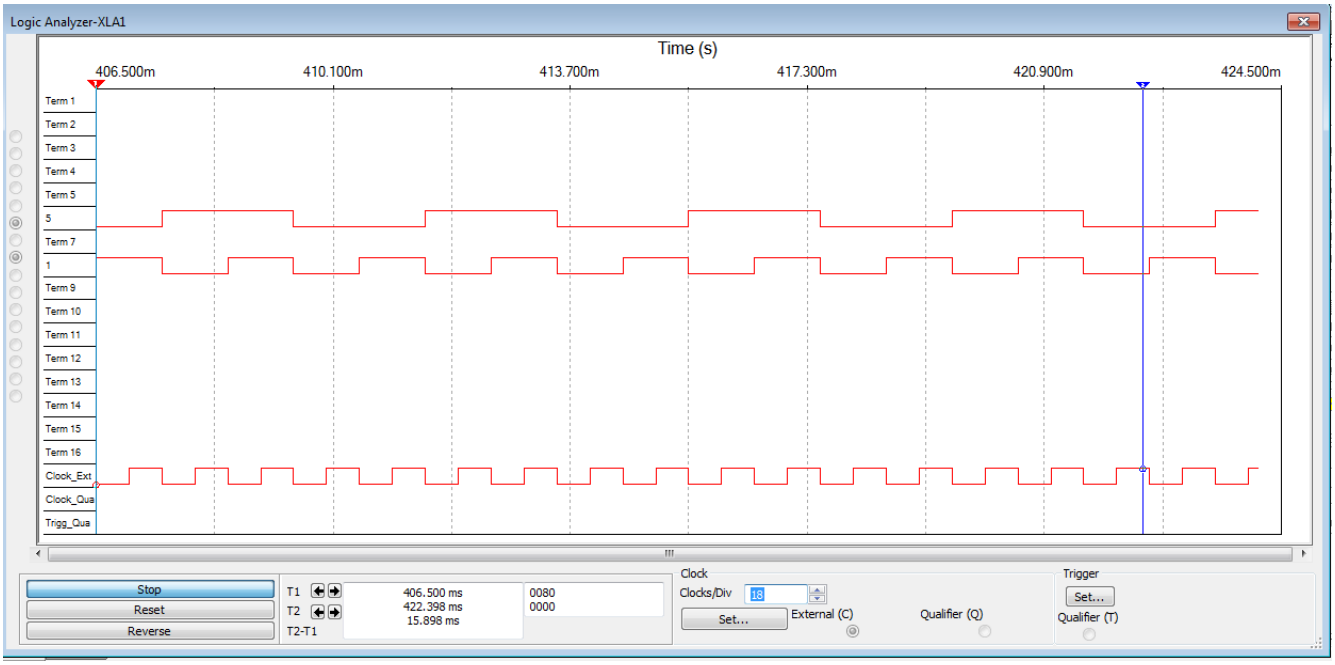
(a) 4-bit Up Counter



(b) 4-bit Down Counter



(c) 4-bit Up/Down Counter



(d) 2-Bit counter

CONCLUSION:

We have designed and implemented 4-bit Up-Counter using J-K FLIP-FLOP

Also we have designed and implemented 4-bit up/Down Counter using

J-K FLIP-FLOP.

We have implemented 4-bit UP/Down Counter using J-K FLIP-FLOP

We have designed and implemented N-Counter(2-Bit UP counter) counter using J-K FLIP-FLOP

REFFRENCE:

1) : R.P. Jain , "Modern digital electronics" , 3rd edition

2) : A. Anand Kumar, "Fundamentals of digital circuits" 1st edition

Subject teacher Sign with Date Remark