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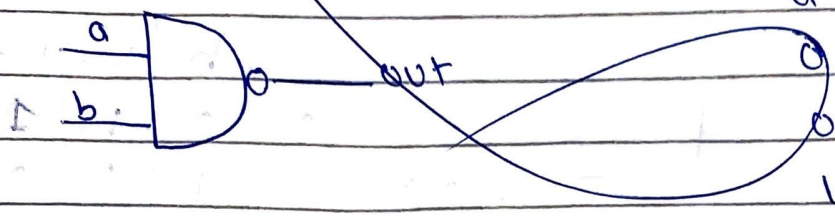
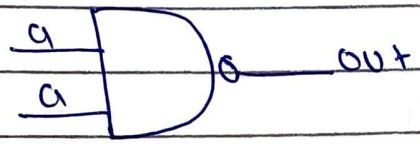
NOT Gate



a	b	out
0	0	
0	1	
1	0	
1	1	

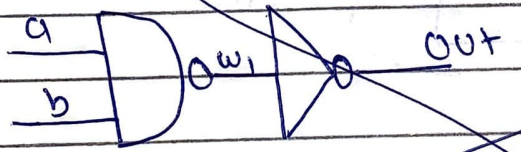
NOT Gate ($Y = \bar{a}$)



using Nand

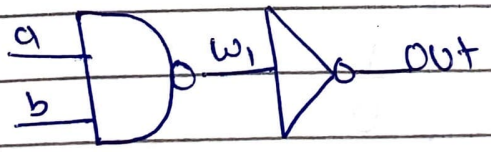
a	a	out
0	0	1
1	1	0

AND Gate



a	b	w_1	out
0	0	0	
0	1	0	
1	0	0	
1	1	1	

AND Gate ($Y = a \cdot b$)



a	b	w_1	out
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

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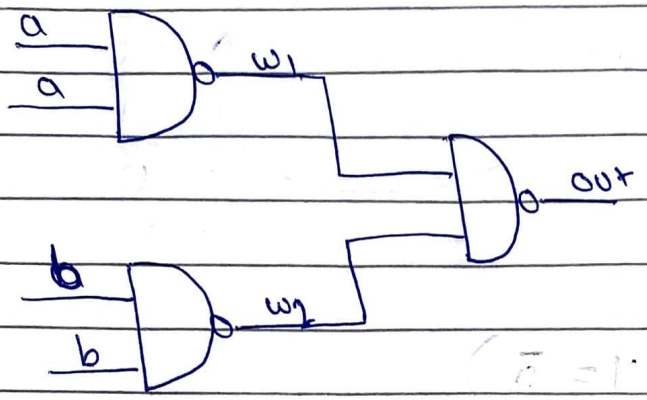
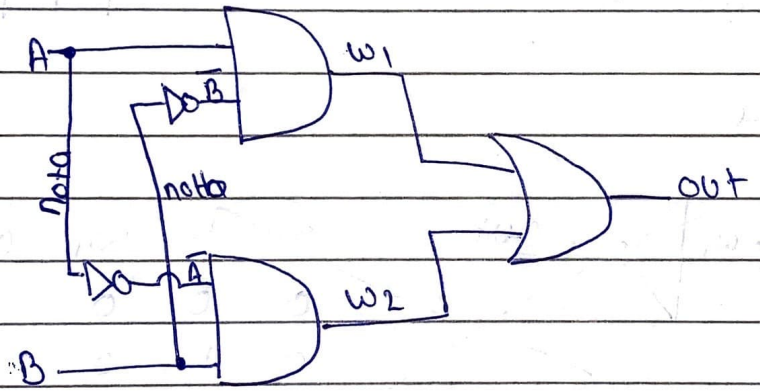
OR gate ($y = a + b$)



a	b	w_1	w_2	out
0	0	1	0	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

XOR gate ($y = A\bar{B} + \bar{A}B$)



$A\ \bar{A}$	$B\ \bar{B}$	w_1	w_2	out
0 1	0 1	0	0	0
0 1	1 0	0	1	1
1 0	0 1	1	0	1
1 0	1 0	0	0	0

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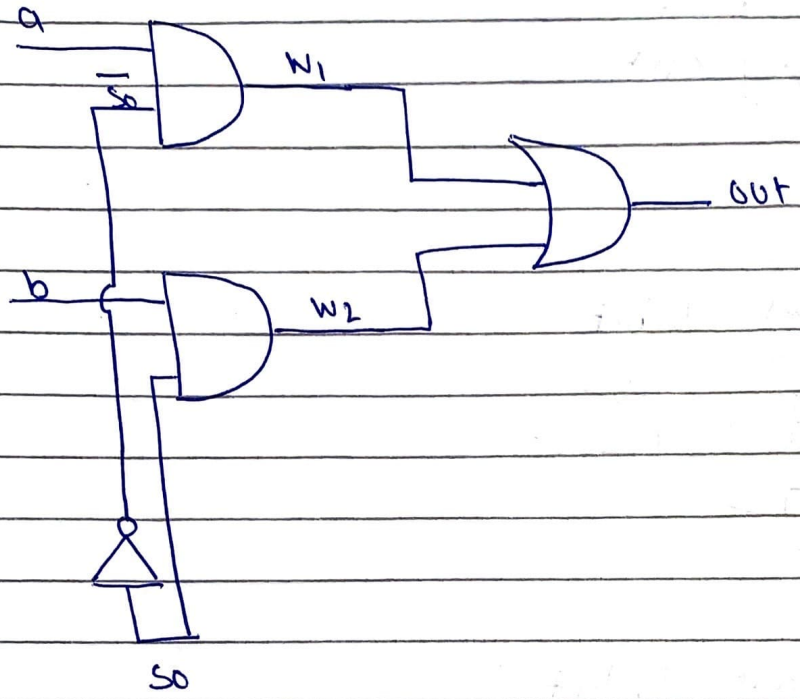
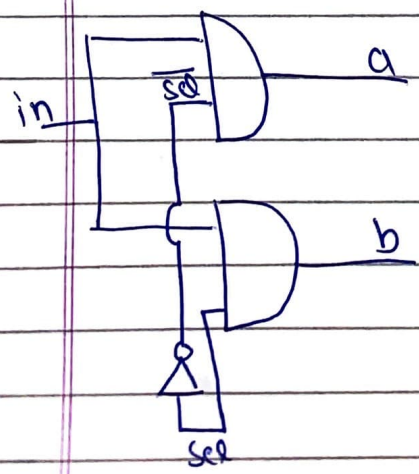
MUX ($y = \bar{s}_0 a + s_0 b$)



s_0	a	b	out
0	1	0	1
1	0	1	1
0	0	1	0
1	1	0	0

DMUX ($a = \overline{sel} \cdot in$, $b = sel \cdot in$)



sel	in	a	b
0	1	1	0
1	0	0	1

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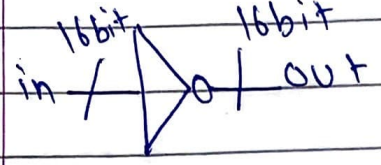
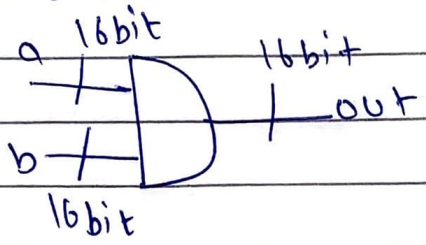
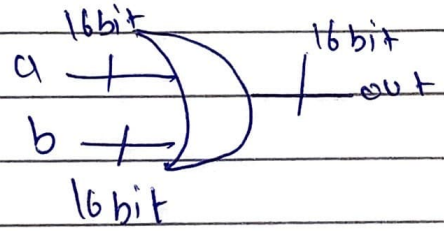
NOT Gate 16-bit



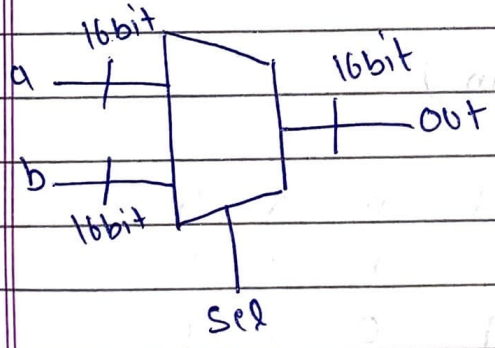
AND Gate 16 bit



OR Gate 16 bit



MUX 16 bit



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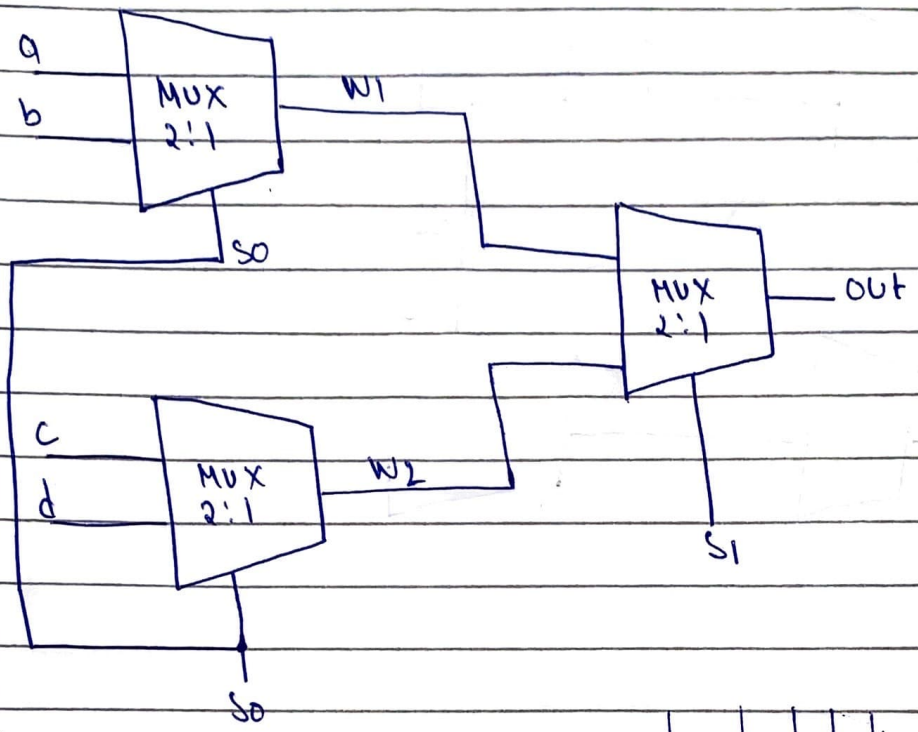
MUX 4:1 16 bit

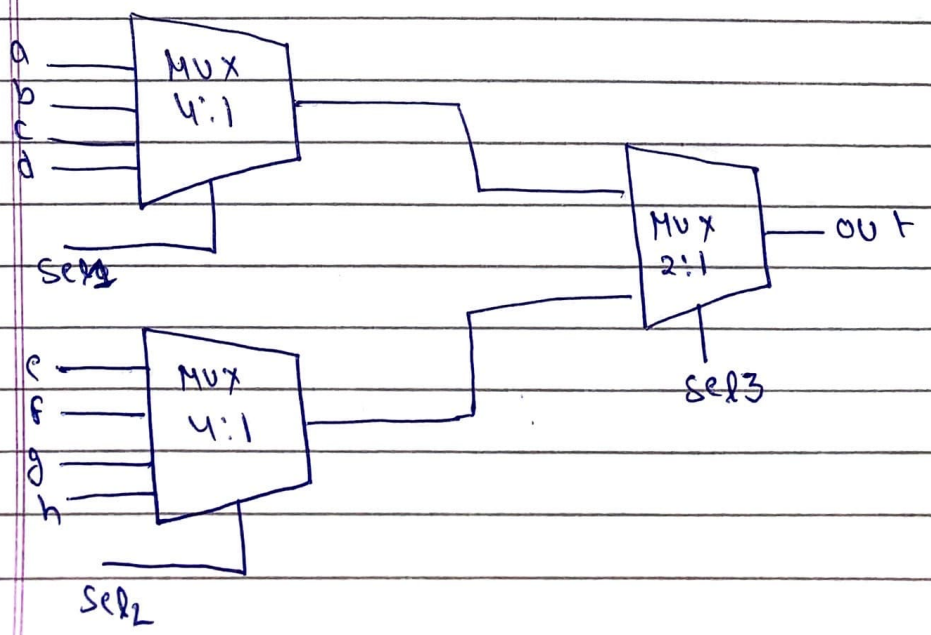


$Out = \bar{S_0}\bar{S_1}a + \bar{S_0}S_1b + S_0\bar{S_1}c + S_0S_1d$

$= \bar{S_0}(\bar{S_1}a + S_1b) + S_0(\bar{S_1}c + S_1d)$

S_0	S_1	a	b	c	d	out
0	0	1	0	0	0	a
0	1	0	1	0	0	b
1	0	0	0	1	0	c
1	1	0	0	0	1	d

MUX 8:1 16 bit



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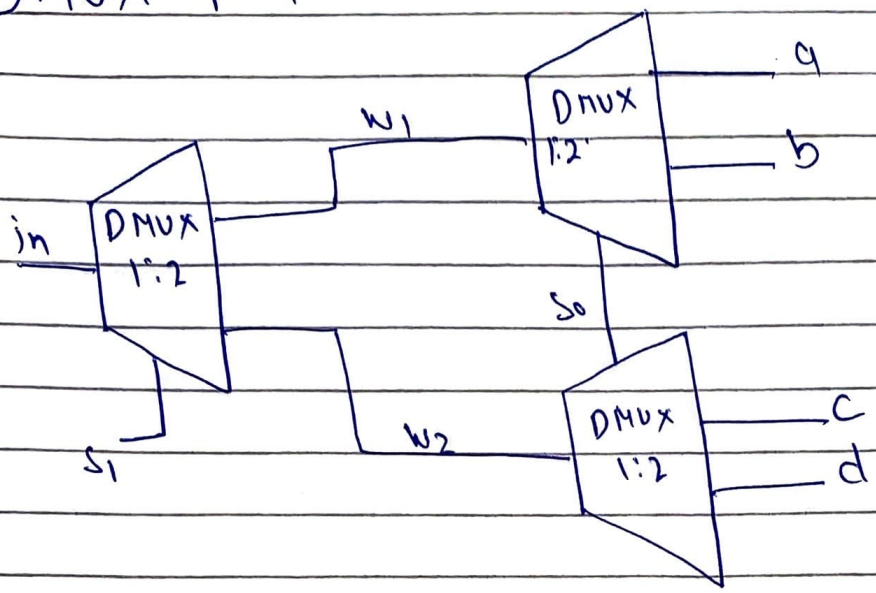
DMUX 1:4



DMUX 1:8