Parastoo Kamranfar

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Summary

More than 3 years of professional experience in IT industry coming from an engineering background worked as a researcher and teaching assistant. Pursuing computer science and algorithms techniques as of 2017 in PhD computer science major, to expand my academic experience starting as a Java graduate teaching assistant and continued as Python GTA. Always adaptive to learn new languages and project's requirements at my own pace in very little time. Have had experience in Telecom industry and workflow. Interested in data science, machine learning algorithms and Java application development. Currently on student visa.

Education

PhD Computer Science – Jan. 2017 – Present

- George Mason University, Fairfax, VA

M.S. Computer Architecture Engineering - Feb. 2010-Sep. 2012

- University of Tehran and Islamic Azad University, Sciences and Research Branch, Tehran, Iran
- Project Title: A Primitive Set of Configurable Processing Elements for System Level Design
- GPA: 19.24 out of 20

B.S. Computer Engineering – Hardware - Sep. 2004–Sep. 2008

- Islamic Azad University South Tehran Branch, Tehran, Iran
- Project Title: Designing and Manufacturing of Automated Test Equipment (ATE) for electronic circuit boards
- GPA: 17.39 out of 20

Professional Experience

ITS Quality Assurance Engineer, MTN Irancell, Tehran, Iran (Nov. 2014 – Dec. 2016**)**

- To ensure end to end channel and product accountability and the implementation of sales and service processes for all Information Technology Systems (ITS) projects
- Closely working with customer on ITIL practices using Marval ticketing system

ITS Project Office Administrator, MTN Irancell, Tehran, Iran (Aug. 2013 – Nov. 2014)

- To assist and coordinate the administrative activities related to project management and Vendor management
- Conducting and managing some ITS projects by means of Microsoft Project Server
- Direct report to CIO

Research Assistant, CAD Research Group, University of Tehran, Iran (Feb. 2010 – Sep. 2016)

- Designing and implementing an out of order execution processor using Verilog language and ModelSim, Quartus II, SoPC Builder, and NIOS II tools

- "An Environment for ESL Synthesis" project, funded by Microelectronics Committee using SystemC (TLM, RTL) language and CatapultC tool

Researcher, Mi'ad San'atgaran Co., Tehran, Iran (Jul. 2008–Jun. 2009)

- Designing and manufacturing of electronic circuit boards using Cadence Pspice, Protel DXP

Network Administrator Intern, Sanan Shimi Co., Tehran, Iran (Aug. 2008- Oct. 2008)

- Network administrative tasks
- Active directory configurations
- Helpdesk support

Teaching Experience

Aug. 2018 – present - Teaching Assistant, CS Department, George Mason University, USA

- Intro Computer Programming (Python), Responsible for leading Lab sessions, grading computer assignments, grading exams and also answering students' questions

Jan. 2018 – May 2018 - Teaching Assistant, CS Department, George Mason University, USA

- Computer Systems and Programming, Responsible for leading Lab sessions, grading computer assignments, grading exams and also answering students' questions

Jan. 2017 – Dec. 2017 - Teaching Assistant, CS Department, George Mason University, USA

- Object Oriented Programming (Java), Responsible for leading Lab sessions, grading computer assignments, grading exams and also answering students' questions

Sep. 2011- Jun. 2013 (4 semesters) - Teaching Assistant, ECE Department, University of Tehran, Iran

- Digital Logic Design, Responsible for grading computer assignments, grading exams and also answering students' questions

Publications

- **Conference Papers**

  [1] **P. Kamranfar**, A. Shahabi, Gh. Vaghbakht and Z. Navabi , "Configurable Systolic Matrix Multiplication," *27th International Conference on VLSI Design and 13th International Conference on Embedded Systems,* Mumbai, January, *2014*.

  [2] F. Javaheri, M. Namaki-Shoushtari, **P. Kamranfar**, and Z .Navabi, "Mapping Transaction Level Faults to Stuck-at Faults in Communication Hardware," *In Proc. Of 20th Asian Test Symposium 2011 (ATS'11),* New Delhi, November, *2011*.

- **University Booth**

  R. Jafari, Gh. Vazhbakht, **P. Kamranfar**, R. Namazian, M. Saffarpour, S. Sadeghi-kohan, Z. Navabi "Synthesizing Abstract Communications to RTL Standard Structures," University Booth of University of Tehran, Design, *Automation and Test in Europe Conference (DATE'13)*, France, March 2013.

Presentation

- "Configurable Systolic Matrix Multiplication," *27th International Conference on VLSI Design and 13th International Conference on Embedded Systems,* Mumbai, January, 2014.

Computer Skills

Programming languages: C/C++, Java, Python, Lisp, MIPS, Assembly (8051, Z80, 8086)
Data base: SQL
Hardware Description Languages: Verilog, VHDL, SystemC (TLM, RTL)
FPGA Tools: Altera Design Package (Quartus II, ModelSim, SoPC Builder and NIOS II), Xilinx Design Suit

EDA Tools: Mentor ModelSim, Cadence Pspice, Protel DXP
Operating Systems: Windows, Linux

Honors and Awards

- Ranked first among 20 MSc students
- Ranked top three among 88 BS students
- Best employee of 2014 at MTN Irancell
- Best employee of December 2015 at MTN Irancell