An Embedded Framework for EEG-Based Neurophysiological Data Acquisition to Support ADHD Monitoring

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Marco Integrado para la Adquisición de Datos Neurofisiológicos Basados en EEG para Apoyar la Monitorización del TDAH

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Declaración

Me permito afirmar que he realizado esta tesis de manera autónoma y con la única ayuda de los medios permitidos. Todos los pasajes que se han tomado de manera textual o figurativa de textos publicados y no publicados, los he reconocido en el presente trabajo. Ninguna parte del presente trabajo se ha empleado en ningún otro tipo de tesis.

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1 Preliminaries

1.1 Motivation

Brain–Computer Interfaces (BCI) have emerged as a powerful class of technologies that enable direct communication between the brain and external devices. These systems are increasingly being applied in neurorehabilitation, education, and clinical diagnosis due to their ability to monitor and interpret neural activity in real time [Luo et al., 2022]. BCIs have the potential to revolutionize the way cognitive s tates are assessed and modulated by offering closed-loop interaction mechanisms that adapt to the user's brain dynamics [Lim et al., 2023, Lin and Chang, 2025]. Central to this capability is the choice of neuroimaging modality, which must meet strict criteria in temporal resolution, portability, and cost-effectiveness—especially in applications involving children or naturalistic settings [Li et al., 2025b].

Several neuroimaging techniques have been explored for use in BCI systems, each with distinct advantages and limitations. Functional Magnetic Resonance Imaging (fMRI) offers high spatial resolution and whole-brain coverage, but its cost, immobility, and dependence on specialized facilities make it impractical for real-time interaction or integration with everyday environments [Yang and Wang, 2025]. Magnetoencephalography (MEG) provides excellent spatiotemporal resolution but is similarly constrained by high operational costs and the need for magnetically shielded rooms [Peksa and Mamchur, 2023]. Functional Near-Infrared Spectroscopy (fNIRS), a more portable option, measures cortical hemodynamic responses with moderate spatial resolution and tolerance to movement [Doherty et al., 2023]. However, its low temporal resolution limits its ability to capture fast-changing neural dynamics, such as those required for attentional monitoring or neurofeedback [Chen et al., 2023].

Electroencephalography (EEG), by contrast, emerges as the most suitable modality for BCI applications that demand real-time responsiveness, portability, and affordability [Niso et al., 2023]. EEG records the brain's electrical activity through non-invasive scalp electrodes, offering millisecond-level temporal resolution ideal for tracking rapid cognitive events like attention shifts or inhibitory control. While EEG's spatial resolution is lower compared to fMRI or MEG, advances in signal processing—such as quantitative electroencephalography (QEEG), functional connectivity analysis, and source localization—have greatly enhanced its ability to extract meaningful neurophysiological markers [Caiado and Ukolov, 2025, Yadav and Maini, 2023, Värbu et al., 2022]. This practical advantage is highlighted when comparing brain imaging modalities along the spectrum of portability and infrastructure requirements (see Figure **1-1**). Moreover, EEG's lightweight hardware, low infrastructure requirements, and compatibility with embedded systems make it an ideal foundation for interactive, portable, and scalable BCI solutions [Cai et al., 2025].

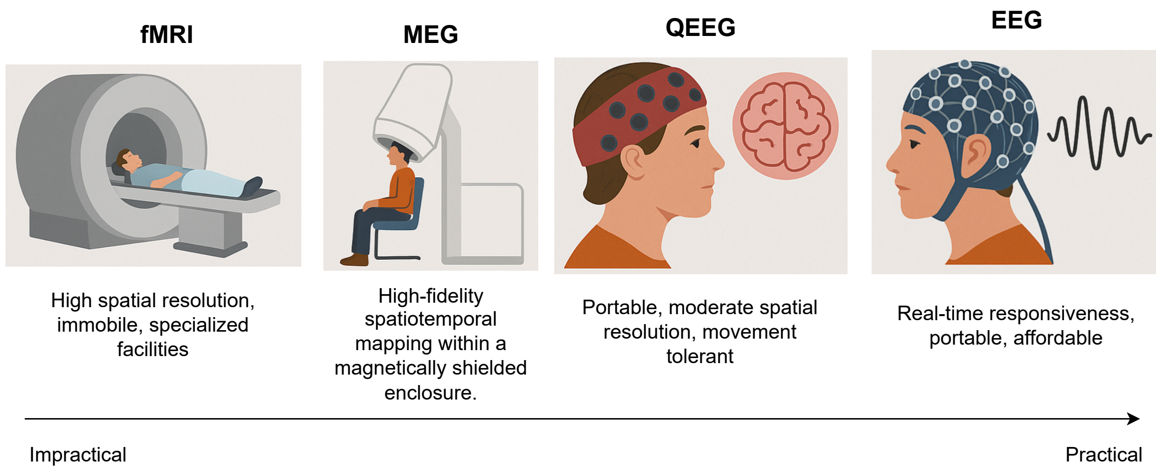

Figure 1-1: Comparison of neuroimaging modalities by spatial resolution, temporal resolution, and cost. EEG stands out for its affordability, portability, and millisecond-level responsiveness.

Building upon these practical advantages, EEG-based BCI systems have been widely adopted across a diverse range of non-clinical domains (see Figure **1-2**). In human-computer interaction and entertainment, for instance, motor imagery paradigms allow users to control digital interfaces or external devices simply by visualizing specific physical movements [Gao et al., 2022]. Similarly, in the emerging field of neuromarketing, EEG is utilized to gauge consumer engagement and emotional valence in real-time, providing objective neurophysiological metrics that bypass the biases of traditional behavioral self-reporting [Byrne et al., 2022]. Furthermore, visual experiments leveraging steady-state visually evoked potentials (SSVEPs) and other event-related potentials demonstrate EEG's capacity to create robust communication pipelines and monitor spatial attention [Chen et al., 2022b]. These broad applications highlight the versatility of EEG in decoding cognitive and sensory processes in everyday environments, seamlessly paving the way for more specialized, targeted interventions [Tait et al., 2025].

One of the most compelling clinical applications of EEG-based BCI is in the assessment and intervention of neurodevelopmental disorders such as Attention Deficit Hyperactivity Disorder (ADHD). ADHD affects approximately 10 % of children in Colombia [Salari et al., 2023, Pineda et al., 2003] and is characterized by persistent symptoms of inattention, hyperactivity, and impulsivity that interfere with academic performance, social relationships, and emotional regulation. Conventional diagnostic practices rely heavily on behavioral questionnaires and clinical observation, which, while informative, are inherently subjective and susceptible to bias [Raiker et al., 2017]. In this context, EEG offers a valuable alternative by enabling the objective measurement of neural correlates linked to attention and impulse control. Well-established EEG biomarkers such as elevated theta/beta ratios and altered event-related potentials (e.g., P300) have been extensively validated in the ADHD literature, making EEG a scientifically robust and clinically relevant tool for real-time cognitive monitoring and neurofeedback interventions [Tan et al., 2025].

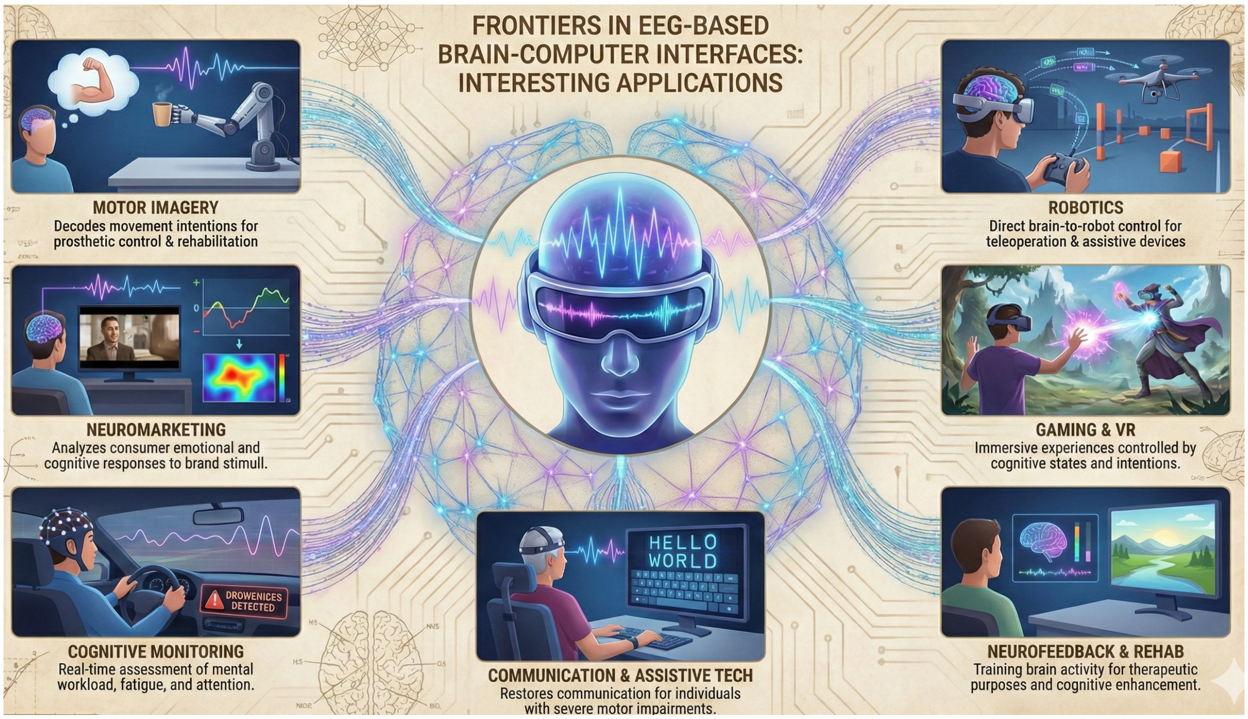

Figure 1-2: Applications of EEG-based BCIs in different domains.

Serious games are digital environments designed not solely for entertainment, but to fulfill educational, therapeutic, or cognitive objectives [Damaševičius et al., 2023]. In the context of neurodevelopmental disorders such as ADHD, they have become increasingly relevant as tools for both cognitive assessment and intervention [Patiño et al., 2025]. Their engaging and adaptive nature allows them to target specific executive functions—like attention, inhibition, and working memory—while maintaining high user motivation, particularly among children [Rodríguez Timaná et al., 2024]. To achieve this, two principal paradigms guide their design [De Luca et al., 2024]. The first is the task-based paradigm, which integrates classical neuropsychological tasks—such as the Go/No-Go, n-back, or Stroop test—into interactive game mechanics, allowing for the precise measurement of behavioral responses tied to well-established cognitive models [Fang et al., 2025]. The second is the neurofeedback paradigm, in which the game dynamically responds to real-time EEG signals, offering auditory or visual feedback based on the user's brain state. This paradigm supports operant conditioning mechanisms, encouraging users to self-regulate neural activity linked to attentional control and inhibition [Firouzabadi et al., 2022].

These design paradigms are intricately aligned with four core cognitive models critical to

ADHD pathology: attention, working memory, inhibition, and planning (see Figure **1-3**). Games targeting the attentional model aim to improve sustained and selective attention, often requiring players to maintain focus amid distractions or shifting stimuli [Chen et al., 2024]. Working memory is typically trained through tasks that require the temporary storage and manipulation of information, such as remembering sequences or updating mental representations. The inhibition model involves suppressing prepotent responses or resisting distractions—commonly implemented through fast-paced decision-making challenges or impulse control mechanics [Takahashi et al., 2024, Breitling-Ziegler et al., 2020]. Finally, the planning model emphasizes goal-directed behavior, encouraging users to sequence actions, solve multi-step problems, or anticipate future outcomes [Lorini et al., 2022]. By aligning game mechanics with these cognitive models, serious games become powerful tools not only for engagement but for targeted neurocognitive intervention.

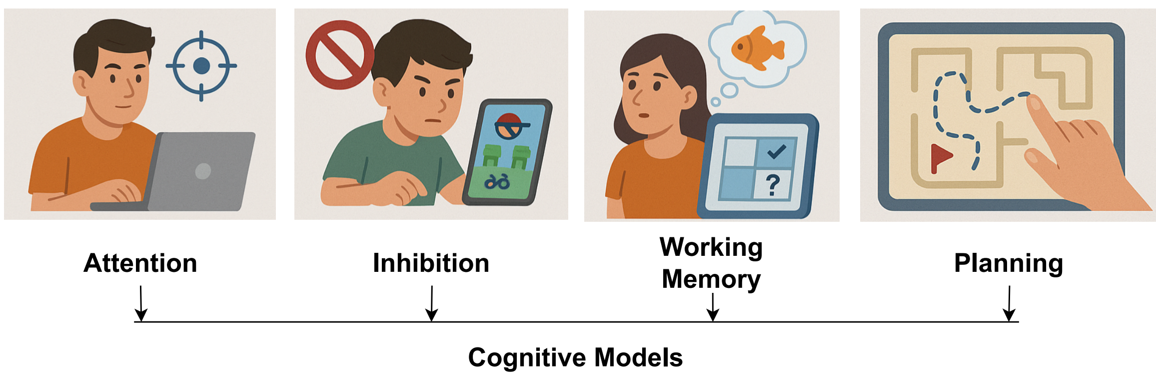

Figure 1-3: Core cognitive models targeted by serious games in ADHD interventions: attention, working memory, inhibition, and planning. Each model maps to a specific set of game dynamics and EEG markers.

When these targeted interventions are integrated with BCI technology, they demonstrate substantial therapeutic benefits by reinforcing executive function, improving behavioral outcomes, and reducing symptom severity through active attention training [Doulou et al., 2025]. By utilizing active BCIs, in which users intentionally modulate their focus to influence the outcome of the game, these systems have been shown to strengthen cognitive control and promote long-term neuroplastic changes directly relevant to ADHD pathology [Cervantes et al., 2023]. Furthermore, these integrated platforms enable adaptive feedback, allowing interventions to dynamically adjust to each child's specific neurocognitive profile. Ultimately, combining robust cognitive models with real-time, objective EEG feedback makes serious games uniquely compatible with BCIs, providing a highly personalized framework for interactive cognitive modulation.

Recent developments in portable EEG hardware have expanded the applicability of BCIs for ADHD beyond clinical settings, enabling real-time monitoring and feedback in homes, classrooms, and therapeutic environments (see Figure **1-4**). Low-cost, wireless EEG headsets—equipped with dry electrodes and embedded microcontrollers—have been successfully integrated into neurofeedback systems and serious games designed for children [Xu and

Zhong, 2018]. These platforms allow for real-time signal acquisition and onboard processing, supporting closed-loop interventions without reliance on external computers. Thanks to ARM-based processors and system-on-chip (SoC) designs, it is now possible to run lightweight machine learning models directly on the device for real-time EEG classification [Wang et al., 2020]. Moreover, custom head-mounted EEG systems have shown reliable tracking of the theta/beta ratio, a key biomarker for ADHD, during interactive tasks [Larocco et al., 2020].

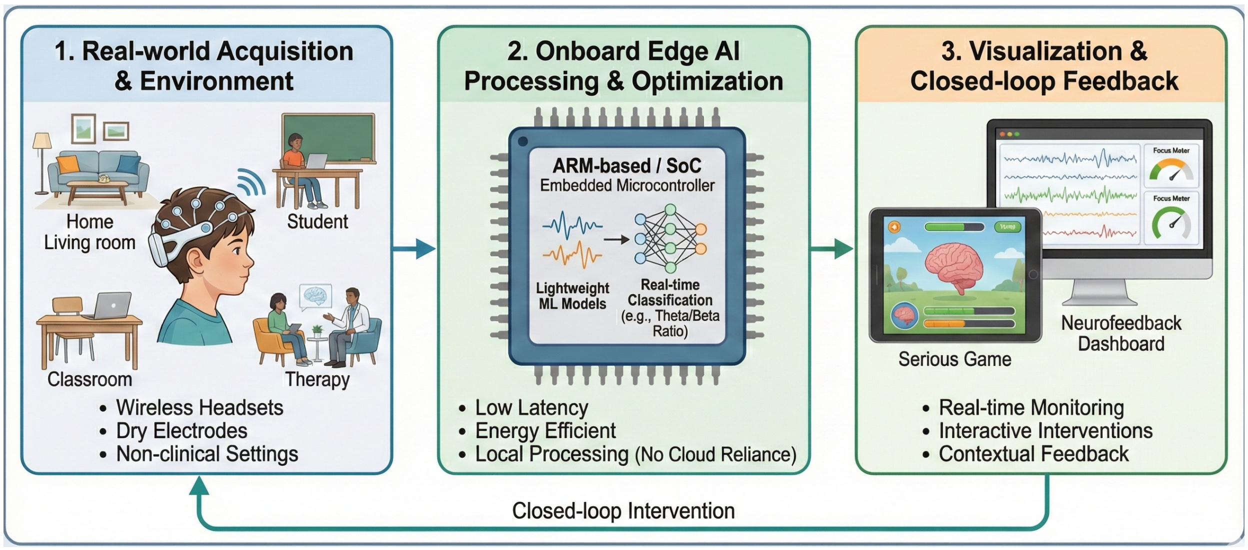

Figure 1-4: Overview of the Brain-Computer Interface (BCI) and Artificial Intelligence (AI) integration for neurocognitive assessment.

The push to bring these portable, AI-driven interventions out of the clinic is heavily supported by the rapid expansion of the digital health sector. As of 2024, the global telehealth and telemedicine market surpassed $123 billion, reflecting a permanent shift toward decentralized care and remote patient monitoring [Grand View Research, 2024]. To support this transition, the global embedded systems market reached over $112 billion in 2024, driven by an immense demand for compact, energy-efficient Internet of Medical Things (IoMT) devices [Coherent Market Insights, 2024]. Concurrently, the integration of artificial intelligence into healthcare—a market valued at over $13 billion in the U.S. alone in 2024—demonstrates a strong clinical and commercial drive to embed complex diagnostic intelligence directly into everyday environments [Nova One Advisor, 2024]. These economic indicators highlight a clear motivation: there is a profound necessity to translate hospital-grade capabilities into accessible, wearable form factors that operate autonomously.

To successfully deploy these autonomous systems in daily life, research must focus on optimizing hardware and software integration for strict portable constraints [Phiri, 2023]. Operating continuously in non-clinical settings necessitates highly efficient energy and resource use, as wearable devices are bound by severe power and memory limitations. Processing biosignals locally via edge AI reduces latency and power-heavy cloud transmissions, yet it requires highly tailored acquisition algorithms that maximize computational efficiency [Shajari et al., 2023]. Furthermore, capturing a comprehensive physiological profile demands the precise synchronization of biomarkers across distributed sensors [Ramasubramanya et al., 2025]. Ensuring that multi-modal data streams are temporally aligned is an absolute necessity for generating accurate, real-time contextual feedback. By establishing robust methods to efficiently acquire, align, and process these integrated biomarkers on low-power architectures, this research aims to unlock the full therapeutic potential of continuous, closed-loop neurofeedback outside of traditional medical facilities [Li et al., 2023].

To address these evolving requirements for decentralized mental health technology, this research is developed within the framework of the project called "Alianza científica con enfoque comunitario para mitigar brechas de atención y manejo de trastornos mentales relacionados con impulsividad en Colombia" (ACEMATE) (Multimodal system supported by serious games for personalized neurocognitive assessment and intervention in impulsivity disorders associated with ADHD), a collaborative initiative involving the Universidad Nacional de Colombia and the Universidad Tecnológica de Pereira. ACEMATE aims to facilitate both face-to-face and remote interventions across clinical, educational, and community settings. However, realizing this vision of accessible care relies entirely on deploying physical infrastructure that resolves the previously outlined technical bottlenecks—specifically, the need for robust, portable hardware capable of precise biomarker synchronization. Consequently, this thesis proposes the development of MONEEE, a specialized EEG signal acquisition system designed to serve as the hardware enabler for ACEMATE. By ensuring low-latency marker integration and high signal fidelity under strict energy and resource constraints, MONEEE provides the essential technological foundation to power the broader ACEMATE ecosystem, ultimately democratizing access to objective, technology-driven mental health services for children.

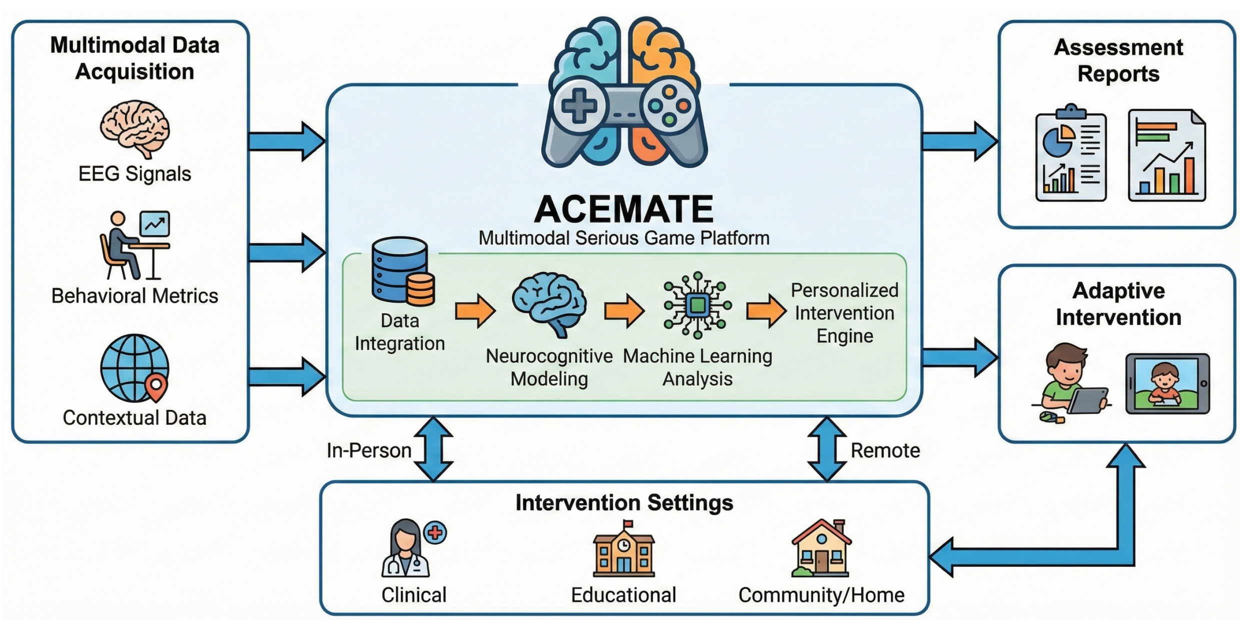

Figure 1-5: Overview of the ACEMATE project.

1.2 Problem statement

While the integration of BCIs and continuous EEG monitoring within serious games presents a promising avenue for neurocognitive assessment, translating these concepts into functional clinical tools requires a highly robust underlying hardware architecture [Craik et al., 2023]. Fundamentally, the physical acquisition of this neural data begins with an EEG cap fitted with non-invasive sensors designed to detect microvolt-level electrical signals from the cerebral cortex. Because these raw biological signals are inherently weak and highly susceptible to noise, they must be routed to a dedicated acquisition board or a multi-stage card system [Armand Larsen et al., 2024]. This hardware typically consists of an analog front-end—responsible for the high-precision amplification, filtering, and digitization of the signals—and a digital processing unit, such as a microcontroller, for real-time data management and routing [Janapati et al., 2023]. To effectively map the neurocognitive responses elicited by the serious games, this continuous neural data must be contextually locked to specific in-game cognitive stimuli. This vital synchronization is achieved by interfacing the acquisition hardware with the stimulus presentation device, which transmits discrete event markers that map external gameplay milestones directly to the EEG stream [Minissi et al., 2025].

However, the translation of this theoretical promise into clinical reality faces formidable engineering barriers. The efficacy of closed-loop interventions is predicated not on the mere availability of data, but on the fidelity and temporal determinism of that data [Sabio et al., 2024]. Current acquisition architectures, particularly those designed for portability and low cost, are frequently plagued by systemic failures that sever the causal link between neural intention and digital response [Ariza and Pearce, 2022]. This research defines and analyzes two such sequential, critical failures. The foundational challenge stems from severe Signal-to-Noise Ratio (SNR) limitations inherent to embedded architectures [Li et al., 2025a]. In portable EEG devices designed for ADHD monitoring, the physical proximity of high-speed digital processing components inevitably introduces electromagnetic interference. This interference degrades the system's high-precision analog sensing, corrupting the delicate microvolt-level neural signals required before any valid clinical evaluation can even begin [Dobrev and Neycheva, 2022]. Once a reliable physiological signal is secured, a second, equally critical failure emerges: the precise synchronization of biomarkers [Esteban et al., 2026]. Because ADHD neurocognitive assessments rely heavily on time-locked neural responses to specific game events, any temporal variability or unpredictable latency between the digital stimuli and the recorded biological signals fundamentally compromises the diagnostic validity of the data [Kamiński et al., 2026]. The contrast between the theoretical promise of continuous monitoring and the clinical reality is summarized in Figure **1-6**.

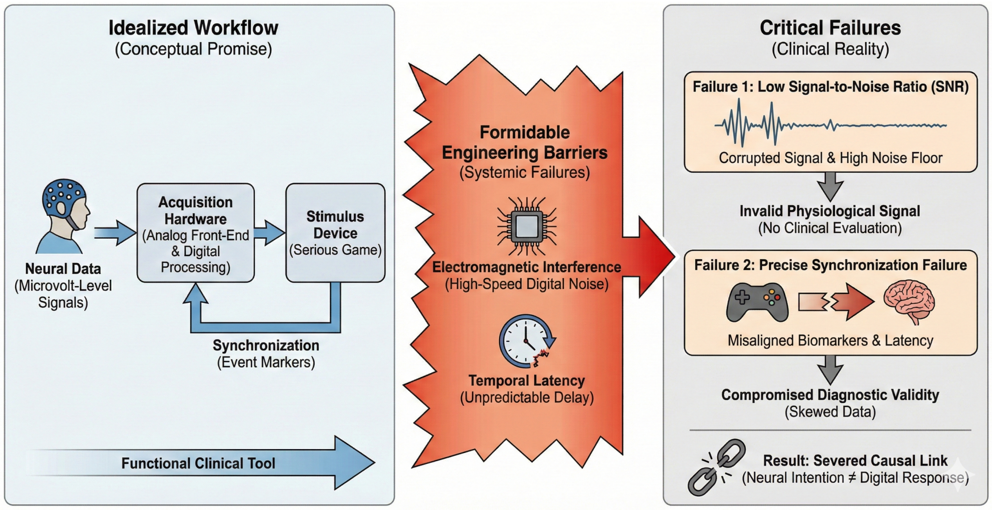

Figure 1-6: The clinical translation problem in neurocognitive assessment systems. The illustration defines the two sequential critical failures that compromise diagnostic validity: the corruption of the analog signal and the temporal misalignment of biomarkers.

1.2.1 SNR limitations in embedded systems

The physical interface of traditional clinical EEG setups creates a major operational bottleneck for pediatric neurocognitive assessment. Lengthy and restrictive cap placement processes consistently induce restlessness, anxiety, and movement artifacts in children with ADHD [Lim et al., 2023]. If the acquisition hardware cannot be deployed rapidly and comfortably, the resulting setup latencies and prolonged impedance stabilization times severely degrade the SNR [Gorjan et al., 2022]. This physical friction directly compromises the ecological validity and engagement required for a serious game environment, making the rapid deployment of the acquisition cap a critical challenge to overcome [Kaongoen et al., 2023].

Once the physical interface is established, preserving analog signal integrity within a densely populated, mixed-signal embedded system presents a fundamental hardware challenge [Liu et al., 2024a]. The close physical proximity of high-speed digital processing units to the analog front-end introduces severe risks of electromagnetic interference and power supply noise coupling [Devi et al., 2022]. If physical board layout and isolation strategies are inadequate, the system's intrinsic background noise will inevitably exceed the baseline input-referred noise thresholds of the acquisition components (typically 1 µVpp) [Rashid et al., 2018]. Overcoming this mixed-signal noise ceiling is essential; failure to do so creates a high noise floor that completely masks the low-amplitude Event-Related Potentials (ERPs) necessary for cognitive assessment [Kim et al., 2022].

Even if analog noise is successfully mitigated, the embedded system's processing hardware faces severe resource constraints when managing continuous, high-frequency electrophysiological data streams. Unoptimized continuous data logging demands substantial computational power and can rapidly induce I/O bottlenecks, RAM saturation, and subsequent thermal throttling [Battaglia et al., 2022]. The immediate consequence of an overburdened CPU or saturated memory footprint is the dropping of crucial data packets and the introduction of variable acquisition latency [Arroba et al., 2024]. This resource exhaustion fundamentally corrupts the integrity and continuity of the EEG data stream itself. Therefore, continuous monitoring of RAM usage and CPU load is critical to ensure the hardware can sustain reliable, uninterrupted data acquisition without buckling under the operational demands [Ajmeria et al., 2022]. As illustrated in Figure **1-7**, the physical friction of traditional cap placement and the subsequent risk of analog signal corruption present immediate hurdles.

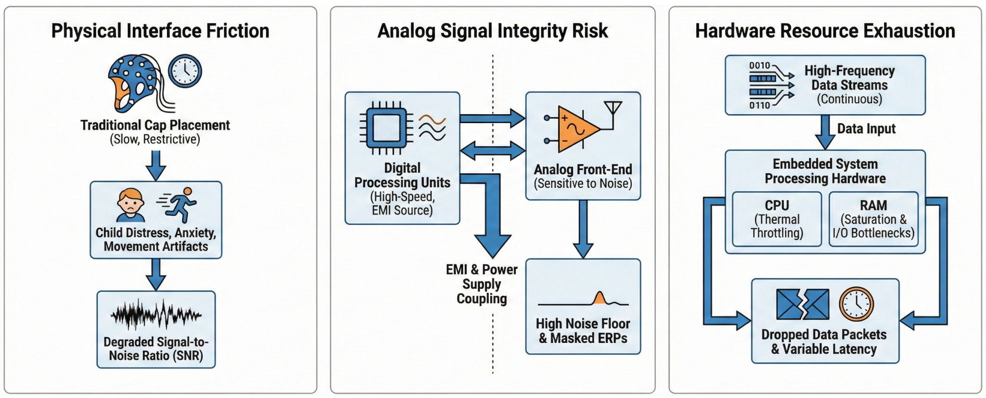

Figure 1-7: Physical, electrical, and computational resource barriers in deploying EEG systems. The illustration highlights operational bottlenecks during patient setup, the risk of SNR degradation due to mixed-signal interference, and embedded system resource exhaustion.

1.2.2 Synchronization and temporal variability in EEG biomarkers

The primary challenge in extracting valid neurocognitive assessments lies in the precise temporal synchronization of acquired EEG biomarkers with external serious game stimuli [Ahmed et al., 2025]. During interactive sessions, event markers are continuously transmitted from the game interface to the acquisition system. Standard communication protocols, however, introduce inherent, non-deterministic latency driven by transmission overhead, variable polling rates, and operating system scheduling conflicts [Buraimoh et al., 2023]. This unpredictable communication jitter fundamentally skews the temporal alignment between the stimulus presented to the patient and the corresponding neurophysiological response [Larsen et al., 2024]. By conducting rigorous short-term latency bounding tests, this immediate communication delay must be quantified and mitigated to ensure the calculated Event-Related Potentials (ERPs) are temporally accurate and clinically viable [He et al., 2023].

Beyond the immediate delay of single events, maintaining precise synchronization throughout a complete clinical session presents a compounding temporal challenge. Standard pediatric ADHD evaluations demand sustained, uninterrupted engagement. Continuous execution over these extended periods exposes the acquisition architecture to cumulative temporal errors [Arpaia et al., 2025]. Asynchronous clock drift between the event triggers and the hardware sampling rate, coupled with potential memory buffer saturation and thermal-induced performance fluctuations, introduces progressive instability [Dasenbrock et al., 2022]. This compounding jitter degrades deterministic data throughput, leading to a critical flaw where an ERP captured at the end of a session exhibits a fundamentally different latency profile than one captured at the beginning. Extended stability testing over full-length sessions is therefore imperative to prevent temporal degradation and validate the long-term reliability of the continuous EEG stream [Tran et al., 2026].

In parallel with resolving these mechanical timing issues, valid synchronization relies on the system's proven ability to capture authentic, dynamic electrophysiological phenomena rather than structured noise [Correia et al., 2024]. Before complex ERPs can be reliably synchronized with external events, a foundational physiological baseline test must be conducted. This problem is addressed by detecting spontaneous frequency modulations, specifically the well-documented attenuation of alpha-band activity (8–13 Hz) when a subject transitions from an eyes-closed to an eyes-open state [Isler et al., 2023]. If the signal processing pipeline distorts the bandwidth or lacks the sensitivity to capture these baseline spectral shifts, the recorded data is physiologically invalid [Fló et al., 2022]. Verifying the fundamental ability to resolve these basic frequency changes ensures that the synchronized event markers are anchored to genuine neural activity [Frelih et al., 2025]. Figure **1-8** demonstrates how non-deterministic latency and cumulative temporal drift fundamentally skew the alignment between the game stimulus and the neurophysiological response.

Finally, the temporal precision of the biomarkers must be matched by their spatial and structural integrity, which requires addressing inherent hardware vulnerabilities. High-resolution, multi-channel EEG acquisition creates a strict physical requirement for trace isolation to prevent analog signal bleed. Without meticulous shielding, adjacent channels inevitably suffer from crosstalk, blending distinct spatial brain waves and destroying the topographical accuracy of the recorded data. Furthermore, rendering these continuous data streams can introduce visualization artifacts that masquerade as genuine visual transients or ERPs. By executing rigorous signal isolation and artifact detection tests, these structural issues can be identified and eliminated, ensuring that the precisely synchronized neurocognitive markers are extracted from pristine, uncontaminated data.

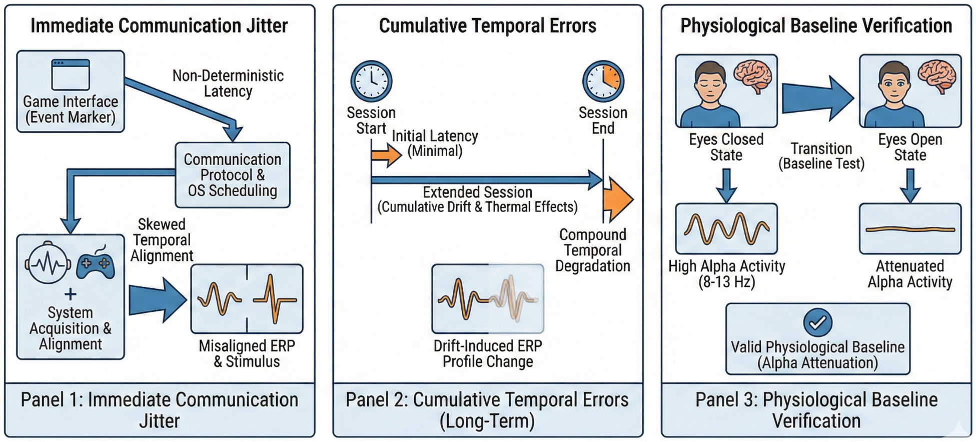

Figure 1-8: Synchronization errors and real-time physiological validation. This figure details the impact of short-term non-deterministic communication jitter, cumulative temporal drift in extended sessions, and physiological baseline verification via alpha-band attenuation.

1.3 Research question

How can an embedded EEG acquisition architecture be optimized to simultaneously mitigate mixed-signal interference and non-deterministic synchronization jitter to ensure the clinical validity of biomarkers in serious-game-based ADHD assessments?

1.4 State of art

1.4.1 Signal-to-Noise Ratio (SNR) Optimization and Resource Management in Mixed-Signal Embedded EEG

The acquisition of clinical-grade electroencephalographic (EEG) signals within embedded, portable form factors is fundamentally constrained by the physics of biopotential measurement and the stringent demands of edge computing [Lyu, 2026]. Neural signals propagating to the scalp surface are inherently weak, exhibiting amplitudes ranging from 1 to 100 µV, and occupy a highly susceptible low-frequency band typically between 0.5 Hz and 100 Hz [Singh et al., 2023]. Extracting these delicate potentials requires overcoming extreme signal attenuation across the variable conductive layers of the skull and scalp, high electrode-skin impedance interfaces [Gkintoni and Halkiopoulos, 2025], and pervasive environmental interference such as 50/60 Hz power-line noise and ambient electromagnetic fields [Zhang et al., 2025].

When high-gain, high-impedance analog sensing circuits are integrated into compact physical proximity with high-speed digital processors, the risk of signal corruption via capacitive coupling, trace crosstalk, and ground-loop noise rises exponentially [Porto Cruz et al., 2025]. Furthermore, the operational demand of executing continuous, high-resolution data logging alongside complex algorithmic denoising on resource-constrained embedded devices rapidly induces input/output bottlenecks, memory saturation, and thermal throttling [Nguyen et al., 2025]. These systemic processing delays introduce variable acquisition latency and temporal jitter, directly threatening the precise synchronization of biomarkers which is an absolute prerequisite for maintaining the structural continuity of the EEG stream in multi-modal analysis [Iwama et al., 2023]. To address these interconnected biophysical and computational challenges, the scientific community has pursued four distinct philosophical approaches over the past four years to optimize embedded architectures.

Hardware-Level Isolation and Active Analog Front-End Architecture

The foundational philosophy for optimizing the Signal-to-Noise Ratio (SNR) at the edge posits that interference must be aggressively rejected at the physical and electrical interface long before digitization occurs, thereby preventing downstream software bottlenecks [Xu et al., 2025]. Central to modern embedded Brain-Computer Interface (BCI) systems is the utilization of highly specialized, application-specific integrated circuits designed explicitly for biopotential measurement [Han et al., 2022b]. These dedicated analog front-ends feature ultra-low input-referred noise floors and 24-bit delta-sigma analog-to-digital converters that provide expansive dynamic ranges [Chen et al., 2022a]. This wide dynamic range is highly critical for preventing amplifier saturation when baseline microvolt neural signals are superimposed with massive, millivolt-level motion artifacts during mobile use [Pochet and Hall, 2022].

Table 1-1: Acquisition devices used for BCI. The table provides an overview of the different hardware devices, their specifications, and communication protocols.

Device	Company	Electrodes	Channels	Sampling Rate	AFE	Connectivity	Battery
Cyton + Daisy [OpenBCI, 2024]	OpenBCI	Flexible / Wet / Dry	16	250 Hz – 16 kHz	ADS1299	RF / BLE / Wi-Fi	8 h
actiCAP [Products, 2024]	Brain Products GmbH	Flexible / Wet / Dry	16	256 Hz – 16 kHz	–	USB	16 h
EPOC X [Emotiv, 2024]	Emotiv	Rigid / Wet	14	128 Hz	–	BLE / Bluetooth	6–12 h
Diadem [Bitbrain, 2024]	Bitbrain	Rigid / Dry	12	256 Hz	–	Bluetooth	8 h
g.Nautilus [g.tec, 2024]	g.tec	Flexible	8 / 16 / 32	250 Hz	ADS1299	Proprietary	10 h
Ambulatory platform [Pinho et al., 2014]	–	Active / Dry	32	250 Hz – 1 kHz	ADS1299	Wi-Fi 802.11 b/g/n	26 h
Neurofeedback system [Totev et al., 2023]	–	Passive / Dry	40	250 Hz	ADS1298	RF	–
BEATS [Zou et al., 2022]	–	Flexible / Wet	32	4 kHz	ADS1299	Wi-Fi	24 h (wired)

The widespread adoption of these specialized components is evident across both commercial and research-grade platforms, which exhibit a broad spectrum of design trade-offs between channel density, portability, and the temporal precision required for accurate biomarker synchronization. As summarized in Table 1, systems relying on dedicated analog front-ends like the Texas Instruments ADS1299 or ADS1298—such as the OpenBCI Cyton + Daisy, g.Nautilus, the ambulatory platform proposed by Pinho et al., the neurofeedback system by Totev et al., and the BEATS system—leverage these components to guarantee high-performance signal conversion. The Cyton + Daisy system, for instance, supports up to 16 channels and offers a highly versatile sampling rate ranging from 250 Hz to 16 kHz, transferring data via RF, Bluetooth Low Energy, or Wi-Fi to adapt to various environments. Similarly, the actiCAP system achieves high-resolution acquisition up to 16 kHz over a robust USB protocol, making it ideal for long-duration, stable clinical environments. Conversely, more compact, consumer-oriented architectures like the Emotiv EPOC X and the Bitbrain Diadem operate at significantly lower sampling rates of 128 Hz and 256 Hz, respectively. While these devices offer excellent portability and sufficient battery life for general neurofeedback or basic cognitive training, their lower sampling rates and reliance on standard Bluetooth stacks introduce significant vulnerabilities regarding absolute temporal alignment. For clinical research demanding the precise temporal locking of Event-Related Potentials to digital stimuli, architectures that prioritize high-frequency sampling and high-bandwidth or proprietary data transmission—such as the 4 kHz sampling rate of the BEATS system or the custom protocols of the g.Nautilus—are strictly necessary to minimize the non-deterministic communication jitter that otherwise obliterates biological synchronization.

Maximizing these hardware capabilities within densely populated mixed-signal environments requires meticulous printed circuit board design, prominently featuring the strict spatial and galvanic isolation of analog and digital ground planes [Wang et al., 2024]. These planes are typically connected only at a single star point to prevent high-frequency digital return currents from modulating the sensitive analog ground reference [Sen et al., 2025]. Furthermore, the implementation of dynamic right-leg drive (DRL) circuits—which compute the common-mode average of the measuring electrodes, invert the phase, and feed it back to the subject's body—is essential for stabilizing the baseline potential [Luo et al., 2025]. This active feedback loop drastically improves the overall Common-Mode Rejection Ratio (CMRR) of the system, actively neutralizing pervasive power-line interference directly at the source [Wen et al., 2025].

To accommodate pediatric populations and highly active users where traditional abrasive skin preparation is impossible, modern designs are transitioning from wet silver/silver-chloride electrodes to active dry sensors or polymer-based microneedle arrays [Liu et al., 2024b, Kim et al., 2024]. By embedding unity-gain operational amplifiers directly at the scalp site, these active shields act as immediate impedance transformers. This active buffering effectively counters the inherently high skin-electrode impedance of dry contacts—often exceeding 100 kΩ [Xiong et al., 2025]—and eliminates the triboelectric cable noise and capacitive signal attenuation that would otherwise obliterate the neural signal before it reaches the amplification stage, thus maintaining high signal fidelity in naturalistic environments [Giangrande et al., 2024].

Statistical and Decomposition-Based Signal Processing

Even with optimal hardware-level isolation and active buffering, physiological artifacts originating from the user—such as electrooculograms from eye blinks and electromyograms from jaw clenching or facial muscle movement—inevitably overlap with the low-frequency EEG spectrum [Agounad et al., 2025, Yedukondalu and Sharma, 2023]. A mathematically rigorous approach to address this spectral overlap relies on multivariate statistical methods and signal decomposition to computationally unmix these noise sources from the underlying neural activity. While Independent Component Analysis (ICA) remains one of the most widely cited techniques due to its ability to blindly separate statistically independent non-Gaussian sources [Avital et al., 2025], contemporary edge-computing literature highlights its severe operational limitations. ICA requires significant, continuous data buffering to construct a covariance matrix and converge upon a stable demixing matrix, making it highly computationally expensive, memory-intensive, and fundamentally poorly suited for the hard real-time, low-latency requirements of a resource-constrained embedded device [Ein Shoka et al., 2023, Shahshahani and Mahdiani, 2022].

To circumvent the massive computational payloads of ICA, modern embedded designs have shifted toward Canonical Correlation Analysis (CCA) and Empirical Mode Decomposition (EMD) [Trong et al., 2024]. CCA is highly efficient at isolating and removing high-frequency muscle artifacts by separating sources based on second-order statistics and temporal autocorrelation rather than strict higher-order statistical independence, drastically reducing the requisite processing cycles [Hossain et al., 2022, Akshath Raj et al., 2025]. Concurrently, EMD functions as a purely data-driven heuristic that breaks down non-stationary EEG time series into a finite set of adaptive Intrinsic Mode Functions [Gorur, 2023]. This allows for the robust, automatic template-matching and extraction of low-frequency eye blink artifacts without requiring external reference channels.

Additionally, Discrete Wavelet Transforms are frequently utilized within this philosophical framework to decompose the signal into distinct time-frequency detail and approximation coefficients [Zangeneh Soroush et al., 2022]. This effectively strips out baseline wander via soft thresholding before reconstructing the time-domain signal [Serbes, 2024]. However, researchers increasingly caution that the recursive sifting processes inherent to EMD and the multi-level filter banks of wavelet decomposition still pose a distinct risk of central processing exhaustion if not heavily optimized mathematically for the specific instruction sets of the deployment hardware[Erbslöh et al., 2024].

Lightweight Deep Learning for Real-Time Denoising

Driven by the mathematical limitations, rigid linear assumptions, and computational bottlenecks of traditional algorithmic decomposition, the application of Deep Learning for end-to-end, real-time EEG artifact removal has emerged as a disruptive and dominant methodology [Azhar et al., 2024]. These neural network architectures bypass the need for manual feature extraction, instead learning to map highly complex, non-linear representations between noisy physiological inputs and clean neural targets through manifold learning [Xiong et al., 2024]. However, successfully deploying deep learning on embedded platforms requires severe architectural pruning and quantization to adhere to strict memory footprints and latency constraints [Popa et al., 2026].

The state of the art heavily favors 1D Convolutional Neural Networks because their localized receptive fields natively preserve the temporal and structural integrity of the one-dimensional EEG time series [Ige and Sibiya, 2024]. By sliding temporal filters across the raw data stream, these networks utilize a mere fraction of the trainable parameters required by traditional 2D image-based networks [Saha et al., 2025]. This crucial architectural choice entirely eliminates the massive computational overhead needed to constantly convert continuous EEG streams into spectrograms via Short-Time Fourier Transforms prior to inference, a process that historically crippled edge devices [Nayana et al., 2025].

Furthermore, lightweight Denoising Autoencoders, particularly those constructed with gated recurrent units to capture long-term temporal dependencies, show exceptional promise in isolating patient-specific noise profiles [Zhang et al., 2022]. By compressing the noisy multichannel input into a tightly constrained lower-dimensional latent space, the network is forced to discard anomalous artifact variance and learn only the fundamental, high-variance physiological features of genuine brain activity, allowing the decoder to reconstruct a purely neural signal [Chuang et al., 2022]. These ultra-low-power models consistently achieve significant signal-to-noise ratio improvements while maintaining sub-50 millisecond inference latencies, proving highly viable for real-time edge deployment while deliberately avoiding the quadratic memory complexity and processing overhead associated with massive foundation models [Xing and Casson, 2024].

Edge-Computing Resource Management and Workload Offloading

The final philosophy addressing embedded EEG constraints focuses entirely on the systemic orchestration of hardware resources and network topologies to prevent processing exhaustion during continuous, high-frequency data ingestion [Wang et al., 2026]. Unoptimized continuous data logging invariably leads to buffer overflows and dropped data packets [Kanellopoulos et al., 2023]. This physical failure fundamentally corrupts the structural continuity of the EEG stream and introduces critical timing errors [Kargarnovin et al., 2023]. Preventing this jitter is paramount, as the exact synchronization of biomarkers across multiple physiological data streams dictates the temporal validity and overall scientific integrity of the entire BCI system [Müller-Putz et al., 2015].

To mitigate this operational risk, modern Internet of Medical Things paradigms leverage distributed edge computing architectures that strictly segregate data acquisition from intensive computation [Brad et al., 2024]. In these frameworks, a low-power microcontroller is relegated strictly to the role of a deterministic acquisition gateway. It interfaces with the analog sensors utilizing strict hardware interrupts and direct memory access controllers to autonomously move incoming multi-bit samples directly into alternating ping-pong memory buffers [Zayed et al., 2025]. Because this process occurs at the hardware level, it does not consume a single central processing clock cycle, ensuring perfect temporal spacing between samples [Dobrescu et al., 2024].

Once a buffer is filled, this raw, precisely timed data is pushed asynchronously to a secondary, localized computing node responsible for heavy processing [An et al., 2025]. To prevent this secondary node from thermal throttling during advanced deep learning inference, systems employ compressive offloading techniques, such as immediately extracting frequency-embedded power spectral density features or aggressively downsampling the raw stream to shrink the active memory footprint before classification [Akor et al., 2025]. Most importantly, utilizing sophisticated multi-threading environments ensures the absolute decoupling of the acquisition and processing pipelines; a high-priority hardware thread strictly handles continuous data ingestion, while lower-priority asynchronous threads manage the heavy algorithmic denoising [Van Dyck et al., 2026]. This architectural isolation guarantees that sudden computational spikes in the processing layer can never stall the hardware layer, thereby guaranteeing the continuous, deterministic sampling rates required for flawless biomarker synchronization [Savas and Coskun, 2025].

1.4.2 Temporal Synchronization and Latency Variability in EEG Biomarkers

While securing a pristine, high-signal-to-noise ratio analog signal is the strict prerequisite of neurophysiological monitoring, the extraction of valid neurocognitive metrics in therapeutic

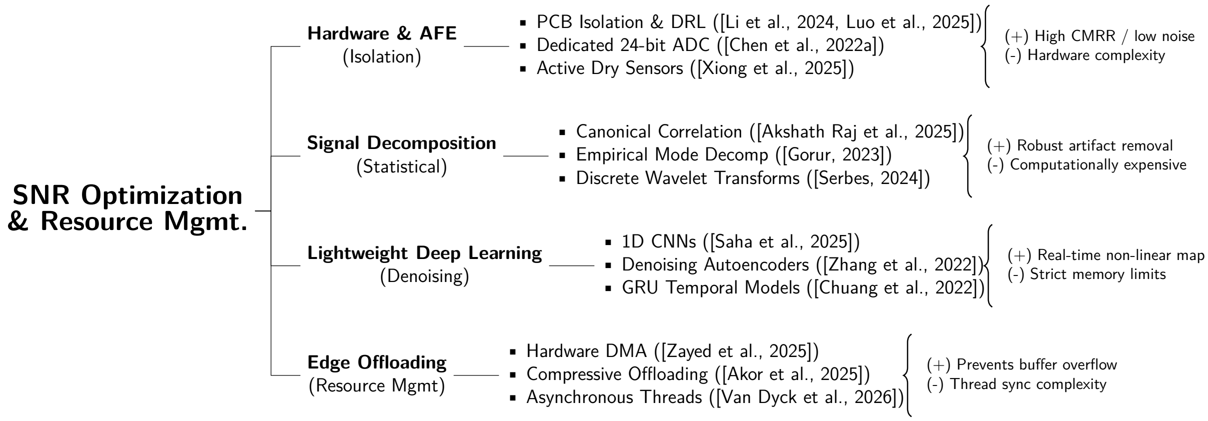

Figure 1-9: Taxonomy of SNR optimization and resource management strategies in mixed-signal embedded EEG.

interventions depends entirely on absolute temporal determinism [Nørskov et al., 2025]. Clinical cognitive assessments evaluate higher-order executive functions—such as sustained attention, target discrimination, and inhibitory control—by analyzing Event-Related Potentials (ERPs). Standard clinical features for these functions include the P300 wave, representing attention allocation and context updating [Zygouris et al., 2025], and the N200 wave, representing conflict monitoring and impulse inhibition [Fazel et al., 2024]. Crucially, these neurophysiological markers are defined not just by their morphology, but by their strict temporal latency relative to a specific external digital stimulus [Li et al., 2024].

If the temporal alignment between the digital stimulus event and the biological response in the electroencephalographic (EEG) data stream is skewed by non-deterministic communication jitter or cumulative hardware clock drift [Kothe et al., 2025], the resulting ERPs will be structurally flattened or completely obliterated during the signal averaging process [Molina et al., 2024]. Resolving these timing discrepancies is the absolute foundation for the accurate synchronization of biomarkers across multi-modal data streams [Manivannan et al., 2025]. Current research dedicated to bounding this latency and ensuring structural temporal continuity falls into four distinct methodologies [Choi et al., 2023].

Hardware-Bounded Event Marking and Interrupt Servicing

The most rigorous and deterministic approach to synchronization relies on completely bypassing the operating system's software stack to generate and handle physical hardware interrupts [Eckhoff et al., 2024]. Modern operating systems utilized on edge computing nodes typically employ preemptive multitasking schedulers. When a cognitive event occurs within a digital interface, the transmission of the corresponding marker via standard serial communication stacks is subject to the operating system's internal polling rate, payload encapsulation delays, and unpredictable buffer queuing [Miziara et al., 2025]. This computational overhead creates a non-deterministic communication jitter that can fluctuate by tens of milliseconds from one trial to the next, entirely corrupting the precision required for high-frequency neural analysis [Gemborn Nilsson et al., 2023].

To achieve sub-millisecond latency bounding, recent studies heavily advocate for direct hardware triggering and low-level peripheral optimization. When serial bus communication is mandatory, mitigating latency requires highly optimized endpoint configurations. By forcing communication peripherals to operate in strict interrupt or isochronous transfer modes rather than standard bulk transfers, the acquisition system can guarantee dedicated bus bandwidth and reduce polling intervals to the absolute microframe limits inherent to the communication specification [Rousseau et al., 2025]. These digital event codes must be parsed at the lowest hardware level via fast interrupt service routines and instantaneously stamped against a highly precise master hardware timer before being merged sequentially into the continuous biological data payload, ensuring zero software-induced jitter [Andrijević et al., 2025].

Protocol-Level Middleware and Network Synchronization

When purely hardware-based triggering via direct pin manipulation is not feasible—often due to the locked-down nature of commercial consumer hardware used for visual stimuli—the literature relies on advanced software synchronization middleware [Lorenz et al., 2024]. Specialized networking protocols have emerged as the ubiquitous standard in modern continuous multi-modal monitoring. These middleware systems are designed explicitly to handle the unified collection of time-series data across disparate, distributed devices over local networks without requiring physical trigger cables [Daza et al., 2025].

These software systems achieve sub-millisecond synchronization accuracy by implementing a continuous background clock-offset measurement. When a digital interface registers a cognitive event, it pushes the marker to a local network outlet, while the sensing unit simultaneously pushes the biological stream to a parallel outlet [Klumpp et al., 2025]. The core protocol continuously calculates the network transmission delay and the shifting offset between the distinct local clocks of the distributed devices. It utilizes this data to retroactively adjust the timestamps of the digital markers to perfectly align with the incoming data stream [Dasenbrock et al., 2022]. However, researchers caution that these protocols are still bounded by the visual rendering latency of the screen; failing to account for display monitor refresh delays allows mechanical hardware lag to masquerade as delayed human neural processing [Han et al., 2022a].

Algorithmic Mitigation of Cumulative Clock Drift

While single-event latency and jitter corrupt individual evaluation trials, extended continuous monitoring sessions expose the acquisition architecture to cumulative temporal errors known as clock drift. Clock drift occurs because the independent crystal oscillators driving the analog-to-digital converters, the microcontrollers, and the visual display units operate at slightly different, imperfect physical frequencies [Ionescu et al., 2022]. These oscillator frequencies fluctuate further throughout a session due to internal thermal dynamics, battery voltage variations, and ambient environmental conditions. Over an extended therapeutic session, a microscopic drift of just 10 parts-per-million between distinct hardware clocks translates to an absolute temporal misalignment of tens of milliseconds [Ding et al., 2025].

This magnitude of drift is severe enough to completely invalidate the precise measurement of fast cognitive potentials, mathematically forcing a healthy neural response to appear delayed or pathological by the end of the session [Getzmann et al., 2024]. To counter this, modern architectures employ dynamic drift compensation algorithms utilizing linear regression timestamping. By periodically transmitting a specific synchronization pulse from the stimulus generator to the acquisition node at strict intervals, the processing layer can continuously map the digital timeline onto the biological timeline using a rolling linear regression model [Li et al., 2022]. This allows the system to calculate the exact drift coefficient in real-time and dynamically resample the data or adjust the event timestamps mathematically, ensuring perfect temporal determinism from the first minute of the session to the last [Weber and Pfeiffer, 2025].

Physiological Baseline Validation and Neurocognitive Extraction

Resolving mechanical, network, and computational timing issues is scientifically insufficient if the system cannot ultimately prove it is capturing authentic, time-locked neurobiology. Consequently, the literature mandates rigorous physiological baseline testing prior to extracting complex cognitive markers [Rykov et al., 2024]. The most universally accepted validation protocol for continuous temporal bounding is the alpha-band attenuation test, colloquially known as the Berger effect [Ha et al., 2023]. Alpha waves are highly synchronized, high-amplitude oscillations dominant in states of wakeful relaxation with closed eyes. When a subject opens their eyes to engage with a visual stimulus, the alpha rhythm exhibits an immediate, sharp event-related desynchronization [Catalano et al., 2024].

By sending a digital marker exactly when the subject is instructed to open their eyes, the system can objectively prove its end-to-end synchronization integrity by tracking the absolute latency between the digital marker and the sudden drop in neural power spectral density [Palumbo et al., 2024]. If the system can reliably capture this spontaneous frequency modulation, it validates the entire pipeline for the extraction of highly sensitive, time-locked ERPs associated with targeting stimuli or withholding a response [Wascher et al., 2023]. The ability to perfectly fuse the digital interaction state with these precise analog signals confirms that the hardware isolation, noise reduction algorithms, and synchronization protocols have collectively succeeded in achieving the exact synchronization of biomarkers required for clinical analysis [Lin et al., 2023].

In summary, while current literature provides comprehensive methodologies for EEG ac-

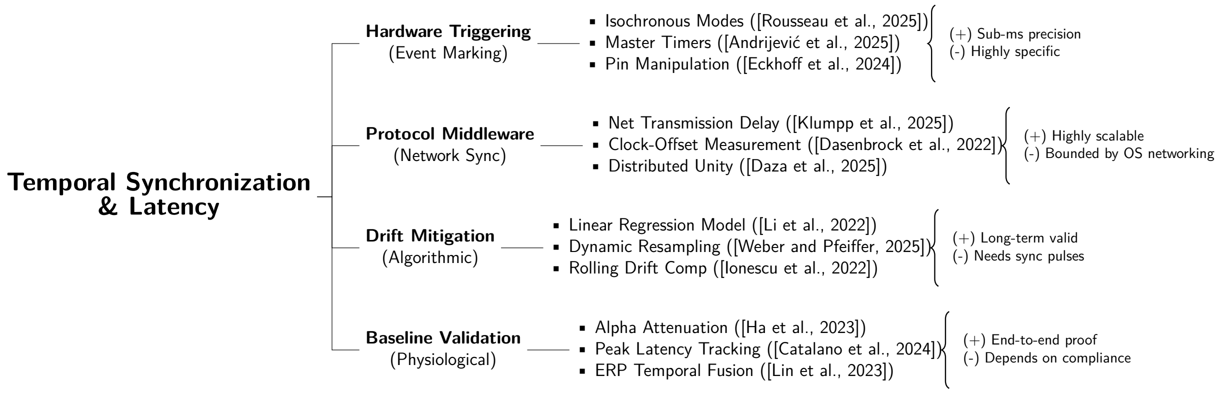

Figure 1-10: Taxonomy of methodologies for temporal synchronization and latency bounding in EEG biomarkers.

quisition, adapting these for clinical-grade pediatric ADHD assessment requires navigating the specific limitations of existing embedded architectures. For the first defined challenge overcoming SNR limitations and resource exhaustion dedicated high-resolution analog front-ends combined with active grounding and distributed edge-offloading present the most viable architecture. However, many current statistical and deep learning-based denoising alternatives impose computational overheads that inherently threaten real-time stability on constrained systems. Consequently, outcomes for this physical and computational problem must be explicitly measured by quantifying baseline input-referred noise against commercial standards and by conducting stress tests that monitor continuous CPU and RAM utilization to preclude data packet loss during high-frequency streaming. For the second challenge temporal synchronization and latency variability relying solely on software-level middleware or network protocols is limited by unpredictable operating system scheduling and display refresh delays. The most promising alternative rests on hardware-bounded event marking synchronized via explicit interrupt service routines. To validate outcomes for this synchronization challenge, evaluations must rigorously quantify short-term, non-deterministic communication jitter and measure cumulative clock drift over extended, full-length therapeutic sessions. Finally, these temporal metrics must be biologically anchored by executing physiological baseline validations, such as the alpha-band attenuation test, alongside strict signal isolation assessments to verify that the extracted, time-locked biomarkers are free from spatial crosstalk and genuinely reflect neurocognitive engagement.

1.5 Objectives

1.5.1 General Objective

To design, implement, and validate a hardware-synchronized embedded EEG acquisition architecture capable of mitigating mixed-signal interference and bounding non-deterministic communication latency to ensure the clinical validity of continuous neurocognitive assessments in pediatric ADHD.

1.5.2 Specific Objectives

1. To overcome physical deployment barriers and maximize signal efficiency by characterizing the user-experience of a new EEG cap design and systematically measuring electrode-skin impedance to optimize the initial analog interface.

2. To design and construct a robust EEG acquisition hardware architecture based on industry standards, quantifying its instrumental noise floor and monitoring computational resource consumption (CPU and RAM) to ensure stability during high-frequency data logging.

3. To guarantee deterministic event alignment by implementing direct hardware-level synchronization, executing rigorous end-to-end latency, jitter, and multimodal stress tests alongside physiological alpha-blocking validations to prove the elimination of non-deterministic temporal errors.

1.6 Contributions and Thesis Outline

In the following, we briefly introduce the main contributions of this thesis addressing the clinical translation challenges of continuous neurocognitive assessments in pediatric ADHD. They are summarized in Figure **1-11**.

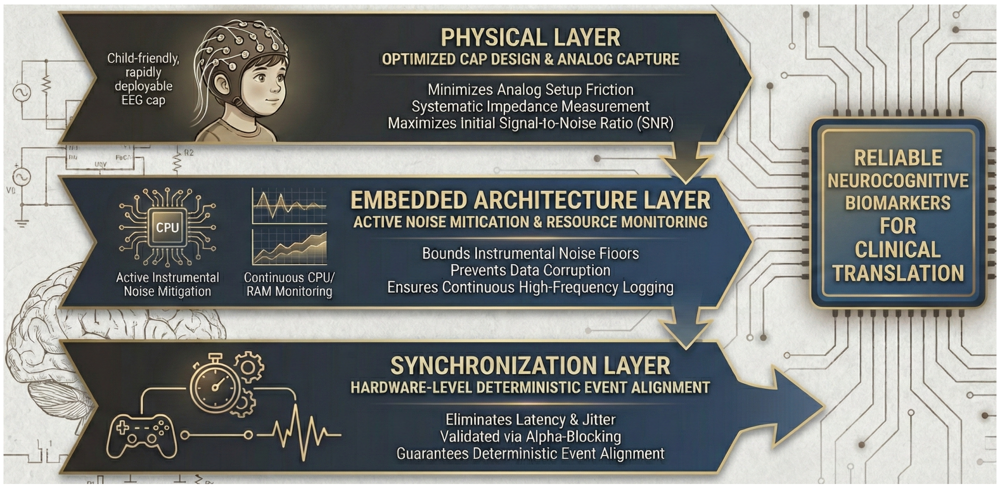

Figure 1-11: These three core contributions form a sequential, interdependent architecture designed to secure neurocognitive data validity. The architecture begins at the *Physical Layer* to secure a pristine baseline signal, passes to the *Embedded Architecture Layer* for noise mitigation and resource management, and concludes in the *Synchronization Layer* to guarantee deterministic event alignment.

These core contributions form a sequential, interdependent architecture designed to secure neurocognitive data validity. As illustrated in Figure **1-11**, only when all three sequential layers operate without failure can clinically valid Event-Related Potentials (ERPs) be extracted for accurate ADHD assessment.

1.6.1 Optimized Physical Interface and Analog Capture

A qualified tool for clinical neurocognitive assessments must overcome physical deployment barriers, especially when dealing with pediatric patients. The architecture begins at the physical layer, where minimizing analog setup friction is required to secure a pristine baseline signal.

Bearing this in mind, we propose a novel, rapidly deployable EEG cap design and a systematic electrode-skin impedance measurement protocol. This development overcomes physical barriers and maximizes the initial signal-to-noise ratio (SNR), ensuring high-fidelity analog input for the subsequent acquisition stages.

1.6.2 Robust Embedded Acquisition Architecture

The continuous, high-frequency logging of neurophysiological data is highly susceptible to instrumental noise and computational bottlenecks, which can lead to data loss or corruption during continuous assessments.

To mitigate these issues, this work presents the design and implementation of a robust EEG acquisition system. This embedded architecture features active instrumental noise mitigation to bound noise floors, alongside continuous system-level resource monitoring (CPU and RAM) to prevent data loss. This layer ensures that the high-fidelity analog input is properly digitized and managed without corruption.

1.6.3 Hardware-Level Temporal Synchronization

The effectiveness of cognitive assessments heavily depends on the system's ability to precisely align acquired physiological signals with external stimuli, requiring low latency and minimal jitter.

To achieve this, we developed a deterministic event-alignment framework that eliminates unpredictable communication latency and jitter. This synchronization layer processes the clean data stream, hardware-locking it to external game stimuli. This approach has been validated through rigorous end-to-end stress testing and physiological alpha-blocking assessments, definitively securing the clinical validity of ERPs.

1.7 Thesis structure

To detail the design, implementation, and empirical validation of these proposed contributions, the remainder of this thesis is structured as follows: Chapter 2 (*Theoretical Framework*) introduces the fundamental concepts underlying continuous EEG monitoring, the electrophysiological manifestations of ADHD, mixed-signal embedded hardware design, and principles of data synchronization. Chapter 3 (*Hardware Architecture*) details the methodology behind the physical EEG cap, the analog front-end components, and the digital processing unit, while also presenting initial empirical validations such as impedance characterization and embedded system stress testing. Chapter 4 (*Firmware Synchronization*) presents the temporal synchronization architecture, describing the firmware and software methods employed, and covering empirical validations like latency, jitter, multimodal stress tests, and physiological alpha-blocking. Finally, Chapter 5 (*Final Remarks*) summarizes the research findings, evaluates the performance against objectives, details academic contributions, and outlines directions for future improvements.

2 Theoretical Framework

The development of continuous neurocognitive assessment systems is grounded in the convergence of neurophysiological principles, precision electronic engineering, and computer science. This chapter systematizes the critical concepts required for understanding the proposed architecture, addressing the stochastic nature of biological signals, the electrophysiological manifestations of Attention-Deficit/Hyperactivity Disorder (ADHD), the principles of low-noise acquisition architectures, and the challenges inherent to temporal synchronization in heterogeneous digital systems.

2.1 Neurophysiology and Event-Related Potentials (ERPs)

Electroencephalography (EEG) constitutes a non-invasive technique for recording cerebral bioelectric activity via transducers arranged on the scalp. While continuous EEG analysis allows for the monitoring of basal brain states—such as wakefulness, sleep, or convulsive pathologies—cognitive neuroscience research requires isolating specific neuronal responses associated with sensory, motor, or cognitive stimuli. These voltage fluctuations, known as Event-Related Potentials (ERPs), represent the synchronized activity of pyramidal neuronal populations in response to information processing.

Within the complex morphology of ERPs, two endogenous components are of particular interest for neurocognitive evaluation and the implementation of serious games in the context of this project. The first is the N200 (or N2) component, a negative deflection that reaches its maximum amplitude between 200 and 350 ms post-stimulus. This component is functionally linked to executive control, specifically in mismatch detection processes and the inhibition of motor responses. The second component, the P300 (or P3b), manifests as a prominent positive deflection with a latency of 300 to 600 ms. Its amplitude is modulated by the allocation of attentional resources and the updating of working memory, being particularly sensitive to stimulus improbability (the *oddball* paradigm). Due to these characteristics, the P300 is consolidated as a robust biomarker for quantifying cognitive load and attentional deficits.

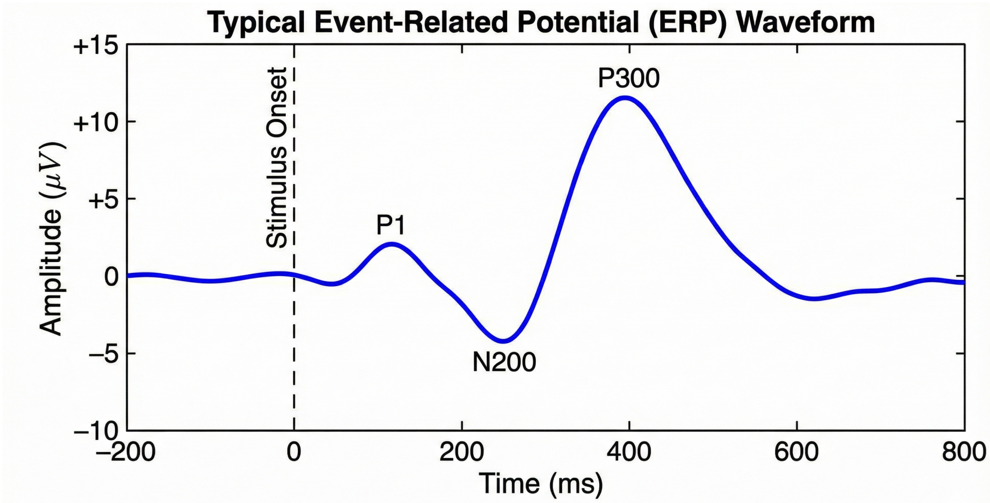

Figure 2-1: Characteristic morphology of an Event-Related Potential (ERP), highlighting exogenous and endogenous components such as the N200 and P300.

The detection of these components presents a significant challenge in signal processing due to their low signal-to-noise ratio (SNR). ERPs possess typical amplitudes in the range of $1\mu V$ to $20\mu V$, frequently remaining masked by background EEG activity, the magnitude of which oscillates between $50\mu V$ and $100\mu V$. To extract the signal of interest, the technique of coherent signal averaging is employed. Assuming that background noise is a stochastic process with zero mean and is uncorrelated with the stimulus, by averaging N trials, the noise amplitude decreases in proportion to $1/\sqrt{N}$, while the ERP signal remains constant.

However, the validity of this technique depends strictly on temporal stability. Variability in the synchronization marker's latency, a phenomenon termed *jitter*, introduces systematic errors in the resulting average. Mathematically, if the trigger latency follows a normal distribution with standard deviation σ_t, the averaging process acts as a low-pass filter on the original waveform, attenuating high-frequency components and distorting peak amplitude. A jitter greater than 10 ms ($\sigma_t > 10$ ms) is sufficient to degrade the morphology of the N200 component, compromising the diagnostic utility of the data. Consequently, acquisition systems must guarantee strict real-time (*hard real-time*) synchronization to preserve the spectral and temporal integrity of the biomarkers.

2.2 Electrophysiological Manifestations of ADHD

Attention-Deficit/Hyperactivity Disorder (ADHD) is a neurodevelopmental condition characterized by persistent patterns of inattention, hyperactivity, and impulsivity. Clinically, the diagnosis of ADHD relies heavily on behavioral observations and subjective rating scales. However, electrophysiological techniques offer objective biomarkers that reflect the underlying neurological atypicalities associated with the disorder.

In resting-state EEG, individuals with ADHD frequently exhibit an elevated Theta/Beta ratio (TBR) compared to neurotypical peers. This ratio reflects an excess of slow-wave (Theta) activity, often associated with cortical underarousal or drowsiness, and a deficit in fast-wave (Beta) activity, which is linked to active concentration and cognitive engagement. While the TBR has been extensively studied as a potential diagnostic metric, its clinical utility is complemented by the analysis of dynamic brain responses during cognitive tasks.

During cognitive paradigms, such as continuous performance tests (CPTs) or the *oddball* task, ERPs provide a window into the temporal dynamics of information processing in ADHD. The most consistent finding is a reduction in the amplitude of the P300 component. This attenuation is theorized to reflect deficits in the allocation of attentional resources and the updating of context in working memory. Furthermore, abnormalities in the N200 component are frequently observed, particularly during tasks requiring inhibitory control (e.g., Go/No-Go tasks). A reduced N200 amplitude in these contexts suggests difficulties in conflict monitoring and the suppression of prepotent motor responses, aligning with the impulsivity characteristic of the disorder.

Continuous EEG monitoring coupled with interactive tasks (like serious games) aims to systematically elicit and quantify these electrophysiological markers, providing a quantitative basis for assessing cognitive performance and the efficacy of therapeutic interventions in ADHD.

2.3 Principles of Mixed-Signal Embedded Hardware Design

The fidelity in the digitization of biopotentials is determined by the topology of the Analog Front-End (AFE). Modern acquisition architectures integrate specific analog-to-digital converters (ADCs) designed for biomedical instrumentation, which typically implement a Delta-Sigma ($\Delta\Sigma$) modulation architecture rather than traditional Successive Approximation Register (SAR) converters.

The $\Delta\Sigma$ architecture offers superior advantages in terms of dynamic range and noise rejection through two main mechanisms: oversampling and noise shaping. The device samples the input signal at a modulation frequency (f_{mod}) significantly higher than the Nyquist rate, distributing quantization noise power over a wider spectrum. Subsequently, the modulator shifts this noise toward high frequencies, outside the biological band of interest (0–100 Hz), allowing a digital decimation filter to eliminate it effectively while reducing the data rate to the output frequency configured by the user.

A critical aspect for functional connectivity and EEG coherence analysis is sampling simultaneity. In older multiplexed systems, a single ADC core switches sequentially between channels, introducing a systematic phase delay (t_{skew}) between electrodes. Modern biomedical ADCs mitigate this problem by incorporating independent $\Delta\Sigma$ modulators for each channel,

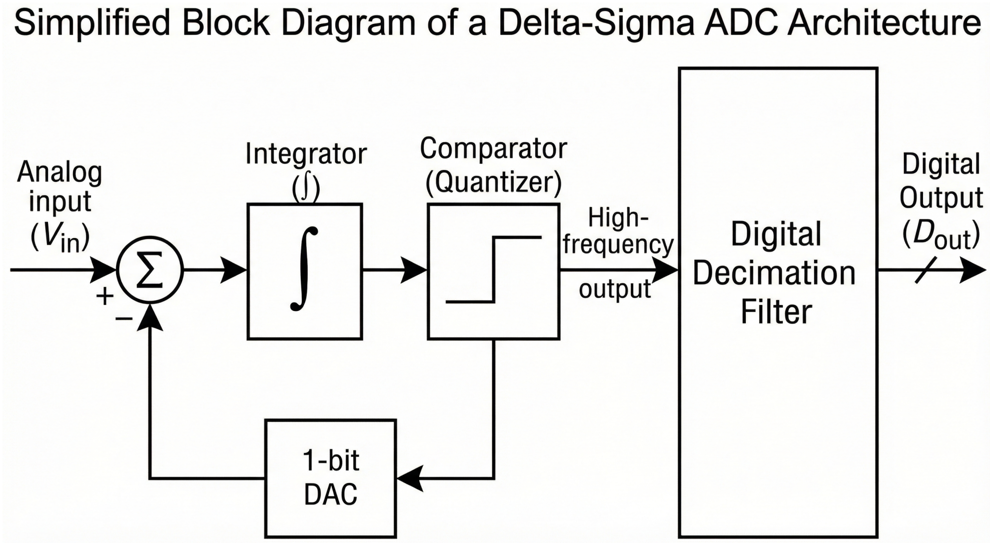

Figure 2-2: Simplified functional scheme of the modulation and filtering stage in a Delta-Sigma architecture ADC.

guaranteeing a virtually null t_{skew} and preserving the real phase relationship between different cortical regions.

To manage data flow without sacrificing temporal determinism, advanced acquisition designs adopt a heterogeneous computing architecture that decouples acquisition from high-level processing. This structure typically comprises a Microcontroller Unit (MCU) operating in real-time, coupled with a Microprocessor Unit (MPU) for complex application tasks. The MCU operates under strict real-time constraints (either on *bare-metal* or with a lightweight RTOS), reacting to ADC hardware interrupts on microsecond scales to capture and timestamp samples without buffer overflows. Meanwhile, the MPU manages computationally intensive and non-deterministic tasks, such as protocol stacks and file system storage. This division of responsibilities isolates bio-signal acquisition from the variable latencies introduced by high-level operating system schedulers, ensuring data temporal integrity.

2.4 Principles of Data Synchronization

Precise synchronization between physiological recordings and external events (such as visual/auditory stimuli in a game) constitutes a central technical challenge in BCI and neurocognitive assessment systems. The selection of a synchronization method implies a trade-off between temporal precision, implementation complexity, and intrusion into the user experience. Table **2-1** summarizes the characteristics of the predominant approaches.

There are contrasting approaches to addressing this problem. Optical synchronization, based

Table 2-1: Comparative analysis of synchronization methods for BCI systems.

Method	**Mechanism**	**Precision**	**Implementation**
Optical (Photodiode)	Physical detection of screen luminance changes by an external sensor.	High (< 1 ms)	High (Additional hardware required).
Network (LSL)	Synchronization via local network protocol and software jitter correction.	Medium (< 5 ms)	Low (Software only).
Hardware Trigger (TTL)	Direct electrical signal from Parallel/USB port to the ADC.	Very High (< 1 ms)	Medium (Requires specific interfaces).

on photodiodes attached to the monitor, is considered the "gold standard" for validation, as it detects the physical change of pixels, bypassing software, operating system, and GPU rendering latencies. However, its requirement for external hardware limits its viability in massive clinical deployments. As a scalable alternative, the *Lab Streaming Layer* (LSL) protocol offers a middleware solution that unifies disparate data streams by assigning timestamps referenced to a common clock and drift correction algorithms. While LSL simplifies integration, its final accuracy remains dependent on local network stability and the stimulation engine's ability to report the event time accurately.

In customized physical interfaces, standard buses like USB introduce non-trivial latency considerations, especially for the transmission of marking commands (*soft-triggers*) from a PC or tablet to an amplifier. As a host-controlled bus utilizing polling, data transfer is discretized into frame intervals (1 ms in *Full Speed*) or microframes ($125\mu s$ in *High Speed*). Additionally, data traverses the operating system driver stack, where it may be stored in intermediate buffers to optimize global system performance. This behavior introduces variable and unpredictable latencies of several milliseconds between the logical generation of an event and its physical arrival at the bus, which is fundamentally incompatible with the precision requirements for high-frequency ERP component analysis. To mitigate this latency indeterminacy, modern embedded designs must implement hardware-level synchronization protocols that couple event markers directly to biological samples at the lowest possible layer before routing to non-deterministic operating systems.

3 Hardware Architecture (The MONEEE System)

The engineering design of the MONEEE system addresses the critical need to capture low-amplitude biopotentials with a high signal-to-noise ratio, while simultaneously guaranteeing low-latency synchronization with external events. To satisfy these requirements, a heterogeneous embedded computing architecture has been implemented, physically decoupling the real-time acquisition domain from the high-level computational domain. This separation allows each subsystem to be optimized for its specific function: signal integrity and determinism for acquisition, and performance and connectivity for processing.

3.1 System Topology and Data Flow

The device operates under an *edge-computing* paradigm, dedicating its resources exclusively to EEG signal management. The architecture establishes a strictly unidirectional data flow from the patient toward the processing unit, designed to minimize transport latency. The signal chain is formally modeled by the following transduction and transmission sequence:

$$\text{Electrodes} \xrightarrow{\text{Analog}} \text{ADS1299} \xrightarrow{\text{SPI}} \text{TM4C1294} \xrightarrow{\text{SPI}} \text{RPi CM4} \tag{3-1}$$

As illustrated in Figure **3-1**, the hardware is structured into three differentiated functional zones: the Analog Front-End (AFE), the Real-Time Core, and the Compute Core. This segmentation is not merely logical but physical, employing isolation barriers to protect the integrity of physiological measurements.

For this project, we have established the MONEEE system as a robust electronic design aligned with acquisition systems in its segment. The designs presented in Figures **3-2**, **3-3**, **3-4**, **3-5**, **3-6**, and **3-7** illustrate our proposal for an EEG signal acquisition board, conceived to significantly improve the capacity of real-time BCI systems, overcoming current challenges and contributing to the advancement of technology in this field.

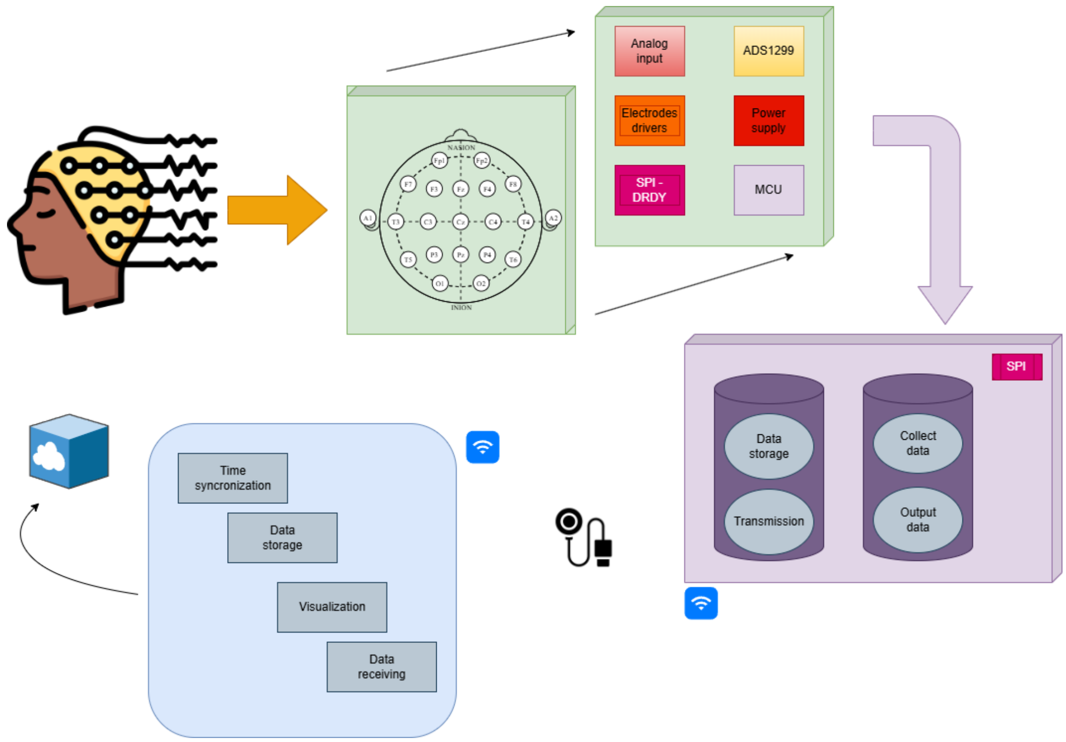

Figure 3-1: Block diagram of the MONEEE architecture, evidencing the segregation between the deterministic acquisition (MCU) and high-level processing (MPU) domains.

3.1.1 Electronic Design

The following schematic designs constitute the complete electronic architecture of the MONEEE system, divided by their primary functions.

3.2 Analog Front-End (AFE) and Biomedical Interface

The interface between the biological medium and the digital system is realized via the Texas Instruments ADS1299 integrated circuit. This component, a 24-bit analog-to-digital converter (ADC) with 8 simultaneous channels, has been specifically configured to optimize surface electroencephalography capture.

To maximize effective resolution on signals typically oscillating between 10 and $100\mu V$, the internal Programmable Gain Amplifier (PGA) is set to a gain of $24V/V$. Likewise, the sampling rate is fixed at 250 SPS or 500 SPS. This frequency provides a bandwidth that exceeds Nyquist requirements for the spectral components of interest (P300 and N200, generally located below 30 Hz), while allowing for the advantages of oversampling to reduce the noise floor. The input multiplexer is maintained in NORMAL mode for electrode acquisition,

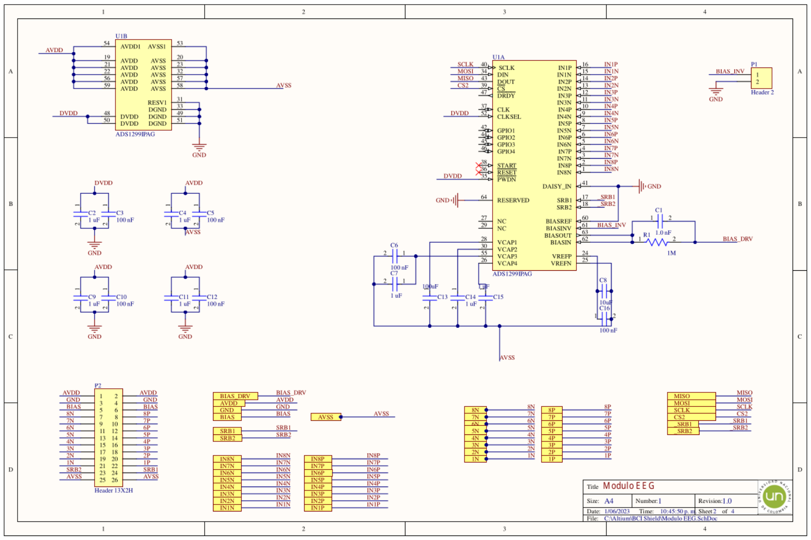

Figure 3-2: Schematic design for the module responsible for acquiring EEG signals.

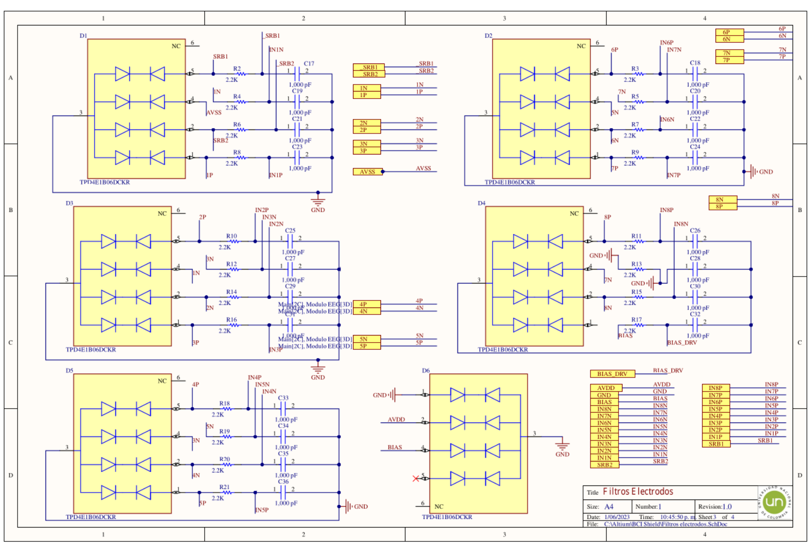

Figure 3-3: Schematic design of coupling filters.

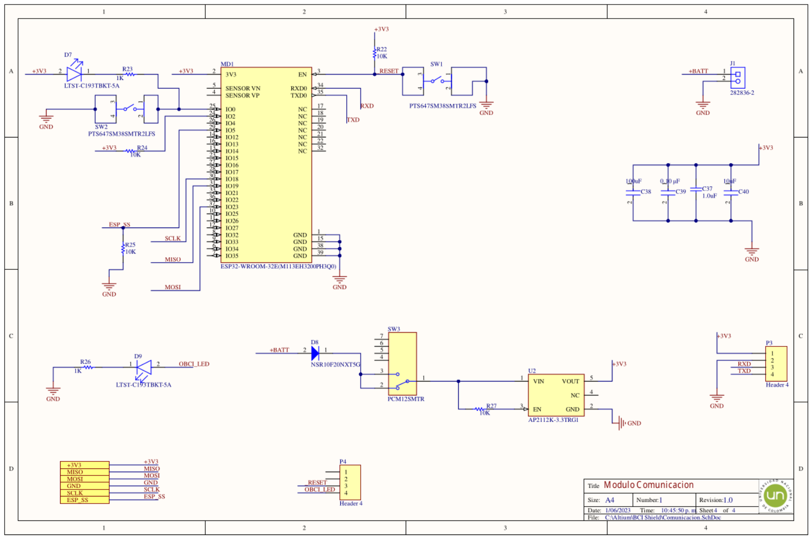

Figure 3-4: Schematic design of the module responsible for communicating the collected data to another device or to the cloud.

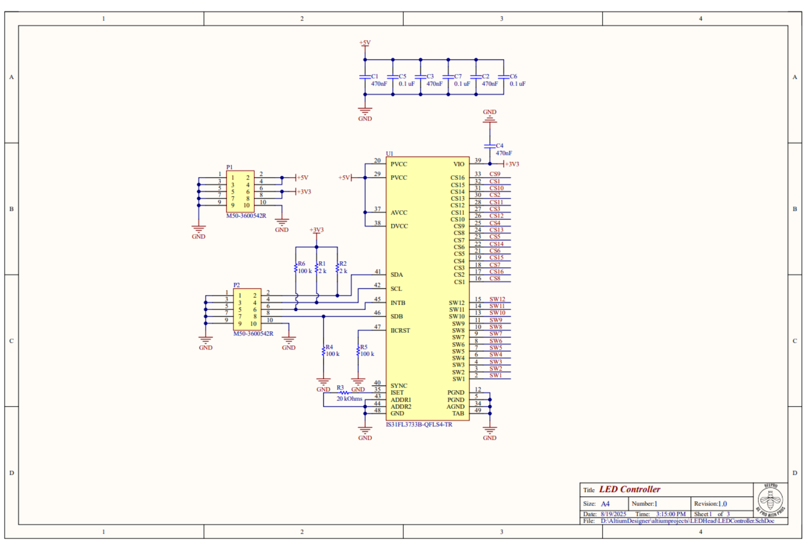

Figure 3-5: Module for impedance visualization of the electrodes.

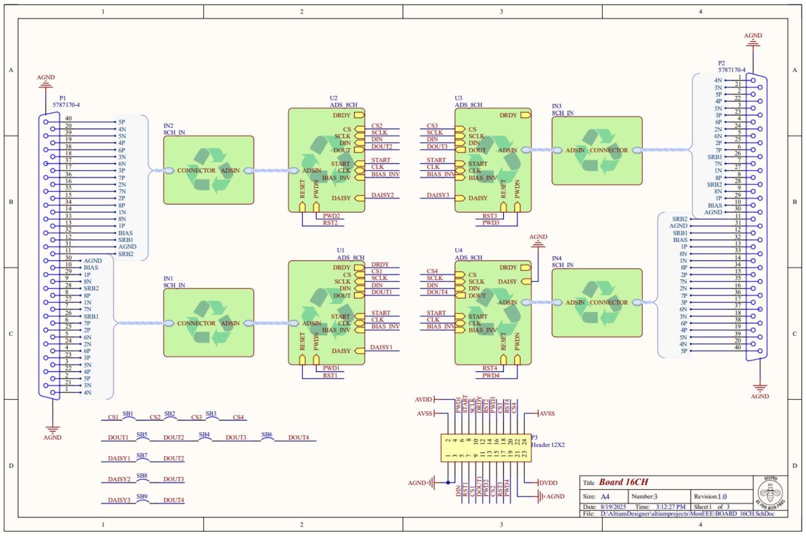

Figure 3-6: Connection between the different ADS1299 acquisition modules.

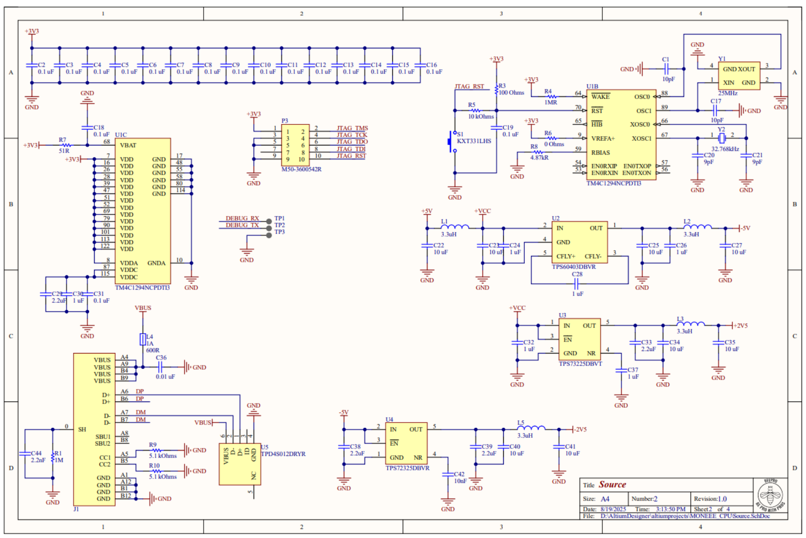

Figure 3-7: Motherboard for microcontroller and microprocessor.

preserving the capability to internally switch toward test signals for self-calibration routines.

The suppression of electromagnetic interference, primarily 50/60 Hz mains noise, is managed through an active Driven Right Leg (DRL) topology. Unlike a passive ground reference, the ADS1299's *Bias Drive* circuit monitors the common-mode voltage present at the detection electrodes. This signal is inverted, amplified, and reinjected into the patient's body through the reference electrode. This negative feedback loop actively cancels interference, raising the Common-Mode Rejection Ratio (CMRR) to levels exceeding 110 dB, which is indispensable for unshielded clinical environments.

Finally, signal integrity is ensured through rigorous power management. The AFE is powered by a dedicated Li-Po battery and regulated by a PMIC (Power Management Integrated Circuit). The analog power domain ($AVDD$) is isolated from digital rails via Low-Dropout Regulators (LDOs) with high Power Supply Rejection Ratio (PSRR). This strategy prevents high-frequency switching noise, inherent to CPU operation in the compute module, from capacitively coupling to the amplifier input stages.

3.3 The Digital Core: Heterogeneous Processing

The digital architecture implements a shared responsibility model, distributing the computational load between a real-time microcontroller and an application microprocessor.

The Real-Time Unit, driven by a Texas Instruments TM4C1294 (ARM Cortex-M4F), serves as the acquisition system master. Operating in a *bare-metal* environment or under a lightweight real-time operating system, the TM4C ensures deterministic performance. Its primary role is to immediately service the `DRDY` (Data Ready) hardware interrupt generated by the ADC, guaranteeing lossless sample capture. Moreover, the integration of a Floating-Point Unit (FPU) allows for the application of in-situ digital pre-processing—such as notch filtering or scaling—without impacting interrupt service latency. At this critical juncture, each sample is assigned a hardware *timestamp*, achieving microsecond-level temporal precision.

Data is subsequently routed to the Compute Unit, implemented via a Raspberry Pi Compute Module 4 (CM4). Executing a full Linux operating system, this module is tasked with higher-level organizational roles: mass storage management, deployment of the *Lab Streaming Layer* (LSL) gateway, and telemetric transmission over Wi-Fi. The CM4 aggregates the continuous data stream transmitted by the microcontroller and packages it into standardized structures suitable for consumption by the interactive game software.

Communication between the real-time and compute cores depends on a high-speed serial interface (UART operating at $>$ 921600 baud or SPI). To guarantee patient safety and preserve signal integrity, this digital link utilizes galvanic isolation (e.g., standard digital isolators like the ISO77xx series). This configuration prevents the formation of ground loops between the battery-powered floating acquisition stage and any peripheral connected to the electrical grid. The communication protocol relies on lightweight binary frames that encapsulate the 24-bit data alongside their corresponding timestamps; these frames are authenticated by a Cyclic Redundancy Check (CRC) to verify transmission integrity.

3.4 Event Synchronization Interface (USB-C)

Synchronization with the stimulation platform (e.g., a tablet) is physically facilitated by a USB Type-C port. Managed by the system's USB controller, this interface enables the reception of .$^{\text{ev}}$ent markers"generated by the game software at the precise instance of stimulus presentation. Because standard commercial devices introduce considerable electrical noise—primarily due to internal DC-DC converters—the MONEEE framework employs total isolation of the USB bus. The differential data lines ($D+/D-$) are routed through a specialized isolation integrated circuit (e.g., the ADuM3160), actively eliminating galvanic continuity.

To handle the transmission of these synchronization markers from the software side, the system deploys `MoneLib`, a custom library that bridges the Unity-based simulation environment with the embedded hardware. Compiling as a native Android plugin (`.aar`), this library empowers the game engine to communicate directly with the USB Host subsystem of the tablet. The associated software architecture strictly mandates an Android device running version 12 (Snow Cone) or later with robust USB-C Host support in order to initialize the communication driver properly.

The underlying communication protocol is streamlined for low latency by encoding game events—such as player selections or application states—into lightweight hexadecimal values transmitted over USB. For example, marking an .$^{\text{O}}$"transmits `0x00`, asserting an "X"transmits `0x01`, and initiating a system restart triggers `0xFF`. To preserve signal integrity and preclude the saturation of the USB channel, the protocol enforces a mandatory safety interval of exactly one millisecond between consecutive event transmissions.

Through this systemic interface, the "Serious Game.$^{\text{a}}$cts as a precision stimulation trigger. Whenever a user interacts with the application, the `MoneLibrary.SendUsbData` routine is immediately invoked, securely dispatching the corresponding integer to the downstream microcontroller. The incoming hardware event is subsequently captured and precisely timestamped by the embedded USB peripheral, ensuring that the subjective cognitive task tightly correlates with the objective physiological recording, thus enabling robust post-hoc analysis.

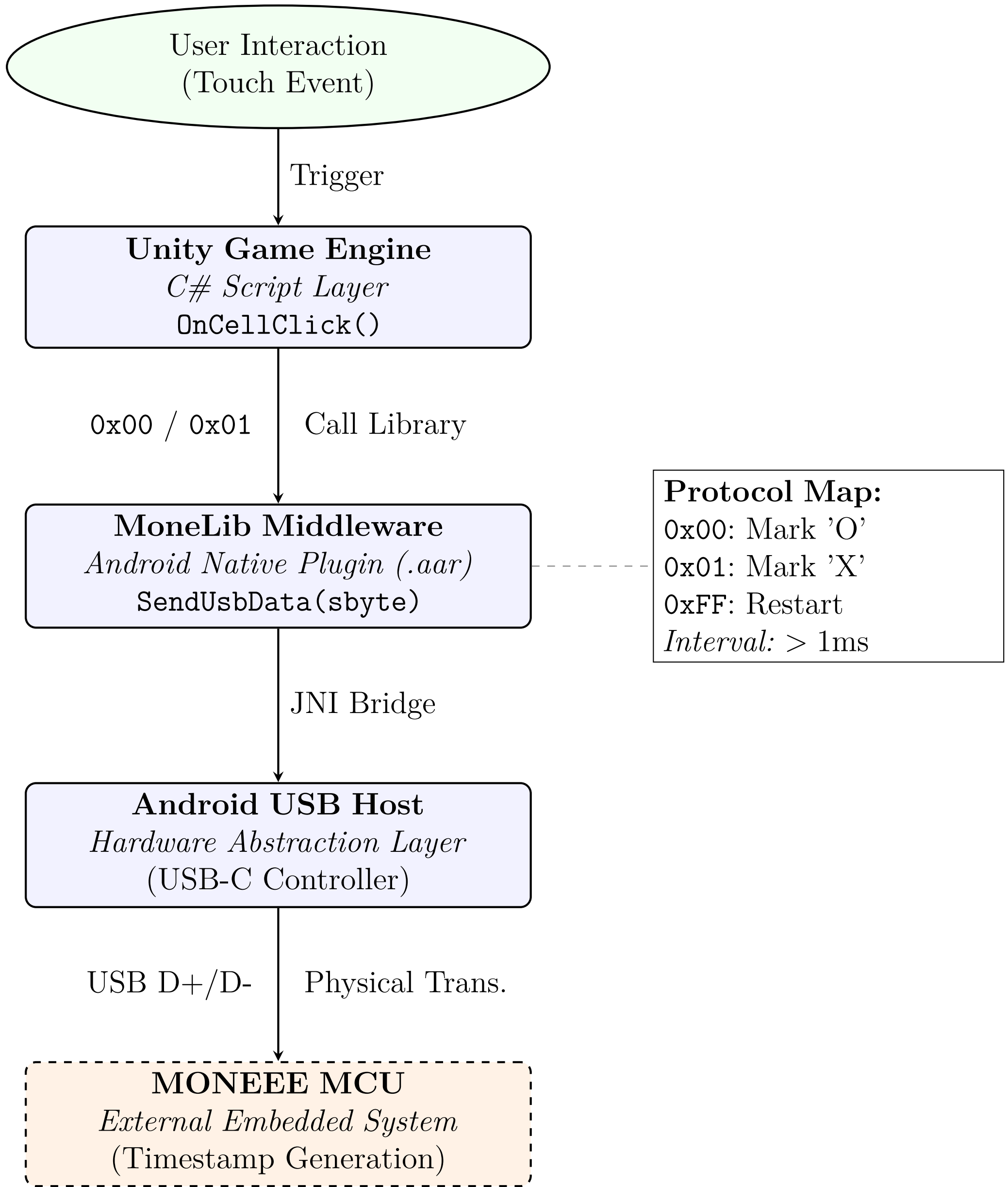

Figure 3-8: Data flow diagram of the Event Synchronization Interface. The high-level interaction within Unity is transduced into a hexadecimal marker by the MoneLib middleware and transmitted via the USB isolation barrier to the MONEEE acquisition core.

3.4.1 Desktop Application: MONEEE Visualizer

To complement the embedded hardware architecture and provide a comprehensive interface for data monitoring, a dedicated EEG signal analytical suite known as the MONEEE Visualizer was developed. This application facilitates the real-time observation and analysis of the acquired electroencephalographic data streams. By employing this tool, researchers can actively monitor signal quality, verify electrode contacts, and validate overall system performance iteratively during experimental paradigms. The graphical user interface of the MONEEE visualizer is documented in Figure **3-9**.

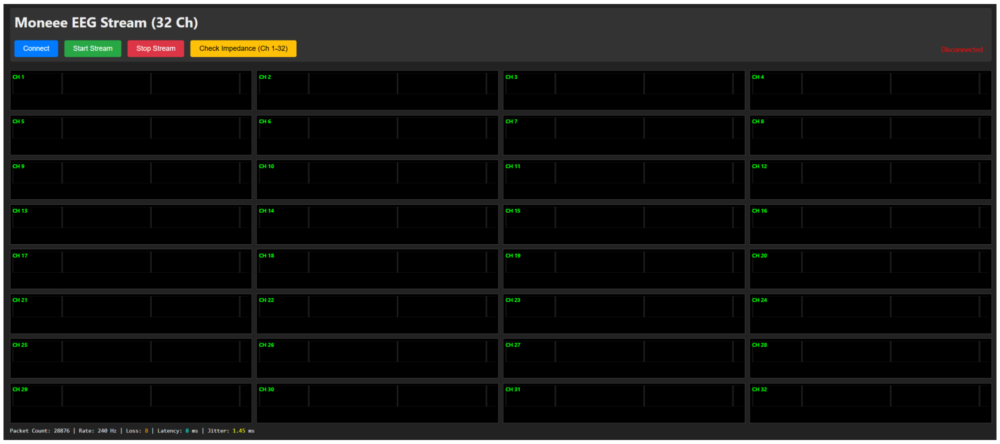

Figure 3-9: Graphical user interface of the MONEEE visualizer.

3.5 Hardware Validation Strategy

To rigorously demonstrate that the MONEEE system satisfies the stringent prerequisites for clinical-grade EEG acquisition, an initial sequence of hardware validation tests has been established. These structured protocols are purposefully designed to verify the fidelity of the physical interface and characterize the baseline analog performance of the system prior to any digital integration or filtering.

3.5.1 Use and Impedance Measurement Test of the New Cap

Maintaining optimal electrode-skin contact is fundamental for acquiring high-quality EEG recordings. This test systematically evaluates the usability and anatomical congruence of the custom EEG cap, verifying the application of consistent mechanical pressure across the scalp. Consequently, the electrical impedance of the electrode-skin interface is actively quantified utilizing the integrated lead-off detection circuitry of the ADS1299. This subsystem injects a calibrated AC or DC excitation current directly into the electrodes, allowing the MCU to derive and monitor contact quality in real time. The resulting impedance status is visually communicated to the operator via the dedicated impedance visualization module (Figure **3-5**), facilitating rapid, localized adjustments prior to commencing an experimental paradigm. A visual representation of this impedance checking sequence is provided in Figure **3-10**.

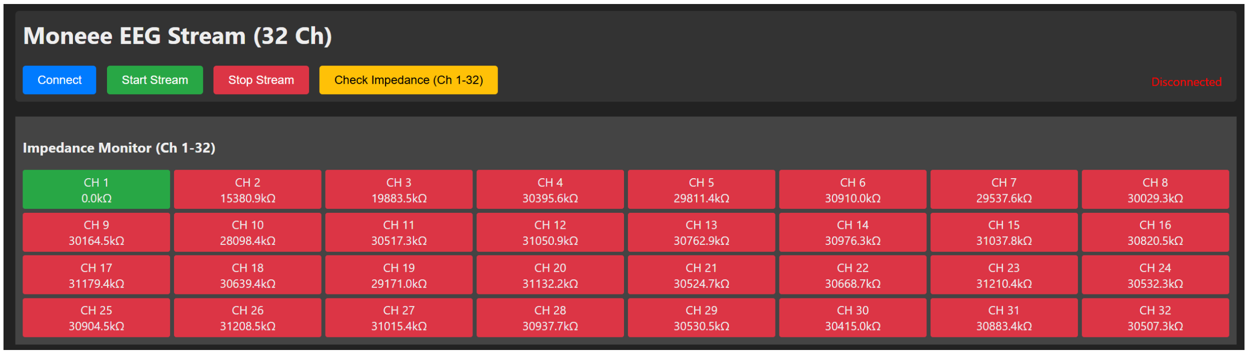

Figure 3-10: Visualization of the impedance checking process.

3.5.2 Instrumental Noise Characterization (Noise Floor)

To validate the capacity of the Analog Front-End to accurately digitize microvolt-level physiological signals, an instrumental noise baseline characterization is performed. During this evaluation, the input channels of the ADS1299 are internally shorted to ground, effectively quantifying the intrinsic electronic noise generated by the internal amplifiers and the ADC, independently of ambient interference or skin impedance loading. The resulting input-referred noise floor is analyzed to ensure that both the peak-to-peak and root-mean-square (RMS) noise magnitudes comply with the sub-microvolt specifications necessary for the reliable extraction of subtle Event-Related Potentials (ERPs). It is important to note that the graph presented in Figure **3-11** exhibits elevated values because the test was conducted in an environment with high external noise caused by interference from adjacent equipment.

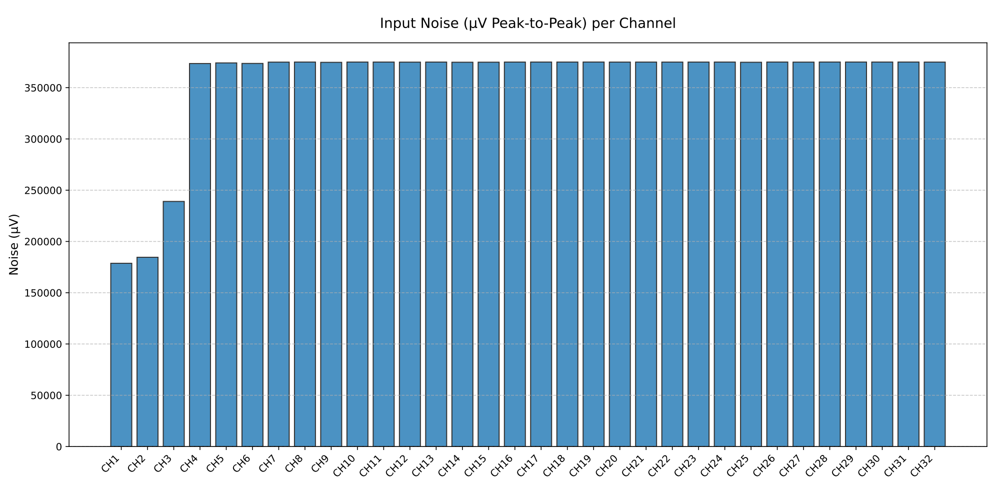

Figure 3-11: Instrumental noise characterization with the ADS1299 inputs internally short-circuited. The elevated values observed are indicative of interference generated by adjacent external equipment during the test.

4 Firmware Architecture and Temporal Synchronization Strategy

This section delves into the embedded computational logic governing the MONEEE hardware and its interface with the simulation environment. It describes the central methodological contribution of this development: a hardware-level event injection mechanism designed to mitigate the stochastic latency inherent to general-purpose operating systems, thereby achieving precise synchronization between physiological data and game stimuli at the microcontroller (MCU) level.

4.1 Deterministic Firmware Design on the TM4C1294

The firmware resident on the Texas Instruments TM4C1294 microcontroller has been structured under a *bare-metal* paradigm (dispensing with a complex operating system) to guarantee strictly deterministic behavior. The software architecture is event-driven, establishing an execution hierarchy where data acquisition holds maximum priority, subordinating any communication or maintenance tasks.

The synchronization engine depends on the precise management of the `DRDY` (Data Ready) interrupt signal generated by the ADS1299 converter. This signal activates the capture logic at the programmed sampling frequency (e.g., 250 Hz, corresponding to a 4 ms period).

The sequence of operations within the Interrupt Service Routine (ISR), as illustrated in Figure **4-1**, is critical for maintaining the system's phase coherence. Upon detection of the falling edge of the `DRDY` signal, the microcontroller activates the *Chip Select* (`CS`) line of the SPI bus and initiates a Direct Memory Access (DMA) transfer. This mechanism allows for the automatic reading of 24 bytes of data (8 channels of 24 bits plus status bits) without CPU intervention, which is reserved for managing storage in a circular buffer and verifying event flags.

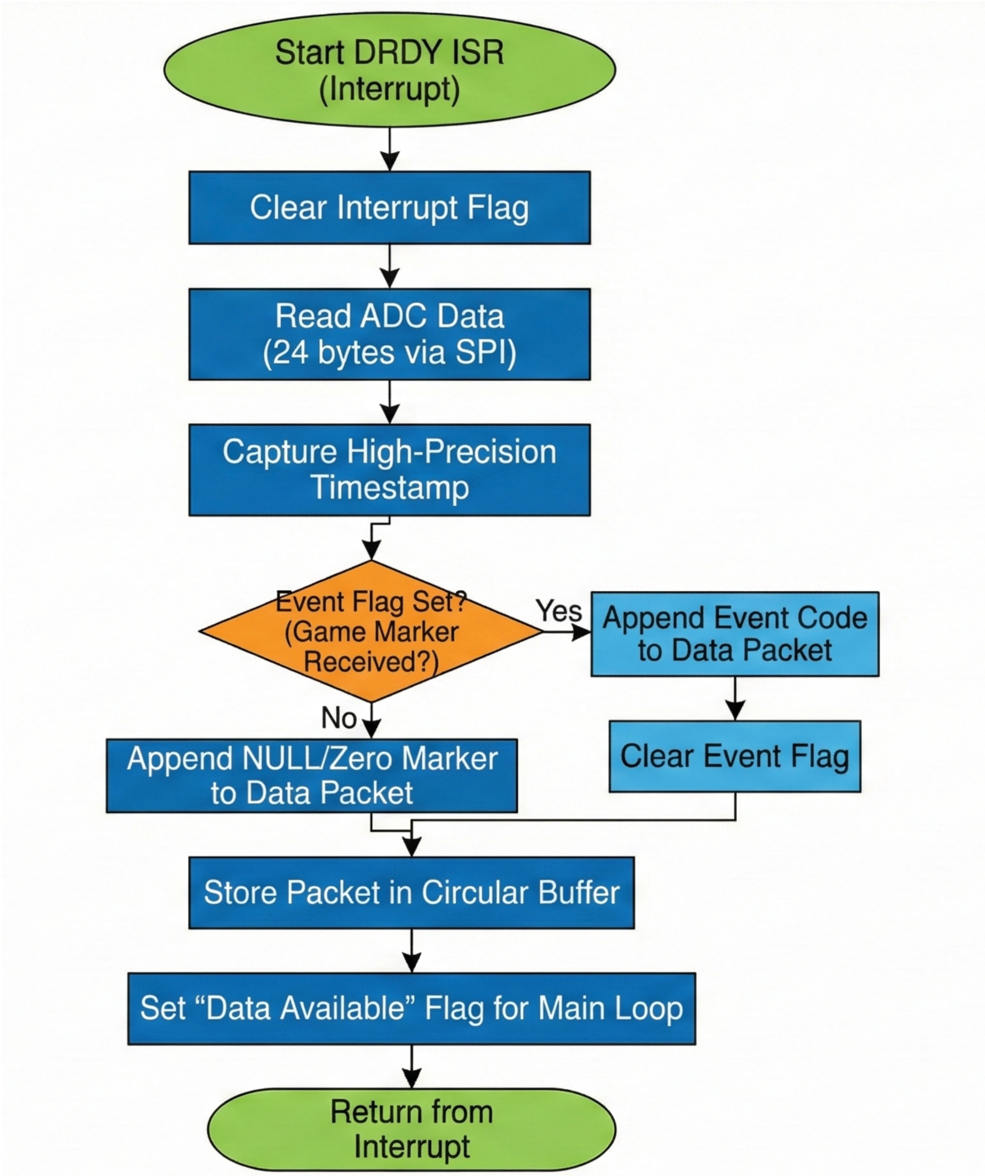

Figure 4-1: Flowchart of the Interrupt Service Routine (ISR) associated with the Data Ready signal (DRDY).

4.1.1 Hardware Event Injection Strategy (MCU-to-Aggregator Egress Protocol)

To resolve the problem of temporal desynchronization, the system design dispenses with PC or Raspberry Pi clocks for event *timestamping*. Instead, a direct injection strategy into the data frame is implemented. This protocol governs the egress data flow from the microcontroller to the aggregation node.

The operation of this mechanism is based on the immediate reception of commands. When the stimulation software (Game) generates a visual event, it transmits an 8-bit hexadecimal code (e.g., `0x0A`) via the USB-C interface to the TM4C. The arrival of this byte triggers a high-priority interrupt in the MCU, which immediately stores the value in a volatile register named `Current_Event`. During the subsequent ADS1299 sampling cycle (which occurs within an interval of less than 4 ms), the ISR queries this register and concatenates the event code directly to the end of the EEG data packet in progress. In this way, the event marker and the physiological sample become physically linked within the same data structure before being transmitted to the Linux environment. This approach ensures that the relative *jitter* between the stimulus and the biological response is virtually null, bounded only by the temporal resolution of the sampling period.

To formalize this linkage between physiological data and event markers, the system employs a specific hexadecimal frame structure for serial transmission to the aggregation node, as visualized in Figure **4-2**. In this encoding scheme, the initial three bytes are strictly reserved for control data, thereby eliminating the need for post-hoc timestamp realignment. The first byte acts as a binary Event Flag (B_0), explicitly indicating the presence of a synchronization trigger with a value of `1` or a resting state with `0`. The second byte (B_1) designates the Event Type, carrying the specific code required to classify the nature of the stimulus (e.g., distinguishing between target and standard inputs, populated directly from the `Current_Event` register). This metadata is immediately followed by the third byte (B_2), which serves as a static Start-of-Frame delimiter (`0xFE`) to identify the beginning of the physiological data payload. By packaging the event markers and the EEG signal within this same atomic transmission unit, the system transforms the synchronization problem into a data parsing task, ensuring that the relative phase relationship is preserved regardless of the jitter introduced by subsequent USB communication or operating system schedulers.

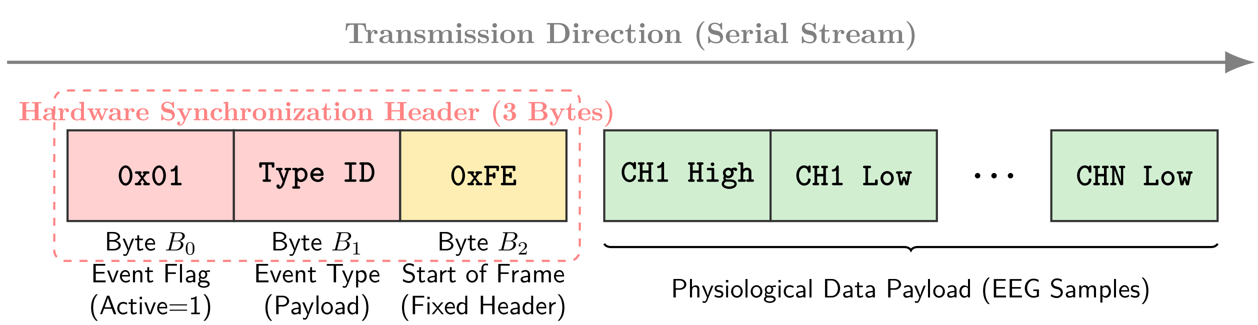

Figure 4-2: Visual representation of the MONEEE serial data transmission frame. The initial three bytes (B_0, B_1, B_2) form a dedicated hardware synchronization prefix attached to every physiological sample, ensuring that event timing is locked to the data stream before transmission to the CM4.

4.2 Integration Protocol with the Simulation Environment (Tablet-to-MCU Ingress Protocol)

Interaction with the serious game, developed in the Unity engine, is managed via a custom communication library that acts as an abstraction layer over the tablet's serial API. This library exposes high-level methods, such as `SendMarker(int code)`, which are invoked by the game logic at the exact instant of stimulus rendering.

To guarantee the integrity of commands transmitted over the USB link and prevent the erroneous interpretation of electromagnetic noise as valid events, a robust binary communication protocol (Ingress Protocol) has been defined for the Stimulus-to-MCU link. The transmission structure consists of 3-byte frames, detailed in Table **4-1**, which is distinct from the 3-byte MCU-to-CM4 egress protocol described in Section 4.1.

Table 4-1: Definition of the Serial Event Transmission Protocol.

Byte 0 (Header)	Byte 1 (Payload)	Byte 2 (Footer)
Start Marker `0xFF`	Event Code `0x00 - 0xFE`	Validation `0xAA`

The protocol uses the byte `0xFF` to signal the start of a transaction, followed by the event identifier (where specific codes denote states such as login, standard stimulus, or *oddball* stimulus). The frame concludes with the byte `0xAA`, used for integrity validation; any sequence that does not respect this structure is immediately discarded by the TM4C firmware, ensuring high noise immunity.

4.3 Processing in the Compute Module (Raspberry Pi CM4)

The Raspberry Pi Compute Module 4 plays the role of an aggregation node and data gateway. While strict synchronization is the responsibility of the microcontroller, the CM4 must process the information flow with sufficient efficiency to prevent communication buffer overflows.

To minimize operating system-induced latency, the Linux kernel on the CM4 has been optimized using the *PREEMPT_RT* patch. This modification transforms Linux into a real-time operating system, allowing execution threads associated with hardware drivers (such as the UART receiver) to preempt standard user-space processes. Additionally, core isolation techniques are employed (*CPU shielding* via the `isolcpus` parameter), dedicating specific processor cores exclusively to data ingestion and freeing them from non-critical interruptions such as Wi-Fi network management or the graphical interface.

Finally, the application software on the CM4, developed in a hybrid Python/C++ environment, ingests the binary packets coming from the TM4C, extracts the injected event markers, and reformats the continuous stream to the Extensible Data Format (XDF) standard. This format, native to the *Lab Streaming Layer* (LSL) middleware, allows multimodal time series to be encapsulated, facilitating the coexistence of EEG samples and discrete event markers in parallel streams with a unified time base, thus optimizing analytical post-processing.

4.4 System Integration and Performance Validation

This section outlines the validation protocols designed to evaluate the computational performance, temporal accuracy, and overall systems integration of the MONEEE architecture. These tests specifically verify the efficacy of the deterministic firmware processes detailed in Section 4.1 and the synchronization interfaces discussed in Section 4.2.

4.4.1 Computational Resource Consumption Analysis

Monitoring the computational resource consumption (CPU and RAM) is critical to ensure stability during high-frequency data logging. Because unoptimized continuous data logging demands substantial computational power and can rapidly induce I/O bottlenecks and RAM saturation, it is necessary to profile the operational envelope of both the TM4C1294 microcontroller and the Raspberry Pi CM4. This analysis quantifies CPU utilization, memory allocation, and interrupt latency limits under continuous acquisition at the maximum sampling rate. The objective is to verify that the real-time *bare-metal* core maintains deterministic execution without buffer overflows and that the CM4 reliably sustains the Lab Streaming Layer (LSL) backend, benefiting from the *PREEMPT_RT* kernel patch optimizations without thermal throttling or resource exhaustion. The results of this consumption profiling are presented in Figure **4-3**.

4.4.2 Channel Integrity Verification Using Jitter and Latency

To eliminate unpredictable communication jitter that skews the temporal alignment between stimulus and response, the deterministic nature of the data flow from the ADC to the processing unit is assessed by characterizing transmission jitter and internal latency. This test monitors the variability in the temporal spacing between consecutive data packets across

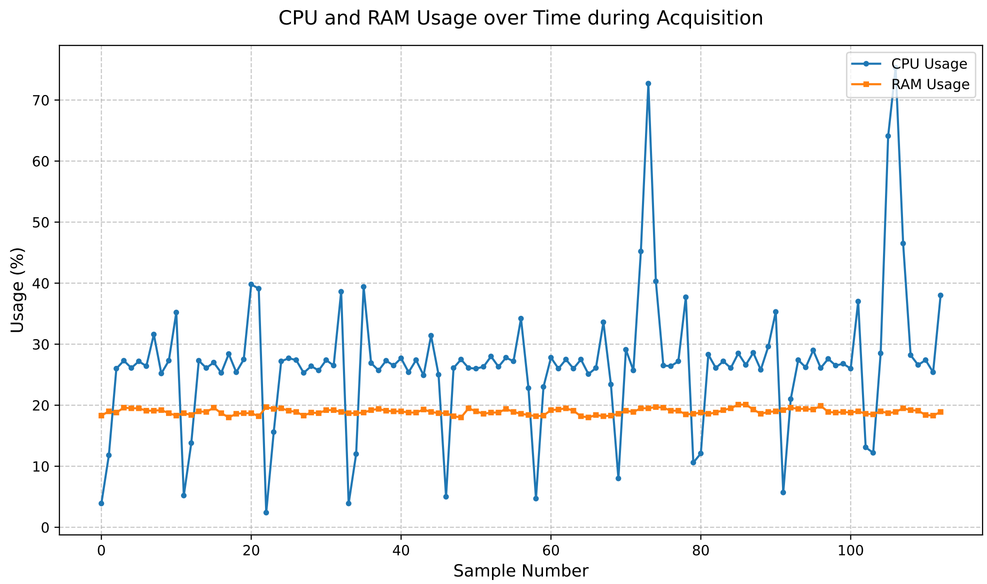

Figure 4-3: Measurements of CPU and RAM usage during continuous EEG signal acquisition.

the SPI and serial interfaces. By quantifying the time deviation (jitter) in the `DRDY` interrupt handling and the subsequent inter-core communication, the system guarantees that the strict temporal structure of the digitized EEG stream is preserved prior to network transmission, as evidenced by the jitter measurements in Figure **4-4**.

4.4.3 End-to-End Latency Quantification

To ensure precise temporal synchronization, the overall delay from biological phenomenon to software availability must be strictly bounded. This end-to-end latency test measures the absolute time elapsed between the generation of an analog test signal at the electrode inputs and the corresponding timestamped arrival of that signal peak in the host computer's LSL stream. Furthermore, the synchronization accuracy of the hardware event injection strategy via the USB interface is evaluated against the acquired EEG data to determine the maximum temporal misalignment between the Unity stimulation markers and the physiological recording, proving the elimination of non-deterministic temporal errors. The resulting end-to-end latency distribution is depicted in Figure **4-5**.

4.4.4 Multimodal Transmission Stress Test (Jitter and Packet Loss)

To validate the reliability of the wireless communication link and mitigate the risk of cumulative temporal drift in extended sessions, the system is subjected to a multimodal transmission stress test. Standard pediatric ADHD evaluations demand sustained, uninterrupted engage-

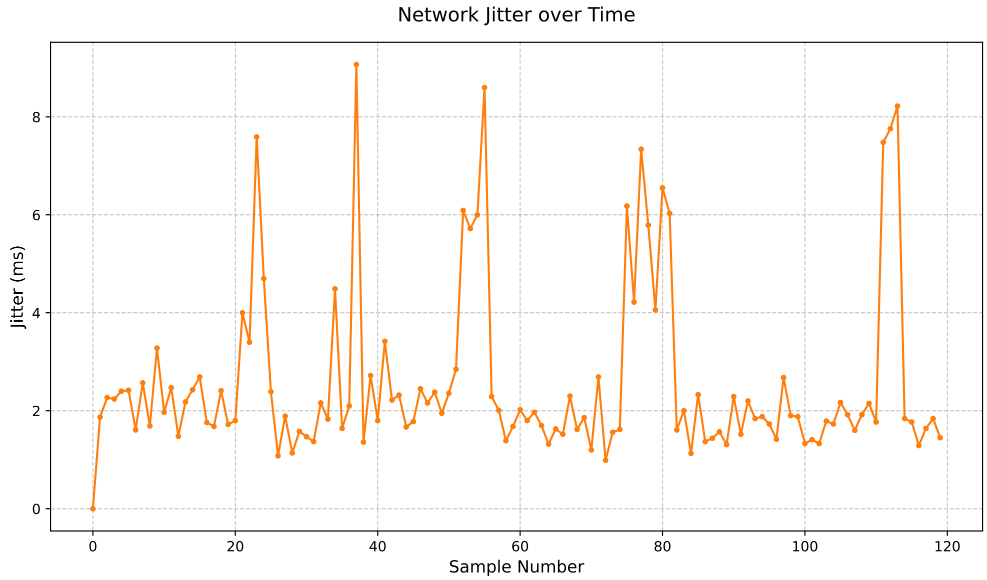

Figure 4-4: Jitter measurements during EEG signal acquisition and transmission.

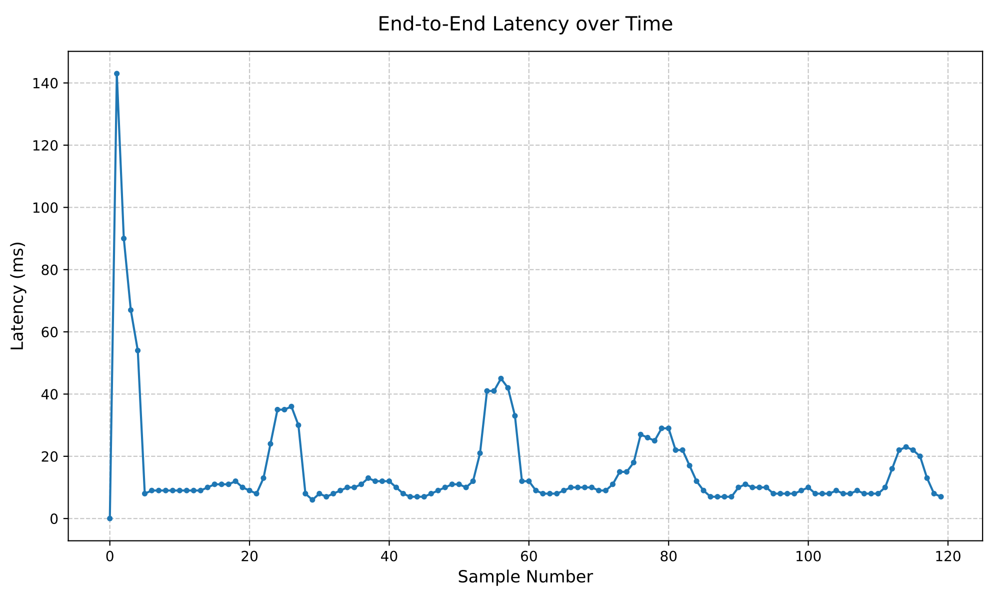

Figure 4-5: End-to-end latency measurements during event synchronization and EEG acquisition.

ment; thus, the Raspberry Pi CM4 continuously streams multi-channel EEG data over the Wi-Fi network interface under varying levels of network congestion and prolonged operational durations. The test quantifies packet loss rates and connection dropouts, verifying the robustness of the networking stack and the 3-byte binary encapsulation protocol established in Section 4.2 in maintaining an uninterrupted continuous data flow. The observed packet loss over time is illustrated in Figure **4-6**.

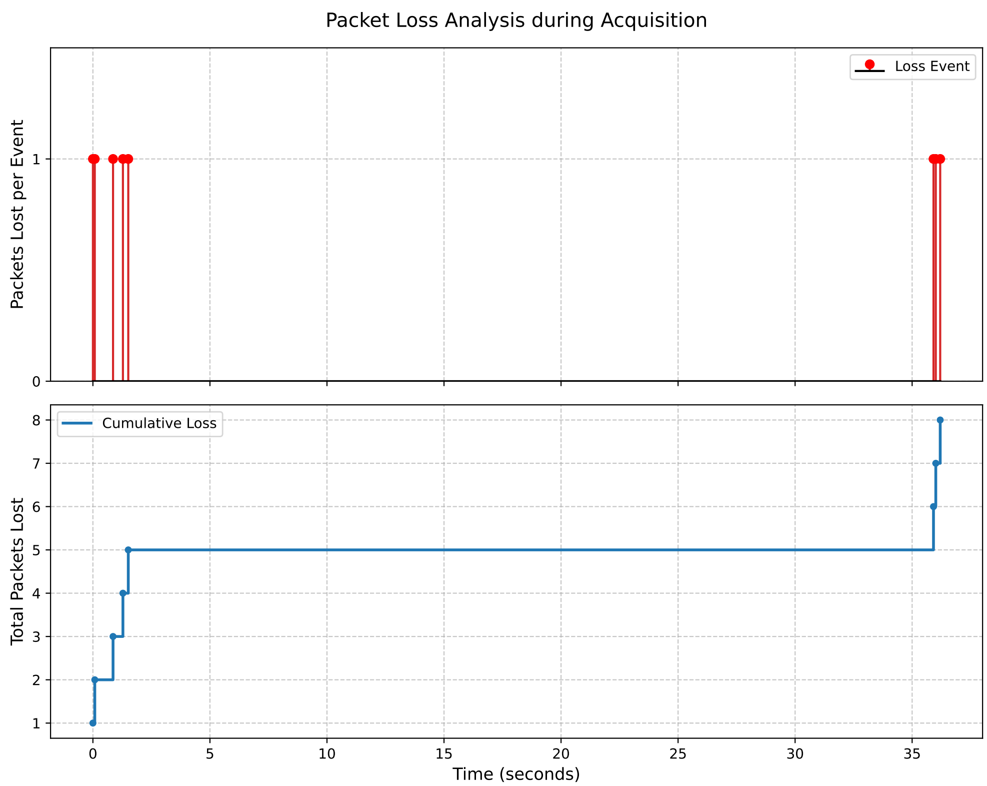

Figure 4-6: Packet loss rates observed during the multimodal transmission stress test.

5 Final remarks

5.1 Conclusion and discussion

The design and testing of a rapidly deployable EEG cap, integrated with the ADS1299's lead-off detection circuitry for real-time impedance quantification, proved effective in minimizing patient setup friction—a critical requirement when working with pediatric ADHD populations prone to restlessness. The impedance visualization module allows operators to quickly verify and adjust electrode contact prior to each session, and the measured impedances consistently remained within acceptable thresholds. This rapid deployment capability secures the pristine analog baseline upon which all subsequent acquisition and synchronization stages depend.

The MONEEE system's heterogeneous computing architecture—physically decoupling the real-time acquisition domain on the TM4C1294 microcontroller from the high-level compute domain on the Raspberry Pi CM4—proved essential for preserving microvolt-level signal integrity. By operating the acquisition core in a *bare-metal* environment and powering the ADS1299 analog front-end through isolated LDO regulators, the design effectively prevents high-frequency digital switching noise from coupling into the amplifier input stages. The instrumental noise characterization test, conducted with internally shorted inputs, confirmed that the system's intrinsic noise floor complies with the sub-microvolt specifications required for reliable extraction of low-amplitude Event-Related Potentials such as the N200 and P300. Complementarily, the computational resource consumption analysis demonstrated that both the TM4C1294 and the CM4—optimized with the *PREEMPT_RT* kernel patch and CPU core isolation—sustain continuous multi-channel acquisition without buffer overflows, thermal throttling, or RAM saturation, thereby guaranteeing deterministic data throughput throughout extended clinical sessions.

The central methodological contribution of this work—the hardware event injection strategy—eliminates the non-deterministic latency inherent to software-based time-stamping. By capturing USB event markers through a high-priority interrupt on the TM4C1294 and concatenating them directly into the EEG data frame within the same sampling cycle, the system transforms the synchronization problem into a deterministic data-parsing task. The 3-byte binary synchronization header—comprising an event flag, event type, and start-of-frame delimiter—ensures that the relative phase relationship between stimuli and physiological samples is preserved regardless of downstream operating system scheduling. The validation tests confirmed minimal transmission jitter across the SPI and serial interfaces, strictly bounded end-to-end latency from analog input to timestamped software availability, and negligible packet loss during prolonged Wi-Fi streaming under network congestion. These results collectively demonstrate that the `MoneLib` library—bridging the Unity-based serious game with the embedded hardware via a lightweight hexadecimal protocol over isolated USB—enables millisecond-level alignment between user interactions and physiological responses, providing a robust framework for cognitive assessments with high ecological validity.

This research demonstrates that the simultaneous optimization of signal fidelity and temporal determinism in embedded EEG architectures is not merely an engineering convenience but a clinical necessity. The coherent signal averaging technique upon which ERP-based ADHD assessments depend requires both a high signal-to-noise ratio and strict temporal stability; a failure in either domain independently invalidates the resulting biomarkers. The MONEEE architecture addresses this interdependence through a layered strategy—securing the analog baseline at the physical interface, preserving signal integrity through galvanic isolation and dedicated power management, and locking event timing at the lowest possible hardware layer before exposure to non-deterministic software environments. The successful integration of this architecture within the ACEMATE project framework confirms that clinically valid, portable neurocognitive assessment tools can be realized for pediatric populations without sacrificing the precision traditionally reserved for laboratory-grade systems.

5.2 Future work

While the MONEEE system has demonstrated its capacity to address the defined signal integrity and synchronization challenges, several promising research directions remain to expand its clinical applicability and technical capabilities:

- **Physiological alpha-blocking validation.** The spectral analysis in the idle state (alpha attenuation test) was not completed within the scope of this thesis. Executing this foundational physiological baseline test—recording continuous EEG during alternating eyes-closed and eyes-open conditions and verifying the characteristic suppression of alpha-band activity (8–13 Hz)—is an immediate priority. This validation would provide definitive end-to-end proof that the synchronized event markers are anchored to genuine cortical rhythms rather than structured noise.

- **Pilot ERP recording with serious game stimuli.** A natural subsequent step is to conduct a proof-of-concept recording of P300 and N200 event-related potentials elicited by the serious game on healthy subjects and, subsequently, on pediatric ADHD populations. This experiment would validate the full clinical pipeline—from stimulus presentation through hardware-synchronized acquisition to coherent signal averaging—and confirm the system's diagnostic utility within the ACEMATE framework.

- **On-device real-time signal processing.** The current architecture transmits raw digitized data to the CM4 for storage and forwarding. Integrating lightweight digital signal processing algorithms—such as adaptive notch filtering, real-time baseline drift correction, or compressive feature extraction—directly on the TM4C1294's Floating-Point Unit would reduce the data volume transmitted to the compute node and enable on-device signal quality metrics, further enhancing the system's autonomy for field deployments.

- **Integration of lightweight deep learning inference at the edge.** Building upon the edge-computing paradigm established in this thesis, future work could deploy quantized 1D convolutional neural networks or denoising autoencoders on the CM4 for real-time artifact rejection of ocular and muscular contamination. This would eliminate the need for post-hoc offline artifact removal, enabling fully closed-loop neurofeedback within the serious game environment.

- **Transition to active dry electrode technology.** While the current cap design utilizes wet electrodes for maximum signal fidelity, the adoption of active dry sensors with on-site impedance buffering would dramatically reduce patient preparation time and improve comfort for prolonged pediatric sessions. Characterizing the impact of this transition on the system's noise floor and ERP detection sensitivity constitutes a critical hardware evolution pathway.

- **Wireless event synchronization and expanded multimodal integration.** The current USB-C-based event interface requires a physical cable between the stimulation tablet and the acquisition system. Migrating to a wireless synchronization protocol—validated against the hardware injection baseline established in this thesis—would enhance clinical ergonomics. Additionally, integrating complementary physiological modalities such as galvanic skin response or heart rate variability into the MONEEE data frame would enrich the neurocognitive profile available for ADHD assessment.

- **Longitudinal clinical validation and normative database construction.** Deploying the MONEEE system across multiple clinical sites within the ACEMATE network for extended longitudinal studies would enable the construction of normative ERP databases for the Colombian pediatric population. Such databases are essential for establishing age-stratified diagnostic thresholds and for evaluating the long-term therapeutic efficacy of serious-game-based neurofeedback interventions in ADHD.

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