



# Low-Latency EEG Marker Integration in Serious Games for Neurocognitive Assessment

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# **Declaración**

Me permito afirmar que he realizado esta tesis de manera autónoma y con la única ayuda de los medios permitidos. Todos los pasajes que se han tomado de manera textual o figurativa de textos publicados y no publicados, los he reconocido en el presente trabajo. Ninguna parte del presente trabajo se ha empleado en ningún otro tipo de tesis.

Manizales, 2025

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Julian Andres Salazar Parias

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2025

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# 1 Preliminaries

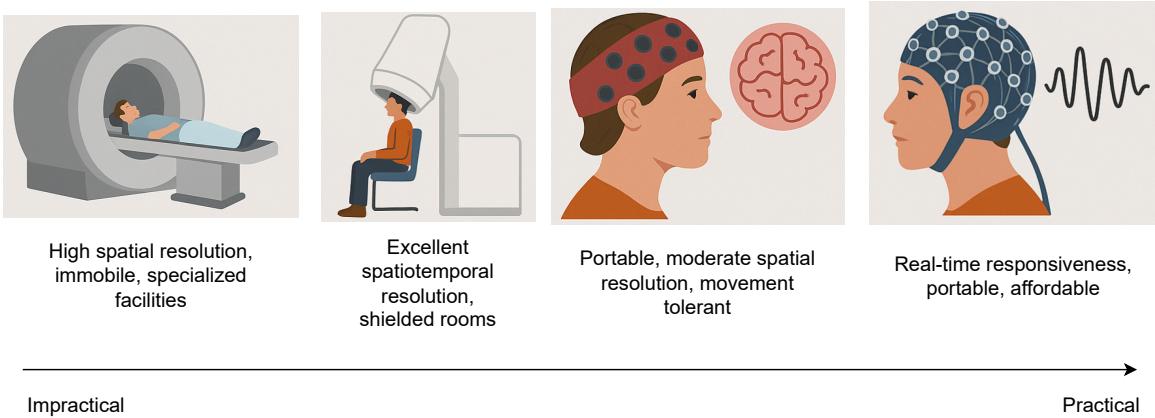
## 1.1 Motivation

Brain–Computer Interfaces (BCIs) have emerged as a powerful class of technologies that enable direct communication between the brain and external devices. These systems are increasingly being applied in neurorehabilitation, education, and clinical diagnosis due to their ability to monitor and interpret neural activity in real time. BCIs have the potential to revolutionize the way cognitive states are assessed and modulated by offering closed-loop interaction mechanisms that adapt to the user’s brain dynamics [Lim et al., 2023, Lin and Chang, 2025]. Central to this capability is the choice of neuroimaging modality, which must meet strict criteria in temporal resolution, portability, and cost-effectiveness—especially in applications involving children or naturalistic settings.

Several neuroimaging techniques have been explored for use in Brain–Computer Interface (BCI) systems, each with distinct advantages and limitations. Functional Magnetic Resonance Imaging (fMRI) offers high spatial resolution and whole-brain coverage, but its cost, immobility, and dependence on specialized facilities make it impractical for real-time interaction or integration with everyday environments [Yang and Wang, 2025]. Magnetoencephalography (MEG) provides excellent spatiotemporal resolution but is similarly constrained by high operational costs and the need for magnetically shielded rooms [Peksa and Mamchur, 2023]. Functional Near-Infrared Spectroscopy (fNIRS), a more portable option, measures cortical hemodynamic responses with moderate spatial resolution and tolerance to movement [Doherty et al., 2023]. However, its low temporal resolution limits its ability to capture fast-changing neural dynamics, such as those required for attentional monitoring or neurofeedback.

Electroencephalography (EEG), by contrast, emerges as the most suitable modality for BCI applications that demand real-time responsiveness, portability, and affordability. EEG records the brain’s electrical activity through non-invasive scalp electrodes, offering millisecond-level temporal resolution ideal for tracking rapid cognitive events like attention shifts or inhibitory control. While EEG’s spatial resolution is lower compared to fMRI or MEG, advances in signal processing—such as QEEG, functional connectivity analysis, and source localization—have greatly enhanced its ability to extract meaningful neurophysiological markers [Caiado and

Ukolov, 2025, Yadav and Maini, 2023, Värbu et al., 2022]. Moreover, EEG's lightweight hardware, low infrastructure requirements, and compatibility with embedded systems make it an ideal foundation for interactive, portable, and scalable BCI solutions.



**Figure 1-1:** Comparison of neuroimaging modalities by spatial resolution, temporal resolution, and cost. EEG stands out for its affordability, portability, and millisecond-level responsiveness.

One of the most compelling clinical applications of EEG-based BCIs is in the assessment and intervention of neurodevelopmental disorders such as Attention Deficit Hyperactivity Disorder (ADHD). ADHD affects approximately 10 % of children in Colombia [Salari et al., 2023, Pineda et al., 2003] and is characterized by persistent symptoms of inattention, hyperactivity, and impulsivity that interfere with academic performance, social relationships, and emotional regulation. Conventional diagnostic practices rely heavily on behavioral questionnaires and clinical observation, which, while informative, are inherently subjective and susceptible to bias [Raiker et al., 2017]. In this context, EEG offers a valuable alternative by enabling the objective measurement of neural correlates linked to attention and impulse control. Well-established EEG biomarkers such as elevated theta/beta ratios and altered event-related potentials (e.g., P300) have been extensively validated in the ADHD literature, making EEG a scientifically robust and clinically relevant tool for real-time cognitive monitoring and neurofeedback interventions.

Serious games are digital environments designed not solely for entertainment, but to fulfill educational, therapeutic, or cognitive objectives. In the context of neurodevelopmental disorders such as ADHD, they have become increasingly relevant as tools for both cognitive assessment and intervention [Patiño et al., 2025]. Their engaging and adaptive nature allows them to target specific executive functions—like attention, inhibition, and working memory—while maintaining high user motivation, particularly among children [Rodríguez Timaná et al., 2024]. These features make serious games particularly compatible with EEG-based BCIs for interactive cognitive modulation.

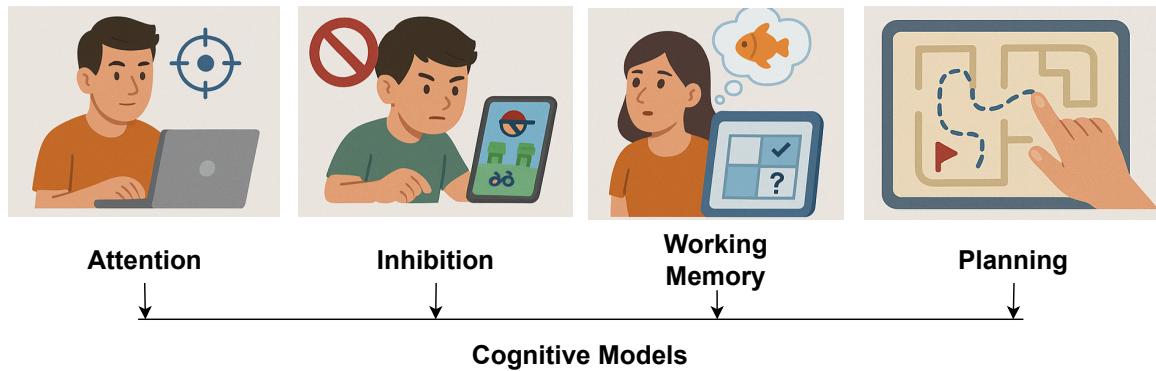
Serious games designed for ADHD not only provide engaging environments for cognitive stimulation, but also serve as structured frameworks for assessing and training specific

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executive functions. Two principal paradigms guide the design of these games. The first is the task-based paradigm, which integrates classical neuropsychological tasks—such as the Go/No-Go, n-back, or Stroop test—into interactive game mechanics. This allows for the precise measurement of behavioral responses tied to well-established cognitive models [Fang et al., 2025]. The second is the neurofeedback paradigm, in which the game dynamically responds to real-time EEG signals, offering auditory or visual feedback based on the user’s brain state. This paradigm supports operant conditioning mechanisms, encouraging users to self-regulate neural activity linked to attentional control and inhibition [Firouzabadi et al., 2022].

These paradigms are often aligned with four core cognitive models critical to ADHD pathology: attention, working memory, inhibition, and planning. Games targeting the attentional model aim to improve sustained and selective attention, often requiring players to maintain focus amid distractions or shifting stimuli [Chen et al., 2024]. Working memory is typically trained through tasks that require the temporary storage and manipulation of information, such as remembering sequences or updating mental representations. The inhibition model involves suppressing prepotent responses or resisting distractions—commonly implemented through fast-paced decision-making challenges or impulse control mechanics [Takahashi et al., 2024, Breitling-Ziegler et al., 2020]. Finally, the planning model emphasizes goal-directed behavior, encouraging users to sequence actions, solve multi-step problems, or anticipate future outcomes [Lorini et al., 2022]. By aligning game mechanics with these cognitive models, serious games become powerful tools not only for engagement but for targeted neurocognitive intervention, particularly when combined with EEG-based BCIs that provide objective feedback on brain performance in real time.



**Figure 1-2:** Core cognitive models targeted by serious games in ADHD interventions: attention, working memory, inhibition, and planning. Each model maps to a specific set of game dynamics and EEG markers.

Serious games integrated with BCI technology have demonstrated therapeutic benefits by reinforcing executive function, improving behavioral outcomes, and reducing symptom severity through active attention training and neurofeedback mechanisms [Doulou et al., 2025]. Active BCIs, in which users intentionally modulate their focus to influence the outcome of the game, have been shown to strengthen cognitive control and promote long-term neuroplastic

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changes relevant to ADHD pathology [Cervantes et al., 2023]. These platforms also enable adaptive feedback, allowing interventions to dynamically adjust to each child’s neurocognitive profile.

However, the effectiveness of such systems depends on precise temporal synchronization between game-generated stimuli and EEG signals. Detecting event-related potentials (such as the P300 wave) or dynamic oscillations in the theta and beta frequency bands during attentional tasks requires sub-millisecond timing accuracy [Wikström et al., 2022, Sandstrak, 2024]. Without rigorous synchronization—typically achieved via TTL triggers or low-latency USB/Wi-Fi communication—EEG signal interpretation is susceptible to noise, jitter, and event misclassification [Iwama et al., 2023]. This challenge is particularly critical in real-time therapeutic environments where accurate feedback is essential.

Recent developments in portable EEG hardware have expanded the applicability of BCIs for ADHD beyond clinical settings, enabling real-time monitoring and feedback in homes, classrooms, and therapeutic environments. Low-cost, wireless EEG headsets—equipped with dry electrodes and embedded microcontrollers—have been successfully integrated into neurofeedback systems and serious games designed for children [Xu and Zhong, 2018]. These platforms allow for real-time signal acquisition and onboard processing, supporting closed-loop interventions without reliance on external computers. Thanks to ARM-based processors and system-on-chip (SoC) designs, it is now possible to run lightweight machine learning models directly on the device for real-time EEG classification [Wang et al., 2020]. Moreover, custom head-mounted EEG systems have shown reliable tracking of the theta/beta ratio, a key biomarker for ADHD, during interactive tasks [Larocco et al., 2020].

Altogether, these technological advances offer a promising foundation for rethinking ADHD diagnosis and intervention—especially in child populations. Nevertheless, critical technical challenges remain, particularly the synchronization of cognitive stimuli with neurophysiological responses in embedded systems. This challenge motivates the present research, which aims to design and implement a portable EEG acquisition and analysis system with precise synchronization to game events, enabling objective, real-time support for cognitive stimulation and diagnostic processes in children with ADHD.

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## 1. Preliminaries

### 1.2 Problem statement

The design and implementation of serious games synchronized with neurophysiological signals such as electroencephalography (EEG) presents a critical challenge, especially when targeting cognitive stimulation and diagnostic support in pediatric populations with Attention Deficit Hyperactivity Disorder (ADHD) [Raza et al., 2025]. The scientific validity of such applications is fundamentally dependent on the precise temporal synchronization of at least two disparate data streams: the high-temporal-resolution physiological data from the EEG system and the context-dependent event data generated by the serious game [Romani et al., 2025]. A core technical obstacle lies in achieving this precise synchronization, a requirement that is essential for both the accuracy of event-related potential (ERP) measurements and the effectiveness of real-time interventions [Fanourakis and Chanel, 2024]. This thesis addresses two primary facets of this challenge: the temporal inaccuracies introduced by system-level operations and the physical limitations of the hardware itself.

#### 1.2.1 Unpredictable Latency and Jitter Between Game Events and EEG Recordings

The primary technical issue in synchronizing EEG data with serious game events is the presence of unpredictable latency and jitter. Latency is the delay between an event's physical occurrence (e.g., a stimulus appearing on screen) and its corresponding timestamp being recorded in the data stream. A more pernicious issue is jitter, defined as the statistical variability in that latency over time. While a constant latency might be correctable in post-processing, jitter introduces random, unpredictable timing errors that cannot be easily removed after data acquisition [Iwama et al., 2023].

This issue is caused by several interrelated factors: buffering delays in data pipelines, the non-deterministic scheduling of non-real-time operating systems, variability in communication protocols (such as USB, Bluetooth, or the Lab Streaming Layer), and asynchronous execution within game engines like Unity. These conditions lead to a lack of temporal precision, where the timestamp of an in-game event does not accurately align with the corresponding entry in the EEG data stream [Cardona-Álvarez et al., 2023].

This misalignment significantly compromises the quality of neurophysiological analysis. ERP components such as the P300 and N200, which are commonly used to evaluate attentional processes in ADHD, depend on millisecond-level synchronization between stimulus onset and neural response. When event markers are not precisely aligned due to jitter, the resulting ERP waveform becomes temporally "smeared," causing a reduction in both amplitude and interpretability, which degrades the signal-to-noise ratio and threatens diagnostic reliability [Klee et al., 2024]. This is particularly critical in pediatric populations where subtle

attentional deficits are being assessed.

Furthermore, in real-time systems like neurofeedback applications, where immediate feedback is essential for operant conditioning, even minor delays can disrupt the feedback loop. If the user receives auditory or visual feedback that no longer corresponds precisely to their brain state, the therapeutic effectiveness is reduced, potentially leading to user disengagement or ineffective training outcomes. The temporal precision required is demanding; some brain-computer interface (BCI) paradigms require accuracy within  $\pm 2$  milliseconds, yet jitter introduced by a game's graphical rendering at 50 frames per second can be as high as 20 milliseconds [Wang et al., 2025].

Recent studies have quantified these challenges. For example, [Larsen et al., 2024] found that even in systems optimized with Unity and LSL, event marker delays averaged 36 milliseconds with a jitter of 5 to 6 milliseconds—well above the acceptable margin for many ERP analyses. Additionally, Brain Products [Brain Products GmbH, 2025] reports that embedded platforms lacking efficient buffering and timestamping can exhibit latencies up to 100 milliseconds, particularly under high computational load. These delays, caused by a lack of dedicated real-time scheduling and protocol optimization, result in a substantial loss of synchronization fidelity, ultimately undermining both research validity and clinical utility.

### 1.2.2 Resource and power constraints in embedded EEG platforms

The second major issue stems from the computational and energy limitations of embedded and wearable EEG systems. Designed to be mobile and unobtrusive, these systems often operate on limited battery power, constrained CPU cycles, and reduced memory [Kaongoen et al., 2023]. These constraints are exacerbated when the system must simultaneously support real-time data acquisition, multichannel EEG streaming, and high-frequency event marker registration. Conventional EEG setups that rely on centralized data processing can also lead to high energy consumption and increased data transmission latency [Zhang et al., 2025, Akhtar and Rozario, 2025]. These limitations make it difficult to implement low-latency communication and high-resolution timestamping. Wireless data transmission, in particular, is very power-intensive [Kumar and Sujatha, 2022]. Protocols such as Bluetooth and Wi-Fi—commonly used in portable EEG systems—can introduce packet retransmissions, buffering delays, and inconsistent delivery times that worsen synchronization accuracy [Lin et al., 2023].

The consequences are significant. System designers are forced to lower EEG sampling rates, simplify marker handling, or accept increased delays—all of which reduce the reliability of the collected data and the interactivity of the game [Keutayeva et al., 2025]. For example, a review of wearable EEG systems found that wireless devices consistently showed worse timing stability and synchronization performance compared to wired configurations, especially when embedded resources were under heavy computational load [Barbera et al., 2025].

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Brain Products [Brain Products GmbH, 2025] corroborates these findings, warning that system performance degrades as channel count and sampling rate increase—conditions commonly required in clinical-grade EEG systems. This creates a fundamental trade-off: increasing signal fidelity and temporal resolution compromises system portability, while optimizing for mobility sacrifices diagnostic precision.

Therefore, a critical gap exists in establishing a robust methodology to reliably synchronize multimodal data streams from EEG systems and dynamic serious games with quantifiable, millisecond-level precision, while also operating within the power and resource constraints of embedded platforms. This thesis addresses the problem of ensuring the temporal integrity of these data streams to enable scientifically valid analysis of neuro-cognitive processes during gameplay.

## 1.3 Research question

How can a low-latency and low-jitter data synchronization framework be developed and validated to ensure the temporal integrity of multimodal data from embedded EEG systems and dynamic serious game events, while respecting the inherent resource and power constraints of such platforms?

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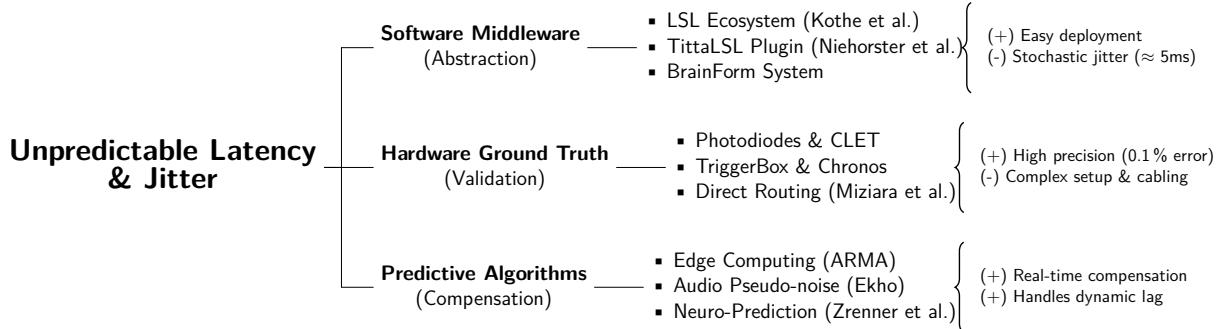
## 1. Preliminaries

### 1.4 State of art

#### Unpredictable Latency and Jitter Between Game Events and EEG Recordings

The integration of electroencephalography (EEG) into serious games necessitates a departure from the deterministic timing of traditional psychophysics toward architectures capable of managing the stochastic nature of modern game engines and wireless transmission. In the literature from 2022 to 2026, the resolution of unpredictable latency and jitter has coalesced around a progression of engineering philosophies, moving from software-defined abstraction to hardware-grounded validation, and finally to predictive algorithmic compensation. The dominant engineering philosophy in recent years has been the abstraction of hardware timing differences through Network-Layer Middleware, with the Lab Streaming Layer (LSL) cementing its status as the de facto standard for multimodal synchronization. In their seminal 2024 reference paper, Kothe et al. validated the LSL ecosystem's ability to achieve sub-millisecond accuracy by employing a distributed clock discovery protocol similar to NTP, which continuously estimates offsets and drifts between source and recording clocks [1], [2]. This software-centric approach has been pivotal for enabling "zero-configuration resilience in complex setups, allowing disparate devices to synchronize without shared hardware triggers [2]. For instance, Larsen et al. (2024) applied this framework to the notoriously difficult task of synchronizing EEG with VR-integrated eye-tracking, quantifying a stable hardware offset of 36 ms but noting a persistent stochastic jitter of 5.76 ms inherent to the buffering of consumer-grade peripherals [3], [4]. To mitigate the specific latencies introduced by game engines like Unity, Niehorster et al. (2024) developed "TittaLSL,"<sup>a</sup> plugin that decouples data transmission from the rendering loop; this allows for end-to-end latencies as low as 3.05 ms, preventing graphical frame drops from corrupting the time-series integrity of the biosignals [5]. This philosophy of software abstraction is further exemplified by the BrainForm system (2025), which leverages LSL to scale gamified BCI data collection to consumer hardware, accepting minor precision trade-offs in exchange for massive ecological validity and ease of deployment [6]. However, a counter-philosophy emphasizes Hardware-Ground Truth, arguing that software timestamps are insufficient for clinical-grade validity due to the "motion-to-photon" latency of display drivers. Ignatious et al. (2023) formalized this rigorous approach with the Computation of Latencies in Event-related potential Triggers"(CLET) method, which mandates the use of photodiodes to physically measure the arrival of photons [7]. Their comparative analysis revealed counter-intuitive findings: modern VR headsets often exhibit lower latencies (approx. 82 ms) than standard LED monitors (approx. 122 ms) due to aggressive low-persistence driver optimizations, yet the variance remains high enough to smear high-frequency ERP components [8], [8]. This necessity for hardware validation was statistically reinforced by Miziara et al. (2025), who compared three synchronization paradigms for TMS-EEG. They demonstrated that direct hardware routing (Paradigm 3) yields a relative timing error of 0.1%, drastically outperforming the 0.8% error of software-parallel methods, effectively proving that software middleware introduces a non-negligible noise floor [9], [9], [10]. Consequently, solutions like the TriggerBox and Chronos adapters remain critical for researchers requiring absolute temporal

precision, serving as a bridge between the digital game state and the analog amplifier [11], [12]. Furthermore, Roy et al. (2024) extended this hardware rigor to networked environments, utilizing custom synchronization protocols to align dry-electrode EEG with vehicle telemetry in multi-participant driving simulators, ensuring that collective neurophysiology is aligned despite network variance [13]. The third and most emergent philosophy treats latency not as a fixed error to be measured, but as a dynamic variable to be managed via Predictive and Compensatory Algorithms. This approach borrows heavily from edge computing and cloud gaming. Kim et al. (2025) introduced the ARMA system, which guarantees latency Service Level Objectives (SLOs) in mobile edge computing by dynamically adjusting the complexity of Deep Neural Networks (DNNs) based on real-time network conditions; effectively, the system trades classification complexity for speed when jitter spikes, maintaining the real-time feedback loop required for serious games [14], [14]. Similarly, Microsoft researchers proposed "Ekho" (2023), a system that embeds inaudible pseudo-noise sequences into game audio to measure and compensate for inter-stream delays in real-time, achieving sub-10ms synchronization across disparate devices [15]. On the neurophysiological side, Zrenner et al. (2025) advanced "Bayesian Temporal Prediction" (BTP), which predicts the phase of ongoing neural oscillations to deliver stimuli with "negative latency"—initiating the rendering pipeline milliseconds \*before\* the brain enters the desired state [16]. Additionally, Zhang et al. (2024) proposed offline stepwise latency correction algorithms that iteratively align single-trial EEG data post-hoc, effectively "de-jittering" the signal mathematically to recover sharp ERP features even from noisy recording environments [17]. Finally, Liu et al. (2025) developed the CLAAP model for cloud gaming, which uses time-series forecasting to predict latency spikes before they occur, allowing the game engine to preemptively adjust its state, a technique highly applicable to remote BCI assessments.



## Resource and Power Constraints in Embedded EEG Platforms

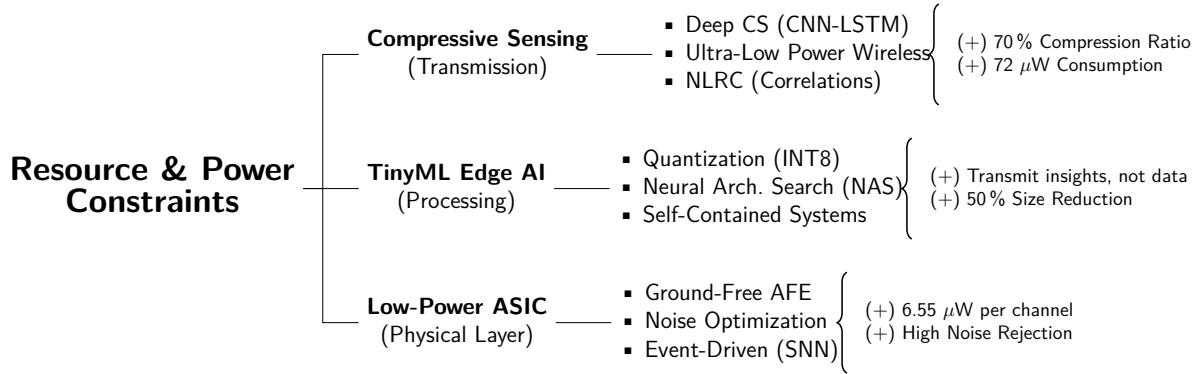
As the MONEEE system targets mobile usage, the engineering challenge shifts to maximizing signal fidelity within the stringent power envelopes of wearable devices. The literature from 2022–2026 addresses this through three synergistic philosophies: reducing data volume via Compressive Sensing, processing data at the edge via TinyML, and optimizing the physical layer via Low-Power ASIC Design. The philosophy of Compressive Sensing (CS) challenges the Nyquist-Shannon theorem, positing that EEG signals can be reconstructed from sparse

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samples to drastically reduce transmission energy—the primary consumer of battery life in wireless nodes [18]. The state-of-the-art has evolved from simple linear reconstruction to "Deep Compressed Sensing"(CS-EEG). Zhang et al. (2024) demonstrated that integrating CNN-LSTM networks into the reconstruction pipeline allows for compression ratios of up to 70 % while maintaining a Percentage Root-mean-square Difference (PRD) of less than 7% [19], [20], [21]. This approach offloads the heavy computational reconstruction to the server, keeping the wearable sensor simple. Yamada et al. (2025) implemented these principles in a wireless EEG transmission system that consumes a mere 72  $\mu\text{W}$ , orders of magnitude lower than standard Bluetooth protocols [22], [22]. Further refinement comes from Zhu et al. (2025), who introduced "Non-local Low-Rank and Cosparse Priors"(NLRC); this technique exploits the high inter-channel correlation of high-density EEG arrays to enhance reconstruction quality without increasing the sampling rate, effectively allowing for denser sensor grids on limited power budgets [23], [23]. Reviews by Damoah and Liang (2024) and Salami et al. (2025) further categorize these methods, highlighting that while lossless methods like ECoT ensure integrity, hybrid lossy methods are essential for the high-bandwidth demands of serious gaming [24], [25].Complementing transmission reduction is the TinyML philosophy: "transmit insights, not data."By processing bio-markers directly on the microcontroller (MCU), these systems eliminate the bandwidth cost of raw data streaming. Tsanika et al. (2025) and Lemoine et al. (2025) have pioneered the deployment of complex seizure detection algorithms on resource-constrained ARM Cortex-M and STM32 chips using quantization techniques [26], [27], [28]. By converting 32-bit floating-point weights to 8-bit integers (INT8), they achieved model size reductions of over 50 % (down to 23KB) with negligible loss in accuracy (maintaining >98 % sensitivity) [29]. To automate the design of these efficient networks, researchers at KAUST (2024) applied "Neural Architecture Search"(NAS) specifically for EEG, generating models that fit within kilobytes of SRAM while optimizing for inference latency [30], [30]. This edge-intelligence capability is realized in systems like CognitiveArm"(2025), a prosthetic control interface that runs deep learning motor imagery classification entirely on embedded hardware [31], [31], and STM32-based emotion recognition systems that adapt game mechanics in real-time based on the user's affective state [32]. Comprehensive surveys by the IEEE Internet of Things Journal (2025) confirm that TinyML is shifting the paradigm from cloud-dependent BCI to "self-contained"neuro-wearables [33], [34].Finally, the foundational Low-Power ASIC philosophy focuses on optimizing the analog front-end (AFE) to reduce the baseline power consumption of signal acquisition. Watcharapongvinit et al. (2023) presented a ground-free AFE design consuming only 6.55  $\mu\text{W}$  per channel while maintaining robust noise rejection, critical for ambulatory settings where motion artifacts are prevalent [35], [36]. Liu et al. (2025) pushed these limits further with a gain-configurable readout circuit achieving an input-referred noise floor of just 0.42  $\mu\text{Vpp}$ , ensuring that low-power operation does not compromise the detection of subtle neurocognitive components [37], [37]. Innovators like CSEM have also introduced cooperative sensor.<sup>a</sup>rchitectures, where active electrodes are connected via a single unshielded bus, reducing the weight and complexity of the headset cabling [38]. Furthermore, the shift toward .<sup>E</sup>vent-Driven"processing is gaining traction; Xie et al. (2023) and other groups have developed hybrid processors that utilize Spiking Neural Networks (SNNs) or Level-Crossing ADCs (LCADC) to process signals only when significant voltage changes occur, mimicking the brain's own energy-efficient sparsity , . Recent work by Zheng et al. (2024) on Ear-EEG AFES demonstrates that these low-power techniques

can be miniaturized into hearable form factors, opening new avenues for unobtrusive serious gaming interfaces [39], [39]. Nguyen et al. (2025) also demonstrated a low-power sonification algorithm on MCU, proving that complex real-time feedback is possible within a 12mW envelope [40].



## 1.5 Objectives

### 1.5.1 General Objective

To design and implement an EEG signal acquisition architecture optimized for applications in educational and clinical settings, focused on latency reduction and precise event synchronization, to improve the objective assessment of cognitive and emotional patterns in children with ADHD.

### 1.5.2 Specific Objectives

1. Analyze the technical limitations of current EEG acquisition systems, including transmission latencies and low channel density.
2. Develop low-latency algorithms and temporal synchronization strategies to ensure precise alignment between serious game stimuli and EEG responses.
3. Evaluate the proposed architecture in clinical and educational settings, verifying its effectiveness in the diagnosis and treatment of ADHD.

## 2 Theoretical Framework

The development of the MONEEE system is grounded in the convergence of neurophysiological principles, precision electronic engineering, and computer science. This section systematizes the critical concepts required for the device's implementation, addressing the stochastic nature of biological signals, the low-noise acquisition architecture, and the challenges inherent to temporal synchronization in heterogeneous digital systems.

### 2.1 Neurophysiology and Event-Related Potentials (ERPs)

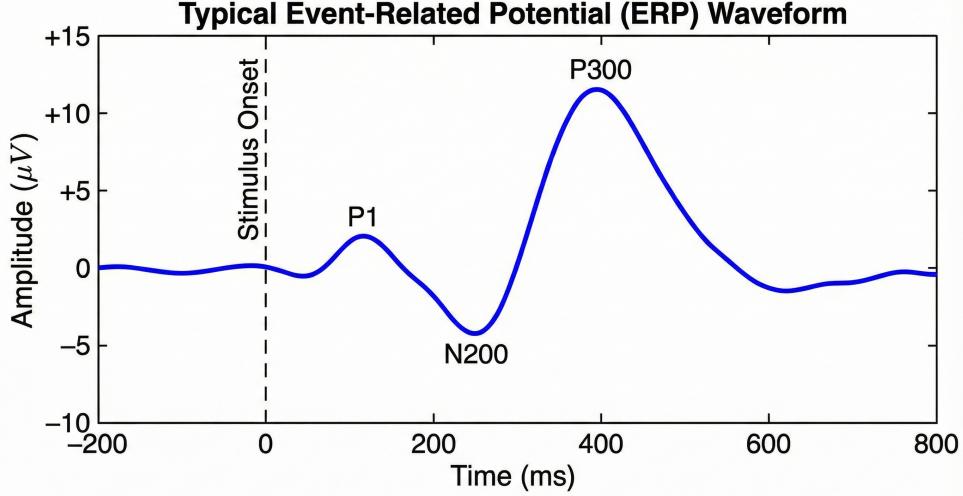
Electroencephalography (EEG) constitutes a non-invasive technique for recording cerebral bioelectric activity via transducers arranged on the scalp. While continuous EEG analysis allows for the monitoring of basal brain states—such as wakefulness, sleep, or convulsive pathologies—cognitive neuroscience research requires isolating specific neuronal responses associated with sensory, motor, or cognitive stimuli. These voltage fluctuations, known as Event-Related Potentials (ERPs), represent the synchronized activity of pyramidal neuronal populations in response to information processing.

Within the complex morphology of ERPs, two endogenous components are of particular interest for neurocognitive evaluation and the implementation of serious games in the context of this project. The first is the N200 (or N2) component, a negative deflection that reaches its maximum amplitude between 200 and 350 ms post-stimulus. This component is functionally linked to executive control, specifically in mismatch detection processes and the inhibition of motor responses. The second component, the P300 (or P3b), manifests as a prominent positive deflection with a latency of 300 to 600 ms. Its amplitude is modulated by the allocation of attentional resources and the updating of working memory, being particularly sensitive to stimulus improbability (the *oddball* paradigm). Due to these characteristics, the P300 is consolidated as a robust biomarker for quantifying cognitive load and attentional deficits.

The detection of these components presents a significant challenge in signal processing due to their low signal-to-noise ratio (SNR). ERPs possess typical amplitudes in the range of

## 2. Theoretical Framework

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**Figure 2-1:** Characteristic morphology of an Event-Related Potential (ERP), highlighting exogenous and endogenous components such as the N200 and P300.

$1\mu V$  to  $20\mu V$ , frequently remaining masked by background EEG activity, the magnitude of which oscillates between  $50\mu V$  and  $100\mu V$ . To extract the signal of interest, the technique of coherent signal averaging is employed. Assuming that background noise is a stochastic process with zero mean and is uncorrelated with the stimulus, by averaging  $N$  trials, the noise amplitude decreases in proportion to  $1/\sqrt{N}$ , while the ERP signal remains constant.

However, the validity of this technique depends strictly on temporal stability. Variability in the synchronization marker's latency, a phenomenon termed *jitter*, introduces systematic errors in the resulting average. Mathematically, if the trigger latency follows a normal distribution with standard deviation  $\sigma_t$ , the averaging process acts as a low-pass filter on the original waveform, attenuating high-frequency components and distorting peak amplitude. A jitter greater than 10 ms ( $\sigma_t > 10$  ms) is sufficient to degrade the morphology of the N200 component, compromising the diagnostic utility of the data. Consequently, the MONEEE system must guarantee strict real-time (*hard real-time*) synchronization to preserve the spectral and temporal integrity of the biomarkers.

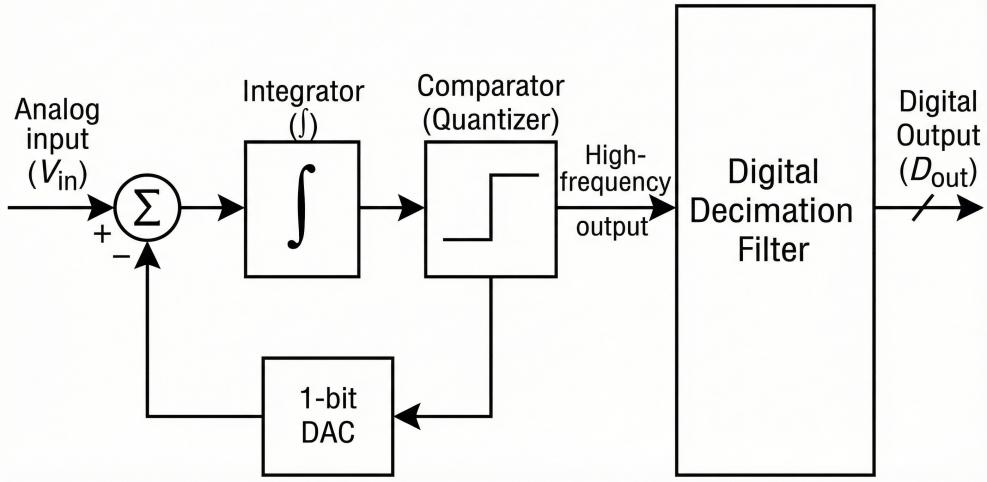
## 2.2 Hardware Architecture for Signal Acquisition

The fidelity in the digitization of biopotentials is determined by the topology of the Analog Front-End (AFE). The proposed system integrates the Texas Instruments ADS1299 integrated circuit, an analog-to-digital converter (ADC) designed specifically for biomedical instrumentation, which implements a Delta-Sigma ( $\Delta\Sigma$ ) modulation architecture.

Unlike the Successive Approximation Register (SAR) converters common in general-purpose microcontrollers, the  $\Delta\Sigma$  architecture offers superior advantages in terms of dynamic range

and noise rejection through two main mechanisms: oversampling and noise shaping. The device samples the input signal at a modulation frequency ( $f_{mod}$ ) significantly higher than the Nyquist rate, distributing quantization noise power over a wider spectrum. Subsequently, the modulator shifts this noise toward high frequencies, outside the biological band of interest (0–100 Hz), allowing a digital decimation filter to eliminate it effectively while reducing the data rate to the output frequency configured by the user.

Simplified Block Diagram of a Delta-Sigma ADC Architecture



**Figure 2-2:** Simplified functional scheme of the modulation and filtering stage in a Delta-Sigma architecture ADC.

A critical aspect for functional connectivity and EEG coherence analysis is sampling simultaneity. In traditional multiplexed systems, a single ADC core switches sequentially between channels, introducing a systematic phase delay ( $t_{skew}$ ) between electrodes. The ADS1299 mitigates this problem by incorporating independent  $\Delta\Sigma$  modulators for each of its 8 channels, guaranteeing a virtually null  $t_{skew}$  and preserving the real phase relationship between different cortical regions.

To manage data flow without sacrificing temporal determinism, the MONEEE system design adopts a heterogeneous computing architecture that decouples acquisition from high-level processing. This structure is composed of a Microcontroller Unit (MCU), such as the TM4C1294, and a Microprocessor Unit (MPU), based on embedded Linux. The MCU operates under real-time constraints (either on *bare-metal* or with a lightweight RTOS), reacting to ADC hardware interrupts (DRDY) on microsecond scales to capture and timestamp samples, preventing FIFO buffer overflows. Meanwhile, the MPU manages computationally intensive and non-deterministic tasks, such as the TCP/IP protocol stack and file system storage. This division of responsibilities isolates bio-signal acquisition from the variable latencies introduced by the Linux kernel scheduler, ensuring data temporal integrity.

## 2.3 Digital Synchronization Protocols

Precise synchronization between the physiological recording and events generated by the stimulation software (video game) constitutes the central technical challenge of this research. The selection of the synchronization method implies a trade-off between temporal precision, implementation complexity, and intrusion into the user experience. Table 2-1 summarizes the characteristics of the predominant approaches.

**Table 2-1:** Comparative analysis of synchronization methods for BCI systems.

Method	Mechanism	Precision	Implementation
Optical (Photodiode)	Physical detection of screen luminance changes by an external sensor.	High (< 1 ms)	High (Additional hardware required).
Network (LSL)	Synchronization via local network protocol and software jitter correction.	Medium (< 5 ms)	Low (Software only).
Hardware Trigger (TTL)	Direct electrical signal from Parallel/USB port to the ADC.	Very High (< 1 ms)	Medium (Requires specific interfaces).

There are contrasting approaches to addressing this problem. Optical synchronization, based on photodiodes attached to the monitor, is considered the “gold standard” for validation, as it detects the physical change of pixels, bypassing software, operating system, and GPU rendering latencies. However, its requirement for external hardware limits its viability in massive clinical deployments. As a scalable alternative, the *Lab Streaming Layer* (LSL) protocol offers a middleware solution that unifies disparate data streams by assigning timestamps referenced to a common clock and drift correction algorithms. While LSL simplifies integration, its final accuracy remains dependent on local network stability and the game engine’s ability to report the event time accurately.

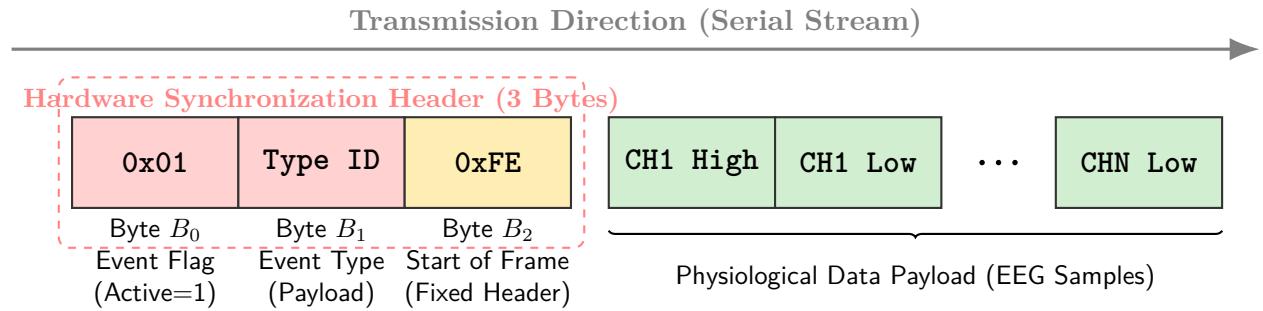
In the context of the MONEEE system’s physical interface, the USB bus introduces non-trivial latency considerations, especially for the transmission of marking commands (*soft-triggers*) from the PC to the amplifier. As a host-controlled bus utilizing polling, data transfer is discretized into frame intervals (1 ms in *Full Speed*) or microframes (125 $\mu$ s in *High Speed*). Additionally, the use of the CDC (*Communication Device Class*) to emulate serial ports implies that data traverses the operating system driver stack, where it may be stored in intermediate buffers to optimize global system performance. This behavior introduces variable and unpredictable latencies of several milliseconds between the logical generation of the event in the game and its physical arrival at the USB bus, which is incompatible with the precision requirements for high-frequency ERP component analysis.

To address the latency indeterminacy introduced by the USB stack and OS buffering, the

## 2. Theoretical Framework

MONEEE system implements a *hardware-embedded synchronization protocol* that couples synchronization logic directly to the biological sample at the firmware level. Unlike architectures that transmit event markers and EEG data through separate logical channels, MONEEE adopts a specific hexadecimal frame structure where the initial three bytes are strictly reserved for control data, thereby eliminating the need for post-hoc timestamp realignment.

In this encoding scheme, the first byte acts as a binary Event Flag ( $B_0$ ), explicitly indicating the presence of a synchronization trigger with a value of 1 or a resting state with 0, while the second byte ( $B_1$ ) designates the Event Type, carrying the specific code required to classify the nature of the stimulus (e.g., distinguishing between target and standard inputs). This metadata is immediately followed by the third byte ( $B_2$ ), which serves as a static Start-of-Frame delimiter to identify the beginning of the physiological data payload. By packaging the event markers and the EEG signal within this same atomic transmission unit, the system transforms the synchronization problem into a data parsing task, ensuring that the relative phase relationship is preserved regardless of the jitter introduced by the USB communication or the operating system scheduler.



**Figure 2-3:** Visual representation of the MONEEE serial data transmission frame. The initial three bytes ( $B_0, B_1, B_2$ ) form a dedicated hardware synchronization prefix attached to every physiological sample, ensuring that event timing is locked to the data stream before USB transmission.

## 3 Hardware Architecture (The MONEEE System)

The engineering design of the MONEEE system addresses the critical need to capture low-amplitude biopotentials with a high signal-to-noise ratio, while simultaneously guaranteeing low-latency synchronization with external events. To satisfy these requirements, a heterogeneous embedded computing architecture has been implemented, physically decoupling the real-time acquisition domain from the high-level computational domain. This separation allows each subsystem to be optimized for its specific function: signal integrity and determinism for acquisition, and performance and connectivity for processing.

### 3.1 System Topology and Data Flow

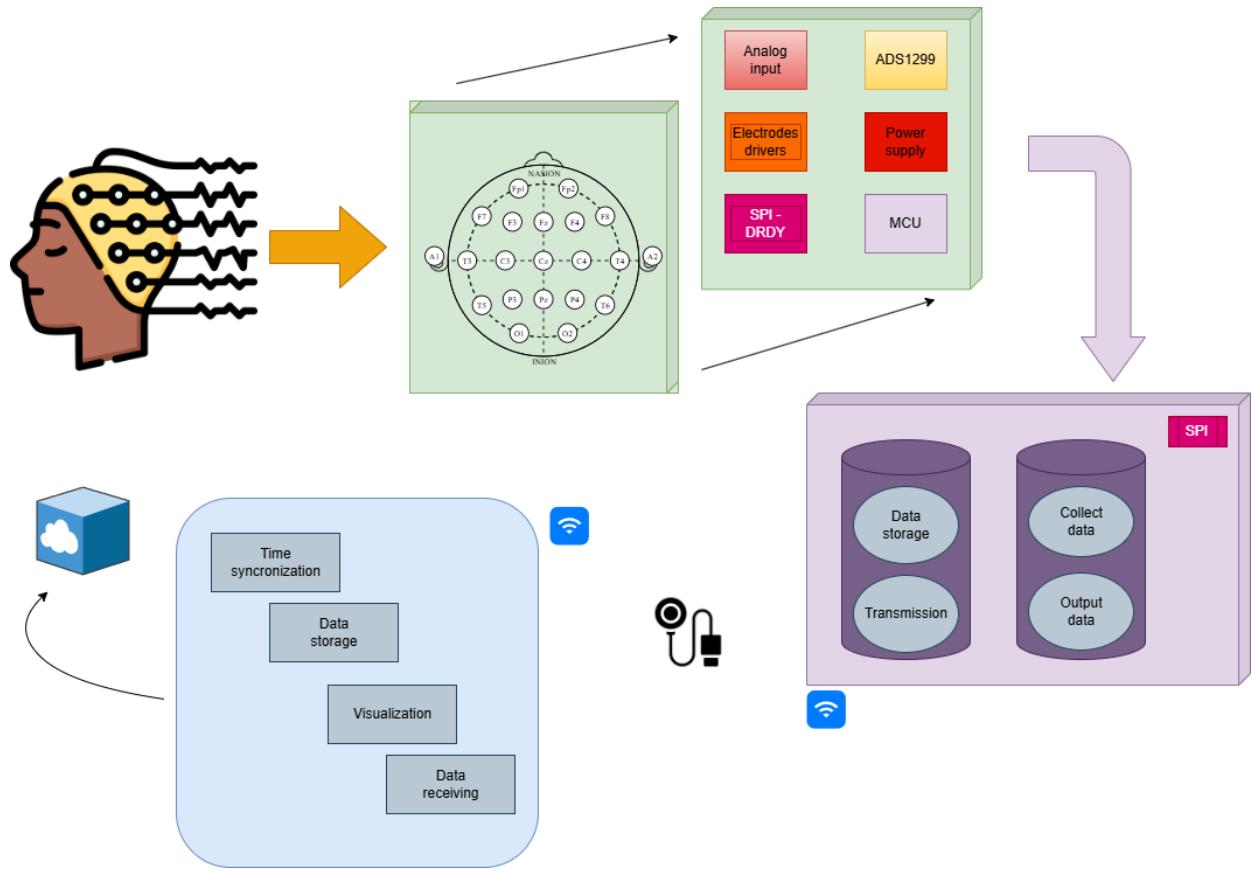
The device operates under an *edge-computing* paradigm, dedicating its resources exclusively to EEG signal management. The architecture establishes a strictly unidirectional data flow from the patient toward the processing unit, designed to minimize transport latency. The signal chain is formally modeled by the following transduction and transmission sequence:

$$\text{Electrodes} \xrightarrow{\text{Analog}} \text{ADS1299} \xrightarrow{\text{SPI}} \text{TM4C1294} \xrightarrow{\text{SPI}} \text{RPi CM4} \quad (3-1)$$

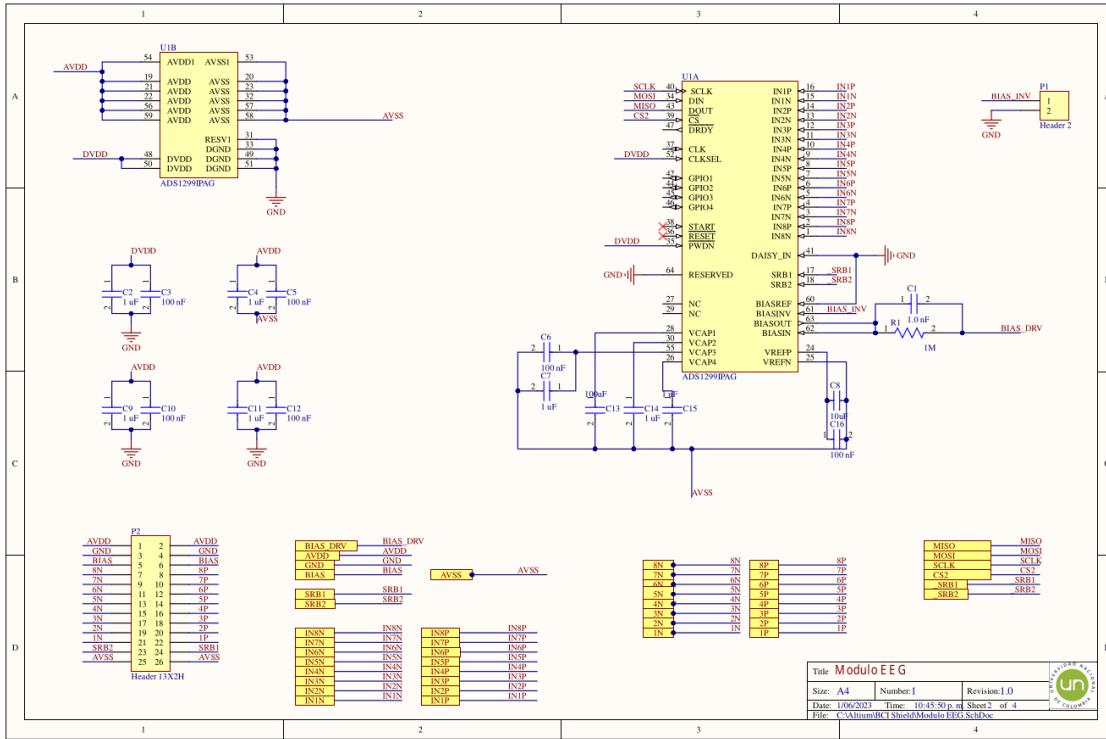
As illustrated in Figure 3-1, the hardware is structured into three differentiated functional zones: the Analog Front-End (AFE), the Real-Time Core, and the Compute Core. This segmentation is not merely logical but physical, employing isolation barriers to protect the integrity of physiological measurements.

For this project, we have established the MONEEE system as a robust electronic design aligned with acquisition systems in its segment. The designs presented in Figures 3-2, 3-3, 3-4, 3-5, 3-6, and 3-7 illustrate our proposal for an EEG signal acquisition board, conceived to significantly improve the capacity of real-time BCI systems, overcoming current challenges and contributing to the advancement of technology in this field.

### 3. Hardware Architecture (The MONEEE System)



**Figure 3-1:** Block diagram of the MONEEE architecture, evidencing the segregation between the deterministic acquisition (MCU) and high-level processing (MPU) domains.



**Figure 3-2:** Schematic design for the module responsible for acquiring EEG signals. 20

### 3. Hardware Architecture (The MONEEE System)

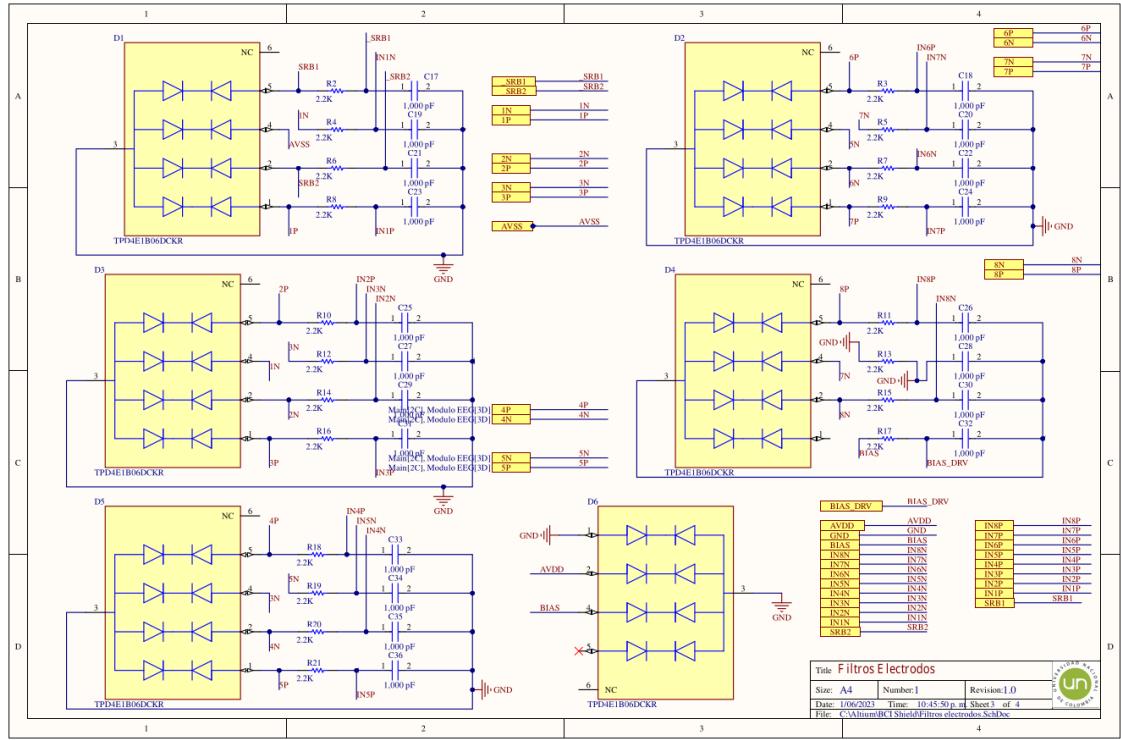


Figure 3-3: Schematic design of coupling filters.

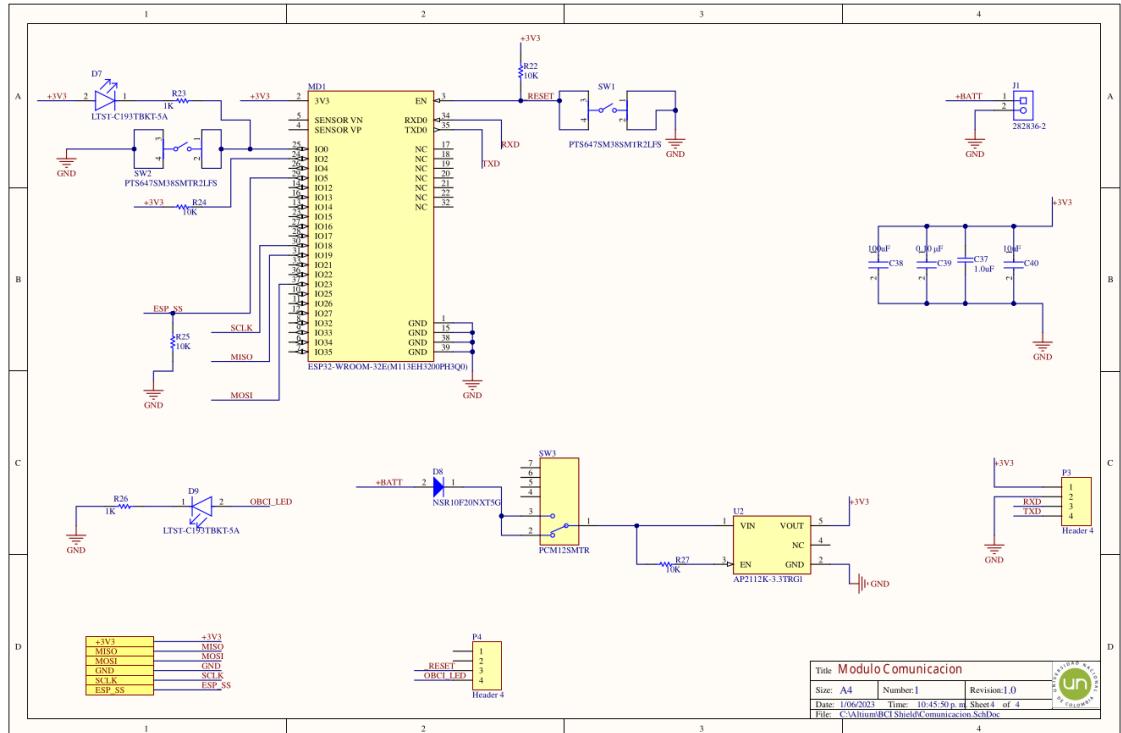


Figure 3-4: Schematic design of the module responsible for communicating the collected data to another device or to the cloud.

### 3. Hardware Architecture (The MONEEE System)

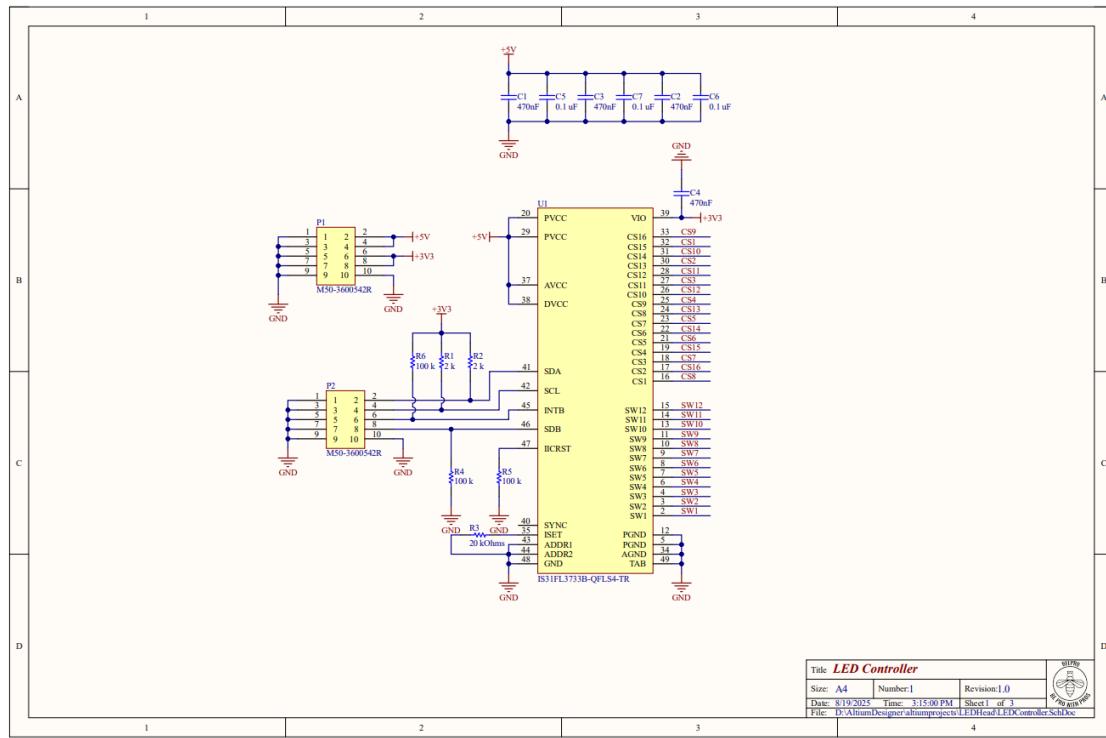


Figure 3-5: Module for impedance visualization of the electrodes.

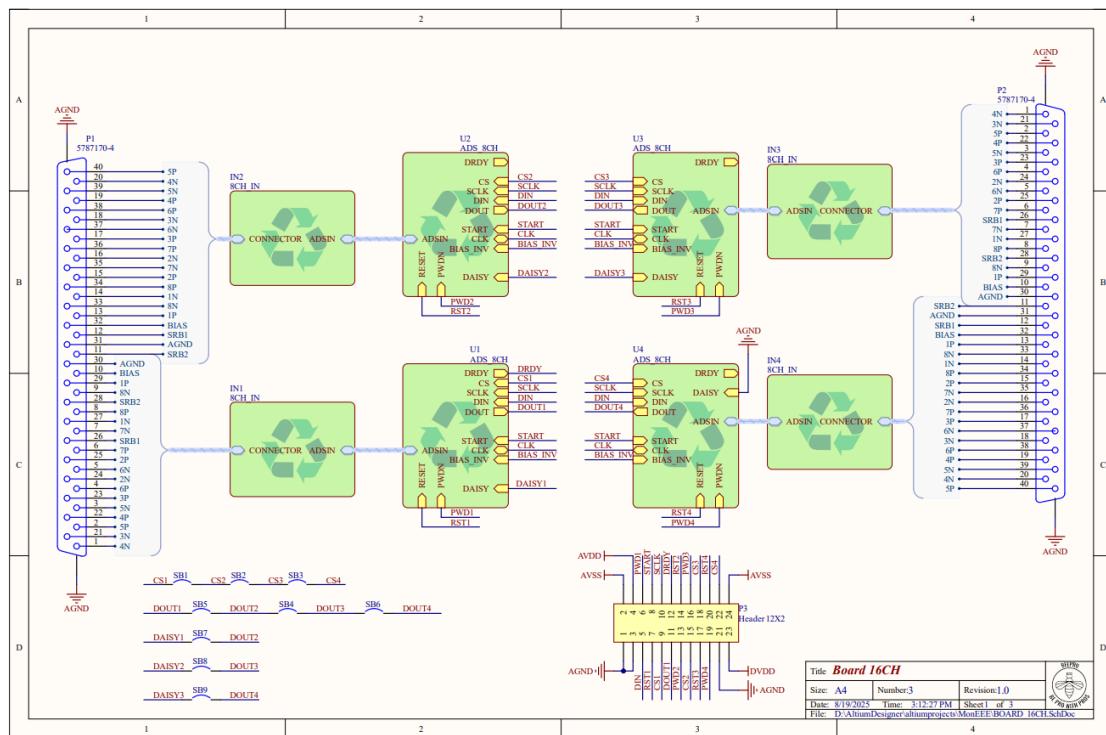


Figure 3-6: Connection between the different ADS1299 acquisition modules.

### 3. Hardware Architecture (The MONEEE System)

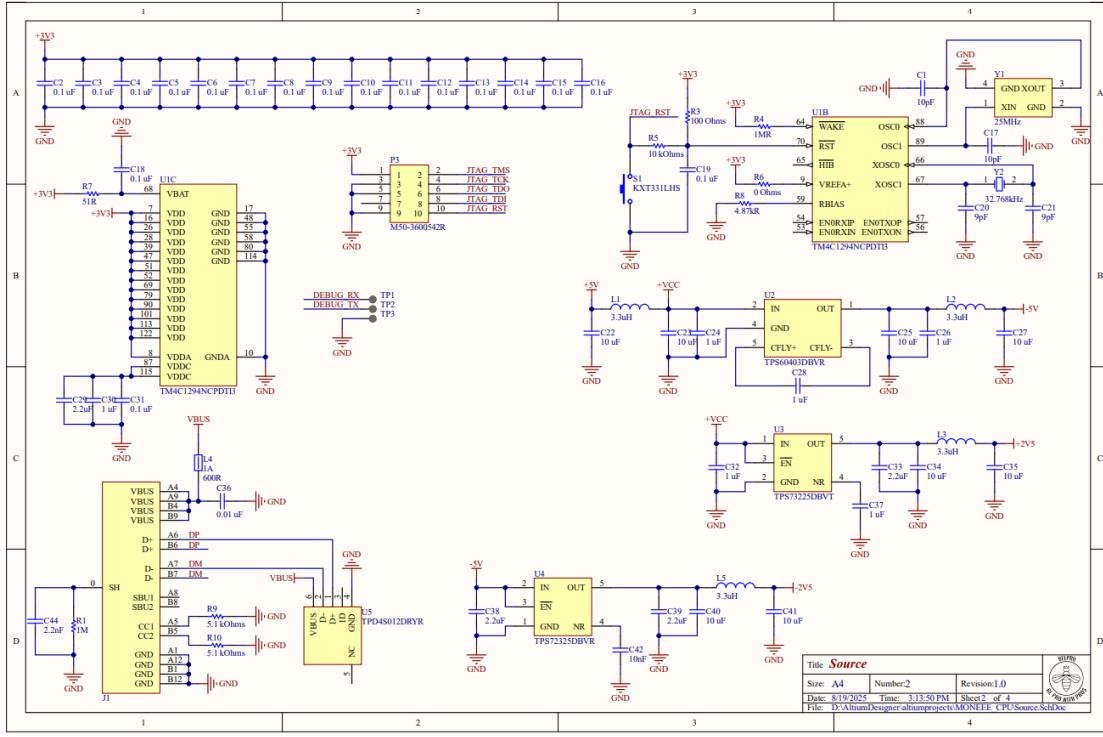


Figure 3-7: Motherboard for microcontroller and microprocessor.

## 3.2 Analog Front-End (AFE) and Biomedical Interface

The interface between the biological medium and the digital system is realized via the Texas Instruments ADS1299 integrated circuit. This component, a 24-bit analog-to-digital converter (ADC) with 8 simultaneous channels, has been specifically configured to optimize surface electroencephalography capture.

To maximize effective resolution on signals typically oscillating between 10 and  $100\mu V$ , the internal Programmable Gain Amplifier (PGA) is set to a gain of  $24V/V$ . Likewise, the sampling rate is fixed at 250 SPS or 500 SPS. This frequency provides a bandwidth that exceeds Nyquist requirements for the spectral components of interest (P300 and N200, generally located below 30 Hz), while allowing for the advantages of oversampling to reduce the noise floor. The input multiplexer is maintained in NORMAL mode for electrode acquisition, preserving the capability to internally switch toward test signals for self-calibration routines.

The suppression of electromagnetic interference, primarily 50/60 Hz mains noise, is managed through an active Driven Right Leg (DRL) topology. Unlike a passive ground reference, the ADS1299's *Bias Drive* circuit monitors the common-mode voltage present at the detection electrodes. This signal is inverted, amplified, and reinjected into the patient's body through

the reference electrode. This negative feedback loop actively cancels interference, raising the Common-Mode Rejection Ratio (CMRR) to levels exceeding 110 dB, which is indispensable for unshielded clinical environments.

Finally, signal integrity is ensured through rigorous power management. The AFE is powered by a dedicated Li-Po battery and regulated by a PMIC (Power Management Integrated Circuit). The analog power domain ( $AVDD$ ) is isolated from digital rails via Low-Dropout Regulators (LDOs) with high Power Supply Rejection Ratio (PSRR). This strategy prevents high-frequency switching noise, inherent to CPU operation in the compute module, from capacitively coupling to the amplifier input stages.

## 3.3 The Digital Core: Heterogeneous Processing

The digital architecture implements a shared responsibility model, distributing the computational load between a real-time microcontroller and an application microprocessor.

The Real-Time Unit, based on the Texas Instruments TM4C1294 (ARM Cortex-M4F), acts as the acquisition system master. Operating on *bare metal* or a lightweight real-time operating system, the TM4C guarantees deterministic behavior. Its primary function is to service the DRDY (Data Ready) hardware interrupt from the ADC immediately, ensuring lossless sample capture. Additionally, its Floating Point Unit (FPU) facilitates the application of in-situ digital pre-processing, such as notch filtering or scaling, without compromising interrupt service times. It is at this stage that the hardware *timestamp* is assigned, achieving microsecond precision.

Subsequently, data is transferred to the Compute Unit, constituted by a Raspberry Pi Compute Module 4 (CM4). This module runs a full operating system (Linux) and assumes high-level tasks: mass storage management, execution of the *Lab Streaming Layer* (LSL) gateway, and telemetric transmission via Wi-Fi. The CM4 processes the continuous stream coming from the microcontroller, packaging it into standardized formats for consumption by the serious game software.

Communication between both cores is established via a high-speed serial interface (UART > 921600 baud or SPI). To guarantee patient safety and signal integrity, this digital link includes galvanic isolation (utilizing digital isolators such as the ISO77xx series). This prevents the formation of ground loops between the floating acquisition stage (battery) and any peripheral connected to the electrical grid. The communication protocol employs lightweight binary frames encapsulating the 24-bit data along with their timestamps, protected by a Cyclic Redundancy Check (CRC) to verify transmission integrity.

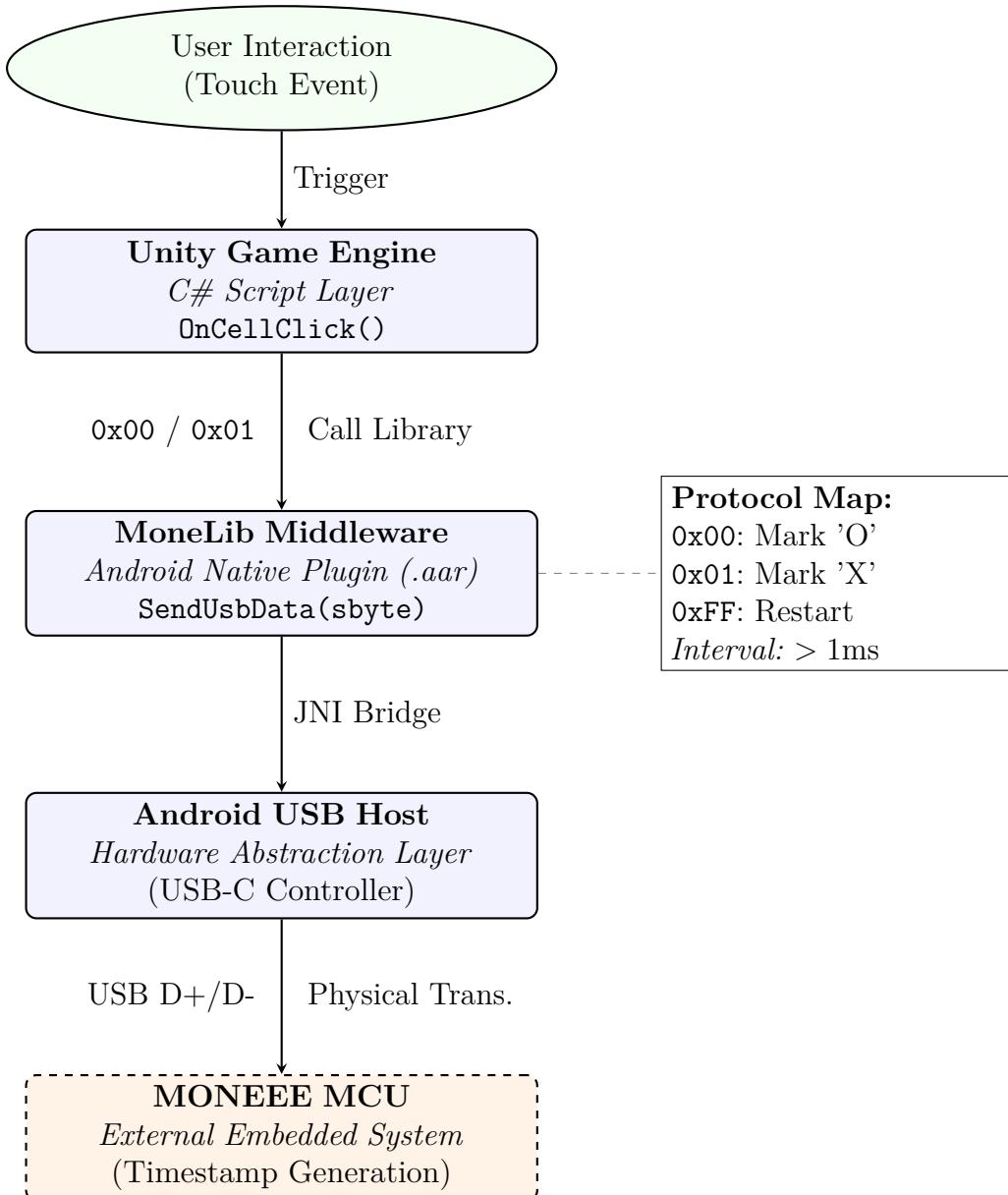
## 3.4 Event Synchronization Interface (USB-C)

Synchronization with the stimulation platform (tablet) is physically performed through a USB Type-C port. This port, managed by the system's USB controller, allows for the reception of ".event markers" generated by the game software at the precise instant of the stimulus. Given that the connection of commercial devices introduces significant electrical noise—a product of the tablet's internal DC-DC converters—the MONEEE system design incorporates total isolation of the USB bus. The data lines ( $D_+ / D_-$ ) traverse a specialized isolation integrated circuit (e.g., ADuM3160), effectively breaking galvanic continuity.

To manage the transmission of these synchronization markers from the software side, the system utilizes **MoneLib**, a specialized library designed to bridge the Unity-based game environment with the embedded hardware. This library operates as a native Android plugin (.aar), enabling the game engine to communicate directly with the USB Host peripheral of the tablet. The software architecture requires an Android device running version 12 (Snow Cone) or higher with USB-C Host support to properly initialize the communication driver.

The communication protocol is optimized for low latency, encoding game events—such as player interactions or system states—into lightweight hexadecimal values sent via USB. For instance, a player marking an "O" transmits the hexadecimal code 0x00, while marking an "X" sends 0x01, and a system restart triggers 0xFF. To ensure signal integrity and prevent saturation of the USB channel, the protocol enforces a minimum safety interval of 1 millisecond between consecutive event transmissions.

This integration allows the "Serious Game" to act as a precise stimulation trigger. When a user interacts with the game (e.g., touching a cell), the **MoneLibrary.SendUsbData** function is called immediately, dispatching the corresponding integer value to the microcontroller. This event is then captured by the embedded system's USB device peripheral and timestamped, ensuring that the cognitive task (the game) and the physiological recording (the EEG) remain temporally aligned for valid post-hoc analysis.



**Figure 3-8:** Data flow diagram of the Event Synchronization Interface. The high-level interaction within Unity is transduced into a hexadecimal marker by the MoneLib middleware and transmitted via the USB isolation barrier to the MONEEE acquisition core.

## 4 Firmware Architecture and Temporal Synchronization Strategy

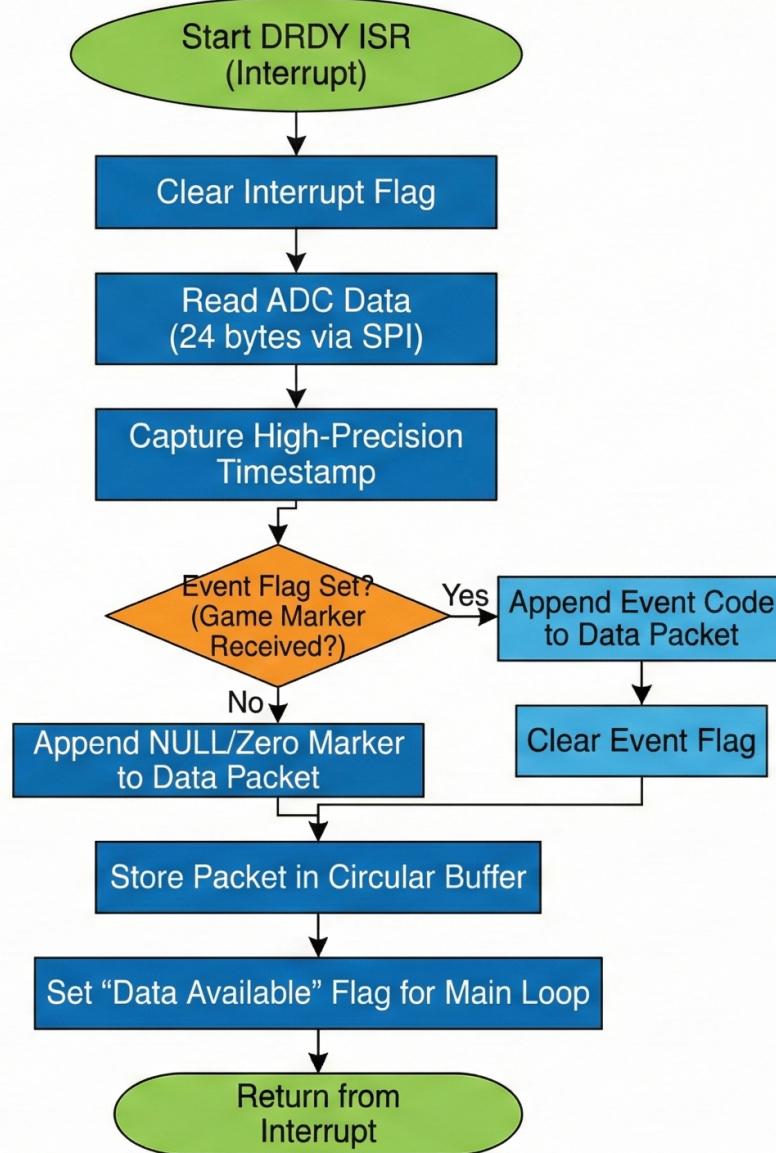
This section delves into the embedded computational logic governing the MONEEE hardware and its interface with the simulation environment. It describes the central methodological contribution of this development: a hardware-level event injection mechanism designed to mitigate the stochastic latency inherent to general-purpose operating systems, thereby achieving precise synchronization between physiological data and game stimuli at the microcontroller (MCU) level.

### 4.1 Deterministic Firmware Design on the TM4C1294

The firmware resident on the Texas Instruments TM4C1294 microcontroller has been structured under a *bare-metal* paradigm (dispensing with a complex operating system) to guarantee strictly deterministic behavior. The software architecture is event-driven, establishing an execution hierarchy where data acquisition holds maximum priority, subordinating any communication or maintenance tasks.

The synchronization engine depends on the precise management of the DRDY (Data Ready) interrupt signal generated by the ADS1299 converter. This signal activates the capture logic at the programmed sampling frequency (e.g., 250 Hz, corresponding to a 4 ms period).

The sequence of operations within the Interrupt Service Routine (ISR) is critical for maintaining the system's phase coherence. Upon detection of the falling edge of the DRDY signal, the microcontroller activates the *Chip Select* (CS) line of the SPI bus and initiates a Direct Memory Access (DMA) transfer. This mechanism allows for the automatic reading of 24 bytes of data (8 channels of 24 bits plus status bits) without CPU intervention, which is reserved for managing storage in a circular buffer and verifying event flags.



**Figure 4-1:** Flowchart of the Interrupt Service Routine (ISR) associated with the Data Ready signal (DRDY).

#### 4.1.1 Hardware Event Injection Strategy

To resolve the problem of temporal desynchronization, the system design dispenses with PC or Raspberry Pi clocks for event *timestamping*. Instead, a direct injection strategy into the data frame is implemented.

The operation of this mechanism is based on the immediate reception of commands. When the stimulation software (Game) generates a visual event, it transmits an 8-bit hexadecimal code (e.g., 0x0A) via the USB-C interface to the TM4C. The arrival of this byte triggers a

#### 4. Firmware Architecture and Temporal Synchronization Strategy

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high-priority interrupt in the MCU, which immediately stores the value in a volatile register named `Current_Event`. During the subsequent ADS1299 sampling cycle (which occurs within an interval of less than 4 ms), the ISR queries this register and concatenates the event code directly to the end of the EEG data packet in progress. In this way, the event marker and the physiological sample become physically linked within the same data structure before being transmitted to the Linux environment. This approach ensures that the relative *jitter* between the stimulus and the biological response is virtually null, bounded only by the temporal resolution of the sampling period.

## 4.2 Integration Protocol with the Simulation Environment

Interaction with the serious game, developed in the Unity engine, is managed via a custom communication library that acts as an abstraction layer over the tablet's serial API. This library exposes high-level methods, such as `SendMarker(int code)`, which are invoked by the game logic at the exact instant of stimulus rendering.

To guarantee the integrity of commands transmitted over the USB link and prevent the erroneous interpretation of electromagnetic noise as valid events, a robust binary protocol has been defined. The transmission structure consists of 3-byte frames, detailed in Table 4-1.

**Table 4-1:** Definition of the Serial Event Transmission Protocol.

Byte 0 (Header)	Byte 1 (Payload)	Byte 2 (Footer)
Start Marker 0xFF	Event Code 0x00 – 0xFE	Validation 0xAA

The protocol uses the byte 0xFF to signal the start of a transaction, followed by the event identifier (where specific codes denote states such as login, standard stimulus, or *oddball* stimulus). The frame concludes with the byte 0xAA, used for integrity validation; any sequence that does not respect this structure is immediately discarded by the TM4C firmware, ensuring high noise immunity.

## 4.3 Processing in the Compute Module (Raspberry Pi CM4)

The Raspberry Pi Compute Module 4 plays the role of an aggregation node and data gateway. While strict synchronization is the responsibility of the microcontroller, the CM4 must process the information flow with sufficient efficiency to prevent communication buffer overflows.

#### 4. Firmware Architecture and Temporal Synchronization Strategy

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To minimize operating system-induced latency, the Linux kernel on the CM4 has been optimized using the *PREEMPT\_RT* patch. This modification transforms Linux into a real-time operating system, allowing execution threads associated with hardware drivers (such as the UART receiver) to preempt standard user-space processes. Additionally, core isolation techniques are employed (*CPU shielding* via the `isolcpus` parameter), dedicating specific processor cores exclusively to data ingestion and freeing them from non-critical interruptions such as Wi-Fi network management or the graphical interface.

Finally, the application software on the CM4, developed in a hybrid Python/C++ environment, ingests the binary packets coming from the TM4C, extracts the injected event markers, and reformats the continuous stream to the Extensible Data Format (XDF) standard. This format, native to the *Lab Streaming Layer* (LSL) middleware, allows multimodal time series to be encapsulated, facilitating the coexistence of EEG samples and discrete event markers in parallel streams with a unified time base, thus optimizing analytical post-processing.

## 5 Final remarks

### 5.1 Conclusion and discussion

- This research confirms that the MONEEE system's partitioned design effectively solves the trade-off between signal fidelity and computational power. By physically decoupling the acquisition domain (TM4C1294) from the compute domain (Raspberry Pi CM4), the system preserves signal integrity against digital switching noise. The results demonstrate that handling biopotentials in a deterministic ("bare metal") environment is a critical requirement for achieving the signal-to-noise ratio necessary to reliably detect low-amplitude ERP components, such as the N200 and P300, without the interference typical of complex operating systems.
- The investigation establishes that the proposed hardware injection strategy offers a superior alternative to traditional software-based time-stamping. By physically coupling event markers with EEG samples at the microcontroller level, the system eliminates the variable latency and *jitter* inherent in software layers. This thesis demonstrates that such precise synchronization—bounded strictly by the sampling rate—is a fundamental prerequisite for preventing signal attenuation during the averaging process, thereby ensuring the diagnostic validity and temporal precision of the recorded data.
- The development and validation of the **MoneLib** library represents a significant contribution to the field of neuroinformatics, bridging the gap between custom hardware and the Unity engine. By functioning as a low-latency interface, **MoneLib** enables a precise millisecond-level alignment between user interactions and physiological responses. This innovation not only proves the technical viability of the system but provides a robust methodological framework for conducting cognitive assessments within "serious games," enabling research in scenarios that offer significantly higher ecological validity than static laboratory paradigms.

## 5.2 Future work

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## 5.3 Academic contributions

### 5.3.1 Journal papers

### 5.3.2 Patents

### 5.3.3 Software registered

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