12

Data Conversion Circuits – D/A and A/D Converters

Digital-to-analogue (D/A) and analogue-to-digital (A/D) converters constitute an essential link when digital devices interface with analogue devices, and vice versa. They are important building blocks of any digital system, including both communication and noncommunication systems, besides having other applications. A D/A converter is important not only because it is needed at the output of most digital systems, where it converts a digital signal into an analogue voltage or current so that it can be fed to a chart recorder, for instance, for measurement purposes, or a servo motor in a control application; it is also important because it forms an indispensable part of the majority of A/D converter types. An A/D converter, too, has numerous applications. When it comes to transmitting analogue data, it forms an essential interface with a digital communication system where the analogue signal to be transmitted is digitized at the sending end with an A/D converter. It is invariably used in all digital read-out test and measuring equipment. Whether it is a digital multimeter or a digital storage oscilloscope or even a pH meter, an A/D converter is an important and essential component of all of them. In this chapter, we will discuss the operational fundamentals, the major performance specifications, along with their significance, and different types and applications of digital-to-analogue and analogue-to-digital converters, in addition to application-relevant information of some of the popular devices. A large number of solved examples is also included to illustrate the concepts.

12.1 Digital-to-Analogue Converters

A D/A converter takes digital data at its input and converts them into analogue voltage or current that is proportional to the weighted sum of digital inputs. In the following paragraphs it is briefly explained

how different bits in the digital input data contribute a different quantum to the overall output analogue voltage or current, and also that the LSB has the least and the MSB the highest weight.

12.1.1 Simple Resistive Divider Network for D/A Conversion

Simple resistive networks can be used to convert a digital input into an equivalent analogue output. Figure 12.1 shows one such resistive network that can convert a three-bit digital input into an analogue output. This network, however, can be extended further to enable it to perform digital-to-analogue conversion of digital data with a larger number of bits. In the network of Fig. 12.1, if R_L is much larger than R, it can be proved with the help of simple network theorems that the output analogue voltage is given by

$$V_A = \frac{[V_1/R] + [V_2/(R/2)] + [V_3/(R/4)]}{[1/R] + [1/(R/2)] + [1/(R/4)]} \tag{12.1}$$

$$= \frac{[V_1/R] + [2V_2/R] + [4V_3/R]}{[1/R] + [2/R] + [4/R]} \tag{12.2}$$

$$= \frac{V_1 + 2V_2 + 4V_3}{7} \tag{12.3}$$

which can be further expressed as

$$V_A = \frac{V_1 \times 2^0 + V_2 \times 2^1 + V_3 \times 2^2}{2^3 - 1} \tag{12.4}$$

The generalized expression of Equation (12.4) can be extended further to an n-bit D/A converter to get the following expression:

$$V_A = \frac{V_1 \times 2^0 + V_2 \times 2^1 + V_3 \times 2^2 + \cdots + V_n \times 2^{n-1}}{2^n - 1} \tag{12.5}$$

In expression (12.5), if $V_1 = V_2 = \ldots = V_n = V$, then a logic '1' at the LSB position would contribute $V/(2^n - 1)$ to the analogue output, and a logic '1' in the next adjacent higher bit position would
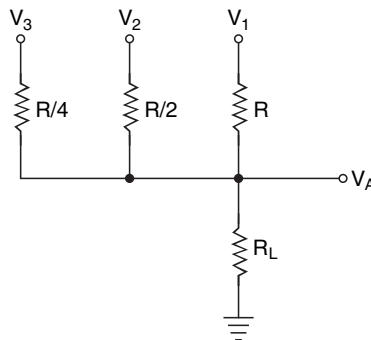

Figure 12.1   Simple resistive network for D/A conversion.

contribute $2V/(2^n - 1)$ to the output. The contributions of successive higher bit positions in the case of a logic '1' would be $4V/(2^n - 1)$, $8V/(2^n - 1)$, $16V/(2^n - 1)$ and so on. That is, the contribution of any given bit position owing to the presence of a logic '1' is twice the contribution of the adjacent lower bit position and half that of the adjacent higher bit position. When all input bit positions have a logic '1', the analogue output is given by

$$V_A = \frac{V(2^0 + 2^1 + 2^2 + \cdots + 2^{n-1})}{2^n - 1} = V \tag{12.6}$$

In the case of all inputs being in the logic '0' state, $V_A = 0$. Therefore, the analogue output varies from 0 to V volts as the digital input varies from an all 0s to an all 1s input.

12.1.2 Binary Ladder Network for D/A Conversion

The simple resistive divider network of Fig. 12.1 has two serious drawbacks. One, each resistor in the network is of a different value. Since these networks use precision resistors, the added expense becomes unattractive. Two, the resistor used for the most significant bit (MSB) is required to handle a much larger current than the LSB resistor. For example, in a 10-bit network, the current through the MSB resistor will be about 500 times the current through the LSB resistor.

To overcome these drawbacks, a second type of resistive network called the *binary ladder* (or *R/2R* ladder) is used in practice. The binary ladder, too, is a resistive network that produces an analogue output equal to the weighted sum of digital inputs. Figure 12.2 shows the binary ladder network for a four-bit D/A converter. As is clear from the figure, the ladder is made up of only two different values of resistor. This overcomes one of the drawbacks of the resistive divider network. It can be proved with the help of simple mathematics that the analogue output voltage V_A in the case of binary ladder network of Fig. 12.2 is given by

$$V_A = \frac{V_1 \times 2^0 + V_2 \times 2^1 + V_3 \times 2^2 + V_4 \times 2^3}{2^4} \tag{12.7}$$

In general, for an *n*-bit D/A converter using a binary ladder network

$$V_A = \frac{V_1 \times 2^0 + V_2 \times 2^1 + V_3 \times 2^2 + \cdots + V_n \times 2^{n-1}}{2^n} \tag{12.8}$$

For $V_1 = V_2 = V_3 = \cdots = V_n = V$, $V_A = [(2^n - 1)/2^n]V$. For $V_1 = V_2 = V_3 = \cdots = V_n = 0$, $V_A = 0$.
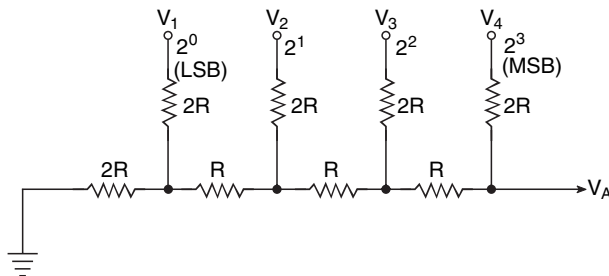

Figure 12.2   Binary ladder network for D/A conversion.
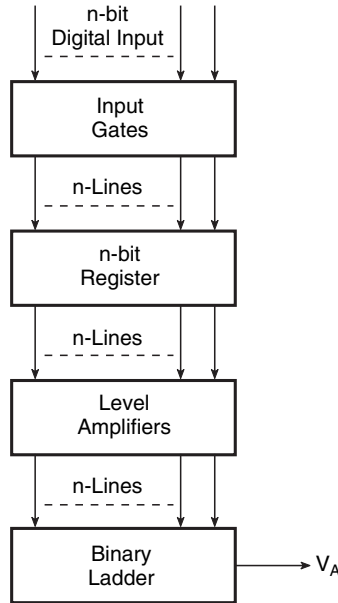
Figure 12.3   Block schematic representation of a D/A converter.

The analogue output voltage in this case varies from 0 (for an all 0s input) to $[(2^n - 1)/2^n]V$ (for an all 1s input).

Also, in the case of a resistive divider network, the LSB contribution to the analogue output is $[1/(2^n - 1)]V$. This is also the minimum possible incremental change in the analogue output voltage. The same in the case of a binary ladder network would be $(1/2^n)V$.

A binary ladder network is the most widely used network for digital-to-analogue conversion, for obvious reasons. Although actual D/A conversion takes place in this network, a practical D/A converter device has additional circuitry such as a register for temporary storage of input digital data and level amplifiers to ensure that the digital signals presented to the resistive network are all of the same level. Figure 12.3 shows a block schematic representation of a complete *n*-bit D/A converter. D/A converters of different sizes (eight-bit, 12-bit, 16-bit, etc.) are available in the form of integrated circuits.

12.2 D/A Converter Specifications

The major performance specifications of a D/A converter include resolution, accuracy, conversion speed, dynamic range, nonlinearity (NL) and differential nonlinearity (DNL) and monotonocity.

12.2.1 Resolution

The *resolution* of a D/A converter is the number of states (2^n) into which the full-scale range is divided or resolved. Here, *n* is the number of bits in the input digital word. The higher the number of bits, the better is the resolution. An eight-bit D/A converter has 255 resolvable levels. It is said to

have a percentage resolution of $(1/255) \times 100 = 0.39\%$ or simply an eight-bit resolution. A 12-bit D/A converter would have a percentage resolution of $(1/4095) \times 100 = 0.0244\%$. In general, for an *n*-bit D/A converter, the percentage resolution is given by $(1/2^n - 1) \times 100$. The resolution in millivolts for the two cases for a full-scale output of 5 V is approximately 20 mV (for an eight-bit converter) and 1.2 mV (for a 12-bit converter).

12.2.2 Accuracy

The *accuracy* of a D/A converter is the difference between the actual analogue output and the ideal expected output when a given digital input is applied. Sources of error include the *gain error* (or full-scale error), the *offset error* (or zero-scale error), *nonlinearity errors* and a drift of all these factors. The gain error [Fig. 12.4(a)] is the difference between the actual and ideal output voltage, expressed as a percentage of full-scale output. It is also expressed in terms of LSB. As an example, an accuracy of $\pm 0.1\%$ implies that the analogue output voltage may be off by as much as ± 5 mV for a full-scale output of 5 V throughout the analogue output voltage range. The offset error is the error at analogue zero [Fig. 12.4(b)].

12.2.3 Conversion Speed or Settling Time

The *conversion speed* of a D/A converter is expressed in terms of its settling time. The *settling time* is the time period that has elapsed for the analogue output to reach its final value within a specified error band after a digital input code change has been effected. General-purpose D/A converters have a settling time of several microseconds, while some of the high-speed D/A converters have a settling
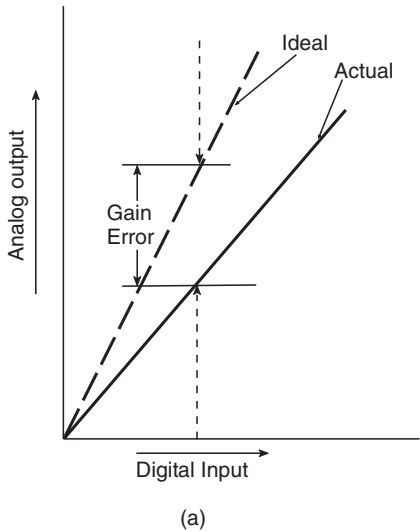

(a)

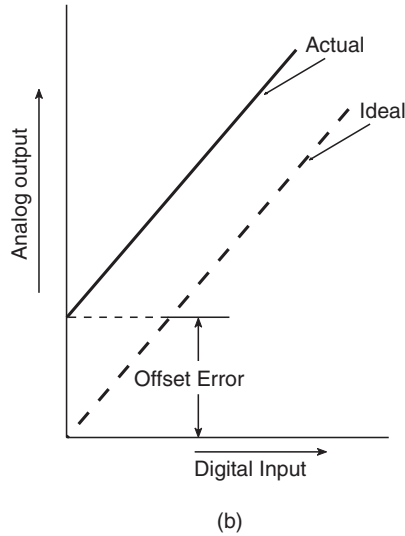**Figure 12.4** (a) Gain error and (b) offset error.

Figure 12.4 (*continued*).

time of a few nanoseconds. The settling time specification for D/A converter type number AD 9768 from Analog Devices USA, for instance, is 5 ns.

12.2.4 Dynamic Range

This is the ratio of the largest output to the smallest output, excluding zero, expressed in dB. For linear D/A converters it is $20 \times \log 2^n$, which is approximately equal to $6n$. For companding-type D/A converters, discussed in Section 12.3, it is typically 66 or 72 dB.

12.2.5 Nonlinearity and Differential Nonlinearity

Nonlinearity (NL) is the maximum deviation of analogue output voltage from a straight line drawn between the end points, expressed as a percentage of the full-scale range or in terms of LSBs. *Differential nonlinearity* (DNL) is the worst-case deviation of any adjacent analogue outputs from the ideal one-LSB step size.

12.2.6 Monotonocity

In an ideal D/A converter, the analogue output should increase by an identical step size for every one-LSB increment in the digital input word. When the input of such a converter is fed from the output of a counter, the converter output will be a perfect staircase waveform, as shown in Fig. 12.5. In such cases, the converter is said to be exhibiting perfect monotonocity. A D/A converter is considered as monotonic if its analogue output either increases or remains the same but does not decrease as the digital input code advances in one-LSB steps. If the DNL error of the converter is less than or equal to twice its worst-case nonlinearity error, it guarantees monotonocity.
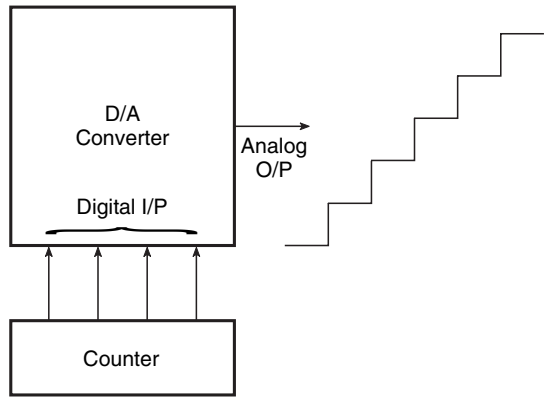
Figure 12.5   Monotonocity in a D/A converter.

12.3 Types of D/A Converter

The D/A converters discussed in this section include the following:

1. Multiplying-type D/A converters.
2. Bipolar-output D/A converters.
3. Companding D/A converters.

12.3.1 Multiplying D/A Converters

In a *multiplying-type D/A converter*, the converter multiplies an analogue reference by the digital input. Figure 12.6 shows the circuit representation. Some D/A converters can multiply only positive digital words by a positive reference. This is known as single quadrant (QUAD-I) operation. Two-quadrant operation (QUAD-I and QUAD-III) can be achieved in a D/A converter by configuring the output for bipolar operation. This is accomplished by offsetting the output by a negative MSB (equal to the analogue output of 1/2 of the full-scale range) so that the MSB becomes the sign bit.
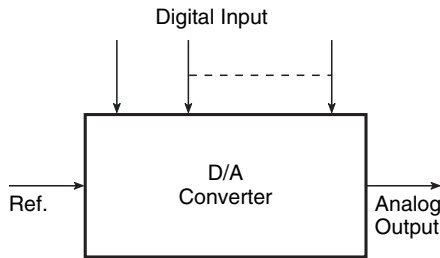

Figure 12.6   Multiplying-type D/A converter.

Some D/A converters even provide four-quadrant operation by allowing the use of both positive and negative reference. Multiplying D/A converters are particularly useful when we are looking for digitally programmable attenuation of an analogue input signal.

12.3.2 Bipolar-Output D/A Converters

In *bipolar-output D/A converters* the analogue output signal range includes both positive and negative values. The transfer characteristics of an ideal two-quadrant bipolar-output D/A converter are shown in Fig. 12.7.

12.3.3 Companding D/A Converters

Companding-type D/A converters are so constructed that the more significant bits of the digital input have a larger than binary relationship to the less significant bits. This decreases the resolution of the more significant bits, which in turn increases the analogue signal range. The effect of this is to compress more data into more significant bits.

12.4 Modes of Operation

D/A converters are usually operated in either of the following two modes of operation:

1. Current steering mode.
2. Voltage switching mode.

12.4.1 Current Steering Mode of Operation

In the *current steering mode* of operation of a D/A converter, the analogue output is a current equal to the product of a reference voltage and a fractional binary value D of the input digital word. D is equal to the sum of fractional binary values of different bits in the digital word. Also, fractional binary values of different bits in an n-bit digital word starting from the LSB are $2^0/2^n, 2^1/2^n, 2^2/2^n, \ldots, 2^{n-1}/2^n$.
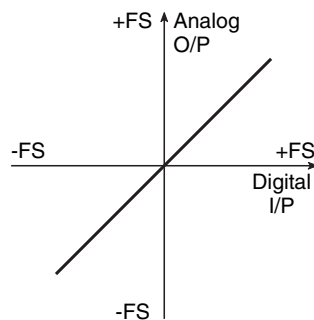

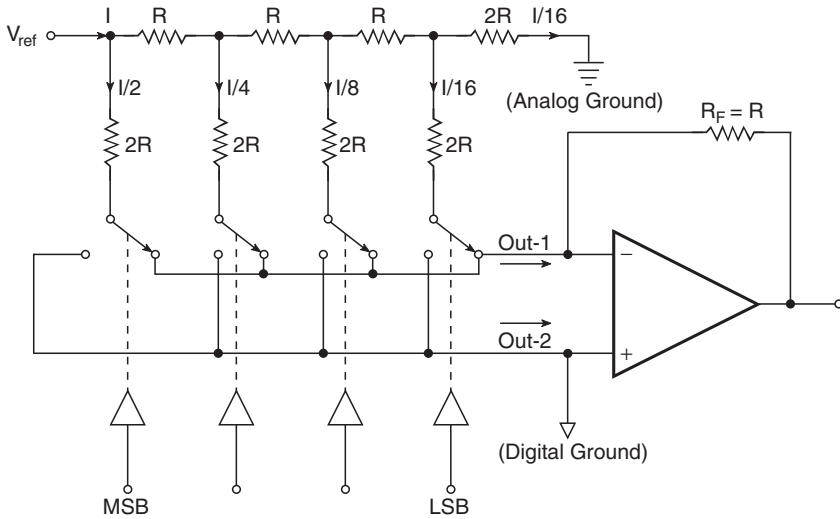**Figure 12.7**   Bipolar-output D/A converter transfer characteristics.

Figure 12.8   Current steering mode of operation of a D/A converter.

The output current is often converted into a corresponding voltage using an external opamp wired as a current-to-voltage converter. Figure 12.8 shows the circuit arrangement. The majority of D/A converters in IC form have an in-built opamp that can be used for current-to-voltage conversion. For the circuit arrangement of Fig. 12.8, if the feedback resistor R_F equals the ladder resistance R, the analogue output voltage at the opamp output is $-(D.V_{ref})$.

The arrangement of the four-bit D/A converter of Fig. 12.8 can be conveniently used to explain the operation of a D/A converter in the current steering mode. The $R/2R$ ladder network divides the input current I due to a reference voltage V_{ref} applied at the reference voltage input of the D/A converter into binary weighted currents, as shown. These currents are then steered to either the output designated Out-1 or Out-2 by the current steering switches. The positions of these current steering switches are controlled by the digital input word. A logic '1' steers the corresponding current to Out-1, whereas a logic '0' steers it to Out-2. For instance, a logic '1' in the MSB position will steer the current $I/2$ to Out-1. A logic '0' steers it to Out-2, which is the ground terminal. In the four-bit converter of Fig. 12.8, the analogue output current (or voltage) will be maximum for a digital input of 1111. The analogue output current in this case will be $I/2 + I/4 + I/8 + I/16 = (15/16)I$. The analogue output voltage will be $(-15/16)IR_F = (-15/16)IR$. Also, $I = V_{ref}/R$ as the equivalent resistance of the ladder network across V_{ref} is also R. The analogue output voltage is then $[(-15/16)(V_{ref})/R] \times R = (-15/16)V_{ref}$. Here, 15/16 is nothing but the fractional binary value of digital input 1111. In general, the maximum analogue output voltage is given by $-(1 - 2^{-n}) \times V_{ref}$, where n is the number of bits in the input digital word.

12.4.2 Voltage Switching Mode of Operation

In the *voltage switching mode* of operation of a $R/2R$ ladder type D/A converter, the reference voltage is applied to the Out-1 terminal and the output is taken from the reference voltage terminal. Out-2 is joined to analogue ground. Figure 12.9 shows a four-bit D/A converter of the $R/2R$ ladder type in
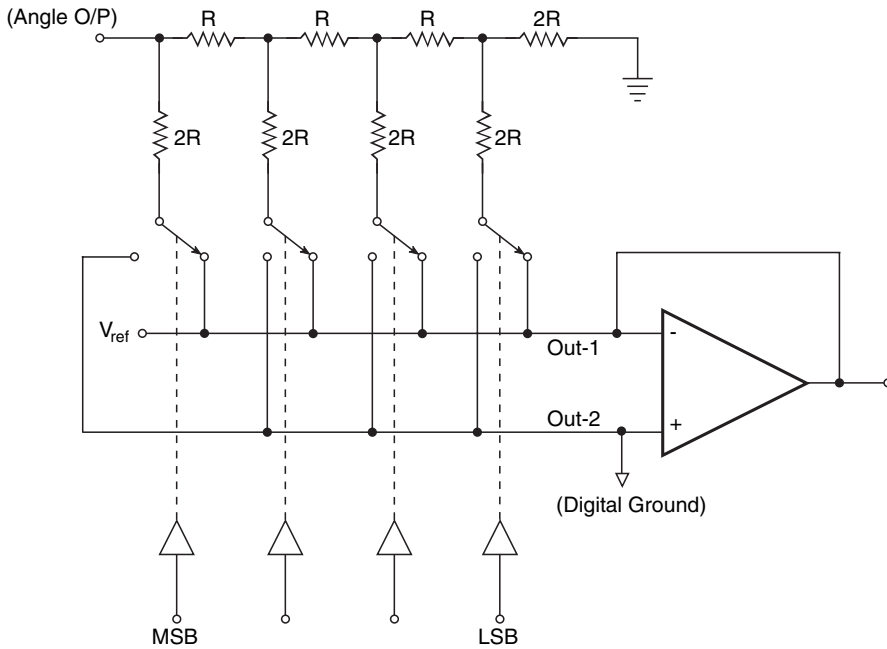
Figure 12.9   Voltage switching mode of operation of a D/A converter.

voltage switching mode of operation. The output voltage is the product of the fractional binary value of the digital input word and the reference voltage applied at the Out-1 terminal, i.e. $D.V_{ref}$. As the positive reference voltage produces a positive analogue output voltage, the voltage switching mode of operation is possible with a single supply. As the circuit produces analogue output voltage, it obviates the need for an opamp and the feedback resistor. However, the reference voltage applied to the Out-1 terminal in this case will see different input impedances for different digital inputs. For this reason, the source of the input is buffered.

12.5 BCD-Input D/A Converter

A BCD-input D/A converter accepts the BCD equivalent of decimal digits at its input. A two-digit BCD D/A converter for instance is an eight-bit D/A converter. Figure 12.10 shows the circuit representation of an eight-bit BCD-type D/A converter. Such a converter has 99 steps and accepts decimal digits 00 to 99 at its input. A 12-bit converter will have 999 steps. The weight of the different bits in the least significant digit (LSD) will be 1 (for A_0), 2 (for B_0), 4 (for C_0) and 8 (for D_0). The weights of the corresponding bits in the next higher digit will be 10 times the weights of corresponding bits in the lower adjacent digit. For the D/A converter shown in Fig. 12.10 the weight of the different bits in the most significant digit (MSD) will be 10 (for A_1), 20 (for B_1), 40 (for C_1) and 80 (for D_1). In general, an n-bit D/A converter of the BCD input type will have $(10^{n/4} - 1)$ steps. The percentage resolution of such a converter is given by $[1/(10^{n/4} - 1)] \times 100$.
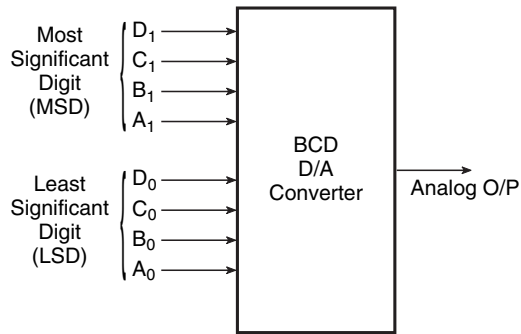
Figure 12.10   BCD-input D/A converter.

Example 12.1

An eight-bit D/A converter has a step size of 20 mV. Determine the full-scale output and percentage resolution.

Solution

- $(1/2^8) \times V = 20 \times 10^{-3}$, where V is the voltage corresponding to a logic '1'.
- This gives $V = 20 \times 10^{-3} \times 2^8 = 5.12$V.
- The full-scale output $= [(2^n - 1)/2^n] \times V = [(2^8 - 1)/2^8] \times 5.12 = (255/256) \times 5.12 = 5.1$V.
- The percentage resolution $= [1/(2^n - 1)] \times 100 = 100/255 = 0.392\%$.
- The percentage resolution can also be determined from: (Step size/full-scale output) $\times$ 100 $=$ $(20 \times 10^{-3}/5.1) \times 100 = 0.392\%$.

Example 12.2

Refer to Fig. 12.11. This BCD D/A converter has a step size of 6.25 mV. Determine the full-scale output.

Solution

- A step size of 6.25 mV implies that A_0 has a weight of 6.25 mV.
- The weights of B_0, C_0 and D_0 would respectively be 12.5, 25 and 50 mV.
- Now, the weight of A_1 will be 10 times the weight of A_0, i.e. the weight of A_1 will be 62.5 mV.
- The weights of B_1, C_1 and D_1 will accordingly be 125, 250 and 500 mV respectively.
- On similar lines, the weights of A_2, B_2, C_2 and D_2 will respectively be 625 mV, 1.25 V, 2.5 V and 5 V.
- For full-scale output, the input will be decimal 999. Each of the three four-bit groups will be 1001.
- Therefore, the full-scale analogue output $= 6.25 + 50 + 62.5 + 500 + 625 + 5000$ mV $= 6.24375$ V.
- The full-scale analogue output can also be determined from the product of the step size and number of steps. That is, the full-scale output $= 6.25 \times 999 = 6.24375$ V.
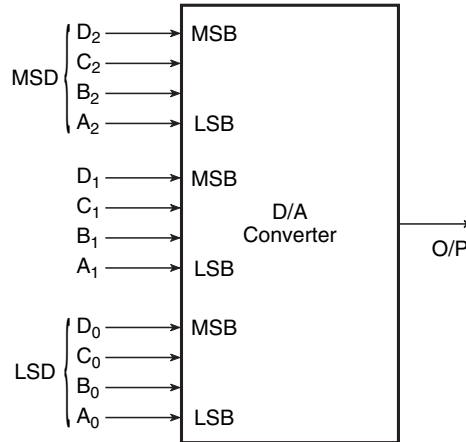
Figure 12.11   BCD-input D/A converter (example 12.2).

Example 12.3

A certain eight-bit D/A converter has a full-scale output of 5 mA and a full-scale error of ±0.25 % of full scale. Determine the range of expected analogue output for a digital input of 10000010.

Solution
- Step size $= \dfrac{\text{Full-scale output}}{\text{Number of steps}}$

$$= \frac{5 \times 10^{-3}}{2^8 - 1}$$

$$= 19.6 \ \mu\text{A}$$

- For a digital input of 10000010 ($= 130_{10}$) the analogue output is given by $130 \times 19.6 = 2.548$ mA.
- Error $= \pm \dfrac{0.25 \times 5 \times 10^{-3}}{100}$

$$= \pm 12.5 \ \mu\text{A}$$

- The expected analogue output will therefore be in the range 2.5355–2.5605 mA.

Example 12.4

An experimenter connects a four-bit ripple counter to a four-bit D/A converter to perform a staircase test using a 1 kHz clock as shown in Fig. 12.12. The output staircase waveform is shown in Fig. 12.13. The cause of the incorrect staircase signal is later determined to be a wrong connection between the counter output and the D/A converter input. What is it?

Solution
The correct staircase waveform would be generated at the output of the D/A converter if the counter outputs Q_0 (LSB), Q_1, Q_2 and Q_3 (MSB) were connected to the corresponding inputs
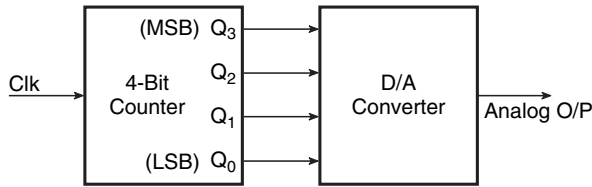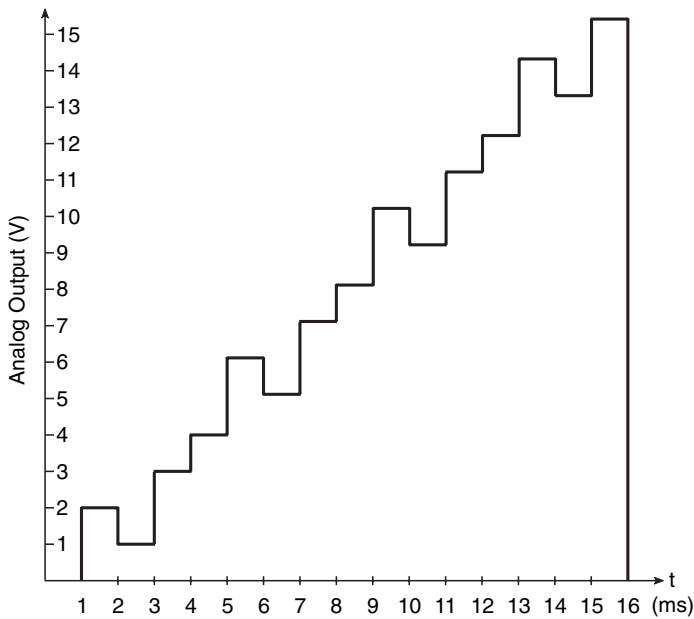
Figure 12.12   Example 12.4.

Figure 12.13   Staircase waveform (example 12.4).

of the D/A converter in the same order. If we carefully examine the given staircase waveform and recall the sequence in which the counter will advance, it can be visualized that the given staircase waveform would result if the interconnections of the LSB and the next adjacent higher bit of the counter output and the corresponding inputs of the D/A converter were interchanged. While in one complete cycle the counter counts as 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110 and 1111, the D/A converter, owing to interchanged connections, gets inputs as 0000, 0010, 0001, 0011, 0100, 0110, 0101, 0111, 1000, 1010, 1001, 1011, 1100, 1110, 1101 and 1111. The corresponding analogue outputs are 0, 2, 1, 3, 4, 6, 5, 7, 8, 10, 9, 11, 12, 14, 13 and 15 V, as shown in the staircase waveform of Fig. 12.13.

12.6 Integrated Circuit D/A Converters

This section presents application-relevant information on some of the commonly used D/A converter IC type numbers, as it is not possible to give a detailed description of each one of them. The type numbers included for this purpose are DAC-08/0800, DAC-80, DAC-0808, AD 7524 and DAC-1408A/1508A.

12.6.1 DAC-08

DAC-08 is an eight-bit monolithic D/A converter. Its major performance specifications include a settling time of 85 ns, a monotonic multiplying performance over a wide 20-to-1 reference current range, a direct interface to all popular logic families, high voltage compliance complementary current outputs, nonlinearities of $\pm0.1\,\%$ over the entire operating temperature range and a wide power supply range of ±4.5 V to ±18 V. Figures 12.14(a) and (b) respectively show the basic circuit configurations for positive low impedance output operation and negative low impedance output operation. DAC-08
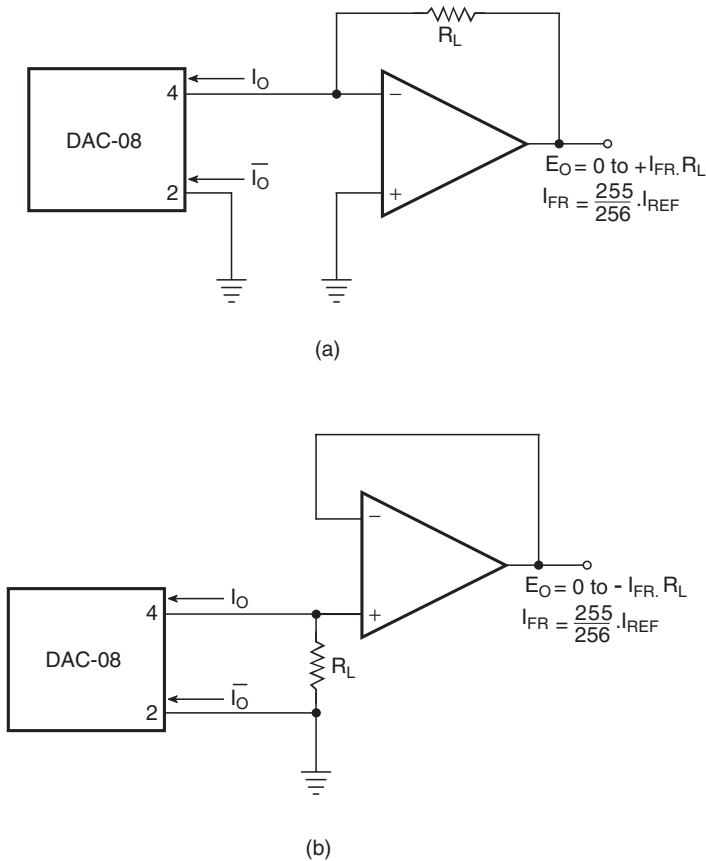

(a)

(b)

Figure 12.14 (a) Basic circuit configuration of DAC-08 for positive output operation and (b) the basic circuit configuration of DAC-08 for negative output operation.

applications include waveform generators, servomotor and pen drivers, audio encoders and digitally controlled attenuators, analogue meter drivers, programmable power supplies, high-speed modems, CRT display drivers, etc.

12.6.2 DAC-0808

DAC-0808 is an eight-bit D/A converter featuring a full-scale output current settling time of 150 ns while dissipating only 33 mW with ± 5 V supplies. Relative accuracies of better than $\pm 0.19\%$ ensure eight-bit monotonocity and linearity, while zero-level output current of less than 4 mA provides eight-bit zero accuracy for $I_{ref} \geq 2$ mA. It has a wide power supply voltage range of ± 4.5 V to ± 18 V. It can interface directly with popular TTL, DTL or CMOS logic families and is a direct replacement for the D/A converter MC 1508/MC 1408. Figure 12.15 shows the application circuit of DAC-0808 wired as a voltage-output D/A converter.

12.6.3 DAC-80

DAC-80 is a 12-bit D/A converter. Both current and voltage-output versions are available. Its salient features include low power dissipation (345 mW), full $\pm$ 10 V swing with ± 12 V supplies, TTL and CMOS-compatible digital inputs, $\pm 1/2$ LSB maximum nonlinearity over 0–70 °C, guaranteed monotonocity over 0–70 °C and 4 ms settling time to $\pm 0.01\%$ of full-scale and monolithic design. Figures 12.16 and 12.17 show the pin connection diagrams of current-output and voltage-output models of DAC-80.
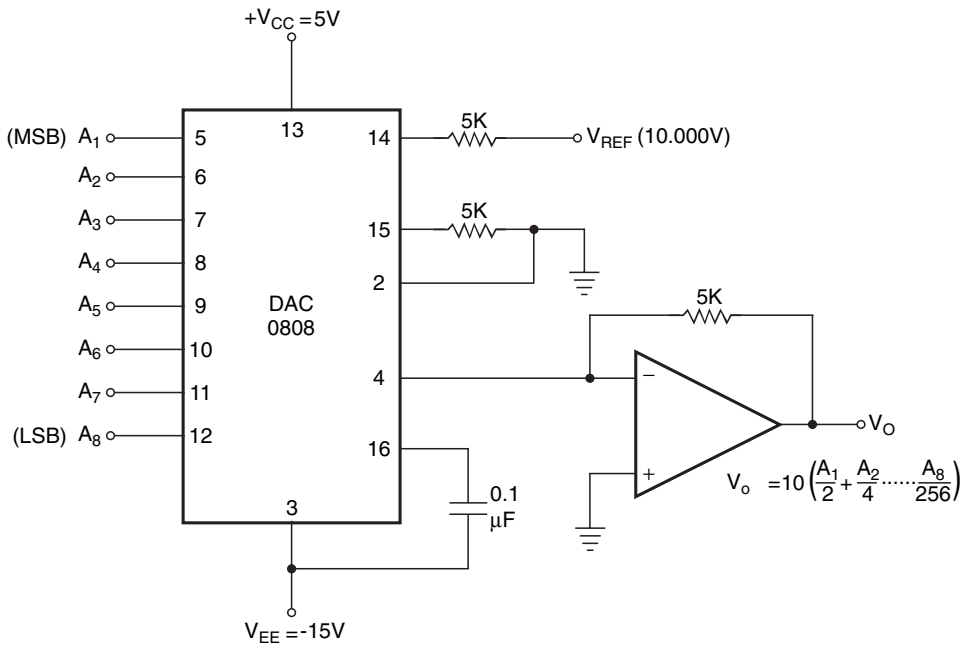

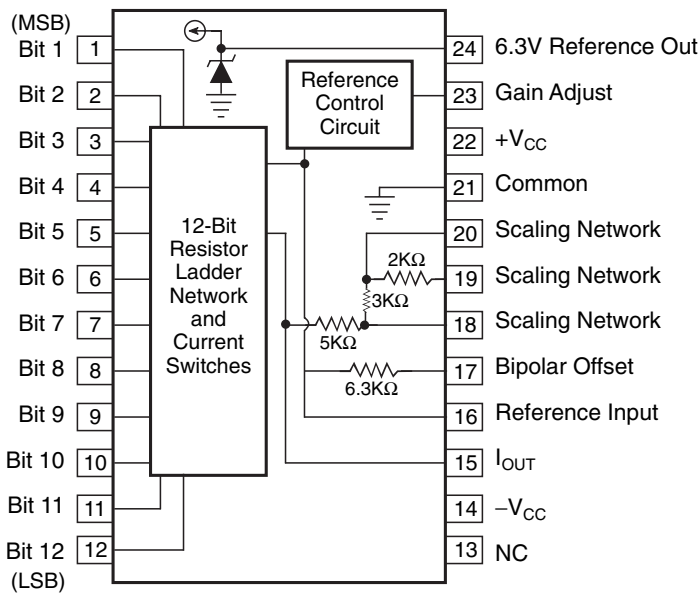**Figure 12.15**   DAC-0808 wired as a voltage-output D/A converter.

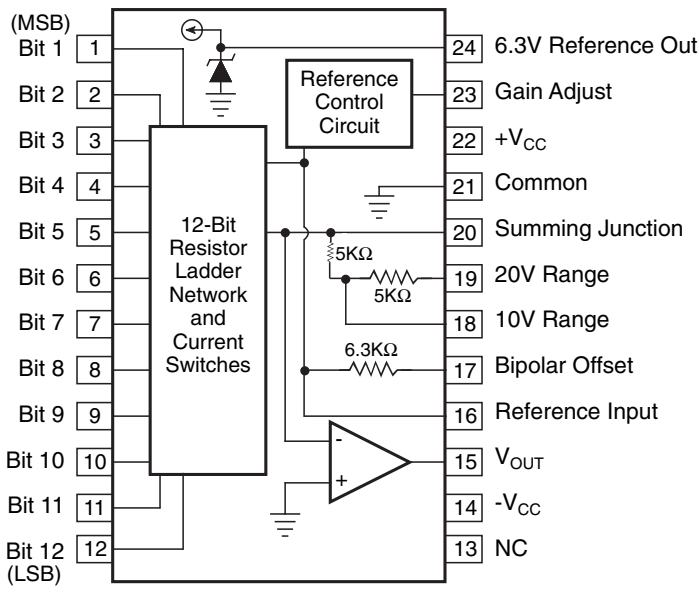**Figure 12.16** Pin connection diagram of DAC-80 (current-output version).

Figure 12.17 Pin connection diagram of DAC-80 (voltage-output version).

12.6.4 AD 7524

AD 7524 is an eight-bit monolithic CMOS DAC designed for direct interface to most microprocessors such as 6800, 8085, Z80, etc. It has an accuracy of 1/8 LSB, with a typical power dissipation of less than 10 mW. Monotonocity is guaranteed over full operation temperature range. It has a settling time of 250 ns (typical) for the output current to settle within 1/2 LSB for a supply voltage of +15 V. Its excellent multiplying characteristics (two or four-quadrant) make AD 7524 an ideal choice for many microprocessor-controlled gain setting and signal control applications. It has a wide power supply range of +5 V to +15 V. Figure 12.18 shows the functional diagram which resembles the functional diagram of any current-output multiplying D/A converter.

12.6.5 DAC-1408/DAC-1508

DAC-1508/1408 is a general-purpose, high-speed multiplying-type eight-bit D/A converter. DAC-1508 is identical to DAC-1408 except for the operational temperature range, which is −55°C to +125 °C in the case of DAC-1508, as against 0–70 °C for DAC-1408. It is pin and functionally compatible with DAC-0808.
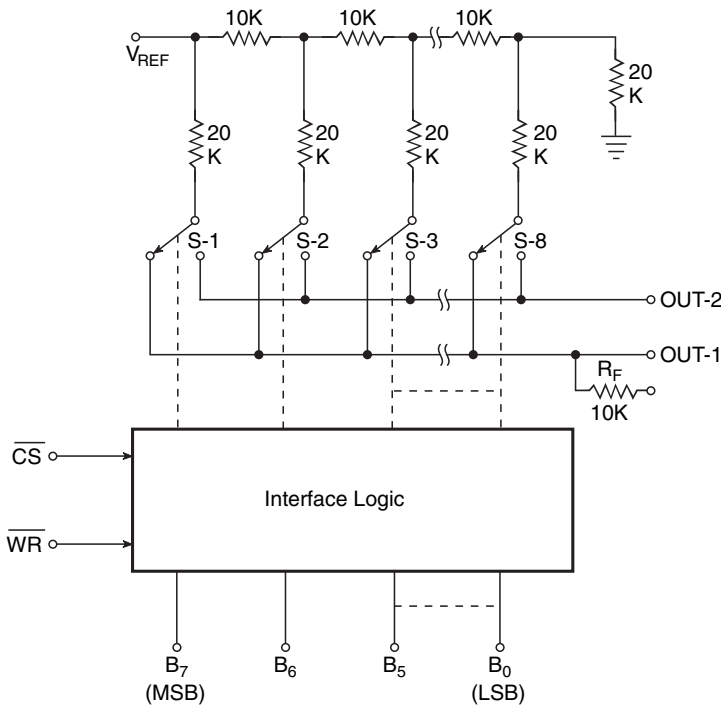

Figure 12.18   Functional diagram of AD 7524.

12.7 D/A Converter Applications

In addition to being an integral part of some of the architectures of popular varieties of A/D converters, D/A converters are extensively used in a variety of other application circuits. Some common applications include multipliers, digitally controlled dividers, programmable integrators, low-frequency function generators and digitally controlled filters.

12.7.1 D/A Converter as a Multiplier

The basic D/A converter operated in the current steering mode with the output opamp wired as a current-to-voltage converter works as a multiplier where the output voltage is the product of the analogue input applied at the V_{ref} terminal and the digital word input. CMOS D/A converters are much better suited to multiplying applications as the multiplying capabilities of other types of D/A converter are restricted to a limited range of input voltage. One such application circuit where the multiplying capability of the D/A converter is used is the digitally controlled audio signal attenuator. Figure 12.19 shows the circuit diagram. The audio signal is applied to the V_{ref} input and the attenuation code is applied to the digital input. The analogue output is the attenuated version of the input.

As audio attenuators, conventional D/A converters provide a limited range of attenuation which is 256:1 or 48 dB for an eight-bit converter and 4096:1 or 72 dB for a 12-bit converter. Logarithmic D/A converters, which give a logarithmic relationship between the digital fraction and the output signal matching the response of the human ear, are particularly suitable for this application. These are coded to give attenuation in equal decimal steps.

12.7.2 D/A converter as a Divider

If the feedback resistance is used as the input resistor and the D/A converter is connected as a feedback element, the circuit acts as a divider or a programmable gain element. Figure 12.20 shows the circuit configuration. The output is given by $V_o = -(V_{in}/D)$. For smaller values of digital fraction D the output increases, and the designer should ensure that the amplifier does not saturate under these conditions.
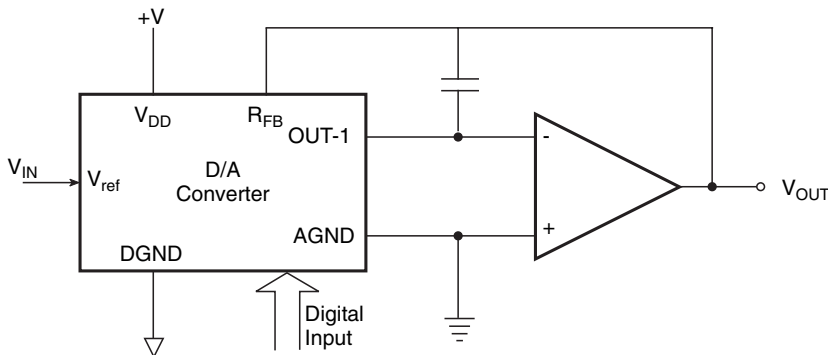

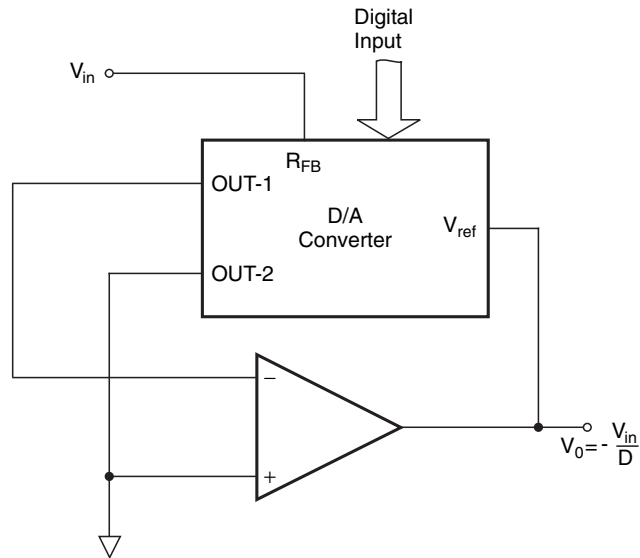**Figure 12.19** Digitally controlled audio signal attenuator.

Figure 12.20   Digitally controlled divider.

12.7.3 Programmable Integrator

The programmable integrator forms the basis of a number of medium-frequency function generators. Figure 12.21 shows an inverting type of programmable integrator. The output is expressed by

$$V_o = [-1/C.(R_{DAC} + R_1)].D \int V_{in}.dt \qquad (12.9)$$

where R_{DAC} isthe input resistance of the D/A converter at the V_{ref} terminal. Resistance R_1 has been used to get an appropriate value of the integrator time constant for the full-scale value of D. The integrator time constant given by $[C.(R_{DAC} + R_1)/D]$ is largest when the input digital code is near zero and
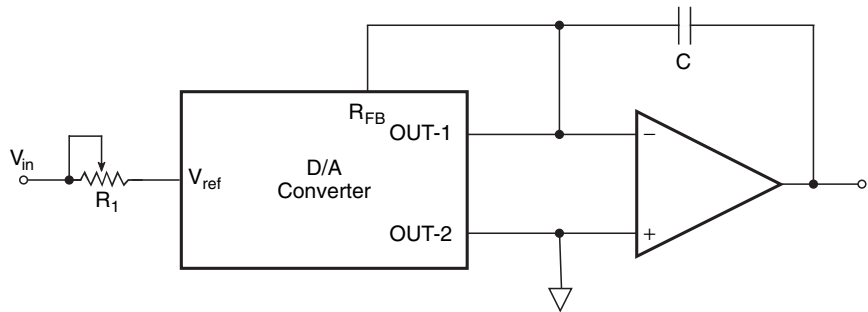

Figure 12.21   Inverting-type programmable integrator.

smallest when D has the full-scale value. Figure 12.22 shows the noninverting type of programmable integrator. The output in this case is given by

$$V_o = (D/CR_1) \int V_{in}.dt \qquad (12.10)$$

12.7.4 Low-Frequency Function Generator

Figure 12.23 shows one possible circuit configuration of a D/A converter based low-frequency function generator. There is no limit to the lowest frequency possible using this configuration. The upper limit
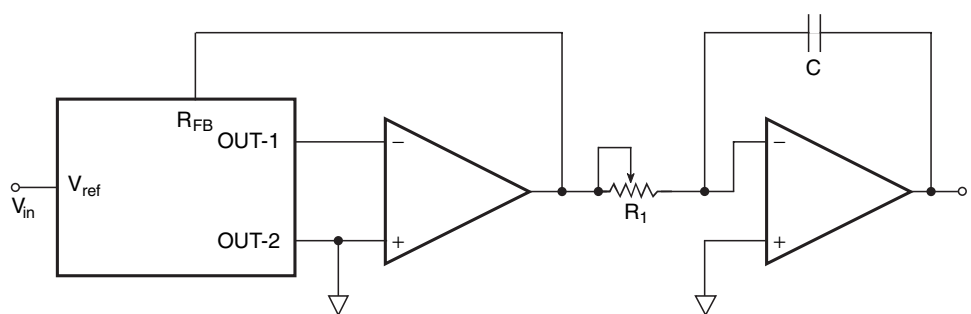

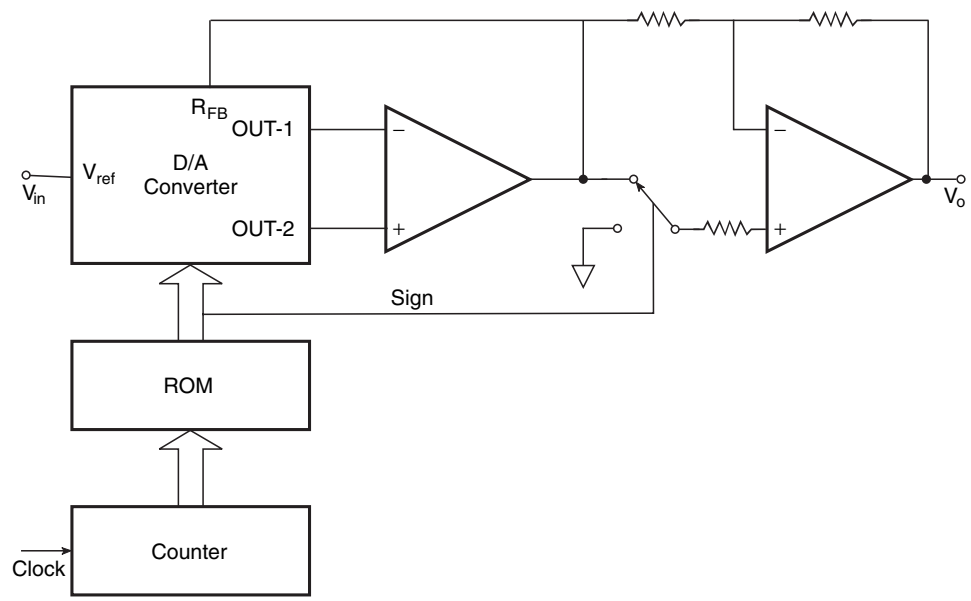**Figure 12.22** Non-inverting programmable integrator.

Figure 12.23 Low-frequency function generator.

is determined by the settling time of the D/A converter, the required resolution and the permissible quantization noise.

Since most of the functions are symmetric, it is usual to synthesize only half of the waveform and then invert it for the second half. This is true for pulse, triangular, ramp and trapezoidal waveforms. For sinusoidal waveforms it is necessary only to synthesize one-quarter of the waveform. In the arrangement of Fig. 12.23, the frequency is determined by the clock frequency and the waveform by the contents of the ROM.

12.7.5 Digitally Controlled Filters

Active filters having low noise and distortion with controllable gain, centre frequency and Q-factor can be constructed using multiplying-type D/A converters. Three basic types of first-order low-pass filter are shown in Figs 12.24, 12.25 and 12.26. The low-pass circuit of Fig. 12.24 has a R_{DAC}-dependent cut-off frequency given by
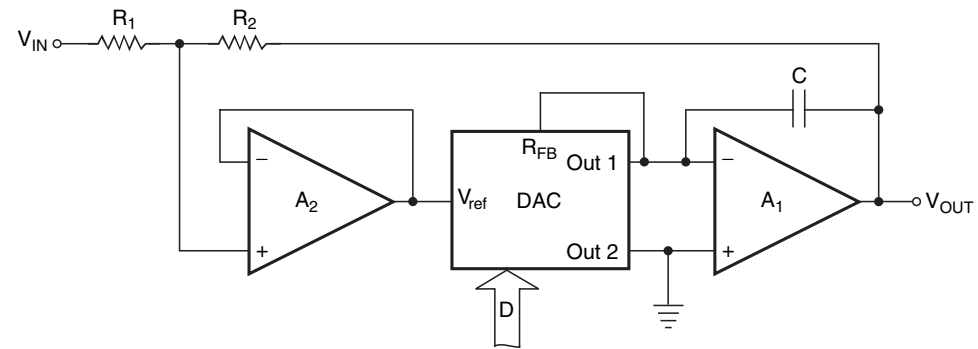
$$\omega = [R_1/(R_1 + R_2)] \times [D/C.R_{DAC}] \qquad (12.11)$$

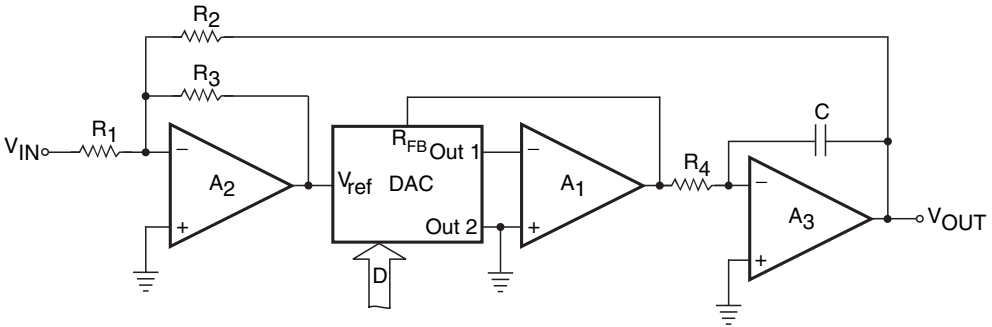**Figure 12.24** Low-pass filter with R_{DAC}-dependent cut-off frequency.

Figure 12.25 Low-pass filter with cut-off frequency independent of R_{DAC}.

Figure 12.26   Low-pass filter with a programmable time constant.

Also, the transfer function for this low-pass filter is given by

$$V_{out}/V_{in} = (-R_2/R_1)\{1/[1+j\omega(R_1+R_2).R_{DAC}.C/R_1.D]\} \tag{12.12}$$

The cut-off frequency can be made independent of R_{DAC} by using the D/A converter as a programmable gain element, as shown in Fig. 12.25. In this case, the cut-off frequency ω is given by

$$\omega = R_3.D/R_2.R_4.C \tag{12.13}$$

and the transfer function is given by

$$V_{out}/V_{in} = (-R_2/R_1)\{1/[1+j\omega(R_2.R_4.C/R_3.D)]\} \tag{12.14}$$

If it is required to have a proportional adjustment of the filter time constant rather than its cut-off frequency, the circuit of Fig. 12.25 is rearranged and the D/A converter is connected in the divider configuration as shown in Fig. 12.26. The time constant is given by

$$Time\ constant = R_2.R_4.C.D/R_3 \tag{12.15}$$

and the transfer function is given by

$$V_{out}/V_{in} = (R_2/R_1)\{1/[1 + j\omega(R_2.R_4.C.D/R_3)]\} \tag{12.16}$$

It may be mentioned here that other types of digitally controlled filter are also possible using D/A converters. One such possibility, for instance, is by using state variable techniques, which can be used to design D/A converter based programmable filters to get low-pass, high-pass and band-pass functions from the same circuit.

12.8 A/D Converters

After digital-to-analogue converters, the discussion in the following paragraphs is on another vital data conversion integrated circuit component known as the analogue-to-digital (A/D) converter. An A/D converter is a very important building block and has numerous applications. It forms an essential interface when it comes to analysing analogue data with a digital computer. It is an indispensable part of any digital communication system where the analogue signal to be transmitted is digitized at the sending end with the help of an A/D converter. It is invariably used in all digital read-out test and measuring equipment. Be it a digital voltmeter or a laser power meter, or for that matter even a pH meter, an A/D converter is the heart of all of them.

An A/D converter takes at its input an analogue voltage and after a certain amount of time produces a digital output code representing the analogue input. The A/D conversion process is generally more complex than the D/A conversion process. There are various techniques developed for the purpose of A/D conversion, and these techniques have different advantages and disadvantages with respect to one another, which have been utilized in the fabrication of different categories of A/D converter ICs. A D/A converter circuit, as we will see in the following paragraphs, forms a part of some of the types of A/D converter.

We begin with a brief interpretation of the terminology and the major specifications that are relevant to the understanding of A/D converters. The idea is to enable the designers to make a judicious choice of A/D converter suitable for their application. A brief comparative study of different types of A/D converter and the suitability of each one of these types for a given application requirement is also discussed. This is followed by application-relevant information on some of the more popular A/D converter IC type numbers.

12.9 A/D Converter Specifications

The major performance specifications of an A/D converter include resolution, accuracy, gain and offset errors, gain and offset drifts, the sampling frequency and aliasing phenomenon, quantization error, nonlinearity, differential nonlinearity, conversion time, aperture and acquisition times and code width. Each one of these is briefly described in the following paragraphs.

12.9.1 Resolution

The *resolution* of an A/D converter is the quantum of the input analogue voltage change required to increment its digital output from one code to the next higher code. An n-bit A/D converter can resolve one part in $2^n - 1$. It may be expressed as a percentage of full scale or in bits. The resolution of an eight-bit A/D converter, for example, can be expressed as one part in 255 or as 0.4 % of full scale or

simply as eight-bit resolution. If such a converter has a full-scale analogue input range of 10 V, it can resolve a 40 mV change in input.

12.9.2 Accuracy

The *accuracy* specification describes the maximum sum of all errors, both from analogue sources (mainly the comparator and the ladder resistors) and from the digital sources (quantization error) of the A/D converter. These errors mainly include the gain error, the offset error and the quantization error. The accuracy describes the actual analogue input and full-scale weighted equivalent of the output code corresponding to the actual analogue input. The accuracy specification is rarely provided on the datasheets, and quite often several sources of errors are listed separately.

12.9.3 Gain and Offset Errors

The *gain error* is the difference between the actual full-scale transition voltage and the ideal full-scale transition voltage. It is expressed either as a percentage of the full-scale range (% of FSR) or in LSBs. The *offset error* is the error at analogue zero for an A/D converter operating in bipolar mode. It is measured in % of FSR or in LSBs.

12.9.4 Gain and Offset Drifts

The *gain drift* is the change in the full-scale transition voltage measured over the entire operating temperature range. It is expressed in full scale per degree Celsius or ppm of full scale per degree Celsius or LSBs. The *offset drift* is the change with temperature in the analogue zero for an A/D converter operating in bipolar mode. It is generally expressed in ppm of full scale per degree Celsius or LSBs.

12.9.5 Sampling Frequency and Aliasing Phenomenon

If the rate at which the analogue signal to be digitized is sampled is at least twice the highest frequency in the analogue signal, which is what is embodied in the Shannon–Nyquist sampling theorem, then the analogue signal can be faithfully reproduced from its quantized values by using a suitable interpolation algorithm. The accuracy of the reproduced signal is, however, limited by the quantization error (discussed in Section 12.9.6). If the sampling rate is inadequate, i.e. if it is less than the Nyquist rate, then the reproduced signal is not a faithful reproduction of the original signal and these spurious signals, called aliases, are produced. The frequency of an aliased signal is the difference between the signal frequency and the sampling frequency. For example, if sampled at a 1.5 kHz rate, a 2 kHz sine wave would be reconstructed as a 500 Hz sine wave. This problem is called *aliasing* and, in order to avoid it, the analogue input signal is low-pass filtered to remove all frequency components above half the sampling rate. This filter, called an *anti-aliasing filter*, is used in all practical A/D converters.

12.9.6 Quantization Error

The *quantization error* is inherent to the digitizing process. For a given analogue input voltage range it can be reduced by increasing the number of digitized levels. An A/D converter having an *n*-bit

output can only identify 2^n output codes while there are an infinite number of analogue input values adjacent to the LSB of the A/D converter that are assigned the same output code. For instance, if we are digitizing an analogue signal with a peak value of 7 V using three bits, then all analogue voltages equal to or greater than 5.5 V and less than or equal to 6.5 V will be represented by the same output code, i.e. 110 (if the output coding is in straight binary form). The error is ±0.5 V or ±1/2 LSB, as a one-LSB change in the output corresponds to an analogue change of 1 V in this case. The ±1/2 LSB limit to resolution is known as the fundamental quantization error. Expressed as a percentage, the quantization error in an eight-bit converter is one part in 255 or 0.4 %.

12.9.7 Nonlinearity

The *nonlinearity* specification [also referred to as the integral nonlinearity (INL) by some manufacturers] of an A/D converter describes its departure from a linear transfer curve. The nonlinearity error does not include gain, offset and quantization errors. It is expressed as a percentage of full scale or in LSBs.

12.9.8 Differential Nonlinearity

This indicates the worst-case difference between the actual analogue voltage change and the ideal one-LSB voltage change. The DNL specification is as important as the INL specification, as an A/D converter having a good INL specification may have a poor-quality transfer curve if the DNL specification is poor. DNL is also expressed as a percentage of full scale or in LSBs. DNL in fact explains the smoothness of the transfer characteristics and is thus of great importance to the user. Figure 12.27 shows the transfer curve for a three-bit A/D converter with a 7 V full-scale range, 1/4-LSB INL and one-LSB DNL. Figure 12.28 shows the same for a 7 V full-scale range, one-LSB INL and 1/4-LSB DNL. Although the former has a much better INL specification, the latter, with a better DNL specification, has a much better and smoother curve and may thus be preferred. Too high a value of DNL may even grossly degrade the converter resolution. In a four-bit converter
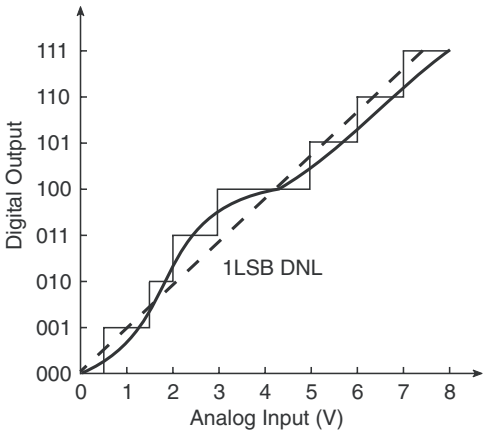

Figure 12.27 Transfer characteristics of a three-bit A/D converter (INL = one LSB, DNL = 1LSB).
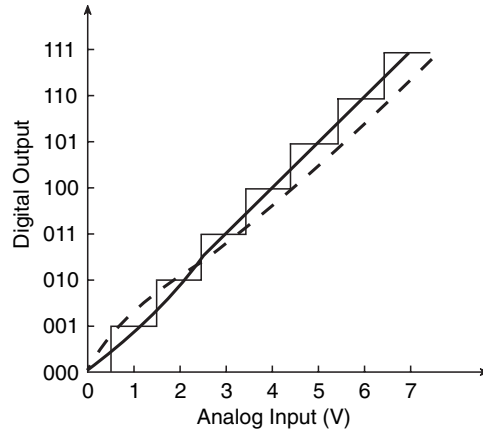
Figure 12.28   Transfer characteristics of a three-bit A/D converter (INL = one LSB, DNL = 1/4 LSB).

with a ±2 LSB DNL, the 16-step transfer curve may be reduced to a six-step curve. The DNL specification should in no case be ignored, unless the INL specification is tight enough to guarantee the desirable DNL.

12.9.9 Conversion Time

This is the time that elapses from the time instant of the start of the conversion signal until the conversion complete signal occurs. It ranges from a few nanoseconds for flash-type A/D converters to a few microseconds for successive approximation type A/D converters and may be as large as tens of milliseconds for dual-slope integrating A/D converters.

12.9.10 Aperture and Acquisition Times

When a rapidly changing signal is digitized, the input signal amplitude will have changed even before the conversion is complete, with the result that the output of the A/D converter does not represent the signal amplitude at the start. A *sample-and-hold* circuit with a buffer amplifier is used at the input of the A/D converter to overcome this problem. The aperture and acquisition times are the parameters of the sample-and-hold circuit. The signal to be digitized is sampled with an electronic switch that can be rapidly turned ON and OFF. The sampled amplitude is then stored on the hold capacitor. The A/D converter digitizes the stored voltage, and, after the conversion is complete, a new sample is taken and held for the next conversion. The *acquisition time* is the time required for the electronic switch to close and the hold capacitor to charge, while the *aperture time* is the time needed for the switch completely to open after the occurrence of the hold signal. Ideally, both times should be zero. The maximum sampling frequency is thus determined by the aperture and acquisition times in addition to the conversion time.

12.9.11 Code Width

The *code width* is the quantum of input voltage change that occurs between the output code transitions expressed in LSBs of full scale. *Code width uncertainty* is the dynamic variation or *jitter* in the code width owing to noise.

12.10 A/D Converter Terminology

Some of the more commonly used terms while interpreting the specifications and salient features of A/D converters are briefly described in the following paragraphs.

12.10.1 Unipolar Mode Operation

In the unipolar mode of operation, the analogue input to the A/D converter varies from 0 to full-scale voltage of one polarity only.

12.10.2 Bipolar Mode Operation

An A/D converter configured to convert both positive and negative analogue input voltages is said to be operating in bipolar mode.

12.10.3 Coding

Coding defines the nature of the A/D converter output data format. Commonly used formats include straight binary, offset binary, complementary binary, 2's complement, low byte and high byte.

12.10.4 Low Byte and High Byte

In A/D converters with a resolution greater than eight bits, some products are offered in high-byte or low-byte format to simplify their interface with eight-bit microprocessor systems. The low-byte output contains the least significant bit and some or all of the lower eight bits of the A/D converter output. In the high byte, the output contains the MSB and some or all of the upper eight bits.

12.10.5 Right-Justified Data, Left-Justified Data

Data bit sets shorter than eight bits are placed in byte-oriented data output format, starting with the right side of the data output transfer register. This could apply to the upper or lower byte. For example, a 12-bit ADC will have four extra bits which could be right justified. Data bit sets shorter than eight bits are placed in left-justified data, starting with the left side of the data output transfer register. This could apply to the lower or upper byte. For example, a 12-bit ADC will have four extra bits which could be left justified.

12.10.6 Command Register, Status Register

The command register is an internal register of the ADC that can be programmed by the user to select various modes of operation such as unipolar or bipolar mode selection, range selection, data output format selection, etc. The status register indicates the current status of the analogue-to-digital conversion with a 'busy' or 'conversion complete' signal.

12.10.7 Control Lines

Digital input/output pins that activate/monitor and control ADC operation are called control lines. Some examples are chip select, write, start convert, conversion complete, etc.

Example 12.5

Determine the resolution of a 12-bit A/D converter having a full-scale analogue input voltage of 5 V.

Solution
- A 12-bit A/D converter resolves the analogue input voltage into $(2^{12} - 1)$ levels.
- The resolution $= 5/(2^{12} - 1) = 5000/(4096 - 1) = (5000/4095) = 1.22mV$.

Example 12.6

The data sheet of a certain eight-bit A/D converter lists the following specifications: resolution eight bits; full-scale error 0.02 % of full scale; full-scale analogue input +5 V. Determine (a) the quantization error (in volts) and (b) the total possible error (in volts).

Solution
(a) The eight-bit A/D converter has $2^8 - 1 = 255$ steps. Therefore, the quantization error $= 5/255 = 5000/255 = 19.607$ mV.
(b) The full-scale error $= 0.02\% \, of \, fullscale = 0.02 \times 5000/100 = 1$ mV. Therefore, the total possible error $= 19.607 + 1 = 20.607mV$.

12.11 Types of A/D Converter

Analogue-to-digital converters are often classified according to the conversion process or the conversion technique used to digitize the signal. Based on various conversion methodologies, common types of A/D converter include flash or simultaneous or direct-conversion A/D converters, half-flash A/D converters, counter-type A/D converters, tracking A/D converters, successive approximation type A/D converters, single-slope, dual-slope and multislope A/D converters and sigma-delta A/D converters.

Each of the above-mentioned types of A/D converter is described in the following paragraphs.

12.11.1 Simultaneous or Flash A/D Converters

The simultaneous method of A/D conversion is based on using a number of comparators. The number of comparators needed for n-bit A/D conversion is $2^n - 1$. One such system capable of converting an
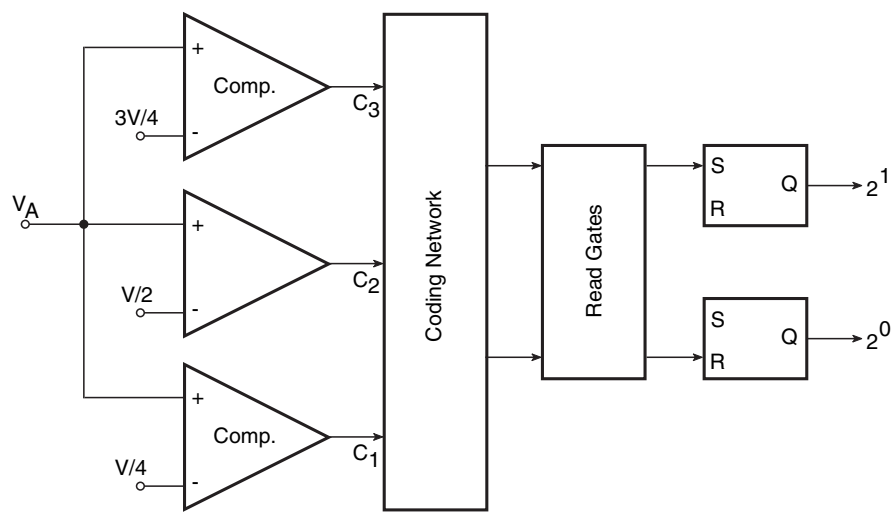
Figure 12.29 Two-bit simultaneous A/D converter.

analogue input signal into a two-bit digital output is shown in Fig. 12.29. The analogue signal to be digitized serves as one of the inputs to each of the comparators. The second input for each of the comparators is a reference input, different for each comparator. The reference voltages to be used for comparators are in general $V/2^n$, $2V/2^n$, $3V/2^n$, $4V/2^n$ and so on. Here, V is the maximum amplitude of the analogue signal that the A/D converter can digitize, and n is the number of bits in the digitized output. In the present case of a two-bit A/D converter, the reference voltages for the three comparators will be $V/4$, $V/2$ and $3V/4$. If we wanted a three-bit output, the reference voltages would have been $V/8$, $V/4$, $3V/8$, $V/2$, $5V/8$, $3V/4$ and $7V/8$. Referring to Fig. 12.29, the output status of various comparators depends upon the input analogue signal V_A. For instance, when the input V_A lies between $V/4$ and $V/2$, the C_1 output is HIGH whereas the C_2 and C_3 outputs are both LOW. The results are summarized in Table 12.1. The three comparator outputs can then be fed to a coding network (comprising logic gates, etc.) to provide two bits that are the digital equivalent of the input analogue voltage. The bits at the output of the coding network can then be entered into a flip-flop register for storage. Figure 12.30 shows the arrangement of a three-bit simultaneous-type A/D converter.

The construction of a simultaneous A/D converter is quite straightforward and relatively easy to understand. However, as the number of bits in the desired digital signal increases, the number of

Table 12.1 Simultaneous or Flash A/D converters.

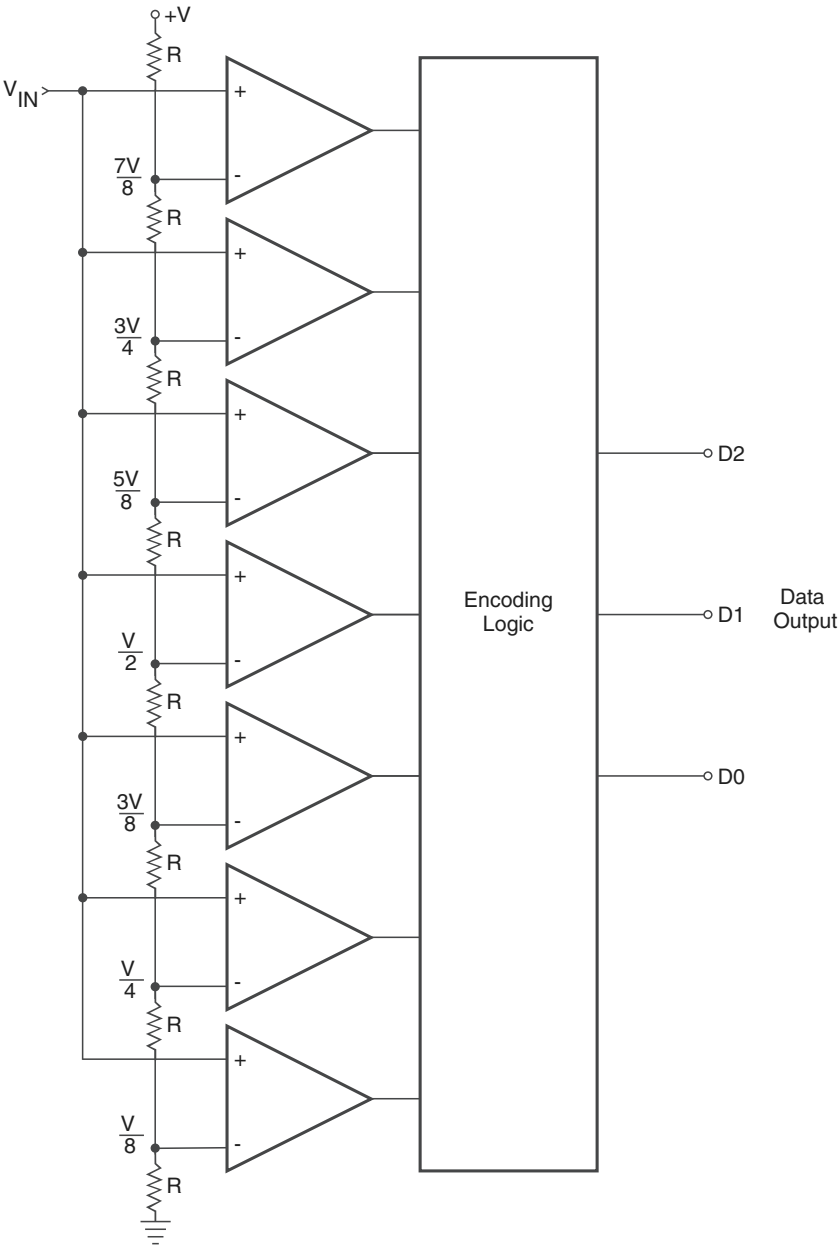| Input analogue voltage(v_a)	C_1	C_2	C_3	2^1	2^2
0 to $V/4$	LOW	LOW	LOW	0	0
$V/4$ to $V/2$	HIGH	LOW	LOW	0	1
$V/2$ to $3V/4$	HIGH	HIGH	LOW	1	0
$3V/4$ to V	HIGH	HIGH	HIGH	1	1

Figure 12.30   Three-bit simultaneous A/D converter.

comparators required to perform A/D conversion increases very rapidly, and it may not be feasible to use this approach once the number of bits exceeds six or so. The greatest advantage of this technique lies in its capability to execute extremely fast analogue-to-digital conversion.

12.11.2 Half-Flash A/D Converter

The *half-flash A/D converter*, also known as the *pipeline A/D converter*, is a variant of the flash-type converter that largely overcomes the primary disadvantage of the high-resolution full-flash converter, namely the prohibitively large number of comparators required, without significantly degrading its high-speed conversion performance. Compared with a full-flash converter of certain resolution, while the number of comparators and associated resistors is drastically reduced in a half-flash converter, the conversion time increases approximately by a factor of 2. For an *n*-bit flash converter the number of comparators required is $2^n [(2^n - 1)$ for encoding of amplitude and one comparator for polarity], while the same for an equivalent half-flash converter would be $2 \times 2^{n/2}$. In the case of an eight-bit converter, the number is 32 (for half-flash) against 256 (for full flash). How it is achieved is explained in the following paragraphs considering the example of an eight-bit half-flash converter.

A half-flash converter uses two full-flash converters, with each full-flash converter having a resolution equal to half the number of bits of the half-flash converter. That is, an eight-bit half-flash converter uses two four-bit flash converters. In addition, it uses a four-bit D/A converter and an eight-bit latch. Figure 12.31 shows the basic architecture of such a converter. The timing and control circuitry is omitted for the sake of simplicity. The circuit functions as follows.

The most significant four-bit A/D converter converts the input analogue signal into a corresponding four-bit digital code, which is stored in the most significant four bits of the output latch. This four-bit digital code, however, represents the low-resolution sample of the input. Simultaneously, it is converted back into an equivalent analogue signal with a four-bit D/A converter. The approximate value of the analogue signal so produced is then subtracted from the sampled value and the difference is converted
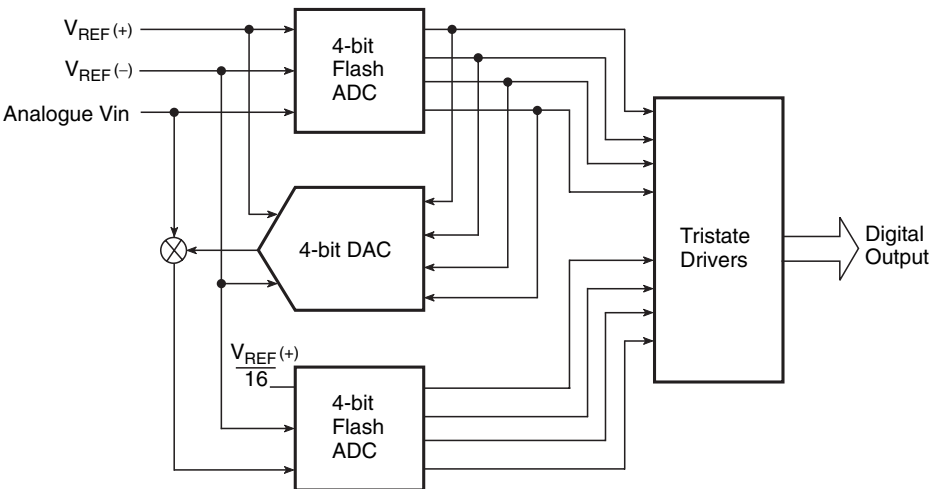

Figure 12.31   Eight-bit half-flash A/D converter.

into digital code using a least significant four-bit A/D converter. The least significant A/D converter is referenced to one-sixteenth ($= 1/2^4$) of the reference voltage used by the most significant A/D converter. The new four-bit digital output is stored in the least significant four bits of the output latch. The latch now contains the eight-bit digital equivalent of the analogue input. The digitized output is the same as would be produced by an eight-bit full-flash converter. The only difference is that the conversion process takes a little longer. It may also be mentioned here that the eight-bit half-flash converter can be used either as a four-bit full-flash converter or as an eight-bit half-flash converter. Some half-flash converters use a single full-flash converter and reuse it for both conversions. This is achieved by using additional sample-and-hold circuitry.

12.11.3 Counter-Type A/D Converter

It is possible to construct higher-resolution A/D converters with a single comparator by using a variable reference voltage. One such A/D converter is the *counter-type A/D converter* represented by the block schematic of Fig. 12.32. The circuit functions as follows. To begin with, the counter is reset to all 0s. When a convert signal appears on the start line, the input gate is enabled and the clock pulses are applied to the clock input of the counter. The counter advances through its normal binary count sequence. The counter output feeds a D/A converter and the staircase waveform generated at the output of the D/A converter forms one of the inputs of the comparator. The other input to the comparator is the analogue input signal. Whenever the D/A converter output exceeds the analogue input voltage, the comparator changes state. The gate is disabled and the counter stops. The counter output at that instant of time is then the required digital output corresponding to the analogue input signal.

The counter-type A/D converter provides a very good method for digitizing to a high resolution. This method is much simpler than the simultaneous method for higher-resolution A/D converters. The drawback with this converter is that the required conversion time is longer. Since the counter always begins from the all 0s position and counts through its normal binary sequence, it may require as many as 2^n counts before conversion is complete. The average conversion time can be taken to be $2^n/2 = 2^{n-1}$ counts. One clock cycle gives one count. As an illustration, if we have a four-bit converter and a 1 MHz clock, the average conversion time would be 8 ms. It would be as large as 0.5 ms for a 10-bit converter of this type at a 1 MHz clock rate. In fact, the conversion time doubles for each bit
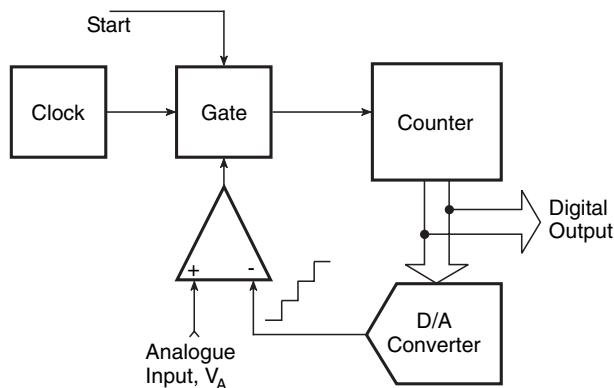

Figure 12.32 Counter-type A/D converter.

added to the converter. Thus, the resolution can be improved only at the cost of a longer conversion time. This makes the counter-type A/D converter unsuitable for digitizing rapidly changing analogue signals.

12.11.4 Tracking-Type A/D Converter

In the counter-type A/D converter described above, the counter is reset to zero at the start of each new conversion. The D/A converter output staircase waveform always begins at zero and increases in steps until it reaches a point where the analogue output of the D/A converter exceeds the analogue input to be digitized. As a result, the counter-type A/D converter of the type discussed above is slow. The *tracking-type A/D converter*, also called the *delta-encoded A/D converter*, is a modified form of counter-type converter that to some extent overcomes the shortcoming of the latter. In the modified arrangement, the counter, which is primarily an UP counter, is replaced with an UP/DOWN counter. It counts in upward sequence whenever the D/A converter output analogue voltage is less than the analogue input voltage to be digitized, and it counts in the downward sequence whenever the D/A converter output analogue voltage is greater than the analogue input voltage. In this type of converter, whenever a new conversion is to begin, the counter is not reset to zero; in fact it begins counting either up or down from its last value, depending upon the comparator output. The D/A converter output staircase waveform contains both positive-going and negative-going staircase signals that track the input analogue signal.

12.11.5 Successive Approximation Type A/D Converter

The development of A/D converters has progressed in a quest to reduce the conversion time. The successive approximation type A/D converter aims at approximating the analogue signal to be digitized by trying only one bit at a time. The process of A/D conversion by this technique can be illustrated with the help of an example. Let us take a four-bit successive approximation type A/D converter. Initially, the counter is reset to all 0s. The conversion process begins with the MSB being set by the start pulse. That is, the flip-flop representing the MSB is set. The counter output is converted into an equivalent analogue signal and then compared with the analogue signal to be digitized. A decision is then taken as to whether the MSB is to be left in (i.e. the flip-flop representing the MSB is to remain set) or whether it is to be taken out (i.e. the flip-flop is to be reset) when the first clock pulse sets the second MSB. Once the second MSB is set, again a comparison is made and a decision taken as to whether or not the second MSB is to remain set when the subsequent clock pulse sets the third MSB. The process continues until we go down to the LSB. Note that, every time we make a comparison, we tend to narrow down the difference between the analogue signal to be digitized and the analogue signal representing the counter count. Refer to the operational diagram of Fig. 12.33. It is clear from the diagram that, to reach any count from 0000 to 1111, the converter requires four clock cycles. In general, the number of clock cycles required for each conversion will be *n* for an *n*-bit A/D converter of this type.

Figure 12.34 shows a block schematic representation of a successive approximation type A/D converter. Since only one flip-flop (in the counter) is operated upon at one time, a ring counter, which is nothing but a circulating register (a serial shift register with the outputs Q and $\overline{Q}$ of the last flip-flop connected to the J and K inputs respectively of the first flip-flop), is used to do the job. Referring to Fig. 12.33, the dark lines show the sequence in which the counter arrives at the desired count, assuming that 1001 is the desired count. This type of A/D converter is much faster than the counter-type A/D converter previously discussed. In an *n*-bit converter, the counter-type A/D converter on average would
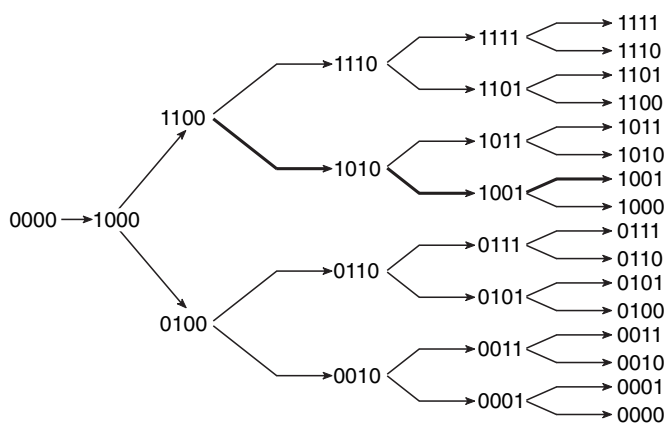
Figure 12.33   Conversion process in a successive approximation type A/D converter.
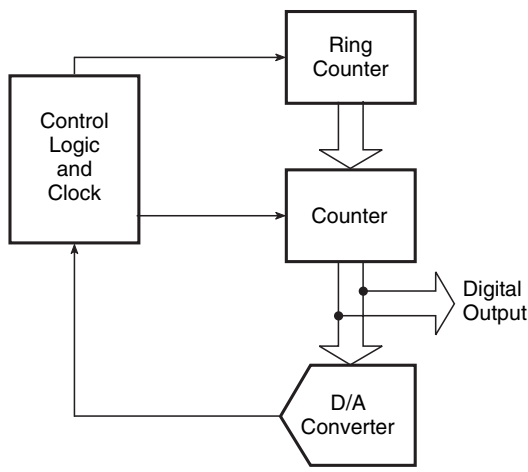

Figure 12.34   Block schematic representation of a successive-approximation A/D converter.

require 2^{n-1} clock cycles for each conversion, whereas a successive approximation type converter requires only n clock cycles. That is, an eight-bit A/D converter of this type operating on a 1 MHz clock has a conversion time of 8 μs.

12.11.6 Single-, Dual- and Multislope A/D Converters

Figure 12.35 shows a block schematic representation of a *single-slope A/D converter*. In this type of converter, one of the inputs to the comparator is a ramp of fixed slope, while the other input is the analogue input to be digitized. The counter and the ramp generator are initially reset to 0s. The
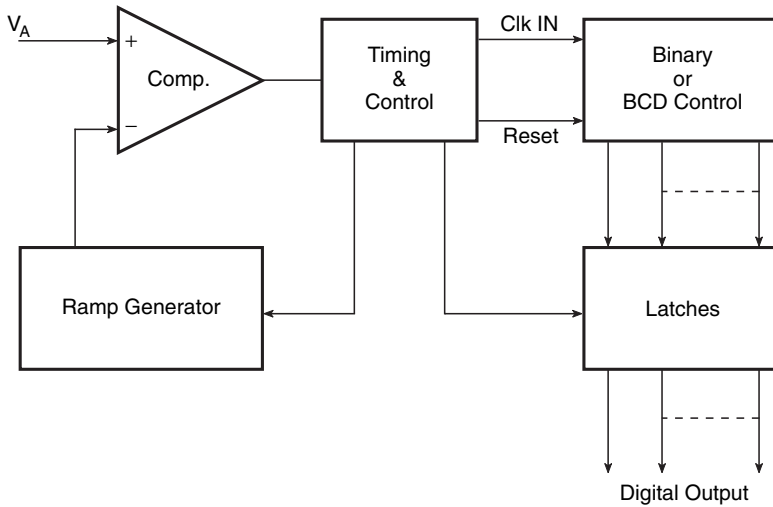
Figure 12.35   Block schematic representation of a single-slope A/D converter.

counter starts counting with the first clock cycle input. The ramp is also synchronized to start with the first clock input. The counter stops when the ramp amplitude equals the analogue input. In this case, the counter count is directly proportional to the analogue signal. It is a low-cost, reasonably high-accuracy converter but it suffers from the disadvantage of loss of accuracy owing to changes in the characteristics of the ramp generator. This shortcoming is overcome in a dual-slope integrating-type A/D converter.

Figure 12.36 shows a block schematic arrangement of a *dual-slope integrating A/D converter*. The converter works as follows. Initially, switch S is connected to the analogue input voltage V_A to be digitized. The output of the integrator is mathematically given by

$$v_o = (-1/RC) \int V_A . dt = (-V_A/RC).t \qquad (12.17)$$

The moment v_o tends to go below zero, clock pulses reach the clock input terminal of the counter which is initially cleared to all 0s. The counter begins counting from $0000 \ldots 0$. At the (2^n)th clock pulse, the counter is again cleared, the '1' to '0' transition of the MSB of the counter sets a flip-flop that controls the state of switch S which now connects the integrator input to a reference voltage of polarity opposite to that of the analogue input. The integrator output moves in the positive direction; the counter has again started counting after being reset (at, say, $t = T_1$). The moment the integrator output tends to exceed zero, the counter stops as the clock pulses no longer reach the clock input of the counter. The counter output at this stage (say, at $t = T_2$) is proportional to the analogue input. Mathematically, it can be proved that $n = (V_A/V_R).2^n$, where n is the count recorded in the counter at $t = T_2$. Figure 12.37 illustrates the concept further with the help of relevant waveforms. This type of A/D converter is very popular in digital voltmeters owing to its good conversion accuracy and low cost. Also, the accuracy is independent of both the integrator capacitance and the clock frequency, as they affect the negative and positive slope in the same manner. Yet another advantage of the dual-slope integrator A/D converter is that the fixed analogue input integration period results in rejection of noise frequencies present
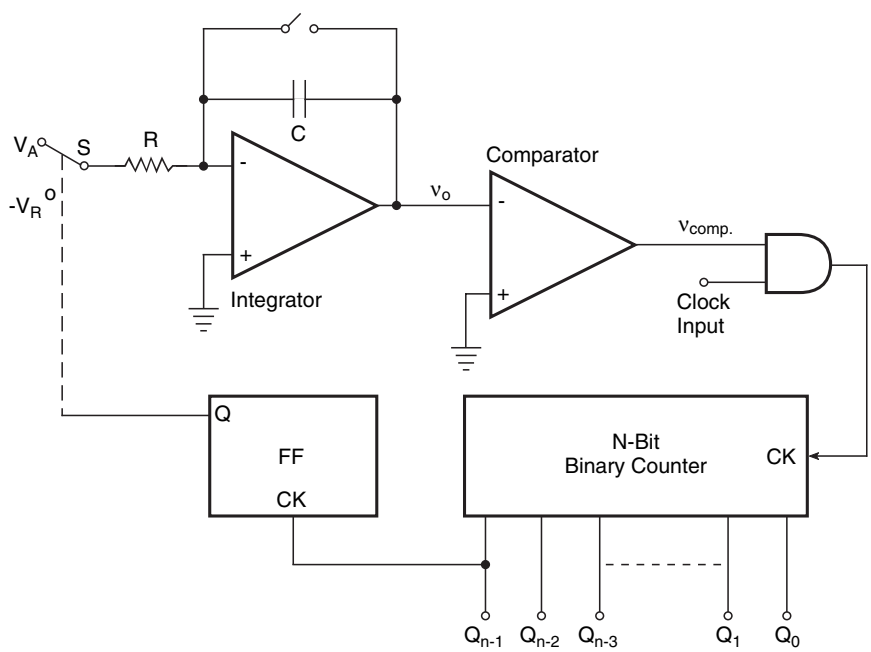
Figure 12.36   Block schematic representation of a dual-slope A/D converter.
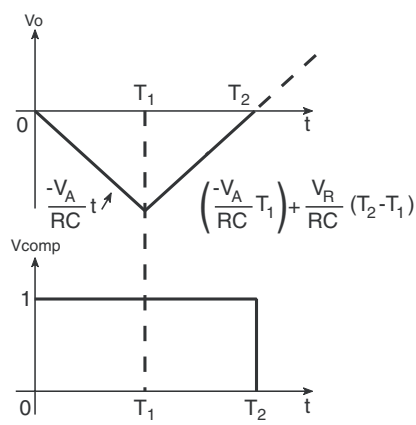

Figure 12.37   Relevant waveforms in a dual-slope A/D converter.

in the analogue input and having time periods that are equal to or submultiples of the integration time. The proper choice of integration time can therefore achieve excellent rejection of 50/60 Hz line ripple.

There are also multislope converter architectures that are aimed at further enhancing the performance of integrating A/D converters. For example, the *triple-slope architecture* is used to increase the

conversion speed at the cost of added complexity. Increase in conversion speed is accomplished by carrying out integration from reference voltage at two distinct rates, a high-speed rate and a low-speed rate. The counter is also divided into two sections, one for MSB bits and the other for LSB bits. A properly designed triple-slope converter achieves increased conversion speed without compromising the inherent linearity, differential linearity and stability characteristics of the dual-slope converter.

Bias currents, offset voltages and gain errors associated with operational amplifiers used as integrators and comparators do introduce some errors. These can be cancelled by using additional charge/discharge cycles and then using the results to correct the initial measurement. One such A/D converter is the *quad-slope converter* which uses two charge/discharge cycles as compared with one charge/discharge cycle in the case of the dual-slope converter. Quad-slope A/D converters have a much higher accuracy than their dual-slope counterparts.

12.11.7 Sigma-Delta A/D Converter

The sigma-delta A/D converter employs a different concept from what has been discussed so far for the case of various types of A/D converter. While the A/D converters covered so far rely on sampling of the analogue signal at the Nyquist frequency and encode the absolute value of the sample, in the case of a sigma-delta converter, as explained in the following paragraphs, the analogue signal is oversampled by a large factor (i.e. the sampling frequency is much larger than the Nyquist value), and also it is not the absolute value of the sample but the difference between the analogue values of two successive samples that is encoded by the converter.

In the case of the A/D converters discussed prior to this and sampled at the Nyquist rate f_s, the RMS value of the quantization noise is uniformly distributed over the Nyquist band of DC to $f_s/2$, as shown in Fig. 12.38(a). The signal-to-noise ratio for a full-scale sine wave input in this case is given by S/N $= (6.02n + 1.76)$ dB, n being the number of bits. The only way to increase the signal-to-noise ratio is by increasing the number of bits. On the other hand, a sigma-delta converter attempts to enhance the signal-to-noise ratio by oversampling the analogue signal, which has the effect of spreading the noise spectrum over a much larger bandwidth and then filtering out the desired band. If the analogue signal were sampled at a rate of Kf_s, the quantization noise would be spread over DC to $Kf_s/2$, as shown in Fig. 12.38(b). K is a constant referred to as the oversampling ratio. The enhanced S/N ratio means higher resolution, which is achieved by other types of A/D converter by way of increasing the number of bits.

It may be mentioned here that, if we simply use oversampling to improve the resolution, it would be required to oversample by a factor of 2^{2N} to achieve an N-bit increase in resolution. The sigma-delta converter does not require to be oversampled by such a large factor because it not only limits the signal pass band but also shapes the quantization noise in such a way that most of it falls outside this pass band, as shown in Fig. 12.38(c). The following paragraphs explain the operational principle of the sigma-delta A/D converter.

The heart of the sigma-delta converter is the delta modulator. Figure 12.39 shows a block schematic representation of a delta modulator, which is basically a one-bit quantizer of the flash type (single comparator). The output of the delta modulator is a bit stream of 1s and 0s, with the number of 1s relative to the number of 0s over a given number of clock cycles indicating the amplitude of the analogue signal over that time interval. An all 1s sequence over a given interval corresponds to the maximum positive amplitude, and an all 0s sequence indicates the maximum negative amplitude. An equal number of 1s and 0s indicates a zero amplitude. Other values between the positive and negative maxima are indicated by a proportional number of 1s relative to the number of 0s. This is further illustrated in Fig. 12.40.
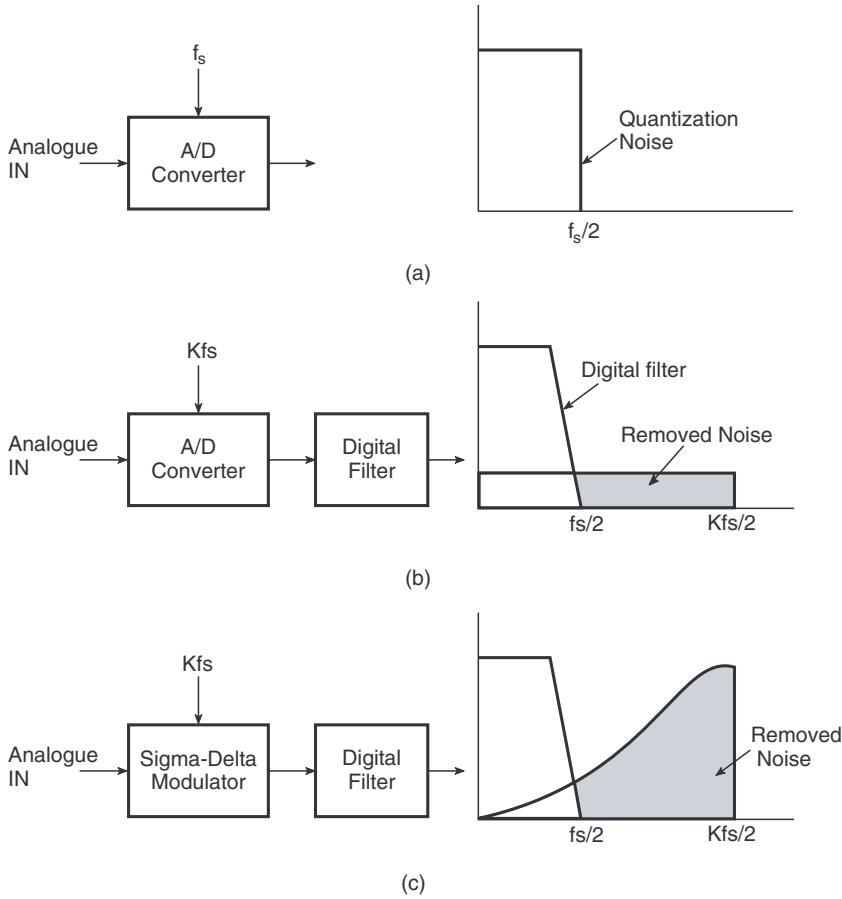
Figure 12.38   (a) Quantization noise spectrum with sampling at the Nyquist rate, (b) the quantization noise spectrum with oversampling and (c) the quantization noise spectrum with oversampling in a sigma-delta converter.

Coming back to the delta modulator (Fig. 12.39), the input to the one-bit quantizer, which is basically a comparator, is from the output of an integrator. The integrator in turn is fed from the difference between the analogue input signal and the analogue equivalent of the quantized output produced by a one-bit D/A converter. A one-bit D/A converter is nothing but a two-way switch that feeds either $+V_{ref}$ or $-V_{ref}$ to the summing point, depending upon the bit status at its input. The negative feedback loop ensures that the average value of the D/A converter output nearly equals the analogue input so as to produce a near-zero input to the integrator.

An increase in analogue signal amplitude produces a larger number of 1s at the quantizer output and consequently a higher average value of the analogue signal at the D/A converter output. This means that the number of 1s in the quantizer output bit stream over a given time interval represents the analogue signal amplitude. The single-bit data stream can then be encoded into the desired output format. One simple way to do this could be to use a counter to count the number of 1s in the data stream over fixed
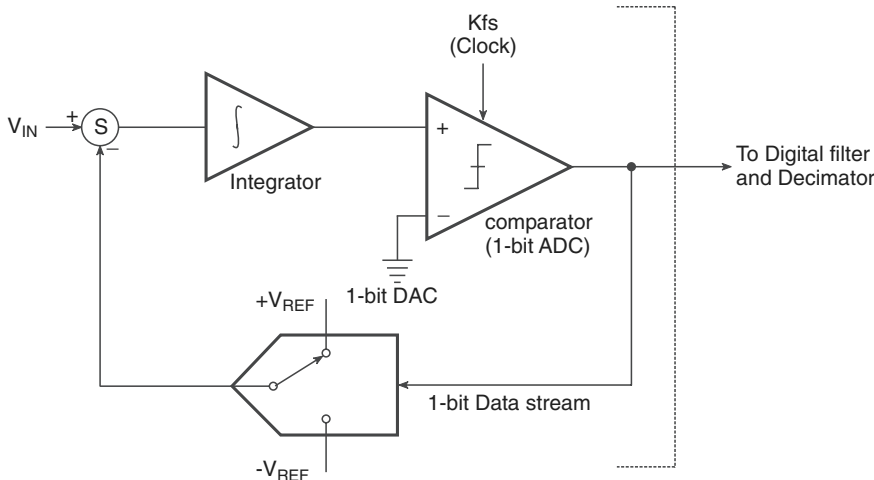
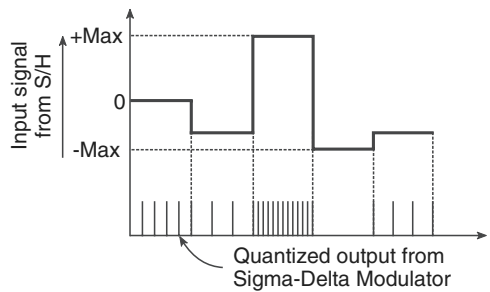**Figure 12.39**   Block schematic representation of a delta modulator.

Figure 12.40   Generation of a one-bit data stream.

intervals of time, in which case the counter output would represent the digital equivalent of the analogue signal over those time intervals. Practical sigma-delta A/D converters use a digital decimation filter at the output of the delta modulator to process the one-bit data stream to produce an output in the desired format.

Sigma-delta A/D converters are widely used for contemporary voice-band, audio and high-resolution precision industrial measurement applications. Their highly digital architecture is ideally suited for such applications as it allows easy addition of digital functionality without significantly increasing the cost. AD 1871 from Analog Devices is one such high-performance A/D converter of sigma-delta architecture intended for digital audio applications.

Example 12.7

Determine the conversion time of a 12-bit A/D converter of the counter type shown earlier in Fig. 12.32 for an input clock frequency of 1 MHz.

Solution
- The counter-type A/D converter shown in Fig. 12.32 has a variable conversion time that is maximum when the input analogue voltage is just below the full-scale analogue input voltage.
- An average conversion time equal to half the maximum conversion time is usually defined in the case of such converters.
- The maximum conversion time equals the time taken by $2^{12} - 1 = 4095$ cycles of clock input.
- The clock time period $= 1/(1 \times 10^6) = 1 \mu s$.
- Therefore, the maximum conversion time $= 4095 \times 1 = 4095 \mu s = 4.095$ ms.
- The average conversion time $= (4.095/2) = 2.047$ ms.

Example 12.8

The D/A converter of a counter-type A/D converter (refer to Fig. 12.32) produces a staircase output having a step size of 10 mV. The A/D converter has a 10-bit resolution and is specified to have a quantization error of $\pm 1/2$ LSB. Determine the digital output for an analogue input of 4.012 V. Assume that the comparator has a comparison threshold of 1 mV.

Solution
- The comparator has a comparison threshold of 1 mV.
- With reference to Fig. 12.32, this implies that, for the comparator to change state, the voltage at the relevant input should be 1 mV more than the voltage at the other input.
- Now, one of the inputs to the comparator is the analogue input voltage ($= 4.012$ V in the present case).
- The other input to the comparator is a voltage that is equal to the sum of the D/A converter output voltage and a fixed voltage corresponding to 1/2 LSB.
- This is the case when the quantization error of the A/D converter is specified to be $\pm 1/2$ LSB.
- In the case of a quantization error of one LSB, the D/A converter directly feeds the other input of the comparator.
- In the present case, one LSB corresponds to 10 mV.
- Therefore, 1/2 LSB corresponds to 5 mV.
- For an analogue input of 4.012 V, the voltage at the other input needs to be 4.013 V (owing to the comparator threshold of 1 mV).
- This implies that the D/A converter output needs to be 4.008 V.
- Therefore, the number of steps $= 4.008/(10 \times 10^{-3}) = 400.8 = 401$.
- The digital output is the binary equivalent of $(401)_{10}$, which equals 0110010001.

Example 12.9

A 10-bit A/D converter of the successive approximation type has a resolution (or quantization error) of 10 mV. Determine the digital output for an analogue input of 4.365 V.

Solution

- In the case of a successive approximation type A/D converter, the final analogue output of its D/A converter portion always settles at a value below the analogue input voltage to be digitized within the resolution of the converter.
- The analogue input voltage = 4.365 V.
- The resolution = 10 mV.
- The number of steps $= 4.365/(10 \times 10^{-3}) = 436.5$.
- Step number 436 will produce a D/A converter output of $436 \times 10 = 4360$mV $= 4.36$V, and step number 437 will produce a D/Aconverter of 4.37 V.
- The A/D converter will settle at step 436.
- The digital output will be the binary equivalent of$(436)_{10}$ which is 0110110100.

Note. When this converter actually performs the conversion, in the tenth clock cycle, the LSB will be set to '1' initially. This would produce a D/A converter output of 4.37 V which exceeds the analogue input voltage of 4.365 V. The comparator changes state, which in turn resets the LSB to '0', bringing the D/A converter output to 4.36 V. This is how a converter of this type settles where a D/A converter output settles at a value that is one step below the value that makes it exceed the analogue input to be digitized.

Example 12.10

Compare the average conversion time of an eight-bit counter-type A/D converter with that of an eight-bit successive approximation type A/D converter if both are working at a 10 MHz clock frequency.

Solution

- The clock time period = 0.1 μs.
- The average conversion time in the case of a counter-type A/D converter is given by $[(2^8 - 1)/2] \times 0.1 = 12.75 \mu s$.
- The conversion time in the case of a successive approximation type A/D converter is given by $8 \times 0.1 = 0.8$ μs.

12.12 Integrated Circuit A/D Converters

This section presents application-relevant information of some of the popular A/D converter IC type numbers, as it is not possible to give a detailed description of each one of them. The type numbers included for this purpose are ADC 0800, ADC 0808, ADC 80, ADC 84, ICL 7106/ICL 7107 and AD 7820.

12.12.1 ADC-0800

ADC-0800 is a successive approximation type eight-bit A/D converter. The internal architecture of ADC-0800 is shown in Fig. 12.41. The digital output is in complementary form and is also tristate to permit bussing on common data lines. Its salient features include ratiometric conversion, no missing codes, tristate outputs and a conversion time of 50 μs (typical), ±1-LSB linearity and a clock frequency range of 50–800 kHz.
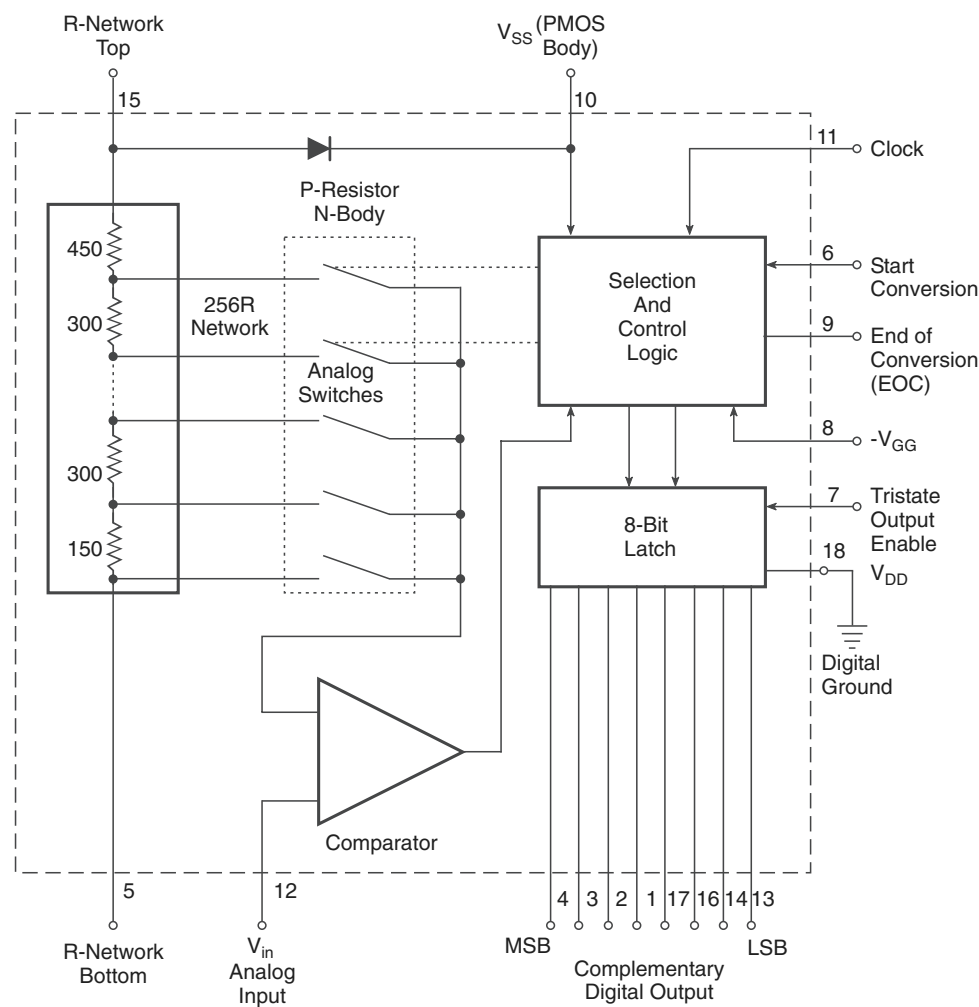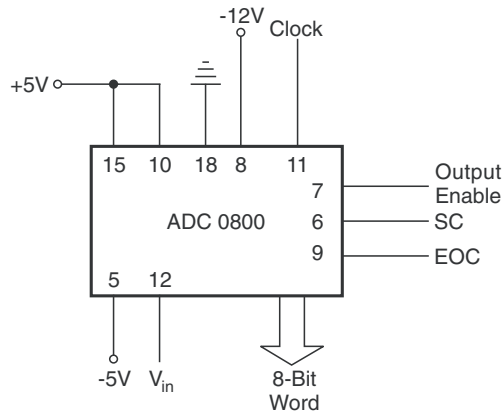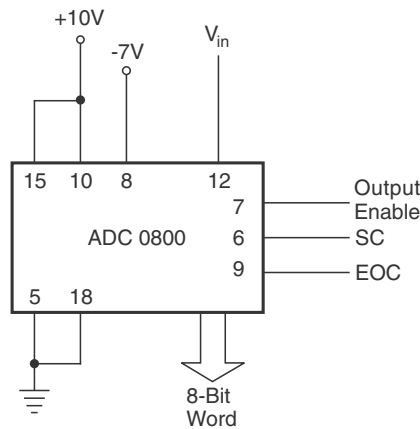
Figure 12.41   Internal architecture of AD 0800.

Figures 12.42(a) and (b) show application circuits using AD-0800. Figure 12.42(a) shows typical circuit connections for a ±5 V input voltage range and TTL-compatible output levels, whereas Fig. 12.42(b) shows the connections for a 0–10 V input range and 0–10 V output levels.

12.12.2 ADC-0808

ADC 0808 is an eight-bit CMOS successive approximation type A/D converter. The device has an eight-channel multiplexer and a microprocessor-compatible control logic. Salient features of the device include eight-bit resolution, no missing codes, a conversion time of 100 μs (typical),

Figure 12.42   Basic application circuits using AD 0800.

stand-alone operation or easy interface to all microprocessors, a 0–5 V analogue input range with a single 5 V supply and latched tristate outputs. Figure 12.43 shows the internal architecture of the device.

12.12.3 ADC-80/AD ADC-80

ADC-80/AD ADC-80 is a 12-bit A/D converter of the successive approximation type. It has an on-chip clock generator, reference and comparator. AD ADC80 is pin-to-pin compatible with industry-standard ADC-80. Figure 12.44 shows the internal block schematic/pin connections of AD-ADC-80. The salient features of the device include low cost, $\pm 0.012\%$ linearity, a conversion time of 25 μs (max.),
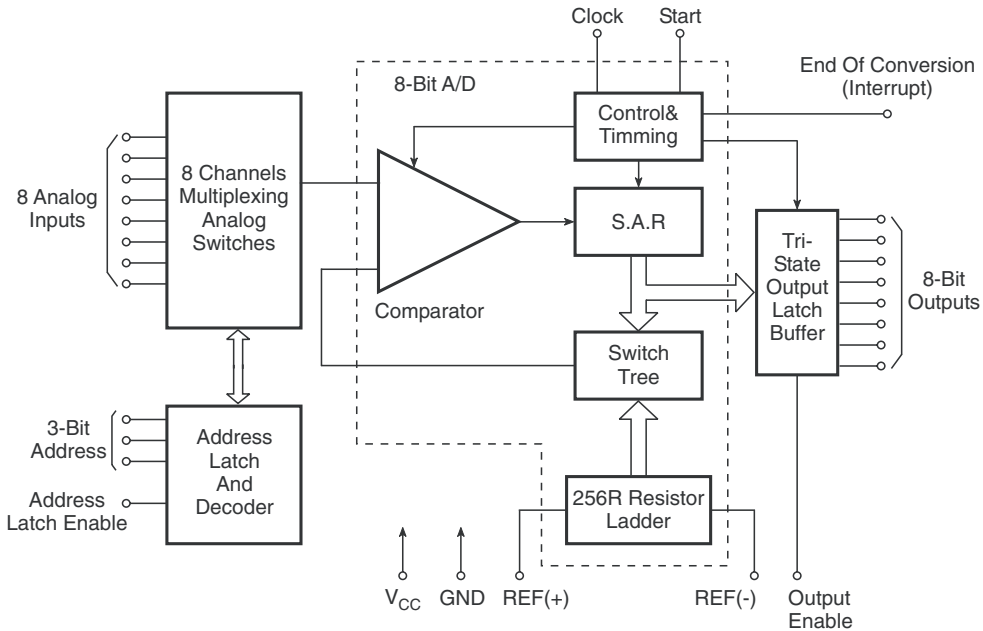
Figure 12.43   Internal architecture of AD 0808.

$\pm\,12$ V or $\pm\,15$ V operation, guaranteed no missing codes over a temperature range from $-25\ ^\circ$C to $+85\ ^\circ$C and a maximum power dissipation of 595 mW.

12.12.4 ADC-84/ADC-85/AD ADC-84/AD ADC-85/AD-5240

ADC-84 and ADC-85 families of 10-bit (ADC 84-10 and ADC 85-10) and 12-bit (ADC 84-12 and ADC 85-12) converters are complete A/D converters like the industry-standard ADC-80, with an internal clock (1.9 MHz in the case of the 10-bit converters and 1.35 MHz in the case of the 12-bit converters), comparator, reference (6.3 V) and input buffer amplifier. These have a conversion time of 10 μs (for 12-bit operation) and 6 μs (for 10-bit operation). Figure 12.45 shows an internal block schematic/pin connection diagram of ADC-84/ADC-85/AD-5240.

12.12.5 AD 7820

AD 7820 is a μP-compatible, eight-bit A/D converter built around half-flash architecture. It incorporates internal sample-and-hold circuitry, which eliminates the need for an external sample-and-hold circuit for signals having slew rates of less than 100 mV/μs. Figure 12.46 shows the internal architecture/pin connection diagram of AD 7820. Other features include a 1.36 μs conversion time, a single +5 V supply and tristate buffered outputs.
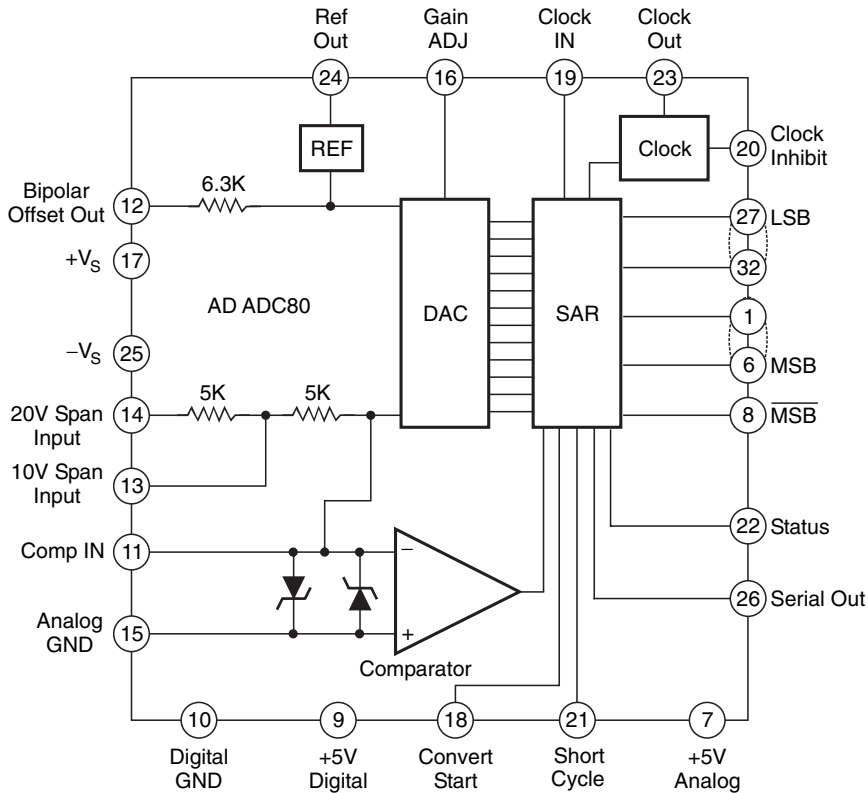
Figure 12.44   Internal architecture/pin connection diagram of AD ADC 80.

12.12.6 ICL 7106/ICL 7107

ICL 7106 and ICL 7107 are the most commonly used A/D converter ICs for digital panel meter (DPM) and digital voltmeter (DVM) applications, with the former used with LCD and the latter used with LED displays. The two types are high-performance, low-power A/D converter ICs of the dual-slope integrating type from Intersil, containing all the necessary building blocks such as a clock generator, a reference, seven segment decoders, display drivers, etc., for directly driving seven segment displays. Figure 12.47 shows the pin connection diagram of ICL 7106/7107 in a dual in-line package. Notice that pin-21 in the case of ICL 7106 is the back plane drive pin, whereas in the case of ICL 7107 it is the ground pin.

Salient features include low cost, low power consumption (typically less than 10 mW), low noise (less than 15 μV peak to peak), true polarity at zero for precise null detection, true differential input and reference, a rollover error of less than one count and so on. The reference voltage is set to be half the full-scale analogue input. For a maximum analogue input of more than what is acceptable at analogue input terminals (± 4 V for ± 5 V supplies), the input should be scaled down by a factor of 10. The scale-down factors are 100 and 1000 for $(20 < V_{in} \leq 200)$ V and $(200 < V_{in} \leq 2000)$ V respectively.

Figures 12.48 and 12.49 show the basic application circuits of ICL 7106 and ICL 7107 respectively. ICL 7106 operates from a single supply (9 V in the circuit shown), whereas ICL 7107 operates from
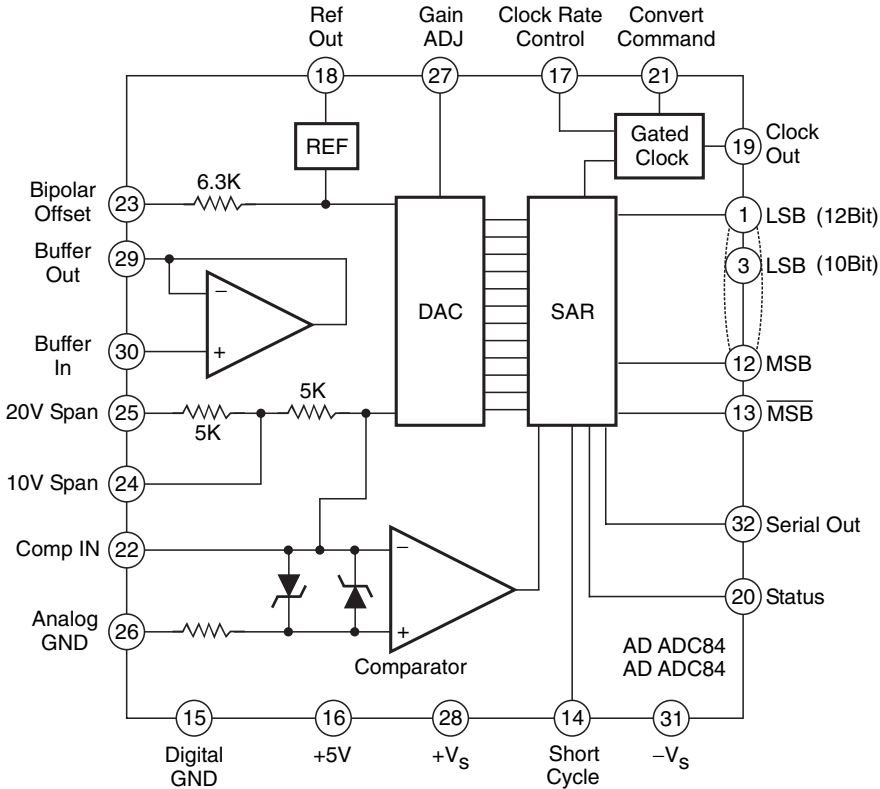
Figure 12.45   Internal architecture/pin connection diagram of AD ADC-84/ADC-85/AD-5240.

dual supplies of ±5 V. The following guidelines should be adhered to when selecting the values of the components for these circuits.

1. The integrating resistor R_1 should be large enough to remain in the linear region over the input voltage range but small enough for undue leakage current requirements not to be placed on the PC board. A value of 470 Ω is the optimum for a 2 V scale. For a 200 mV scale, 47 Ω should be used.

2. For a conversion rate of three readings per second (48 kHz clock), the nominal value of the integrating capacitor C_7 is 0.22 μF. A capacitor with low dielectric absorption should be used to prevent rollover errors. Polypropylene or polycarbonate capacitors should be preferred. If the oscillator frequency is different, C_7 should be changed in inverse proportion in order to maintain the same output swing.

3. Capacitor C_8, the auto zero capacitor, influences the noise of the system. For a 200 mV full scale, where the system noise is critical, a 0.47 μF capacitor is recommended for C_8. A smaller-value capacitor can be used on larger scales. For instance, 0.047 μF would do for a 2 V full scale. A smaller auto zero capacitor has the additional advantage of a faster recovery from overload condition.
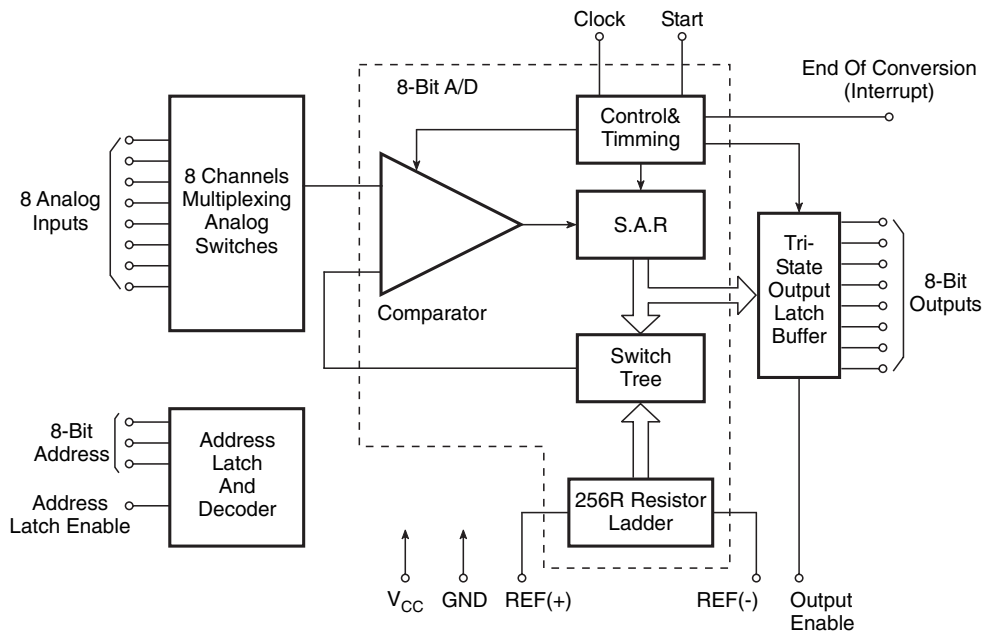
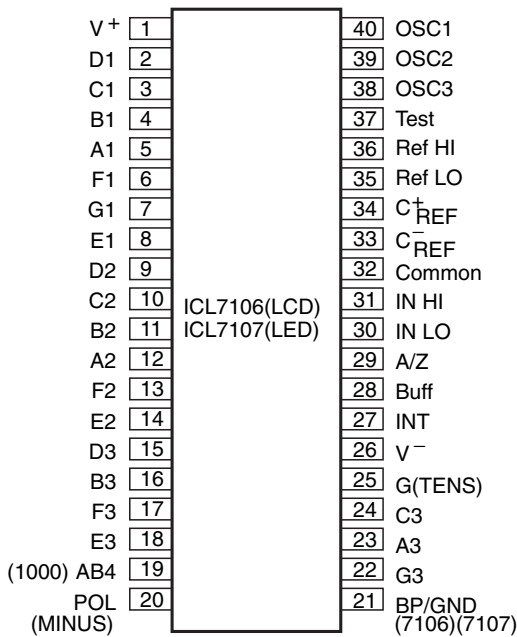**Figure 12.46**   Internal architecture/pin connection diagram of AD 7820.
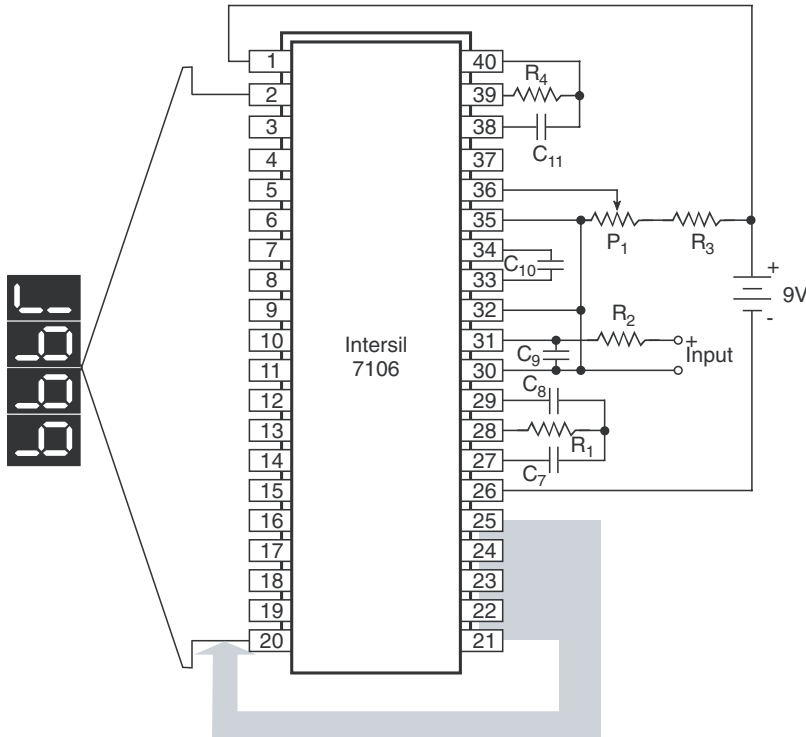

Figure 12.47   Pin connection diagram of ICL 7106/7107.

Figure 12.48 Application circuit using ICL 7106.

4. A 0.1 μF capacitor generally works well as the reference capacitor C_{10} connected between pins 33 and 34. However, if the REF/LO (pin 35) is not at analogue common (pin 30) and a 200 mV scale is being used, a larger value is generally required to prevent rollover error. A 1 μF capacitor will hold the rollover error in this case to 0.5 count.
5. The oscillator frequency is given by $f = [0.45/(R_4.C_{11})]$. R_4 is selected to be 100 Ω. C_{11} is computed from the equation for a known value of oscillator frequency. For $f = 48$ kHz (three readings per second), C_{11} turns out to be 100 pF.
6. The reference voltage V_{ref} is selected on the basis of the analogue input required to generate a full-scale output of 2000 counts and is $V_{in}/2$. It will be 100 mV for a 200 mV full scale and 1 V for a 2 V full scale.

12.13 A/D Converter Applications

Like D/A converters, A/D converters have numerous applications. A/D converters are used in virtually all those applications where the analogue signal is to be processed, stored or transported in digital form. They form an essential interface when it comes to analysing analogue data with a digital computer, the process being known as 'data acquisition'. They are an indispensable component of any digital communication system where the analogue signal to be transmitted is
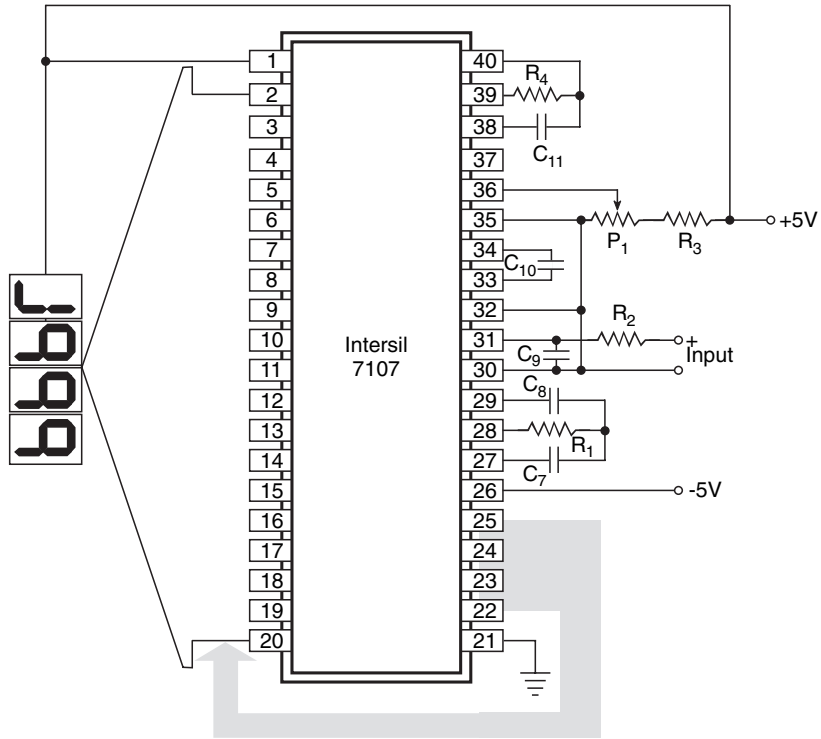
Figure 12.49   Application circuit using ICL 7107.

digitized at the sending end with an A/D converter. They are invariably used in all digital read-out test and measuring equipment such as digital multimeters (DMMs), digital storage oscilloscopes (DSOs), etc. Also, A/D converters are integral to contemporary music reproduction technology, as most of it is done on computers. In the case of analogue recording too, an A/D converter is needed to create the PCM data stream that goes onto a compact disc. While digital test and measurement instruments are discussed in detail in Chapter 16, the use of A/D converters for data acquisition, which forms the basis of most other applications, is discussed in the next section.

12.13.1 Data Acquisition

There are a large number of applications where an analogue signal is digitized to be subsequently stored or processed in a digital computer. The computer may store the data to be later passed on to a D/A converter to reconstruct the original signal, as in a digital-storage oscilloscope. It may process the digitized signal to generate the desired outputs in a process control application. Figure 12.50 shows the basic data acquisition building block. The computer generates a start-of-conversion signal. At the time instant of occurrence of the end-of-conversion signal generated by the A/D converter, the computer loads the digital output of the A/D converter onto its memory.
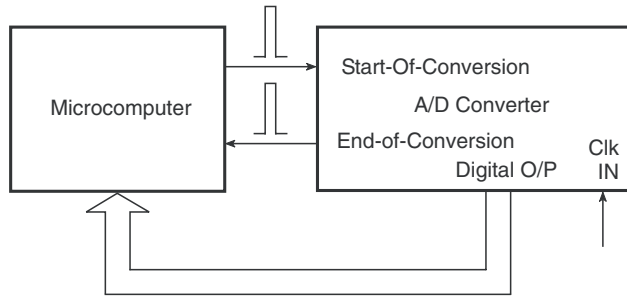
Figure 12.50   A/D converter for data acquisition.

Review Questions

1. Briefly describe the process of digital-to-analogue conversion in a binary ladder network. How does it differ from the simple resistive network used for the same purpose? Write an expression for the output analogue voltage for an *n*-bit binary ladder network.
2. Briefly describe the *resolution*, *accuracy*, *conversion time* and *monotonocity* specifications of a D/A converter.
3. Briefly describe the following with reference to D/A converters:

    (a) a multiplying-type D/A converter;
    (b) a companding-type D/A converter;
    (c) the current steering mode of operation;
    (d) the voltage switching mode of operation.

4. With reference to A/D converters, differentiate between:

    (a) resolution and accuracy;
    (b) nonlinearity (NL) and differential nonlinearity (DNL).

5. Briefly describe the principle of operation of a simultaneous or flash-type A/D converter. What are the merits and demerits of this type of converter? How does the architecture of a flash converter differ from that of a half-flash converter?
6. Describe with the help of a schematic diagram the operation of a tracking-type A/D converter. Explain how it overcomes the inherent disadvantage of a longer conversion time of the conventional counter-type A/D converter.
7. Describe with the help of a schematic diagram the principle of operation of a successive approximation type A/D converter. Explain the sequence of operation of conversion of an analogue signal to its digital equivalent when the expected digital output is 1010.
8. Explain the following:

    (a) why a tracking type A/D converter is particularly suitable for fast-changing analogue signals;
    (b) the use of a D/A converter as a programmable integrator;
    (c) why a dual-slope integrating-type A/D converter has a higher accuracy than a single-slope integrating-type A/D converter;
    (d) the use of a D/A converter as a digitally controlled voltage attenuator.

Problems

1. Determine the percentage resolution of (a) an eight-bit and (b) a 12-bit D/A converter.

(a) 0.39 %; (b) 0.024 %

2. An eight-bit D/A converter produces an analogue output of 12.5 mV for a digital input of 00000010. Determine the analogue output for a digital input of 00000100.

25 mV

3. A 12-bit D/A converter has a resolution of 2.44 mV. Determine its analogue output for a digital input of 111111111111.

10 V

4. How many bits should a current-output D/A converter have for its full-scale output to be 20 mA and its resolution to be better than 25 mA?

10 bits

5. Compare (a) the step size and (b) the percentage resolution of a D/A converter having an eight-bit binary input with those of a D/A converter having an eight-bit BCD input. Both have a full-scale output of 10 V.

Binary input: (a) 39.2 mV, (b) 0.39 %; BCD input: (a) 101 mV, (b) 1 %

6. Compare the average conversion time of an eight-bit counter-type A/D converter with the conversion time of a 12-bit successive approximation type A/D converter. Assume a clock frequency of 10 MHz.

Counter-type A/D converter 12.8 μs, successive approximation type 1.2 μs

7. A certain 12-bit successive approximation type A/D converter has a full-scale analogue input of 10 V. It operates at a clock frequency of 1MHz. Determine the conversion time for an analogue input of (a) 1.25 V, (b) 2.50 V, (c) 3.75 V, (d) 7.5 V and (e) 10 V.

(a) 12 μs; (b) 12 μs; (c) 12 μs; (d) 12 μs; (e) 12 μs

Further Reading

1. Demler, M. (2006) *High Speed Analog-to-Digital Conversion*, Academic Press, CA, USA.
2. Jespers, P. G. A. (2001) *Integrated Converters: D to A and A to D Architectures, Analysis and Simulation* (Textbooks in Electrical and Electronic Engineering), Oxford University Press, New York, USA.
3. Razavi, B. (2001)*Principles of Data Conversion System Design*, Oxford University Press, New York, USA.
4. Coombs Jr, C. F. (1999) *Electronic Instrument Handbook*, McGraw-Hill Inc., USA
5. Webster, J. G. (1999) *The Measurement, Instrumentation and Sensors Handbook*, CRC Press (in cooperation with IEEE Press), FL, USA.