Assignment 6

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1 Abstract

In this assignment, we integrated caches into our ToyRISC processor architecture. Specifically, we introduced a level 1 instruction cache between the Instruction Fetch unit and main memory, as well as a level 1 data cache between the Memory Access Unit and main memory. The primary objective of incorporating caches is to mitigate latency by leveraging frequent read and write operations within the cache, thereby enhancing overall processor performance.

To optimize cache utilization, we implemented the LRU (Least Recently Used) replacement policy. This policy ensures that the cache maintains the most recently accessed data while evicting the least recently used data when capacity limits are reached. By adopting the LRU policy, we aim to maximize cache efficiency and further augment the responsiveness of our processor system.

2 IPC for Various size of L1icache

	Data Values of Graph1			
Program	16B	128B	512B	1024B
Descending	0.022976112	0.11489008	0.100362316	0.093962006
Evenorodd	0.022140222	0.02173913	0.021352313	0.02097902
Fibonacci	0.020515518	0.049087476	0.04710145	0.045269877
Palindrome	0.022961574	0.06603774	0.062025316	0.058472555
Prime	0.023052463	0.04489164	0.043026708	0.04131054

Figure 1:

3 IPC Plots

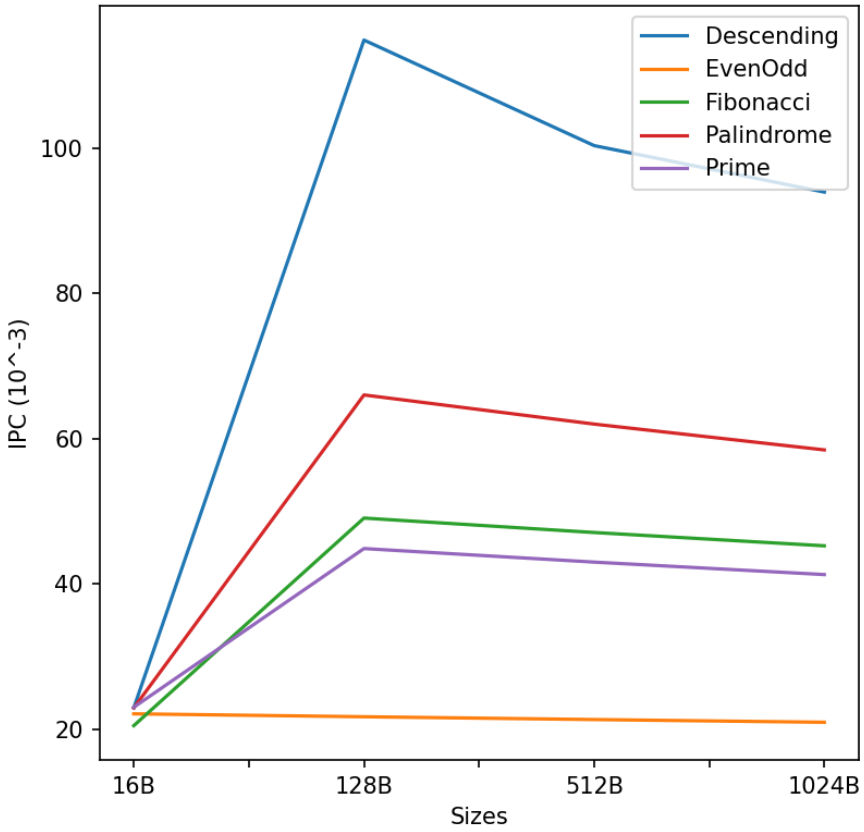

Figure 2: Q1 Plot

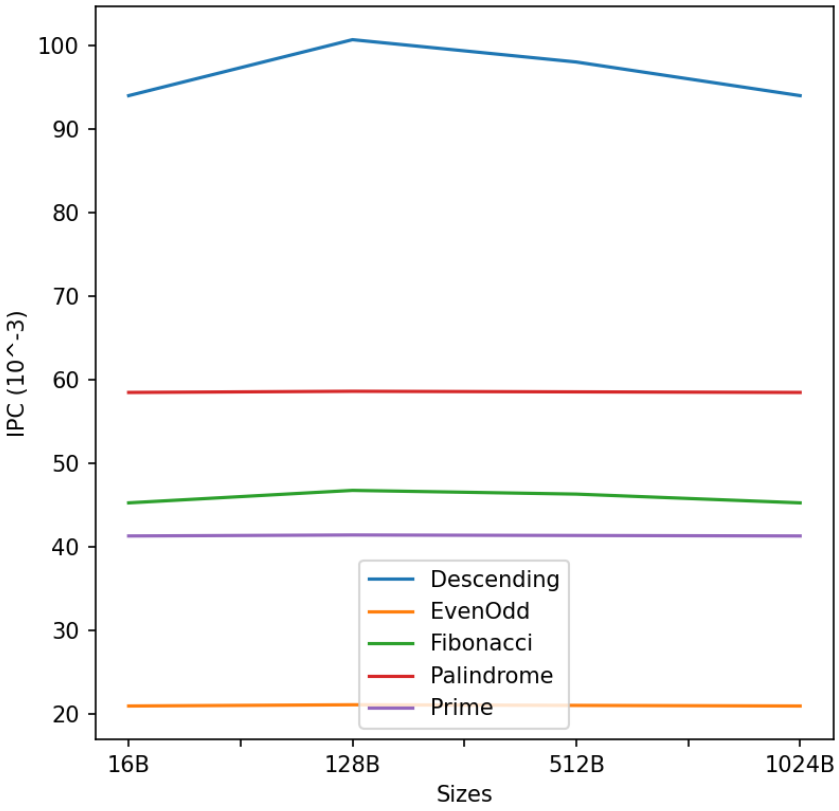

Figure 3: Q2 Plot