Assignment 4

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1 Table

In the following table, we have documented the number of cycles, the number of OF stalls, and the number of wrong branches taken.

Program Name	**Cycles**	**No. of OF stages Stalled**	**No. of Wrong Branch Instructions**
descending.asm	694	122	176
evenorodd.asm	19	6	0
palindrome.asm	124	51	18
fibonacci.asm	165	40	32
prime.asm	83	15	10

2 Comments on Observations

The cycle count of the programs dropped to almost half when they are run on a pipelined processor compared to the non-pipelined processor. In ideal conditions, the cycle count should drop to around one-fifth of the number of cycles in a processor without pipelining. However, ideal conditions are mostly not met due to various data hazards occurring in the execution of the programs. The number of wrong branch instructions and the number of OF stage stalls are also affected depending on the number of data hazards in the program.