A Flexible Power Control Method of VSC-HVDC Link for the Enhancement of Effective Short-Circuit Ratio in a Hybrid Multi-Infeed HVDC System

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Abstract—With the emerging use of voltage source converter high voltage direct current (VSC-HVDC) links, the hybrid multi-infeed HVDC (HMIDC) system that includes the line commutated converter (LCC) HVDC and the VSC-HVDC links is becoming a promising power transmission structure in the modern power systems. To evaluate the contribution of the VSC-HVDC link on the voltage stability of HMIDC system, this paper proposes an effective short circuit ratio (ESCR) calculation method. Through the calculation, the voltage support capability of the VSC-HVDC link can be quantitatively represented by the ESCR. Furthermore, based on the calculation results, a flexible power control strategy for the VSC-HVDC link is developed to provide maximum reactive power support under grid faults. The theoretical analysis of the HMIDC system is based on the Danish transmission grid, evaluated through PSCAD simulations under different grid fault conditions. Simulation results are presented to validate the expected performance of the proposed method.

Index Terms—Effective short-circuit ratio (ESCR), hybrid multi-infeed HVDC (HMIDC) system, voltage source converter high voltage direct current (VSC-HVDC), voltage stability.

I. INTRODUCTION

HE high voltage direct current (HVDC) technology has been widely applied for the long distance, bulk power delivery in transmission grids [1]. With the increased use of HVDC systems, two or more HVDC links tend to feed into an AC system with short electrical distance, and form a so-called multi-infeed direct current (MIDC) transmission system [2], [3]. In such a system, the mutual interactions between the different HVDC links tend to bring a number of operation challenges, particularly when feeding into a weak AC grid [4]. Since conventional HVDC links are generally built using the line commutated converters (LCC), the voltage stability of MIDC systems has become an important concern [5], [6].

Recently, driven by the growing installations of large-scale off-shore wind farms as well as the rapid evolution of power electronics technology, the voltage source converter (VSC) HVDC system, also named as HVDC light or HVDC plus, is gaining a wide acceptance [10]. For example, the world's first VSC-HVDC link was commissioned in Sweden at 1997 [11], and

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the VSC-HVDC link "Tjaereborg" connecting a wind farm was built in 2000 [12]. Thus, together with the existing LCC-HVDC links, a hybrid MIDC (HMIDC) system that consists of the VSC-HVDC and LCC-HVDC links can be envisioned in the near future [13]. In comparison to the conventional MIDC systems with LCC-HVDC links, the flexible power control of VSC-HVDC links brings more possibilities for the voltage stability enhancement of the HMIDC system [14]–[16].

Over the last years, a number of research efforts have been made to investigate the voltage stability of multi-infeed HVDC systems [3]-[9]. However, few literatures for the HMIDC system can be found, particularly the contribution of VSC-HVDC link to the voltage stability of the HMIDC system [14]-[16]. Furthermore, these studies are only performed on the simplified models, and all of them have certain limits for voltage stability analysis. In [14], the VSC-HVDC and LCC-HVDC links feed into an AC grid represented by a voltage source in series with grid impedance, which neglect the dynamic interactions between the HMIDC system and the AC network as well as the impact of electric loads. Recently, the HMIDC system feeding a passive network constituted by the exponential static load and induction motor load was built in [15]. In such system, the load impact on the voltage stability was discussed, whereas the dynamic behavior of AC network was not involved. In [16], an HMIDC system including two LCC-HVDC links and one VSC-HVDC link was developed, where neither the AC grid dynamics nor the load effect were considered.

In the above studies, the enhancement of VSC-HVDC link on the voltage stability of an HMIDC system is only discussed qualitatively. Little information regarding the impacts of the power capacity and control methods of VSC-HVDC link were presented. There is, consequently, a need to find a quantitative method for the voltage stability analysis. The effective short circuit ratio (ESCR) is known as an important index for the voltage stability assessment of a power system with HVDC links [17]. A higher ESCR value indicates a better system voltage stability, which is usually increased by installing either the synchronous condenser or the static synchronous compensator (STATCOM). The ESCR calculation method of the MIDC system has been well discussed in [18]. However, the formulation of the ESCR of an HMIDC system and the contribution of VSC-HVDC on the improvement of the ESCR still remain to be clarified.

It is noted that the control method of the VSC-HVDC link has an important effect on the enhancement of ESCR. Several con-

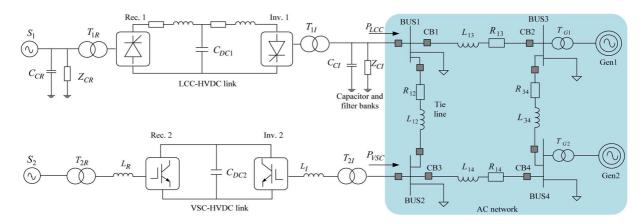


Fig. 1. Simplified one-line diagram of the built HMIDC system.

trol approaches have been reported to allow the VSC-HVDC system to generate a certain amount of reactive power under the grid voltage drops [19]–[21]. However, most of them assumed that the reactive current reference is under a pre-set limit, which restricts the voltage support capability, especially during the severe voltage drops [22]. Hence, it is important to develop a proper control scheme for the VSC-HVDC link, in order to dynamically adjust the output reactive power under different voltage drops.

In this paper, a more realistic HMIDC system model based on the power system of western Denmark is built, where the LCC-HVDC link and the VSC-HVDC link feed, respectively, into two AC buses connected with a tie-line. Taking into account the AC system dynamics, two interconnecting synchronous generators are adopted instead of using the ideal voltage sources. Also, both the static load and the induction motor load are connected to the infeed buses. Furthermore, the formulation of ESCR of the HMIDC system is derived. Thus, the contribution of the VSC-HVDC link to the system voltage stability can be quantitatively analyzed. Based on the ESCR analysis result, a flexible power control method of the VSC-HVDC link is proposed, where the active current reference is dynamically adjusted based on the output of the AC voltage controller. Thus, the maximum use of reactive power support capability of the VSC-HVDC link can be realized. In addition, in the case that the sending end voltage drops, the operation mode switch is designed to keep a stable operation of the VSC-HVDC link. Finally, the case studies of the built HMIDC system under the different grid fault conditions are performed in PSCAD/EMTDC. The simulation results validate the theoretical analysis and the performance of the proposed control method.

The rest of this paper is organized as follows. Section II presents the built HMIDC system based on the western Danish grid. Then, the ESCR of the HMIDC system is formulated from the system equivalent circuit in Section III. Section IV discusses the conventional control method with its limitation on utilizing the voltage support ability of VSC. Section V presents the proposed flexible power control method of VSC-HVDC link. Section VI validates the theoretical analysis through case studies of the HMIDC system. Finally, the paper is concluded by brief remarks in Section VII.

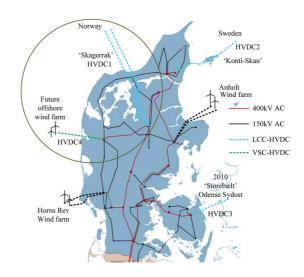


Fig. 2. Western Danish transmission grid

II. HMIDC SYSTEM CONFIGURATION

Fig. 1 illustrates a simplified one-line diagram of the studied HMIDC system. The system consists of an LCC-HVDC link and a VSC-HVDC link, and is modeled based on Western Danish transmission grid (400 kV) shown in Fig. 2. The built HMIDC system model corresponds to the marked area of Fig. 2, where the LCC-HVDC link represents the HVDC link connecting with Norway (HVDC 1), while the VSC-HVDC denotes the planned HVDC link delivering power from a planned offshore wind farm (HVDC 4). The AC network in Fig. 1 models the rest part of western Danish transmission system in Fig. 2. The sending ends of the HVDC links are represented by the voltage sources S_1 and S_2 for the sake of simplicity.

A. AC Network

To consider the dynamic behavior of the infeed AC network, two interconnecting synchronous generators (Gen 1 and Gen 2), the tie-line between two infeed buses, and the electrical loads are modeled to constitute the infeed AC grid. Table I summarizes the main parameters of the AC network.

Parameters	Values	
Frequency	50Hz	
Rated (base)voltage	400kV	
Capacity of Gen1 and Gen2	500MVA	
Load at BUS1	480MW, 320MVar	
Load at BUS2	400MW, 280MVar	
Load at BUS3	350MW, 120MVar	
Load at BUS4	380MW, 120MVar	
	Between BUS1 and BUS3	15km
Transmission line	Between BUS2 and BUS4	15km
distance	Between BUS1 and BUS2	100km
	Retween BUS3 and BUSA	360km

TABLE I AC NETWORK PARAMETERS

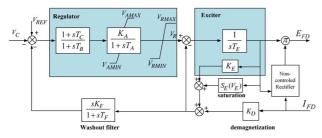


Fig. 3. Block diagram of the AC1A excitation system [24].

The exponential load model is used to represent the static loads, which are given by [23]

$$P = P_0 \left(\frac{V}{V_0}\right)^{NP} \left(1 + K_{PF} \cdot dF\right) \tag{1}$$

$$Q = Q_0 \left(\frac{V}{V_0}\right)^{NQ} \left(1 + K_{QF} \cdot dF\right) \tag{2}$$

where P and Q are the active and reactive power of the load when the bus voltage magnitude is V. P_0 and Q_0 are the load active and reactive power when the bus voltage is V_0 and the system frequency, F, has no error. The NP, NQ, K_{PF} and K_{QF} represent the load characteristics to voltage and frequency, respectively, which can be typically chosen as NP = NQ = 2.0, $K_{PF} = 1$, $K_{QF} = -1$.

B. Synchronous Generators Model

Fig. 3 illustrates the block diagram of the excitation system model for the synchronous generators, which adopts the IEEE type Alternator Supplied Rectifier Excitation System No. 1 (AC1A) in [24]. The AC1A model uses an alternator with the non-controlled rectifier for producing the field current.

The terminal voltage of the generator V_C is first compared with the reference voltage V_{REF} , and then the voltage error is passed through a regulator, which generates the voltage V_R for the exciter in Fig. 3. The field voltage E_{FD} is thus regulated to keep a constant terminal voltage of the generator. The sample parameters given in [24] are used in this system.

It is noted that for each generator, the ability of controlling the terminal voltage is limited by the capacity of generator and the reactive power margin. In the studied system, the power factor of generator is kept higher than 0.8, i.e., the maximum reactive power support has been set as 60% of the capacity.

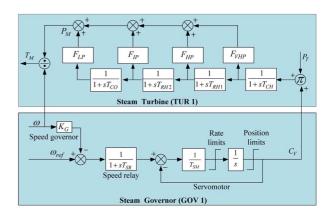


Fig. 4. Block diagram of the governor model and steam turbine [25].

TABLE II HVDC SYSTEM PARAMETERS

Parameters	LCC-HVDC	VSC-HVDC	
Rated capacity	700 MVA	500 MVA	
Active power delivered	500MW	400MW	
Rated AC voltage (line-line)	210 kV	150 kV	
DC voltage	500 kV	300 kV	
Switching frequency	50 Hz	1650Hz	

Base capacity: 500 MVA, Base voltage: 400 kV

Fig. 4 shows the diagrams of the steam turbine model and the associated speed-governing system adopted by generators. The Generic Turbine Model (TUR 1) is adopted as the turbine systems, and the approximate nonlinear mechanical-hydraulic speed-governing (GOV 1) is used as the speed governors for the generators Gen 1 and Gen 2 [25].

The speed governing system consists of a speed regulator, speed relay and a servomotor. The main distinct component in this system is the speed governor, which uses the reciprocal of the primary frequency droop, K_G , to regulate a valve position that indicates the synchronous generator speed. The output of GOV 1 is passed to the TUR 1 model which is based on the approximate linear model of the Tandem Compound Double Reheat system. The typical parameters of the GOV 1 and TUR 1 given in [26] are used here.

C. HVDC Links

Table II lists the voltage ratings and power capacities of the two HVDC links studied in this HMIDC system. The LCC-HVDC link adopts the widely accepted CIGRE benchmark model [27]. A group of capacitors C_C and filter banks Z_C are connected to the AC buses of the LCC-HVDC link to perform reactive power compensation and harmonic filtering, of which the parameters are obtained by scaling the CIGRE benchmark model.

In the control system of the LCC-HVDC link, the transferred active power is regulated to provide frequency support in the presence of disturbances in the western Danish grid. A voltage dependent current limit controller is used to prevent absorbing more reactive power during voltage dips. For the pole control units, the constant DC current control is used at the rectifier side, whereas the minimum extinction angle control is applied at the inverter side.

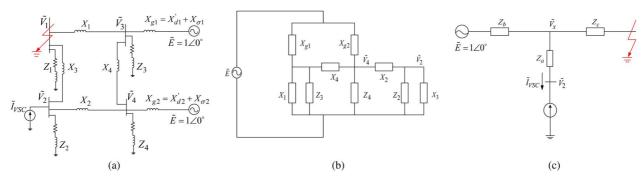


Fig. 5. Equivalent circuits of the HMIDC system under short-circuit condition. (a) Equivalent network of the HMIDC system. (b) Simplified equivalent circuit of (a). (c) Delta-star transformed equivalent circuit.

The VSC-HVDC system that consists of the transformers, the VSCs, the phase reactors, and the DC cables is modeled in the HMIDC system, as shown in Fig. 1. The three-phase two-level bridges based on the IGBT power devices are adopted to represent the VSCs. The DC capacitors of VSCs are designed as an energy buffer to reduce the DC voltage ripple. Detailed control diagrams including the conventional and the proposed schemes will be discussed in Section IV and V.

III. ESCR ANALYSIS OF THE HMIDC SYSTEM

A. ESCR Calculation

The effective short-circuit ratio (ESCR) is generally deemed as an important index for the strength of an AC system with an HVDC link. It can be simply calculated as [28]

ESCR =
$$\frac{S_{sc} + S_{scc} - Q_C}{P_{DC}} = \frac{\sqrt{3}V_s I_{sc} + S_{scc} - Q_C}{P_{DC}}$$
 (3)

where S_{sc} and I_{sc} are the short-circuit capacity and the RMS short-circuit current at the commutated bus, respectively. S_{scc} is the synchronous condenser capacity and Q_C is the reactive power generated from the capacitor banks. V_S is the rated rms line-to-line bus voltage, and P_{DC} is the power of HVDC link.

It is seen that the value of ESCR is dependent on the types of reactive power compensators, which is increased in the case of using the synchronous condensers and reduced in the presence of capacitors. As mentioned in the last section, capacitors are used to compensate the reactive power needed by the LCC-HVDC link, which implies the S_{scc} is zero, while the Q_C is approximately 0.6 times of the P_{DC} under the typical value of extinction angle (15°) in the studied HMIDC system. Hence, the derivation of the system ESCR depends on the magnitude of short-circuit current I_{sc} .

Fig. 5 illustrates the studied system equivalent circuit under a three-phase-to-ground fault at the BUS1 [29]. The load models are simply equivalent as constant impedances $Z_1 \sim Z_4$. The 400-kV transmission lines are represented by the reactance $X_1 \sim X_4$. It is noted that the synchronous generator can be equivalent as a voltage source in series with its transient reactance for the derivation of short-circuit current [30].

Since Gen 1 and Gen 2 are equivalent as the same back electromotive force (EMF) \tilde{E} in series with their own transient re-

TABLE III
PARAMETERS OF EQUIVALENT CIRCUIT

Circuit Parameters	Values	
Transient reactance X'_{dl}	0.15 p.u.	
Transient reactance X'_{d2}	0.13 p.u.	
Transformer leakage reactance $X_{\sigma I}$	0.015 p.u	
Transformer leakage reactance $X_{\sigma 2}$	0.04 p.u.	
Transmission line reactance (per km)	0.001 p.u	

actance, X'_{d1} and X'_{d2} , respectively. The leakage inductances of the transformers T_{G1} and T_{G2} in Fig. 1 are identified as $X_{\sigma 1}$ and $X_{\sigma 2}$.

Under the short-circuit condition, the voltage and delivered power at BUS2 drops significantly. The power controllers of the VSC are consequently saturated and the current references, i_d^* and i_q^* , reach the limit. Hence, the VSC-HVDC link can be equivalent as the constant current source, where the magnitude and the phase angle of the \tilde{I}_{VSC} depend on the VSC capacity limit and the power control methods. To derive the ESCR at BUS1, the equivalent circuit in Fig. 5(a) is redrawn in Fig. 5(b). With the help of the delta-star transformation, Fig. 5(b) can be further simplified as shown in Fig. 5(c), and the related parameters are given in Table III. Notice that the system base voltage is 400 kV and the base capacity is 500 MVA.

Generally, the current limit of the VSC could be 1.5 times of the rated value. The current output of VSC can be given by

$$\tilde{I}_{VSC} = 1.5 \times \frac{S_{VSC}}{\sqrt{3}V_2} (\cos \varphi + j \sin \varphi)$$

$$= I_{VSC} \cos \varphi + j I_{VSC} \sin \varphi$$
(4)

where S_{VSC} is the rated capacity of VSC, V_2 is the rated RMS value of the VSC-HVDC infeed bus voltage, and φ is the phase angle of \tilde{I}_{VSC} referred to the back EMF of generators, \tilde{E} .

From Fig. 5(c), the short-circuit current at BUS1 can be obtained as

$$\tilde{I}_{sc} = \frac{\tilde{V}_x}{Z_c} = \frac{Z_c - Z_c Z_b \tilde{I}_{VSC}}{Z_c (Z_c + Z_b)} = \frac{1 - Z_b \tilde{I}_{VSC}}{Z_c + Z_b}$$
 (5)

where Z_a , Z_b and Z_c are the delta-star transformations of the circuit constants X_{g1} , X_{g2} , $X_1 \sim X_4$ and $Z_1 \sim Z_4$. It is noted that the real parts of the Z_b and Z_c are much smaller compared

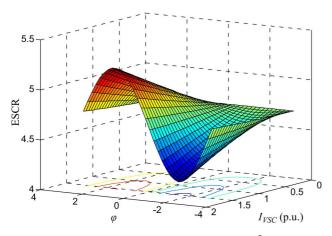


Fig. 6. Relationship between ESCR and the current vector \tilde{I}_{VSC} .

to the imaginary parts, which consequently can be neglected. Thus, Z_b and Z_c are substituted by their imaginary parts X_b and X_c , respectively. Substituting the X_b, X_c and (4) into (5), the magnitude of the short-circuit current \tilde{I}_{sc} can be derived as

$$I_{sc} = |\tilde{I}_{sc}| = \sqrt{G_m^2 I_{VSC}^2 + G_n^2 + 2G_m G_n I_{VSC} sin\varphi}$$
 (6)

where G_m and G_n are

$$\begin{cases}
G_m = \frac{X_b}{X_c + X_b} \\
G_n = \frac{1}{X_c + X_b}
\end{cases}$$
(7)

Substituting (6) into (3), the ESCR at BUS1 is derived as

$$=\frac{\sqrt{3}V_s\sqrt{G_m^2I_{VSC}^2+G_n^2+2G_mG_nI_{VSC}sin\varphi}-0.6P_{DC}}{P_{DC}}.$$
(8)

B. Enhancement of ESCR by VSC-HVDC

From (8), it is found that the ESCR is dependent on the magnitude and phase angle of the output current of the VSC-HVDC link, I_{VSC} and φ , in addition to other circuit parameters.

Fig. 6 depicts the ESCR variations with the changes of I_{VSC} (from 0 p.u. to 2 p.u.) and φ (from $-\pi$ to π). Since the G_m and G_n are positive, the system ESCR can be enhanced through the increase of I_{VSC} . Under the certain VSC-HVDC capacity, i.e., certain I_{VSC} , the ESCR reaches the minimum and maximum values at $\varphi = -\pi/2$ and $\varphi = \pi/2$, respectively.

Note that the vector current control of VSC-HVDC link is oriented to the voltage vector at BUS2, \tilde{V}_2 , whereas the phase angle φ is referred to the back EMF of the generator, \tilde{E} . Hence, to quantitatively analyze the enhancement of ESCR by VSC-HVDC link, the phase shift between the voltage at BUS2 and the generator back EMF needs to be identified under short-circuit condition. From Fig. 5(c), the voltage vector \tilde{V}_2 can be obtained by

$$\tilde{V}_2 = \frac{|Z_x|}{(X_c + X_b)} I_{VSC} \angle \left(\varphi + \theta - \frac{\pi}{2}\right) + \frac{X_c}{X_c + X_b} \tag{9}$$

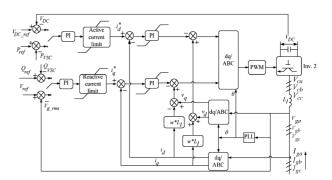


Fig. 7. Block diagram of the conventional control on VSC-HVDC converter.

where Z_x can be expressed as

$$Z_x = (X_c + X_b)Z_a - X_cX_b = |Z_x| \angle \theta \tag{10}$$

where the θ is the phase angle of Z_x referred to \tilde{E} . Based on the parameters in Tables I–III, the voltage vector \tilde{V}_2 is

$$\tilde{V}_2 = 0.018 \angle \left(\varphi + \theta - \frac{\pi}{2}\right) + 0.204 \angle 0. \tag{11}$$

It can be seen that the phase angle of \tilde{V}_2 is almost 0 and in phase with \tilde{E} . Hence, the phase angle φ of \tilde{I}_{VSC} referred to \tilde{E} can be equivalent as the angle between \tilde{I}_{VSC} and \tilde{V}_2 .

Furthermore, since \tilde{I}_{VSC} can be decomposed into i_d^* and i_q^* in the rotating reference frame, the outer power control loop that yields i_d^* and i_q^* determines the extent of ESCR enhancement of VSC-HVDC link. Traditionally, the i_d^* and i_q^* are subjected to the limit of the outer power controllers, such that the phase angle φ and the consequent ESCR are constrained as certain values. Hence, it is needed to develop a proper power control method to enhance the ESCR to a maximum extent within the VSC power capacity.

IV. CONVENTIONAL CONTROL METHOD OF VSC-HVDC

Fig. 7 shows the block diagram of the conventional vectorcurrent control system, which consists of the inner current control loop and the outer power control loop [31].

A. Inner Vector Current Control Loop

The basic idea behind the vector current control method is to align the d-axis of the reference frame to the grid voltage vector, such that the active power and reactive power can be independently controlled using the active and reactive current control loops [32].

The instantaneous powers absorbed by the VSC converter can be expressed in dq-coordinate as

$$\begin{bmatrix}
P_{VSC} \\
Q_{VSC}
\end{bmatrix} = \frac{3}{2} i_d \begin{bmatrix} V_d \\ V_q \end{bmatrix} + \frac{3}{2} i_q \begin{bmatrix} V_q \\ -V_d \end{bmatrix}$$
(12)

where i_d and i_q are the grid-side converter currents in the d-axis and q-axis. V_d and V_q are the grid voltages in the d-axis and q-axis.

By using the phase locked-loop (PLL), the voltage vector is aligned to the d-axis in the dq-coordinate, such that V_q is zero and V_d is the grid voltage amplitude. As a consequence, the

active power and reactive power exchanged between the grid and VSC would be proportional to i_d and i_g , respectively:

$$\begin{bmatrix} P_{VSC} \\ Q_{VSC} \end{bmatrix} = \frac{3}{2} i_d \begin{bmatrix} V_d \\ 0 \end{bmatrix} + \frac{3}{2} i_q \begin{bmatrix} 0 \\ -V_d \end{bmatrix}. \tag{13}$$

The steady-state VSC model for the vector current control loop can be derived based on the basic voltage and current relationship at the grid-side of VSC shown in Fig. 7, which are expressed by the following differential equation:

$$L_{I} \frac{d}{dt} \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{qc} \end{bmatrix} = \begin{bmatrix} V_{ga} \\ V_{gb} \\ V_{qc} \end{bmatrix} - \begin{bmatrix} V_{ca} \\ V_{cb} \\ V_{cc} \end{bmatrix}$$
(14)

where V_{ga} , V_{gb} , and V_{gc} denote the three-phase grid voltage, i_{ga} , i_{gb} , and i_{gc} are the three-phase output current. V_{ca} , V_{cb} , and V_{cc} are the three-phase VSC output voltage. L_I denotes the grid-side inductance including the phase reactor and transformer leakage inductance. With the Park transformation, the VSC model is expressed in the dq-reference frame as

$$L_{I} \frac{d}{dt} \begin{bmatrix} i_{d} \\ i_{q} \end{bmatrix} = \begin{bmatrix} V_{d} \\ V_{q} \end{bmatrix} - \begin{bmatrix} V_{cd} \\ V_{cg} \end{bmatrix} + \omega L \begin{bmatrix} i_{q} \\ -i_{d} \end{bmatrix}$$
 (15)

where V_{cd} and V_{cq} are the grid-side converter voltages at the d-axis and q-axis, respectively. ω is the electrical angular velocity of the grid voltage. Thus, the inner current controller can be obtained directly from (15).

B. Outer Power Control Loop

The outer power control loop is used to generate the current references for regulating the output active power and reactive power of the VSC-HVDC link. Depending on the different control purposes, the active current reference can be obtained through either DC voltage control loop or active power control loop. The reactive current reference can be derived from either reactive power or AC voltage control loop [33].

In the case that the HVDC link connects to a weak system or a passive network, the AC voltage controller can be used to stabilize the system voltage. In the other case that the infeed system is strong, the reactive power controller can be adopted by the VSC-HVDC link. Notice that for an HVDC system, the power flows into and out of DC link must be equal, neglecting the DC losses. Thus, if the receiving-end converter uses active power control, the DC voltage needs to be controlled on the sending-end converter, and vice versa.

C. Current Limit and the ESCR

To prevent the VSC-HVDC from the over-current trip, the current references are generally limited at the output of power control loop, as shown in Fig. 7. The maximum current of the converter are generally chosen as 1.5 times of the rated value. Hence the current reference limit of VSC is defined as

$$i_{\text{lim}}^* = 1.5 i_{rated} \tag{16}$$

where i_{rated} is the rated current of VSC-HVDC.

The current limit i_{lim}^* comprises an active current limit and a reactive current limit, which can be given by

$$i_{\text{lim}}^* = \sqrt{i_{d \text{ lim}}^{*2} + i_{q \text{ lim}}^{*2}}$$
 (17)

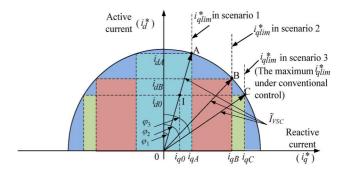


Fig. 8. Current control margin and current vector of receiving end VSC.

where i_{dlim}^* and i_{qlim}^* are the active and reactive current limits, and the choice of them depends on the application. Under the short-circuit condition, the VSC current vector \tilde{I}_{VSC} can be obtained by the current limits, i_{dlim}^* and i_{qlim}^* , which thus has an important effect on the system ESCR. With the different pre-setting limits i_{dlim}^* and i_{qlim}^* , the magnitude of \tilde{I}_{VSC} is fixed as i_{lim}^* due to (17), whereas the phase angle φ can be different so that the enhancement of system ESCR by the VSC-HVDC link is different.

Fig. 8 shows the current controller margins of the VSC and the different current vector \tilde{I}_{VSC} when changing the limit setpoints, i.e., i_{dlim}^* and i_{qlim}^* . Three different current limit setpoints corresponding to the three operating scenarios are chosen in Fig. 8 as follows:

- 1) The limit set-point is set at the point A, where the power factor is kept equal to the value at the initial operating point, I.
- 2) The limit set point is set at the point B, where the i_{dlim}^* and i_{qlim}^* have the same value.
- 3) The limit set point is set at the point C, where the current margin of VSC is only given to the reactive current.

It is worthy to mention that the limit i_{dlim}^* has to be equal or higher than the rated active current i_{rated} , in order to guarantee the active power transmission at steady state. Thus the reactive current limit in the scenario 3) reaches its maximum value as

$$i_{q \lim \Delta Max}^* = \sqrt{i_{\lim}^{*2} - i_{rated}^2} = 1.12 i_{rated}.$$
 (18)

With the different current limits, the current references are limited in the different shaded areas, as shown in Fig. 8, which can be seen as the current controller margin of VSC. Under the short circuit situation (see Fig. 5), the locus of the current reference is driven to the current limit point, "A" "B" or "C", thus the current vector \tilde{I}_{VSC} in three scenarios can be obtained in Fig. 8. The relationship between the phase angles of these current vectors can be given by

$$\varphi_1 < \varphi_2 < \varphi_3 < \pi/2. \tag{19}$$

As a consequence, from (8) it is known that the ESCR values of the HMIDC system in these three scenarios are

$$ESCR_1 < ESCR_2 < ESCR_3.$$
 (20)

It can be concluded that the pre-set limit of the VSC-HVDC restricts the current phase angle φ in the conventional control method, which consequently limits the enhancement of the

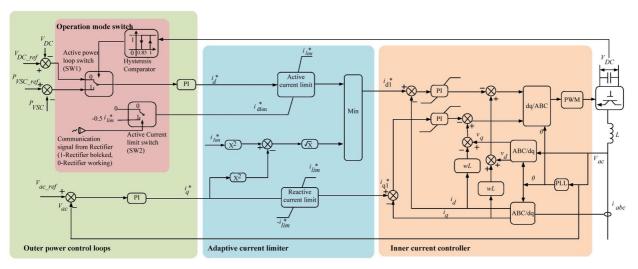


Fig. 9. Block diagram of proposed control method of the VSC-HVDC link at the receiving end.

system ESCR. Hence, it is needed to develop proper control methods so that the maximum system ESCR can be obtained within the capacity of VSC-HVDC link.

V. PROPOSED POWER CONTROL METHOD OF VSC-HVDC

From the above analysis, it is known that the ESCR of the HMIDC system reaches the maximum value when the phase angle between the output current of VSC and the grid voltage, φ , is equal to $\pi/2$. In light of this, instead of pre-setting the output limits in the outer power controllers, a flexible power control method for the VSC-HVDC link is proposed, which allows the phase angle φ to dynamically approach to $\pi/2$ under the grid voltage drops.

Fig. 9 depicts the block diagram of the proposed control method for the VSC-HVDC system. In the approach, a multi-layer control scheme is employed, which includes 1) the inner vector-current controller for the independent control of active power and reactive power, 2) the intermediate adaptive current limiter for realizing maximum reactive power support under the voltage drops of the infeed grid, and 3) the AC voltage as well as active power controllers. Furthermore, to ride-through the grid faults at the sending-end grid, an improved active power control loop is developed. Notice that although only the receiving-end converter of VSC-HVDC is discussed here, the sending-end converter has the same control structure.

A. Adaptive Current Limiter

To overcome the drawback of the pre-setting current limit at the outputs of power controllers, an adaptive current limiter is developed. The idea behind this approach is to dynamically adjust the active current reference according to the change of reactive current reference for restoring the grid voltage during system faults.

The operation principle of the adaptive current limiter can be expressed as follows:

$$i_{q1}^* = \begin{cases} i_q^*, & -i_{\text{lim}}^* < i_q^* < i_{\text{lim}}^* \\ i_{\text{lim}}^*, & i_q^* \ge i_{\text{lim}}^* \\ -i_{\text{lim}}^*, & i_q^* \le -i_{\text{lim}}^* \end{cases}$$
(21)

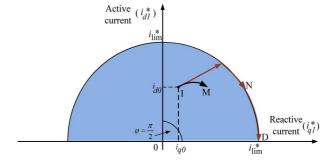


Fig. 10. Current trajectory with the regulation of adaptive current limiter.

$$i_{d1}^{*} = \begin{cases} i_{d}^{*}, & i_{d \text{ lim}}^{*} < i_{d}^{*} \le \sqrt{i_{\text{lim}}^{*2} - i_{q}^{*2}} \\ \sqrt{i_{\text{lim}}^{*2} - i_{q}^{*2}}, & \sqrt{i_{\text{lim}}^{*2} - i_{q}^{*2}} < i_{d}^{*} < i_{\text{lim}}^{*} \\ i_{\text{lim}}^{*}, & i_{d}^{*} \ge i_{\text{lim}}^{*} \\ i_{d \text{ lim}}^{*}, & i_{d}^{*} \le i_{d \text{ lim}}^{*} \end{cases}$$
(22)

where i_d^* and i_q^* are the current signals generated by the outer power control loops. i_{d1}^* and i_{q1}^* are the actual current references regulated by the adaptive current limiter. i_{lim}^* is the VSC current limit defined in (16) and i_{dlim}^* is the lower limit of active current coming from active power control loop.

According to (21) and (22), the current trajectory of i_{d1}^* and i_{q1}^* under the grid voltage drops can be illustrated in Fig. 10. Assuming that the VSC-HVDC system operates at the steady-state point, I. With small grid voltage disturbances, the current references generated from the outer power control loops is still inside the circle shown in Fig. 10. Thus, the system achieves a new stable operation point, M, where the current references i_{d1}^* and i_{q1}^* remain equal to i_{d}^* and i_{q}^* , respectively. On the other hand, under a severe voltage drop, large imbalances between the active power and ac voltage arise, which tends to increase current signals i_{d}^* and i_{q}^* significantly. Once the current signals reach the VSC current limit, i.e., $i_{d}^{*2} + i_{q}^{*2} = i_{lim}^{*2}$, the adaptive current limiter changes the active current reference i_{d1}^* as equal to $\sqrt{i_{lim}^{*2} - i_{q}^{*2}}$ instead of the i_{d}^* based on (22), which indicates that the current reference vector rotates in clockwise along the current limit circle, as shown in Fig. 10. Depending on the fault

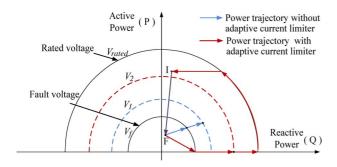


Fig. 11. Capability curve of VSC under voltage drop.

condition, the current reference vector tends to reach at a new stabile operation point N, or continues to rotate until point D where the current phase angle φ is $\pi/2$ and the whole power capacity of the VSC is utilized for the reactive power support.

Fig. 11 shows the VSC capability circle under different AC voltages. Under the certain operation mode, the active power transmission by the VSC-HVDC link is unidirectional. Hence, the VSC capacity circle is drawn in two quadrants. With the various voltage drops, the capability circle shrinks differently. Notice that the steady-state operating point should always be inside the capacity circle, take the point I for example. Under a voltage drop, the output power of VSC drops to the point, F, inside a smaller circle. And the current vector reference meets its limit rapidly.

With the conventional control method, the reactive current reference is limited to be lower than $1.12i_{rated}$, as shown in (18). In contrast, the reactive current reference i_{q1}^* can be increased to i_{lim}^* with the adaptive current limiter. The different reactive current limits result in different voltage restoration, as shown in Fig. 11. The lower restored voltage in turn leads to a smaller capacity of VSC, which is more difficult for a further voltage recovery, and the infeed system tends to become unstable with the conventional control method.

B. Operation Mode Switch

Considering the impact of the sending-end grid fault on the stability of the VSC-HVDC system, an operation mode switch controller is developed in the active power control loop, as highlighted in Fig. 9. This method employs a hysteresis-based active power loop switch (SW1) and an active current limit switch (SW2).

Depending on the system conditions, three operation modes are available for the VSC-HVDC link, which are chosen by the operation mode switch. Table IV gives the operation modes and corresponding switch states under different system conditions. Notice that in all the operation modes, AC voltage control is applied in power control loops of VSCs at both sides of VSC-HVDC link to keep the grid voltage constant.

During the steady-state operation, SW1 = SW2 = 0, and the active power control is applied at the receiving-end VSC. The lower limit of the active current, i_{dlim}^* , is set as zero to prevent inverse active power, as shown in Fig. 9. In the presence of the sending-end voltage drops, the active power transmission by the VSC-HVDC link is limited, and the DC voltage drops down rapidly, due to the loss of DC voltage control capability

TABLE IV
OPERATION MODES AND SWITCH STATES

SW1	SW2	Operation mode	System condition (event)
0	0	Active power control at Inverter; DC voltage control at Rectifier.	Under steady stated or infeed grid fault.
1	0	DC voltage control at Inverter; Active power control at Rectifier.	Under sending end grid fault.
1	1	Rectifier blocked and rest of the VSC-HVDC is controlled as a STATOM.	Under sending end grid fault which is not cleared in time.

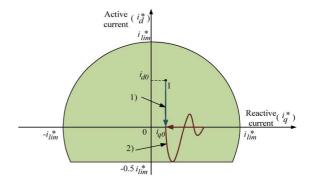


Fig. 12. Current reference trajectory of VSC in the presence of permanent fault at sending end grid.

at the sending-end converter. Thus, to prevent the DC voltage from collapse, SW1 is set to 1 through a hysteresis comparator once the DC voltage drops down lower than the 0.9 p.u. Consequently, the DC voltage is regulated at the receiving-end converter, which decreases the output active power rapidly. If the fault is temporary and be cleared in a short period, along with the recovery of active power injected into VSC-HVDC link, the DC voltage is restored. Once the DC voltage is higher than the rated value, the SW1 will be set to zero and the power control loop changes back to the pre-event situation.

On the other hand, if the fault is not cleared in time, the sending-end converter should be blocked to isolate the fault. In this case, the SW2 is set as 1 through the communication signal form the sending-end and the i_{dlim}^* becomes lower than zero. Thus, the receiving-end VSC operates like a STATCOM to stabilize the infeed system voltage. The DC voltage is kept constant by the inverse active current. It is noted that the lower limit of active current i_{dlim}^* is designed based on the expected restoring speed of DC voltage, which is chosen as $-0.5\ i_{lim}^*$.

Fig. 12 shows the current controller margin and the current reference trajectory of the receiving-end VSC during the permanent fault at the sending-end grid. The trajectory can be divided into two parts: 1) the i_d^* first drops down quickly to maintain the DC voltage by setting SW1 as 1, and then 2) the sending-end converter is blocked, the i_{dlim}^* is changed to be -0.5 i_{lim}^* . The output current of VSC-HVDC becomes pure reactive current after a short transient.

C. Impact of Adaptive Current Limiter on Active Power Delivery

It is noted that to realize the maximum voltage support by the VSC-HVDC under a severe grid voltage drop, the adaptive current limiter reduces the active current reference to release the current control margin for reactive current reference. Thus, it is needed to first evaluate the infeed AC system response through case studies before using the proposed control method for the VSC-HVDC link.

However, the frequency deviation brought by the proposed control method is usually small and decays in a short period. Take the studied system for example, the frequency fluctuations shown in Section VI is within the grid code, due to the following reasons:

- The active power imbalance in the infeed AC system is low, since both the output active power of VSC-HVDC link and active power demand from the load are reduced under the voltage drop. Thus, a further active power reduction by the adaptive current limiter on this basis will not result in large system frequency deviation.
- 2) Furthermore, the active power reduction of the VSC-HVDC link is a transient phenomenon. During the transient, the inertia energy stored in the rotating mass of the infeed system maintains the system frequency within the reasonable limit.

On the other hand, in the studied system, with the reduction of active power delivery by the VSC-HVDC link, the frequency of the sending-end grid tends to increase. It is worthy to mention that the power system with HVDC links is normally designed with a certain tolerance of frequency deviation, particularly in the cases of emergency power change in HVDC systems or the grid faults at the other side of HVDC links [34]. Therefore, the small frequency fluctuation at the sending-end grid does not bring additional stability problems.

VI. SIMULATION RESULTS

To validate the calculation method of the system ESCR and the performance of the proposed power control method, case studies on the HMIDC system shown in Fig. 1 are conducted in PSCAD/EMTDC. The system parameters are summarized in Tables I–III. The following initial operating conditions are assumed in the case studies.

- 1) The synchronous generators (Gen1 and Gen2) deliver 0.75 p.u. active power, respectively, to the transmission system.
- 2) The voltage magnitudes at the terminals of generators are set as 1.05 p.u., respectively.
- 3) The VSC-HVDC and the LCC-HVDC deliver 0.8 p.u. power (P_{VSC}) and 0.7 p.u. power (P_{LCC}) to the AC system, respectively.
- 4) The VSC current limit is 1.5 times of the rated current.

A. Validation of the ESCR Calculation

Fig. 13 shows the simulation results of system symmetrical short circuit current [35], when the three-phase-to-ground fault appears at BUS1. Notice that the current peaks during the first line frequency period is the sub-transient fault currents, while the short circuit currents used for the ESCR calculation ($|\tilde{I}_{SC}|$) is the transient fault current values as marked in Fig. 13.

In the case of without the VSC-HVDC link, based on the system parameters shown in Tables I–III, the short circuit current $|\tilde{I}_{SC}|$ and the system ESCR can be derived from (6) and (8) as 4.6 kA and 4.27, respectively. Compared with the blue

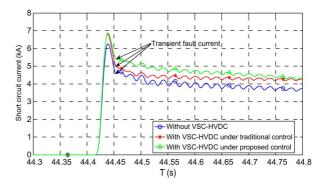


Fig. 13. System short circuit current on BUS1 with different situations.

TABLE V PARAMETERS OF DYNAMIC LOADS

Parameters	Induction motor I	Induction motor II
Location	BUS1	BUS2
MVA	500	500
Percentage in local load	75%	60%
Mechanical torque	0.7p.u.	0.6p.u.
Inertia	3.412 s	3.412 s

curve shown in Fig. 13, it can be seen that the theoretical analysis matches well with the time-domain simulation result.

When applying the VSC-HVDC link with the conventional control method, the active and reactive currents of VSC reach to their own limits, which are $i_d=1.3~\mathrm{p.u.},\,i_q=0.75~\mathrm{p.u.}$ Then, substituting them into (6) and (8), the $|\tilde{I}_{SC}|$ is 4.99 kA and the ESCR is obtained as 4.67, which are verified by the red curve in Fig. 13.

When applying the VSC-HVDC link with the proposed control method, the VSC current phase angle φ is $\pi/2$, which implies the $i_d=0$ p.u. and $i_q=1.5$ p.u. Thus, the short circuit current and ESCR can be derived from (6) and (8) as 5.4 kA and 5.02, which matches well with the green curve in Fig. 13.

B. Voltage Stability Enhancement of the Proposed Control Method

The system voltage stability is heavily dependent on the load characteristics. It is known that the induction machine is sensitive to the variation of system voltage, which is a typical load for voltage stability analysis. Thus, two induction motor loads are connected with the BUS1 and BUS2 via the 500-MVA transformers, respectively. The parameters of the induction motors are listed in Table V.

Two different grid fault cases are considered to compare the performances of the proposed and the conventional control methods. Furthermore, three different scenarios corresponding to the different pre-setting current limits discussed in Section IV are evaluated.

Case 1: Three-Phase-to-Ground Fault at the Transmission Line Between BUS1 and BUS3: Fig. 14 shows the simulated waveforms for the system with a three-phase-to-ground fault at the transmission line between BUS1 and BUS3. The fault occurs at the instant of 40 s and is cleared by CB1 and CB2 0.1 s later. A reclosure takes place at 40.7 s. Before the fault is cleared, it is seen from Fig. 14(a) and (b) that the voltage at

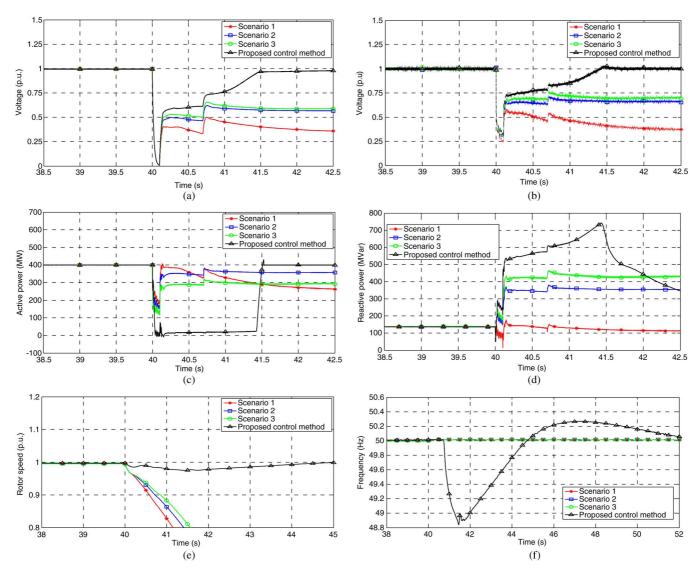


Fig. 14. System performance under grid fault of three phase to ground with different control law. (a) Voltage at BUS1. (b) Voltage at BUS2. (c) Active power of VSC-HVDC. (d) Reactive power of VSC-HVDC. (e) Rotor speed of induction machine at BUS1. (f) System frequency.

BUS1 drops to nearly zero and the voltage at BUS2 drops to 0.3 p.u. once the fault occurs. The induction motors decelerate due to the mismatch between the electromagnetic torque and the mechanical torque, as shown in Fig. 14(e).

From Fig. 11 it is known that the capability of the VSC-HVDC link decreases significantly with the voltage drop at BUS2. Furthermore, depending on the setting of current limits, the extents of reducing active power and increasing reactive power are different, as shown in Fig. 14 (c) and (d). It can be seen that with the proposed adaptive current limiter, the severe voltage drop at BUS2 moves the current reference vector to the current boundary and then rotate clockwise until the point D in Fig. 10, where all the VSC-HVDC capability are utilized to contribute reactive power support to the system. Notice that little change arises on the system frequency before the fault is cleared, as shown in Fig. 14(f), due to the voltage-dependent load characteristic.

Once the fault is cleared at the instant of 40.1 s, the system voltages begin to recover. From Fig. 14(c) and (d), it is clearly seen that the higher the reactive current reference limit, the more

reactive power support can be obtained in the three scenarios of the conventional control method. In contrast, with the proposed adaptive current limiter, the reactive current limit reaches the full current limit and the maximum reactive power support is obtained. Consequently, the adaptive current limiter realizes the highest system voltage recovery level and lowest speed reduction of the induction motors, as shown in Fig. 14(a), (b), and (e).

At the instant of 40.7 s, the CB1 and CB2 reclose and the system structure is restored. From the voltage waveforms, it can be seen that the adaptive current limiter enables the VSC to provide sufficient reactive power support in order to restore the system voltages, whereas the conventional control method fails to recover the system voltages and the speed of induction motors keeps reducing to make the system unstable. It implies that a full reactive power support capability is needed under the severe voltage drops to ensure a stable operation of power system.

Furthermore, once the voltage at BUS2 recovers back to the rated value using the adaptive current limiter, the reactive current reference drops down quickly and release the control margin to the active current. Then, the current reference vector

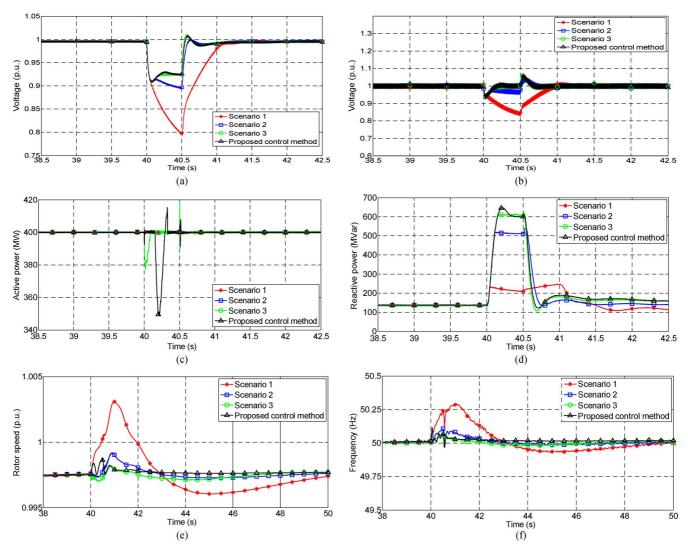


Fig. 15. System performance under grid fault of voltage sag. (a) Voltage at BUS1. (b) Voltage at BUS2. (c) Active power of VSC-HVDC. (d) Reactive power of VSC-HVDC. (e) Rotor speed of induction machine at BUS1. (f) System frequency.

of the VSC-HVDC moves back to the original operation point, and the output powers of the VSC-HVDC go back to nominal value. However, before the voltage at BUS2 reaches the rated value, the reactive current reference is kept as the full current limit value. Then, the active power injected from VSC-HVDC is kept almost zero, whereas the active power demanded from the load increases due to the restoration of the system voltage. As a consequence, the system frequency keeps reducing till the instant of 41.5 s when the system voltage becomes higher than the rated voltage, as shown in Fig. 14(f). Nevertheless, it is worthy to note that such a transient fluctuation of the system frequency is in the acceptable area according to the Grid Code [36], hence it is not perceived as a stability problem.

Case 2: Voltage Sag Caused by the Remote Grid Fault: Fig. 15 shows the simulated waveforms under the system voltage sag resulting from a remote grid fault. In this case, the voltage disturbance is represented by a short circuit to ground through an inductance at BUS3. The voltage sag is assumed small compared to the Case 1, so that there is no action on any circuit breakers in the HMIDC system. The voltage sag occurs at 40 s and last about 0.5 s.

Fig. 15(a) and (b) shows the different system voltage sags corresponding to different settings of the current limit during the fault period. It is clearly seen that the higher the reactive current reference limit, the smaller the voltage sag presents in the three scenarios of the conventional control method. Also, from Fig. 15(d), it can be seen that the reactive power support from the VSC is enhanced with the increase of reactive current reference limit.

Notice that the presence of the active power dip in scenario 3 is caused by the low active current margin in this case. Once the fault occurs, the small voltage dip at BUS2 has little effect on the capability of the VSC-HVDC. Thus, an increase on the active current is needed to maintain the output active power, whereas the active current limit in scenario 3 is still kept as the rated active current as discussed in Section IV. Hence, a small active power dip appears at the beginning of the fault and then disappears rapidly.

Fig. 15(e) shows the speed change of the induction motor at BUS1. It is seen that an increase with different extent arises during the voltage sag, and the less the reactive current limit reference, the higher the motor speed increases. Notice that sim-

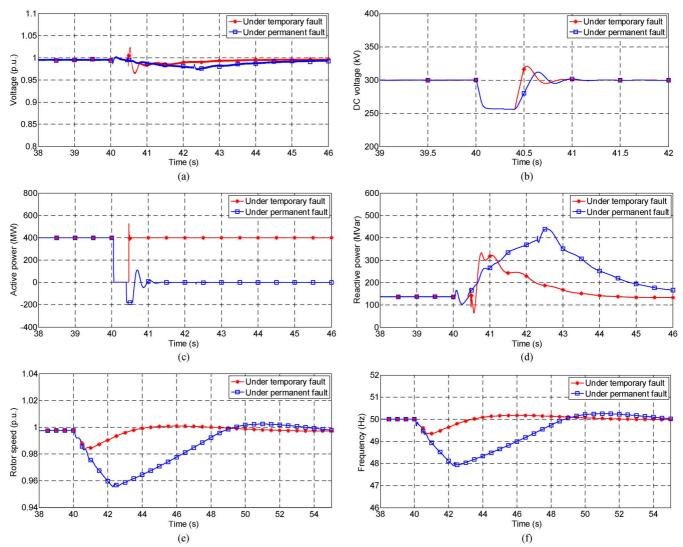


Fig. 16. System performance under grid fault at sending end of VSC-HVDC. (a) Voltage at BUS1. (b) DC voltage of VSC-HVDC link. (c) Active power of VSC-HVDC. (d) Reactive power of VSC-HVDC. (e) Rotor speed of induction machine at BUS1. (f) System frequency.

ilar variation can also be observed in the system frequency, as shown in Fig. 15(f). This is resulted from a temporary unbalance of active power. Little change on the output active power of LCC-HVDC and generators appears due to the small voltage sag in system. And the active power of VSC-HVDC is kept almost the same by the active power controller, whereas the active power demand from the load is reduced with the voltage drop. Hence, the extra active power accelerates the induction motor and increase the system frequency correspondingly. However, with the proposed control method, the temporary active power drop of VSC-HVDC instead alleviates this unbalance of active power. As a consequence, the fluctuations of the induction motor speed and the system frequency is the smallest one.

C. Sending-End Grid Fault

To further confirm the performance of the proposed control method, the effect of the sending-end grid fault in the HMIDC system is evaluated in the simulation study. Fig. 16 shows the system waveforms under both the temporary and permanent fault conditions at the sending-end grid.

Considering the worst situation, a three-phase short circuit to ground is assumed to occur at the connection bus of VSC-HVDC link in the sending-end grid. Two cases are considered, which includes 1) the fault is temporary and cleared after 0.4 s of fault occurrence, and 2) the fault is permanent and rectifier of HVDC link is blocked after 0.4 s of fault occurrence. Notice that in the second case, the fault results in a permanent loss of the active power injection from VSC-HVDC to the grid. Thus, some other controllers have to be activated to keep the system frequency stable, such as the injection of spinning reserve of generator or the load shedding. In this simulation study, 50% of the active load at BUS3 and BUS4 are shed once the system frequency drops down to 48 Hz.

Fig. 16(a) and (d) shows the simulated system voltage and the reactive power waveforms of the VSC-HVDC link. During the sending-end grid faults, the delivered active power drops down significantly, whereas little reactive power disturbance is imposed on the receiving-end grid, hence the infeed AC system voltages keep around the rated values, as shown in Fig. 16(a), and the reactive power of VSC-HVDC in such case has little fluctuation, as shown in Fig. 16(d).

Fig. 16(b) and (c) shows the DC voltage and active power waveforms of the VSC-HVDC system. Notice that the active power transmission failure decreases the DC-link voltage of VSC-HVDC system. Thus, the sending-end grid fault can be detected by measuring the DC-link voltage at the receiving-end converter. Once the DC voltage drops below 0.9 p.u., the active power loop switches from controlling the active power to keeping the DC voltage constant, as shown in Fig. 16(b). Thus, the output active power is controlled to be zero, as shown in Fig. 16(c). Due to the loss of active power, the system frequency and the induction motor speed becomes decreased, as shown in Fig. 16(e) and (f).

In the first case of temporary grid fault, after the fault clearance (40.4 s), the active power transmission is thus restored and DC voltage is increased to the rated value, as shown by the red lines in Fig. 16(b) and (c). Also, the system frequency is increased to 50 Hz again and the rotor speed restore to the rated value. During the recovery period, it is noted that the reactive power demand from the static load is higher than the normal operation due to its frequency-dependent characteristic in (2), and meanwhile, the speed restoration of the induction motor needs both the active and reactive power support. Thus, an increase of the reactive power consequently appears at the output of VSC, as shown in Fig. 16(d), such that the system voltage only has a small dip, as shown in Fig. 16(a).

In the second case of permanent grid fault, after 0.4 s of fault occurrence, the sending-end converter of the VSC-HVDC link is blocked, and the receiving-end converter is switched into a STATCOM operation, in which the active current reference is extended below zero, as shown in Fig. 12. The DC voltage is maintained by injecting active power from the infeed system to the DC capacitor, as shown in Fig. 16(b). Fig. 16(c) shows the inverse active power flow of the receiving-end converter.

To maintain the system frequency stable, the load shedding at BUS3 and BUS4 is enabled once the system frequency is lower than 48 Hz. After the load shedding, system frequency is increased and the speed of induction motor is also increased consequently, as shown by the blue lines in Fig. 16(e) and (f). Furthermore, from Fig. 16(d), it is clearly seen that due to the larger drops of induction motor speed and system frequency compared to the temporary fault case, the needed reactive power is consequently higher.

VII. CONCLUSIONS

A hybrid multi-infeed HVDC system model has been developed based on Western Danish power system, including two types of HVDC links: LCC-HVDC and VSC-HVDC.

The system ESCR has been derived and calculated with an equivalent circuit method. As a consequence, a method of quantitatively evaluating the improvement of system voltage stability by a VSC-HVDC link can be obtained.

To make the AC grid stiffer with higher ESCR value, the paper has proposed a power control method for the VSC-HVDC link. The control method can achieve the required current angle of VSC under short circuit situation, which increase the ESCR to a satisfactory value. Thereby, system voltage stability can be improved.

The analysis on the system ESCR and the proposed control method has been verified by simulation study in PSCAD. Three disturbance situations in the AC system have been considered and the simulation results show that the proposed power control method can support system voltage more effectively. Hence the system voltage stability can be significantly improved in comparison with the traditional VSC-HVDC control method.

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