Vivado Design Suite Tutorial

Design Flows Overview

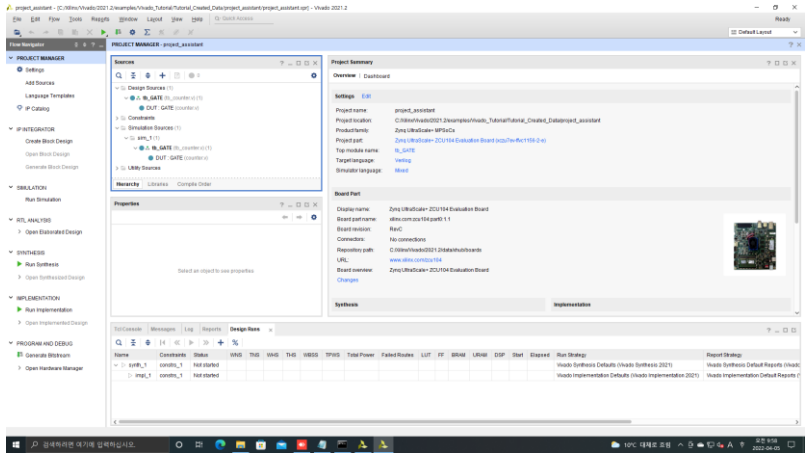
4th April 2022

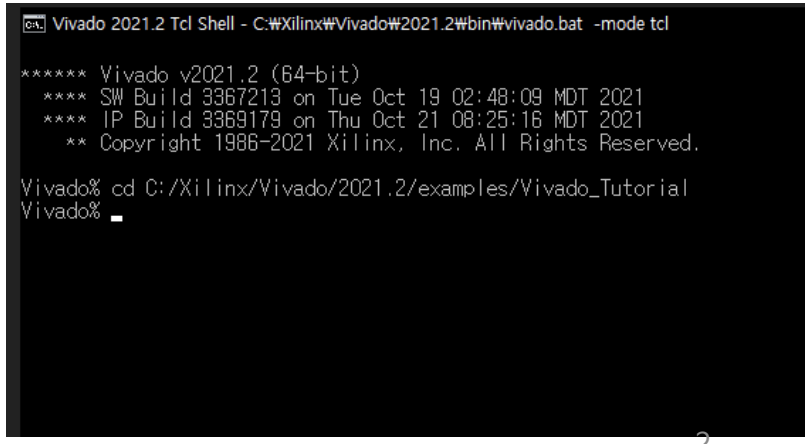
Introduction

- Vivado design overflow
  - Xilinx 사의 Vivado Integrated Design Environment(IDE)

- Vivado의 2가지 모드
  - Project mode
    - Gui를 통해 design들을 컴파일
      - 개발 각 단계마다 reports, run design rule checks, write design checkpoint
    - 프로젝트 파일(.xpr) 및 디렉토리 구조
      → 디자인 소스 파일, IP 데이터, 합성, 구현 결과 관리
    - 소스 파일, IP 디자인, 소스 파일과의 cross-probing과 같은 기능
      →전반적인 디자인 프로세스 관리

  - Non-project mode
    - Vivado가 아닌, 커멘드 라인을 이용하는 스크립트 방식
      - tcl의 커멘드라인에 명령어를 쳐서 직접 관리하는 방식
    - Vivado 프로젝트 기반의 기능 사용 X
      - 소스파일/실행 관리, 소스 파일과의 cross-probing
    - 필요하다면, report나 design checkpoint 직접 생성





Introduction

- Tcl 명령어
  - 모드에 따라 Tcl 명령어는 달라짐
  - Non-project mode
    - read_Verilog/vhdl/edif/ip/xdc
      → 소스파일이 로딩됨
  - Project mode
    - create_project, add_files, import_files, and add_directories
      → 프로젝트, 파일, 디렉토리를 만드는 명령어를 사용해서 design 관련 파일을 관리
    - launch_runs
      - synthesis, place, route, bitstream을 한번에 수행할 수 있습니다.

Introduction

- Lab 1: the Non-Project Design Flow
  - Bft 디자인을 구현하기 위한 명령어 예제 검토
  - 각 과정마다 결과를 리뷰
  - design checkpoints 쓰기
  - timing constraint definition& I/O planning 탐색, constraints 업데이트
  - 구현된 Design checkpoint를 open: timing, power, utilization and routing 분석
  - 로그파일 리뷰

- Lab 2: Using the Project Based Design Flow
  - Create a new project.
  - 비바도 IDE를 이용하여 Bft 디자인을 구현하기 위한 준비
  - 각 과정마다 결과를 리뷰
  - timing constraint definition, I/O planning and design analysis 탐색
  - 구현된 design을 open: timing, power, resource utilization, routing, and cross- probing 분석

Step 1: Examine the Example Script

- Sample design: bft
- Design target: xc7k70T
- Vivado design suite 버전: 2020.1 이상
- 튜토리얼 파일 위치
  - <비바도 설치위치>/Vivado/<version>/examples/Vivado_Tutorial

- Open the example scrip
  - Create_bft_kintex7_batch 파일
    - review the different steps

create_bft_kintex7_batch - Windows 메모장

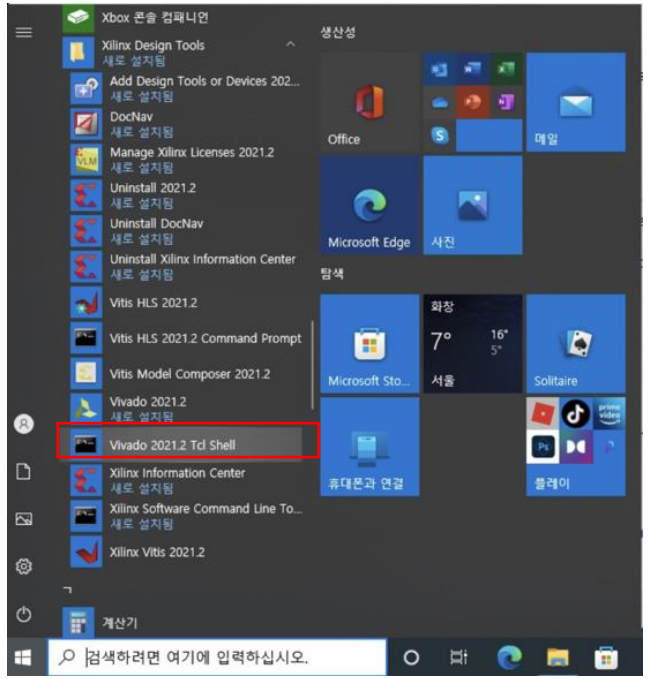
파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

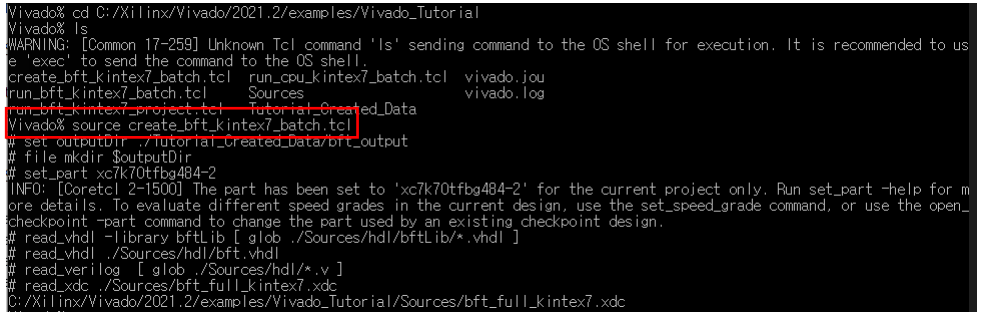
```
# STEP#0: define output directory area and set part
#
set outputDir ./Tutorial_Created_Data/bft_output
file mkdir $outputDir
set_part xc7k70tfbg484-2
#
# STEP#1: setup design sources and constraints
#
read_vhdl -library bftLib [ glob ./Sources/hdl/bftLib/*.vhdl ]
read_vhdl ./Sources/hdl/bft.vhdl
read_verilog  [ glob ./Sources/hdl/*.v ]
read_xdc ./Sources/bft_full_kintex7.xdc
#
# STEP#2: run synthesis, report utilization and timing estimates, write checkpoint design
#
#synth_design -top bft
#write_checkpoint -force $outputDir/post_synth
#report_timing_summary -file $outputDir/post_synth_timing_summary.rpt
#report_power -file $outputDir/post_synth_power.rpt
#report_clock_interaction -delay_type min_max -file $outputDir/post_synth_clock_interaction.rpt
#report_high_fanout_nets -fanout_greater_than 200 -max_nets 50 -file $outputDir/post_synth_high_fanout_nets.rpt

# STEP#3: run placement and logic optimzation, report utilization and timing estimates, write checkpoint design
#
#opt_design
#place_design
#phys_opt_design
#write_checkpoint -force $outputDir/post_place
#report_timing_summary -file $outputDir/post_place_timing_summary.rpt
#
# STEP#4: run router, report actual utilization and timing, write checkpoint design, run drc, write verilog and xdc out
#
#route_design
#write_checkpoint -force $outputDir/post_route
#report_timing_summary -file $outputDir/post_route_timing_summary.rpt
#report_timing -max_paths 100 -path_type summary -slack_lesser_than 0 -file $outputDir/post_route_setup_timing_violations.rpt
#report_clock_utilization -file $outputDir/clock_util.rpt
#report_utilization -file $outputDir/post_route_util.rpt
#report_power -file $outputDir/post_route_power.rpt
#report_drc -file $outputDir/post_imp_drc.rpt
#write_verilog -force $outputDir/bft_impl_netlist.v
#write_xdc -no_fixed_only -force $outputDir/bft_impl.xdc
#
# STEP#5: generate a bitstream
```

Step 2: Starting Vivado with the Example Design

- Launch the Vivado Design Suite Tcl shell
  - 윈도우 – 모든 프로그램 – Xilinx design tools – Vivado tcl shell

- Source a Tcl script to create the tutorial design
  - cd <비바도 설치위치>/Vivado_Tutorial
  - source create_bft_kintex7_batch.tcl

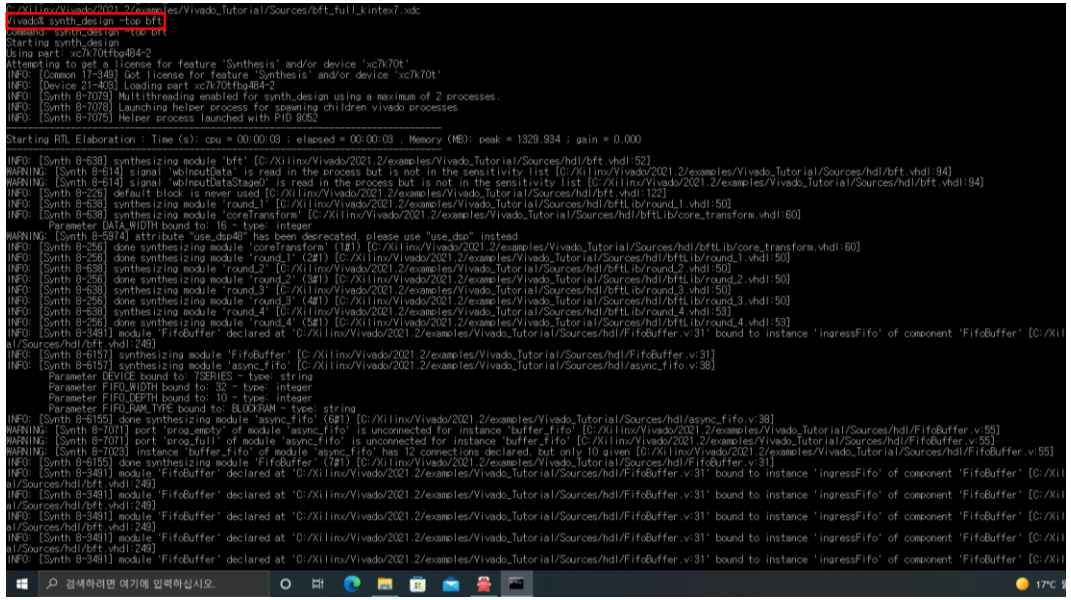




Step 3: Synthesizing the Design

- synth_design -top bft
  - Synth_design 명령어를 create_bft_kintex7_batch.tcl에서 복사/붙여넣기
    - 복사한 명령어는 마우스 오른쪽 버튼을 클릭하여 붙여넣기 가능
  - Synthesis(합성) 완료

```
# STEP#1: setup design sources and constraints
#
read_vhdl -library bftLib [ glob ./Sources/hdl/bftLib/*.vhdl ]
read_vhdl ./Sources/hdl/bft.vhdl
read_verilog  [ glob ./Sources/hdl/*.v ]
read_xdc ./Sources/bft_full_kintex7.xdc
#
# STEP#2: run synthesis, report utilization and timing estimates, write checkpoint design
#
#synth_design -top bft
#write_checkpoint -force $outputDir/post_synth
#report_timing_summary -file $outputDir/post_synth_timing_summary.rpt
#report_power -file $outputDir/post_synth_power.rpt
#report_clock_interaction -delay_type min_max -file $outputDir/post_synth_clock_interaction.rpt
#report_high_fanout_nets -fanout_greater_than 200 -max_nets 50 -file $outputDir/post_synth_high_fanout_nets.rpt

# STEP#3: run placement and logic optimzation, report utilization and timing estimates, write checkpoint design
#
#opt_design
#place_design
#phys_opt_design
#write_checkpoint -force $outputDir/post_place
#report_timing_summary -file $outputDir/post_place_timing_summary.rpt
#
```



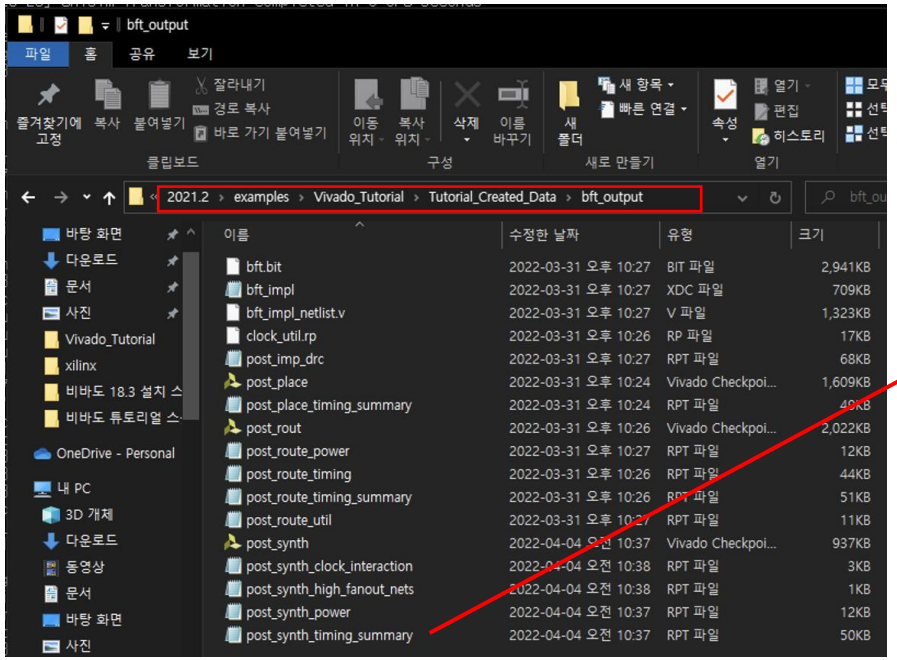
Step 3: Synthesizing the Design

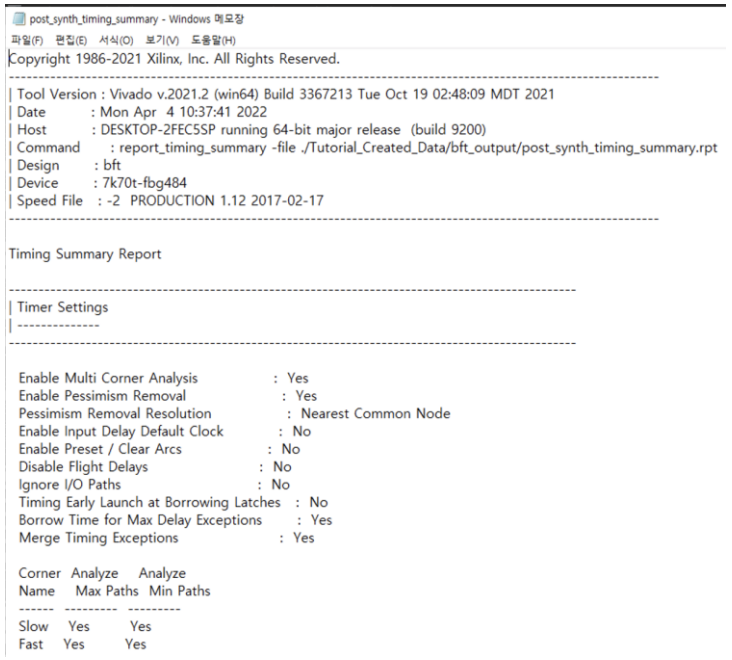
- Checkpoint 쓰기
  - write_checkpoint -force $outputDir/post_synth
- Timing 속성 확인
  - report_timing_summary -file $outputDir/post_synth_timing_summary.rpt
- Power 확인
  - report_power -file $outputDir/post_synth_power.rpt
- Clock interaction 확인
  - report_clock_interaction -delay_type min_max -file ₩ $outputDir/post_synth_clock_interaction.겟
- High fanout nets 확인
  - report_high_fanout_nets -fanout_greater_than 200 -max_nets 50 -file ₩ $outputDir/post_synth_high_fanout_nets.rpt

```
Vivado% write_checkpoint -force $outputDir/post_synth
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.027 . Memory (MB): peak = 1422.781 ; gain = 0.000
INFO: [Common 17-1381] The checkpoint 'C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output
/post_synth.dcp' has been generated.
C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output/post_synth.dcp
Vivado% report_timing_summary -file $outputDir/post_synth_timing_summary.rpt
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -2, Delay Type: min_max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
Vivado% report_power -file $outputDir/post_synth_power.rpt
Command: report_power -file ./Tutorial_Created_Data/bft_output/post_synth_power.rpt
Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation
0 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
report_power completed successfully
Vivado% report_clock_interaction -delay_type min_max -file $outputDir/post_synth_clock_interaction.rpt
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -2, Delay Type: min_max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
WARNING: [Timing 38-164] This design has multiple clocks. Inter clock paths are considered valid unless explicitly exclu
ded by timing constraints such as set_clock_groups or set_false_path.
Vivado% report_high_fanout_nets -fanout_greater_than 200 -max_nets 50 -file $outputDir/post_synth_high_fanout_nets.rpt
report_high_fanout_nets: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.036 . Memory (MB): peak = 1667.152 ; gain = 0.000

C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output/post_synth_high_fanout_nets.rpt
Vivado%
```

Step 3: Synthesizing the Design

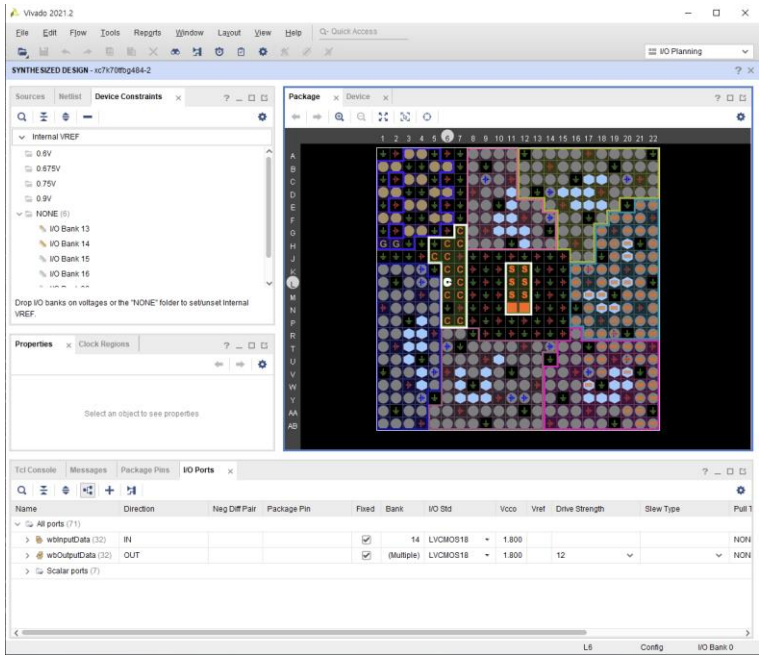
- Report된 결과들은 output directory에 저장
  - <비바도 설치위치>/Vivado_Tutorial/Tutorial_Created_Data/bft_output
  - Report들은 text editor(or 메모장)로 확인

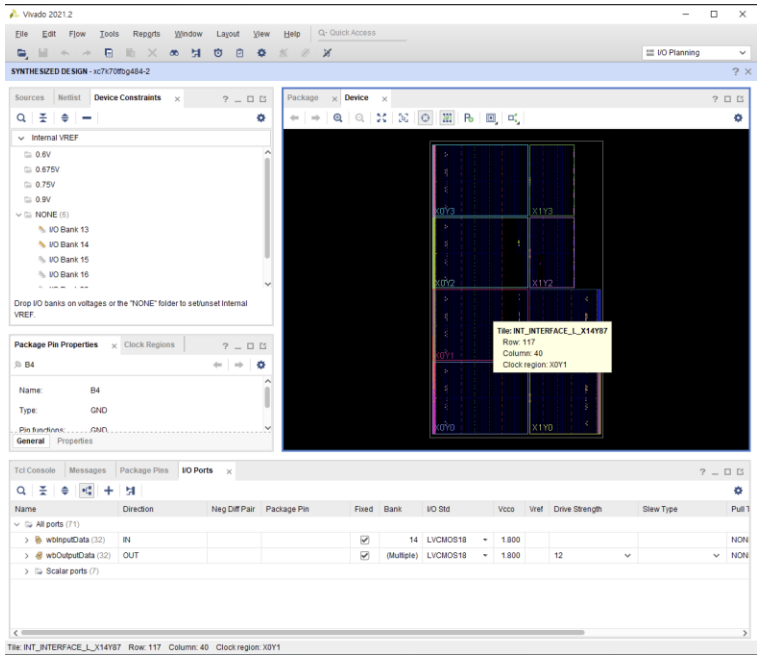




Step 4: Launching the Vivado IDE

- Non-project 모드
  - 각 design process에 대해 vivado 사용가능
- Start_gui
  - Design과 설정 변경(constraint manipulation), 분석(analysis)을 시각화하여 사용자의 편의↑

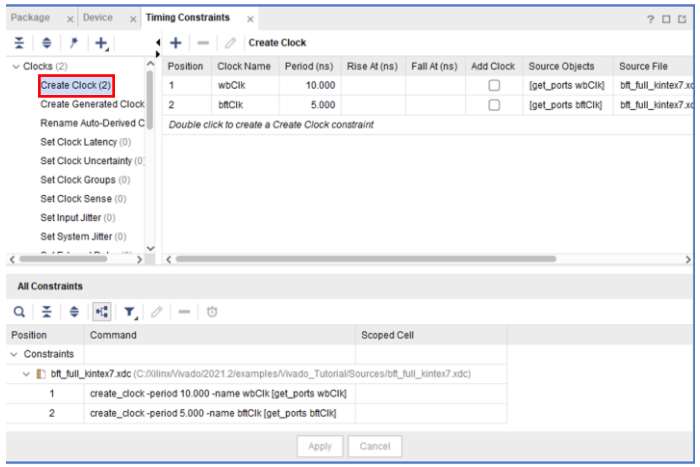


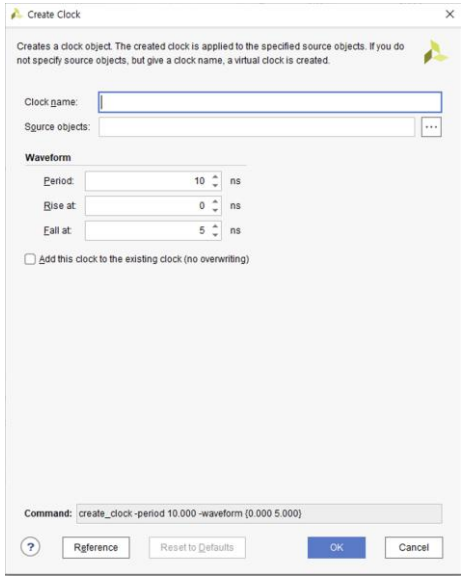


Step 5: Defining Timing Constraints and I/O Planning

- Timing Constraints 정의
  - Window > Timing Constraints
  - tree view of the different types of constraints
    - Timing constraint를 빠르게 찾을 수 있음
  - wbClk, bftClk
    - 현재 정의된 값들은 편집 기능으로 수정 가능

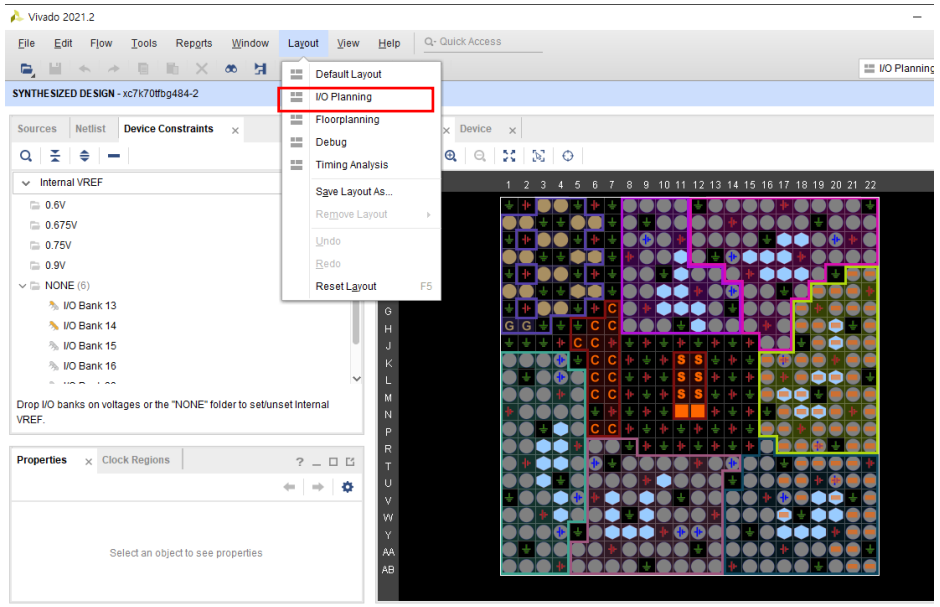
- Create Clock wizard
  - Timing constraints의 왼쪽 트리에서 Clocks의 Create Clock을 더블 클릭
  - Clock constraints를 정의하는 데에 사용
  - 아래의 command 라인은 Tcl 명령어로 실행될 XDC 명령어를 표시

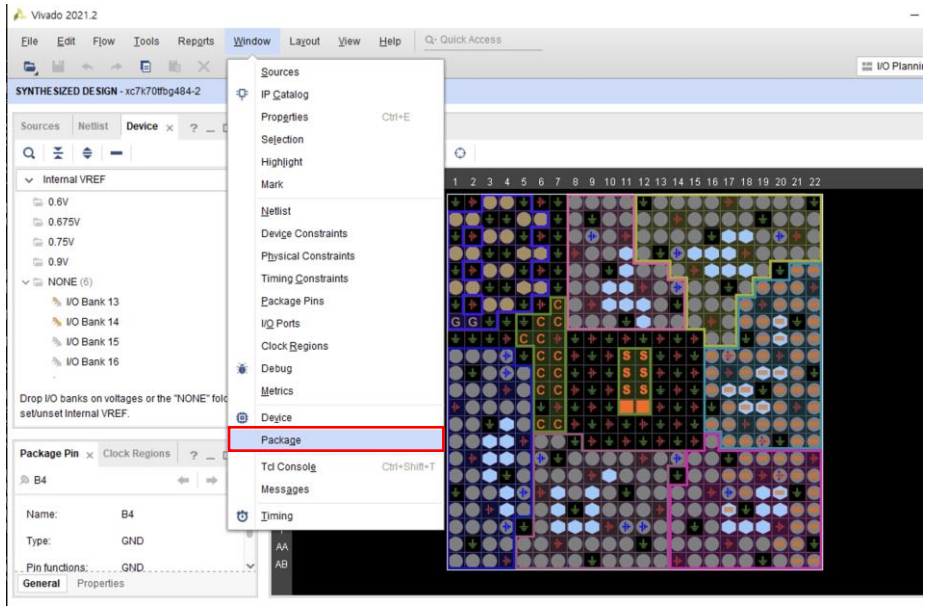




Step 5: Defining Timing Constraints and I/O Planning

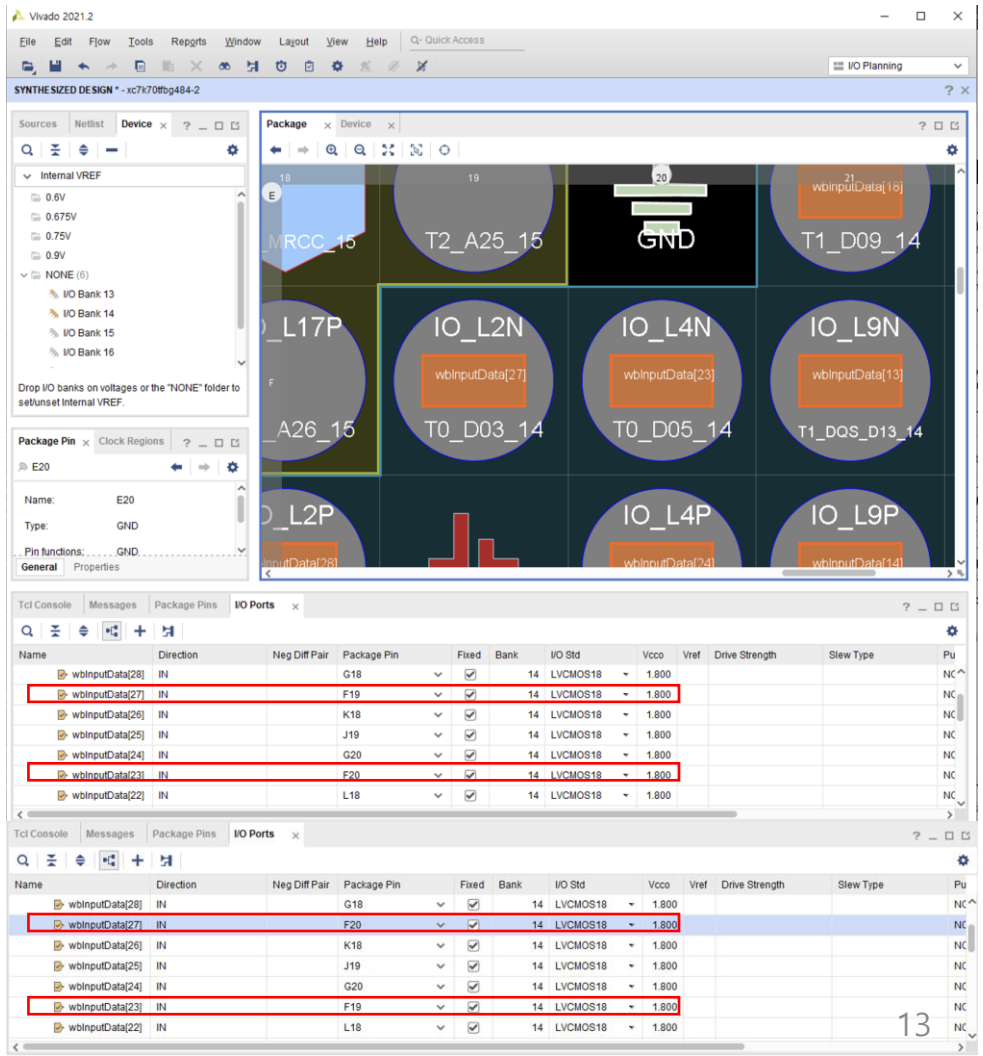
- I/O Planning
  - I/O Planning view layout
    - Layout Selector – I/O Planning
  - Package window
    - Package window 활성화
    - Windows – Package





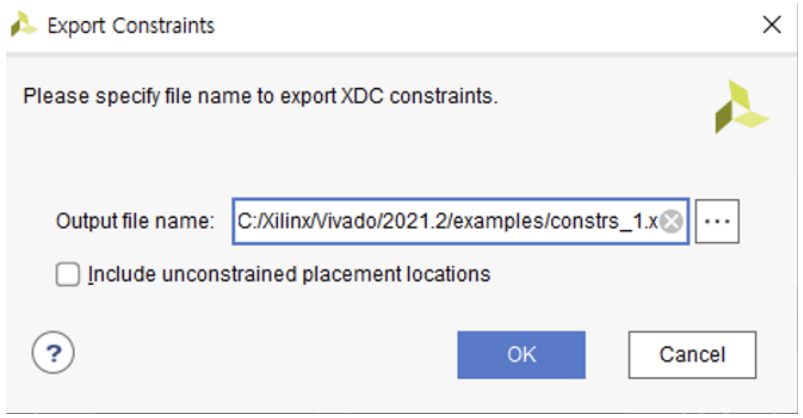
Step 5: Defining Timing Constraints and I/O Planning

- Examine the I/O Ports window
  - I/O Port안의 box
  - Package window에서 I/O port에 있는 오렌지색 블록을 더블클릭하여 선택
  - Inputdata선 [27], [23]이 각각 패키지 핀 번호 F19, F20에 위치해 있음을 확인
  - 드래그하여 오렌지색 블록을 서로 바꿔 위치시킴
  - I/O Ports에서 확인
    - 포트 이름, 패키지 핀에 대한 행들



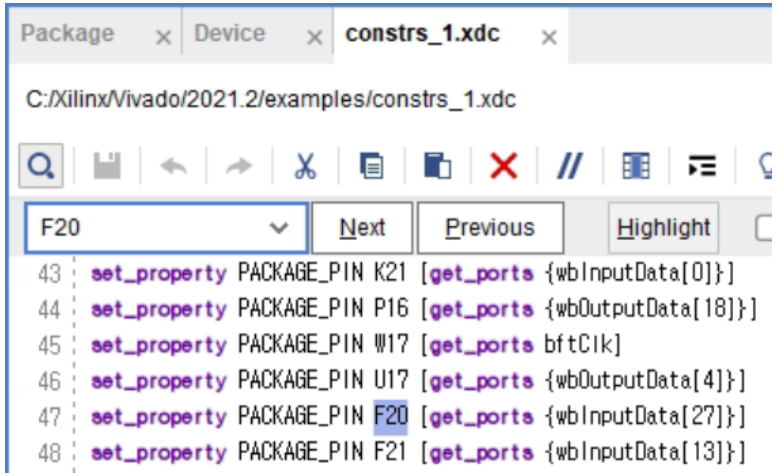
Step 6: Exporting the Modified Constraints

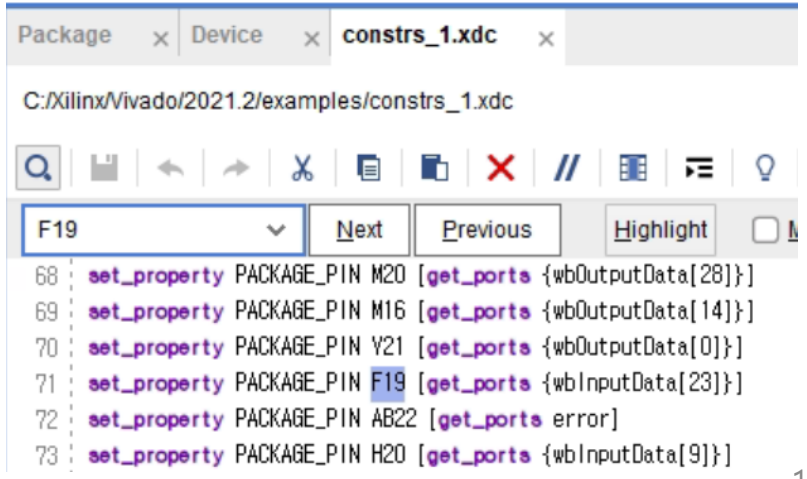
- Export Constraints
  - File – Export – Export Constraints
  - 수정된 XDC constraints 파일을 출력



- Constraints file
  - File – Text Editor – Open File
  - Export한 파일을 찾아 open
  - 파일에서 변경된 부분을 확인

- Stop_gui





Step 7: Implementing the Design

- Create_bft_kintex7_batch.tcl

  - **Opt_design**
  - **place_design**
  - **phys_opt_design**
  - Write_checkpoint –force $outputDir/post_place
  - Report_timing_summary –file $outputDir/post_place_timing_summary.겟

  - **route_design**
  - Write_checkpoint –force $outputDir/post_route
  - Report_timing_summary –file $outputDir/post_route_timing_summary.겟
  - report_timing –sort_by group –max_paths 100 –path_type summary –file $outputDir/post_route_timing.겟

  - report_clock_utilization -file $outputDir/clock_util.rpt
  - report_utilization -file $outputDir/post_route_util.rpt
  - report_power -file $outputDir/post_route_power.rpt
  - report_drc -file $outputDir/post_imp_drc.겟

  - write_verilog -force $outputDir/bft_impl_netlist.v
  - write_xdc -no_fixed_only -force $outputDir/bft_impl.xdc
  - **write_bitstream -force $outputDir/bft.bit**

Step 7: Implementing the Design

opt_design

```
Vivado 2021.2 Tcl Shell - C:₩Xilinx₩Vivado₩2021.2₩bin₩vivado.bat -mode tcl

C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output/post_synth_high_fanout_nets.rpt
Vivado% opt_design
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7k70t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7k70t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 2 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.805 . Memory (MB): peak = 2339.406 ; gain = 0.000

Starting Cache Timing Information Task
Ending Cache Timing Information Task | Checksum: e262e4e1

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 2339.406 ; gain = 0.000

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: e262e4e1

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.148 . Memory (MB): peak = 2520.023 ; gain = 0.000
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: e262e4e1

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.186 . Memory (MB): peak = 2520.023 ; gain = 0.000
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: e6425d34

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.278 . Memory (MB): peak = 2520.023 ; gain = 0.000
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 224 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: e6425d34

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.377 . Memory (MB): peak = 2520.023 ; gain = 0.000
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization
INFO: [Opt 31-1064] SRL Remap converted 0 SRLs to 0 registers and converted 0 registers of register chains to 0 SRLs
Phase 5 Shift Register Optimization | Checksum: e6425d34

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.386 . Memory (MB): peak = 2520.023 ; gain = 0.000
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: e6425d34

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.396 . Memory (MB): peak = 2520.023 ; gain = 0.000
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells
Opt_design Change Summary
```

place_design

```
Vivado 2021.2 Tcl Shell - C:₩Xilinx₩Vivado₩2021.2₩bin₩vivado.bat -mode tcl
0
Vivado% place_design
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7k70t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7k70t'
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [DRC 23-27] Running DRC with 2 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 2 threads
WARNING: [DRC CHECK-3] Report rule limit reached: REQP-1839 rule limit reached: 20 violations have been found.
WARNING: [DRC REQP-1839] RAMB36 async control check: The RAMB36E1 egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_
ram_performance.fifo_ram_reg has an input control pin egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_ram_performa
nce.fifo_ram_reg/ADDRARDADDR[10] (net: egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr[5]) which is driven by a
register (egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr_reg[5]) that has an active asychronous set or reset. T
his may cause corruption of the memory contents and/or read values when the set/reset is asserted and is not analyzed by
the default static timing analysis. It is suggested to eliminate the use of a set/reset to registers driving this RAMB
pin or else use a synchronous reset in which the assertion of the reset is timed by default.
WARNING: [DRC REQP-1839] RAMB36 async control check: The RAMB36E1 egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_
ram_performance.fifo_ram_reg has an input control pin egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_ram_performa
nce.fifo_ram_reg/ADDRARDADDR[11] (net: egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr[6]) which is driven by a
register (egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr_reg[6]) that has an active asychronous set or reset. T
his may cause corruption of the memory contents and/or read values when the set/reset is asserted and is not analyzed by
the default static timing analysis. It is suggested to eliminate the use of a set/reset to registers driving this RAMB
pin or else use a synchronous reset in which the assertion of the reset is timed by default.
WARNING: [DRC REQP-1839] RAMB36 async control check: The RAMB36E1 egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_
ram_performance.fifo_ram_reg has an input control pin egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_ram_performa
nce.fifo_ram_reg/ADDRARDADDR[12] (net: egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr[7]) which is driven by a
register (egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr_reg[7]) that has an active asychronous set or reset. T
his may cause corruption of the memory contents and/or read values when the set/reset is asserted and is not analyzed by
the default static timing analysis. It is suggested to eliminate the use of a set/reset to registers driving this RAMB
pin or else use a synchronous reset in which the assertion of the reset is timed by default.
WARNING: [DRC REQP-1839] RAMB36 async control check: The RAMB36E1 egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_
ram_performance.fifo_ram_reg has an input control pin egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_ram_performa
nce.fifo_ram_reg/ADDRARDADDR[13] (net: egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr[8]) which is driven by a
register (egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr_reg[8]) that has an active asychronous set or reset. T
his may cause corruption of the memory contents and/or read values when the set/reset is asserted and is not analyzed by
the default static timing analysis. It is suggested to eliminate the use of a set/reset to registers driving this RAMB
pin or else use a synchronous reset in which the assertion of the reset is timed by default.
WARNING: [DRC REQP-1839] RAMB36 async control check: The RAMB36E1 egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_
ram_performance.fifo_ram_reg has an input control pin egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_ram_performa
nce.fifo_ram_reg/ADDRARDADDR[14] (net: egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr[9]) which is driven by a
register (egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr_reg[9]) that has an active asychronous set or reset. T
his may cause corruption of the memory contents and/or read values when the set/reset is asserted and is not analyzed by
the default static timing analysis. It is suggested to eliminate the use of a set/reset to registers driving this RAMB
pin or else use a synchronous reset in which the assertion of the reset is timed by default.
WARNING: [DRC REQP-1839] RAMB36 async control check: The RAMB36E1 egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_
ram_performance.fifo_ram_reg has an input control pin egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_ram_performa
nce.fifo_ram_reg/ADDRARDADDR[5] (net: egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr[0]) which is driven by a r
egister (egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr_reg[0]) that has an active asychronous set or reset. Th
is may cause corruption of the memory contents and/or read values when the set/reset is asserted and is not analyzed by
the default static timing analysis. It is suggested to eliminate the use of a set/reset to registers driving this RAMB p
in or else use a synchronous reset in which the assertion of the reset is timed by default.
WARNING: [DRC REQP-1839] RAMB36 async control check: The RAMB36E1 egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_
ram_performance.fifo_ram_reg has an input control pin egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_ram_performa
nce.fifo_ram_reg/ADDRARDADDR[6] (net: egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr[1]) which is driven by a r
egister (egressLoop[0].egressFifo/buffer_fifo/infer_fifo.wr_addr_reg[1]) that has an active asychronous set or reset. Th
is may cause corruption of the memory contents and/or read values when the set/reset is asserted and is not analyzed by
the default static timing analysis. It is suggested to eliminate the use of a set/reset to registers driving this RAMB p
in or else use a synchronous reset in which the assertion of the reset is timed by default.
WARNING: [DRC REQP-1839] RAMB36 async control check: The RAMB36E1 egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_
ram_performance.fifo_ram_reg has an input control pin egressLoop[0].egressFifo/buffer_fifo/infer_fifo.block_ram_performa
```

phys_opt_design

```
Vivado% phys_opt_design
Command: phys_opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7k70t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7k70t'
INFO: [Vivado_Tcl 4-383] Design worst setup slack (WNS) is greater than or equal to 0.000 ns. Skipping all physical synt
hesis optimizations.
INFO: [Vivado_Tcl 4-232] No setup violation found. The netlist was not modified.
INFO: [Common 17-83] Releasing license: Implementation
4 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
phys_opt_design completed successfully
```

checkpoint

```
Vivado% write_checkpoint -force $outputDir/post_place
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.209 . Memory (MB): peak = 2606.148 ; gain = 0.000
INFO: [Common 17-1381] The checkpoint 'C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output
/post_place.dcp' has been generated.
C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output/post_place.dcp
```

Timing summary

```
Vivado% report_timing_summary -file $outputDir/post_place_timing_summary.rpt
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -2, Delay Type: min_max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
```

Step 7: Implementing the Design

Route_design

```
Vivado 2021.2 Tcl Shell - C:₩Xilinx₩Vivado₩2021.2₩bin₩vivado.bat -mode tcl
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.208 . Memory (MB): peak = 2606.148 ; gain = 0.000
INFO: [Common 17-1381] The checkpoint 'C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output
/post_place.dcp' has been generated.
C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output/post_place.dcp
Vivado% report_timing_summary -file $outputDir/post_place_timing_summary.rpt
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -2, Delay Type: min_max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
Vivado% route_design
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7k70t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7k70t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 2 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.


Starting Routing Task
INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs

Phase 1 Build RT Design
Checksum: PlaceDB: ca47dc11 ConstDB: 0 ShapeSum: 8eaffldc RouteDB: 0
Post Restoration Checksum: NetGraph: 316c6bf0 NumContArr: fc94caed Constraints: 0 Timing: 0
Phase 1 Build RT Design | Checksum: 12e0226dd

Time (s): cpu = 00:00:09 ; elapsed = 00:00:06 . Memory (MB): peak = 2606.148 ; gain = 0.000

Phase 2 Router Initialization

Phase 2.1 Create Timer
Phase 2.1 Create Timer | Checksum: 12e0226dd

Time (s): cpu = 00:00:09 ; elapsed = 00:00:06 . Memory (MB): peak = 2606.148 ; gain = 0.000

Phase 2.2 Fix Topology Constraints
Phase 2.2 Fix Topology Constraints | Checksum: 12e0226dd

Time (s): cpu = 00:00:09 ; elapsed = 00:00:07 . Memory (MB): peak = 2606.148 ; gain = 0.000

Phase 2.3 Pre Route Cleanup
Phase 2.3 Pre Route Cleanup | Checksum: 12e0226dd

Time (s): cpu = 00:00:09 ; elapsed = 00:00:07 . Memory (MB): peak = 2606.148 ; gain = 0.000
 Number of Nodes with overlaps = 0

Phase 2.4 Update Timing
Phase 2.4 Update Timing | Checksum: 110c2fb44

Time (s): cpu = 00:00:10 ; elapsed = 00:00:07 . Memory (MB): peak = 2606.148 ; gain = 0.000
INFO: [Route 35-416] Intermediate Timing Summary | WNS=1.917  | TNS=0.000  | WHS=-0.361 | THS=-157.618|


Router Utilization Summary
  Global Vertical Routing Utilization    = 0 %
  Global Horizontal Routing Utilization  = 0 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets                  = 5181
    (Failed Nets is the sum of unrouted and partially routed nets)
  Number of Unrouted Nets                = 5181
  Number of Partially Routed Nets        = 0
```

Checkpoint

```
Vivado% write_checkpoint -force $outputDir/post_route
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.306 . Memory (MB): peak = 2606.148 ; gain = 0.000
INFO: [Common 17-1381] The checkpoint 'C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output
/post_route.dcp' has been generated.
C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output/post_route.dcp
```

Timing summary

```
Vivado% report_timing_summary -file $outputDir/post_route_timing_summary.rpt
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -2, Delay Type: min_max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
```

Timing sort by group

```
Vivado% report_timing -max_paths 100 -path_type summary -slack_lesser_than 0 -file $outputDir/post_route_setup_timing_vi
olations.rpt
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -2, Delay Type: max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
INFO: [Timing 38-78] ReportTimingParams: -max_paths 100 -nworst 1 -delay_type max -sort_by slack.
WARNING: [Timing 38-164] This design has multiple clocks. Inter clock paths are considered valid unless explicitly exclu
ded by timing constraints such as set_clock_groups or set_false_path.
INFO: [Timing 38-72] No paths found.
```

Clock Utilization

```
Vivado% report_clock_utilization -file $outputDir/clock_util.rpt
C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output/clock_util.rpt
```

power

```
Vivado% report_power -file $outputDir/post_route_power.rpt
Command: report_power -file ./Tutorial_Created_Data/bft_output/post_route_power.rpt
Running Vector-less Activity Propagation...
```

DRC(design rule checks)

```
Vivado% report_drc -file $outputDir/post_imp_drc.rpt
Command: report_drc -file ./Tutorial_Created_Data/bft_output/post_imp_drc.rpt
INFO: [IP_Flow 19-1839] IP Catalog is up to date.
INFO: [DRC 23-27] Running DRC with 2 threads
INFO: [Vivado_Tcl 2-168] The results of DRC are in file C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Create
d_Data/bft_output/post_imp_drc.rpt.
report_drc completed successfully
0
```

Step 7: Implementing the Design

Write_Verilog

```
Vivado% write_verilog -force $outputDir/bft_impl_netlist.v
C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output/bft_impl_netlist.v
```

write_xdc

```
Vivado% write_xdc -no_fixed_only -force $outputDir/bft_impl.xdc
C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/bft_output/bft_impl.xdc
```

write_bitstream

```
선택 Vivado 2021.2 Tcl Shell - C:₩Xilinx₩Vivado₩2021.2₩bin₩vivado.bat -mode tcl
Time (s): cpu = 00:00:15 ; elapsed = 00:00:11 . Memory (MB): peak = 2515.203 ; gain = 0.000

Routing is Done.
INFO: [Common 17-83] Releasing license: Implementation
12 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:17 ; elapsed = 00:00:12 . Memory (MB): peak = 2515.203 ; gain = 0.000
Vivado% write_bitstream -force $outputDir/bft.bit
Command: write_bitstream -force ./Tutorial_Created_Data/bft_output/bft.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7k70t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7k70t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-1839] IP Catalog is up to date.
INFO: [DRC 23-27] Running DRC with 2 threads
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG_VOLTAGE volta
ge property is set in the current_design.  Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CO
NFIG_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pin
s in bank 0.  It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly
 in the XDC file using the following syntax:

 set_property CFGBVS value1 [current_design]
 #where value1 is either VCCO or GND

 set_property CONFIG_VOLTAGE value2 [current_design]
 #where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
WARNING: [DRC CHECK-3] Report rule limit reached: REQP-1839 rule limit reached: 20 violations have been found.
WARNING: [DRC DPOP-2] MREG Output pipelining: DSP arnd1/transformLoop[0].ct/xOutReg_reg multiplier stage arnd1/transform
Loop[0].ct/xOutReg_reg/P[47:0] is not pipelined (MREG=0). Pipelining the multiplier function will improve performance an
d will save significant power so it is suggested whenever possible to fully pipeline this function.  If this multiplier
was inferred, it is suggested to describe an additional register stage after this function.  If there is no registered a
dder/accumulator following the multiply function, two pipeline stages are suggested to allow both the MREG and PREG regi
sters to be used.  If the DSP48 was instantiated in the design, it is suggested to set both the MREG and PREG attributes
 to 1 when performing multiply functions.
WARNING: [DRC DPOP-2] MREG Output pipelining: DSP arnd1/transformLoop[0].ct/xOutStepReg_reg multiplier stage arnd1/trans
formLoop[0].ct/xOutStepReg_reg/P[47:0] is not pipelined (MREG=0). Pipelining the multiplier function will improve perfor
mance and will save significant power so it is suggested whenever possible to fully pipeline this function.  If this mul
tiplier was inferred, it is suggested to describe an additional register stage after this function.  If there is no regi
stered adder/accumulator following the multiply function, two pipeline stages are suggested to allow both the MREG and P
REG registers to be used.  If the DSP48 was instantiated in the design, it is suggested to set both the MREG and PREG at
tributes to 1 when performing multiply functions.
WARNING: [DRC DPOP-2] MREG Output pipelining: DSP arnd1/transformLoop[1].ct/xOutReg_reg multiplier stage arnd1/transform
Loop[1].ct/xOutReg_reg/P[47:0] is not pipelined (MREG=0). Pipelining the multiplier function will improve performance an
d will save significant power so it is suggested whenever possible to fully pipeline this function.  If this multiplier
was inferred, it is suggested to describe an additional register stage after this function.  If there is no registered a
dder/accumulator following the multiply function, two pipeline stages are suggested to allow both the MREG and PREG regi
sters to be used.  If the DSP48 was instantiated in the design, it is suggested to set both the MREG and PREG attributes
 to 1 when performing multiply functions.
WARNING: [DRC DPOP-2] MREG Output pipelining: DSP arnd1/transformLoop[1].ct/xOutStepReg_reg multiplier stage arnd1/trans
formLoop[1].ct/xOutStepReg_reg/P[47:0] is not pipelined (MREG=0). Pipelining the multiplier function will improve perfor
mance and will save significant power so it is suggested whenever possible to fully pipeline this function.  If this mul
tiplier was inferred, it is suggested to describe an additional register stage after this function.  If there is no regi
stered adder/accumulator following the multiply function, two pipeline stages are suggested to allow both the MREG and P
REG registers to be used.  If the DSP48 was instantiated in the design, it is suggested to set both the MREG and PREG at
tributes to 1 when performing multiply functions.
WARNING: [DRC DPOP-2] MREG Output pipelining: DSP arnd1/transformLoop[2].ct/xOutReg_reg multiplier stage arnd1/transform
Loop[2].ct/xOutReg_reg/P[47:0] is not pipelined (MREG=0). Pipelining the multiplier function will improve performance an
d will save significant power so it is suggested whenever possible to fully pipeline this function.  If this multiplier
was inferred, it is suggested to describe an additional register stage after this function.  If there is no registered a
dder/accumulator following the multiply function, two pipeline stages are suggested to allow both the MREG and PREG regi
sters to be used.  If the DSP48 was instantiated in the design, it is suggested to set both the MREG and PREG attributes
 to 1 when performing multiply functions.
```

Step 7: Implementing the Design

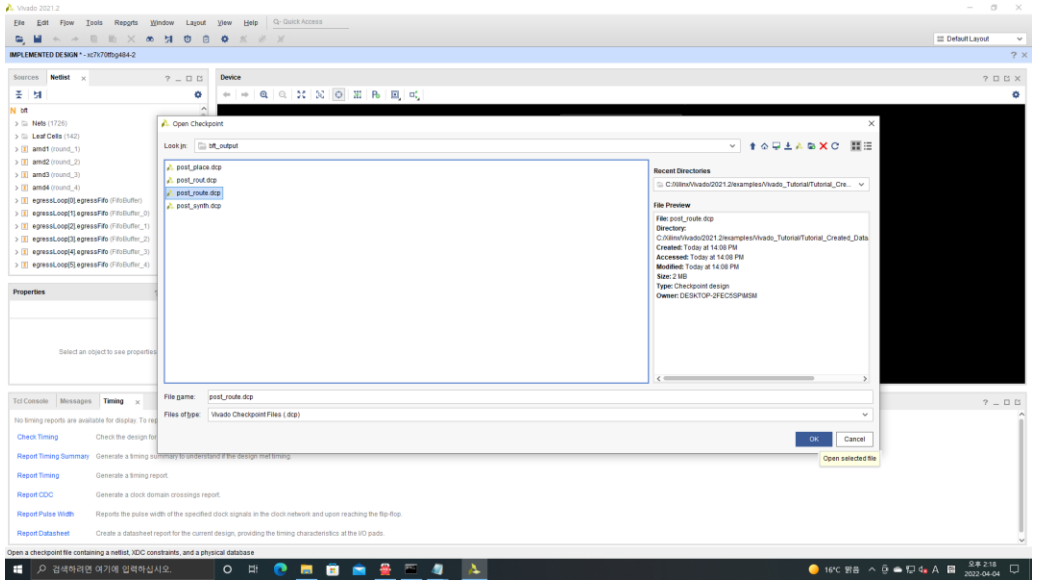
- Output 디렉토리에 있는 files
  - 비바도/Vivado_Tutorial/Tutorial_Created_Data/bft_output
  - Bft_impl.xdc 파일
  - Implement된 design에 아까 우리가 수정했던 I/O port constraint가 똑같이 바뀌었는지 확인

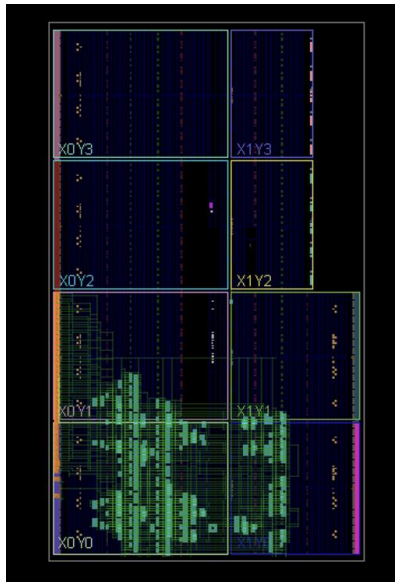
```
set_property PACKAGE_PIN AB21 [get_ports wbWriteOut]
set_property PACKAGE_PIN M21 [get_ports {wbOutputData[29]}]
set_property PACKAGE_PIN R22 [get_ports {wbOutputData[15]}]
set_property PACKAGE_PIN U20 [get_ports {wbOutputData[1]}]
set_property PACKAGE_PIN G20 [get_ports {wbInputData[24]}]
set_property PACKAGE_PIN J20 [get_ports {wbInputData[10]}]
set_property PACKAGE_PIN AA21 [get_ports wbDataForOutput]
set_property PACKAGE_PIN M20 [get_ports {wbOutputData[28]}]
set_property PACKAGE_PIN M16 [get_ports {wbOutputData[14]}]
set_property PACKAGE_PIN Y21 [get_ports {wbOutputData[0]}]
set_property PACKAGE_PIN F19 [get_ports {wbInputData[23]}]
```

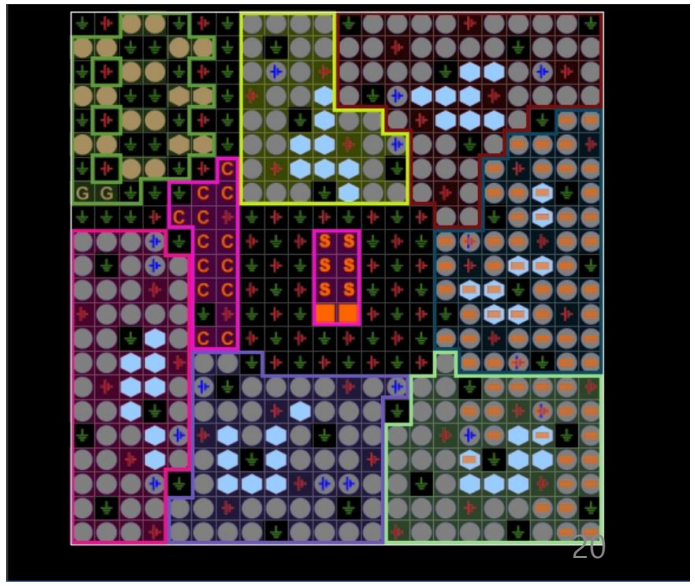
```
set_property PACKAGE_PIN W22 [get_ports {wbOutputData[5]}]
set_property PACKAGE_PIN V20 [get_ports wbClk]
set_property PACKAGE_PIN G18 [get_ports {wbInputData[28]}]
set_property PACKAGE_PIN G21 [get_ports {wbInputData[14]}]
set_property PACKAGE_PIN K21 [get_ports {wbInputData[0]}]
set_property PACKAGE_PIN P16 [get_ports {wbOutputData[18]}]
set_property PACKAGE_PIN W17 [get_ports bftClk]
set_property PACKAGE_PIN U17 [get_ports {wbOutputData[4]}]
set_property PACKAGE_PIN F20 [get_ports {wbInputData[27]}]
set_property PACKAGE_PIN F21 [get_ports {wbInputData[13]}]
set_property PACKAGE_PIN K22 [get_ports {wbOutputData[31]}]
```

Step 8: Opening a Design Checkpoint

- Design checkpoint
  - VIVADO IDE
    - 저장된 design checkpoint 열기 가능
    - IDE의 시각화와 분석 기능 사용 가능
  - Start_gui
  - File – Checkpoint – Open
  - 비바도/Vivado_Tutorial/Tutorial_Created_Data/bft_output/
  - post_route.dcp



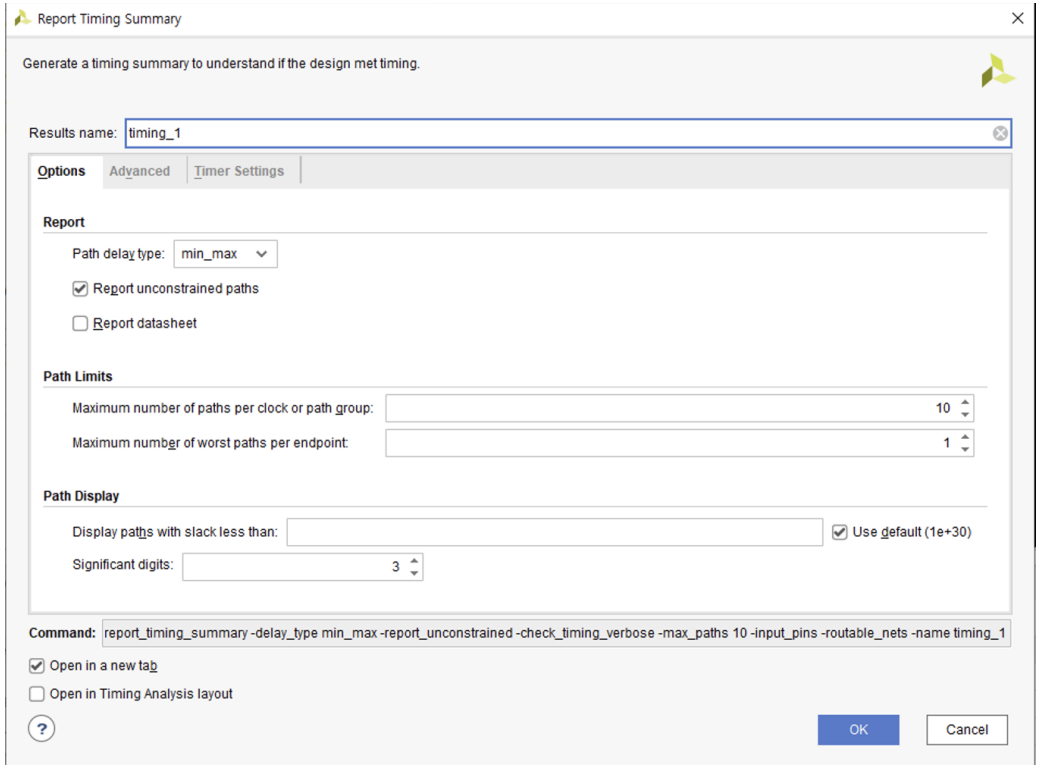




Step 9: Analyzing Implementation Results

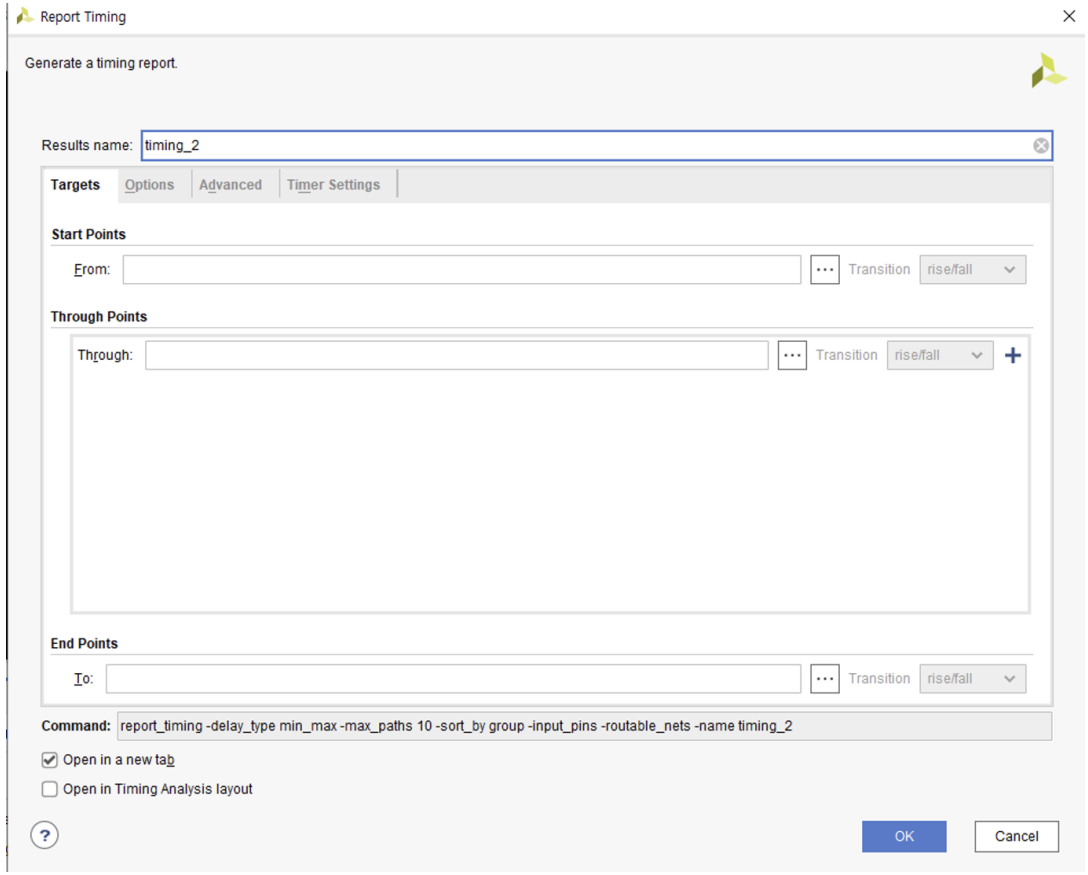
- Vivado를 통해 design과 device data에 관한 다양한 분석
  - Power, timing, utilization, clocks 등의 기본적인 특성 뿐만 아니라 Tcl API를 통해 원하는 특성들을 커스텀하여 추출 가능

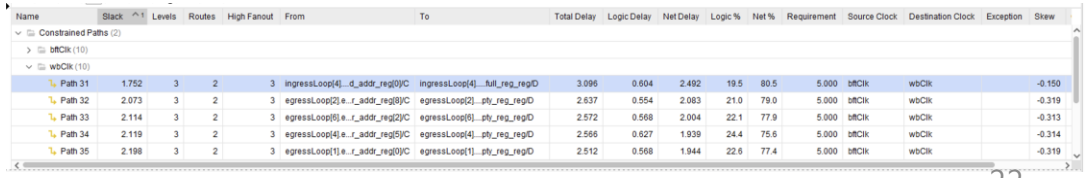
- Report timing summary
  - Device window tab
  - Reports – timing – report timing summary
  - Timing summary window에서 setup, hold, pulse width와 관련된 정보



Step 9: Analyzing Implementation Results

- Report timing
  - Timing 분석 수행
  - Reports – timing – report timing
  - wbClk
    - 첫번째 패스 선택





Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception	Skew
Constrained Paths (2)																
bftClk (10)																
wbClk (10)																
Path 31	1.752	3	2	3	ingressLoop[4]...d_addr_reg[0]/C	ingressLoop[4]....full_reg_reg/D	3.096	0.604	2.492	19.5	80.5	5.000	bftClk	wbClk		-0.150
Path 32	2.073	3	2	3	egressLoop[2]:e...r_addr_reg[8]/C	egressLoop[2]...pty_reg_reg/D	2.637	0.554	2.083	21.0	79.0	5.000	bftClk	wbClk		-0.319
Path 33	2.114	3	2	3	egressLoop[6]:e...r_addr_reg[2]/C	egressLoop[6]...pty_reg_reg/D	2.572	0.568	2.004	22.1	77.9	5.000	bftClk	wbClk		-0.313
Path 34	2.119	3	2	3	egressLoop[4]:e...r_addr_reg[5]/C	egressLoop[4]...pty_reg_reg/D	2.566	0.627	1.939	24.4	75.6	5.000	bftClk	wbClk		-0.314
Path 35	2.198	3	2	3	egressLoop[1]:e...r_addr_reg[0]/C	egressLoop[1]...pty_reg_reg/D	2.512	0.568	1.944	22.6	77.4	5.000	bftClk	wbClk		-0.319

Step 9: Analyzing Implementation Results

- Path properties window
  - The path details
  - Window floating: restore 버튼이나 dock 버튼

Path 31 - timing_1

Summary

Name	Path 31
Slack	1.752ns
Source	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.rd_addr_reg[0]/C (rising edge-triggered cell FDCE clocked by bftClk {rise@0.000ns fall@2.500ns period=5.000ns})
Destination	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.full_reg_reg/D (rising edge-triggered cell FDCE clocked by wbClk {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	wbClk
Path Type	Setup (Max at Slow Process Corner)
Requirement	5.000ns (wbClk rise@10.000ns - bftClk rise@5.000ns)
Data Path Delay	3.096ns (logic 0.604ns (19.507%) route 2.492ns (80.493%))
Logic Levels	3 (CARRY4=1 LUT4=1 LUT6=1)
Clock Path Skew	-0.150ns
Clock Uncertainty	0.035ns
Clock Dom...Crossing	Inter clock paths are considered valid unless explicitly excluded by timing constraints such as set_clock_groups or set_false_path.

Show clock path skew equation for -0.150ns

Source Clock Path

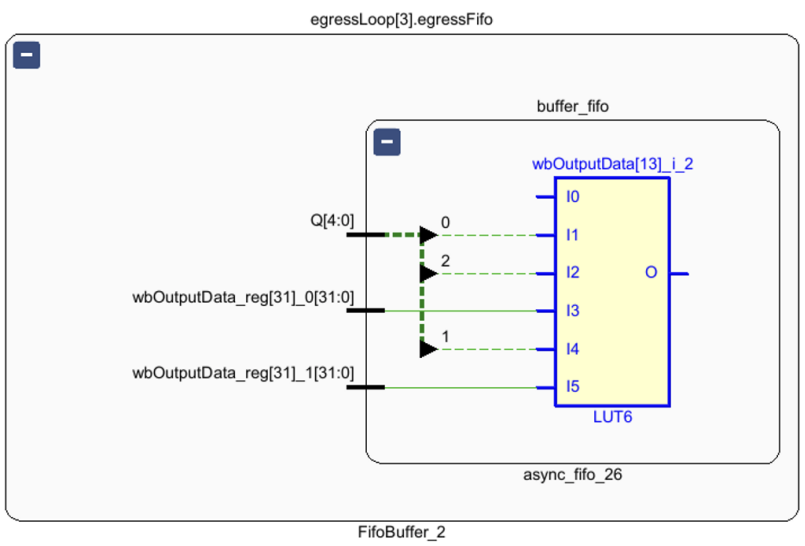
Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
(clock bftClk rise edge)	(r) 5.000	5.000		
	(r) 0.000	5.000	Site: W17	bftClk
net (fo=0)	0.000	5.000		bftClk
			Site: W17	bftClk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.749	5.749	Site: W17	bftClk_IBUF_inst/O
net (fo=1, routed)	1.901	7.650		bftClk_IBUF
			Site: BUF...TRL_X0Y0	bftClk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.093	7.743	Site: BUF...TRL_X0Y0	bftClk_IBUF_BUFG_inst/O
net (fo=730, routed)	1.222	8.965		ingressLoop[4].ingressFifo/buffer_fifo/clk
FDCE			Site: SLICE_X44Y50	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.rd_addr_reg[0]/C

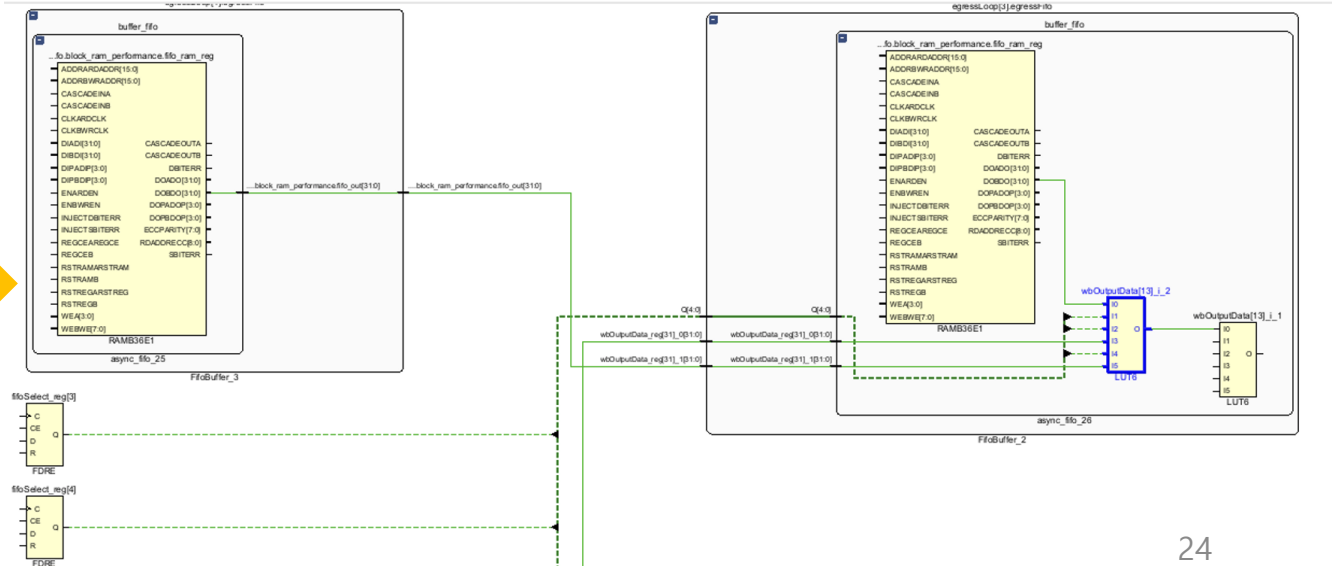
Data Path

Delay Type	Incr (ns)	Path (...	Location	Netlist Resource(s)
FDCE (Prop_fdce_C_Q)	(r) 0.259	9.224	Site: SLICE_X44Y50	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.rd_addr_reg[0]/Q
net (fo=3, routed)	1.583	10.807		ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.rd_addr[0]
			Site: SLICE_X43Y50	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.empty_reg_reg2_carry_i_4__3/I1
LUT6 (Prop_lut6_I1_O)	(r) 0.043	10.850	Site: SLICE_X43Y50	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.empty_reg_reg2_carry_i_4__3/O
net (fo=1, routed)	0.000	10.850		ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.empty_reg_reg2_carry_i_4__3_n_0
			Site: SLICE_X43Y50	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.empty_reg_reg2_carry/S[0]
CARRY4 (Prop_c...4_S[0]_CO[3])	(r) 0.259	11.109	Site: SLICE_X43Y50	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.empty_reg_reg2_carry/CO[3]
net (fo=2, routed)	0.909	12.019		ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.empty_reg_reg2
			Site: SLICE_X40Y48	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.full_reg_i_1__5/I2
LUT4 (Prop_lut4_I2_O)	(r) 0.043	12.062	Site: SLICE_X40Y48	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.full_reg_i_1__5/O
net (fo=1, routed)	0.000	12.062		ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.full_reg_reg0
FDCE			Site: SLICE_X40Y48	ingressLoop[4].ingressFifo/buffer_fifo/infer_fifo.full_reg_reg/D
Arrival Time		12.062		

Step 9: Analyzing Implementation Results

- Schematic
  - Report timing window에서 마우스의 오른쪽을 클릭하여 Schematic을 실행 (or F4)
  - 셀, 와이어, 핀같은 schematic 요소를 더블 클릭하여 schematic 연결과 구조를 확장 가능

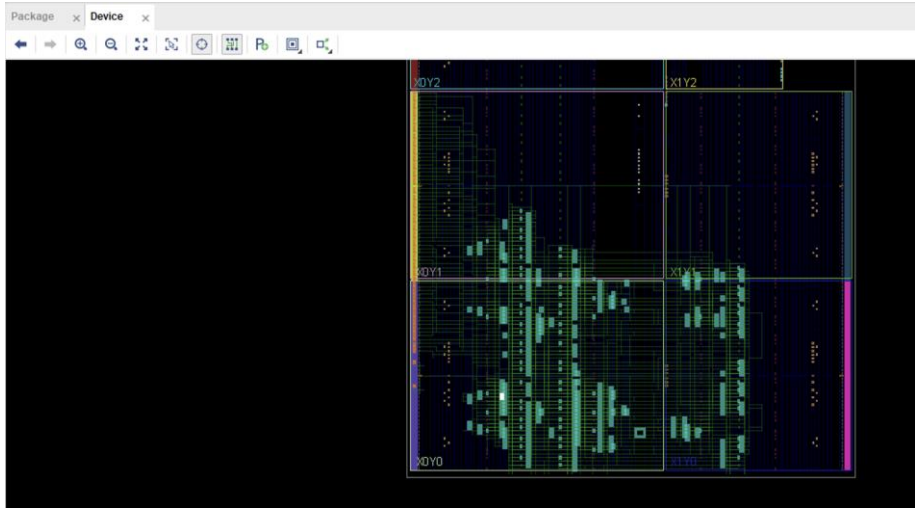


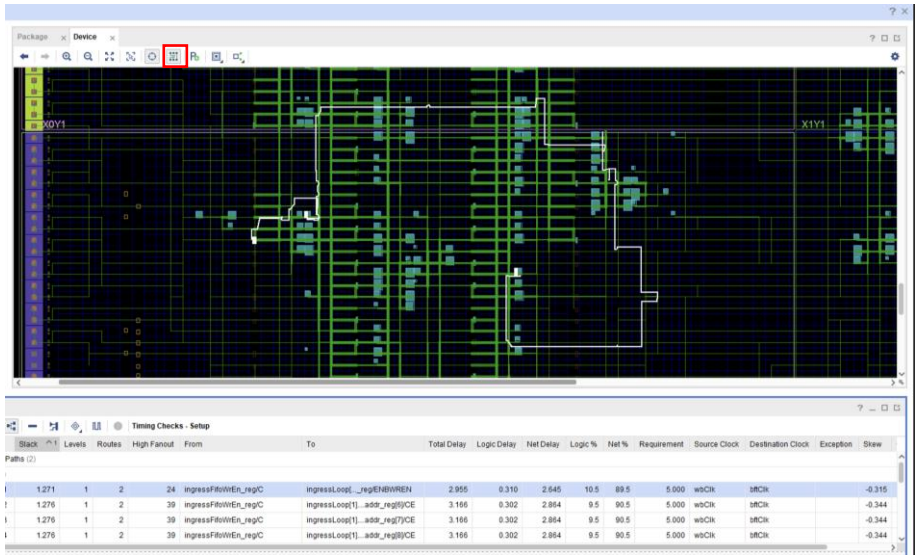


Step 9: Analyzing Implementation Results

- 그 후, Schematic 닫기
- Device window tab 클릭

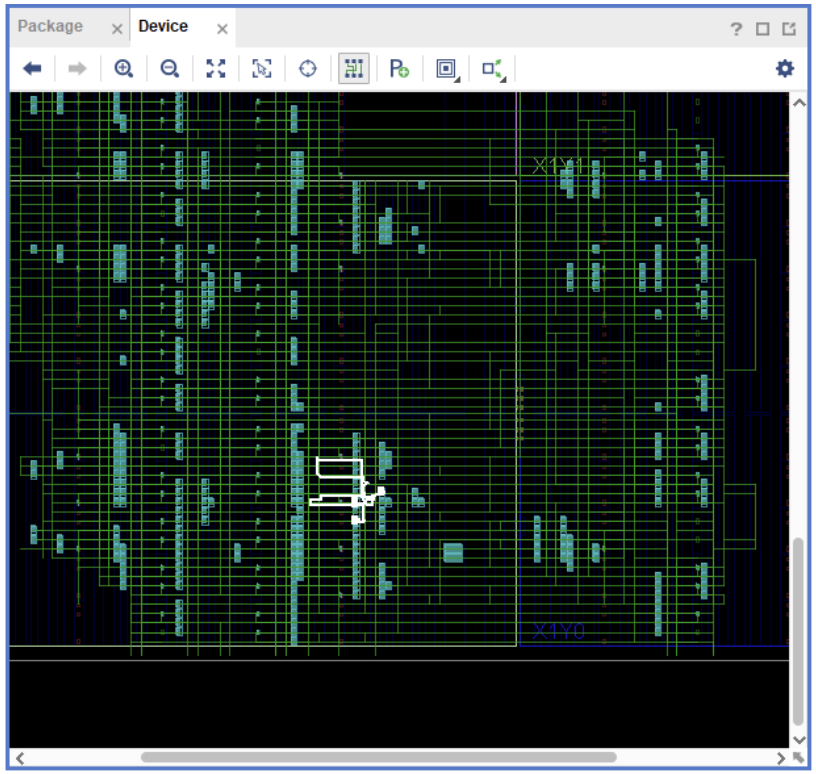
- Routing Resources button
  - 자세한 device routing을 보여줌
  - 선택한 path들에 대한 routing을 하얀색으로 표시

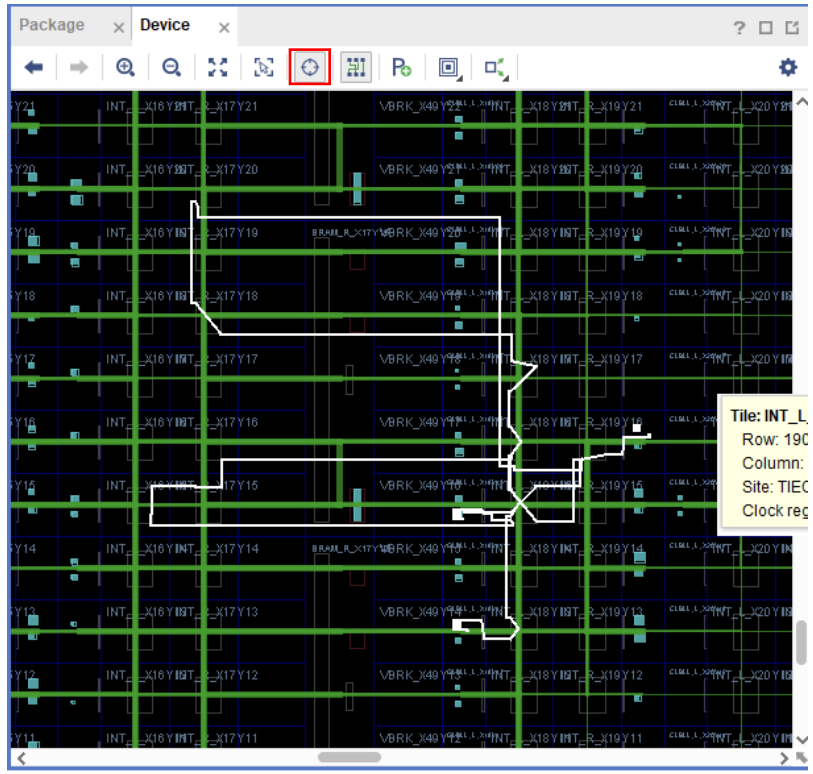




Step 9: Analyzing Implementation Results

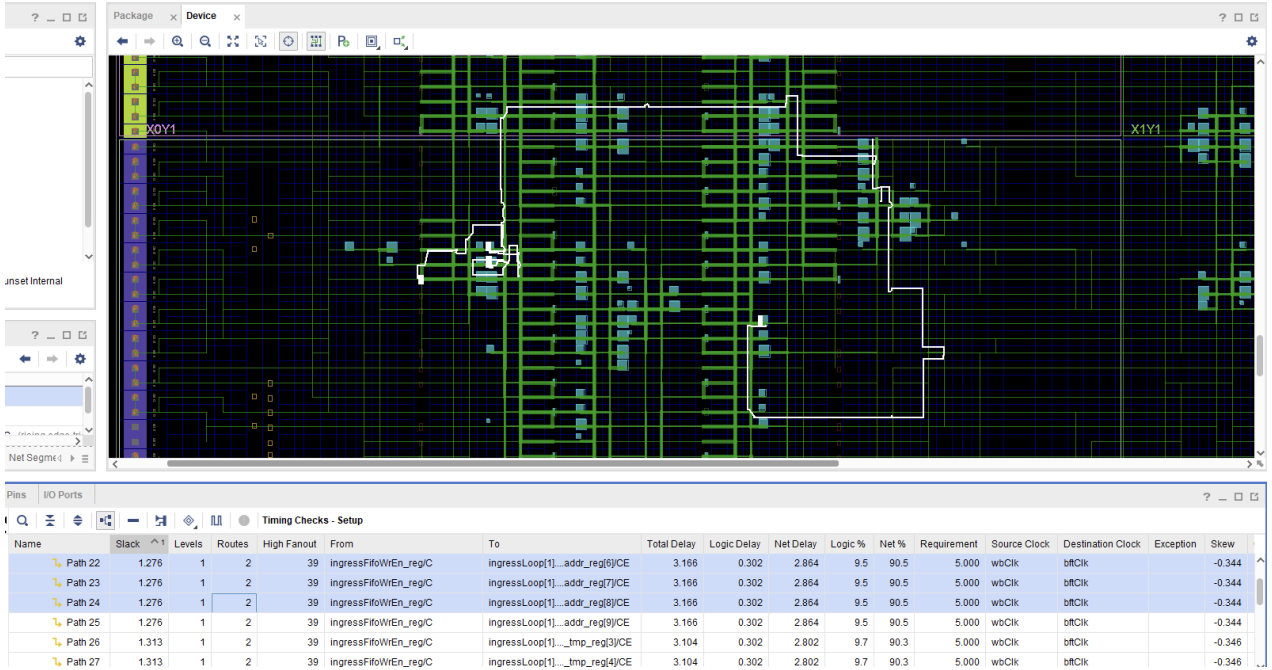
- Auto-fit Selection
- 선택한 객체의 크기에 알맞게 자동으로 zoom





Step 9: Analyzing Implementation Results

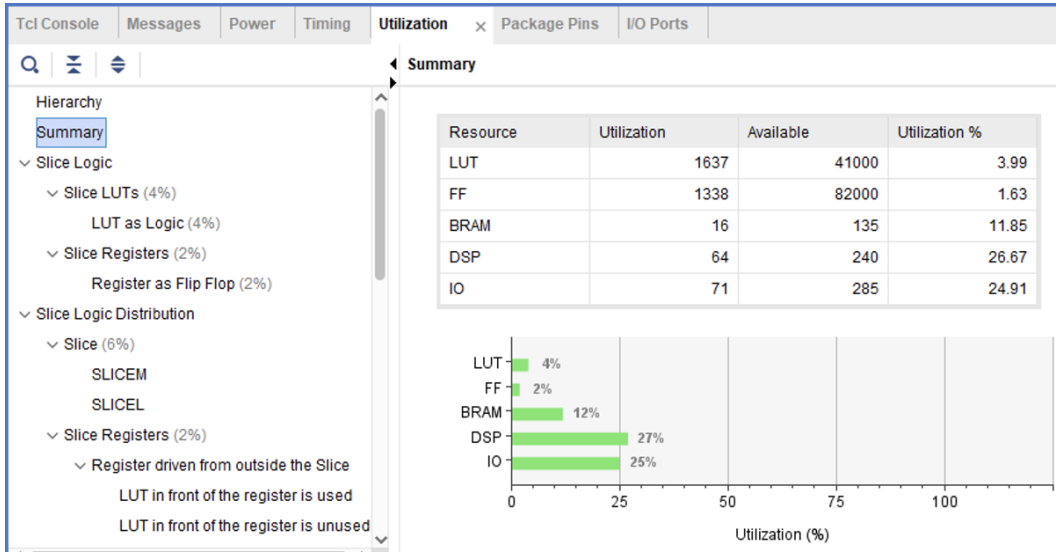
- Analysis on schematic
  - 여러 개의 paths를 선택
  - Device에서 직접 선택 혹은 timing tab에서 선택

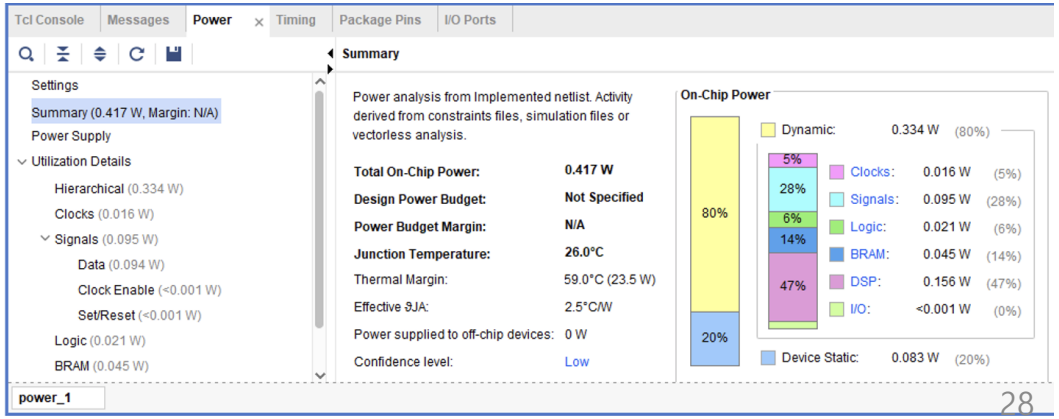


Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exception	Skew
Path 22	1.276	1	2	39	ingressFifoWrEn_reg/C	ingressLoop[1]...addr_reg[6]/CE	3.166	0.302	2.864	9.5	90.5	5.000	wbClk	bftClk		-0.344
Path 23	1.276	1	2	39	ingressFifoWrEn_reg/C	ingressLoop[1]...addr_reg[7]/CE	3.166	0.302	2.864	9.5	90.5	5.000	wbClk	bftClk		-0.344
Path 24	1.276	1	2	39	ingressFifoWrEn_reg/C	ingressLoop[1]...addr_reg[8]/CE	3.166	0.302	2.864	9.5	90.5	5.000	wbClk	bftClk		-0.344
Path 25	1.276	1	2	39	ingressFifoWrEn_reg/C	ingressLoop[1]...addr_reg[9]/CE	3.166	0.302	2.864	9.5	90.5	5.000	wbClk	bftClk		-0.344
Path 26	1.313	1	2	39	ingressFifoWrEn_reg/C	ingressLoop[1]..._tmp_reg[3]/CE	3.104	0.302	2.802	9.7	90.3	5.000	wbClk	bftClk		-0.346
Path 27	1.313	1	2	39	ingressFifoWrEn_reg/C	ingressLoop[1]..._tmp_reg[4]/CE	3.104	0.302	2.802	9.7	90.3	5.000	wbClk	bftClk		-0.346

Step 9: Analyzing Implementation Results

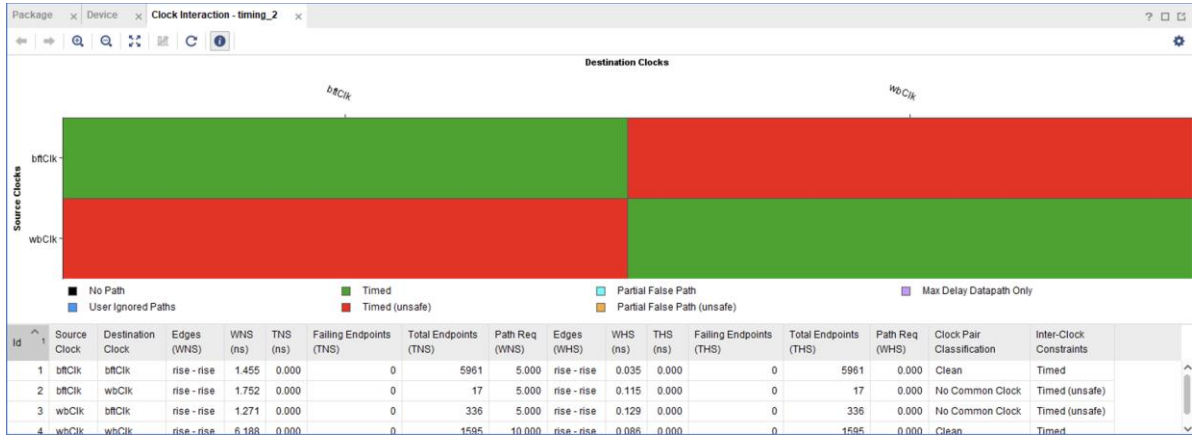
- Reports
  - Report power, report clock interaction, report clock Networks, report utilization 등
  - 위의 명령어를 사용하여 해당 design의 많은 특성들을 알 수 있음





Step 9: Analyzing Implementation Results

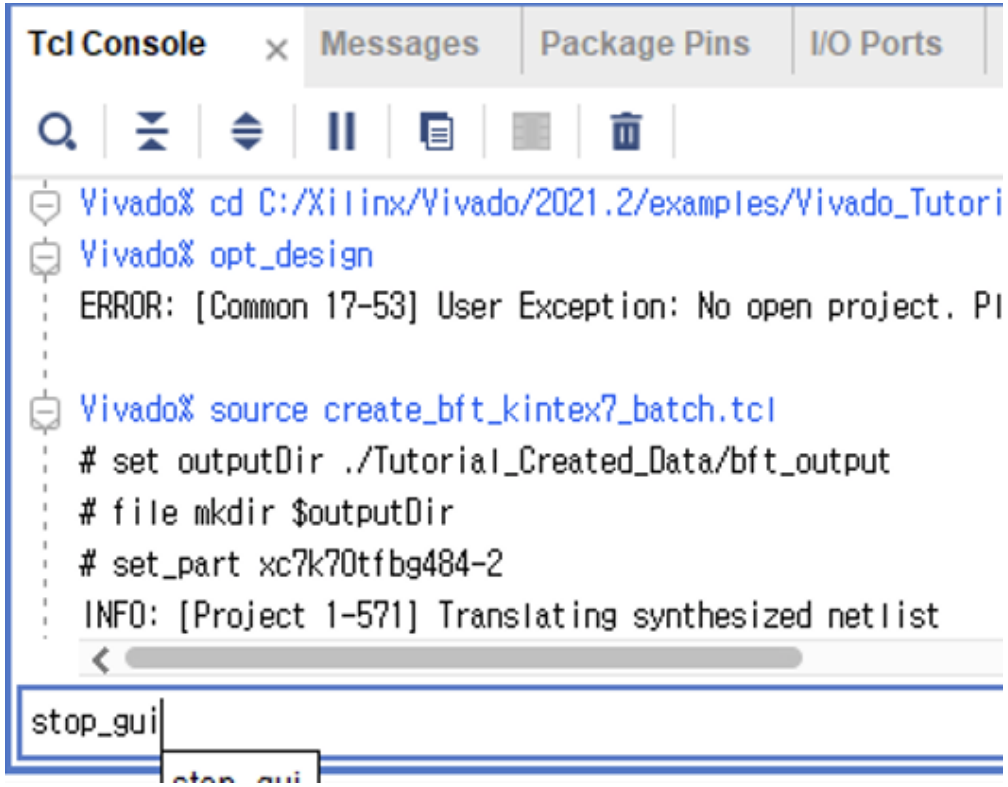
- Reports
  - Report power, report clock interaction, report clock Networks, report utilization 등
  - 위의 명령어를 사용하여 해당 design의 많은 특성들을 알 수 있음

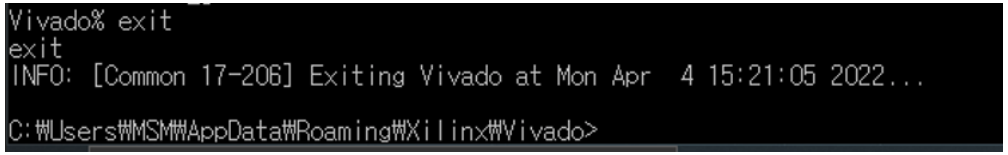


Id	Source Clock	Destination Clock	Edges (WNS)	WNS (ns)	TNS (ns)	Failing Endpoints (TNS)	Total Endpoints (TNS)	Path Req (WNS)	Edges (WHS)	WHS (ns)	THS (ns)	Failing Endpoints (THS)	Total Endpoints (THS)	Path Req (WHS)	Clock Pair Classification	Inter-Clock Constraints
1	bftClk	bftClk	rise - rise	1.455	0.000	0	5961	5.000	rise - rise	0.035	0.000	0	5961	0.000	Clean	Timed
2	bftClk	wbClk	rise - rise	1.752	0.000	0	17	5.000	rise - rise	0.115	0.000	0	17	0.000	No Common Clock	Timed (unsafe)
3	wbClk	bftClk	rise - rise	1.271	0.000	0	336	5.000	rise - rise	0.129	0.000	0	336	0.000	No Common Clock	Timed (unsafe)
4	wbClk	wbClk	rise - rise	6.188	0.000	0	1595	10.000	rise - rise	0.086	0.000	0	1595	0.000	Clean	Timed

Step 10: Exiting the Vivado Tool

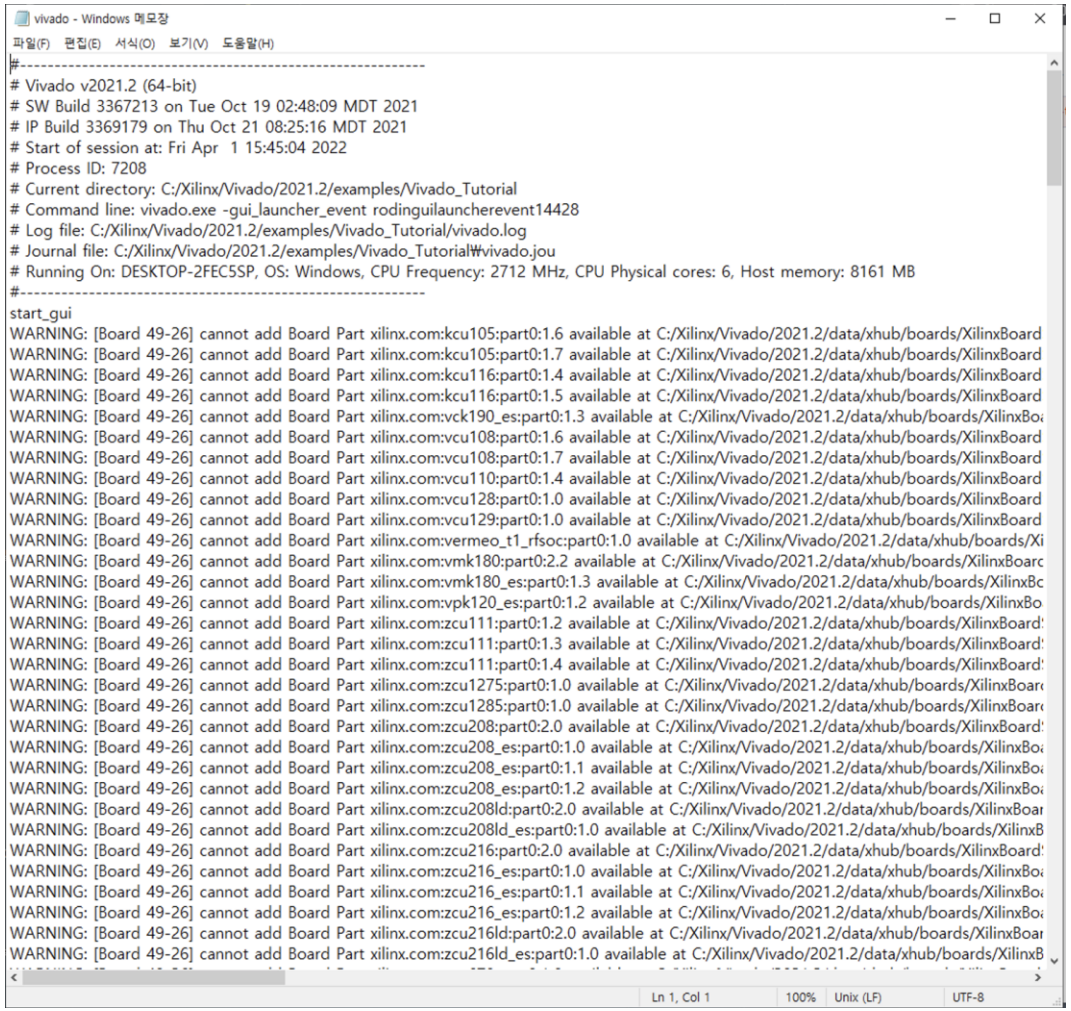
- Stop_gui
  - Tcl console window tab
- Exit
  - Tcl shell window on windows





Step 10: Exiting the Vivado Tool

- Vivado log file
  - Vivado 실행 실행 중에 실행되었던 Tcl 명령어들과 그 결과 모두를 저장합니다.
  - <비바도 설치위치>/Vivado_Tutorial/vivado.log
  - /APPDATA/Xilinx/Vivado/
  - /home 디렉토리



Step 10: Exiting the Vivado Tool

- Vivado journal file
  - Vivado 실행 중에 실행되었던 Tcl 명령어들만 저장합니다.
  - <비바도 설치위치>/Vivado_Tutorial/vivado.jou
  - /APPDATA/Xilinx/Vivado/
  - /home 디렉토리

vivado - Windows 메모장

파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
#-----------------------------------------------------------
# Vivado v2021.2 (64-bit)
# SW Build 3367213 on Tue Oct 19 02:48:09 MDT 2021
# IP Build 3369179 on Thu Oct 21 08:25:16 MDT 2021
# Start of session at: Fri Apr  1 15:45:04 2022
# Process ID: 7208
# Current directory: C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial
# Command line: vivado.exe -gui_launcher_event rodinguilauncherevent14428
# Log file: C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/vivado.log
# Journal file: C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial₩vivado.jou
# Running On: DESKTOP-2FEC5SP, OS: Windows, CPU Frequency: 2712 MHz, CPU Physical cores: 6, Host memory: 8161 MB
#-----------------------------------------------------------
start_gui
create_project project_bft C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Tutorial_Created_Data/project_bft -part xc7k70tfbg484-2
add_files {C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Sources/hdl/bftLib/core_transform.vhdl C:/Xilinx/Vivado/2021.2/examples/Vivado_T
set_property library bftLib [get_files  {C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Sources/hdl/bftLib/core_transform.vhdl C:/Xilinx/Vivad
add_files {C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Sources/hdl/FifoBuffer.v C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Sources,
add_files -fileset sim_1 C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Sources/hdl/bft_tb.v
import_files -force
import_files -fileset constrs_1 -force -norecurse C:/Xilinx/Vivado/2021.2/examples/Vivado_Tutorial/Sources/bft_full_kintex7.xdc
update_compile_order -fileset sources_1
synth_design -rtl -rtl_skip_mlo -name rtl_1
launch_simulation
source bft_tb.tcl
launch_runs synth_1
wait_on_run synth_1
launch_runs impl_1
wait_on_run impl_1
launch_runs impl_1 -to_step write_bitstream
wait_on_run impl_1
open_run impl_1
```

Lab2

Continue..