

# I/O Clock Planning

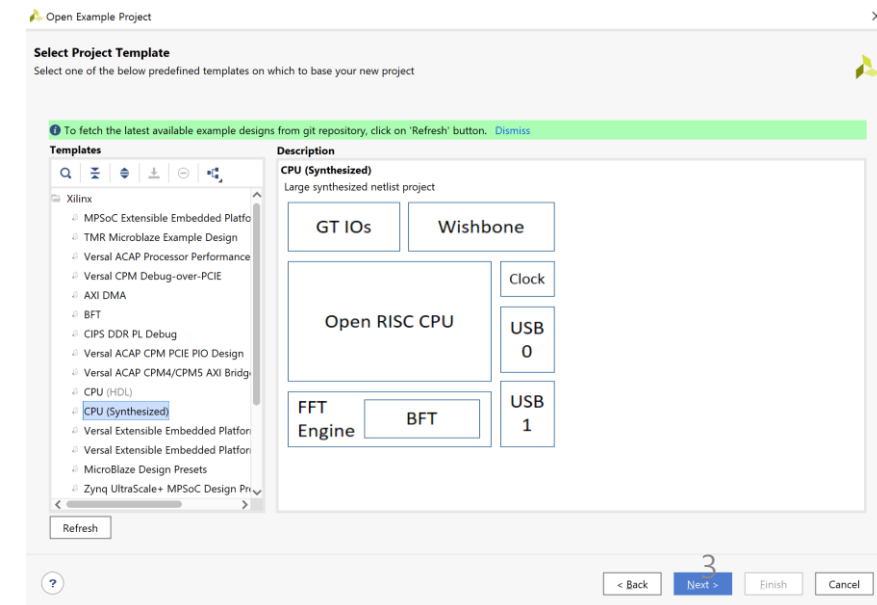
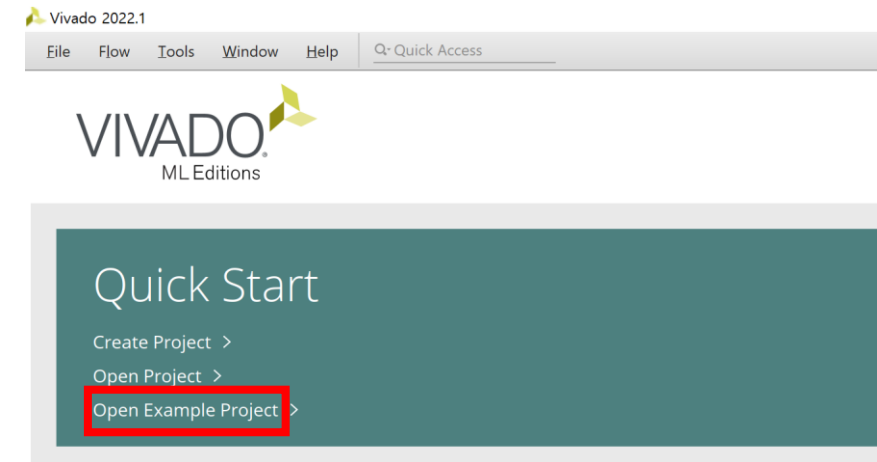
28<sup>th</sup> June 2022

# LAB 1

- 이번 Lab을 통해 알 수 있는 것들
  - How to Create a **constraint set** and set a **target constraint file**
  - How to add **timing constraints** to a design using the **Timing Constraints Wizard**
  - How to add **timing exceptions** using the **Timing Constraints Editor**
  - The importance of **saving constraints** to disk versus in-memory constraints
  - How to generate the **clock interaction report** and properly interpret the resulting matrix
  - How to generate the **timing summary report** and properly interpret the results

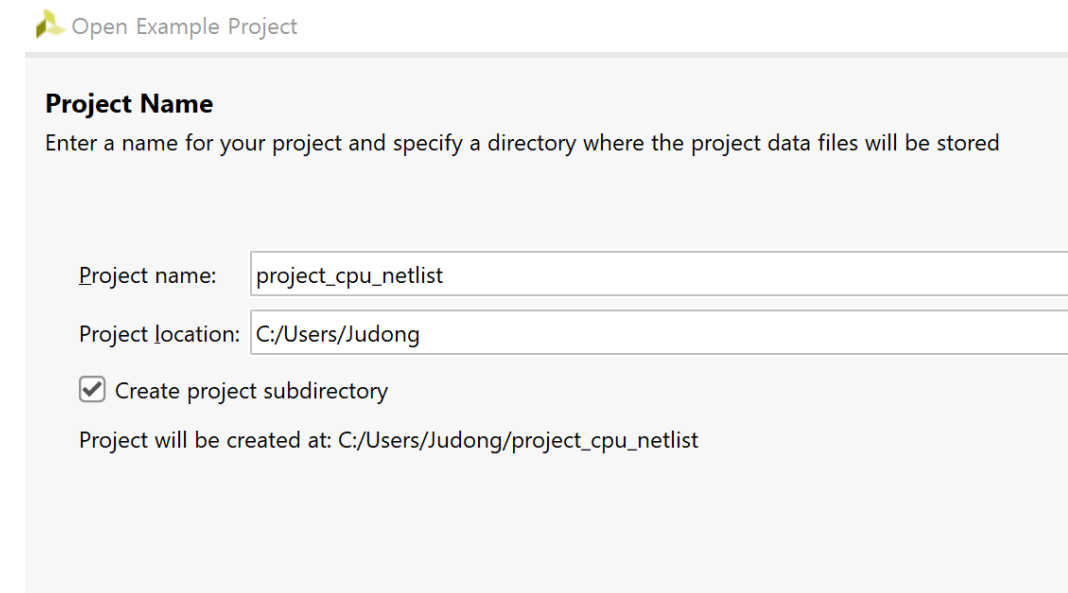
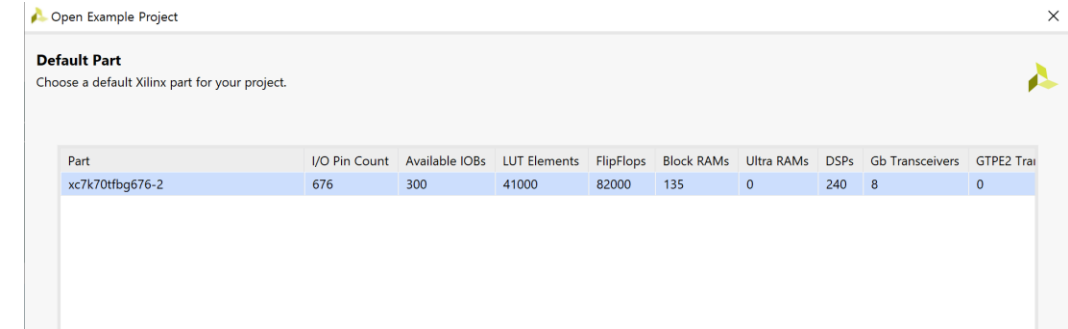
# LAB 1

- Defining Timing Constraints and Exceptions
- 이번 lab에서는 constraints를 생성하는 2가지 방법을 알아 볼 것임
- Step1 예제 프로젝트 열기
  - Start → All Programs → Xilinx Design Tools → Vivado 실행
  - **Open Example Project** 클릭
  - Next 클릭
  - Select Project Template에서, **CPU(Synthesized)** 클릭



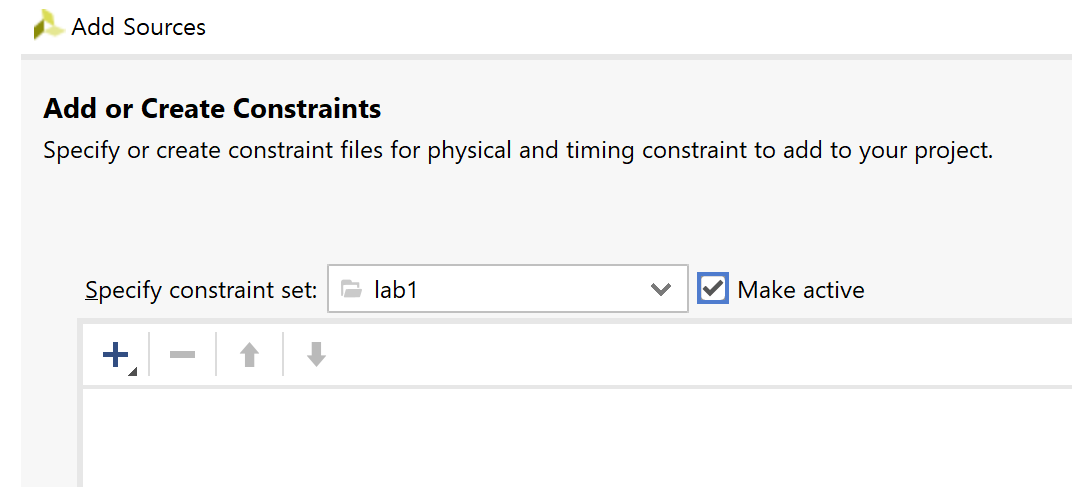
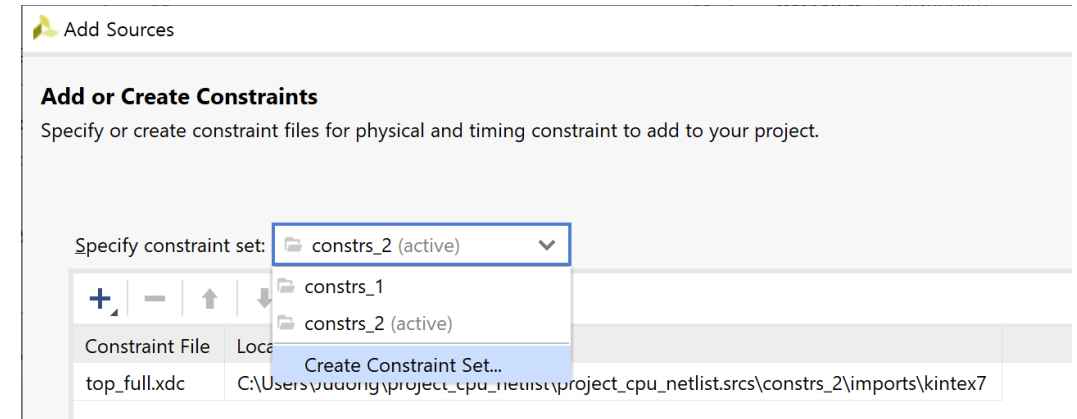
# LAB 1

- Step 1
  - Project Name page에서, 다음과 같이 설정
  - Project name: **project\_cpu\_netlist** (위치는 상관없음)
  - Next 클릭
  - Default Part page에서, default part:
  - **xc7k70tfbg676-2** 입력
  - Next 클릭
  - Finish 클릭 -> 프로젝트 생성



# LAB 1

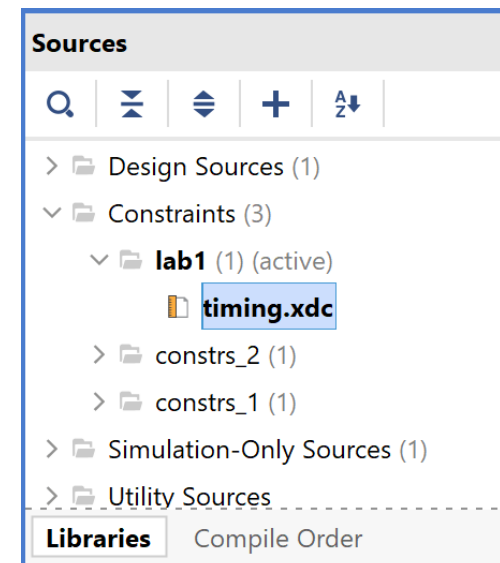
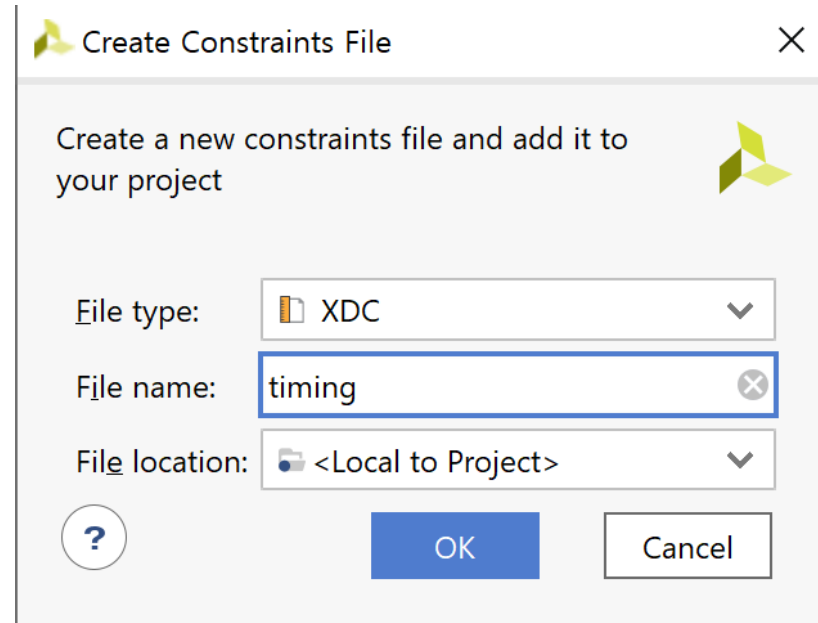
- Step2 Constraint sets와 files 생성하기
  - Flow Navigator에서, Add Source 클릭
  - Add Sources dialog box에서, Add or create constraints 선택
  - Next 클릭
  - Constraint set에서, **Create Constraint Set** 선택
  - Constraint set 이름: lab1 으로 설정
  - OK 클릭
  - Make active 체크
  - Create File 클릭



# LAB 1

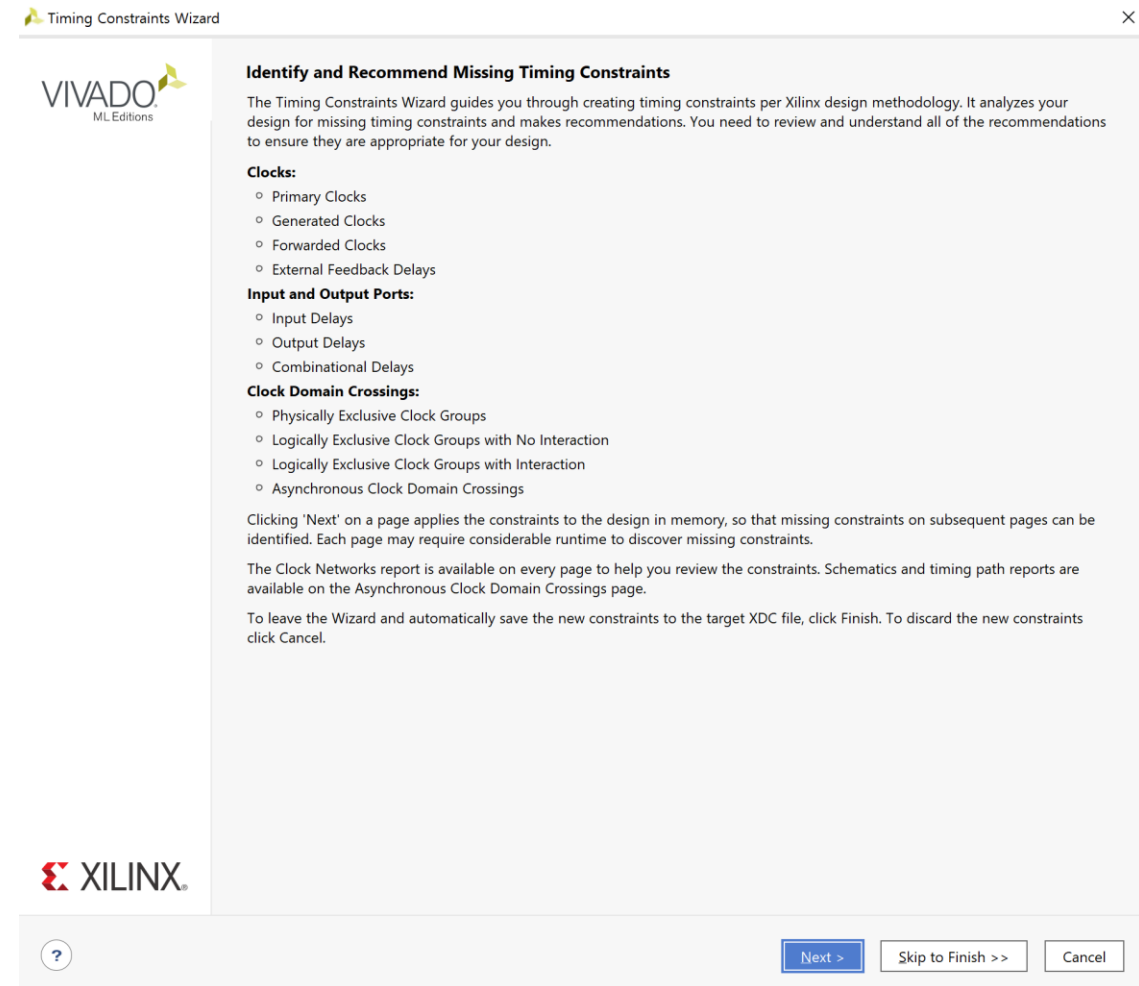
## • Step2

- File type(이름): timing
- File location: Local to Project
- OK 클릭 -> timing.xdc 파일이 lab1 constraint set에 추가됨
- Finish 클릭 -> 새 constraint 파일 생성 완료, 다음 그림과 같이 XDC



# LAB 1

- Step3 Timing Constraints 생성하기
  - Flow Navigator에서, **Open Synthesized Design** 클릭
  - **Constraints Wizard** 클릭
  - > wizard가 생성하는 constraints 종류
  - : Clocks, Input and Output Ports, and Clock Domain Crossings

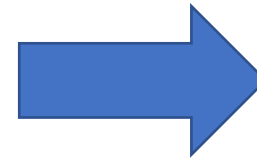


# LAB 1

- Step3
  - Next 클릭
  - 그림과 같이 값을 입력 -> Next 클릭 -> Next 클릭 -> Next 클릭
  - (timing constraints primary, in/output clock 설명하면서 설명 필요)

**Recommended Constraints**

| Object                                       | Name   | Frequency (MHz) | Period (ns) | Rise At (ns) | Fall / |
|--|--|-----------------|-------------|--------------|--------|
| <input checked="" type="checkbox"/> TXOUTCLK | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT0_TXOUTCLK_OUT | 78.125          | 12.800      | 0.000        |        |
| <input checked="" type="checkbox"/> TXOUTCLK | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt2_ROCKETIO_WRAPPER_TILE_i/GT2_TXOUTCLK_OUT | 78.125          | 12.800      | 0.000        |        |
| <input checked="" type="checkbox"/> TXOUTCLK | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt4_ROCKETIO_WRAPPER_TILE_i/GT4_TXOUTCLK_OUT | 78.125          | 12.800      | 0.000        |        |
| <input checked="" type="checkbox"/> TXOUTCLK | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt6_ROCKETIO_WRAPPER_TILE_i/GT6_TXOUTCLK_OUT | 78.125          | 12.800      | 0.000        |        |
| <input checked="" type="checkbox"/> sysClk   | sysClk   | 100.000         | 10.000      | 0.000        |        |



**Timing Constraints Wizard**

**Primary Clocks**  
Primary clocks usually enter the design through input ports. Specify the period and optionally a name and waveform (rising and falling edge times) to describe the duty cycle if not 50%. [More info](#)

**Recommended Constraints**

| Object                                       | Name   | Frequency (MHz) | Period (ns) | Rise At (ns) | Fall / |
|--|--|-----------------|-------------|--------------|--------|
| <input checked="" type="checkbox"/> TXOUTCLK | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT0_TXOUTCLK_OUT | undefined       | undefined   |              |        |
| <input checked="" type="checkbox"/> TXOUTCLK | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt2_ROCKETIO_WRAPPER_TILE_i/GT2_TXOUTCLK_OUT | undefined       | undefined   |              |        |
| <input checked="" type="checkbox"/> TXOUTCLK | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt4_ROCKETIO_WRAPPER_TILE_i/GT4_TXOUTCLK_OUT | undefined       | undefined   |              |        |
| <input checked="" type="checkbox"/> TXOUTCLK | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt6_ROCKETIO_WRAPPER_TILE_i/GT6_TXOUTCLK_OUT | undefined       | undefined   |              |        |
| <input checked="" type="checkbox"/> sysClk   | sysClk   | undefined       | undefined   |              |        |

**Constraints for Pulse Width Check Only**

| Object                   | Name                  | Frequency (MHz) | Period (ns) | Rise At (ns) | Fall At (ns) | Jitter (ns) |
|--------------------------|-----------------------|-----------------|-------------|--------------|--------------|-------------|
| <input type="checkbox"/> | TILE0_REFCLK_PAD_P_IN | undefined       | undefined   |              |              |             |
| <input type="checkbox"/> | TILE1_REFCLK_PAD_P_IN | undefined       | undefined   |              |              |             |
| <input type="checkbox"/> | TILE2_REFCLK_PAD_P_IN | undefined       | undefined   |              |              |             |
| <input type="checkbox"/> | TILE3_REFCLK_PAD_P_IN | undefined       | undefined   |              |              |             |

**Tcl Command Preview (5)** Existing Create Clock Constraints (0)

```

create_clock -name mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT0_TXOUTCLK_OUT [get_pins {mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT0_TXOUTCLK_OUT}]
create_clock -name mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt2_ROCKETIO_WRAPPER_TILE_i/GT2_TXOUTCLK_OUT [get_pins {mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt2_ROCKETIO_WRAPPER_TILE_i/GT2_TXOUTCLK_OUT}]
create_clock -name mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt4_ROCKETIO_WRAPPER_TILE_i/GT4_TXOUTCLK_OUT [get_pins {mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt4_ROCKETIO_WRAPPER_TILE_i/GT4_TXOUTCLK_OUT}]
create_clock -name mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt6_ROCKETIO_WRAPPER_TILE_i/GT6_TXOUTCLK_OUT [get_pins {mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt6_ROCKETIO_WRAPPER_TILE_i/GT6_TXOUTCLK_OUT}]
create_clock -name sysClk [get_ports {sysClk}]
  
```

< Back Next > Skip to Finish >> Cancel



# LAB 1

- (Clock순으로 정렬), Input Constraint 값들을 다음과 같이 설정

Timing Constraints Wizard

**Input Delays**  
Input delays describe relative phase between reference clocks (usually board clocks) and input signals at the FPGA boundary. Inaccurate input delay values can make timing fail and affect implementation quality of results. [More info](#)

**Recommended Constraints**

| Interface  | Clock  |
|--|--|
| <input checked="" type="checkbox"/> DataIn_pad_0_i[*]    | sysClk   |
| <input checked="" type="checkbox"/> DataIn_pad_1_i[*]    | sysClk   |
| <input checked="" type="checkbox"/> LineState_pad_0_i[*] | sysClk   |
| <input checked="" type="checkbox"/> LineState_pad_1_i[*] | sysClk   |
| <input checked="" type="checkbox"/> VStatus_pad_0_i[*]   | sysClk   |
| <input checked="" type="checkbox"/> VStatus_pad_1_i[*]   | sysClk   |
| <input checked="" type="checkbox"/> GTPRESET_IN          | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT0_TXOUTC |
| <input checked="" type="checkbox"/> GTPRESET_IN          | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt2_ROCKETIO_WRAPPER_TILE_i/GT2_TXOUTC |
| <input checked="" type="checkbox"/> GTPRESET_IN          | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt4_ROCKETIO_WRAPPER_TILE_i/GT4_TXOUTC |
| <input checked="" type="checkbox"/> GTPRESET_IN          | mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt6_ROCKETIO_WRAPPER_TILE_i/GT6_TXOUTC |
| <input checked="" type="checkbox"/> RxActive_pad_0_i     | sysClk   |
| <input checked="" type="checkbox"/> RxActive_pad_1_i     | sysClk   |
| <input checked="" type="checkbox"/> RxError_pad_0_i      | sysClk   |
| <input checked="" type="checkbox"/> RxError_pad_1_i      | sysClk   |

**Delay Parameters**

Clock period: 10 ns

tco\_min: undefined ns

tco\_max: undefined ns

trce\_dly\_min: undefined ns

trce\_dly\_max: undefined ns

Rise Max = tco\_max + trce\_dly\_max  
Rise Min = tco\_min + trce\_dly\_min

Apply

Tcl Command Preview (49) Existing Set Input Delay Constraints (0) **Waveform - System | Edge | Single Rise**

input clock

data

tco\_min: Minimum clock-to-output delay  
tco\_max: Maximum clock-to-output delay  
trce\_dly\_min: Minimum trace delay  
trce\_dly\_max: Maximum trace delay

(tco\_min + trce\_dly\_min)

(tco\_max + trce\_dly\_max)

< Back Next > Skip to Finish >> Cancel

Table 2: Input Constrain Values

| Interface            | Clock         | Synchronous | Alignment | Data Rate and Edge | tco_min (ns)                               | tco_max (ns) | trce_dly_min (ns) | trce_dly_max (ns) |
|----------------------|---------------|-------------|-----------|--------------------|--|--------------|-------------------|-------------------|
| GTPRESET_IN          | mgtEngine/... | System      | Edge      | Single Rise        | Uncheck constraint - will false path later |              |                   |                   |
| GTPRESET_IN          | mgtEngine/... | System      | Edge      | Single Rise        | Uncheck constraint - will false path later |              |                   |                   |
| GTPRESET_IN          | mgtEngine/... | System      | Edge      | Single Rise        | Uncheck constraint - will false path later |              |                   |                   |
| GTPRESET_IN          | mgtEngine/... | System      | Edge      | Single Rise        | Uncheck constraint - will false path later |              |                   |                   |
| DataIn_pad_0_i[*]    | sysClk        | System      | Edge      | Single Rise        | 1  | 2            | 1                 | 1                 |
| DataIn_pad_1_i[*]    | sysClk        | System      | Edge      | Single Rise        | 1  | 2            | 1                 | 1                 |
| LineState_pad_0_i[*] | sysClk        | System      | Edge      | Single Rise        | 1  | 2            | 1                 | 1                 |
| LineState_pad_1_i[*] | sysClk        | System      | Edge      | Single Rise        | 1  | 2            | 1                 | 1                 |
| VStatus_pad_0_i[*]   | sysClk        | System      | Edge      | Single Rise        | 1  | 2            | 1                 | 1                 |
| VStatus_pad_1_i[*]   | sysClk        | System      | Edge      | Single Rise        | 1  | 2            | 1                 | 1                 |
| RxActive_pad_0_i     | sysClk        | System      | Edge      | Single Rise        | 1  | 2            | 1                 | 1                 |
| RxActive_pad_1_i     | sysClk        | System      | Edge      | Single Rise        | 1  | 2            | 1                 | 1                 |
| Rx_Error_pad_0_i     | sysClk        | System      | Edge      | Single Rise        | 1  | 2            | 1                 | 1                 |
| Rx_Error_pad_1_i     | sysClk        | System      | Edge      | Single Rise        | 1  | 2            | 1                 | 1                 |

# LAB 1

- Input Constraint 값들을 다음과 같이 설정
- Next 클릭

**Table 2: Input Constrains Values (cont'd)**

| Interface        | Clock            | Synchronous | Alignment | Data Rate and Edge | tco_min (ns) | tco_max (ns) | trce_dly_min (ns) | trce_dly_max (ns) |
|------------------|------------------|-------------|-----------|--------------------|--------------|--------------|-------------------|-------------------|
| Rx_Valid_pad_0_i | sysClk           | System      | Edge      | Single Rise        | 1            | 2            | 1                 | 1                 |
| Rx_Valid_pad_1_i | sysClk           | System      | Edge      | Single Rise        | 1            | 2            | 1                 | 1                 |
| TxReady_pad_0_i  | sysClk           | System      | Edge      | Single Rise        | 1            | 2            | 1                 | 1                 |
| TxReady_pad_1_i  | sysClk           | System      | Edge      | Single Rise        | 1            | 2            | 1                 | 1                 |
| usb_vbus_paf_0_i | sysClk           | System      | Edge      | Single Rise        | 1            | 2            | 1                 | 1                 |
| usb_vbus_paf_1_i | sysClk           | System      | Edge      | Single Rise        | 1            | 2            | 1                 | 1                 |
| or1200_clmode    | VIRTUAL_cpuClk_5 | System      | Edge      | Single Rise        | 0.1          | 2.5          | 0.1               | 0.2               |
| or1200_pic_ints  | VIRTUAL_cpuClk_5 | System      | Edge      | Single Rise        | 0.1          | 2.5          | 0.1               | 0.2               |
| reset            | VIRTUAL_cpuCLK_5 | System      | Edge      | Single Rise        | 0.1          | 2.5          | 0.1               | 0.2               |

# LAB 1

- Output constraint 값을 다음과 같이 설정
- (Clock을 클릭해서 정렬)

Table 3: Output Constraint Values

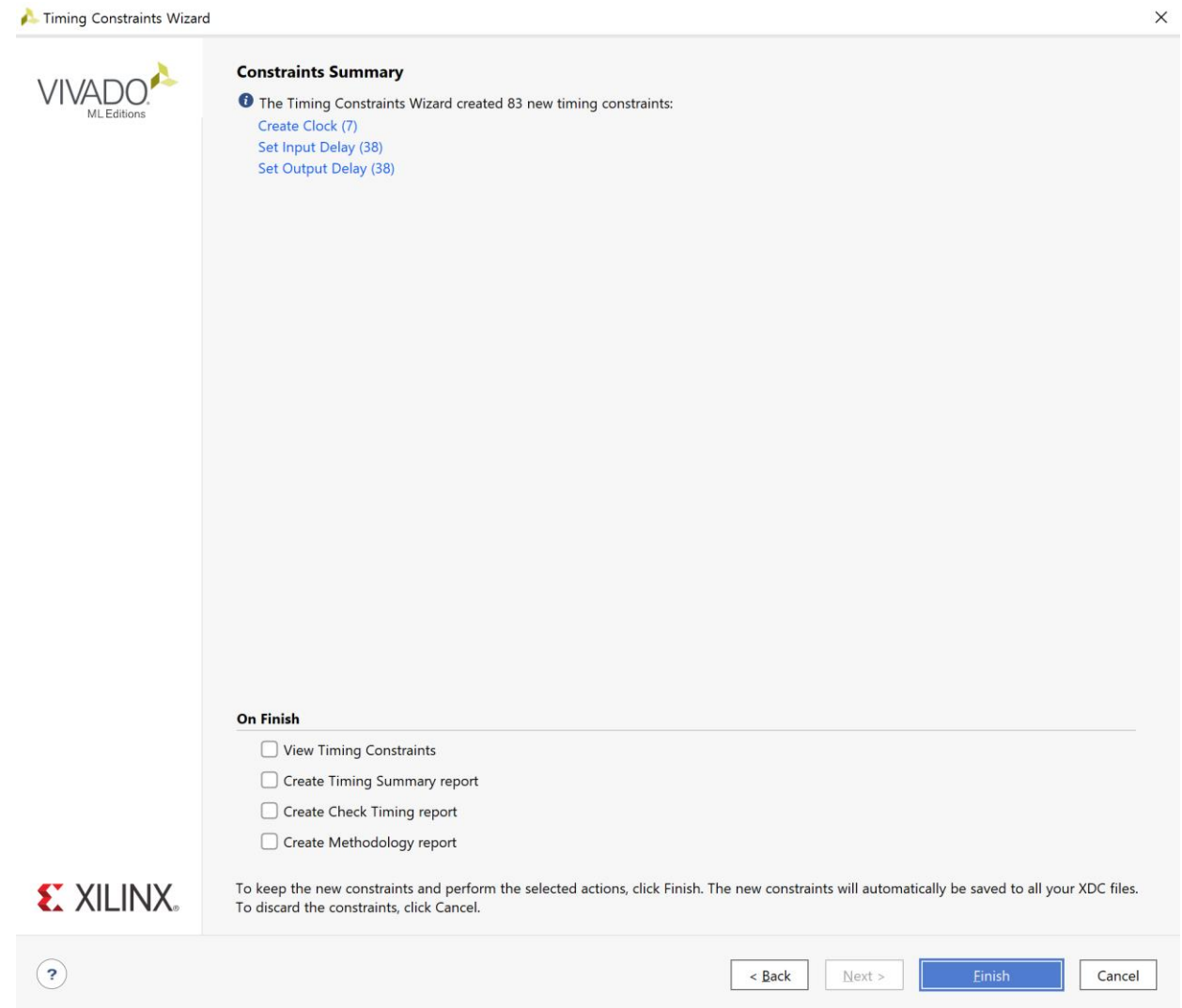
| Interface           | Clock  | Synchronous | Alignment  | Data Rate and Edge | tsu (ns) | thd (ns) | trce_dly_max (ns) | trce_dly_min (ns) |
|---------------------|--------|-------------|------------|--------------------|----------|----------|-------------------|-------------------|
| OpMode_pad_0_o[*]   | sysClk | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| OpMode_pad_1_o[*]   | sysClk | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| VControl_pad_0_o[*] | sysClk | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| VControl_pad_0_o[*] | sysClk | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |

Table 3: Output Constraint Values (cont'd)

| Interface             | Clock           | Synchronous | Alignment  | Data Rate and Edge | tsu (ns) | thd (ns) | trce_dly_max (ns) | trce_dly_min (ns) |
|-----------------------|-----------------|-------------|------------|--------------------|----------|----------|-------------------|-------------------|
| SuspendM_pad_0_o      | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| SuspendM_pad_1_o      | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| TermSel_pad_0_o       | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| TermSel_pad_1_o       | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| TxValid_pad_0_o       | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| TxValid_pad_1_o       | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| VControl_Load_pad_0_o | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| VControl_Load_pad_1_o | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| XcvSelect_pad_0_o     | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| XcvSelect_pad_1_o     | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| phy_rst_pad_0_o       | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| phy_rst_pad_1_o       | sysClk          | System      | Setup/Hold | Single Rise        | 1.0      | 0.1      | 0.1               | 0.1               |
| DataOut_pad_0_o[*]    | VIRTUAL_wbClk_4 | System      | Setup/Hold | Single Rise        | 2.1      | 0.6      | 0.1               | 0.0               |
| DataOut_pad_1_o[*]    | VIRTUAL_wbClk_4 | System      | Setup/Hold | Single Rise        | 2.1      | 0.6      | 0.1               | 0.0               |
| or1200_pm_out[*]      | VIRTUAL_wbClk_4 | System      | Setup/Hold | Single Rise        | 2.1      | 0.6      | 0.1               | 0.0               |

# LAB 1

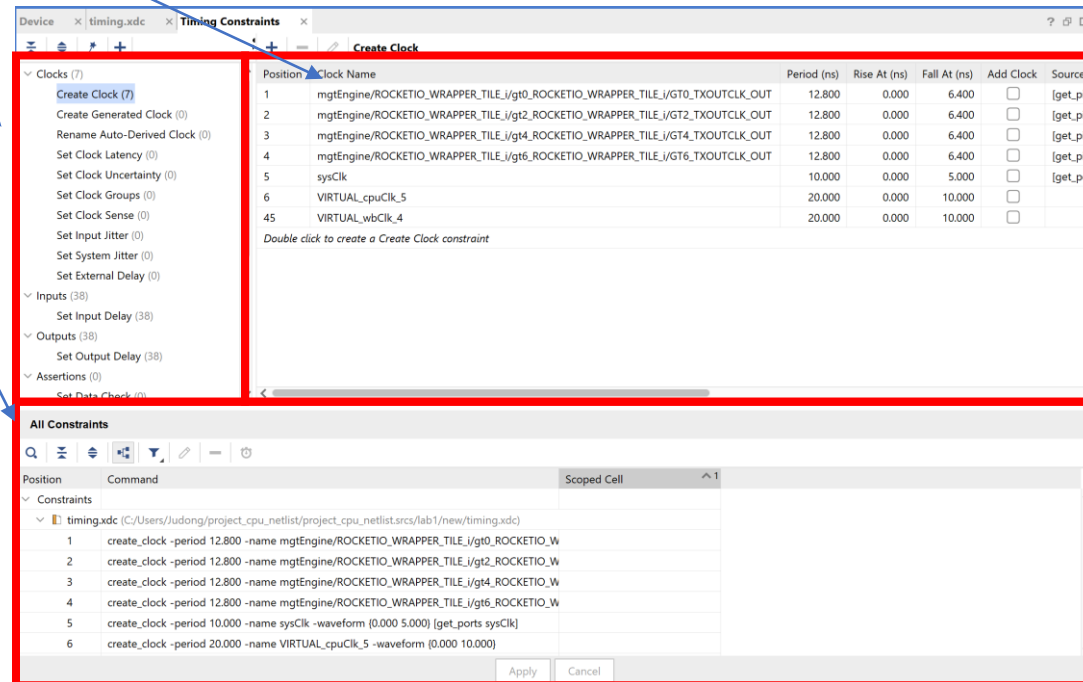
- Next 클릭
- Wizard finish -> Wizard 종료



# LAB 1

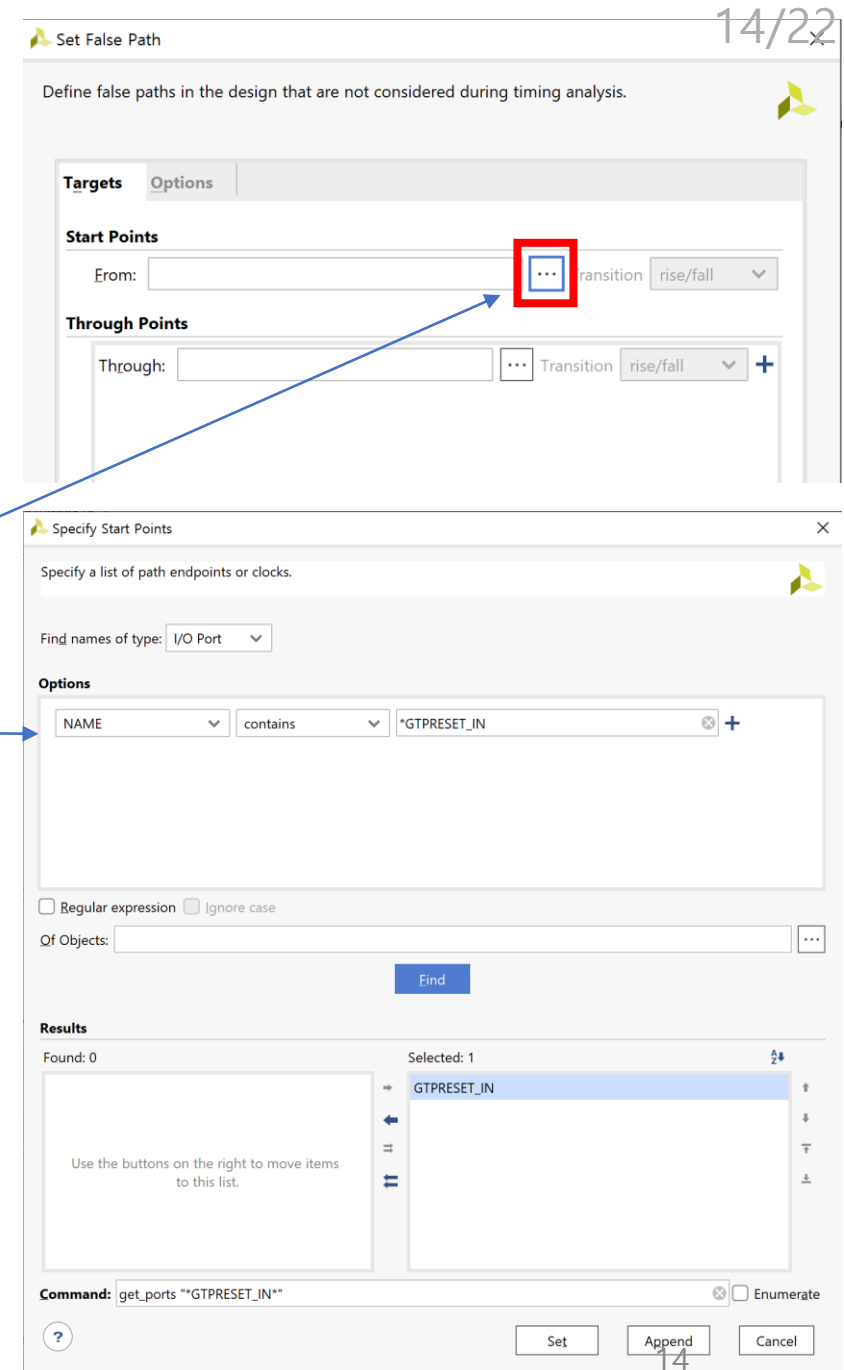
## • Step4 **Constraints Editor** 사용하기

- Synthesized Design에서, **Edit Timing Constraints** 클릭
  - **Constraints tree view**: 카테고리 별로 timing constraints 그룹을 볼 수 있음
  - **Constraints Spreadsheet**: 선택된 그룹의 timing constraints. Constraints Wizard에서 수정했던 것처럼 주기 등을 수정할 수 있음
  - **All Constraints**: design의 모든 Constraints를 다 표시



# LAB 1

- Step4 False path exception 생성
  - Constraints tree view에서, **Exception** 카테고리 스크롤
  - **Set False Path** 더블 클릭
  - Start Points 탭에서, Choose Start Points button 클릭
    - Type 이름: **I/O Port**
    - Option: **GTPRESET\_IN**
    - Find 클릭
    - Results에서 해당 포트를 선택
    - Set 클릭 -> set false path의 시작포트를 정할 수 있음
  - OK 클릭 -> Timing Constraint Editor 닫음
  - -> **false path exception** 생성

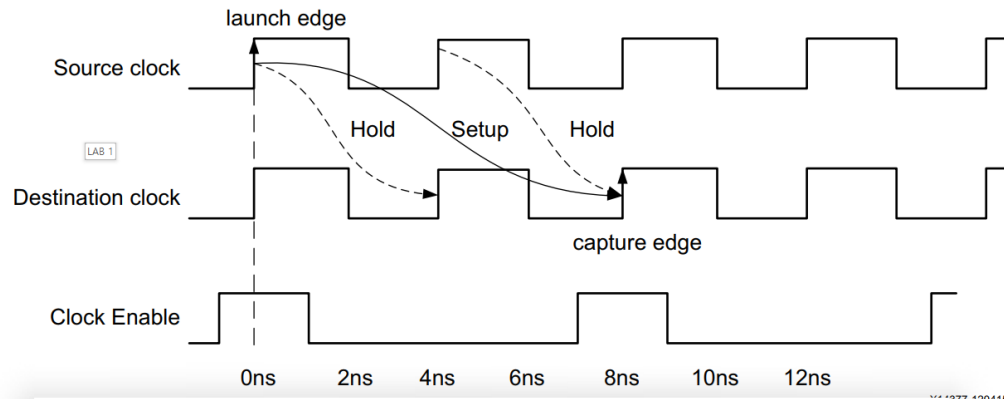


# LAB 1

## • Step4 MultiCycle Path 추가하기

- 다시 Exceptions에서, **Set Multicycle Path** 더블 클릭
  - Path multiplier: **2**로 설정
  - **Through entry box**에서,
  - [get\_pins cpuEngine/or1200\_cpu/or1200\_alu/\*] 입력
  - OK 클릭
- > multicycle path가 생성된 것을 알 수 있음

### AFTER



Set Multicycle Path

Define multicycle path. This command allows specifying the total number of clock cycle required for propagation of a signal from its origin to destination when that propagation is longer than a single clock cycle.

Specify path multiplier:

**Targets** **Options**

**Start Points**

From:  ... Transition: rise/fall

**Through Points**

Through:  ... Transition: rise/fall

**End Points**

To:  ... Transition: rise/fall

**Command:** set\_multicycle\_path -through [get\_pins cpuEngine/or1200\_cpu/or1200\_alu/\*] 2

? Reference Reset to Defaults OK Cancel

# LAB 1

## • Step4

- 다시 **Set multicycle path**를 더블클릭
- Pass multiplier를 1로 설정
- **Option** 탭 클릭
- Setup/Hold 탭에서, **Use path multiplier** 체크'
- OK 클릭

Set Multicycle Path

Define multicycle path. This command allows specifying the total number of clock cycle required for propagation of a signal from its origin to destination when that propagation is longer than a single clock cycle.

Specify path multiplier: 1

**Targets** **Options**

**Setup/Hold**

☒ Use path multiplier for hold (minimum delay) calculation

**Rise/Fall**

☐ Use path multiplier for endpoint rising delays

**Start/End**

☐ Multicycle information is relative to the startpoint clock


☐ Remove existing path exceptions before setting multicycle path

**Command:** set\_multicycle\_path -hold -through [get\_pins cpuEngine/or1200\_cpu/or1200\_alu/\*] 1

? Reference Reset to Defaults OK Cancel



# LAB 1

- Step5 Constraints 저장
  - 앞에서 설정한 setting들은 아직 저장되지 않은 상태임
  - 따라서 설정한 exceptions을 timing.xdc 파일에 저장해야 함
- Sources 탭 – Constraints – timing.xdc 더블 클릭
- Constraints 목록에서 스크롤
- -> set\_false\_path, set\_multicycle\_path constraints 저장 아직 안됨
- **File – Constraints – Save As** 
- Constraints 저장
- 2개의 constraints가 저장됨을 확인

All Constraints

| Position              | Command   | Scoped Cell |
|-----------------------|---|-------------|
| 80                    | set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.0 [get_ports phy_rst_pad_0_o] |             |
| 81                    | set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.1 [get_ports phy_rst_pad_0_o] |             |
| 82                    | set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.0 [get_ports phy_rst_pad_1_o] |             |
| 83                    | set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.1 [get_ports phy_rst_pad_1_o] |             |
| <unsaved constraints> |   |             |
| 84                    | set_false_path -from [get_ports *GTPRESET_IN*]  |             |
| 85                    | set_multicycle_path -through [get_pins cpuEngine/or1200_cpu/or1200_alu/*] 2                 |             |
| 86                    | set_multicycle_path -hold -through [get_pins cpuEngine/or1200_cpu/or1200_alu/*] 1           |             |

Apply Cancel



All Constraints

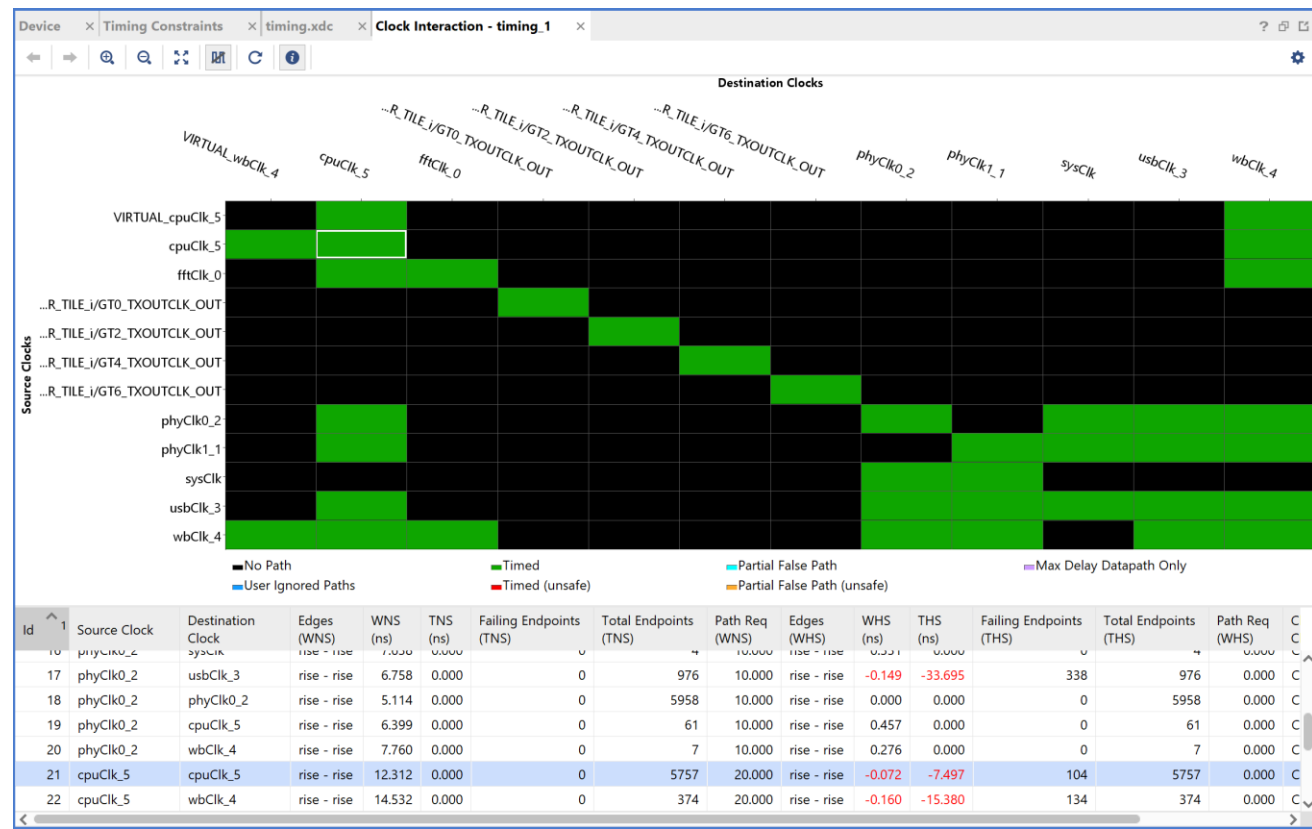
| Position | Command   | Scoped Cell |
|----------|---|-------------|
| 79       | set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.1 [get_ports phy_rst_pad_0_o] |             |
| 80       | set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.0 [get_ports phy_rst_pad_0_o] |             |
| 81       | set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.1 [get_ports phy_rst_pad_0_o] |             |
| 82       | set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.0 [get_ports phy_rst_pad_1_o] |             |
| 83       | set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.1 [get_ports phy_rst_pad_1_o] |             |
| 84       | set_false_path -from [get_ports *GTPRESET_IN*]  |             |
| 85       | set_multicycle_path -through [get_pins cpuEngine/or1200_cpu/or1200_alu/*] 2                 |             |
| 86       | set_multicycle_path -hold -through [get_pins cpuEngine/or1200_cpu/or1200_alu/*] 1           |             |

Apply Cancel

# LAB 1

## • Step6 Clock Interaction Report

- Synthesized Design -> **Report Clock Interaction**
- 모든 설정 Default -> OK 클릭



# LAB 1

- Step7 Timing Summary Report
  - Reports -> Timing -> **Report Timing Summary**
  - 모든 설정 Default -> OK 클릭
  - 그림과 같이 Timing Summary 생성
  - **Worst Negative Slack** 클릭
  - -> 해당 design에서 worst timing path를 확인할 수 있음

**Timing**

Design Timing Summary

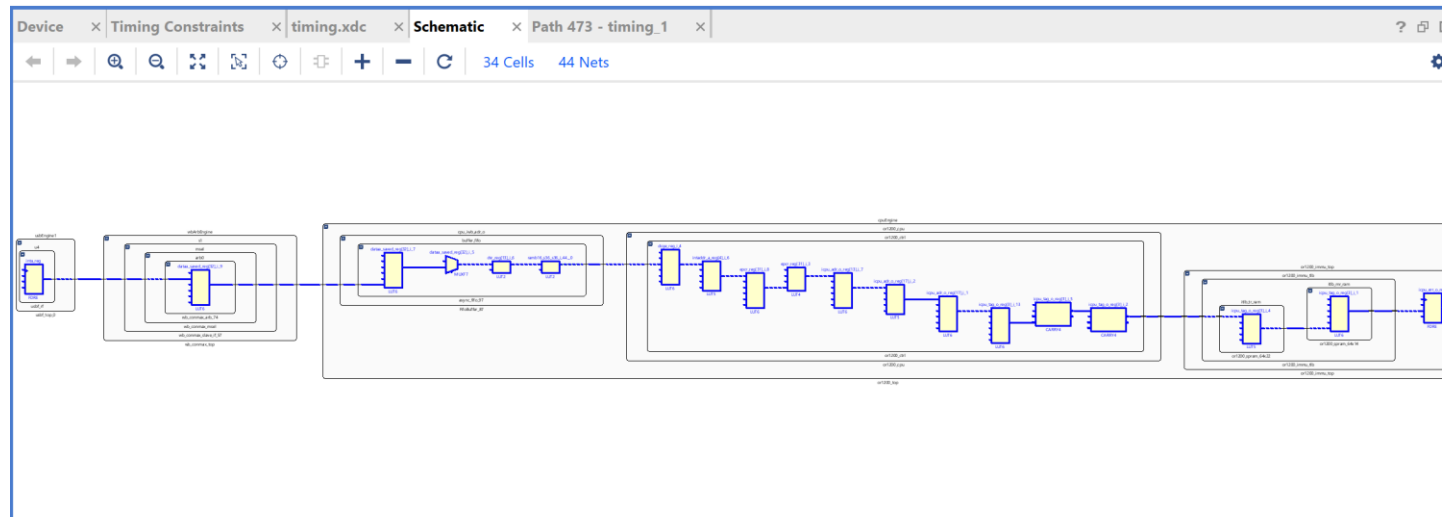
| Setup                                | Hold                                | Pulse Width                                       |
|--------------------------------------|-------------------------------------|---|
| Worst Negative Slack (WNS): 2.250 ns | Worst Hold Slack (WHS): -0.274 ns   | Worst Pulse Width Slack (WPWS): 3.000 ns          |
| Total Negative Slack (TNS): 0.000 ns | Total Hold Slack (THS): -372.506 ns | Total Pulse Width Negative Slack (TPWS): 0.000 ns |
| Number of Failing Endpoints: 0       | Number of Failing Endpoints: 6476   | Number of Failing Endpoints: 0                    |
| Total Number of Endpoints: 46377     | Total Number of Endpoints: 46377    | Total Number of Endpoints: 16037                  |

**Timing constraints are not met.**

Timing Summary - timing\_1

# LAB 1

- Step7
  - F4를 누르면 그 path를 Schematic으로 관찰가능



Timing

Inter-Clock Paths - usbClk\_3 to cpuClk\_5 - Setup

| Name     | Slack | Levels | Routes | High Fanout | From            | To              | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock |
|----------|-------|--------|--------|-------------|-----------------|-----------------|-------------|-------------|-----------|-------------|--------------|
| Path 473 | 2.250 | 17     | 18     | 165         | usbEng..._reg/C | cpuEng..._reg/D | 7.406       | 1.583       | 5.823     | 10.0        | usbClk_3     |
| Path 474 | 2.250 | 17     | 18     | 165         | usbEng..._reg/C | cpuEng...g[0]/D | 7.406       | 1.583       | 5.823     | 10.0        | usbClk_3     |
| Path 475 | 2.250 | 17     | 18     | 165         | usbEng..._reg/C | cpuEng...g[1]/D | 7.406       | 1.583       | 5.823     | 10.0        | usbClk_3     |
| Path 476 | 2.250 | 17     | 18     | 165         | usbEng..._reg/C | cpuEng...g[3]/D | 7.406       | 1.583       | 5.823     | 10.0        | usbClk_3     |
| Path 477 | 2.257 | 17     | 18     | 165         | usbEng..._reg/C | cpuEng...g[2]/D | 7.399       | 1.583       | 5.816     | 10.0        | usbClk_3     |
| Path 478 | 2.257 | 17     | 18     | 165         | usbEng..._reg/C | cpuEng...reg/D  | 7.399       | 1.583       | 5.816     | 10.0        | usbClk_3     |
| Path 479 | 2.581 | 16     | 17     | 165         | usbEng..._reg/C | cpuEng...[13]/D | 7.075       | 1.540       | 5.535     | 10.0        | usbClk_3     |
| Path 480 | 2.581 | 16     | 17     | 165         | usbEng..._reg/C | cpuEng...[14]/D | 7.075       | 1.540       | 5.535     | 10.0        | usbClk_3     |

Timing Summary - timing\_1

# LAB 1

- Step7
  - timing summary tree에서, Clock Summary 선택
  - 해당 design의 모든 clock들 확인 가능
  - Clock들의 **frequency, 주기, waveform(최소, 최대값)** 확인 가능
  - sysClk에 속해있는 clock들은 sysClk에 관계가 있음
    - 예를 들어, cpuClk\_5는 sysClk로부터 생성되었고 주기는 sysClk의 2배라는 것을 알 수 있음
  - Timing 탭의 나머지 부분들은 종류 별로 묶인 path 그룹들임

| Tcl Console Messages Log Reports Design Runs Timing x |                      |                |             |                 |
|---|----------------------|----------------|-------------|-----------------|
| Clock Summary   |                      |                |             |                 |
| General Information                                   | Name                 | Waveform       | Period (ns) | Frequency (MHz) |
| Timer Settings  | VIRTUAL_cpuClk_5     | {0.000 10.000} | 20.000      | 50.000          |
| Design Timing Summary                                 | VIRTUAL_wbClk_4      | {0.000 10.000} | 20.000      | 50.000          |
| Clock Summary (14)                                    | mgtEngine/ROCKETIO_1 | {0.000 6.400}  | 12.800      | 78.125          |
| Methodology Summary                                   | mgtEngine/ROCKETIO_1 | {0.000 6.400}  | 12.800      | 78.125          |
| > Check Timing (9)                                    | mgtEngine/ROCKETIO_1 | {0.000 6.400}  | 12.800      | 78.125          |
| > Intra-Clock Paths                                   | mgtEngine/ROCKETIO_1 | {0.000 6.400}  | 12.800      | 78.125          |
| > Inter-Clock Paths                                   | sysClk               | {0.000 5.000}  | 10.000      | 100.000         |
| > Other Path Groups                                   | clkfbout             | {0.000 5.000}  | 10.000      | 100.000         |
| > User Ignored Paths                                  | cpuClk_5             | {0.000 10.000} | 20.000      | 50.000          |
| > Unconstrained Paths                                 | fftClk_0             | {0.000 5.000}  | 10.000      | 100.000         |
|   | phyClk0_2            | {0.000 5.000}  | 10.000      | 100.000         |
|   | phyClk1_1            | {0.000 5.000}  | 10.000      | 100.000         |
|   | usbClk_3             | {0.000 5.000}  | 10.000      | 100.000         |
|   | wbClk_4              | {0.000 10.000} | 20.000      | 50.000          |

# Lab2...