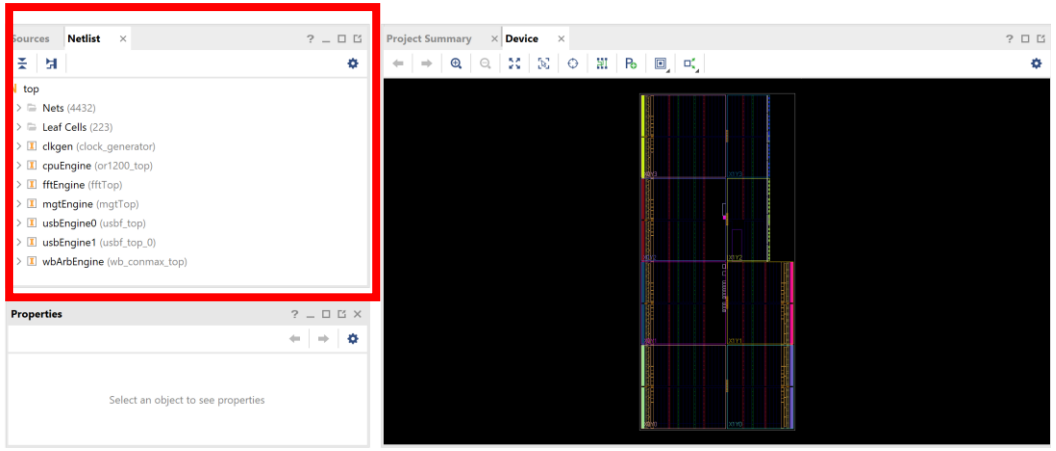
Using Constraints

Ug 945 Lab2

6th July 2022

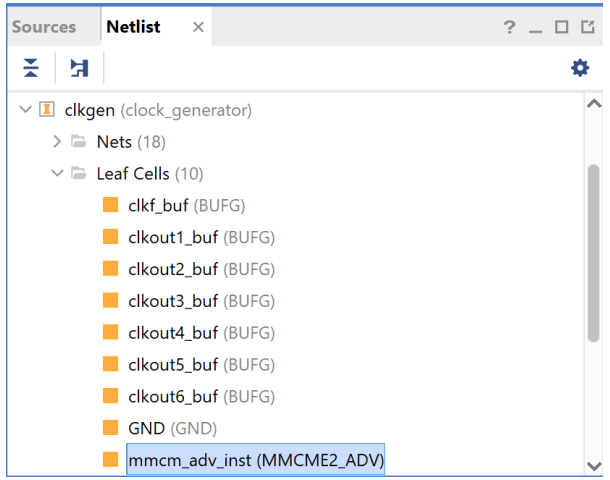
LAB 2

- Setting Physical Constraints
- 이번 lab에서는 CPU Netlist design에 대한 physical constraints를 설정해 볼 예정



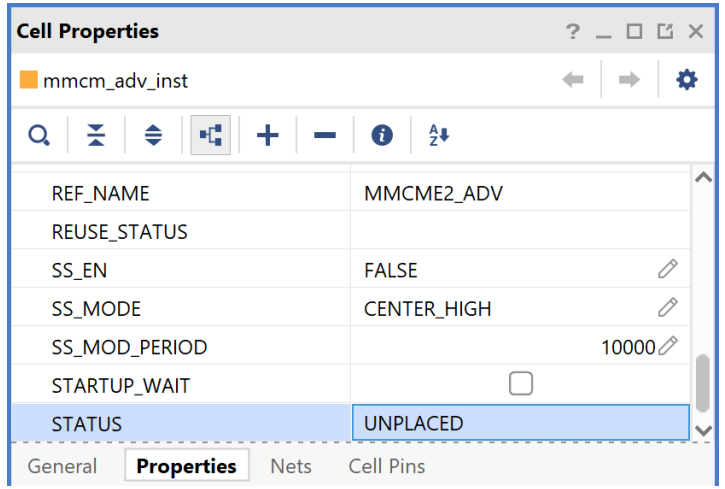
- Step1 placement constraints 추가하기
  - Flow Navigator에서, **Open Synthesized Design** 클릭

  -> **synthesized netlist** 열림
  - Netlist에서, **clkgen hierarchy** 확장
  - Leaf cells 확장 -> **mmcm_adv_inst** 선택

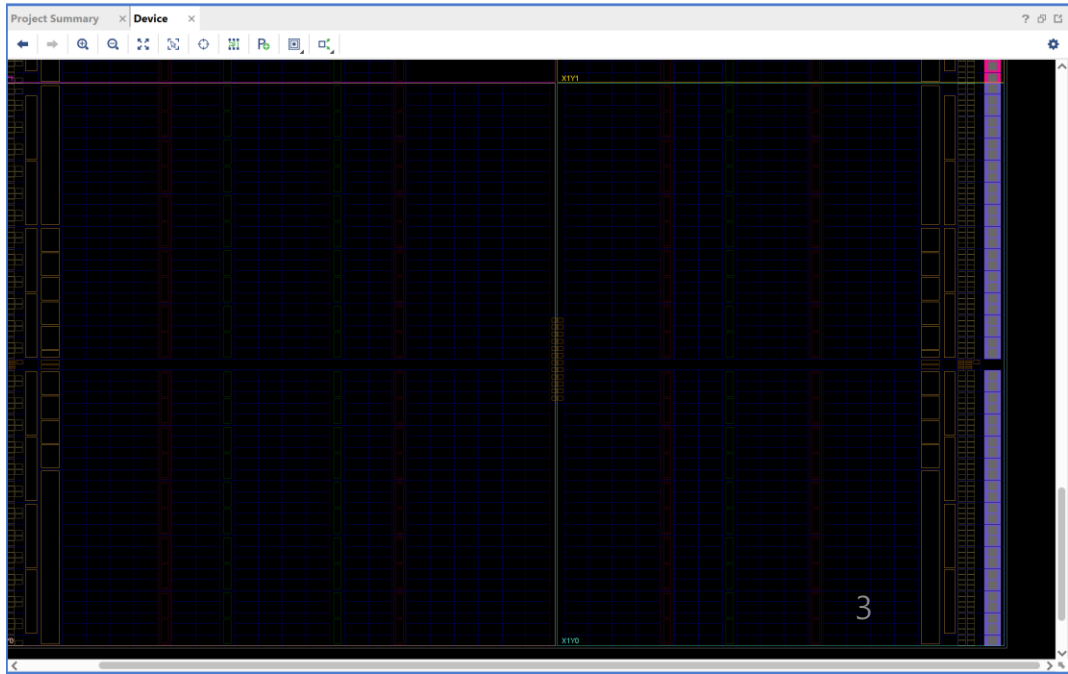


LAB 2

- Step2
  - Cell properties 탭에서, STATUS가 **UNPLACED** 임을 확인 (IS_LOC_FIXED, IS_BEL_FIXED는 보이지 않음)
  - 아래의 Tcl 명령어로 확인 가능
    - get_property IS_LOC_FIXED [get_cells clkgen/mmcm_adv_inst]
    - 결과가 0으로 나왔다면, 해당 Netlist의 위치가 정해지지 않았다는 의미
  - Device view 오른쪽 하단 부(X1Y0)를 확대(zoom)
    - Clock과 관련한 부분을 관찰할 수 있음

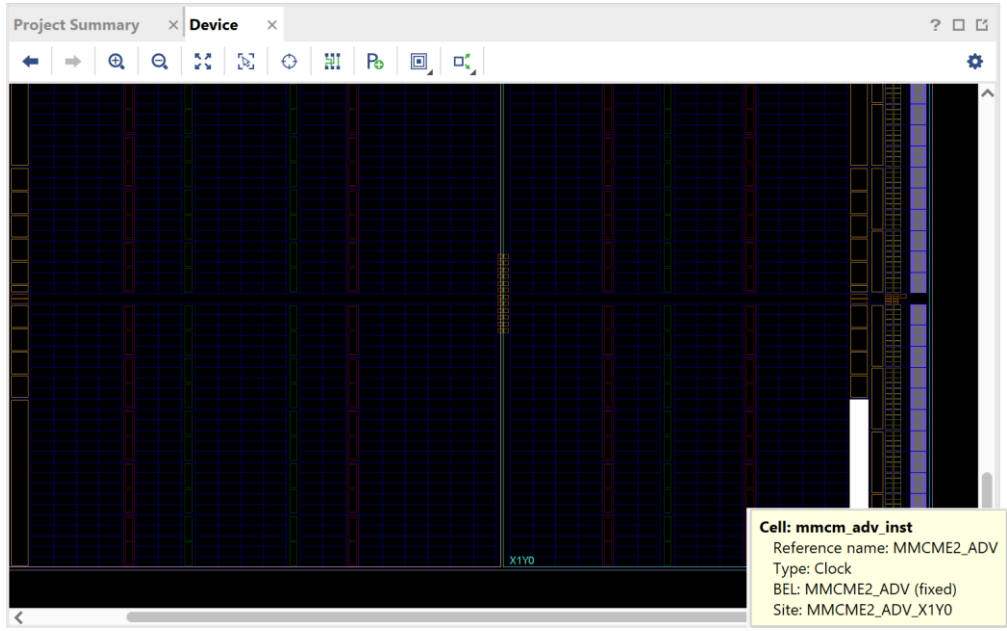


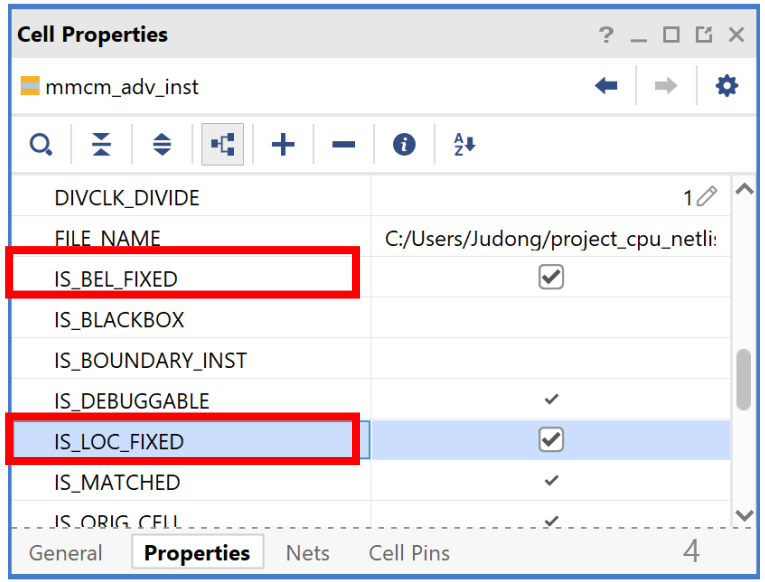

```
get_property IS_LOC_FIXED [get_cells clkgen/mmcm_adv_inst]
0
```



LAB 2

- Step2
  - Netlist에서, mmcm_adv_inst를 확대한 Device 위치로 드래그
  - 드래그 후에 Tcl 명령어에서 다음과 같은 명령어를 볼 수 있음
    - startgroup
    - place_cell clkgen/mmcm_adv_inst MMCME2_ADV_X1Y0/MMCME2_ADV
    - endgroup
  - 다시 mmcm net의 Cell Properties에서,
  - IS_BEL_FIXED, IS_LOC_FIXED가 생겨난 것을 볼 수 있음
  - STATUS는 FIXED로 설정됨
  - Save Constraints 클릭(기존 timing.xdc로)



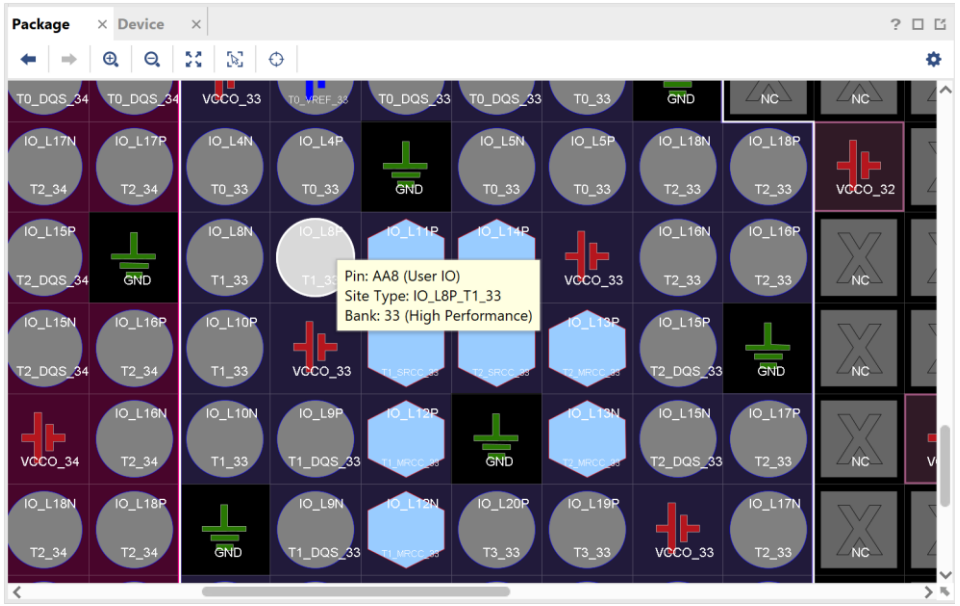


LAB 2

- Step3 Physical Constraints 추가로 설정하기
  - PACKAGE_PIN, PROHIBIT constraints 설정

  - **Layout -> I/O Planning**
  - **I/O Planning view layout** 열기

  - AA8 핀 선택
    - 해당 핀에 오른쪽 마우스 클릭 -> **Set Prohibit** 클릭
    - 오른쪽 그림처럼 해당 포트는 사용금지라는 표시가 뜸



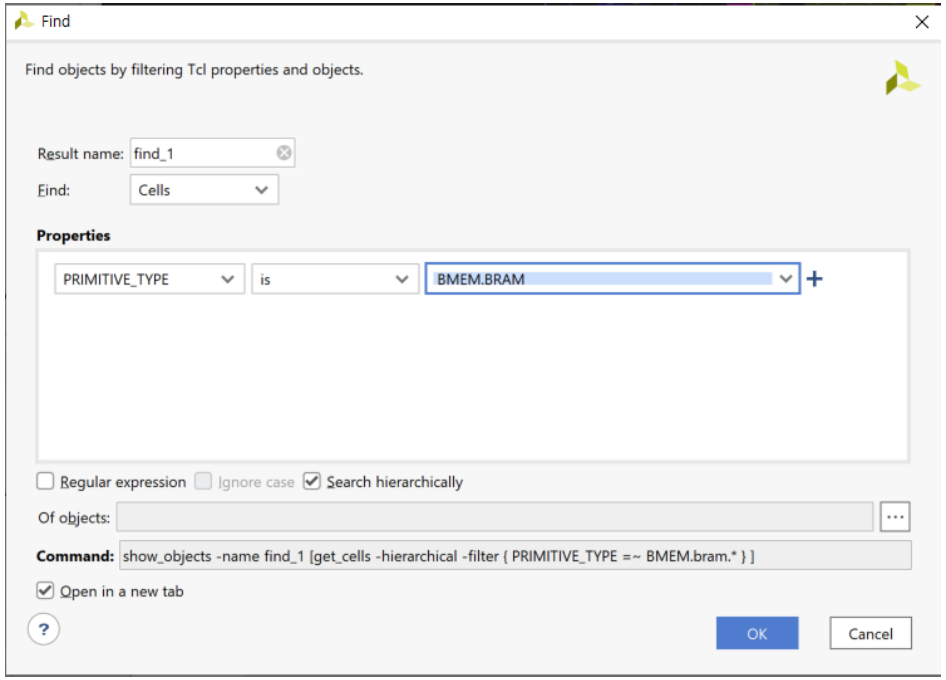
LAB 2

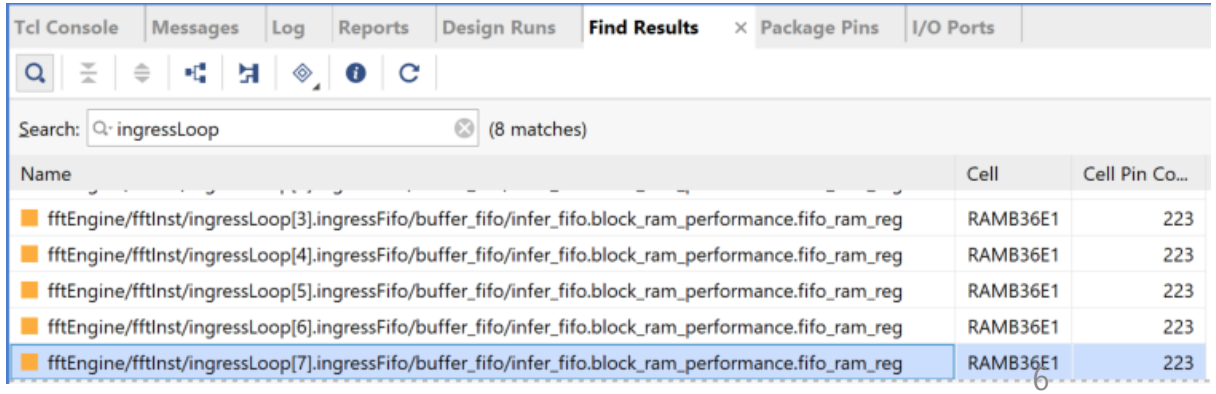
- Step4 Physical Constraints 추가로 설정하기
  - Cell Properties 설정

    - **Edit -> Find** 클릭
    - the Find drop-down list에서, **cells** 선택
    - Properties 칸에서, PRIMITIVE_TYPE을 **BMEM.BRAM**으로 설정
    - **Search Hierarchy** 체크
    - OK 클릭

    - Find Result 탭에서, **ingressLoop** 검색
    - fftEngine/fftInst/ ingressLoop**[7]**.ingressFifo/ 클릭

    - Cell Properties에서, **DOA_REG, DOB_REG 0** 확인





LAB 2

- Step4
  - 다음 Tcl 명령어로 timing report 확인 가능
    - report_timing -from [get_cells fftEngine/fftInst/ ingressLoop[7].ingressFifo/
    - buffer_fifo/infer_fifo.block_ram_performance.fifo_ram_reg]
    - Data path 부분에서, RAMB에 의해 **1.8ns**가 더 소요된 것을 확인 가능
  - Cell Properties에서, **DOA_REG, DOB_REG 1**로 설정
  - 다시 Tcl 명령어로 timing report 확인
    - report_timing -from [get_cells fftEngine/fftInst/ ingressLoop[7].ingressFifo
    - /buffer_fifo/infer_fifo.block_ram_performance.fifo_ram_reg]
    - Data path 부분에서, RAMB에 의해 **0.62ns**가 더 소요된 것을 확인 가능

```
Timing Report

Slack (MET) :              7.255ns  (required time - arrival time)
  Source:                  fftEngine/fftInst/ingressLoop[7].ingressFifo/buffer_fifo/infer_fifo.block_ram_performance.fifo_ram_reg/CLKBWRCLK
                             (rising edge-triggered cell RAMB36E1 clocked by fftClk_0  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:             transformLoop[7].ct/xOutReg_reg/A[0]
                             (rising edge-triggered cell DSP48E1 clocked by fftClk_0  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:              fftClk_0
  Path Type:               Setup (Max at Slow Process Corner)
  Requirement:             10.000ns  (fftClk_0 rise@10.000ns - fftClk_0 rise@0.000ns)
  Data Path Delay:         2.266ns  (logic 1.800ns (79.448%)  route 0.466ns (20.552%))
  Logic Levels:            0
  Clock Path Skew:         -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    -1.820ns = ( 8.180 - 10.000 )
    Source Clock Delay      (SCD):    -2.326ns
    Clock Pessimism Removal (CPR):    -0.651ns
  Clock Uncertainty:       0.074ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Discrete Jitter          (DJ):    0.129ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock fftClk_0 rise edge)
                                                      0.000     0.000 r
                                                      0.000     0.000 r  sysClk (IN)
                         net (fo=0)                   0.000     0.000    sysClk
                         IBUF (Prop_ibuf_I_O)         0.752     0.752 r  clkin1_buf/O
                         net (fo=2, unplaced)         0.466     1.217    clkgen/sysClk_int
    MMCME2_ADV_X1Y0      MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT5)
                                                     -4.686    -3.469 r  clkgen/mmcm_adv_inst/CLKOUT5
                         net (fo=1, unplaced)         0.466    -3.003    clkgen/fftClk_0
                         BUFG (Prop_bufg_I_O)         0.093    -2.910 r  clkgen/clkout6_buf/O
                         net (fo=1468, unplaced)      0.584    -2.326    fftEngine/fftInst/ingressLoop[7].ingressFifo/buffer_fifo/fftClk
                         RAMB36E1                                     r  fftEngine/fftInst/ingressLoop[7].ingressFifo/buffer_fifo/infer_fifo.block_ram_performance.fifo_ram_reg/CLKBWRCLK
  -------------------------------------------------------------------    -------------------
                         RAMB36E1 (Prop_ramb36e1_CLKBWRCLK_DOBDO[16])
                                                      1.800    -0.526 r  fftEngine/fftInst/ingressLoop[7].ingressFifo/buffer_fifo/infer_fifo.block_ram_performance.fifo_ram_reg/DOBDO[16]
                         net (fo=2, unplaced)         0.466    -0.061    fftInst/toBft[15]_55[0]
                         DSP48E1                                      r  transformLoop[7].ct/xOutReg_reg/A[0]
```

```
  -------------------------------------------------------------------    -------------------
                         RAMB36E1 (Prop_ramb36e1_CLKBWRCLK_DOBDO[16])
                                                      0.622    -1.704 r  fftEngine/fftInst/ingressLoop[7].ingressFifo/buffer_fifo/infer_fifo.block_ram_performance.fifo_ram_reg/DOBDO[16]
                         net (fo=2, unplaced)         0.466    -1.239    fftInst/toBft[15]_55[0]
                         DSP48E1                                      r  transformLoop[7].ct/xOutReg_reg/A[0]
  -------------------------------------------------------------------    -------------------
```

LAB 2

- Step4
  - Design Properties 설정

    - 다음 Tcl로 현재 Design의 Properties 종류를 볼 수 있음
      - list_property [current_design]
      - join [list_property [current_design]] ₩n

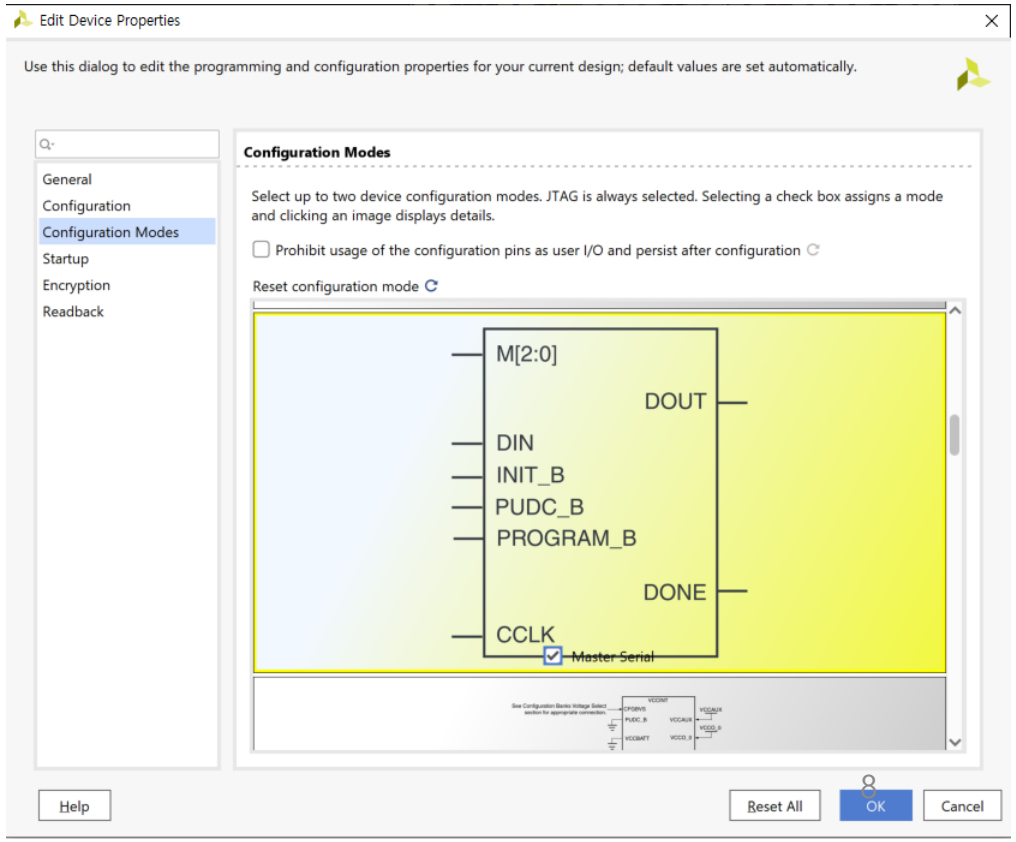
    - **CONFIG_MODE**라는 property가 어떤 value를 가질 수 있는지 다음 Tcl 명령어로 볼 수 있음
      - join [list_property_value CONFIG_MODE [current_design]] ₩n

    - **Tools -> Edit Device Properties**에서, CONFIG_MODE 설정 가능
    - **Configuration Modes** 클릭
    - **Master Serial configuration mode**를 찾아 클릭

    - 다음 Tcl 명령어로 CONFIG_MODE가 잘 set되었는지 확인
      - Get_property CONFIG_MODE [current_design]

    - 설정한 Constraints **저장**

```
join [list_property_value CONFIG_MODE [current_design]] ₩n
SPIx1
SPIx2
SPIx4
M_SERIAL
S_SERIAL
BPI8
BPI16
S_SELECTMAP
S_SELECTMAP16
S_SELECTMAP32
B_SCAN
M_SELECTMAP
```



감사합니다. Q&A...