I/O Clock Planning

28th June 2022

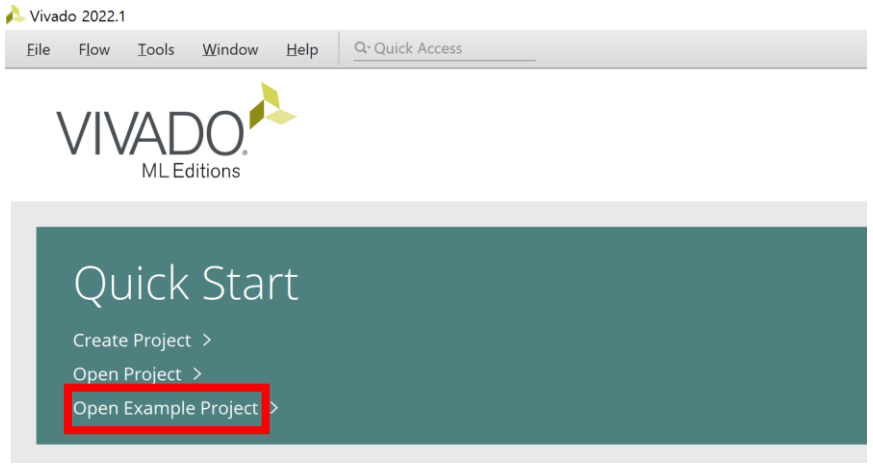
LAB 1

- 이번 Lab을 통해 알 수 있는 것들

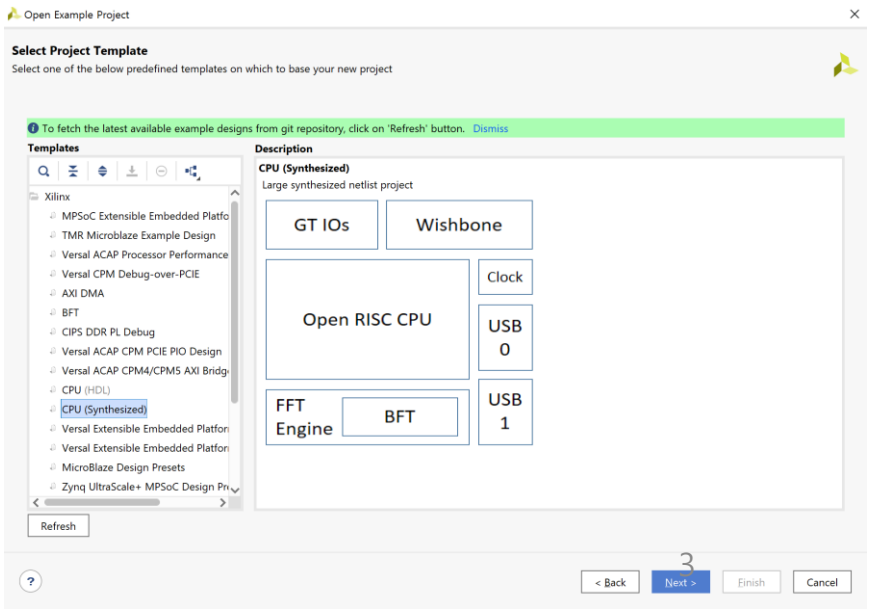
  - How to Create a **constraint set** and set a **target constraint file**
  - How to add **timing constraints** to a design using the **Timing Constraints Wizard**
  - How to add **timing exceptions** using the **Timing Constraints Editor**
  - The importance of **saving constraints** to disk versus in-memory constraints
  - How to generate the **clock interaction report** and properly interpret the resulting matrix
  - How to generate the **timing summary report** and properly interpret the results

LAB 1

- Defining Timing Constraints and Exceptions
- 이번 lab에서는 constraints를 생성하는 2가지 방법을 알아볼 것임

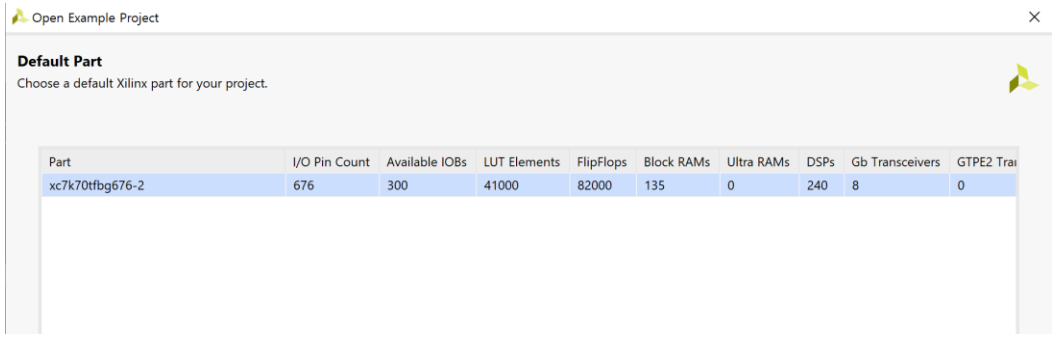


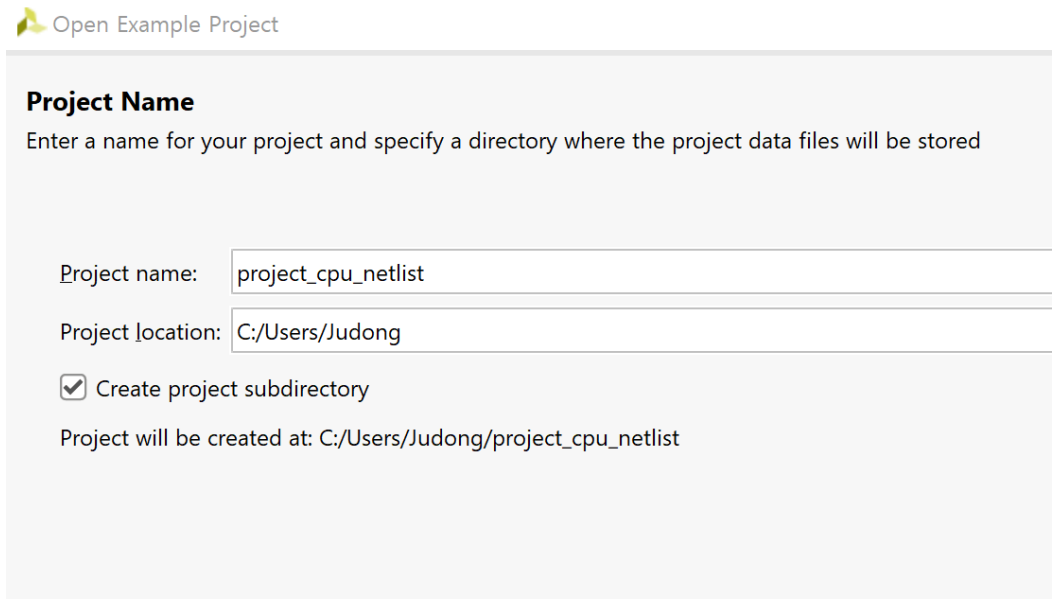
- Step1 예제 프로젝트 열기
  - Start → All Programs → Xilinx Design Tools → Vivado 실행
  - **Open Example Project** 클릭
  - Next 클릭
  - Select Project Template에서, **CPU(Synthesized)** 클릭



LAB 1

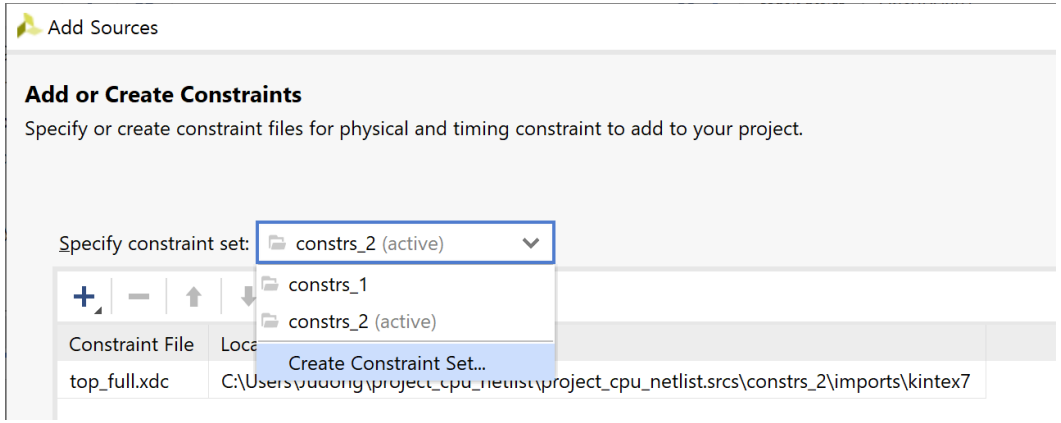
- Step 1
  - Project Name page에서, 다음과 같이 설정
  - Project name: **project_cpu_netlist** (위치는 상관없음)
  - Next 클릭
  - Default Part page에서, default part:
  - **xc7k70tfbg676-2** 입력
  - Next 클릭
  - Finish 클릭 -> 프로젝트 생성

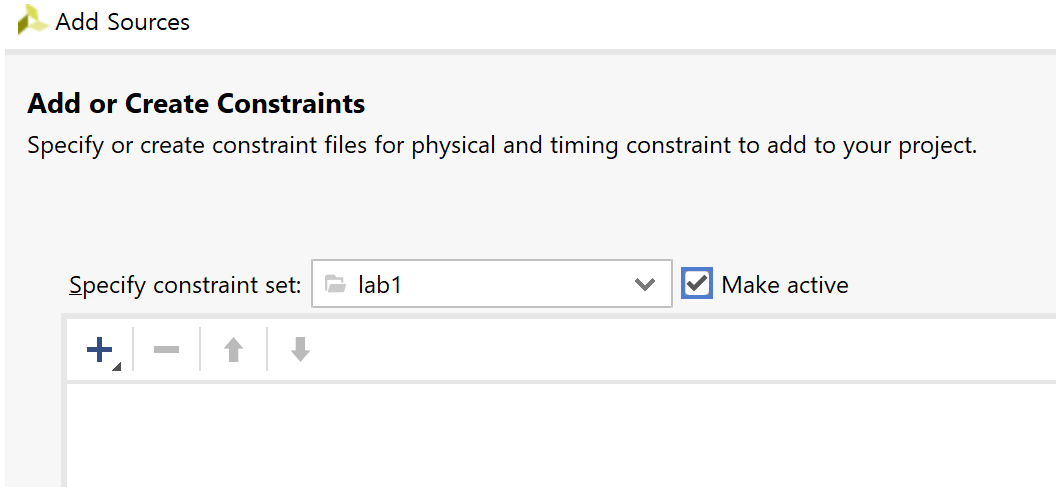




LAB 1

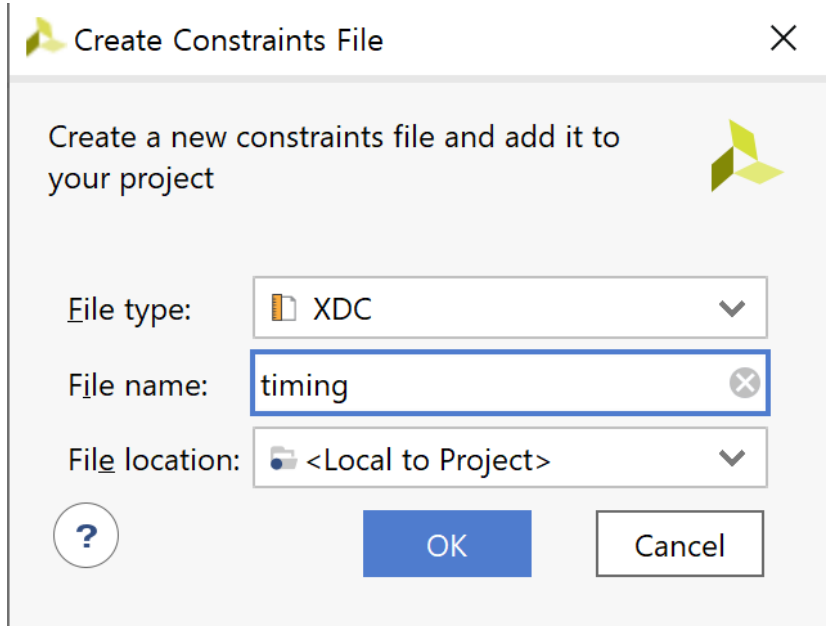
- Step2 Constraint sets와 files 생성하기
  - Flow Navigator에서, Add Source 클릭
  - Add Sources dialog box에서, Add or create constraints 선택
  - Next 클릭
  - Constraint set에서, **Create Constraint Set** 선택
  - Constraint set 이름: lab1 으로 설정
  - OK 클릭
  - Make active 체크
  - Create File 클릭

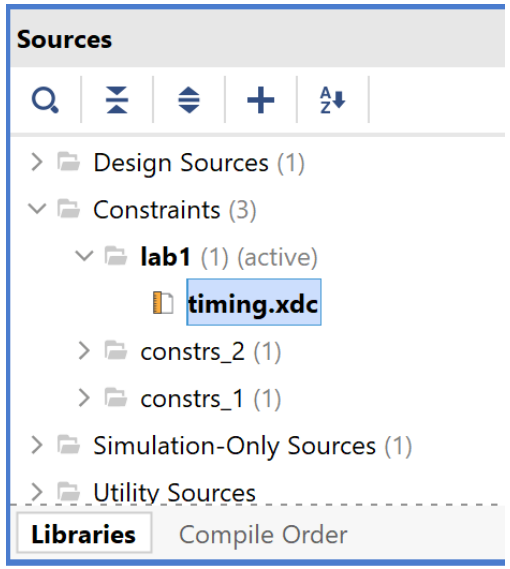




LAB 1

- Step2
  - File type(이름): timing
  - File location: Local to Project
  - OK 클릭 -> timing.xdc 파일이 lab1 constraint set에 추가됨
  - Finish 클릭 -> 새 constraint 파일 생성 완료, 다음 그림과 같이 XDC



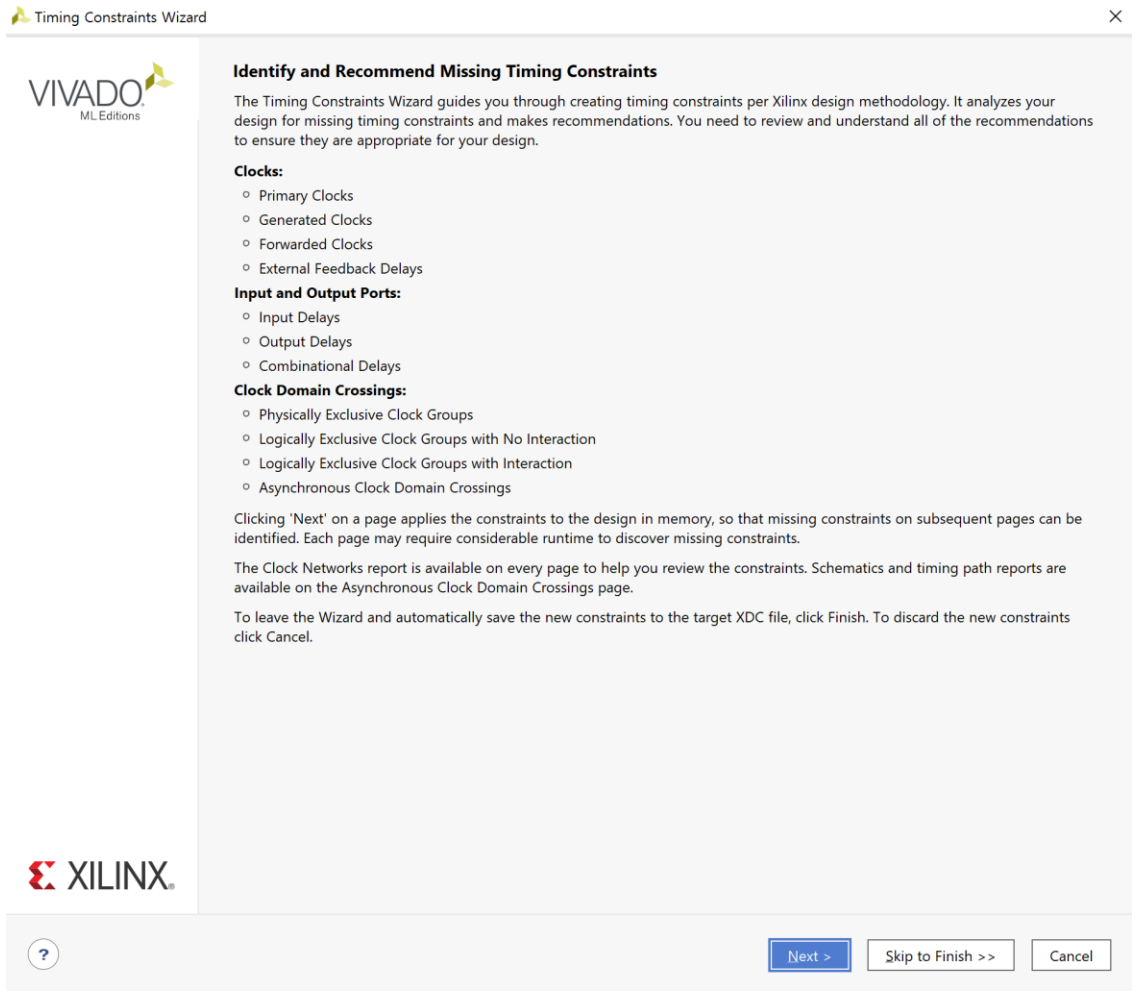


LAB 1

- Step3 Timing Constraints 생성하기
  - Flow Navigator에서, **Open Synthesized Design** 클릭
  - **Constrains Wizard** 클릭

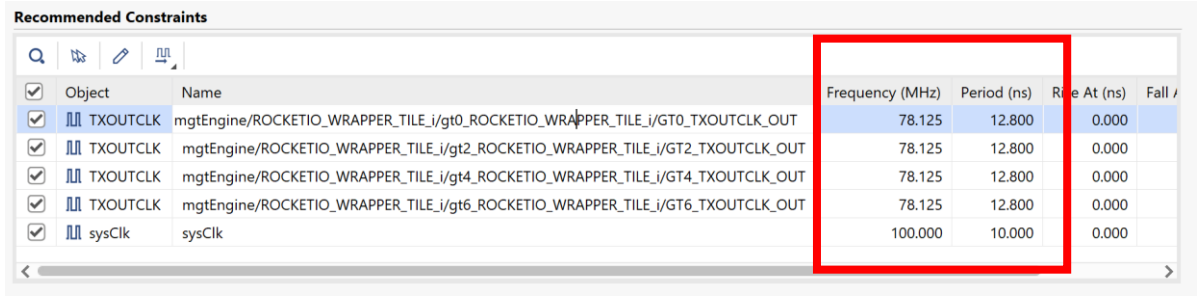
  -> wizard가 생성하는 constraints 종류

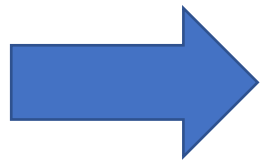
  : Clocks, Input and Output Ports, and Clock Domain Crossings

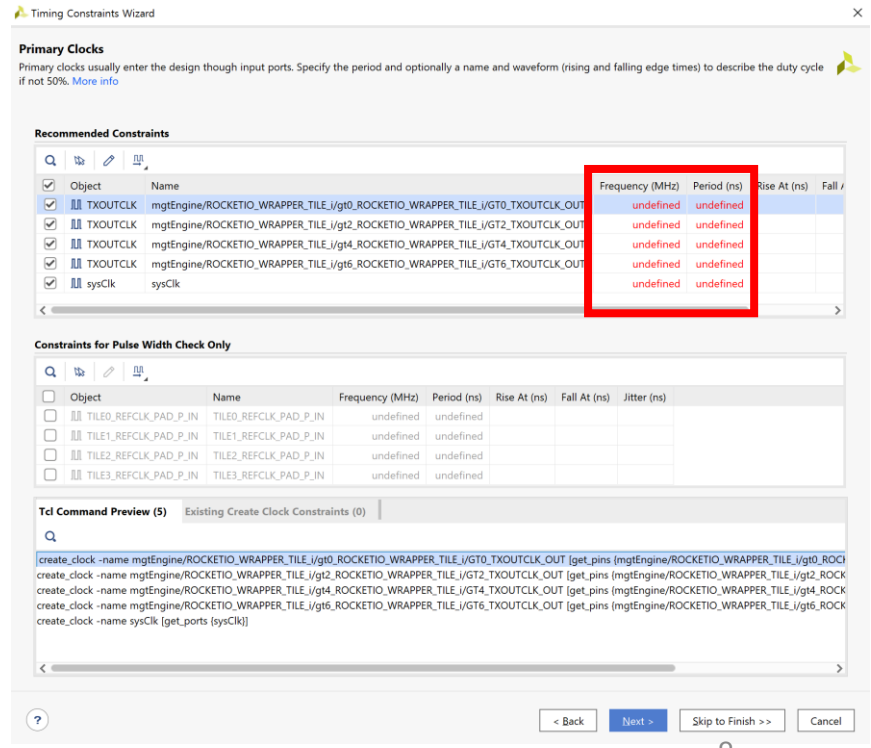


LAB 1

- Step3
  - Next 클릭
  - 그림과 같이 값을 입력 -> Next 클릭 -> Next 클릭 -> Next 클릭
  - (timing constraints primary, in/output clock 설명하면서 설명 필요)







LAB 1

- (Clock순으로 정렬), Input Constraint 값들을 다음과 같이 설정

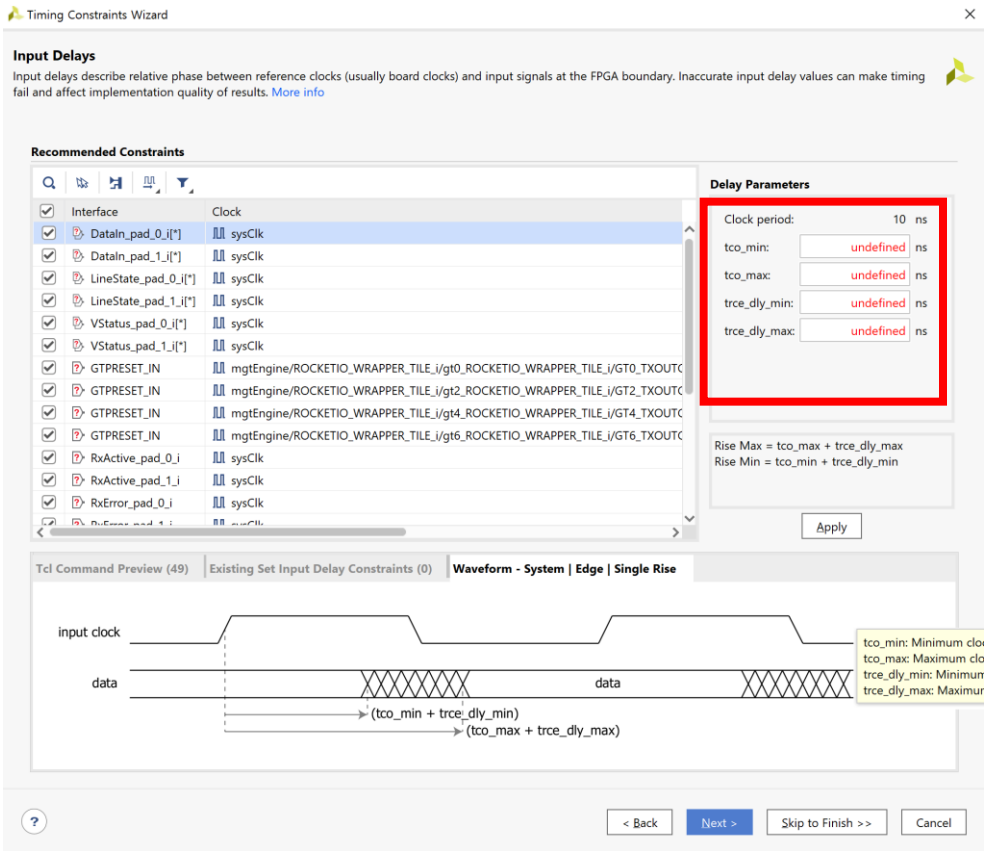


Table 2: **Input Constrain Values**

Interface	Clock	Synchronous	Alignment	Data Rate and Edge	tco_min (ns)	tco_max (ns)	trce_dly_min (ns)	trce_dly_max (ns)
GTPRESET_IN	mgtEngine/...	System	Edge	Single Rise	Uncheck constraint – will false path later			
GTPRESET_IN	mgtEngine/...	System	Edge	Single Rise	Uncheck constraint – will false path later			
GTPRESET_IN	mgtEngine/...	System	Edge	Single Rise	Uncheck constraint – will false path later			
GTPRESET_IN	mgtEngine/...	System	Edge	Single Rise	Uncheck constraint – will false path later			
DataIn_pad_0_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
DataIn_pad_1_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
LineState_pad_0_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
LineState_pad_1_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
VStatus_pad_0_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
VStatus_pad_1_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
RxActive_pad_0_i	sysClk	System	Edge	Single Rise	1	2	1	1
RxActive_pad_1_i	sysClk	System	Edge	Single Rise	1	2	1	1
Rx_Error_pad_0_i	sysClk	System	Edge	Single Rise	1	2	1	1
Rx_Error_pad_1_i	sysClk	System	Edge	Single Rise	1	2	1	1

LAB 1

- Input Constraint 값들을 다음과 같이 설정
- Next 클릭

Table 2: **Input Constrain Values** *(cont'd)*

Interface	Clock	Synchronous	Alignment	Data Rate and Edge	tco_min (ns)	tco_max (ns)	trce_dly_min (ns)	trce_dly_max (ns)
Rx_Valid_pad_0_i	sysClk	System	Edge	Single Rise	1	2	1	1
Rx_Valid_pad_1_i	sysClk	System	Edge	Single Rise	1	2	1	1
TxReady_pad_0_i	sysClk	System	Edge	Single Rise	1	2	1	1
TxReady_pad_1_i	sysClk	System	Edge	Single Rise	1	2	1	1
usb_vbus_paf_0_i	sysClk	System	Edge	Single Rise	1	2	1	1
usb_vbus_paf_1_i	sysClk	System	Edge	Single Rise	1	2	1	1
or1200_clmode	VIRTUAL_cpuClk_5	System	Edge	Single Rise	0.1	2.5	0.1	0.2
or1200_pic_ints	VIRTUAL_cpuClk_5	System	Edge	Single Rise	0.1	2.5	0.1	0.2
reset	VIRTUAL_cpuCLK_5	System	Edge	Single Rise	0.1	2.5	0.1	0.2

LAB 1

- Output constraint 값을 다음과 같이 설정
- (Clock을 클릭해서 정렬)

Table 3: **Output Constraint Values**

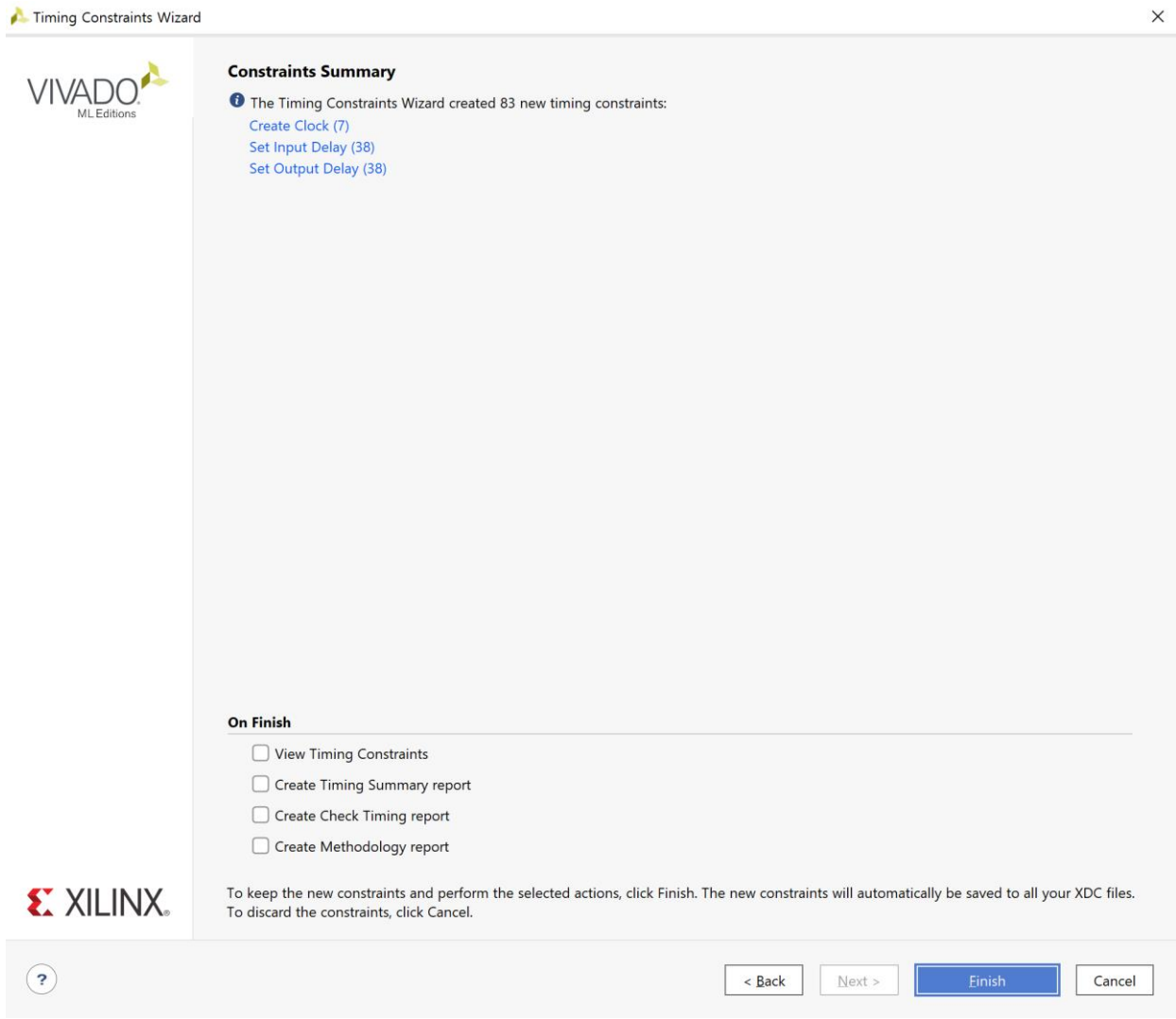
Interface	Clock	Synchronous	Alignment	Data Rate and Edge	tsu (ns)	thd (ns)	trce_dly_max (ns)	trce_dly_min (ns)
OpMode_pad_0_o[*]	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
OpMode_pad_1_o[*]	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
VControl_pad_0_o[*]	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
VControl_pad_0_o[*]	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1

Table 3: **Output Constraint Values** *(cont'd)*

Interface	Clock	Synchronous	Alignment	Data Rate and Edge	tsu (ns)	thd (ns)	trce_dly_max (ns)	trce_dly_min (ns)
SuspendM_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
SuspendM_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
TermSel_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
TermSel_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
TxValid_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
TxValid_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
VControl_Load_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
VControl_Load_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
XcvSelect_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
XcvSelect_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
phy_rst_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
phy_rst_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
DataOut_pad_0_o[*]	VIRTUAL_wbClk_4	System	Setup/Hold	Single Rise	2.1	0.6	0.1	0.0
DataOut_pad_1_o[*]	VIRTUAL_wbClk_4	System	Setup/Hold	Single Rise	2.1	0.6	0.1	0.0
or1200_pm_out[*]	VIRTUAL_wbClk_4	System	Setup/Hold	Single Rise	2.1	0.6	0.1	0.0

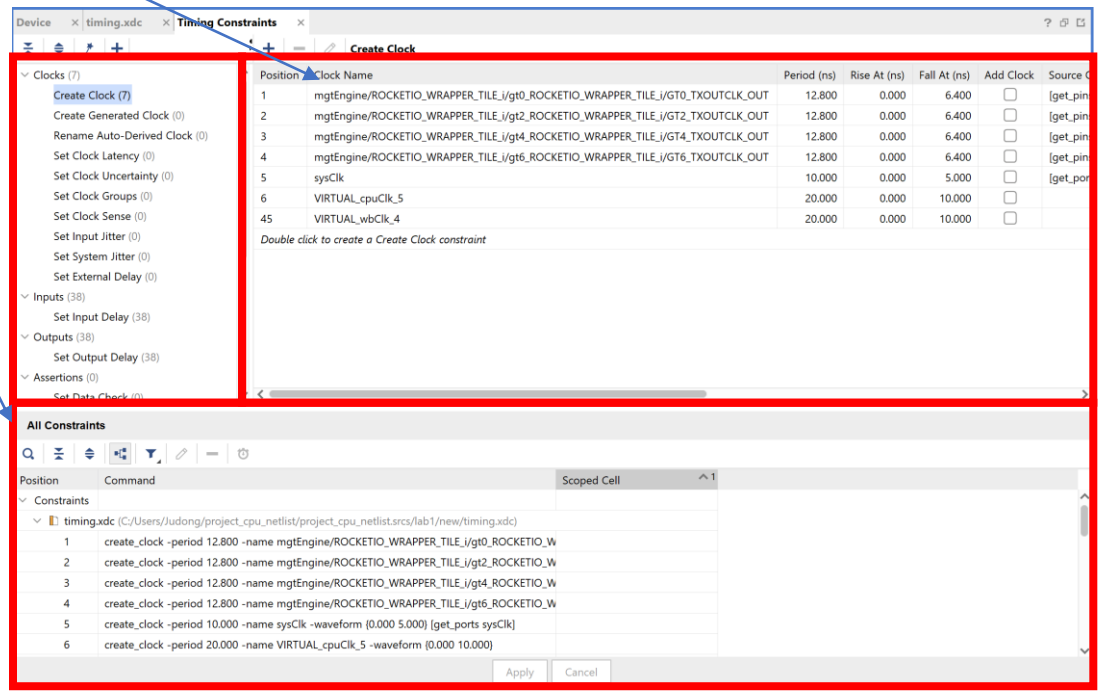
LAB 1

- Next 클릭
- Wizard finish -> Wizard 종료



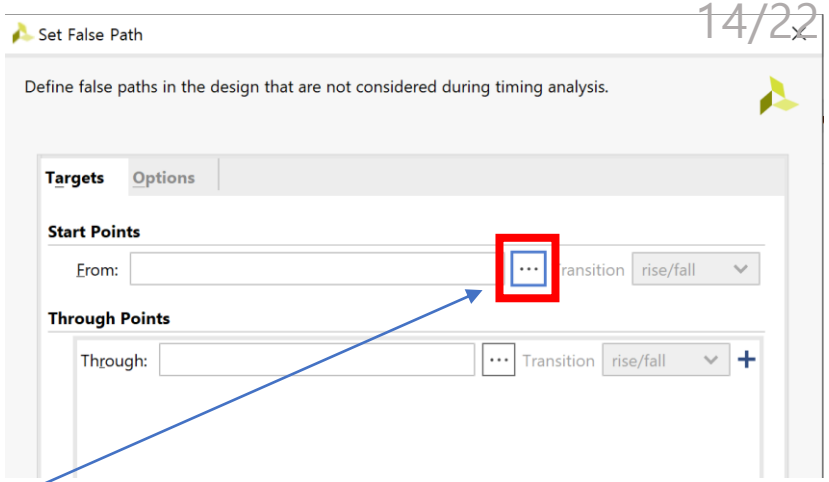
LAB 1

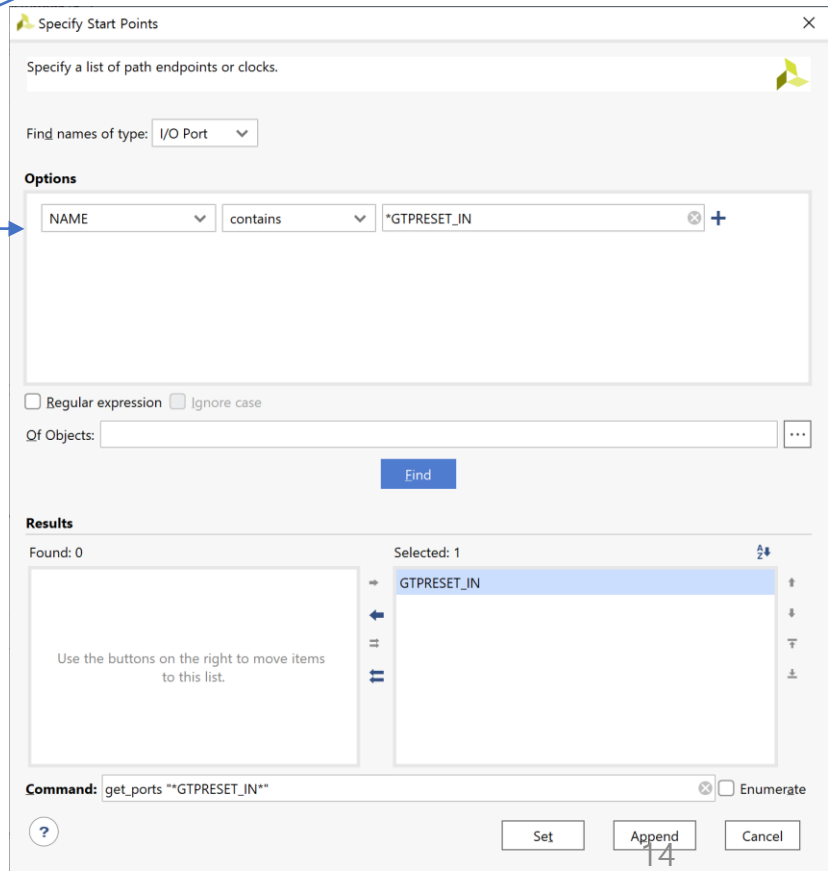
- Step4 **Constraints Editor** 사용하기
  - Synthesized Design에서, **Edit Timing Constraints** 클릭
    - **Constraints tree view**: 카테고리 별로 timing constraints 그룹을 볼 수 있음
    - **Constraints Spreadsheet**: 선택된 그룹의 timing constraints. Constraints Wizard에서 수정했던 것처럼 주기 등을 수정할 수 있음
    - **All Constraints**: design의 모든 Constraints를 다 표시



LAB 1

- Step4 False path exception 생성
  - Constraints tree view에서, **Exception** 카테고리 스크롤
  - **Set False Path** 더블 클릭
  - Start Points 탭에서, Choose Start Points button 클릭
    - Type 이름: **I/O Port**
    - Option: **GTPRESET_IN**
    - Find 클릭
    - Results에서 해당 포트를 선택
    - Set 클릭 -> set false path의 시작포트를 정할 수 있음
  - OK 클릭 -> Timing Constraint Editor 닫음
  - -> **false path exception** 생성

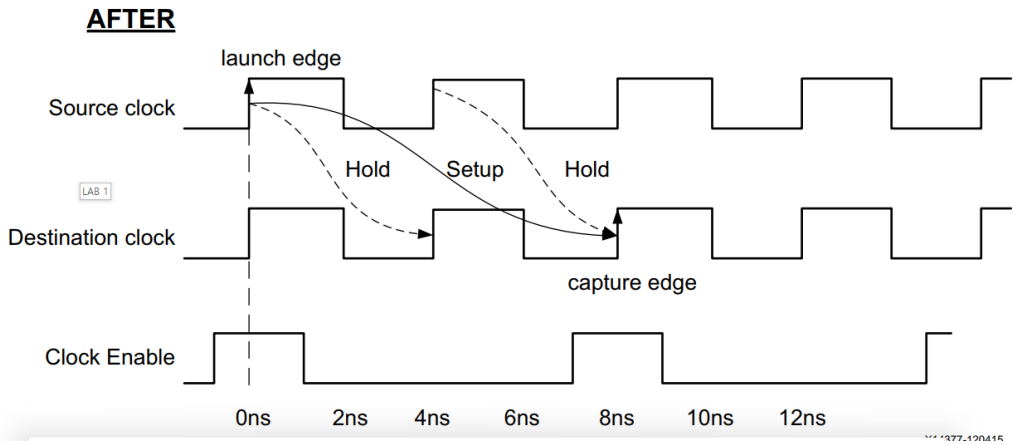


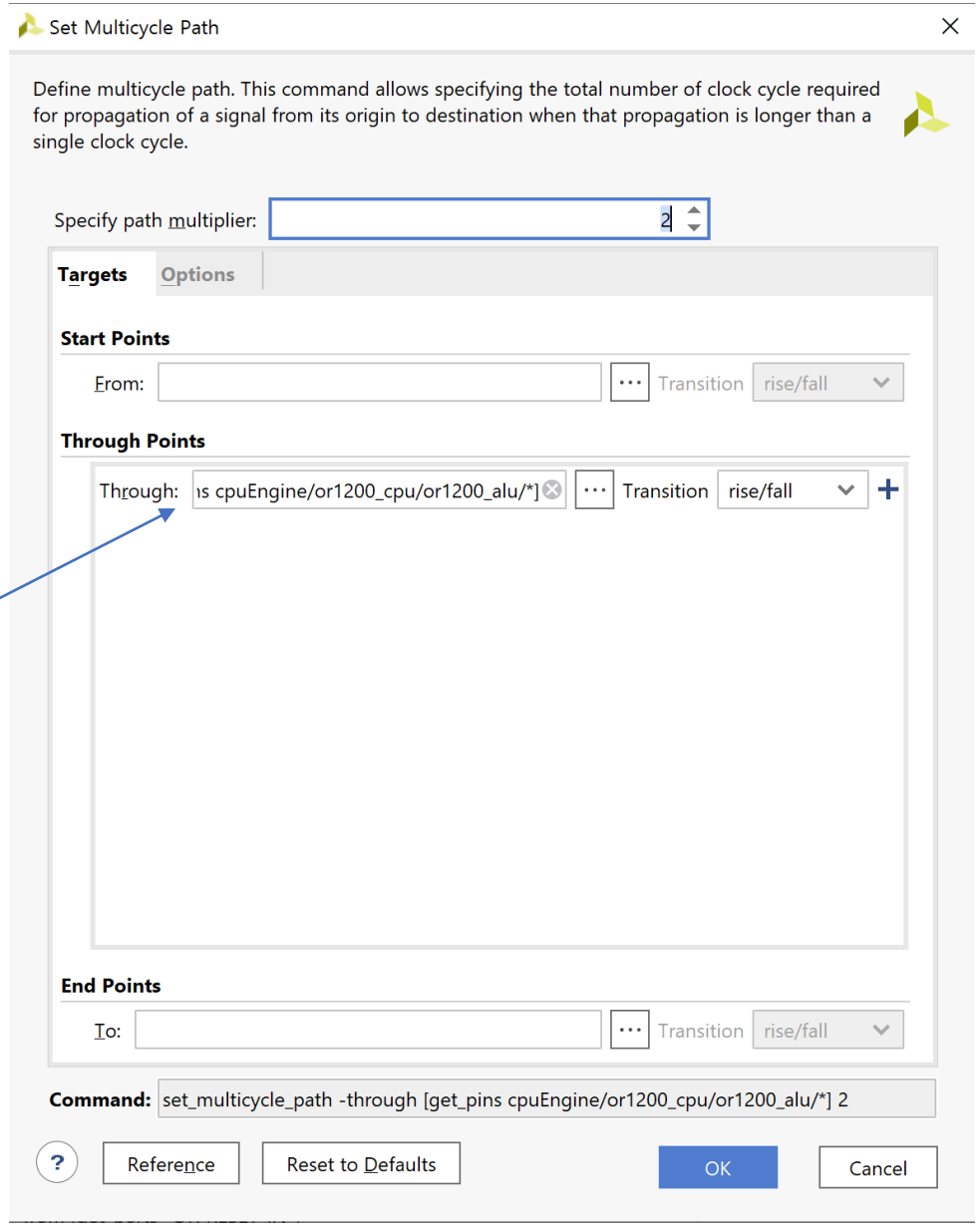


LAB 1

- Step4 MultiCycle Path 추가하기
  - 다시 Exceptions에서, **Set Multicycle Path** 더블 클릭
  - Path multiplier: **2**로 설정
  - **Through entry box**에서,
  - [get_pins cpuEngine/or1200_cpu/or1200_alu/*] 입력
  - OK 클릭

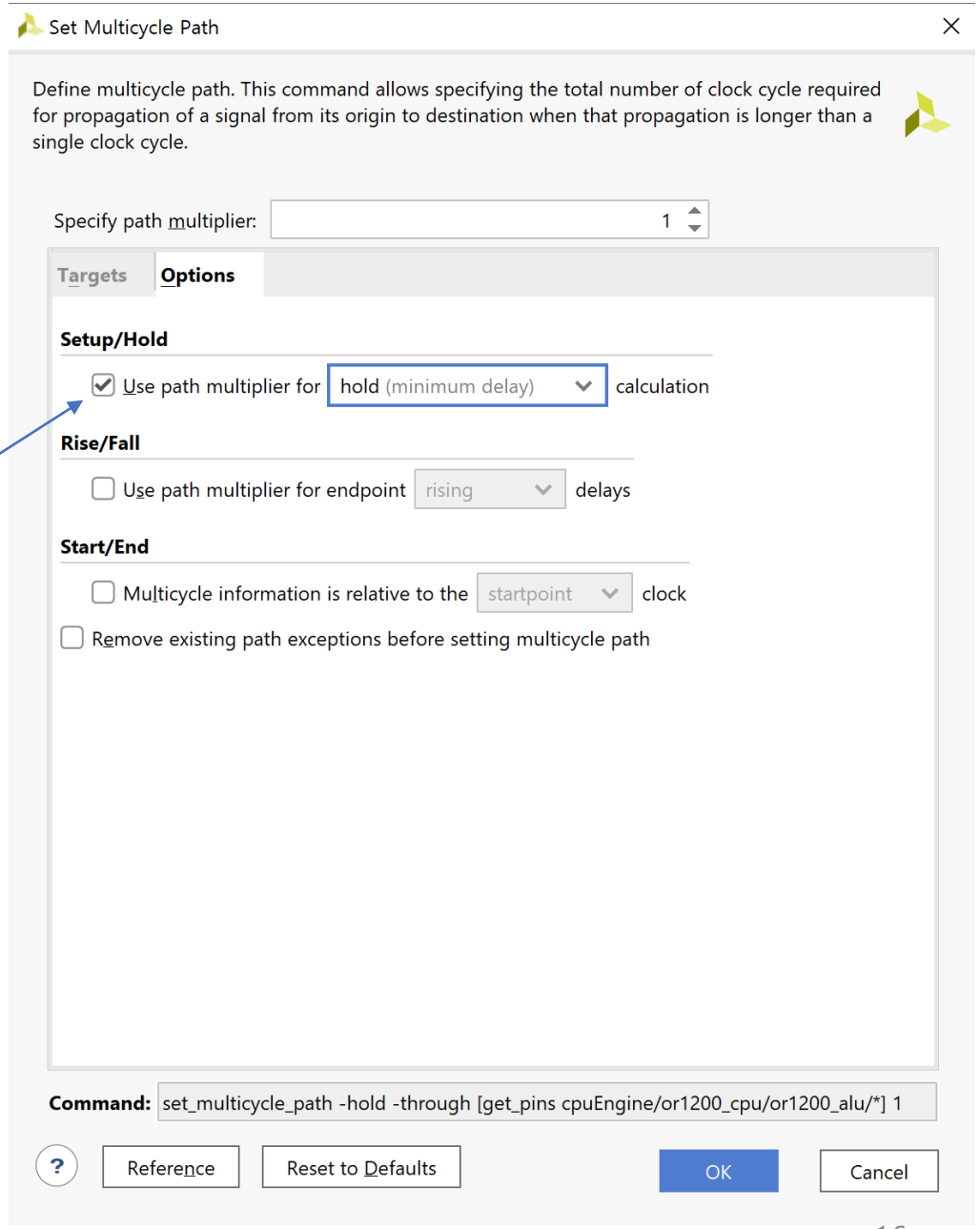
  -> multicycle path가 생성된 것을 알 수 있음





LAB 1

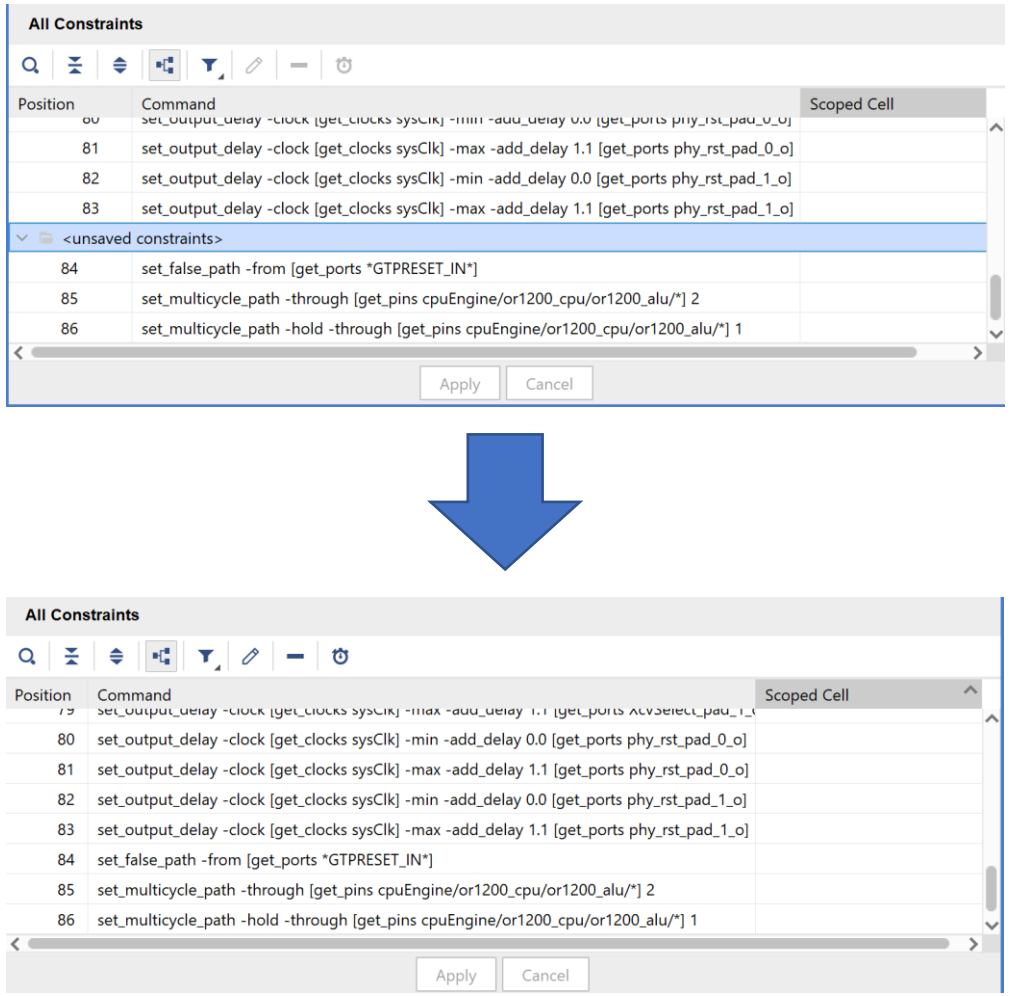
- Step4
  - 다시 **Set multicycle path**를 더블클릭
  - Pass multiplier를 **1**로 설정
  - **Option** 탭 클릭
  - Setup/Hold 탭에서, **Use path multiplier** 체크'
  - OK 클릭



LAB 1

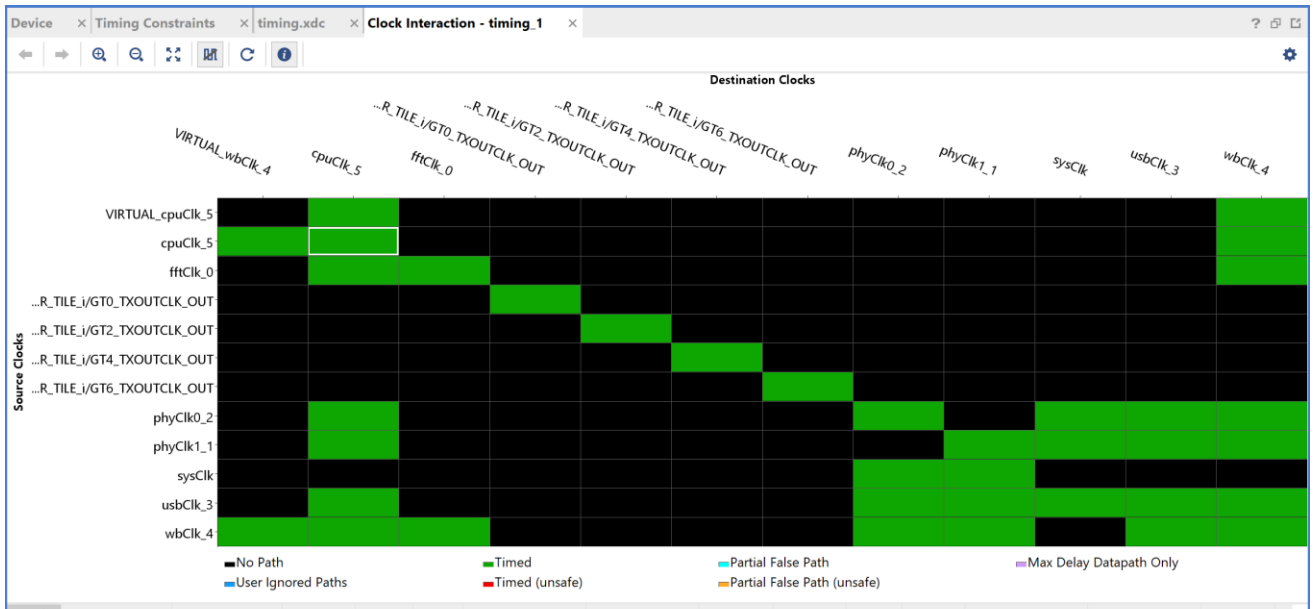
- Step5 Constraints 저장
  - 앞에서 설정한 setting들은 아직 저장되지 않은 상태임
  - 따라서 설정한 exceptions을 timing.xdc 파일에 저장해야 함

  - Sources 탭 – Constraints – timing.xdc 더블 클릭
  - Constraints 목록에서 스크롤
  - -> set_false_path, set_multicycle_path constraints 저장 아직 안됨
  - **File – Constraints – Save As** 
  - Constraints 저장
  - 2개의 constraints가 저장됨을 확인



LAB 1

- Step6 Clock Interaction Report
  - Synthesized Design -> **Report Clock Interaction**
  - 모든 설정 Default -> OK 클릭

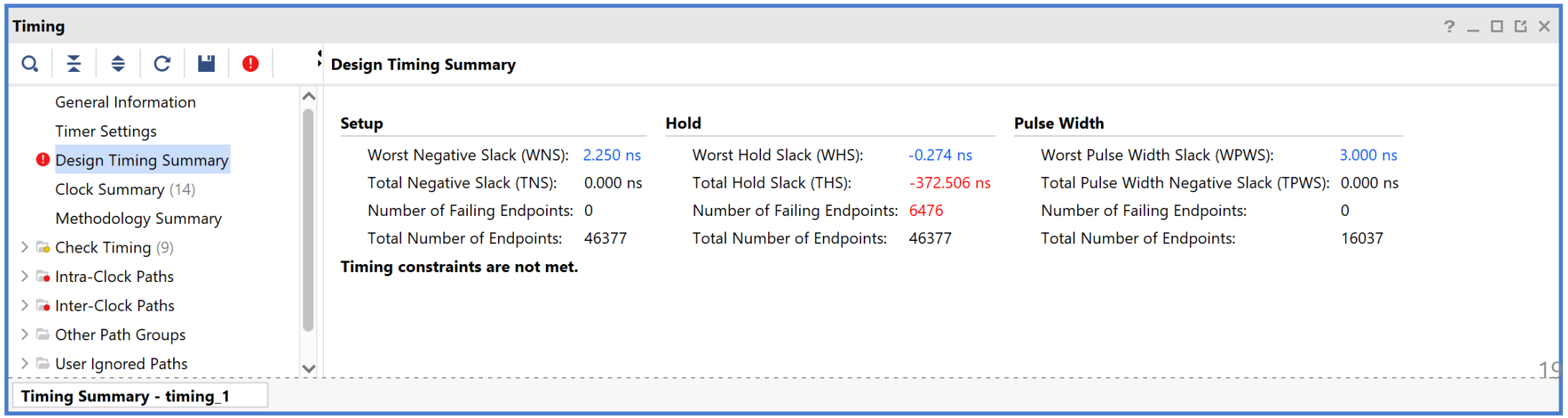


Id	Source Clock	Destination Clock	Edges (WNS)	WNS (ns)	TNS (ns)	Failing Endpoints (TNS)	Total Endpoints (TNS)	Path Req (WNS)	Edges (WHS)	WHS (ns)	THS (ns)	Failing Endpoints (THS)	Total Endpoints (THS)	Path Req (WHS)
17	phyClk0_2	usbClk_3	rise - rise	6.758	0.000	0	976	10.000	rise - rise	-0.149	-33.695	338	976	0.000
18	phyClk0_2	phyClk0_2	rise - rise	5.114	0.000	0	5958	10.000	rise - rise	0.000	0.000	0	5958	0.000
19	phyClk0_2	cpuClk_5	rise - rise	6.399	0.000	0	61	10.000	rise - rise	0.457	0.000	0	61	0.000
20	phyClk0_2	wbClk_4	rise - rise	7.760	0.000	0	7	10.000	rise - rise	0.276	0.000	0	7	0.000
21	cpuClk_5	cpuClk_5	rise - rise	12.312	0.000	0	5757	20.000	rise - rise	-0.072	-7.497	104	5757	0.000
22	cpuClk_5	wbClk_4	rise - rise	14.532	0.000	0	374	20.000	rise - rise	-0.160	-15.380	134	374	0.000

LAB 1

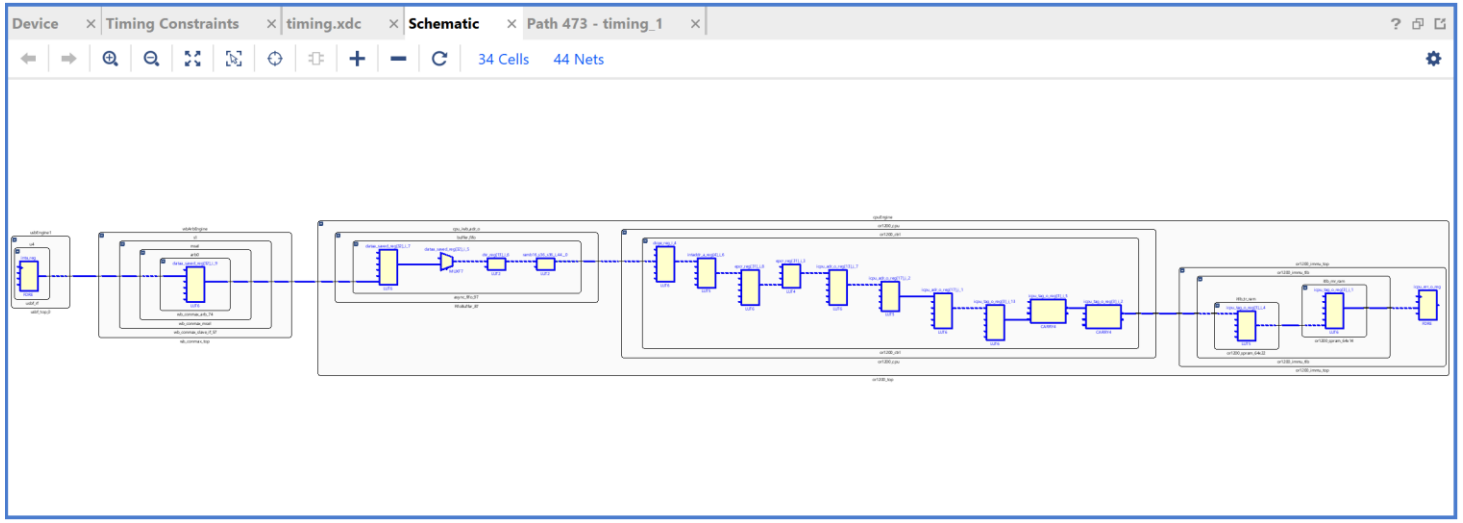
- Step7 Timing Summary Report

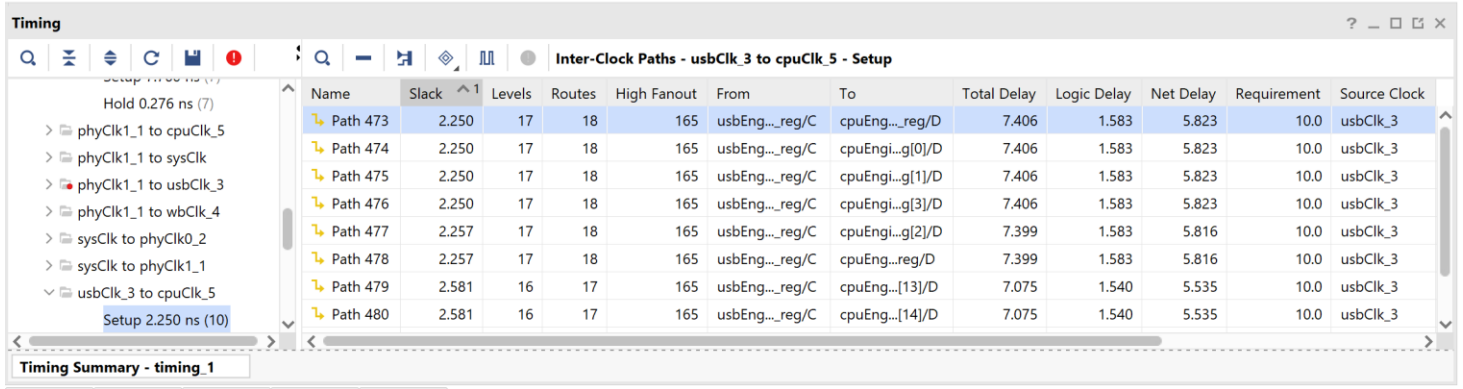
  - Reports -> Timing -> **Report Timing Summary**
  - 모든 설정 Default -> OK 클릭
  - 그림과 같이 Timing Summary 생성
  - **Worst Negative Slack** 클릭
  - -> 해당 design에서 worst timing path를 확인할 수 있음



LAB 1

- Step7
  - **F4**를 누르면 그 path를 Schematic으로 관찰가능

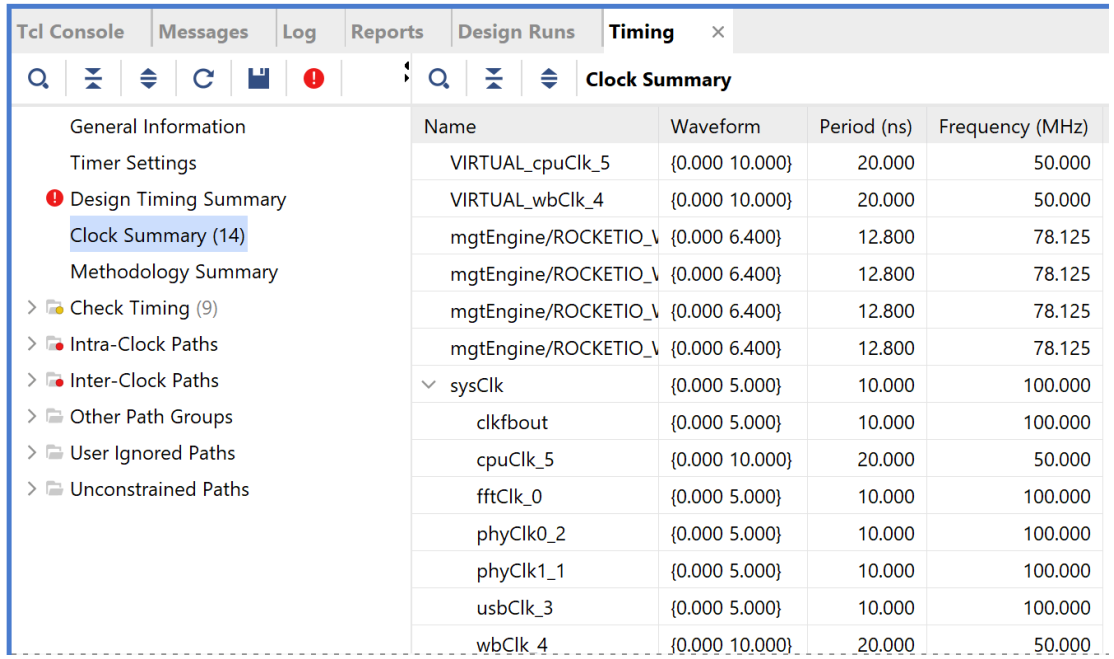




Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 473	2.250	17	18	165	usbEng..._reg/C	cpuEng..._reg/D	7.406	1.583	5.823	10.0	usbClk_3
Path 474	2.250	17	18	165	usbEng..._reg/C	cpuEngi...g[0]/D	7.406	1.583	5.823	10.0	usbClk_3
Path 475	2.250	17	18	165	usbEng..._reg/C	cpuEngi...g[1]/D	7.406	1.583	5.823	10.0	usbClk_3
Path 476	2.250	17	18	165	usbEng..._reg/C	cpuEngi...g[3]/D	7.406	1.583	5.823	10.0	usbClk_3
Path 477	2.257	17	18	165	usbEng..._reg/C	cpuEngi...g[2]/D	7.399	1.583	5.816	10.0	usbClk_3
Path 478	2.257	17	18	165	usbEng..._reg/C	cpuEng...reg/D	7.399	1.583	5.816	10.0	usbClk_3
Path 479	2.581	16	17	165	usbEng..._reg/C	cpuEng...[13]/D	7.075	1.540	5.535	10.0	usbClk_3
Path 480	2.581	16	17	165	usbEng..._reg/C	cpuEng...[14]/D	7.075	1.540	5.535	10.0	usbClk_3

LAB 1

- Step7
  - timing summary tree에서, Clock Summary 선택
  - 해당 design의 모든 clock들 확인 가능
  - Clock들의 **frequency, 주기, waveform(최소, 최대값)** 확인 가능
  - sysClk에 속해있는 clock들은 sysClk에 관계가 있음
    - 예를 들어, cpuClk_5는 sysClk로부터 생성되었고 주기는 sysClk의 2배라는 것을 알 수 있음
  - Timing 탭의 나머지 부분들은 종류 별로 묶인 path 그룹들임



Lab2…