Lab05 Pipeline

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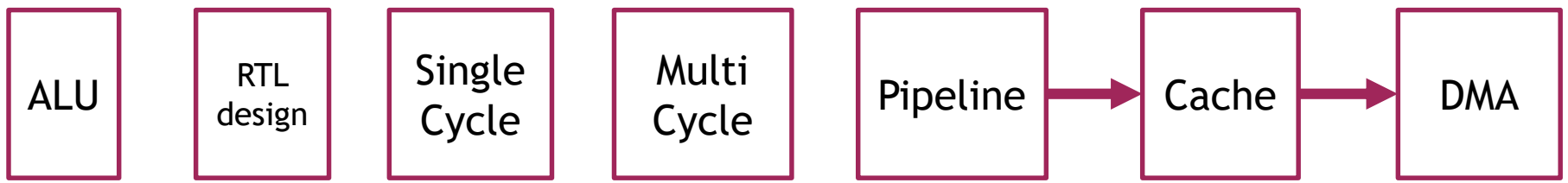
Lab Dependency

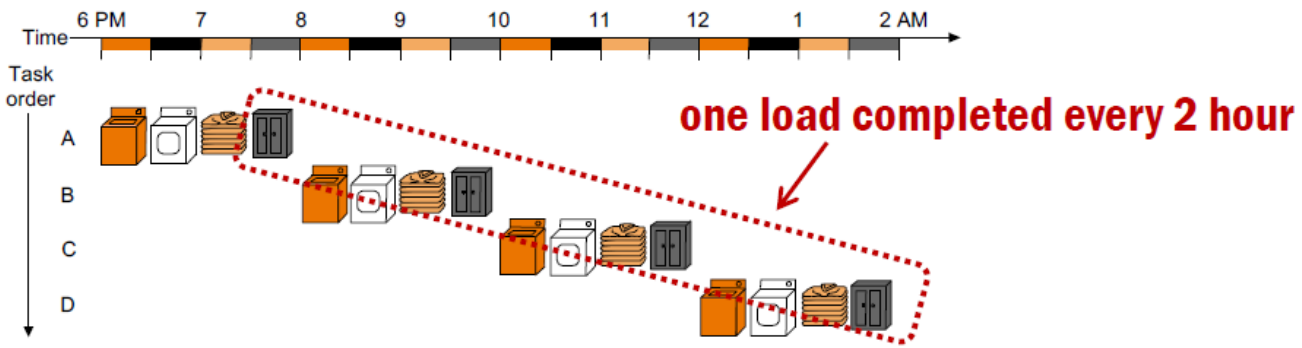


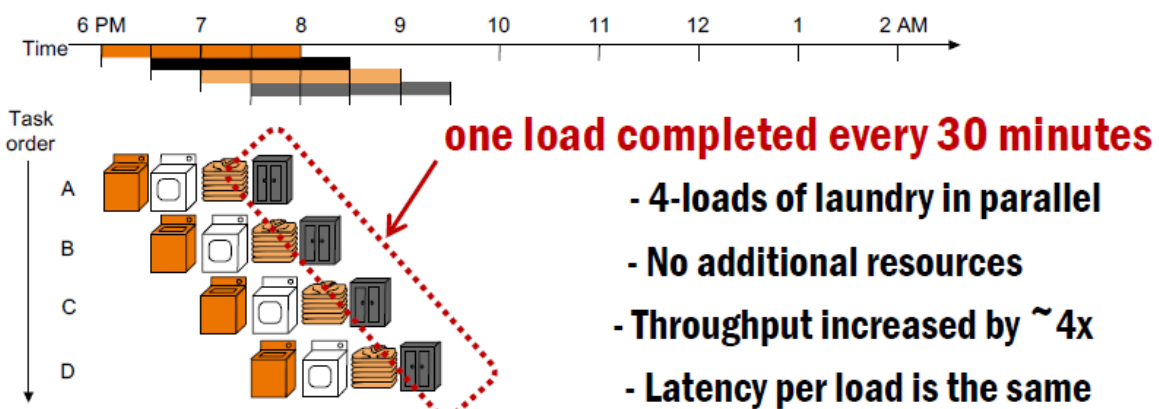
- From now on, you have to complete your assignment to start the next one.
- Your implementation should be functionally correct.
- So please start early! (This one will take a long time…)

Objective

- To understand the reason why pipelined CPUs have better throughput
- To understand data & control hazards and how to solve them
- To design and implement the pipelined CPU

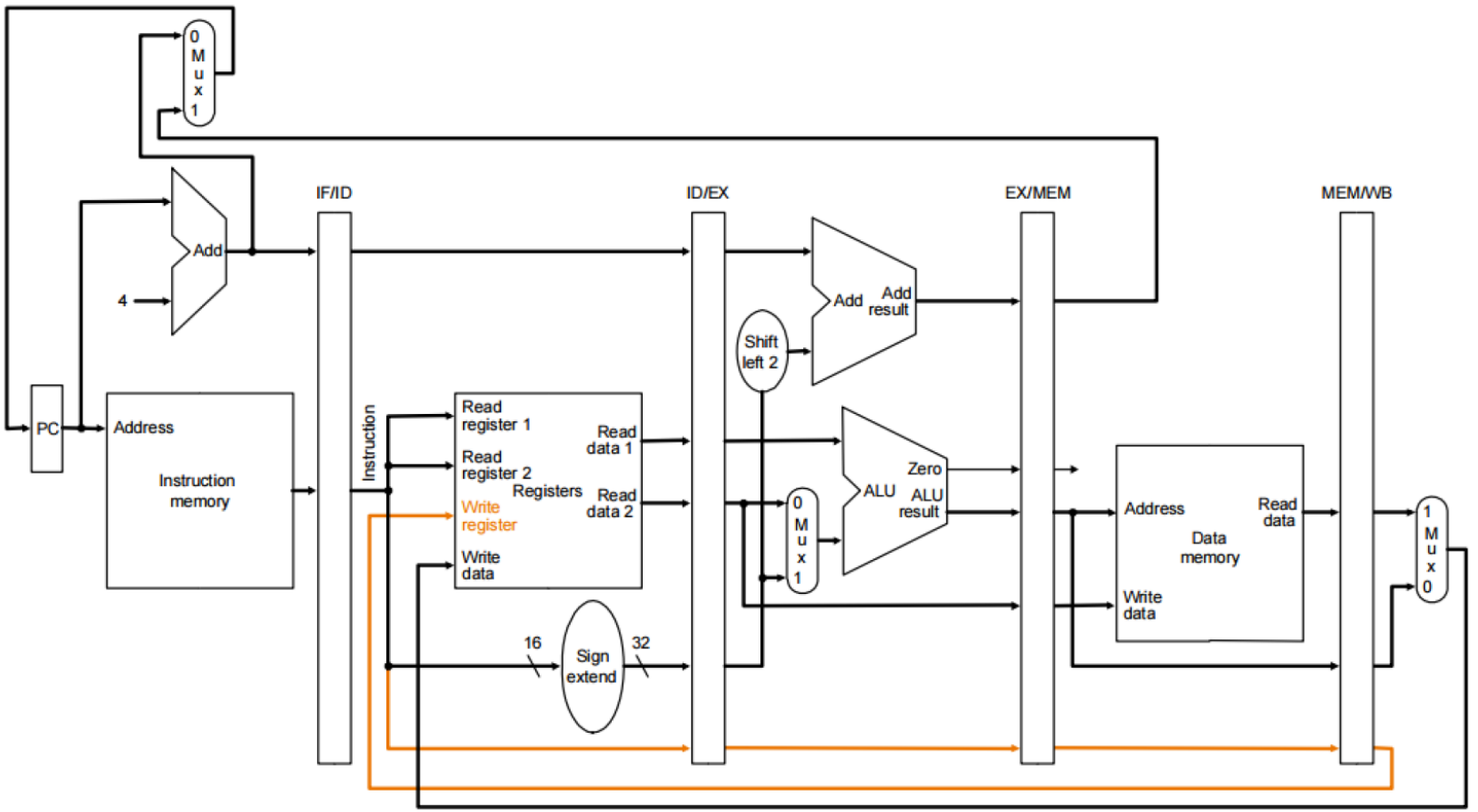
Why Do We Use Pipeline?



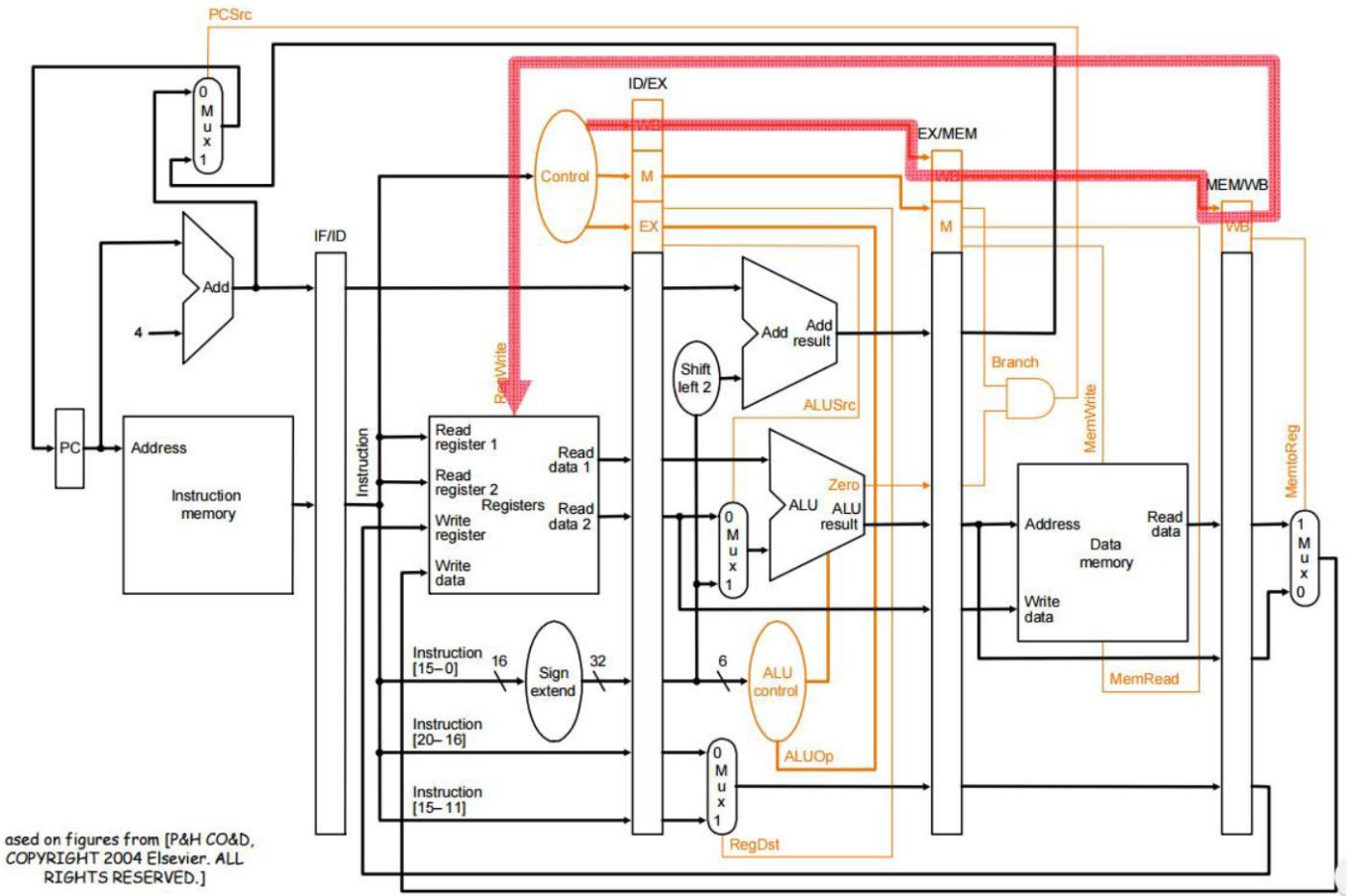


- 4-loads of laundry in parallel
- No additional resources
- Throughput increased by ~4x
- Latency per load is the same

Pipeline: Datapath



Pipeline: Control



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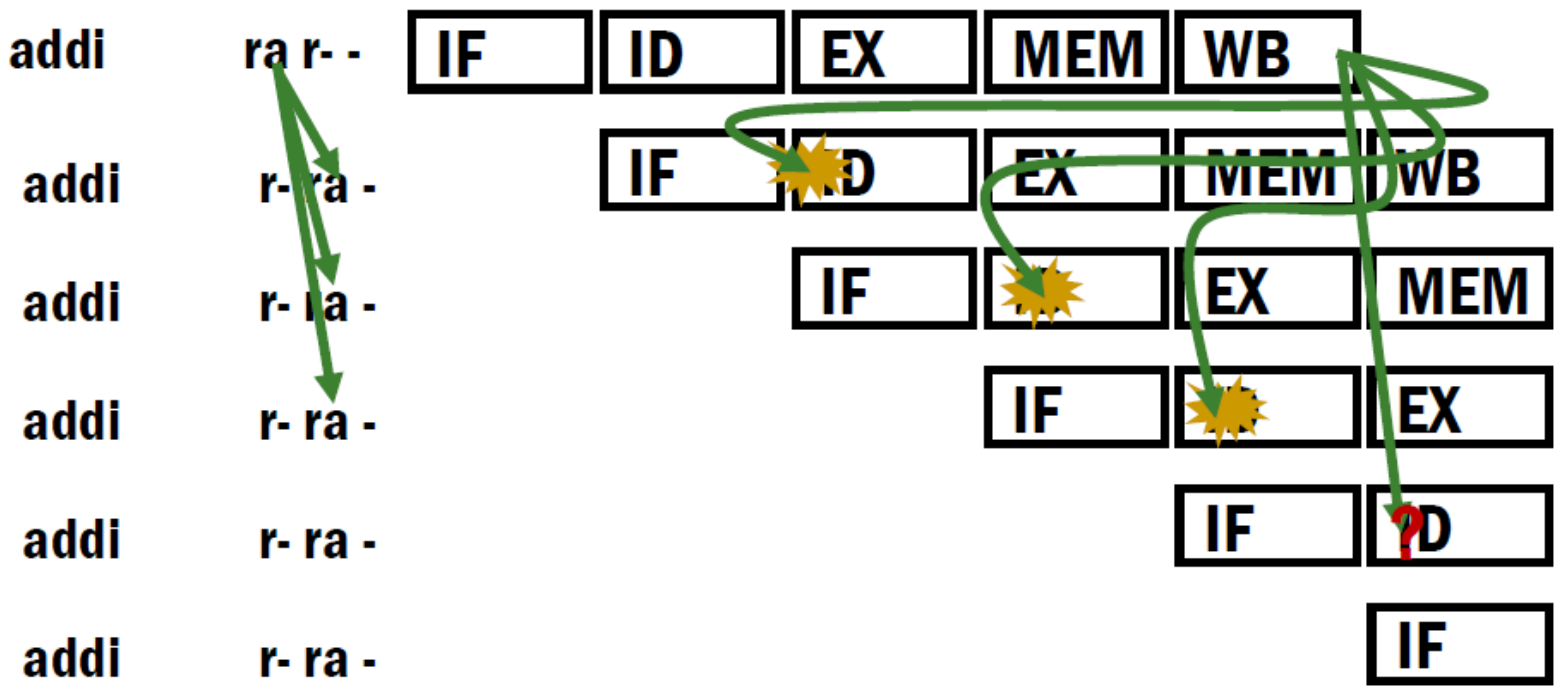
Hazards

- Pipeline hazards: the next instruction cannot execute in following clock cycle.
  - Data hazard
  - Control hazard
  - Structural hazard

Data Hazard


addi ra r- -
addi r- ra -
addi r- ra -
addi r- ra -
addi r- ra -
addi r- ra -
IF
ID
EX
MEM
WB
IF
D
EX
MEM
WB
IF
EX
MEM
IF
EX
IF
?D
IF

Data Hazard - Stall

	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
IF	i	j	k	k	k	k	l				
ID	h	i	j	j	j	j	k	l			
EX		h	i	bub	bub	bub	j	k	l		
MEM			h	i	bub	bub	bub	j	k	l	
WB				h	i	bub	bub	bub	j	k	l

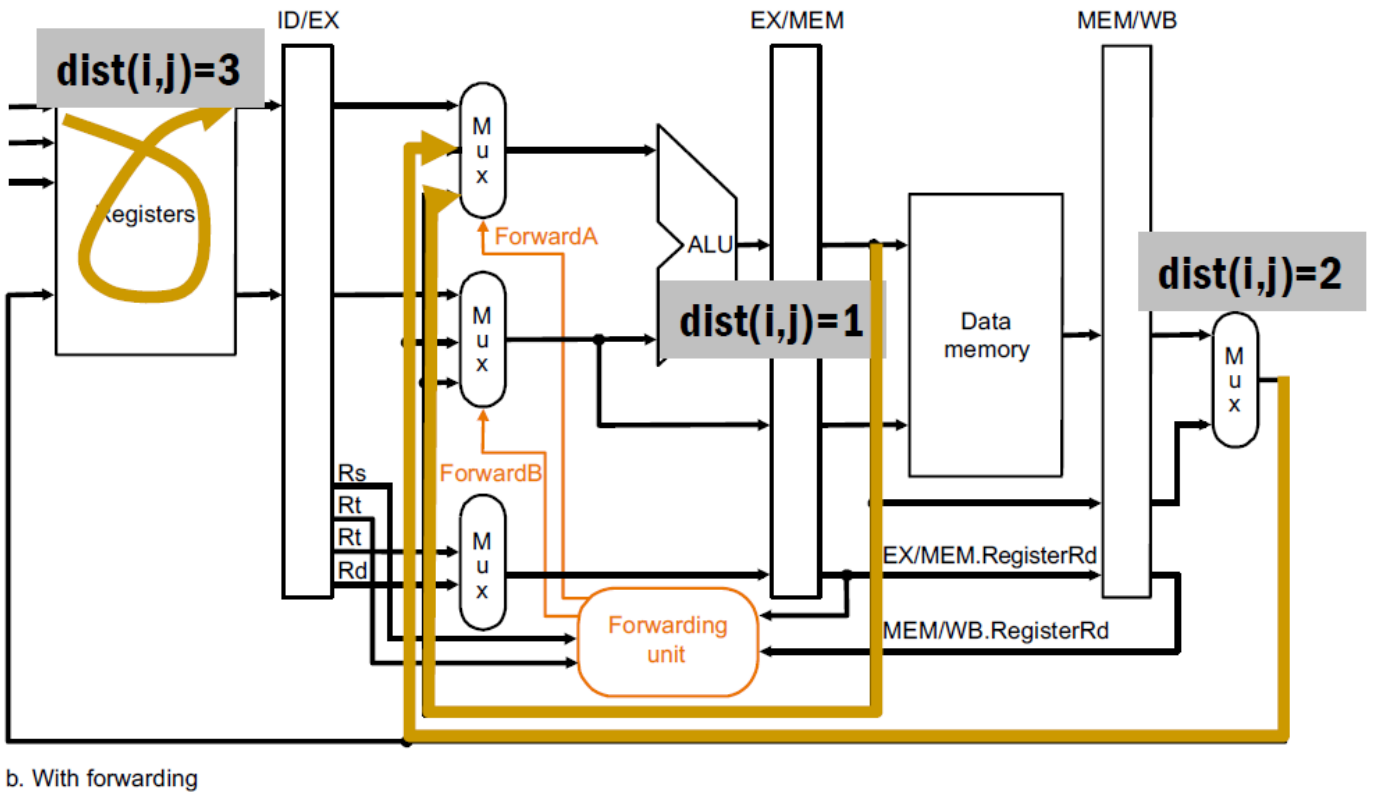
i: rx ← _

j: _ ← rx

For this "updating register file in clock negative edge will be allowed!"

You will see why negedge is needed on register file update

Data Hazard – Forwarding (Extra Credit)



b. With forwarding

Implementing forwarding is one of the extra credit!

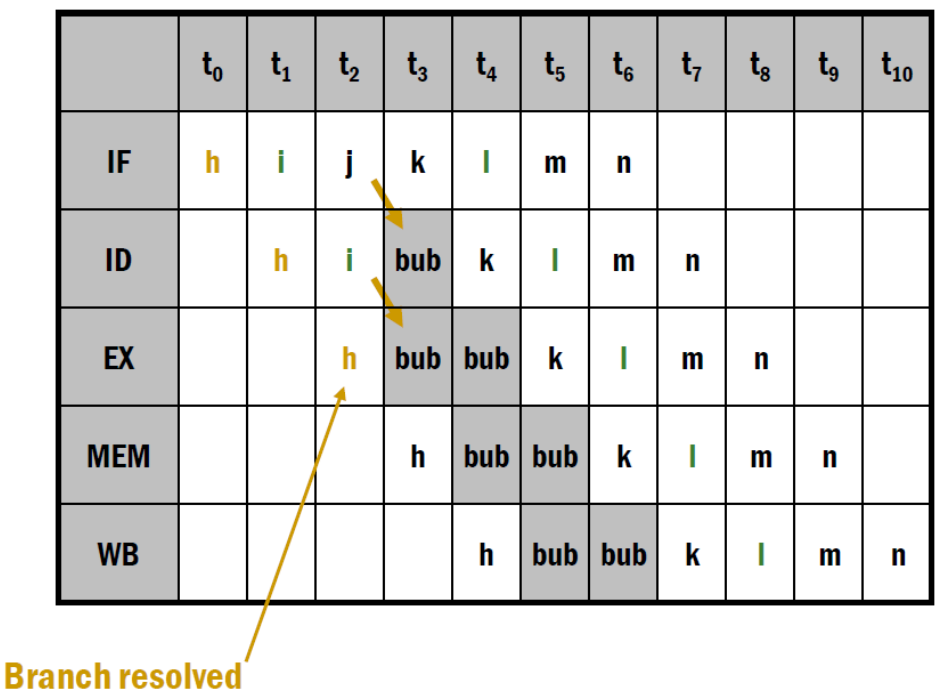
Control Hazard

	R/I-Type	LW	SW	Br	J	Jr
IF	use	use	use	use	use	use
ID	produce	produce	produce		produce	produce
EX				produce		
MEM						
WB						

- PC hazard distance is at least 1
- Does that mean we must stall after every instruction?
  - IF stage can't know which PC to fetch next until the current PC is fetched and decoded

Control Hazard - Flush

- You need to predict next PC as PC + 4
- Flush on miss prediction
- Read textbook and lecture slides
- This is not optional!



Control Hazard – Branch Prediction (Extra Credit)

- Always not taken (no extra credit)
- Always taken
- 2 bit global prediction (full extra credit for branch prediction)

----------<Just for your highly motivated students>----------

- Gshare
- Two-Level predictor
- Etc.

Requirements

- Implement the pipelined CPU
- Compare the performance of multi-cycle CPU and pipeline CPU – write on report
- *Your implementation should be functionally correct!*
  - *The last test bench will be passed only if your implementation is functionally correct!*