CSED311 Lab3: Single Cycle CPU

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- Modularization
- Magic memory
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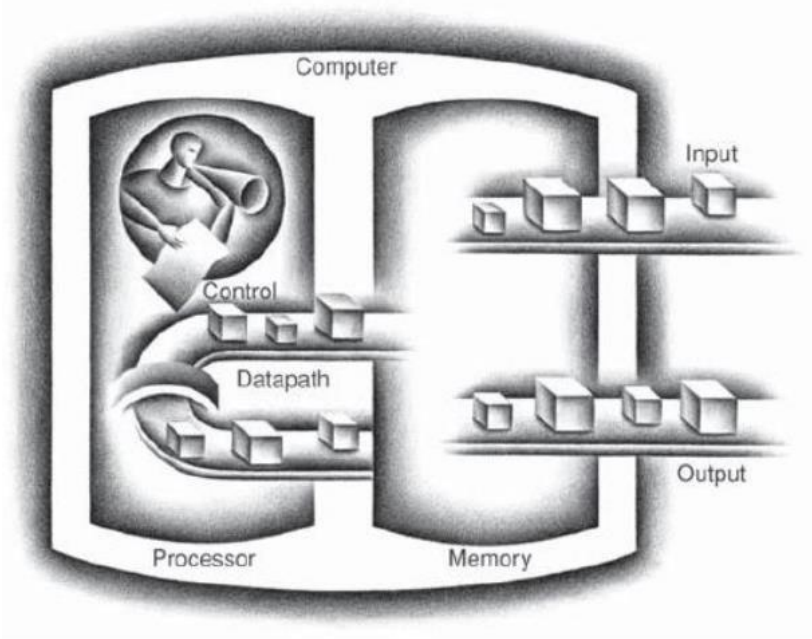
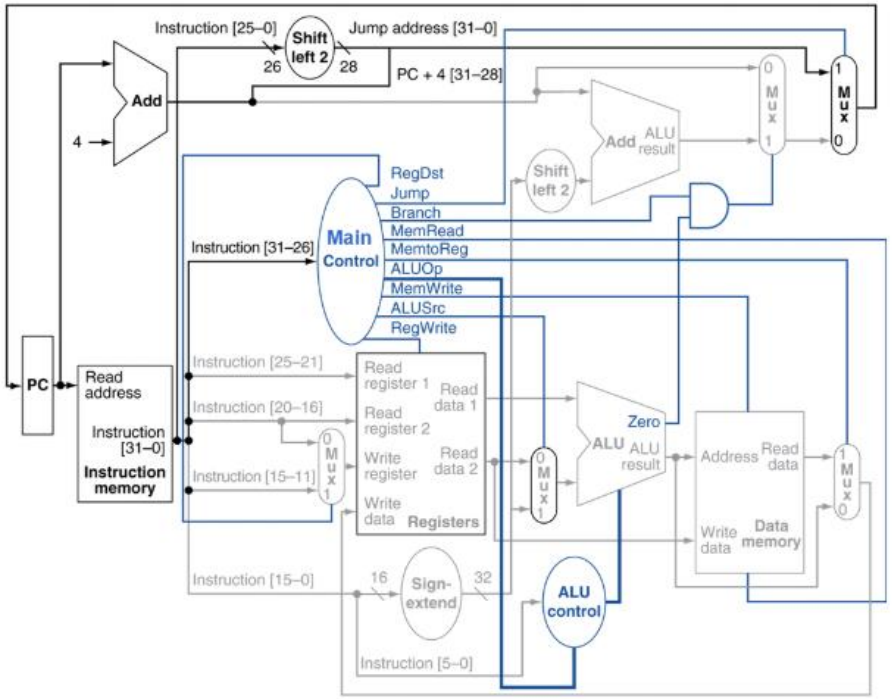
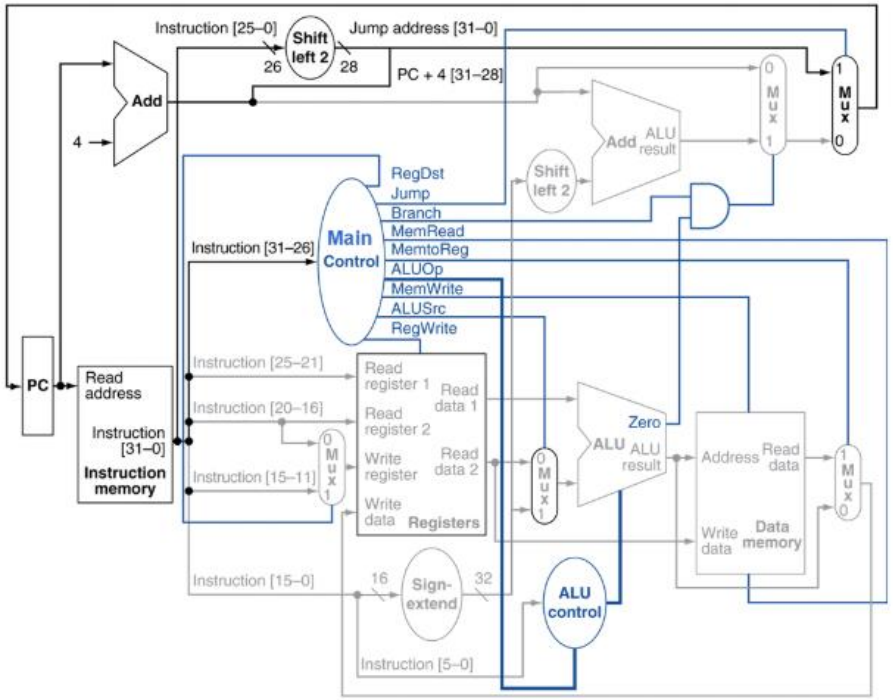
CPU structure

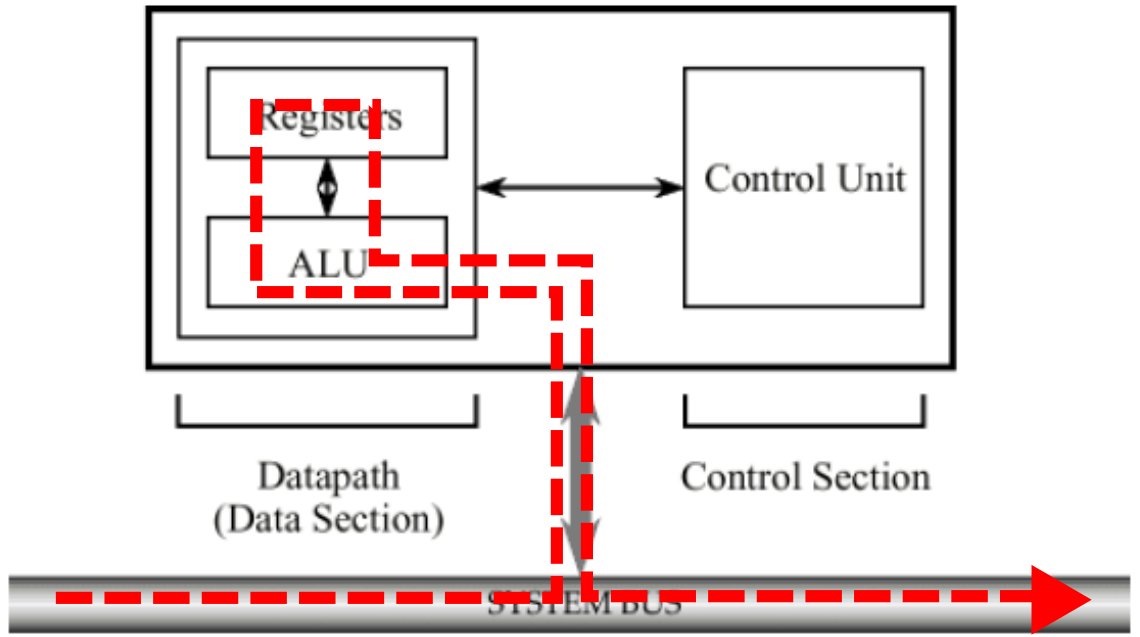




- CPU consists of several components
  - Datapath
    - ALU, Register file, etc..
  - Control Unit

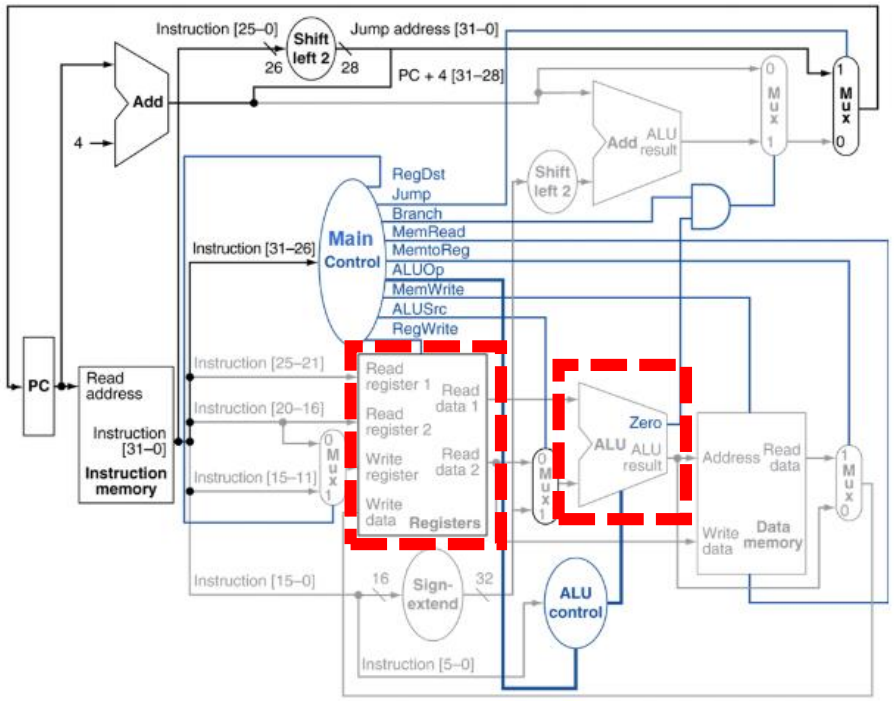
Datapath





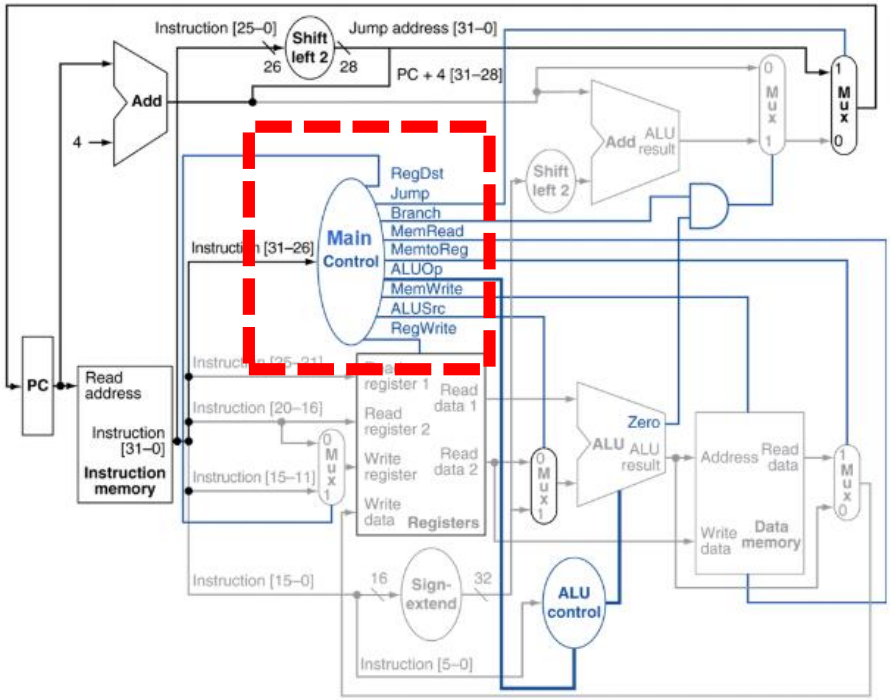
- Datapath:
  - Units in the path of data
    - SYSTEM BUS(deliver the memory data) → ALU → Register → ALU → SYSTEM BUS
  - ALU, Register file

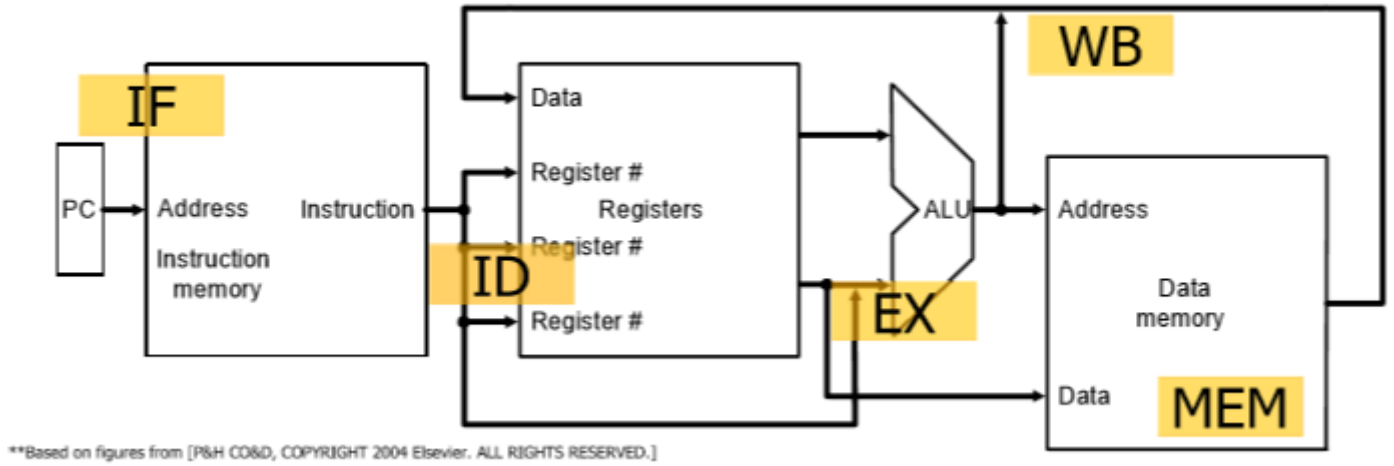
Datapath



- Datapath
  - Contains register file, ALU and the other data-wires

Control Unit





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- Control Unit:
  - Decodes instruction
  - Then, generates control signals that control the components in the datapath

Modularization

- Modularize the main CPU structure (**strongly** recommended)
  - Datapath
    - ALU
    - Register file
  - Control Unit

- Etc.
    - MUX, sign-extender, adder

Magic Memory

- In testbench code (line 38~58)
  - It gives you memory data with a slight delay (less than a clock cycle)

- It is NOT a realistic model of the main memory
  - Memory is much slower than CPU
  - However, we assume there is a magic memory which is faster than CPU!

```
always begin
    loadedData = `WORD_SIZE'bz;
    #`PERIOD1;
    forever begin
        wait (readM == 1 || writeM == 1);
        if (readM == 1) begin
            #`READ_DELAY;
            loadedData = memory[address];
            inputReady = 1;
            #(`STABLE_TIME);
            inputReady = 0;
            loadedData = `WORD_SIZE'bz;
        end else if (writeM == 1) begin
            memory[address] = data;
            #`WRITE_DELAY;
            ackOutput = 1;
            #(`STABLE_TIME);
            ackOutput = 0;
        end
    end  // of forever loop
end  // of always block for memory read
```

TSC CPU

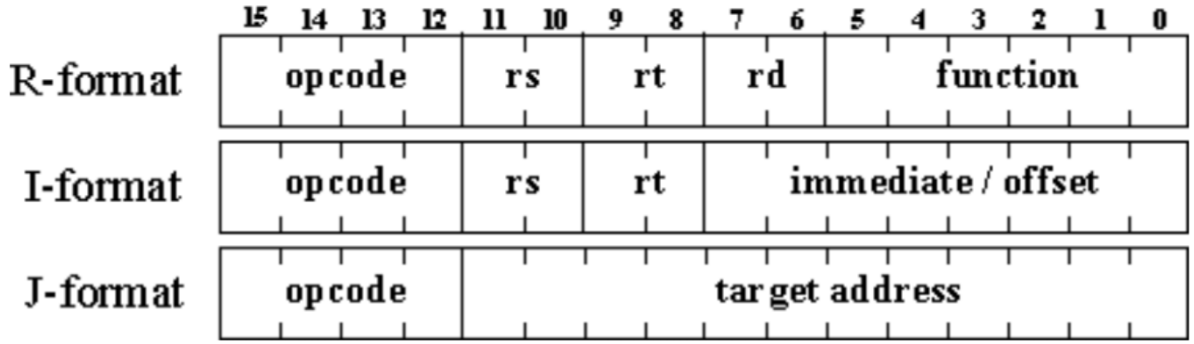
- RISC-V CPU vs TSC CPU

Name (Field Size)	Field 7 bits	5 bits	5 bits	3 bits	5 bits	7 bits	Comments
R-type	funct7	rs2	rs1	funct3	rd	opcode	Arithmetic instruction format
I-type	immediate[11:0]		rs1	funct3	rd	opcode	Loads & immediate arithmetic
S-type	immed[11:5]	rs2	rs1	funct3	immed[4:0]	opcode	Stores
B-type*	immed[12,10:5]	rs2	rs1	funct3	immed[4:1,11]	opcode	Conditional branch format
J-type*	immediate[20,10:1,11,19:12]				rd	opcode	Unconditional jump format
U-type	immediate[31:12]				rd	opcode	Upper immediate format

Remove

*in the textbook and old versions of the RISC-V manual, referred to as SB-type and UJ-type

[From P&H CO&D RISC-V ed.]



- Has shorter instructions, smaller registers, and fewer instruction types!
  - A simple ISA
- More details in TSC_manual.pdf

Assignment

- Implement a single-cycle TSC CPU
  - Single-cycle CPU
    - Datapath
      - ALU
      - Register file (with 4 registers)
    - Control unit
      - Generate the control signals used in the datapath
  - Your implementation of the CPU should process one instruction in each clock cycle
  - Due date : ~4/20 (2-week assignment)
  - Instructions
    - Read the given TSC_manual.pdf, opcode.v

Tips

- CPU module port

output	readM	"read" signal to memory
output	writeM	"write" signal to memory
output	[`WORD_SIZE-1:0] address	target memory address
inout	[`WORD_SIZE-1:0] data	data for reading or writing (can be used as both **input and output**)
input	ackOutput	signal from memory ("data is written")
input	inputReady	signal from memory ("data is ready for reading")
input	reset_n	reset your CPU (registers, PC, etc..)
input	clk	clock signal

About inout port

- Can be used as both input and output port
- Set wire value ‘z’ (high impedance) if you are using it as input
  - You could get the input value only if it’s ‘z’ value

```
assign data= readOrWrite? writeData : 16'bz;
```

- Google for more details!

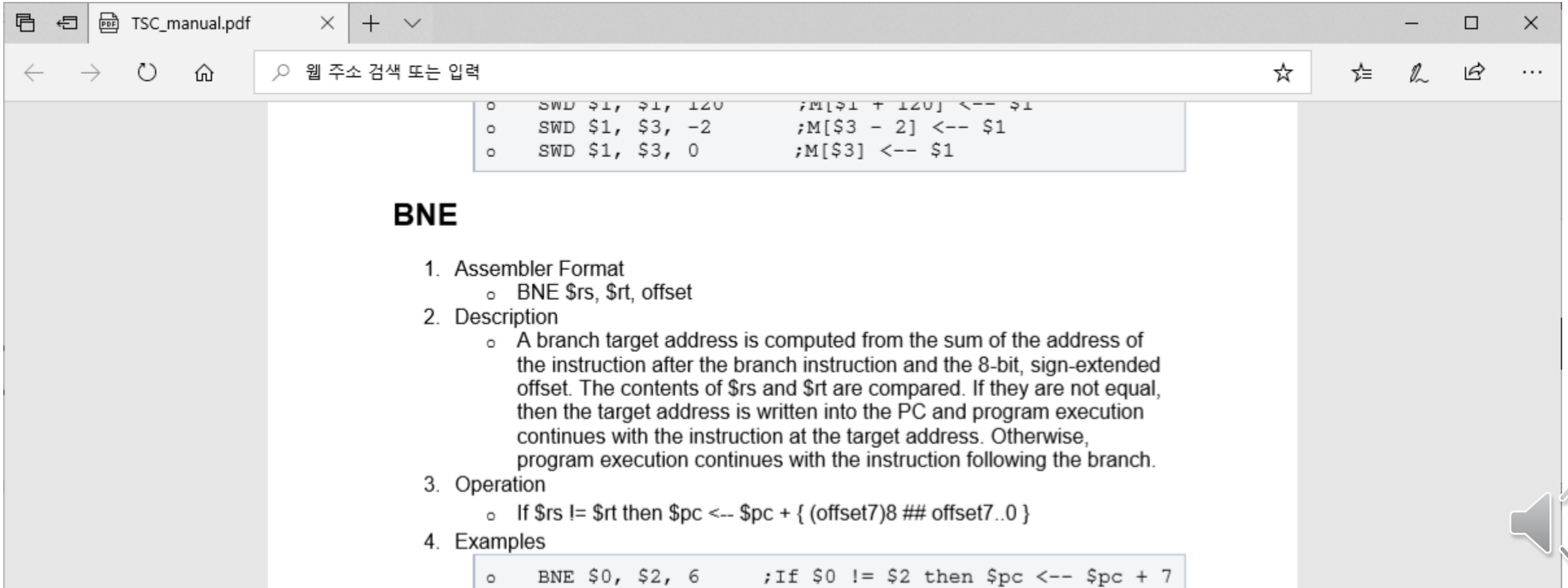
Negedge clk

- You might need 2 events in one clock cycle
  - For example, CPU fetches instruction and need one more memory data f etch for load store instruction

- You can use both @(posedge clk) and @(negedge clk)

Tips

- TSC_manual.pdf



Thanks

Exemplary Single-cycle CPU Dataflow