Lecture 6

Time-Dependent Behaviour of Digital Circuits with Feedback

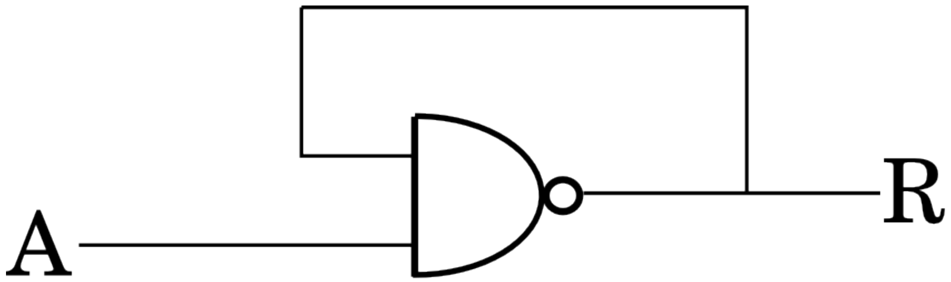
In this lecture we will:

Examine the behaviour of a digital circuit in which connections between gate outputs and inputs create a loop which we call feedback.

Remember, it is perfectly legal to connect any gate output to any gate input as long as outputs are not connected together.

.... knowing this, student "V. Mischievous" presented me (on paper) the following circuit:

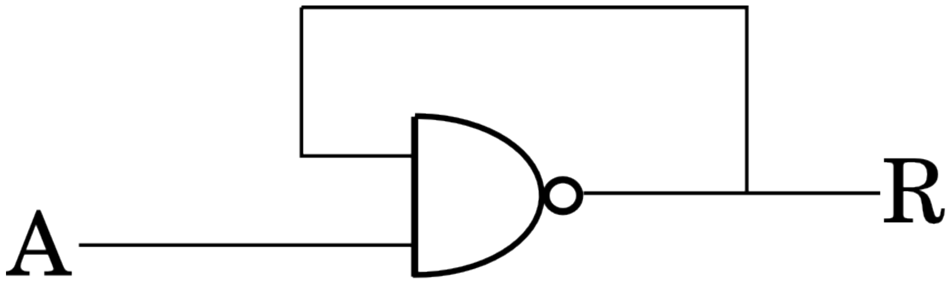
A Curious Circuit



What is the output of this circuit?

If input A is logic 0, R is logic 1, [0, 1] input to a NAND gate produces logic 1 and R is logic 1 .. ok..

A Curious Circuit



Given that A=1 Boolean algebra tells us:

$$R = (R.A)' = (R.1)' = R'$$

Impossible!   Now what????

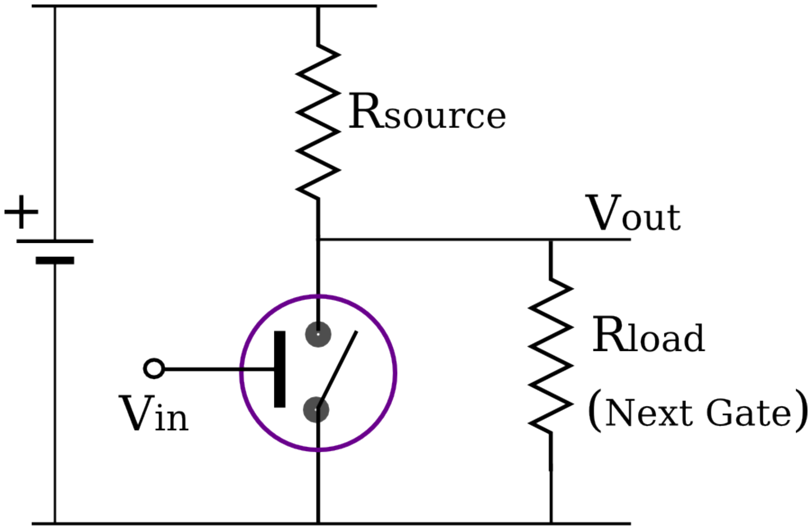
Engineering Approach

When a model (like the Boolean algebra model of a digital gate) breaks down, and its behaviour is unpredictable, we must go down one "physical description" level and examine how the actual physical device was constructed.

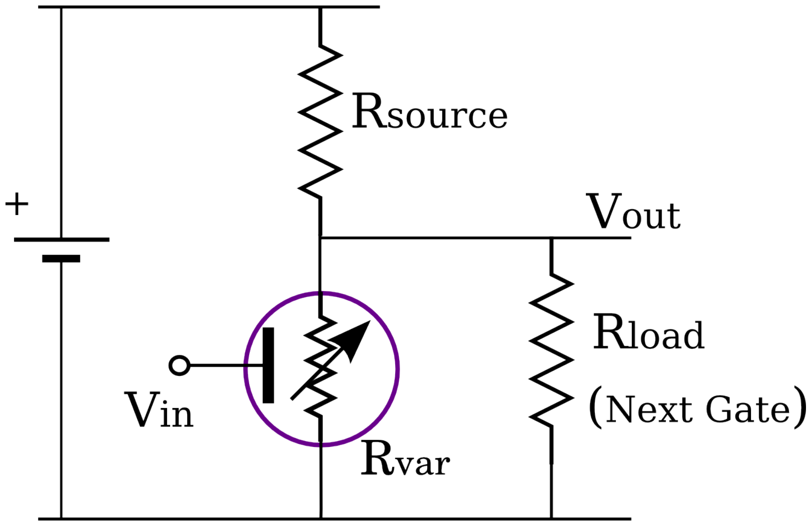
This may help us to predict what will happen.

So what were those models from the last lecture?

Quasi-Physical Models



Switch and Delay

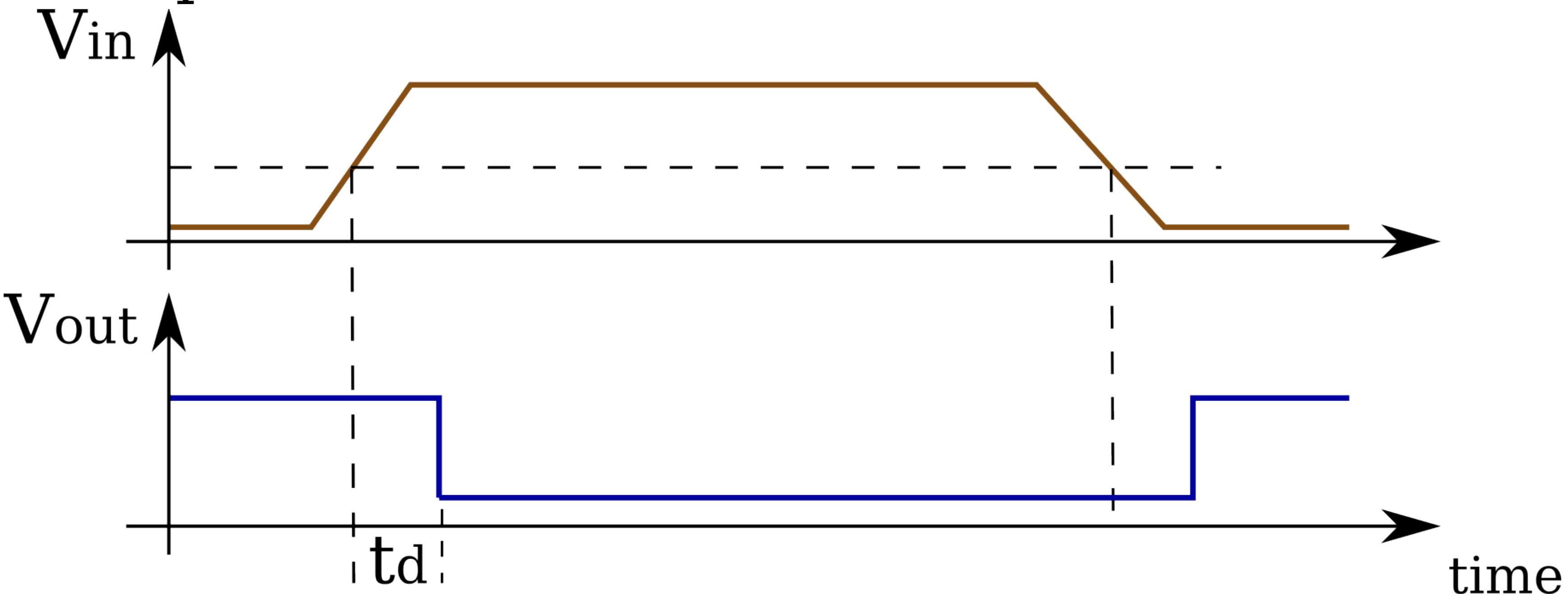


Variable Resistance

These are needed only to construct a logical model which can be used to analyse unusual behaviour in the laboratory.

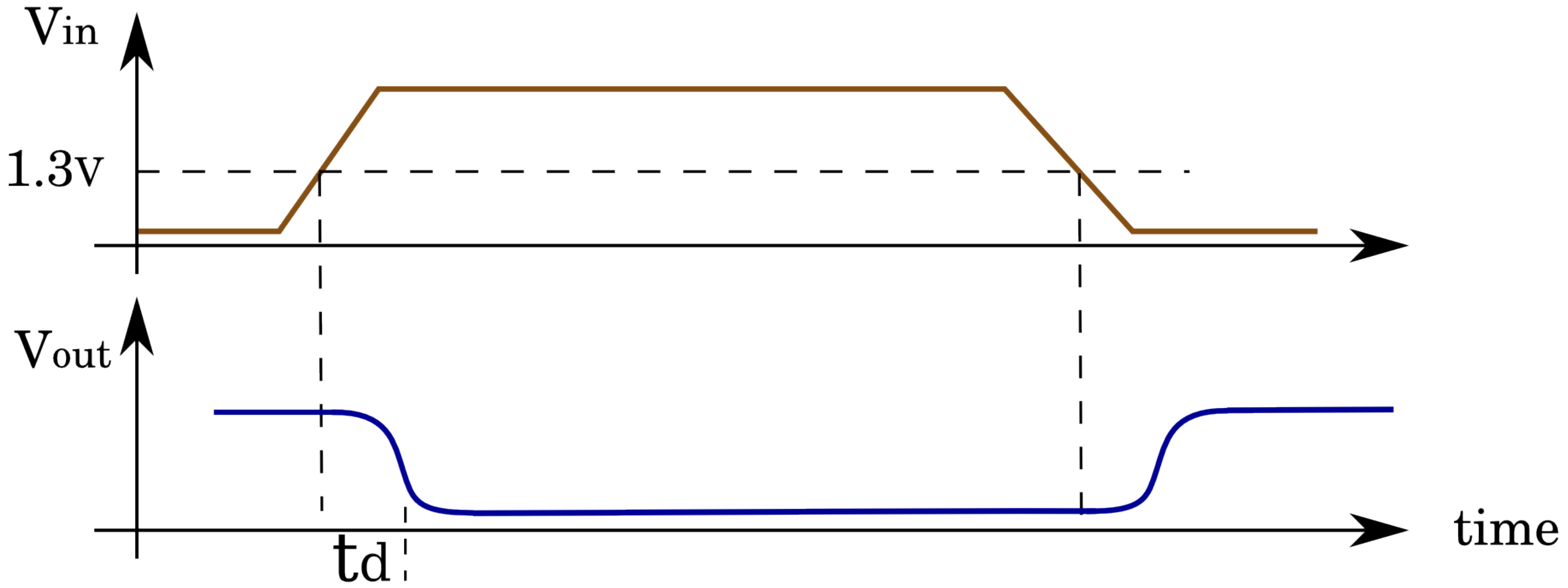
The Switch and Delay Model

This model only really differs from Boolean algebra by the inclusion of a time delay between input (left hand side) and output (right hand side). Its time behaviour is described by the following example:



The variable resistance model

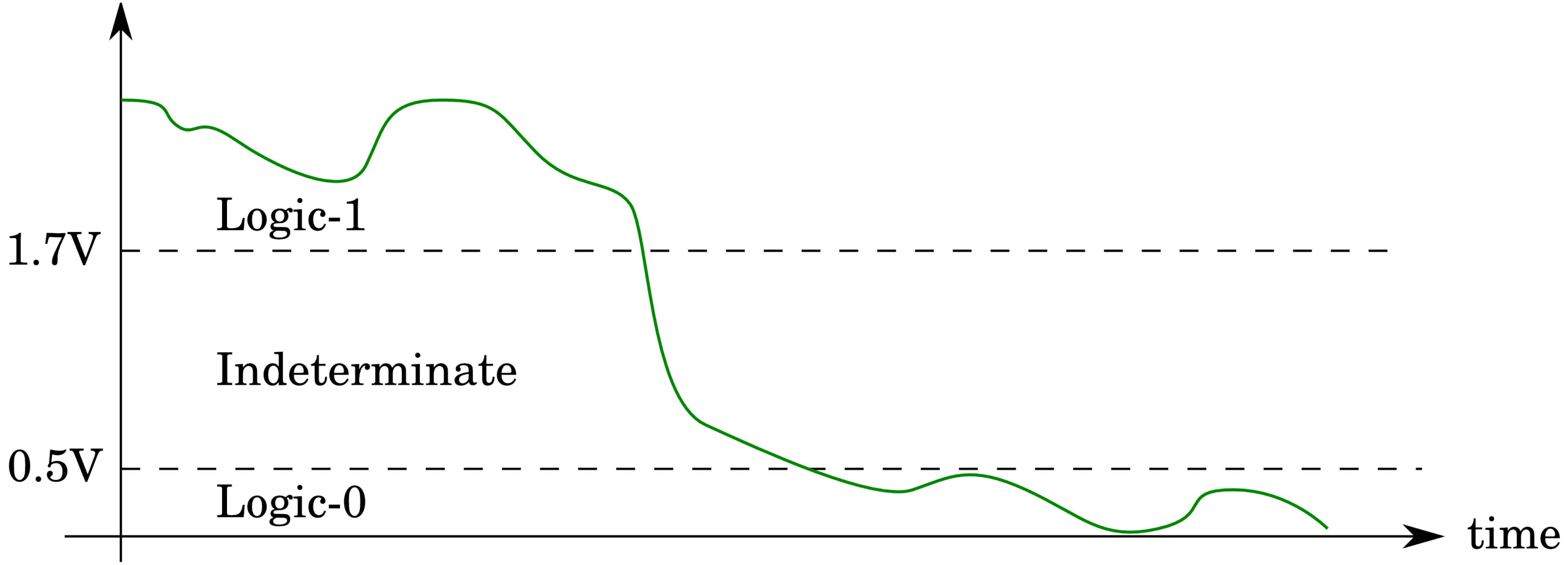
This gives us a more accurate representation of the real behaviour



We no longer have a valid Boolean signal output when changing from 0 to 1 and back.

Analogue Model

The variable resistance model is not digital but analogue. The variable resistor can be adjusted continuously. To interpret its behaviour as a digital circuit we need to introduce the concept of a noise margin.



Noise Margin

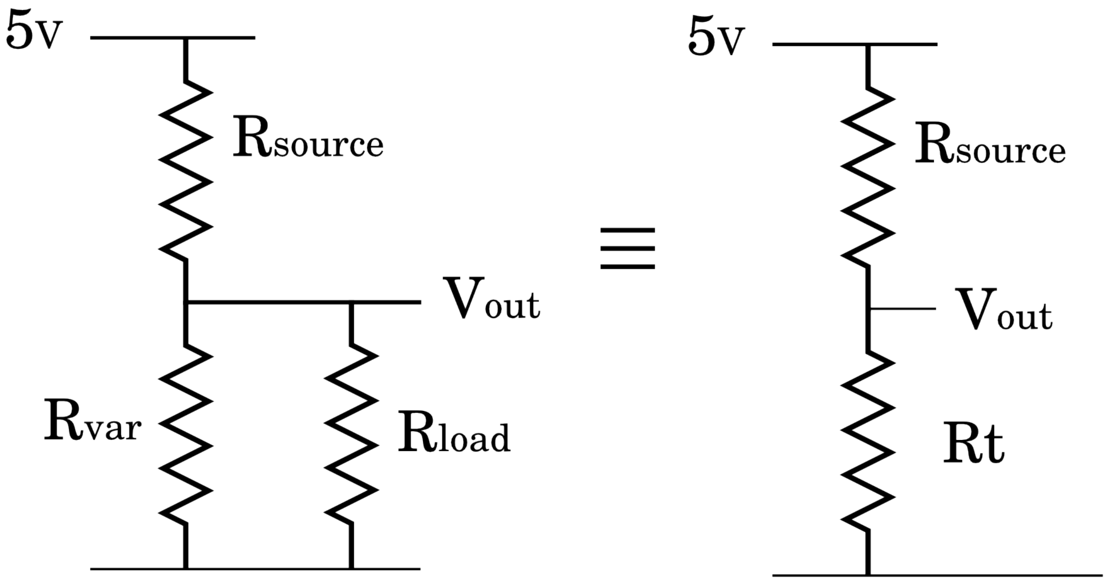
The noise margin gives us a definite threshold (1.7volts) above which we know that our signal represents a Boolean 1, and similarly a a definite threshold (0.5Volts) below which we know our signal represents Boolean 0.

We aim to design our circuits so that they operate well away from the threshold, so normally we aim to make Boolean 1 around 3.5 Volts, and Boolean 0 around 0.3 Volts

Potential Dividers

For any input voltage, the variable resistance model acts like a potential divider. So:

$$V_{out} = \frac{5R_t}{R_{source} + R_t}$$



Rt is made up of the transistor resistance (Rvar) and the input resistance of the next gate (Rload)

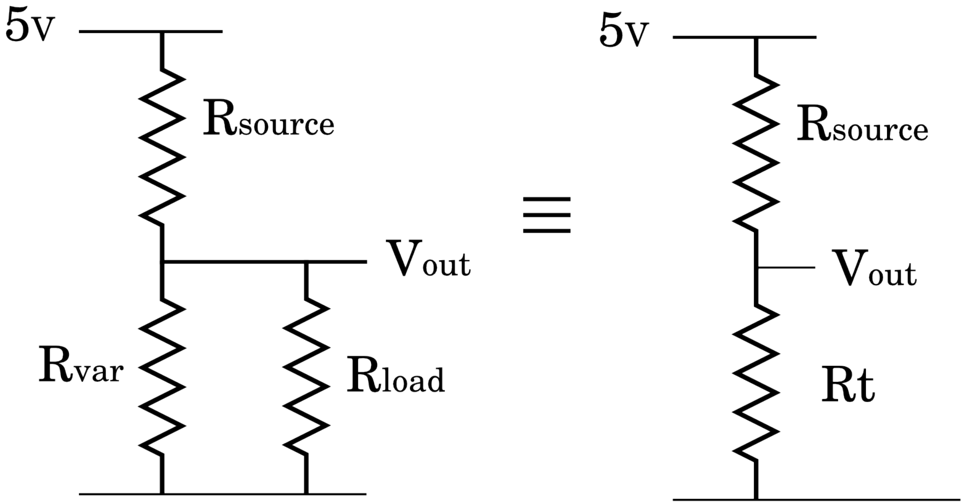
$$\frac{1}{R_t} = \frac{1}{R_{var}} + \frac{1}{R_{load}}$$

Putting in some real resistances

For typical resistances the circuit seems to work well with good noise margins.

	$R_{source}(\Omega)$	$R_{load}(\Omega)$	$R_{var}(\Omega)$	$R_t(\Omega)$	V_{out} (Volts)
Logic-1	1000	10000	3000	2308	3.5
Logic-0	1000	10000	60	59	0.28

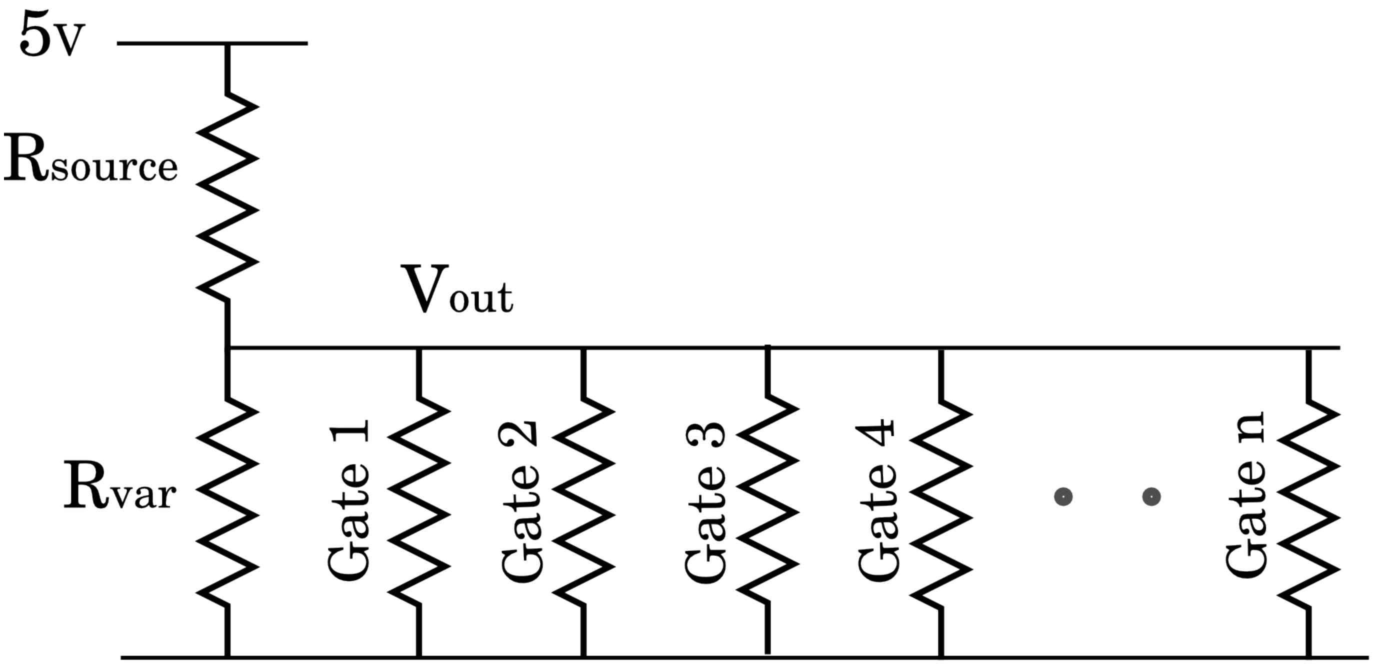
$$\frac{1}{R_t} = \frac{1}{R_{var}} + \frac{1}{R_{load}}$$



Fan-Out

The fan-out of a gate is the number of different gate inputs to which it is connected.

If a transistor is connected to n gates, the circuit becomes:

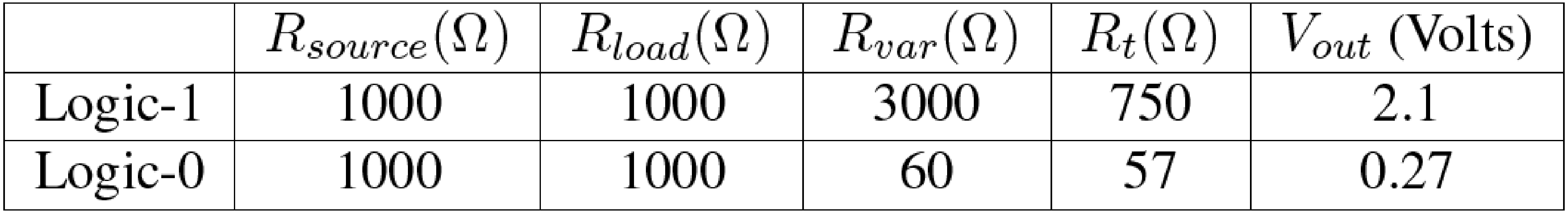


Fan-Out

Resistors in parallel combine according to the inverse law:

1/R = 1/R1 + 1/R2 + 1/R3 + . . .

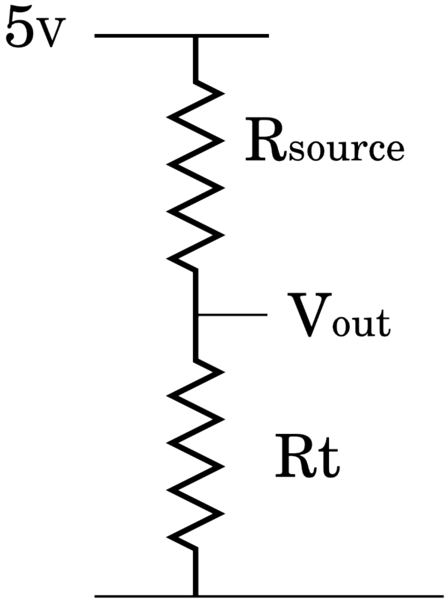
So if a gate output is connected to 10 gate inputs the load resistance becomes 1/10 of a single gate. The operating voltages become:



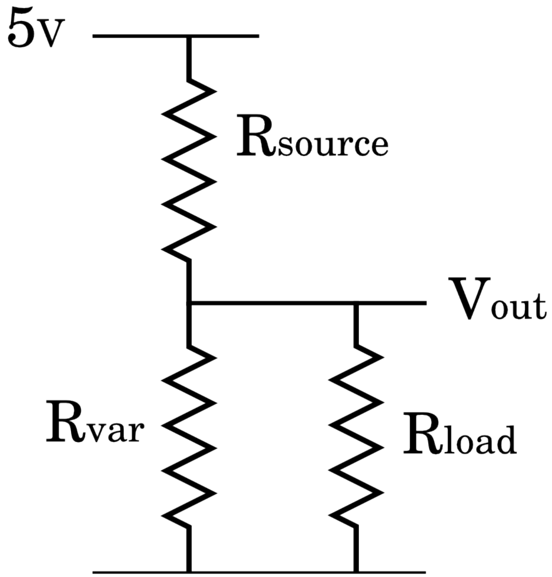
	$R_{source}(\Omega)$	$R_{load}(\Omega)$	$R_{var}(\Omega)$	$R_t(\Omega)$	V_{out} (Volts)
Logic-1	1000	1000	3000	750	2.1
Logic-0	1000	1000	60	57	0.27

Problem Time!

Given that R_{source}=1000 Ohms, estimate the value of Rt when the circuit will fail, ie when the output voltage corresponding to Boolean 1 will be below 1.7.



Given R_{var} is 3000 Ohms for logic 1 and R_{load} for a single gate (fan-out=1) is 10000 Ohms, estimate the fan-out that will cause a failure.



Solution

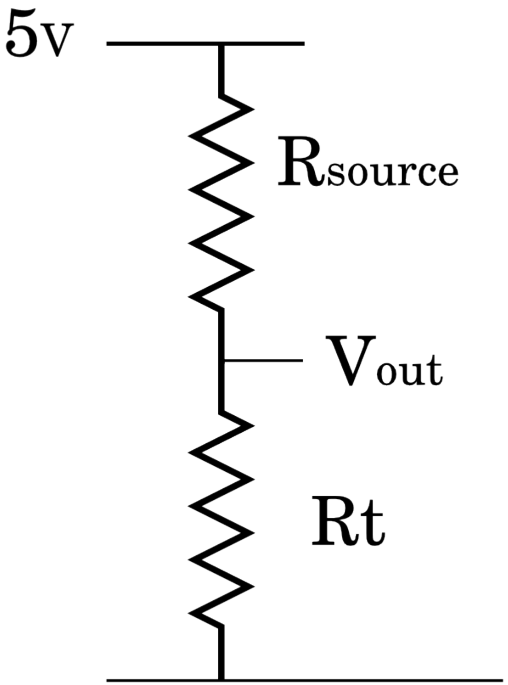
The output voltage is calculated by a potential divider.

$V_{out} = 5Rt/(R_{source}+Rt) = 1.7$

$(5-1.7)Rt = 1.7R_{source}$

$Rt = (1.7/3.3)\ R_{source} \sim R_{source}/2$

Rt is approximately 500 Ohms



Solution 2

$1/R_{load} + 1/R_{var} = 1/Rt$

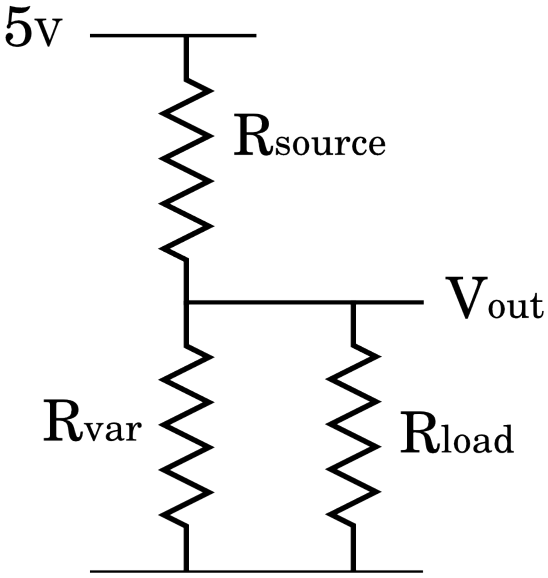
Rt=500 Ohms causes failure

$1/R_{load} + 1/3000 = 1/500$

$R_{load} = 600$

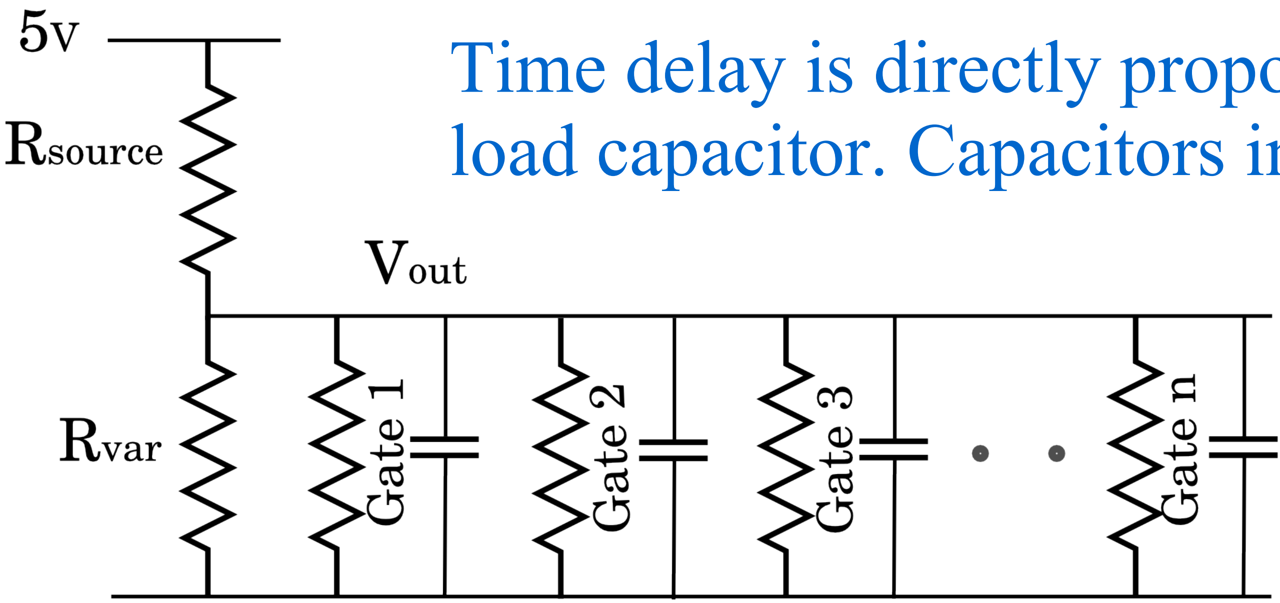
For a fan out of n, $R_{load} = 10000/n$

Do n = 10000/600 ~ 17



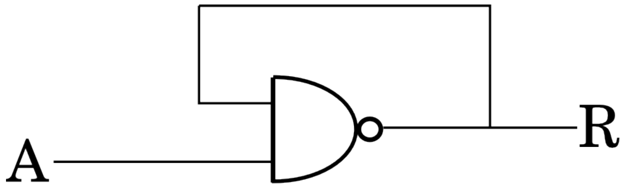
Fan-Out

Another undesirable property of large fan-outs is that the time delay increases. This is because the load capacitor increases.



Time delay is directly proportional to the load capacitor. Capacitors in parallel add.

Returning to the curious circuit:



Analysis using Switch-and-Delay Model

Let A=1, and assume that R=1 initially

The gate senses inputs 11 and waits a bit (delay!)

The output stage switches to the correct output: R=0

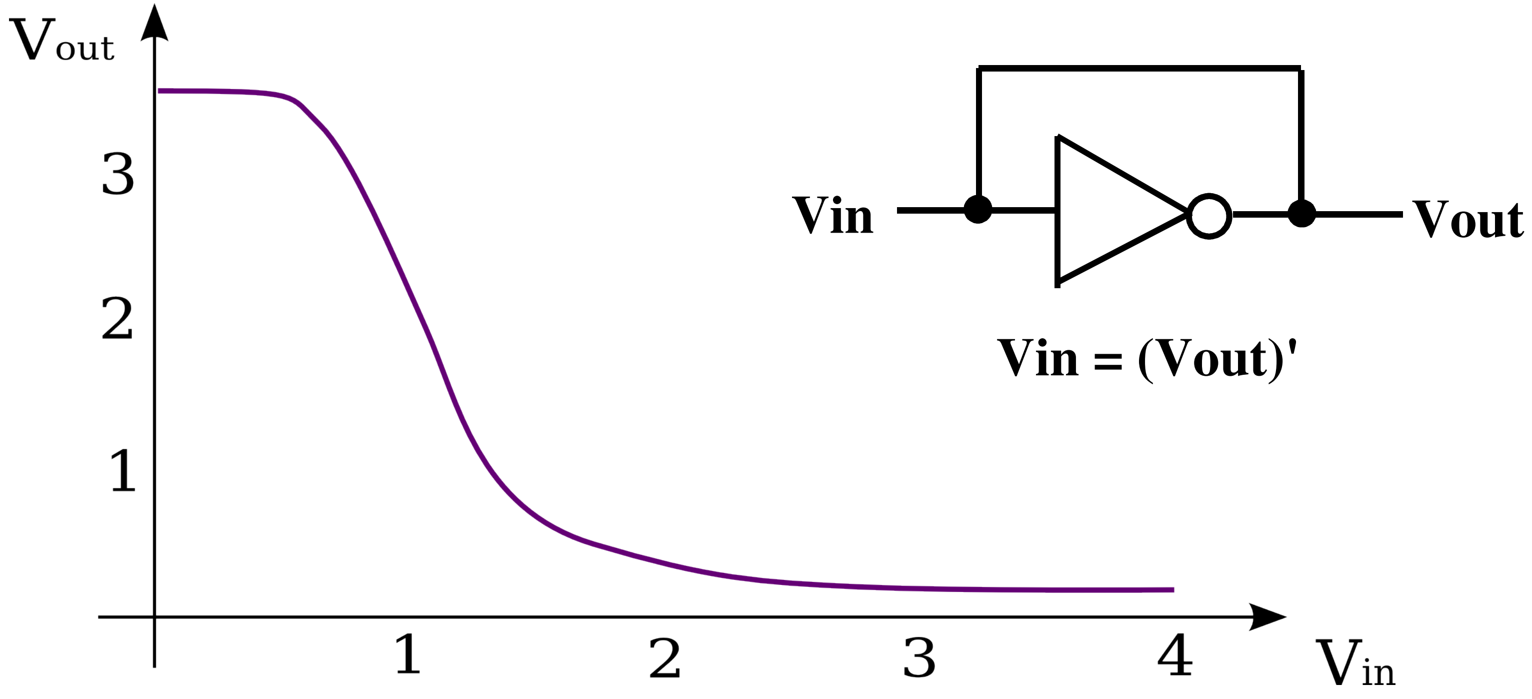
The gate senses inputs 01 and waits a bit (delay!)

The output stage switches to the correct output: R=1

… and so on … We have oscillation !

Analysis using the Variable Resistor Model

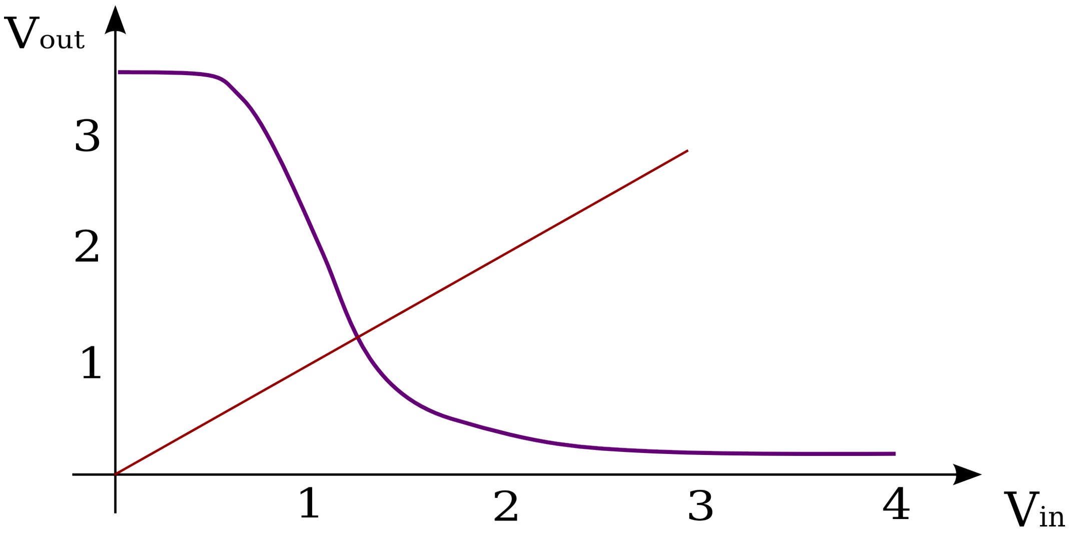
We assume that the input of our circuit A=1; therefore, the NAND gate is equivalent to an inverter:



Vin = (Vout)'

Analysis using the Variable Resistor Model

We CAN solve this impossible looking problem graphically, since Vin=Vout represents a straight line through the origin.



What this model says is that the output of this circuit will settle at an invalid digital value around 1.2 volts.

So, what will happen in the lab?

The most likely result is that a bad digital output value would result.

However, we do not not know for certain unless a very very very high frequency oscilloscope is connected to the output of the circuit.

Any oscillation will be very fast and difficult to detect.

Feedback Circuits

The curious circuit we have been studying seems pretty useless!

However we have at least learned how to begin to analyse circuits with feedback.

For the moment we will ignore all the problems caused by fan-out, and use the simpler switch and delay model for our analysis.

Analysis of Digital Circuits with Feedback

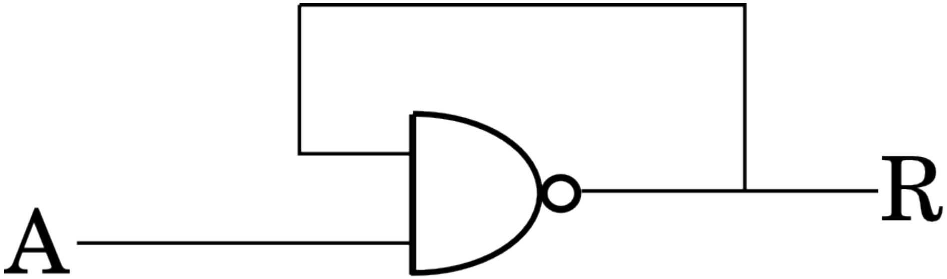
1. Assign names to the independent inputs of the circuit and to all its gate outputs.

2. Create a table with two columns of numbers. The first column is labelled NOW and has all the possible combinations of 1s and 0s for the independent inputs and gate outputs.

3. Calculate the values the gate outputs will become after the gate delays; this will be the NEXT column of values.

4. Find stable, bistable, and unstable states.

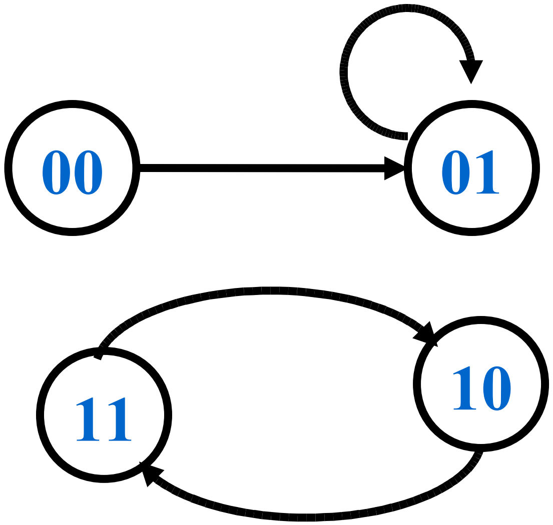
Analysis of our Curious Circuit



Transition Table

A R (now)	A R (next)
0 0	0 1
0 1	0 1
1 0	1 1
1 1	1 0

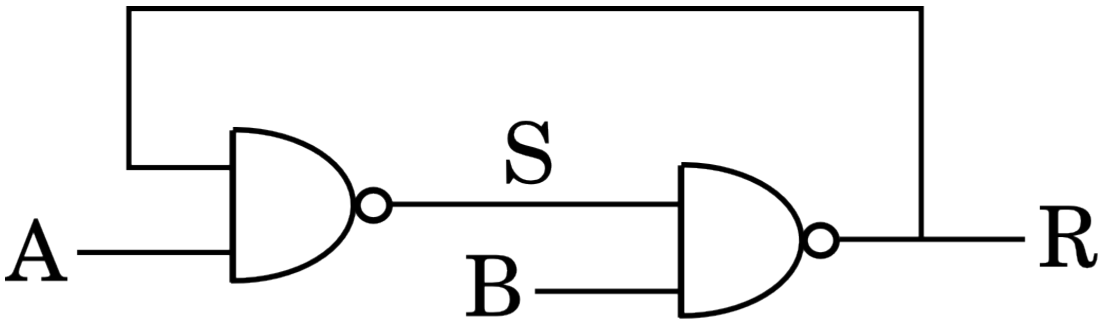
Transition Diagram



Stable

Bistable

Analysis of a More Useful Circuit

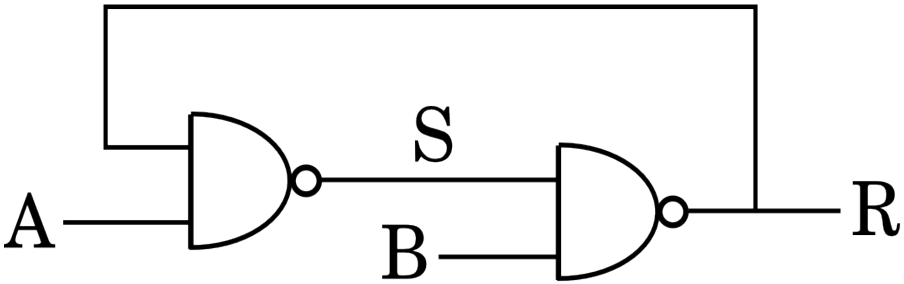


The Boolean Equations for this circuit are:

S = (A•R)’ R = (S•B)’

We have four variables so there will be sixteen states.

Transition Table of a More Useful Circuit

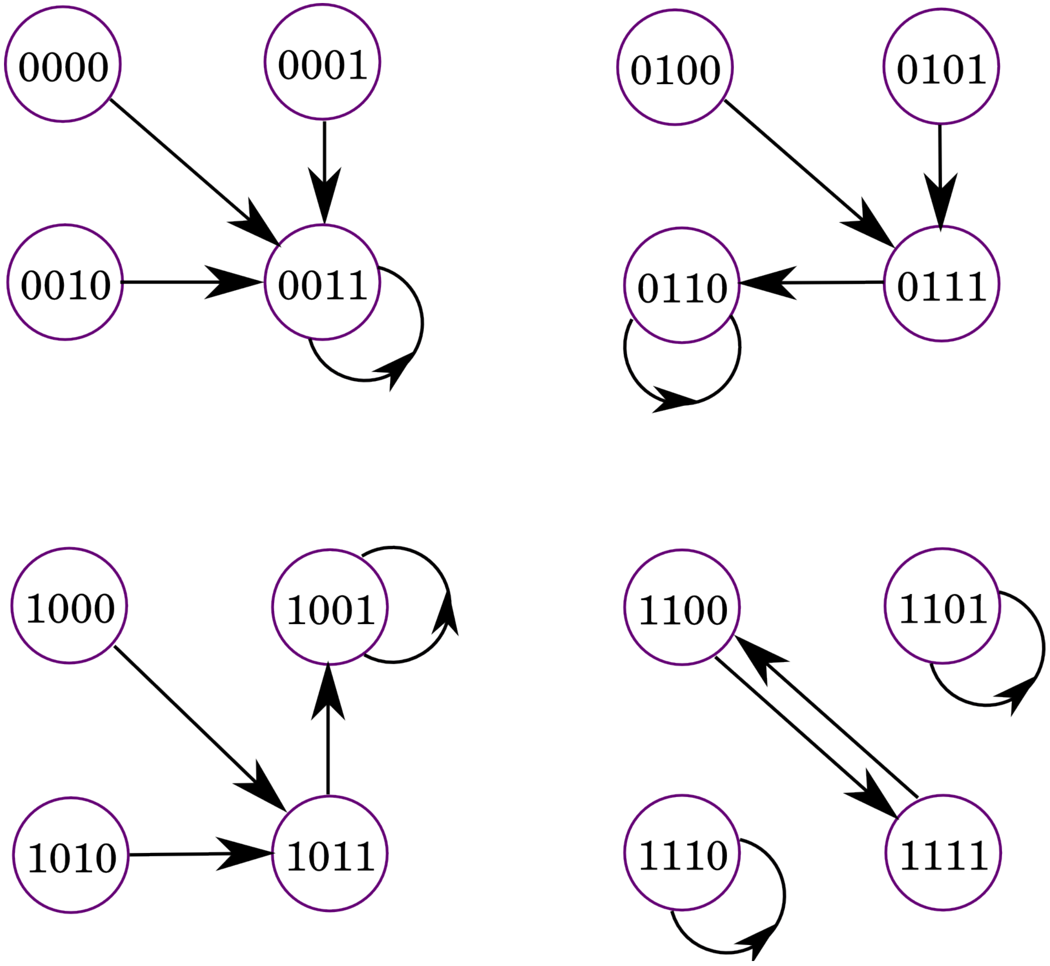


A	B	S	R	A	B	S	R	
(now)				(next)				
0	0	0	0	0	0	1	1	
0	0	0	1	0	0	1	1	
0	0	1	0	0	0	1	1	
0	0	1	1	0	0	1	1	Stable
0	1	0	0	0	1	1	1	
0	1	0	1	0	1	1	1	
0	1	1	0	0	1	1	0	Stable
0	1	1	1	0	1	1	0	
1	0	0	0	1	0	1	1	
1	0	0	1	1	0	0	1	Stable
1	0	1	0	1	0	1	1	
1	0	1	1	1	0	0	1	
1	1	0	0	1	1	1	1	
1	1	0	1	1	1	0	1	
1	1	1	0	1	1	1	0	Stable
1	1	1	1	1	1	0	0	

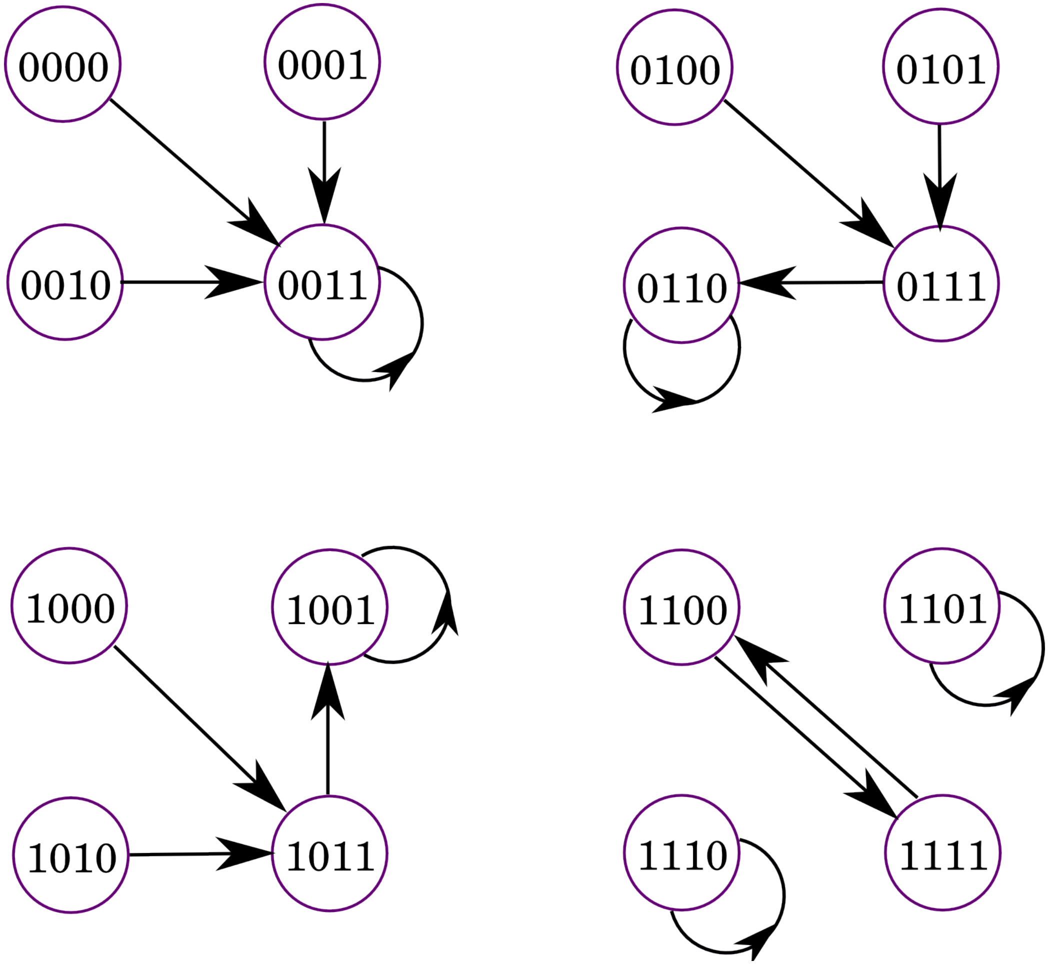
The Transition Diagram

From the Transition Table we can construct the Transition Diagram

A	B	S	R	A	B	S	R
(now)				(next)			
0	0	0	0	0	0	1	1
0	0	0	1	0	0	1	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	0	1
1	1	0	0	1	1	1	1
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	0	0



Conclusions



From the diagram we see the following:

Input 00 -> Output 11

Input 01 -> Output 10

Input 10 -> Output 01

Input 11: Hold or oscillate

Next time we will use this to make a memory