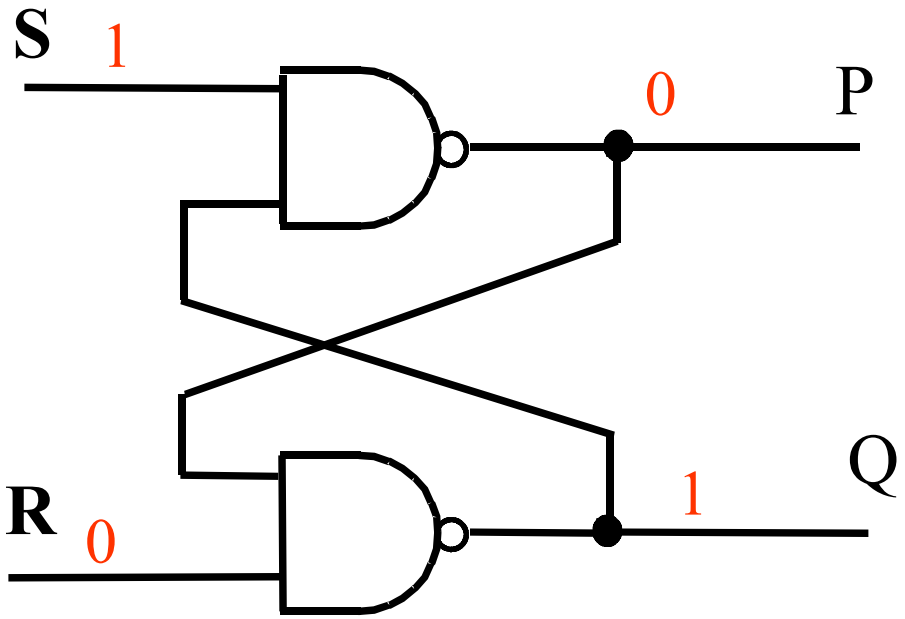
Lecture 7:

Flip-Flops

The R-S flip flop

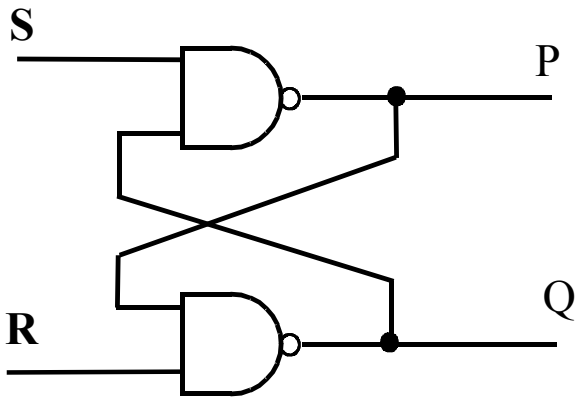
We analysed this circuit in the last lecture.



S	R	P	Q
0	0	1	1
0	1	1	0
1	0	0	1
1	1	?	?

Non determinism

For input 1,1 we can only compute the output if we know what is was at the previous time interval



S	R	Pp	Qp	P	Q	
1	1	0	0	1	1	Unstable
1	1	0	1	0	1	Stable
1	1	1	0	1	0	Stable
1	1	1	1	0	0	Unstable

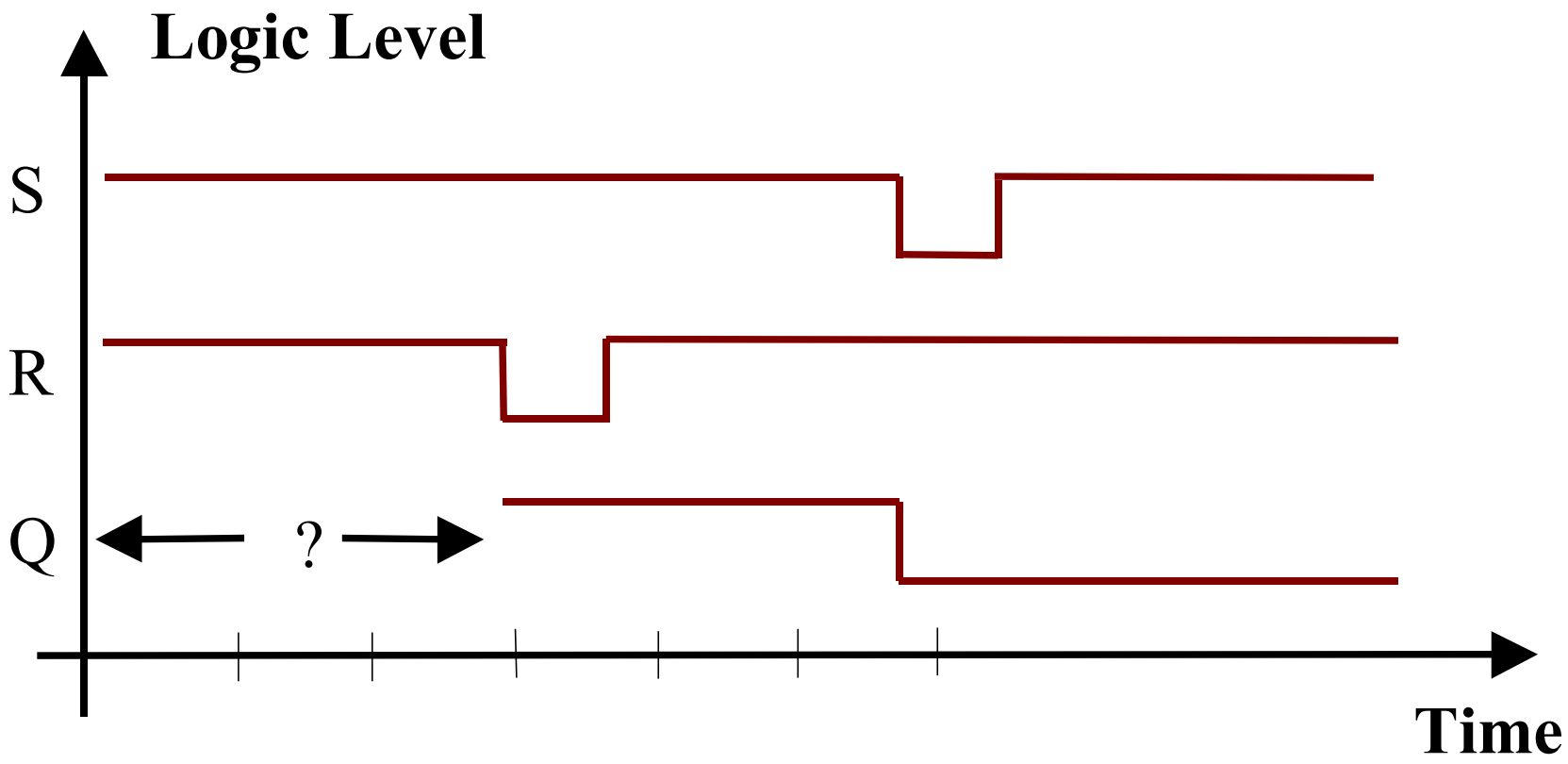
The nature of the non-determinism

Theoretically the circuit could flip between the two unstable states, oscillating indefinitely.

In practice the two gates will not have identical time delays, so one will change before the other and the circuit will fall into a stable state.

We do not know what that stable state is.

Non determinism when the circuit is switched on



The flip flop and memory

The R-S flip flop can be looked upon as a very simple memory.

It has two states which can be thought of as Q=1 and Q=0, or to put it another way it is a one bit memory.

The inputs are labeled S for set and R for reset.

Sequential Circuits

Notice that we can only describe the behaviour of the R-S if we know the time sequence of the inputs. For this reason it is referred to as a sequential circuit.

In all practical cases we shall avoid using S=R=0, and thus it will always be the case that P=Q’

The input S=R=1 ensures that the output cannot change

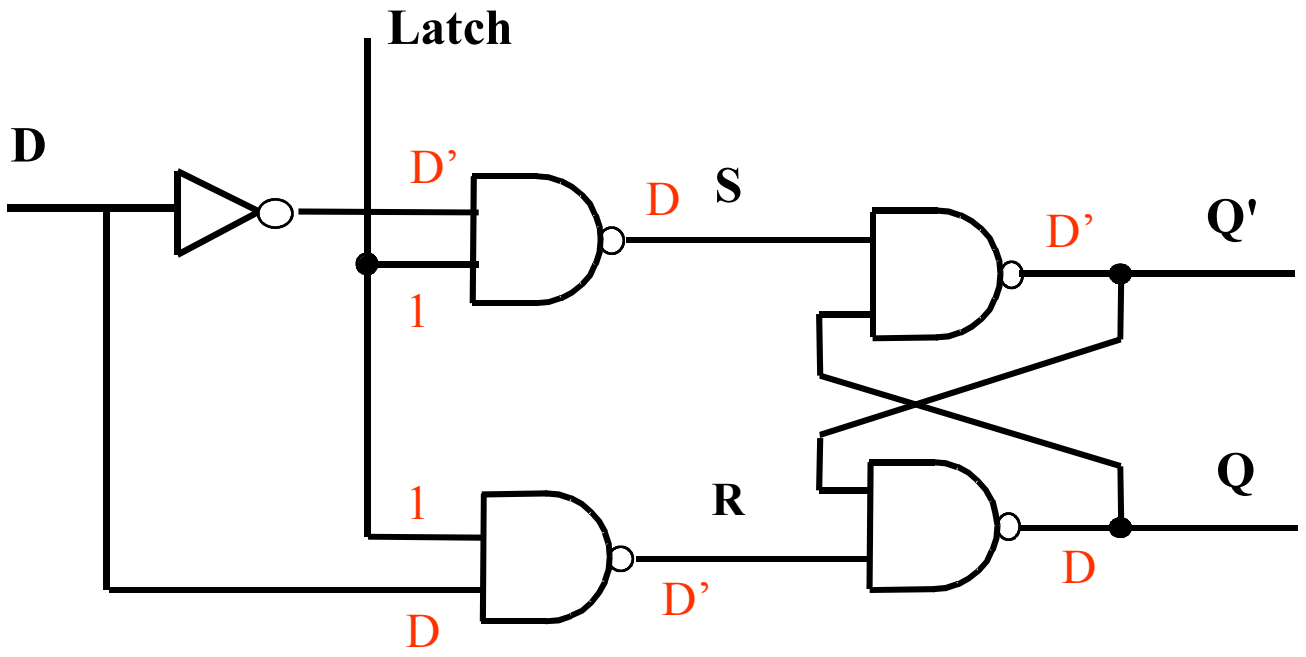
The D-Type latch

The set-reset mechanism of the R-S flip flop is not very convenient.

It would be much better if a memory circuit could be set to one or zero depending on its input.

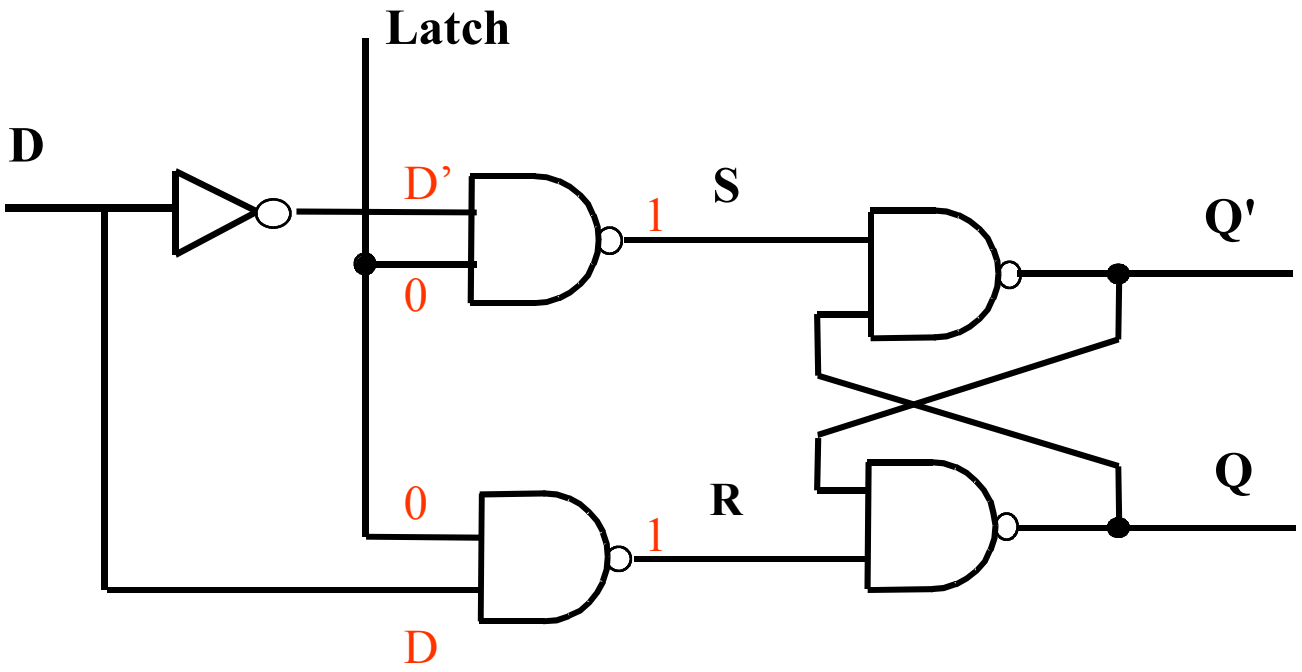
This is the purpose of the D-type latch.

The D type latch, open



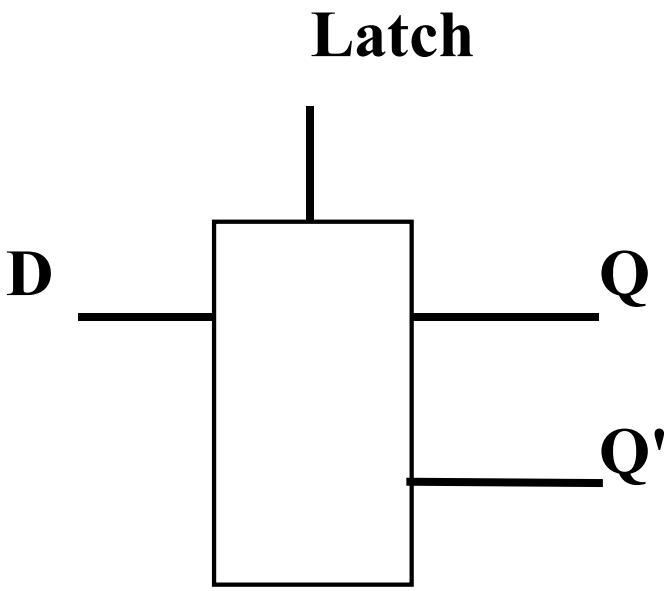
If the latch is 1 then S=D=Q and R=D'=(Q')

The D type latch, closed



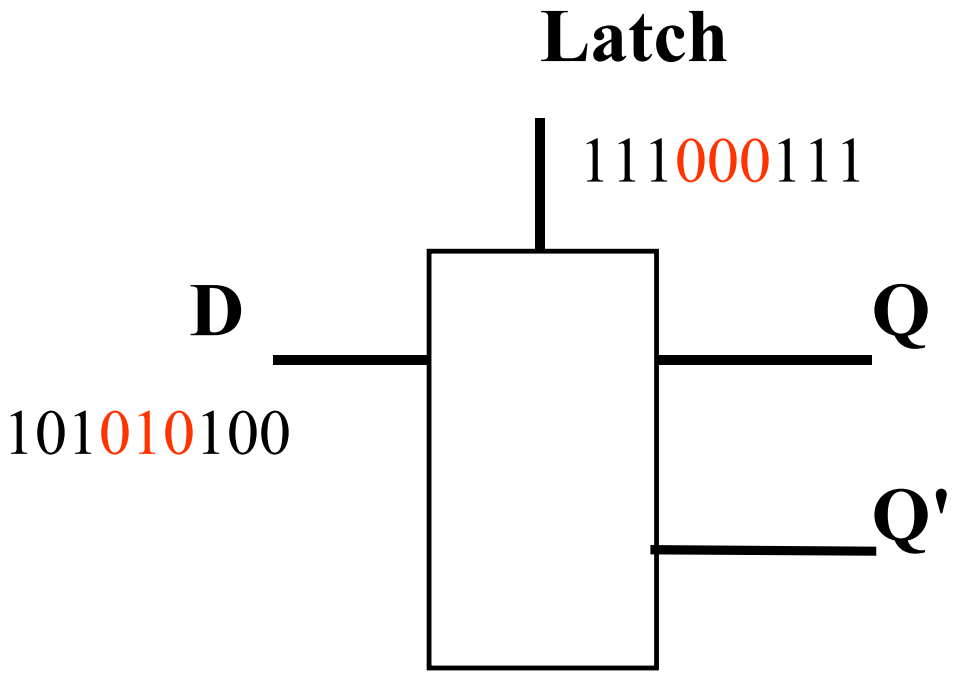
If the latch is 0, then S=R=1 Q and Q' cannot change

Symbol for a D-Type latch



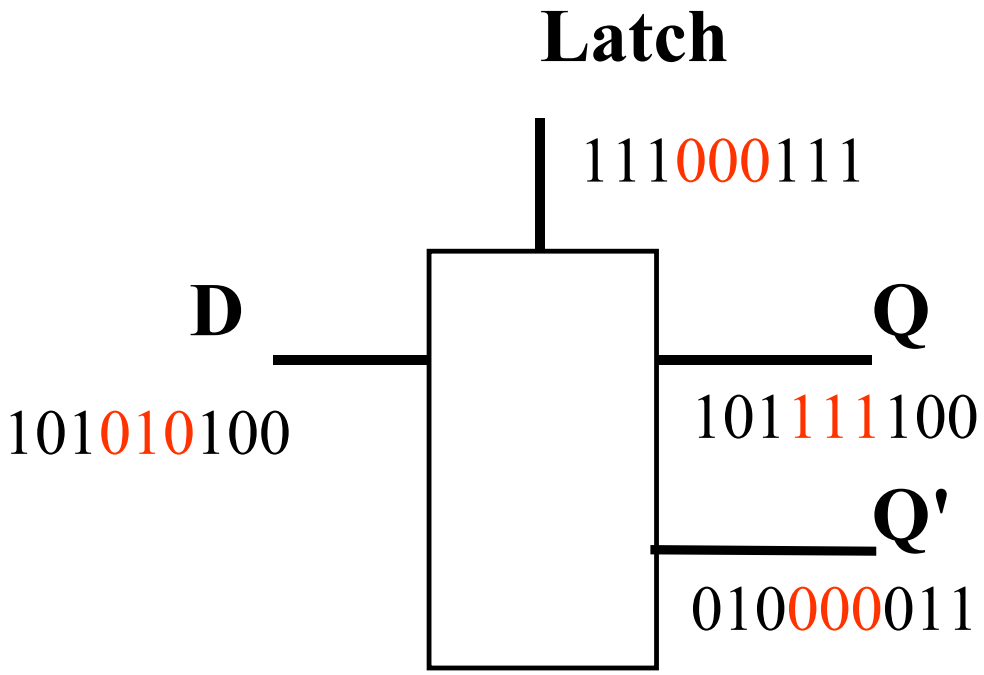
Problem Break

For the given values of D and L calculate the values of Q and Q’



Problem Break

For the given values of D and L calculate the values of Q and Q’

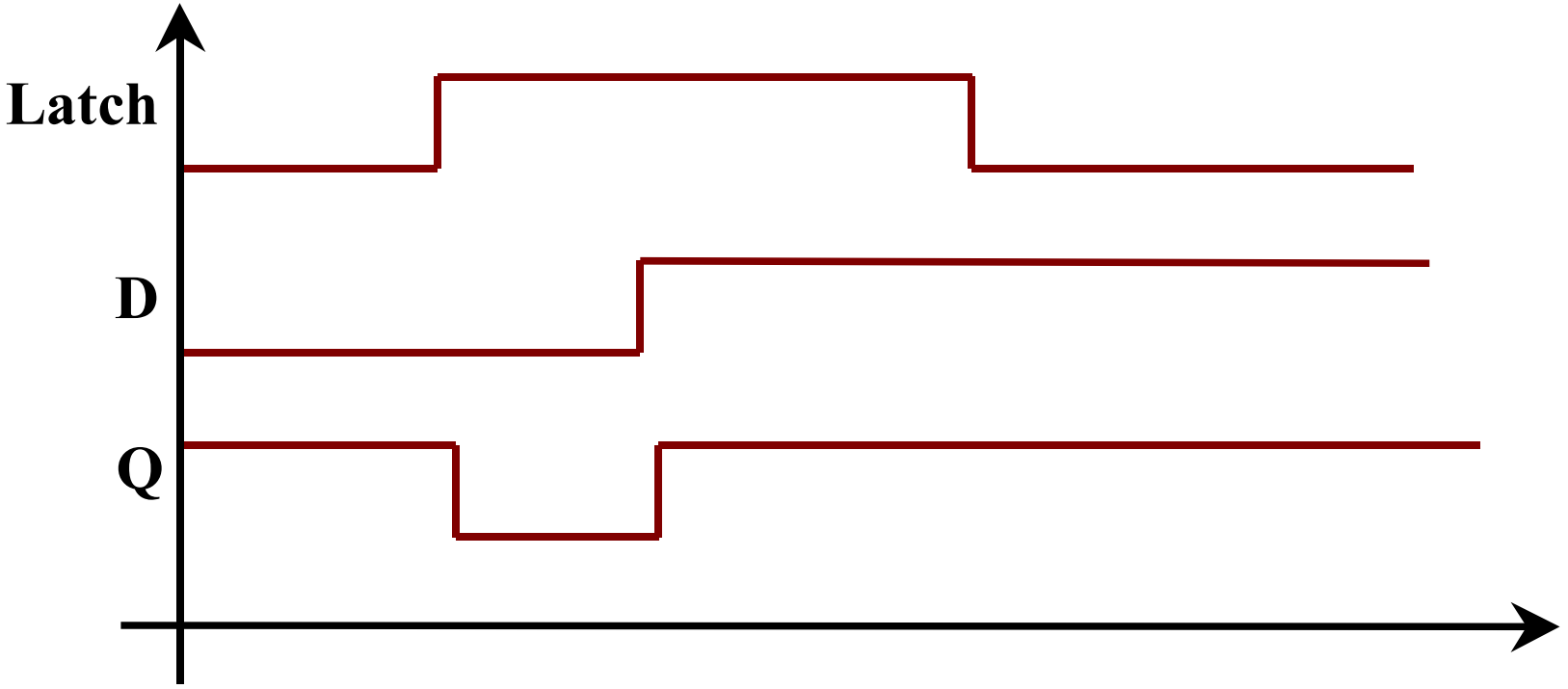


Limitations of a D-Type latch

The value that is held on the Q output of a D-Type latch is the value of D at the instant at which the latch goes from 1 to 0.

When the latch is at 1, any change on D causes a change of Q, and this is undesirable.

Undesirable output on Q when latching

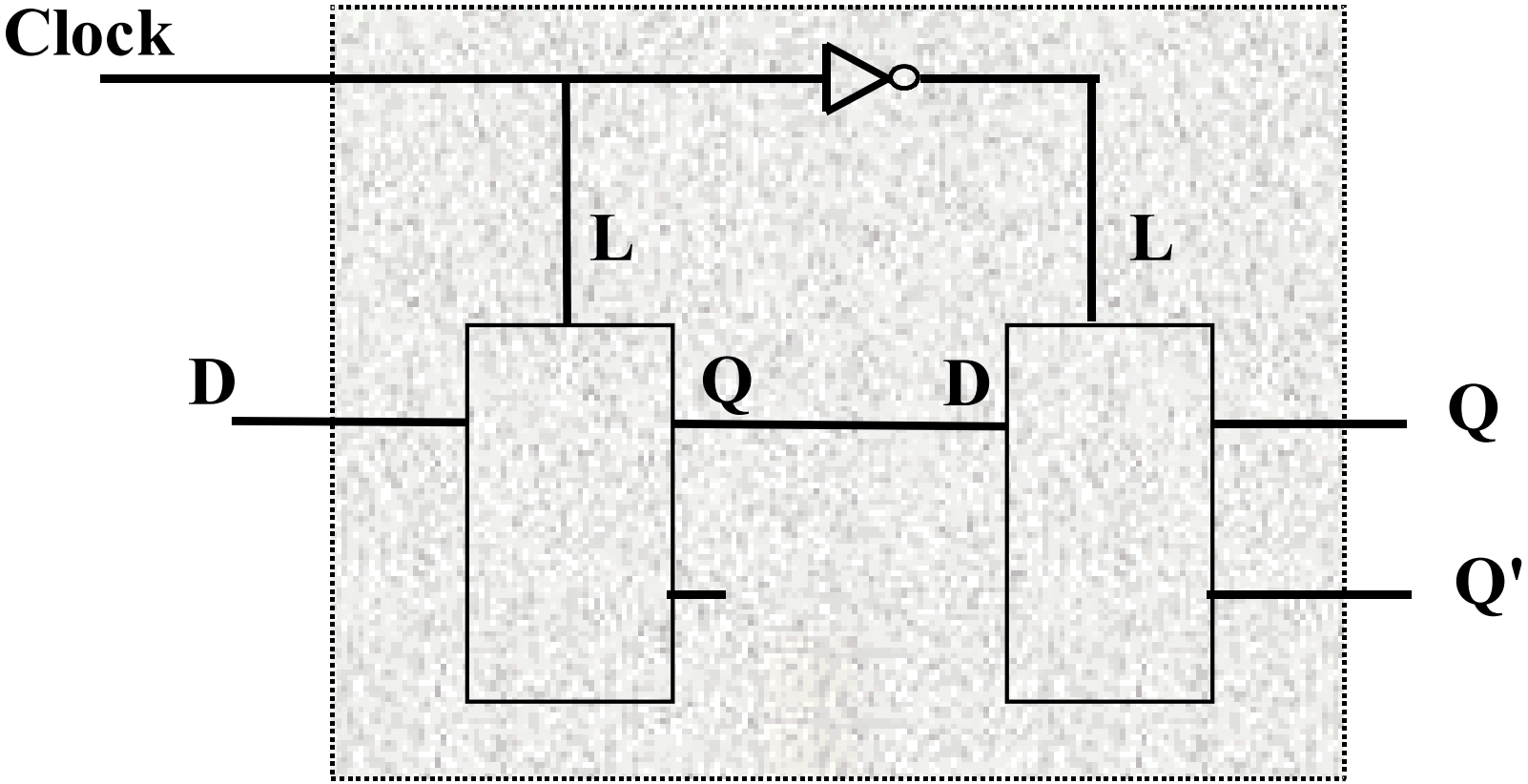


Edge triggering

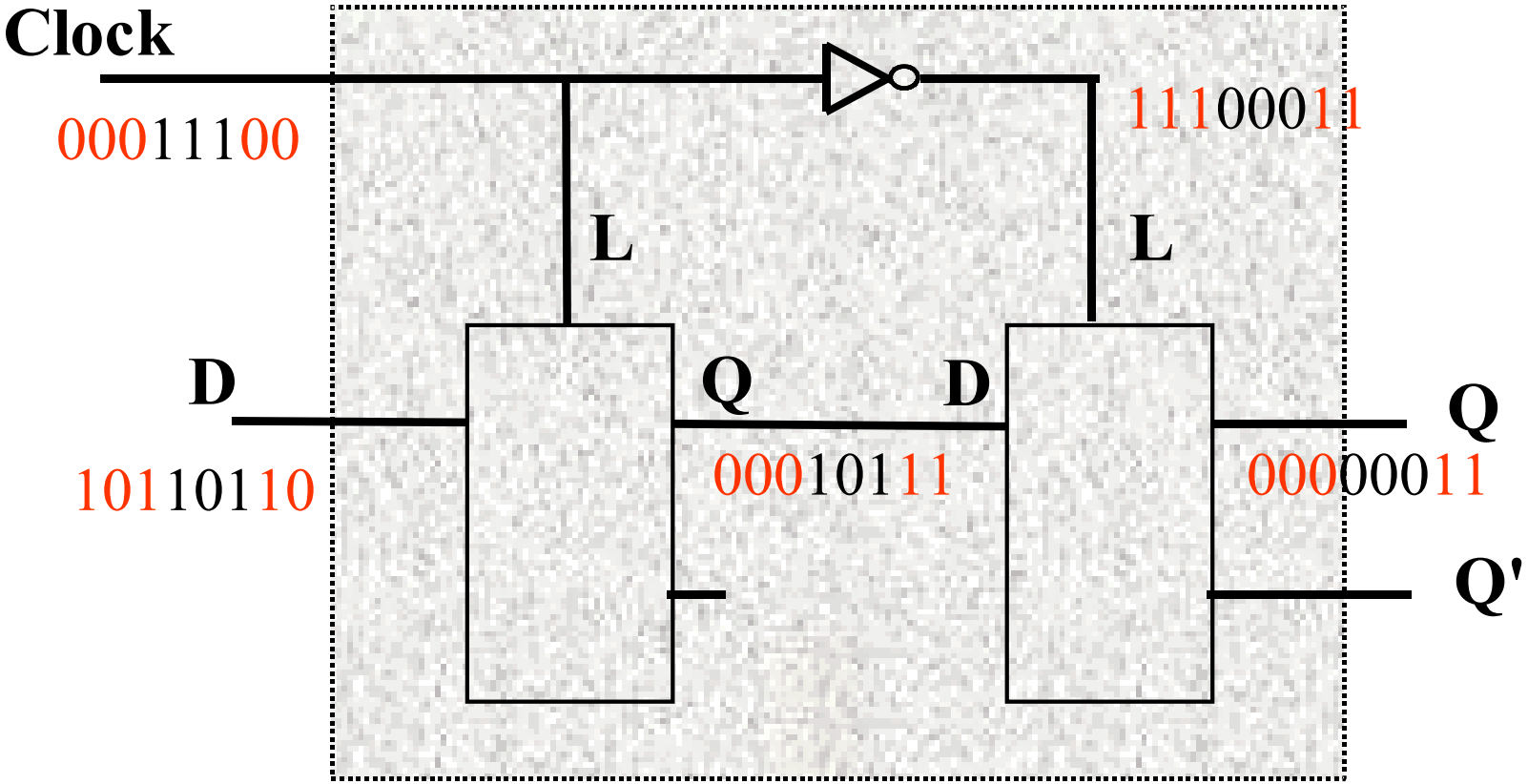
In order to avoid the undesirable "spike", we adapt the circuit so that the value of D is transferred to Q only when the control input goes from 1 to 0.

This is called an edge triggered circuit

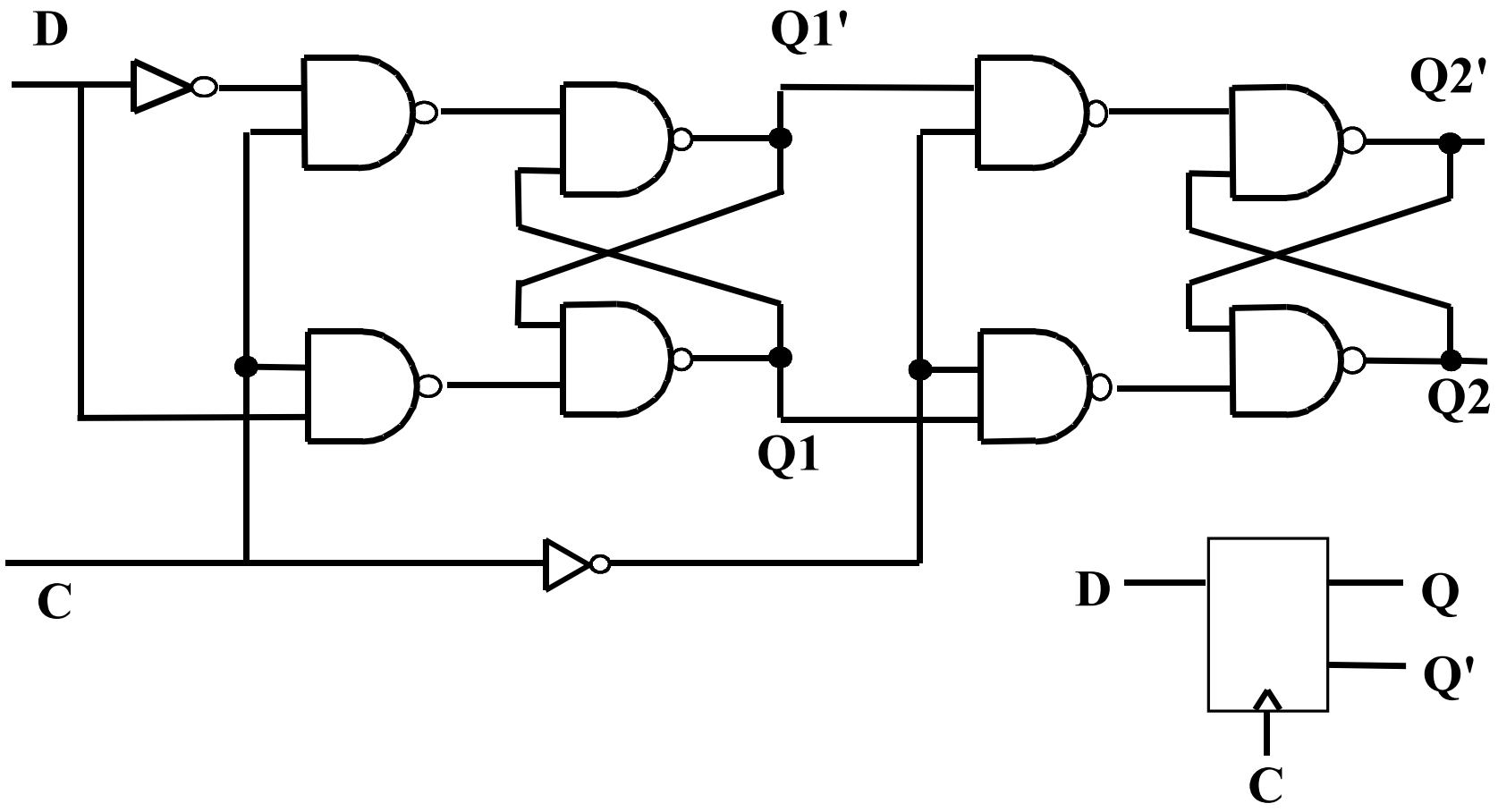
Making a D-Type flip flop from two latches



Making a D-Type flip flop from two latches



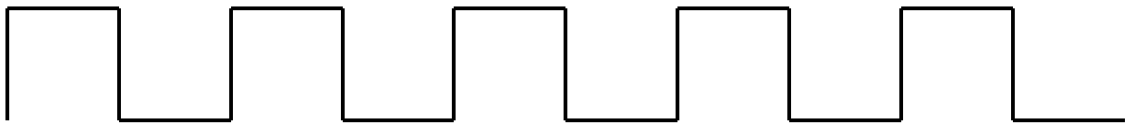
The Master-Slave D-Type flip flop



Clocks

Notice that in the master slave design of the D type flip flop we have started to refer to the control input as a clock.

Computers have clocks to drive their sequences of actions. Essentially they control the storage of bits on D-Type flip flops. They produce simply square waves.



Flip flops as finite state machines

Flip flops can be thought of as circuits that have only two states:

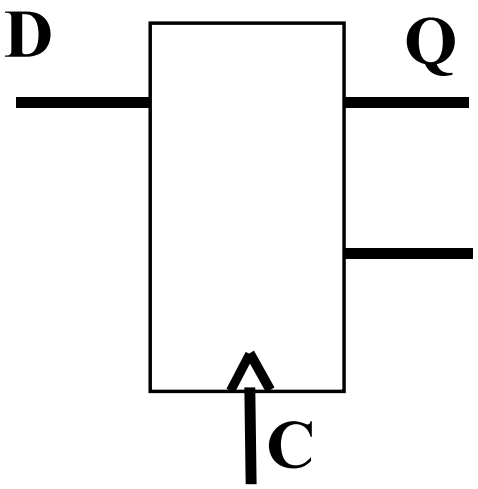
Q=0

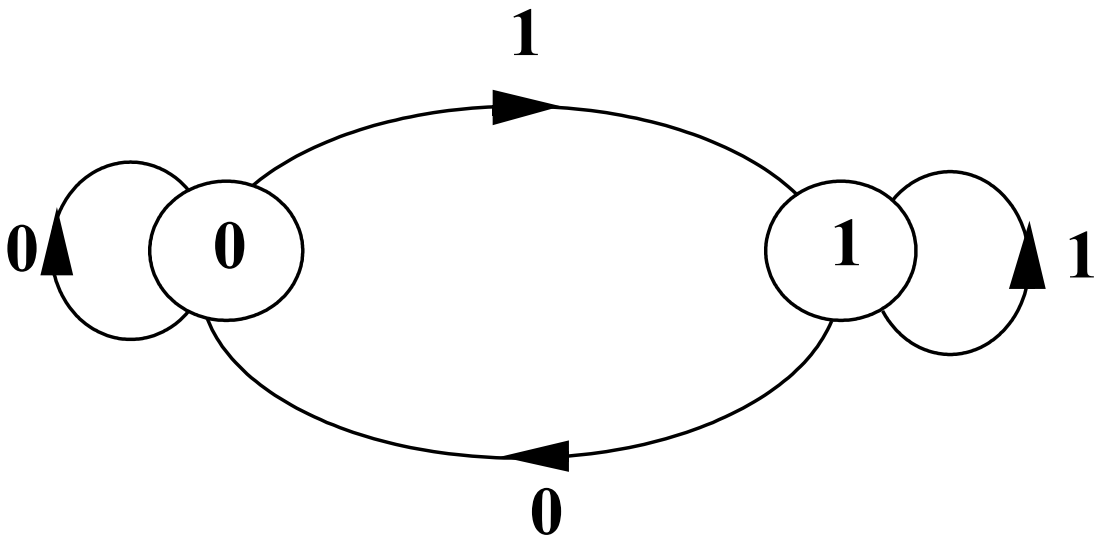
Q=1

They can change state only when falling edge is applied to the clock input.

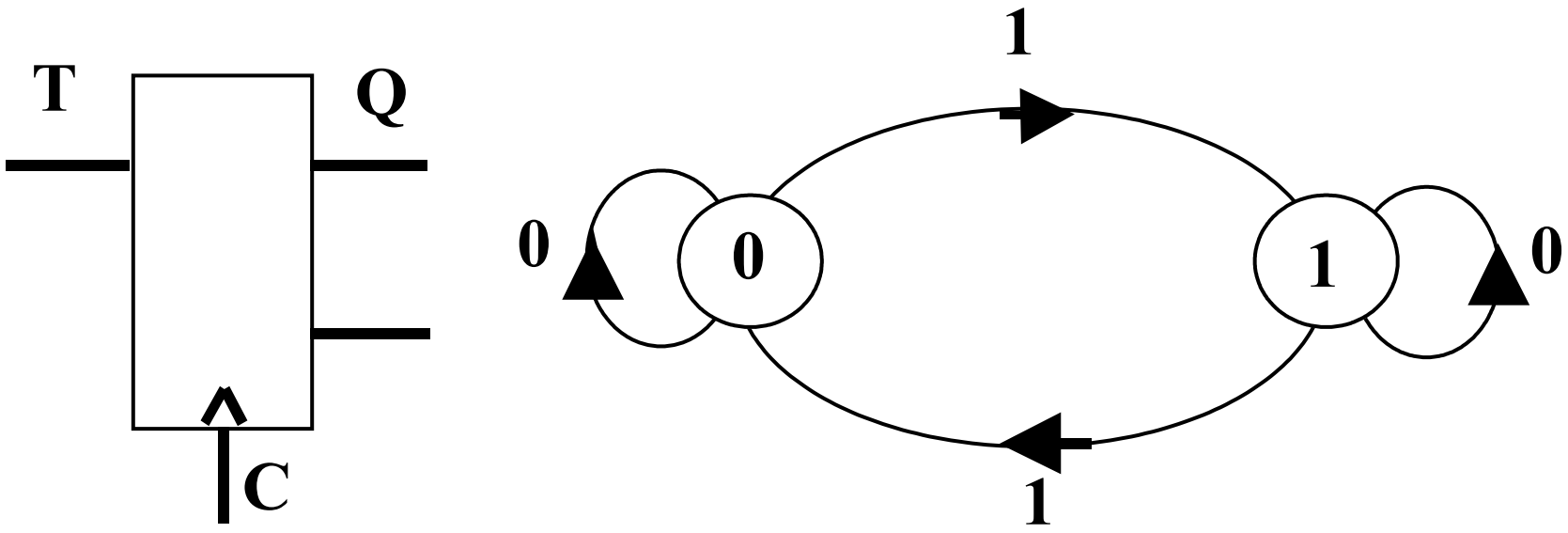
They can be thought of as finite state machines.

The D-Type flip flop and its finite state machine

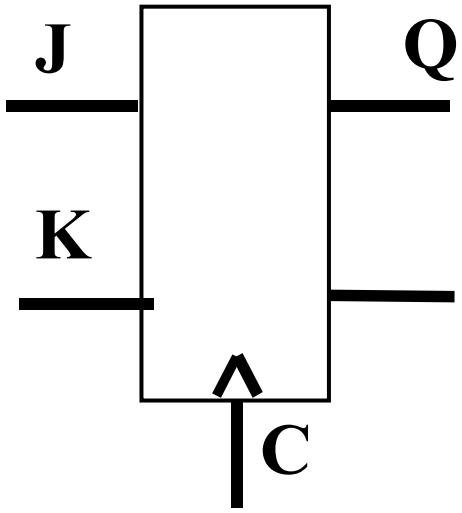


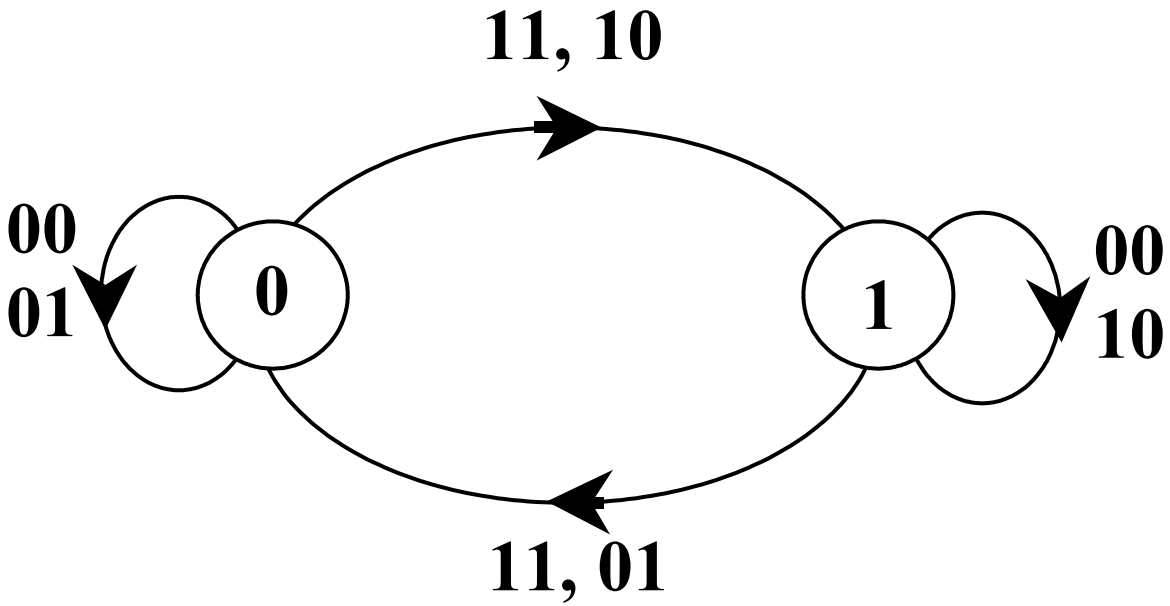


The T-Type flip flop (toggle)

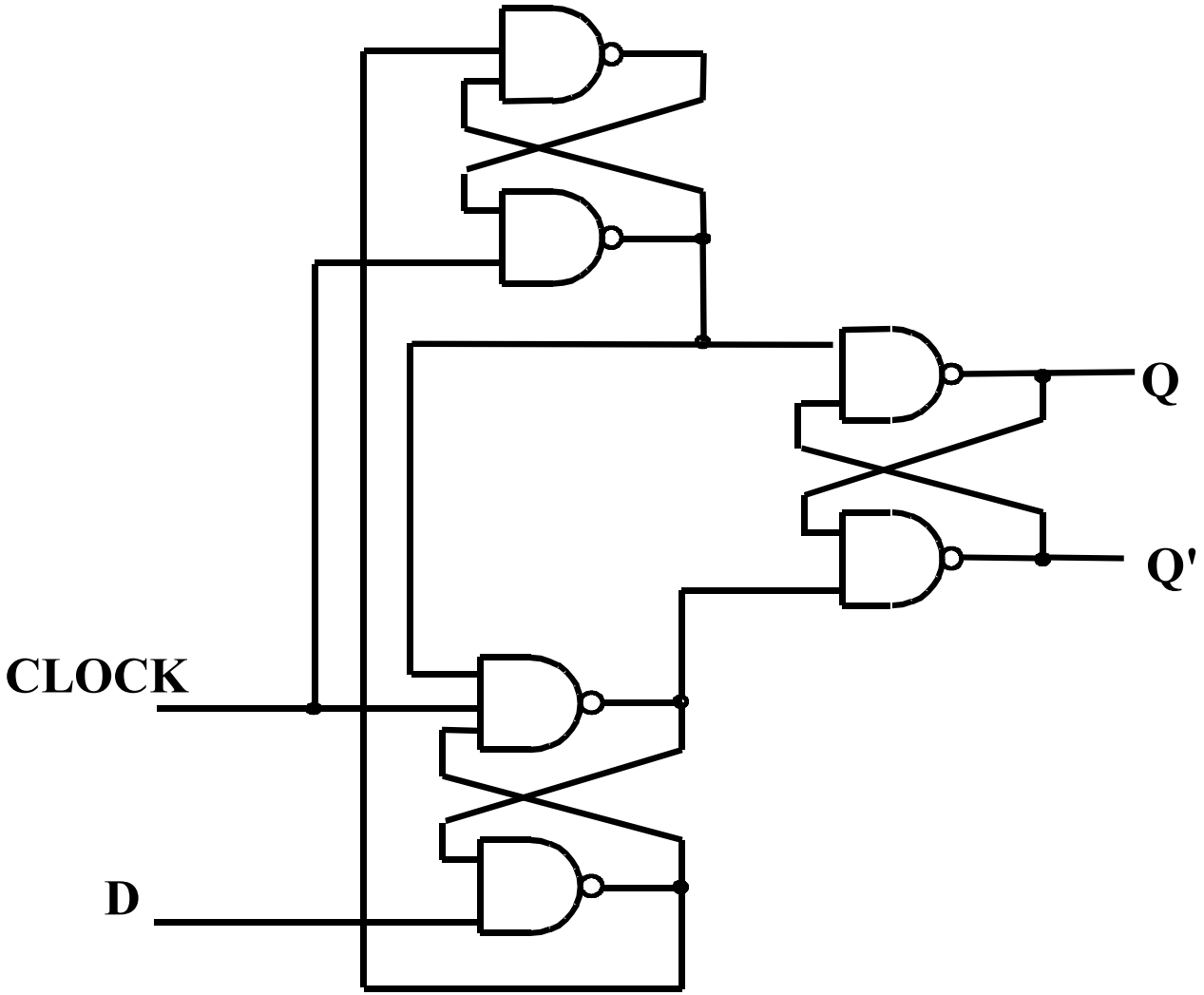


The J-K flip flop





The (rising) edge triggered flip flop



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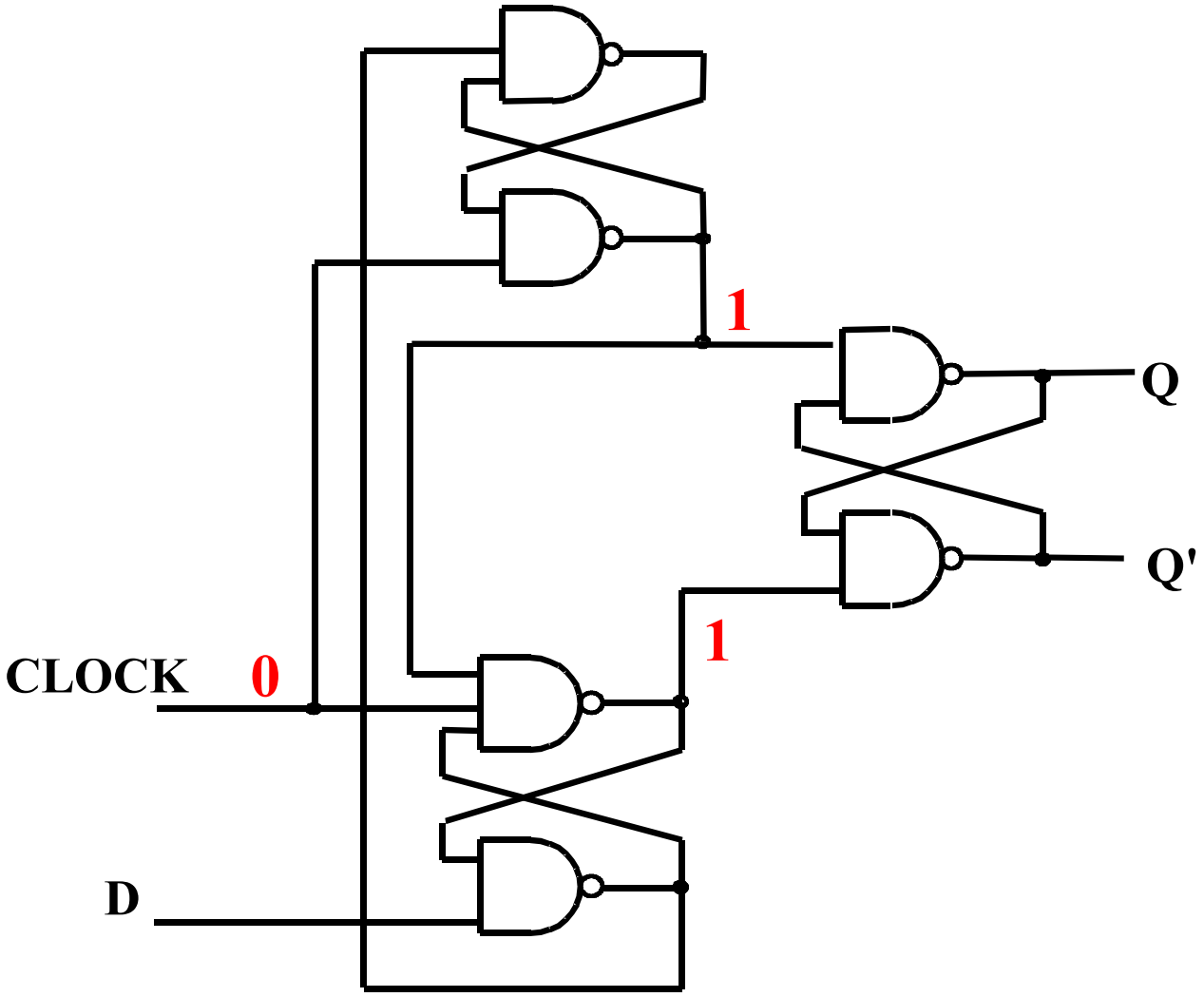

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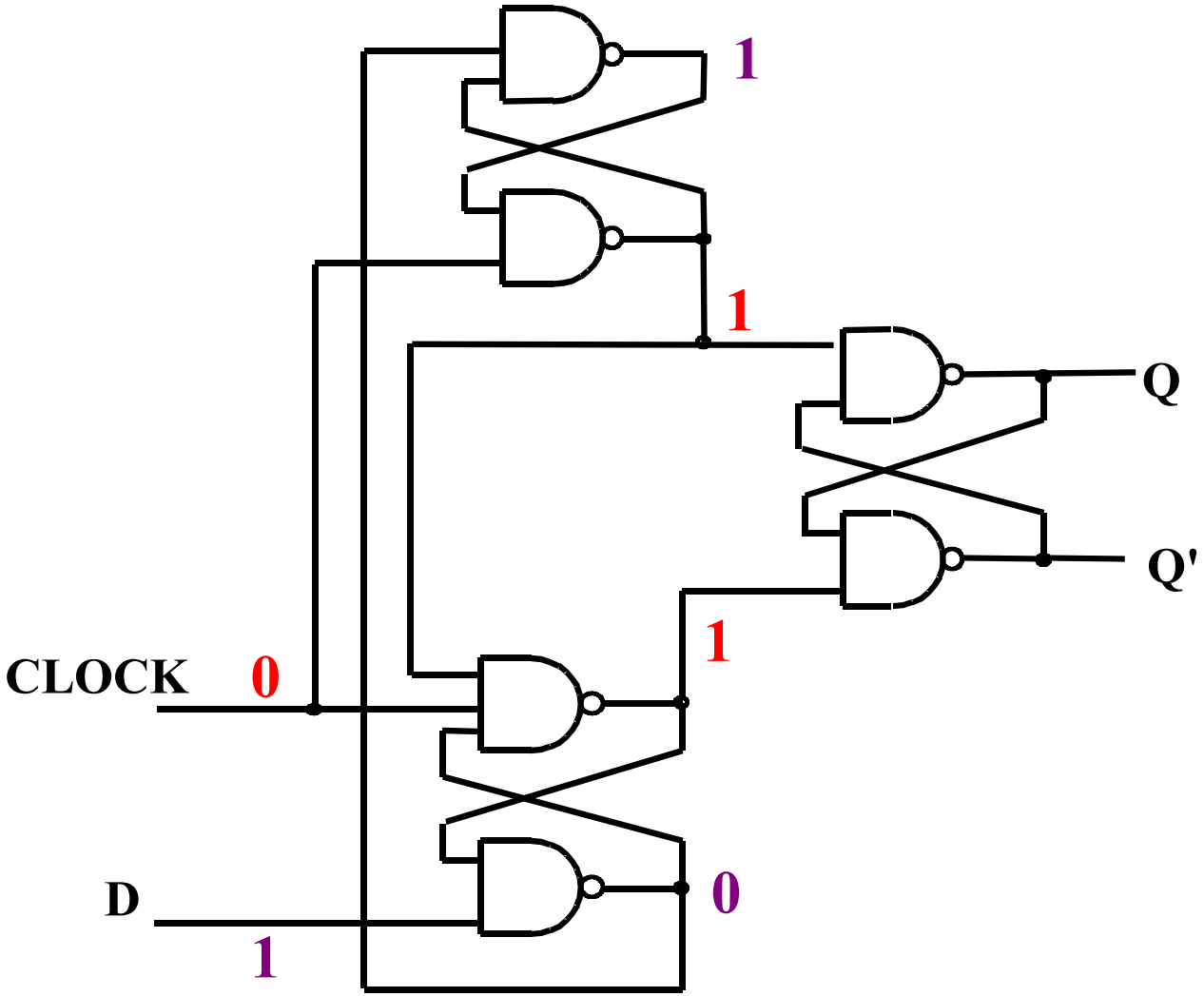
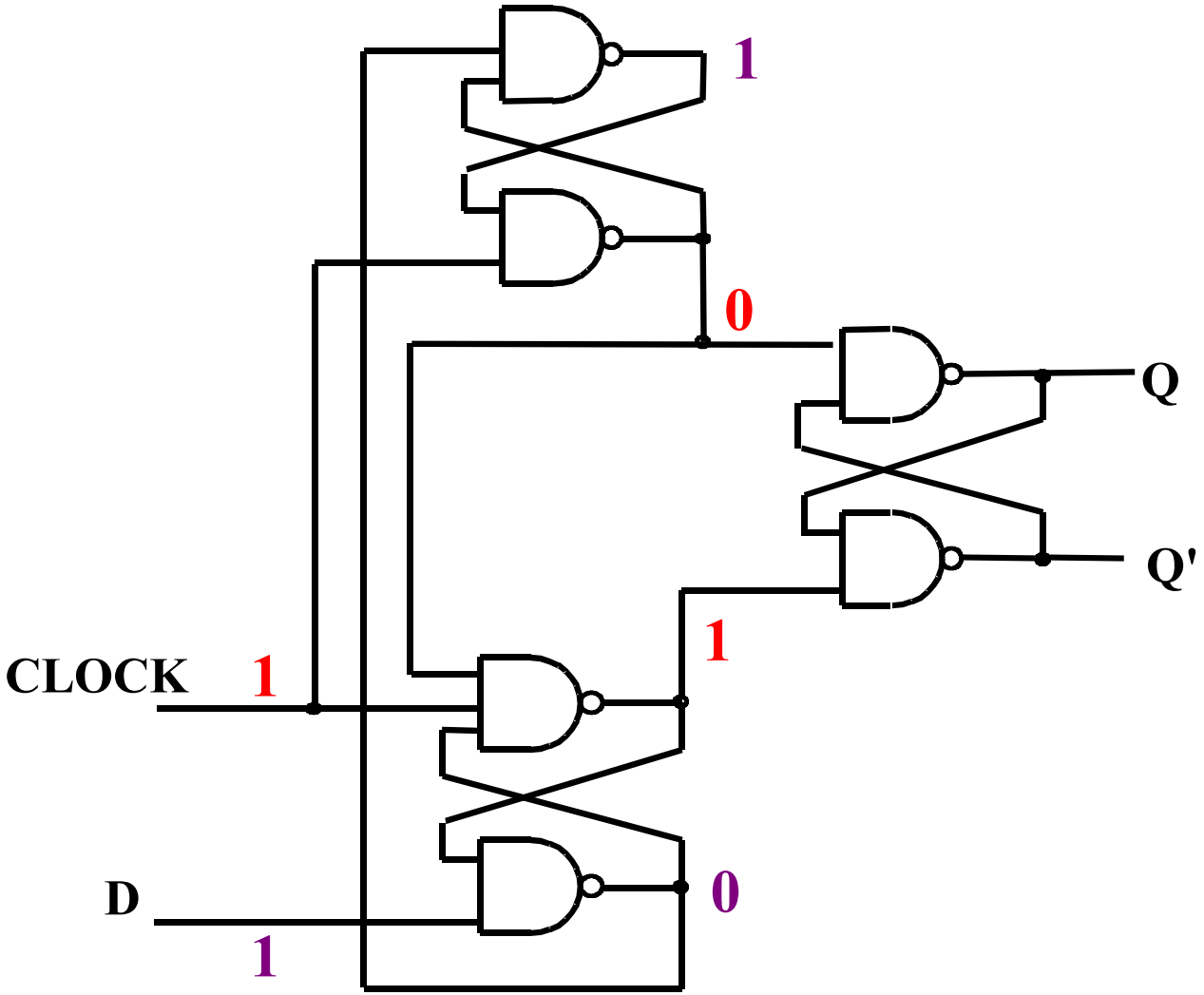


The (rising) edge triggered flip flop



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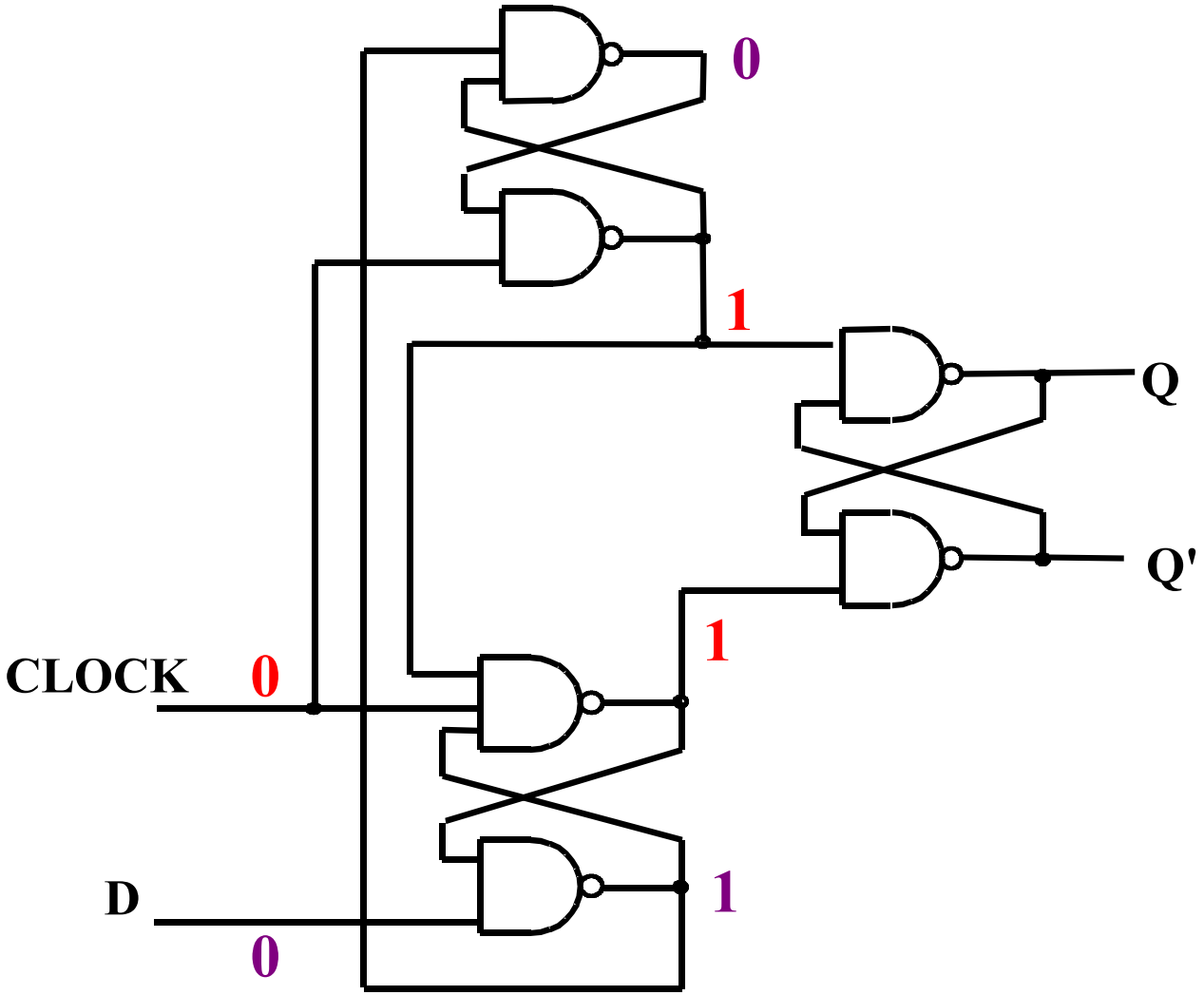

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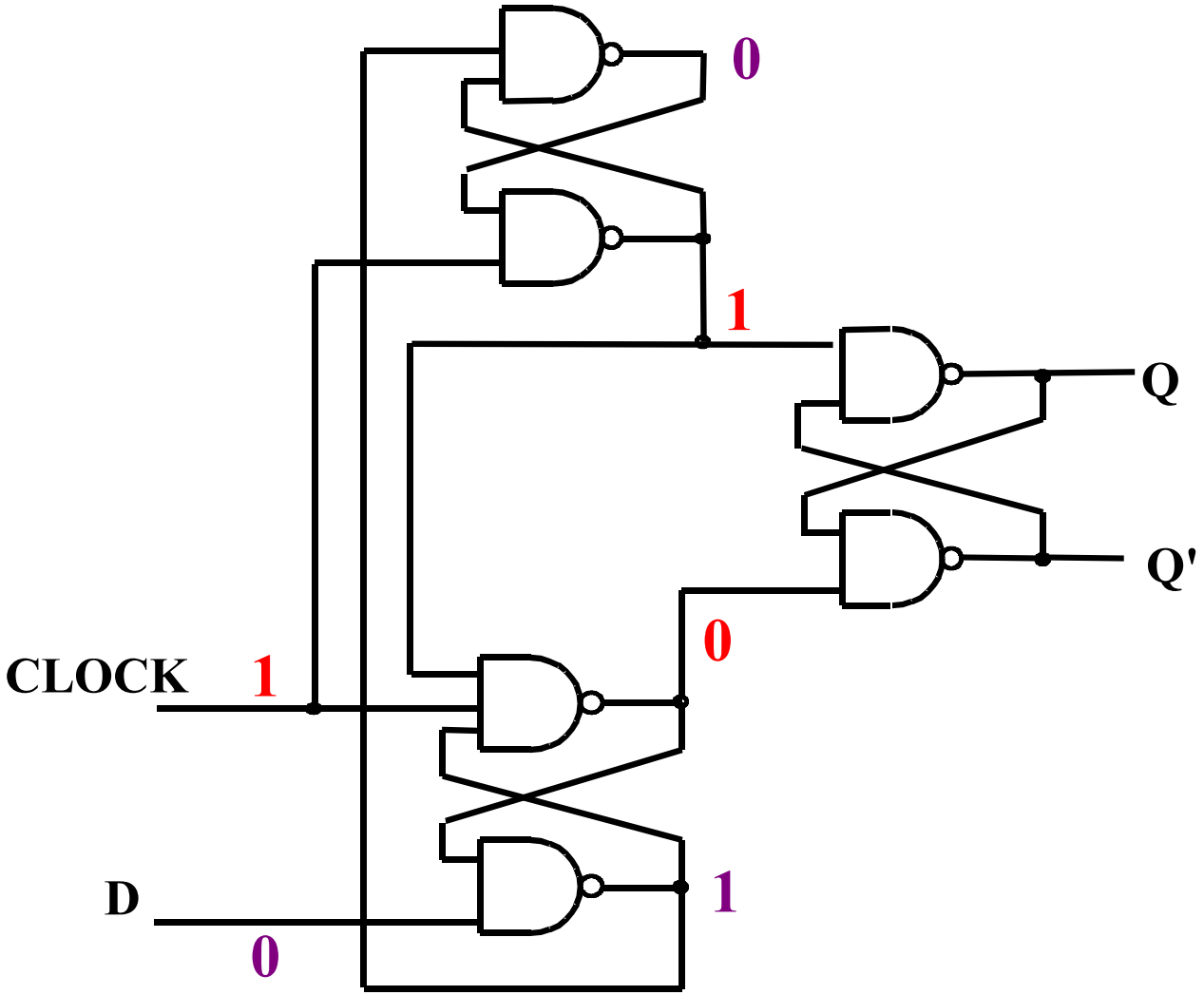

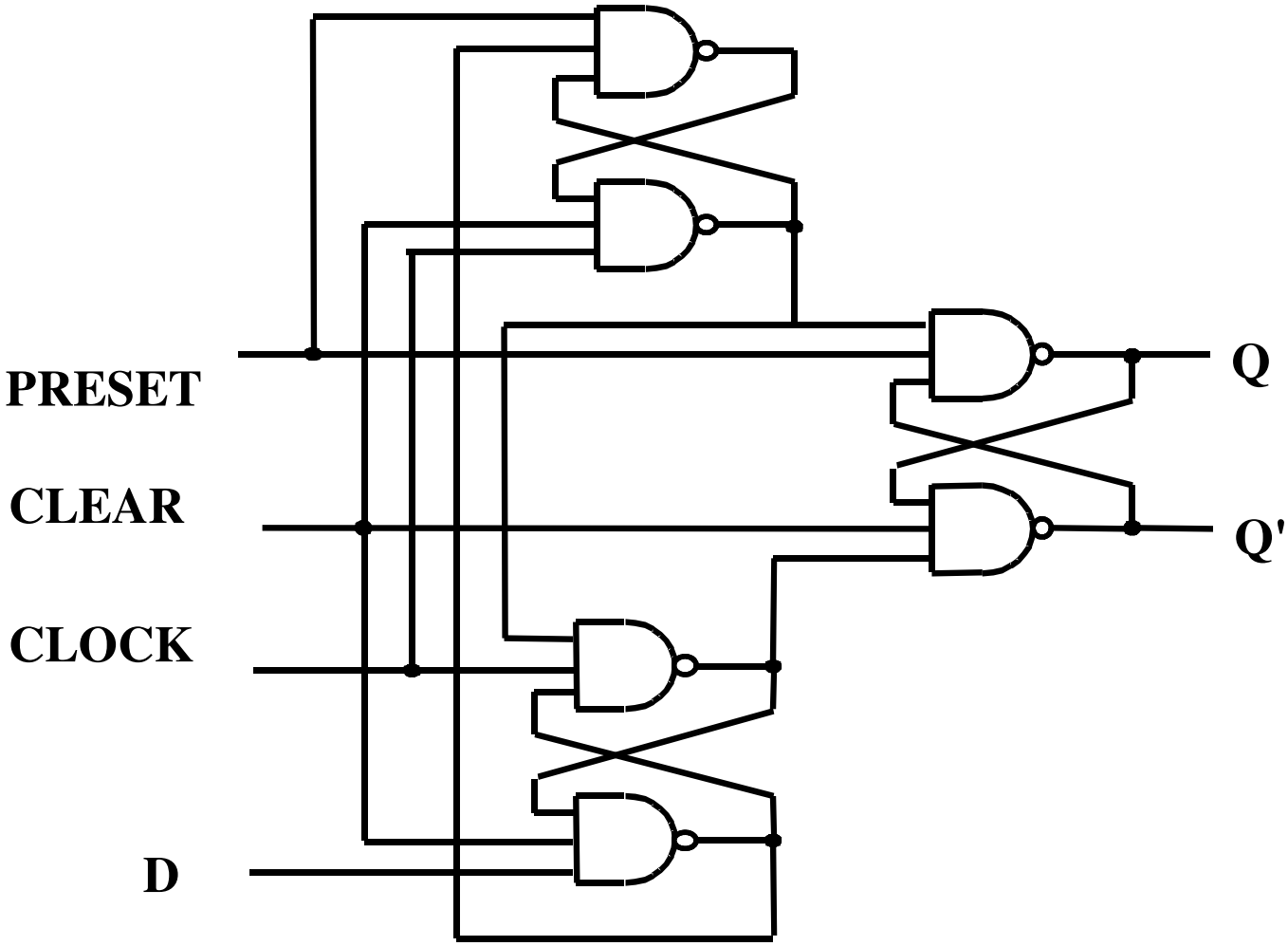
PRESET
CLEAR
CLOCK
D
Q
Q'