## **VPMP Polytechnic**

# Department of Computer Engineering Computer Organization and Architecture (4350701) Assignments

## **Assignment 1**

- 1. Explain Basic CPU Structure with diagram.
- 2. List out various 8bit, 16 bit, 32 bit intel microprocessor
- 3. Explain Various Registers used in CPU with its applications.
- 4. Differentiate: Serial Bus v/s Parallel Bus.

#### **Assignment 2**

- 1. Draw and Describe 8085 Microprocessor Architecture.
- 2. Draw the PIN DIAGRAM of 8085 & explain the detail of each pin.
- 3. Explain flag register of 8085.
- 4. Explain registers organization of 8085.
- 5. Define following terms: Instruction, Machine Cycle, T- State &Instruction Cycle.
- 6. Draw and explain the Timing Diagram for Opcode Fetch operation.

## **Assignment 3**

- 1. Define 1-Byte, 2-Byte and 3-Byte Instruction format.
- 2. Explain the addressing mode of 8085.
- 3. List and Define Data Transfer Instructions of 8085 microprocessor.
- 4. Explain the Arithmetic instructions of 8085 with example.
- 5. Define following Logical Instructions of 8085 microprocessor.
  - i) ORA ii) ORI iii) XRI iv) RLC
- 6. Define following Jump Instructions of 8085 microprocessor.
  - i) JC
  - ii) JNZ
  - iii) JPE
  - iv) JP
- 7. Explain the Machine Control instructions of 8085 with example.
- 8. What is stack? Explain stack related instruction with example.
- 9. Explain 8085 Vectored interrupts: TRAP, RST 7.5, RST 6.5, RST 5.5 and RST.
- 10. Write an assembly language program to add two numbers stored at memory locations 2040h and 2050h and also store the result into memory location 2060h.

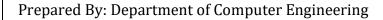
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## **Assignment 4**

- 1. Explain RAM, ROM, PROM, EPROM and EEPROM.
- 2. Describe Memory Hierarchy.
- 3. Explain Virtual Memory.
- 4. Explain cache memory with any one mapping technique.
- 5. Explain Associative Memory.
- 6. Explain Auxiliary Memory.

## Assignment 5

- 1. List and Define Modes of Data Transfer with I/O.
- 2. Explain I/O interface unit with proper diagram.
- 3. Explain Method of Asynchronous Data Transfer.
- 4. Explain CPU-IOP Communication.



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