PARMVIR SINGH

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OBJECTIVE:

Actively seeking an internship/job in the areas of Hardware, Firmware, or Software Engineering.

EDUCATION:

Bachelor of Science, Computer Engineering ***Expected:*** May 2020
California State University, Sacramento, CA
GPA: 3.34

WORK EXPERIENCE:

Cashier and Cook ***Mountain Mikes Pizza*** ***August 2015 - December 2015***

- Engaged with customers warmly and provided immediate and dedicated assistance.
- Assisted customers with prompt and polite support in-person and via telephone.

Prime Now Associate ***Amazon*** ***October 2017 – February 2020***

- Worked in a super-fast paced environment to meet daily goals.
- Provided services efficiently with high level of accuracy and problem solved minor technical difficulties.

SKILLS-LANGUAGES, TOOLS, PLATFORMS:

C/C++, Verilog, Python, JavaScript, Java, VHDL, Git, x86 Assembly, ARM Assembly, HTML/CSS, MYSQL, Eclipse IDE, Xilinx Vivado Design Suite, Multisim, OrCAD PSpice, Cadence Virtuoso, Control, DOS, Windows (XP, Vista, 8.1, 10), MS-DOS, UNIX, Linux (Ubuntu, Debian), VMWare, Punjabi,Hindi,

RELATED PROJECTS:

Senior Design Project

- *Semi-Autonomous Hydroponic Greenhouse:* Currently involved in designing and building a Semi-Autonomous Hydroponic Greenhouse with 4 other team members. The team consists of 1 Electrical Engineer (EE) and 4 Computer Engineering (CpE) students. Directly assisting with designing the Control System for all sensors and implementing the desired measurables in code for these sensors.

Java/C Projects

- *Multi-threading:* Experimenting with the performance impact of multithreading using real time measurements using the POSIX thread library on a UNIX system. I was in charge of writing a program that sorts an array of random integers first sequentially and then using multi-threading.
- *User-level Threading:* Implementing context switching using *sisetjmp* and *silongjmp.* Also, implementing two preemptive scheduling algorithms: Round-robin and Lottery scheduling and designing data structures for thread entities.

Computer Hardware Designs

- *Direct Mapped Cache Design*: In Verilog, designed and simulated a cache controller module that utilized the direct mapping scheme to store data onto cache blocks. The controller would be able to interface between a CPU and Main Memory to perform read or write operations.
- *PCI Bus Arbiter:* In Verilog, designed and simulated a PCI Bus Arbiter that performed bus arbitration among multiple master devices on a PCI Bus. The bus arbiter utilized the Round-Robin Priority Scheme to designate the PCI Bus to the appropriate master device.
- *Multi-cycle Datapath Model*: Designed and simulated a multi-cycle data path that performed either the RTN R ← A + B +C - D or the RTN R ← A -B + C + D. A control unit (FSM) was also created to provide the proper control signals to the data path.

AWARDS/CLUBS:

Deans Honor List ***Spring 2017 – Spring 2019***
MEP, *Member* ***Fall 2017 – Spring 2020***
SWE, *Member* ***Fall 2017 – Spring 2020***
SSA, *President/Member* ***Fall 2017 – Spring 2020***