Computer Architecture
(PCC-CS 492)

Laboratory Instructor's Manual

Last Revised

July, 2022

Dept. of CSE
Techno Main, Salt Lake

General INSTRUCTIONS FOR STUDENTS

1. **Do not enter into the Laboratory without prior permission.**
2. **Switch off your mobile during Lab schedule and maintain silence.**
3. **Save your file only on the specific destination as instructed.**
4. **Do not play games, view movies, chat and listen music.**
5. **Do not change desktop setting, screen saver or any other system settings.**
6. **Do not use any external storage device without prior permission.**
7. **Do not install any software without prior permission.**
8. **Do not browse any restricted, illegal or spam sites.**

INSTRUCTIONS FOR LABORATORY TEACHERS

1. **Submission related to lab assignments, which are completed, should be done during the next lab session.**
2. **The promptness of submission should be encouraged by way of marking and evaluation patterns that will benefit the sincere students.**

Program Outcomes (POs)

PO1. **Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and engineering specialization to the solution of complex engineering problems.

PO2. **Problem analysis:** Identify, formulate, research literature, and analyze engineering problems to arrive at substantiated conclusions using first principles of mathematics, natural and engineering sciences.

PO3. **Design/Development of solutions:** Design solutions for complex engineering problems and design system components, processes to meet the specifications with consideration for the public health and safety and the cultural societal and environmental considerations.

PO4. **Conduct investigations of complex problems:** Use research based knowledge including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions.

PO5. **Modern tool usage:** Create, select and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to access societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of and need for sustainable development.

PO8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. **Individual and team work:** Function effectively as an individual, and as a member or leader in teams, and in multidisciplinary settings.

PO10. **Communications:** Communicate effectively with the engineering community and with the society at large. Be able to comprehend and write effective reports documentation. Make effective presentations and give and receive clear instructions.

PO11. **Project management and finance:** Demonstrate knowledge and understanding of engineering and management principles and apply these to one's own work, as a member and leader in a team. Manage projects in multidisciplinary environments.

PO12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

PSO1: Ability to develop the solutions for scientific, analytical and research-oriented problems in the area of Computer Science and Engineering.

PSO2: Ability to apply suitable programming skills integrated with professional competence to develop applications catering to the industrial and societal needs in the field of Computer Science and Engineering and its allied areas.

NAME OF THE PROGRAM: *CSE*	**DEGREE:** *B.Tech*
COURSE NAME: *Computer Architecture*	**SEMESTER:** *4th*
COURSE CODE: *PCC-CS 492*	**COURSE CREDIT:** *2*
COURSE TYPE: *LAB*	**CONTACT HOURS:** *4P*

Syllabus

All laboratory assignments are based on Hardware Description Language (VHDL or Verilog) Simulation.

Pre-requisite: The hardware based design has been done in the Analog & Digital Electronics laboratory and Computer Organization laboratory

1. HDL introduction

2. Basic digital logic base programming with HDL

3. 8-bit Addition, Multiplication, Division

4. 8-bit Register design

5. Memory unit design and perform memory operations.

6. 8-bit simple ALU design

7. 8-bit simple CPU design

8. Interfacing of CPU and Memory

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COURSE TYPE: ***LAB***	**CONTACT HOURS:** ***4P***

Course Outcomes (CO)

After this course students will be able to:

CO1: Construct suitable combinational or sequential module's solution circuit schematic in Xilinx platform using VHDL.

CO2: Develop a formal test bench using informal requirements in VHDL and simulate the test cases to check the productivity of the circuit.

CO3: Construct integrated circuit designs like memory and processing units and further integrate them together to observe their behavioral and functional execution using Xilinx and iSim.

CO4: Inspect various schematic presentation and simulation features of Xilinx as an environment through hardware description language and gather expertise as an individual.

CO5: Compose structured and informative report of the solution to the corresponding problem along with verifies test cases.

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Exp. No.	List of Experiments	Date
1.	Illustration of basic Gates: AND, OR & NAND	**Week 1**
	Verify the results using a test bench	
2.	Design a HALF ADDER (Using Basic Gate), FULL ADDER (Using Basic Gate) and FULL ADDER using 2 HALF ADDERs.	**Week 2**
	Verify the results using a test bench	
3.	Design a HALF SUBTRACTOR (Using Basic Gate), FULL SUBTRACTOR (Using Basic Gate), FULL SUBTRACTOR using 2 HALF SUBTRACTORs.	**Week 3**
	Verify the results using a test bench	
4.	Design of 4-BIT ADDER and 4-BIT SUBTRACTOR using FULL ADDER and FULL SUBTRACTOR as component. Use buses for each of the input signal lines.	**Week 4**
	Verify the results using a test bench	
5.	Create a 4-BIT COMPOSITE ADDER-SUBTRACTOR UNIT using 1-BIT ADDER and XOR gate as components. Use buses for each of the input signal lines.	**Week 5**
	Verify the results using a test bench	
6.	Create a 4-BIT COMPARATOR. Use buses for each of the input signal lines.	**Week 6**
	Verify the results using a test bench	
7.	Create 8:1 MULTIPLEXER with select lines. Use buses for each of the input signal. lines	**Week 7**
	Create 1:8 DEMULTIPLEXER with select lines. Use buses for each of the input signal lines.	
	Verify the results using a test bench	
8.	Design a behavioral simulation of JK, SR, D and T FLIP FLOP. Consider clock period = 2 ps	**Week 8**
	Verify the results using a test bench	
9.	Design a 4-BIT SERIAL IN and PARALLEL OUT (SIPO) SHIFT REGISTER.	**Week 9**
	Design a 4-BIT PARALLEL IN and SERIAL OUT (PISO) SHIFT REGISTER.	
	Verify the results using a test bench	
10.	Design a 4-BIT UP-DOWN COUNTER.	**Week 10**
	Verify the results using a test bench	

Exp. No.	List of Experiments	Date
11.	Design a 4-BIT ALU.	**Week 11**
	Verify the results using a test bench	
12.	Design a 128 x 8 RAM	**Week 12**
	Verify the results using a test bench	
Beyond Syllabus: Build a 4-Bit ALU and realize its operations on Altera DE2-115 FPGA board.		

Rubrics for Lab PCC-CS 492

Criteria / Score	Excellent (10-8)	Good (7-6)	Average (5-4)	Poor (3-1)	CO Mapping	PO/PSO Mapping
Lab Participation (Following Procedure +Lab Techniques+ Subject Knowledge + Contribution)	Student demonstrates an accurate understanding of the lab assignments. The student can correctly answer questions and if appropriate, can explain concepts to fellow classmates. Student is eager to develop new ideas and assists when needed.	Student arrives on time to lab, but may be underprepared. Answers to questions are basic and superficial suggesting that concepts are not fully grasped. Able to follow the instruction and somehow managed to execute the program.	Student unpreparedness makes it impossible to fully participate. If able to participate, student has difficulty explaining key lab concepts.	There was no attempt to make prior arrangements to make up the lab. Attendance is not regular. Not able to run the program even after getting help from the peers.	**CO1, CO2, CO3, CO4**	**PO1, PO2, PO3, PO5 PSO1, PSO2**
Interaction with Group (Team work)	Very good participation with a good leadership quality; is respectful of others and their point of view; makes sure that everyone gets a turn; conscious of time; shares test cases with everyone for thorough reporting	Good participation; appears interested; enthusiastic but talks over teammates; try to help group complete tasks; somewhat conscious of time; shares test cases with everyone for thorough reporting	Minimal participation; shows little interest; doesn't pay attention to other group members; may argue to get point across; helps group only when asked; little emphasis on time; not very keen on sharing	No participation; sits on the sidelines with no interaction; disinterested; no stake in time management; not keen to share at all	**CO4, CO5**	**PO9**
Execution and Testing (Modern tool usage)	Follow the logical ideas; can develop suitable schematic from	Can develop suitable schematic from specific circuit with	Can develop suitable schematic from specific circuit with	Not be able to develop schematic from specific circuit; need	**CO2, CO3, CO4**	**PO5, PSO2**

Criteria / Score	Excellent (10-8)	Good (7-6)	Average (5-4)	Poor (3-1)	CO Mapping	PO/PSO Mapping
	specific circuit; debug the program with proficiency; Able to check the reliability with suitable test benches.	the help of the instructor; debug the program with proficiency; Able to check the reliability with suitable test benches	the help of the instructor; debug the program with the help of technical assistant; Not able to check the reliability.	assistance to debug the program. Not able to check the reliability		
Lab Report	Student demonstrates an accurate understanding of the lab concepts. Questions are answered and reported completely and correctly. Output of each program is neat, creative and includes complete titles. Errors, if any are minimal	Student has a basic knowledge of content, but may lack some understanding of some concepts. Questions are answered and reported fairly well and/or output could have been done more neatly, accurately or with more complete information	Student has problems with both the output and the answers. Student appears to have not fully grasped the lab content and the code possess multiple errors	Student turns in lab report late or the report is so incomplete and/or so inaccurate that it is unacceptable.	**CO5**	**PO10**