Parnian Shabani Kamran

Electrical and Computer Engineering Department, University of California, Davis, CA, 95616
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RESEARCH INTERESTS

Development of safe software systems using static and dynamic analysis, fuzz testing and formal verification, Analysis and measurement of open source supply chain threats, Development of safe and reliable Transformer-based code generation and code completion tools with using formal verification

SKILLS

Programming:	Rust, Python, Dafny, C++11, JavaScript
Libraries:	Hypothesis, Pandas, NumPy, PyTorch, OpenCV, LangChain
Software & Tools:	**Theorem Prover:** Z3
	Parallel Programming: OpenCilk
	Performance Analyzer: Intel VTune, AMD uProf, Perf
	Machine Learning: WEKA, LangChain

EDUCATION

Ph.D. Computer Engineering *2021 - 2025*
Department of Electrical and Computer Engineering, University of California, Davis
Current Research: Improving Large Language Models trustworthy in code completion tasks using formal verification methods with using the most recent prompting and reasoning techniques including Chain of Thought (COT), using LLM agents and external knowledge with Retrieval-Augmented Generation (RAG)
Supervisor: Caleb Stanford

M.Sc. Computer Engineering *2014 - 2016*
Department of Computer Engineering, Tehran Polytechnic, Tehran, Iran
Thesis: Design and development of a process-variation resilient aging sensor for detecting hardware aging in the presence of process verification
Supervisor: Hamid R. Zarandi

B.Sc. Computer Engineering *2008 - 2013*
Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, Iran
Thesis: Development of an Android application for currency recognitions for visually-impaired people

RESEARCH PUBLICATIONS

Parnian Kamran, Premkumar Devanbu, and Caleb Stanford. 2024. **Vision Paper: Proof-Carrying Code Completions**. In 39th IEEE/ACM International Conference on Automated Software Engineering Workshops (ASEW '24), October 27-November 1, 2024, Sacramento, CA, USA. ACM, New York, NY, USA, 7 pages. https://doi.org/10.1145/3691621.3694932

A. A. Zeraatkar, **P. S. Kamran**, I. Kaur, N. Ramu, T. Sheaves and H. Al-Asaad, **On the Performance of Malware Detection Classifiers Using Hardware Performance Counters**, 2024 International Conference on Smart Applications, Communications and Networking (SmartNets), Harrisonburg, VA, USA, 2024, pp. 1-6, doi: 10.1109/SmartNets61466.2024.10577644.

A. A. Zeraatkar, **P. S. Kamran** and H. Al-Asaad, **Advancements in Secure Computing: Exploring Automated Repair Debugging and Verification Techniques for Hardware Design**, 2024 IEEE 14th Annual Computing and Communication Workshop and Conference (CCWC), Las Vegas, NV, USA, 2024, pp. 0357-0364, doi: 10.1109/CCWC60891.2024.10427806.

WORK EXPERIENCE

Software Engineer, Snapptrip, Tehran, Iran *2017 - 2020*

- I worked on development of a single page applications for B2C to improve customer's experience and automating manual tasks of agents and service providers

Intern in Huawei LTE Network Optimization Team, Tehran, Iran *2016 - 2017*

- I worked on automation of tracking network failures to improve customer's experience and decrease the network failure rate

RESEARCH & TEACHING EXPERIENCE

Research Assistant, UC Davis, CA *Fall 2021 - present*

- My research focus is on enhancing the trustworthy of Transformer-based code completion and code generation tools using formal verification methods and applying the most recent prompting and reasoning methods to improve the models ability in satisfying the user's demanded safety policies in their tasks

Teaching Assistant, UC Davis, CA *Spring 2024*

- I was TA for ECS 189C Software Correctness, A sophomore-level course in Dafny, Z3 and Hypothesis, and Rust

Teaching Assistant, UC Davis, CA *Winter 2023*

- I was TA for EEC 180 Digital Systems II, A sophomore-level course in Verilog

Teaching Assistant, UC Davis, CA *Fall 2022*

- I was TA for EEC 193A Senior Design Project, A sophomore-level course in Internet of Things

Research Assistant, DADS Lab, Tehran Polytechnic, Tehran, Iran *2014 - 2016*

- My research focus was on design and development of a process-variation resilient aging sensor that mitigated digital circuits degradation caused by aging

Teaching Assistant, Tehran Polytechnic, Tehran, Iran *Fall 2016*

- I was TA for Computer Architecture, A sophomore-level course in VHDL

Teaching Assistant, Isfahan University of Technology, Isfahan, Iran *Spring 2013*

- I was TA for Digital System Design II, A sophomore-level course in Verilog

Teaching Assistant, Isfahan University of Technology, Isfahan, Iran *Fall 2011*

- I was TA for Digital System Design, A sophomore-level course in Verilog

ACADEMIC SERVICES

- Session chair for ASE *October 2024*
- Reviewer for IEEE Access *Summer 2024*
- Committee Member of FPGA Hackathon, Tehran Polytechnic (Amirkabir University), Tehran, Iran *Fall 2015*

VOLUNTEER EXPERIENCES

- Student volunteer for ASE *October 2024*