Experiment #1 - Clock and Periodic Signal Generation

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***Abstract*— This document is a student report to experiment #1 of Digital Logic Laboratory course at ECE Department, University of Tehran. In this series of experiments, the method of using Power Supply, Function Generator, Oscilloscope and ICs was learned, and at the end the Counter as a Frequency Divider with T Flip-Flop was created.**

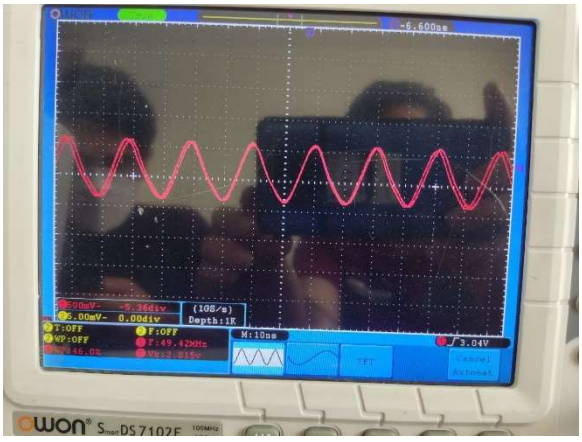
***Keywords*— LM555, Counter, Ring Oscillator, 74HC193N, HD74LS04P.**

I.INTRODUCTION

In this experiment, a Ring Oscillator, LM555 timer, Schmit Trigger, Frequency Divider Counter with T FLIP-FLOP were made.

II. CLOCK GENERATION USING ICs AND ANALOG COMPONENTS

A. Ring Oscillator



This is the waveform of a Ring Oscillator made by five parallel inverters. IC 74HCT04 is used.

$$T = 2N * delay_{inverter}$$

T = 20.2 ns
F = 48 MHz
N = 5

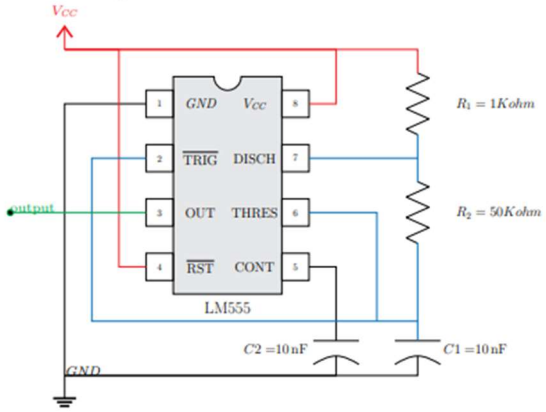
So the delay of one inverter is:

$$delay_{inv} = \frac{20.2}{10} = 2.02ns$$

B. LM555 timer

LM555 was used with this wiring for generating clock signal.

Figure 4: LM555 in astable mode



For calculating the duty cycle we used this formula:

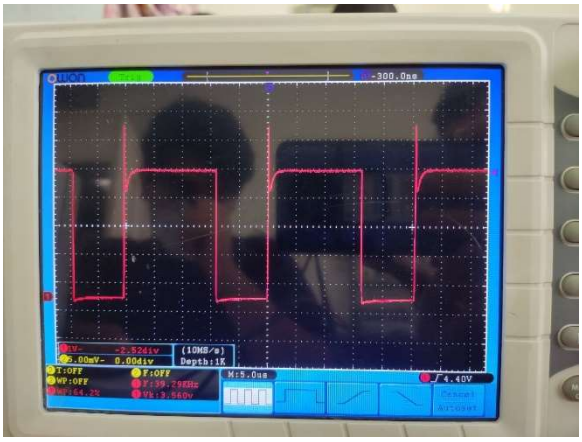
$$duty\ cycle = \frac{R1+R2}{R1+2R2}$$

But for calculating the real duty cycle we used this formula:

$$duty\ cycle = \frac{rising\ time}{cycle\ time}$$

We performed this experiment in three stages with different values for the R2, and the data obtained are as follows.

1)



R1 = 1 kΩ, R2 = 1 kΩ,

f = 40 KHz

$$expected\ duty\ cycle = \frac{1+1}{1+2} = \frac{2}{3}$$

$$real\ duty\ cycle = \frac{16.5 * 5\mu s}{25.5 * 5\mu s} = 0.64\mu s$$

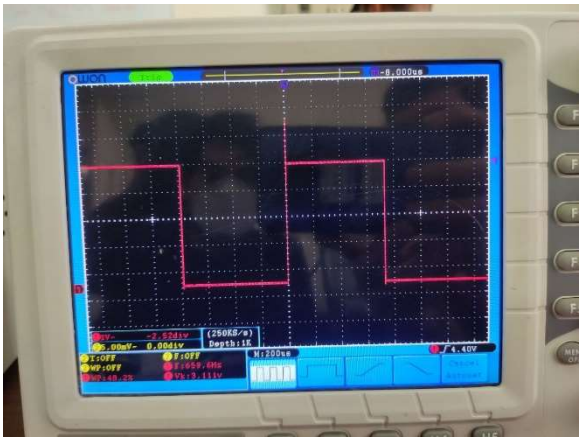
2)

R1 = 1 kΩ, R2 = 10 kΩ
f = 5 KHz

$$expected\ duty\ cycle = \frac{1+10}{1+20} = \frac{11}{21}$$

$$real\ duty\ cycle = \frac{20.5 * 20\mu s}{22 * 20\mu s} = 0.48\mu s$$

3)



R1 = 1 kΩ, R2 = 100 kΩ
f = 650 Hz

$$expected\ duty\ cycle = \frac{1+100}{1+200} = \frac{101}{201}$$

$$real\ duty\ cycle = \frac{18.3 * 200\mu s}{20 * 200\mu s} = 0.48\mu s$$

According to the test results, it is concluded that the wavelength increases and the frequency decreases with the increase of the R2 value, And the real duty cycle becomes closer to 0.5.

C. Schmitt Trigger Oscillator

D. Synchronous Counter as a Frequency Divider

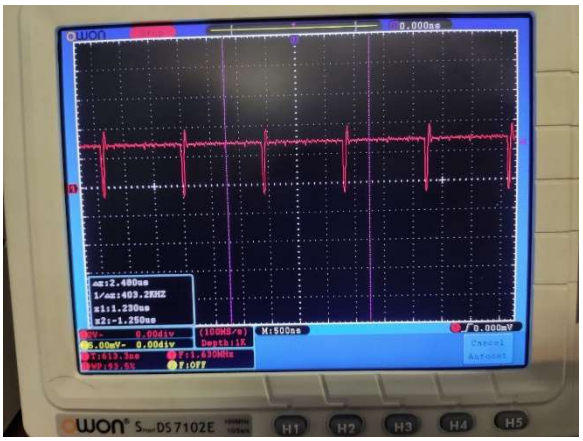
We made a frequency divider using 74HC193N and HD74LS04P ICs. 74HC193N was used to make the counter and HD74LS04P was used to make the And gates.
The piece in part 1.1 was also used for the Not gates.

To make a 200 divider, we need to cascade two 4-bit counters together. Then give the result 255 - 200 to the counters.

255 – 200 = 55 = 00111000
Then upload 0011 to MSB, and 1000 to LSB.
The Ring Oscillator output frequency was equal to 12 MHz.
The output frequency from LMB was equal to 1.6 MHz, which is approximately equal to 1/8 of the output frequency from the Ring Oscillator, and the reason for this frequency is that we gave 1000 as an P0-p3 to LMB, which causes Cout to become 1 every 8 cycles. And the frequency becomes 1/8.
In a similar way, the output frequency MSB is almost equal to 800 KHz.

E. T FLIP-FLOP

In the last part of experiment, we made a t flip-flop with 74HC74 IC. Then connected the output of frequency divider to the input of t flip-flop.
The output frequency of the t flip-flop is half of the input frequency. $f = \frac{800}{2} = 400khz$



The output frequency of the t flip-flop that was connected to the LMB output was 800 KHz, which was ½ of the LMB frequency. In the picture above, the output of the t flip-flop is shown.