دانشکده مهندسی کامپیوتر

آزمایشگاه طراحی سیستم‌های دیجیتال

گزارش آزمایش دوم

دکتر سیاوش بیات سرمدی

پارسا محمدیان — ۹۸۱۰۲۲۸۴

۱۸ فروردین ۱۴۰۰

فهرست مطالب

۱ مقدمه

عنوان گزارش

طراحي مدارهاي تركيبي با استفاده از امكانات شماتيك.

موضوع

استفاده از نرم‌افزارهای طراحی به کمک کامپیوتر [۱] و امکانات شماتیک آن‌ها برای طراحی و پیاده‌سازی مدار ترکیبی.

شرح ابزارها و برنامه‌های مورد استفاده

در این آزمایش از نرم‌افزار ISE Desgin Suite که محصول شرکت Xilinx است استفاده کرده‌ام.

۲ چارچوب نظری و شرح آزمایش

در این آزمایش مداری برای کنترل ورود و خروج به اتاق طراحی کردیم. برای این کار از دو شمارنده استفاده کردیم. یکی برای نگه داشتن تعداد افراد حاضر در اتاق و دیگری برای نگه داشتن زمان باز ماندن در ورودی. به دلیل کوچک بودن مدار، این ماژول‌ها در خود ماژول اصلی آمده‌اند. تمامی کدها در ماژول اصلی Main.v وجود دارند.

۳ گزارش متنی

```
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.15 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.15 secs

--> Reading design: Main.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
```

[۱] CAD

```
37  ---- Source Parameters
38  Input File Name                    : "Main.prj"
39  Input Format                       : mixed
40  Ignore Synthesis Constraint File   : NO
41
42  ---- Target Parameters
43  Output File Name                   : "Main"
44  Output Format                      : NGC
45  Target Device                      : xc3sd3400a-4-fg676
46
47  ---- Source Options
48  Top Module Name                    : Main
49  Automatic FSM Extraction           : YES
50  FSM Encoding Algorithm             : Auto
51  Safe Implementation                : No
52  FSM Style                          : LUT
53  RAM Extraction                     : Yes
54  RAM Style                          : Auto
55  ROM Extraction                     : Yes
56  Mux Style                          : Auto
57  Decoder Extraction                 : YES
58  Priority Encoder Extraction        : Yes
59  Shift Register Extraction          : YES
60  Logical Shifter Extraction         : YES
61  XOR Collapsing                     : YES
62  ROM Style                          : Auto
63  Mux Extraction                     : Yes
64  Resource Sharing                   : YES
65  Asynchronous To Synchronous        : NO
66  Use DSP Block                      : Auto
67  Automatic Register Balancing       : No
68
69  ---- Target Options
70  Add IO Buffers                     : YES
71  Global Maximum Fanout              : 500
72  Add Generic Clock Buffer(BUFG)     : 24
73  Register Duplication               : YES
74  Slice Packing                      : YES
75  Optimize Instantiated Primitives   : NO
76  Use Clock Enable                   : Yes
77  Use Synchronous Set                : Yes
78  Use Synchronous Reset              : Yes
79  Pack IO Registers into IOBs        : Auto
80  Equivalent register Removal        : YES
81
82  ---- General Options
83  Optimization Goal                  : Speed
84  Optimization Effort                : 1
85  Keep Hierarchy                     : No
86  Netlist Hierarchy                  : As_Optimized
87  RTL Output                         : Yes
88  Global Optimization                : AllClockNets
89  Read Cores                         : YES
90  Write Timing Constraints           : NO
91  Cross Clock Analysis               : NO
92  Hierarchy Separator                : /
93  Bus Delimiter                      : <>
94  Case Specifier                     : Maintain
95  Slice Utilization Ratio            : 100
96  BRAM Utilization Ratio             : 100
97  DSP48 Utilization Ratio            : 100
98  Verilog 2001                       : YES
99  Auto BRAM Packing                  : NO
100 Slice Utilization Ratio Delta      : 5
101
102 =========================================================================
103
104
105 =========================================================================
106 *                          HDL Compilation                              *
107 =========================================================================
108 Compiling verilog file "Main.v" in library work
109 Module <Main> compiled
110 No errors in compilation
111 Analysis of file <"Main.prj"> succeeded.
112
113
114 =========================================================================
115 *                     Design Hierarchy Analysis                         *
116 =========================================================================
117 Analyzing hierarchy for module <Main> in library <work>.
118
119
120 =========================================================================
121 *                            HDL Analysis                               *
122 =========================================================================
123 Analyzing top module <Main>.
124 Module <Main> is correct for synthesis.
125
126
127 =========================================================================
```

```
*                        HDL Synthesis                        *
=============================================================================

Performing bidirectional port resolution...

Synthesizing Unit <Main>.
Related source file is "Main.v".
Found 1-bit register for signal <close>.
Found 1-bit register for signal <in>.
Found 1-bit register for signal <open>.
Found 1-bit register for signal <out>.
Found 1-bit register for signal <keepOpen>.
Found 4-bit up counter for signal <members>.
Found 4-bit addsub for signal <members$mux0000>.
Found 4-bit comparator less for signal <old_keepOpen_2$cmp_lt0000> created at
line 36.
Found 4-bit comparator greatequal for signal <open$cmp_ge0000> created at line
36.
Found 2-bit up counter for signal <waitOpen>.
Summary:
inferred   2 Counter(s).
inferred   5 D-type flip-flop(s).
inferred   1 Adder/Subtractor(s).
inferred   2 Comparator(s).
Unit <Main> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some
arithmetic operations in this design can share the same physical resources for
reduced device utilization. For improved clock frequency you may try to disable
resource sharing.

=============================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
4-bit addsub                                         : 1
# Counters                                             : 2
2-bit up counter                                     : 1
4-bit up counter                                     : 1
# Registers                                            : 5
1-bit register                                       : 5
# Comparators                                          : 2
4-bit comparator greatequal                          : 1
4-bit comparator less                                : 1

=============================================================================

=============================================================================
*                     Advanced HDL Synthesis                      *
=============================================================================


=============================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
4-bit addsub                                         : 1
# Counters                                             : 2
2-bit up counter                                     : 1
4-bit up counter                                     : 1
# Registers                                            : 5
Flip-Flops                                           : 5
# Comparators                                          : 2
4-bit comparator greatequal                          : 1
4-bit comparator less                                : 1

=============================================================================

=============================================================================
*                        Low Level Synthesis                      *
=============================================================================

Optimizing unit <Main> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Main, actual ratio is 0.

Final Macro Processing ...

=============================================================================
Final Register Report

Macro Statistics
# Registers                                            : 11
Flip-Flops                                           : 11

=============================================================================

```

```
219 ==========================================================================
220 *                          Partition Report                              *
221 ==========================================================================
222
223 Partition Implementation Status
224 -------------------------------
225
226 No Partitions were found in this design.
227
228 -------------------------------
229
230 ==========================================================================
231 *                          Final Report                                  *
232 ==========================================================================
233 Final Results
234 RTL Top Level Output File Name     : Main.ngr
235 Top Level Output File Name         : Main
236 Output Format                      : NGC
237 Optimization Goal                  : Speed
238 Keep Hierarchy                     : No
239
240 Design Statistics
241 # IOs                              : 7
242
243 Cell Usage :
244 # BELS                            : 21
245 #      INV                         : 2
246 #      LUT2                        : 3
247 #      LUT2_D                      : 1
248 #      LUT2_L                      : 1
249 #      LUT3                        : 1
250 #      LUT4                        : 9
251 #      LUT4_L                      : 1
252 #      MUXF5                       : 2
253 #      VCC                         : 1
254 # FlipFlops/Latches               : 11
255 #      FDE                         : 4
256 #      FDR                         : 4
257 #      FDRE                        : 3
258 # Clock Buffers                   : 1
259 #      BUFGP                       : 1
260 # IO Buffers                      : 6
261 #      IBUF                        : 2
262 #      OBUF                        : 4
263 ==========================================================================
264
265 Device utilization summary:
266 ---------------------------
267
268 Selected Device : 3sd3400afg676-4
269
270 Number of Slices:                       12  out of  23872     0%
271 Number of Slice Flip Flops:             11  out of  47744     0%
272 Number of 4 input LUTs:                 18  out of  47744     0%
273 Number of IOs:                          7
274 Number of bonded IOBs:                  7  out of    469     1%
275 Number of GCLKs:                        1  out of     24     4%
276
277 ---------------------------
278 Partition Resource Summary:
279 ---------------------------
280
281 No Partitions were found in this design.
282
283 ---------------------------
284
285
286 ==========================================================================
287 TIMING REPORT
288
289 NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
290 FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
291 GENERATED AFTER PLACE-and-ROUTE.
292
293 Clock Information:
294 ------------------
295 +------------------------------------+------------------------+-------+
296 | Clock Signal                       | Clock buffer(FF name)  | Load  |
297 +------------------------------------+------------------------+-------+
298 | clk                                | BUFGP                  | 11    |
299 +------------------------------------+------------------------+-------+
300
301 Asynchronous Control Signals Information:
302 ----------------------------------------
303 No asynchronous control signals found in this design
304
305 Timing Summary:
306 ---------------
307 Speed Grade: -4
308
309 Minimum period: 4.179ns (Maximum Frequency: 239.292MHz)
```

```
Minimum input arrival time before clock: 4.168ns
Maximum output required time after clock: 5.531ns
Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
Clock period: 4.179ns (frequency: 239.292MHz)
Total number of paths / destination ports: 82 / 21
-------------------------------------------------------------------------
Delay:               4.179ns (Levels of Logic = 2)
Source:            members_2 (FF)
Destination:       out (FF)
Source Clock:      clk rising
Destination Clock: clk rising

Data Path: members_2 to out
Gate     Net
Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
FDE:C->Q              8   0.591   0.900  members_2 (members_2)
LUT2_D:I0->LO         1   0.648   0.103  Mcount_members111 (N15)
LUT4:I3->O            1   0.648   0.420  out_or000011 (out_or0000)
FDR:R                     0.869          out
----------------------------------------
Total                     4.179ns (2.756ns logic, 1.423ns route)
(65.9% logic, 34.1% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
Total number of paths / destination ports: 22 / 12
-------------------------------------------------------------------------
Offset:              4.168ns (Levels of Logic = 3)
Source:            ent (PAD)
Destination:       members_0 (FF)
Destination Clock: clk rising

Data Path: ent to members_0
Gate     Net
Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
IBUF:I->O             3   0.849   0.674  ent_IBUF (ent_IBUF)
LUT4:I0->O            2   0.648   0.450  open_not00011 (open_not0001)
LUT4:I3->O            4   0.648   0.587  members_not00011 (members_not0001)
FDE:CE                    0.312          members_0
----------------------------------------
Total                     4.168ns (2.457ns logic, 1.711ns route)
(58.9% logic, 41.1% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
Total number of paths / destination ports: 4 / 4
-------------------------------------------------------------------------
Offset:              5.531ns (Levels of Logic = 1)
Source:            in (FF)
Destination:       in (PAD)
Source Clock:      clk rising

Data Path: in to in
Gate     Net
Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
FDR:C->Q              1   0.591   0.420  in (in_OBUF)
OBUF:I->O                 4.520          in_OBUF (in)
----------------------------------------
Total                     5.531ns (5.111ns logic, 0.420ns route)
(92.4% logic, 7.6% route)

=========================================================================


Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 4.45 secs

-->

Total memory usage is 4514000 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```

۴ فرکانس کاری مدار

همانطور که در خط ۳۲۳ گزارش متنی مشخص است، Delay مدار ۴/۱۷۹ نانو ثانیه است.

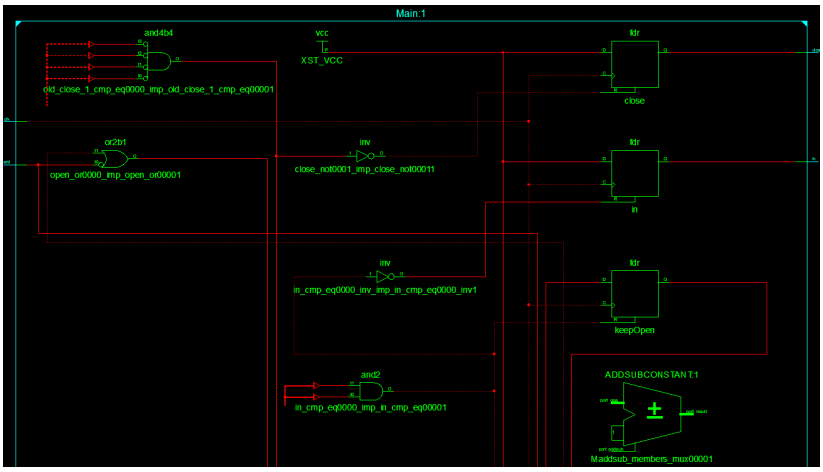
$$f = \frac{1}{4.179ns \times 10^{-9}} \approxeq 0.239 \times 10^{9} Hz = 239MHz$$

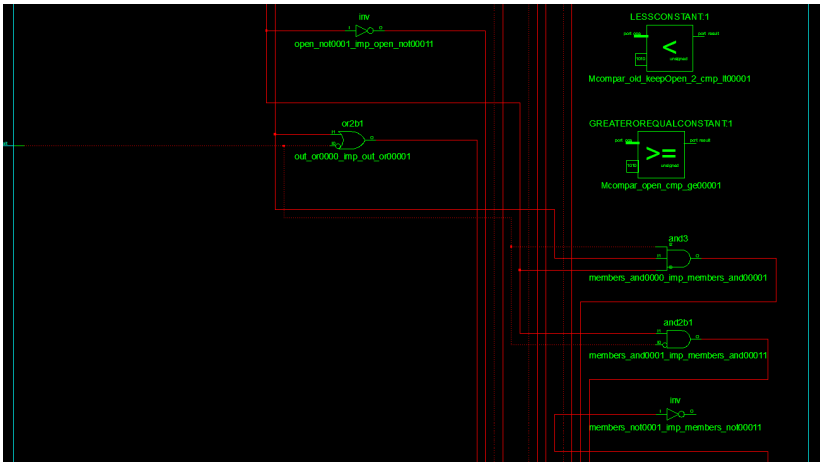
پس فرکانس کاری ۱۹۱ مگاهرتز است.

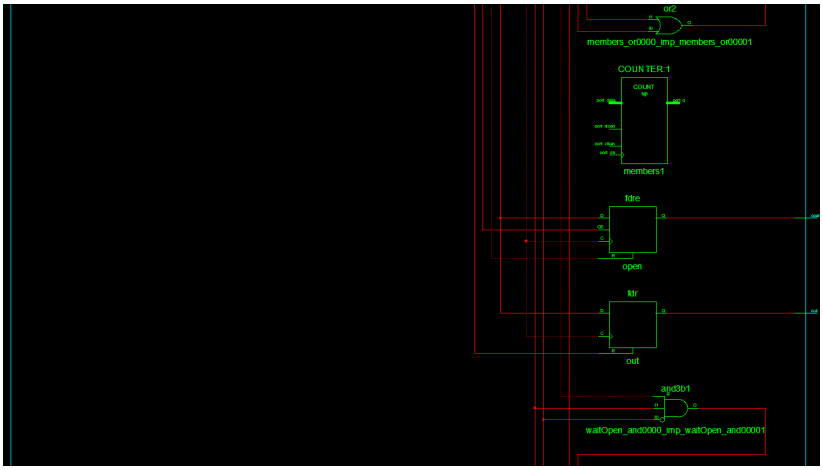
۵ تست مدار

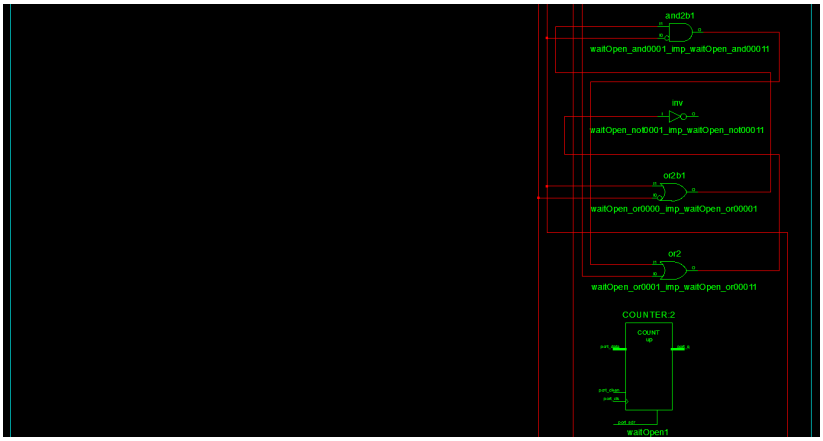
تستی برای بررسی صحت عملکرد مدار در فایل MainTest.v نوشته شده است که اتاق را پر میکند و همچین حالت‌های لبه‌ای (خروجی در صورت خالی بودن اتاق و ورود در صورت پر بودن اتاق) را هم چک می‌کند.

۶ شماتیک




inv
open_not0001_imp_open_not00011
LESSCONSTANT:1
Mcompar_old_keepOpen_2_cmp_lt00001
or2b1
out_or0000_imp_out_or00001
GREATEROREQUALCONSTANT:1
Mcompar_open_cmp_ge00001
and3
members_and0000_imp_members_and00001
and2b1
members_and0001_imp_members_and00011
inv
members_not0001_imp_members_not00011


or2
members_or0000_imp_members_or00001
COUNTER:1
members1
fdre
open
fdr
out
and3b1
waitOpen_and0000_imp_waitOpen_and00001


and2b1
waitOpen_and0001_imp_waitOpen_and00011
inv
waitOpen_not0001_imp_waitOpen_not00011
or2b1
waitOpen_or0000_imp_waitOpen_or00001
or2
waitOpen_or0001_imp_waitOpen_or00011
COUNTER:2
COUNT
UP
waitOpen1


_old_keepOpen_2_imp
_old_keepOpen_2_imp
Main