Shiraz University

Computer Aided Digital Systems Design

Third Assignment

Deadline: 31 December 2025 (10 Dey 1404)

1. Binary divisibility by 3 Construct, an FSM that checks if a binary number is divisible by 3. Specifically, your FSM should take the bits sequentially (i.e. one by one) starting from the LSB ,and output REM = 1 if the number is not divisible and REM = 0 if it is divisible. Do not try modulo statement in verilog, as it is not synthesizable. (Implement this problem in Mealy form.)

2. (a) Without using a DCM, write a module that takes an input clock and an arbitrary 8-bit number, and generates a clock enable (CE – Clock Enable) signal in such a way that, using this signal, another module can be operated at a speed from 1 to 256 times slower than the maximum possible speed (i.e., the case without CE, where the module is active on every clock cycle).

   Note: The clock of the target module is the same as the main system clock, and the use of a gated clock is not allowed.

   (b) Using the module from part (A), write a counter circuit with adjustable speed.

3. Design and implement a parameterized FIFO module using only two stack modules ,(`StackA` and `StackB`) that you must **instantiate** (do not implement a FIFO directly as a circular buffer and do not use FIFO/RAM IP cores).
   The FIFO must satisfy the following:

   (a) Data written first must be read first (FIFO order).

   (b) On a read request, if the output stack is empty, transfer data from the input stack to the output stack while preserving FIFO order.

   (c) All operations must be synchronous to the system clock.

   (d) Gated clocks are not allowed.

4. Design a controller for a smart application that uses a single mechanical push button.During the hardware testing following issues observed:

   (a) the button pin is asynchronous with respect to the system clock.

   (b) A single physical button press sometimes cause multiple state transitions

   (c) The controller enters unexpected states

   System Behavior:
   The controller operates using the following four states:

   (a) Reset :

      i. initial state after power-up when reset is asserted.

      ii. all outputs are deasserted

      iii. Automatically transition to Idle on the next rising edge

   (b) Idle :

      i. Appliance is off.

      ii. Waiting for a valid user button event.

   (c) Active :

      i. Appliances is on.

      ii. Remains active for exactly 10 clock cycles.

      iii. If user generates another button event during this state, the system transitions immediately to Error

   (d) Error :

      i. Appliances enters a fault condition.

      ii. Remains in this state until reset.

   Design Requirements :

   (a) The button input is asynchronous to clock .

   (b) All state transitions must be fully synchronous.

   (c) Avoid combinational loops and unintended latches.

   Tasks :

   (a) Design the FSM that meets the functional requirements.

   (b) Add any necessary input condition logic to ensure reliable operation.

   (c) Ensure that the FSM respond only to clean , clock-aligned button events.

   (d) Clearly comment your code to explain how asynchronous input issues are addressed.

Note: All answers must be submitted via Quera The deadline has not been extended.

Late Submission Policy:

Submitting one day late will result in a 25% grade reduction.
Submitting two days late will result in a 50% grade reduction.

Submissions beyond two days will not be accepted under any circumstances.

Deliverables:The following items must be submitted:

1. Verilog source codes
2. Testbench files
3. Documentation (report)

Note: In addition, the documentation must include the following screenshots taken directly from Xilinx Vivado:

1. Successful compilation/synthesis results
2. Simulation waveform results corresponding to the testbench
3. Any other relevant outputs demonstrating correct functionality

Notes:

1. All implementations, simulations, and results must be performed exclusively using Xilinx Vivado.
2. All screenshots must be captured from Vivado.
3. Submitting the assignment using any other software, simulator, or method will result in a grade deduction.

If you have any questions regarding the installation or usage of Xilinx Vivado, you are encouraged to ask for assistance.