Shiraz University

Computer Aided Digital Systems Design

Second Assignment

Deadline: 23 December 2025 (2 Dey 1404)

1. Write the Verilog code for the circuit below.

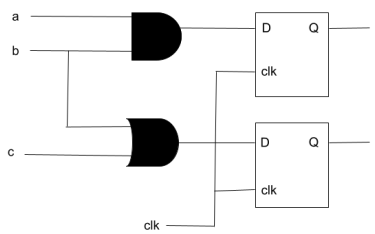
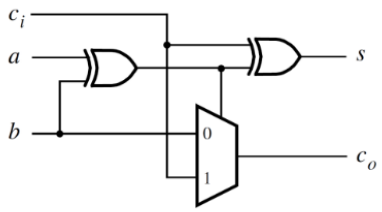
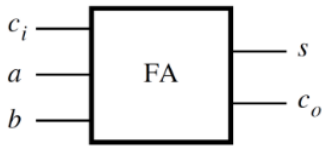


Figure 1

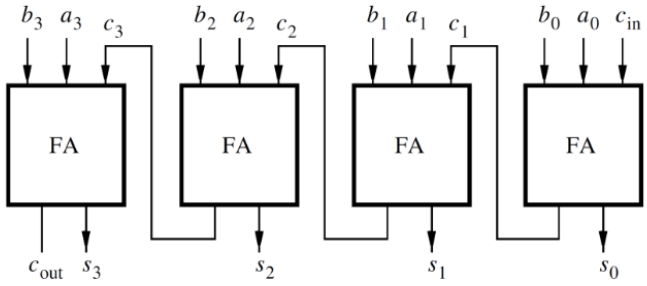
2. Fig. 2a shows a circuit for a *full adder*, which has the inputs a, b, and c_i, and produces the outputs s and c_o. Parts b and c of the figure show a circuit symbol and truth table for the full adder, which produces the two-bit binary sum $\{c_o, s\} = a + b + c_i$ (Note: in this expression, the + symbol means *addition*, as opposed to logical OR). Fig. 2c shows how four instances of this full adder module can be used to design a circuit that adds two four-bit numbers. This type of circuit is usually called a *ripple-carry* adder, because of the way that the carry signals are passed from one full adder to the next.



(a) Full adder circuit



(b) Full adder symbol



(c) Four-bit ripple-carry adder circuit

Figure 2: A ripple-carry adder circuit.

3. (a) Design a JK Flip-Flop module.
   (b) Using the JK Flip-Flop with the help of the diagram below, design a 4-bit up-counter.
   (c) Design an up-counter directly using an always block.
   (d) Compare the designs of the previous two parts in terms of RTL schematic and in terms of maximum clock speed and resource utilization on a desired chip produced by Xilinx

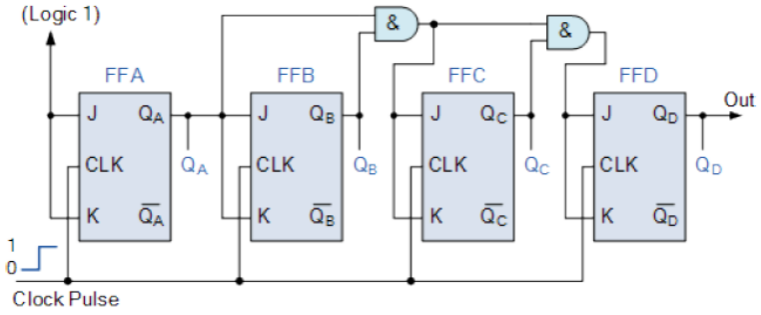


Figure 3: Counter With JK Flip-Flop

4. Consider the following FIR filter, described by the following equation:
   $Y(n) = a\,x(n) + b\,x(n\text{-}1) + c\,x(n\text{-}2)$
   For each of the following designs (a to c):

   1. Draw the proposed circuit manually on paper
   2. The corresponding Verilog code
   3. Simulation results in the form of the printed waveforms
   4. Determine the critical path on the architecture and find the maximum operating frequency
   5. The summary of the compilation report

   (a) The design with the lowest latency

   (b) The design with the highest throughput

   (c) The design with the lowest area (hint: resource sharing should be done)

Note: All answers must be submitted via Quera The deadline has not been extended.
Late Submission Policy:
Submitting one day late will result in a 25% grade reduction.
Submitting two days late will result in a 50% grade reduction.

Submissions beyond two days will not be accepted under any circumstances.

Required Software:
The required software for this assignment is Xilinx Vivado (Version 2020). The installation file can be obtained from Mr. Sargazi or Mr. Amin. Additionally, students may download Vivado from the following link if needed:

https://downloadly.ir/software/engineering-specialized/xilinx-vivado-design-suite/

Note: If students are unable to install Vivado on their personal systems, they may use the Digital Laboratory computers to complete the assignment.

Deliverables:The following items must be submitted:

1. Verilog source codes
2. Testbench files
3. Documentation (report)

Note: In addition, the documentation must include the following screenshots taken directly from Xilinx Vivado:

1. Successful compilation/synthesis results
2. Simulation waveform results corresponding to the testbench
3. Any other relevant outputs demonstrating correct functionality

Important Notes:

1. All implementations, simulations, and results must be performed exclusively using Xilinx Vivado.
2. All screenshots must be captured from Vivado.
3. Submitting the assignment using any other software, simulator, or method will result in a grade deduction.

If you have any questions regarding the installation or usage of Xilinx Vivado, you are encouraged to ask for assistance.