SOM Project Status (12/12/2018 - 21:37:59)			
Project File:	Parsa8.xise	**Parser Errors:**	No Errors
Module Name:	SOM	**Implementation State:**	Synthesized
Target Device:	xc7a100t-3csg324	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	No Warnings
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	97	126800	0%
Number of Slice LUTs	611	63400	0%
Number of fully used LUT-FF pairs	92	616	14%
Number of bonded IOBs	29	210	13%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	30	240	12%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed Dec 12 21:37:58 2018	0	0	9 Infos (9 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	Wed Dec 12 21:37:23 2018	

Date Generated: 12/12/2018 - 23:09:00