top_module Project Status (01/21/2019 - 04:28:23)			
Project File:	FSMD.xise	**Parser Errors:**	No Errors
Module Name:	top_module	**Implementation State:**	Synthesized
Target Device:	xc7a100t-3csg324	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	90 Warnings (0 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	289	126800	0%
Number of Slice LUTs	1766	63400	2%
Number of fully used LUT-FF pairs	209	1846	11%
Number of bonded IOBs	24	210	11%
Number of BUFG/BUFGCTRLs	2	32	6%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon Jan 21 04:28:22 2019	0	90 Warnings (0 new)	2 Infos (0 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	Mon Jan 21 04:02:27 2019	

Date Generated: 01/21/2019 - 04:28:23