Mem_Cntl Project Status (11/24/2018 - 19:13:23)			
Project File:	hw6_parsa.xise	**Parser Errors:**	No Errors
Module Name:	Mem_Cntl	**Implementation State:**	Synthesized
Target Device:	xc7a100t-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	15 Warnings (15 new)
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	5	126800	0%
Number of Slice LUTs	5	63400	0%
Number of fully used LUT-FF pairs	0	10	0%
Number of bonded IOBs	7	210	3%
Number of BUFG/BUFGCTRLs	1	32	3%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat Nov 24 19:13:21 2018	0	15 Warnings (15 new)	1 Info (1 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	Sat Nov 24 18:51:20 2018	

Date Generated: 11/24/2018 - 19:13:23