Question-1: Which of the following is true:

a) L1 serves as a cache for DRAM
b) L2 servers as a cache for DRAM
c) L3 serves as a cache for DRAM
d) DRAM serves as a cache for disk
e) All of the above
f) None of the above

Answer: e

Question-2: Which of these register(s) is/are used in transforming the logical address to virtual address?

A. PTBR
B. CS
C. SS
D. GDTR

a. All of the above
b. None of the above
c. A, B, and C
d. B, C, and D
e. A, B, and D

Answer: d.

Question-3: What is 90-10 rule all about?

a) 90% of the total number of processes running in any OS consumes only 10% of the memory
b) A process could access 90% of its code/data only during 10% of the execution time
c) All of the above
d) None of the above

Answer: b

Question-4: Which of these are designed in the processors to make use of 90-10 rule?

A. GDTR
B. PTBR
C. TLB
D. L3 cache

a. A, B, C
b. A, D
c. B, D
d. B, C
e. C, D

Answer: e

Question-5: How many bits are needed in a 128-bit VA to store the VPNs. Assume the page size to be 16KB.

a) 110
b) 114
c) 118
d) 128

Answer: b

Question-6: In 16-bit addressing mode, what will be the maximum size of a regular array-based page table? Assume page size and pointer size as 16 bytes and 4 bytes respectively.

a) 16Kb
b) 8Kb
c) 32Kb
d) 4Kb

Answer: a

Question-7: Which of the followings is/are true for two consecutive calls to pthread_create in a program?

a) Open file descriptors will be shared
b) Registers will be shared
c) Stack segment will be shared
d) Data segment will be shared
e) Heap segment will be shared
f) BSS segment will be shared
g) None of the above
h) a, b, c
i) a, c, d
j) a, c, d, e
k) a, d, e, f

Answer: k

Question-8: How many page faults will be there in LRU page replacement policy for the following stream of page access for a page table of size 2: Page-A, Page-B, Page-C, Page-D, Page-D, Page-B, Page-A, Page-B?

a) 5
b) 6
c) 4
d) 3
e) 7

Answer: b

Question 9: Which of the following APIs can be used to avoid deadlocks? (1 marks)

a) pthread_mutex_lock
b) pthread_mutex_timedlock
c) none of the above
d) both of them

Answer: b

Question 10: Which one of these statements is/are incorrect about x86 processors?

a) Paging can be used alone.
b) Segmentation can be used alone.
c) Paging and segmentation can be used together.
d) None of the above
e) All the above

Answer: a

Question 11: Arrange the following events in the order of occurrence when physical memory is full.

A. Page fault
B. Process moved to the ready queue
C. Context switch
D. Present bit invalid for a page in PT
E. LRU
F. Present bit valid for the page in PT

a) D-A-E-C-F-B
b) D-A-C-E-F-B
c) D-A-C-E-B-F
d) D-C-A-E-F-B

Answer: b

Question-12: Which of the followings is/are true?

a) TLB is most effective for programs with spatial locality
b) TLB is most effective for programs with temporal locality
c) None of the above

Answer: b

Question-13: How many lock objects are there in the standard implementation of dining philosopher's problem with 10 philosophers.

a) 5
b) 20
c) 10
d) None of the above

Answer: c

Question-14: What kind of locality is exploited in an iterative averaging program? Assume that outer loop iterates a single time:

a) Spatial
b) Temporal
c) All of the above
d) None of the above

Answer: a

Question-15: In the worst case, what will be the total memory allocation (size) used by the OS for maintaining the page table of a single process using a two-level page table approach? Assume pointer size and page size as 4 bytes and 4Kb respectively.

a) 4MB
b) More than 4MB
c) Greater than 2MB but less than 4MB
d) 2MB
e) None of the above

Answer: b

Question-16: Which one(s) of the following is/are true when there is large number of page faults due to demand paging:

a) Increased CPU utilization
b) Increased Disk utilization
c) Reduced memory utilization
d) Decreased number of context switches

Answer: b

Question-17: Which of these should be avoided for implementing a producer consumer multithreaded program:

a) Mutex
b) Semaphores
c) Condition variables
d) Try locking mutex

Answer: d

Question-18: Thread T1, T2, and T3 are running in parallel on separate cores. Each one of them has to randomly update one of the three shared resources Queue1, Queue2, and Queue3, only one at a time. How many mutex variables would be needed to avoid a race condition?

a) One
b) Two
c) Three
d) Zero

Answer: c