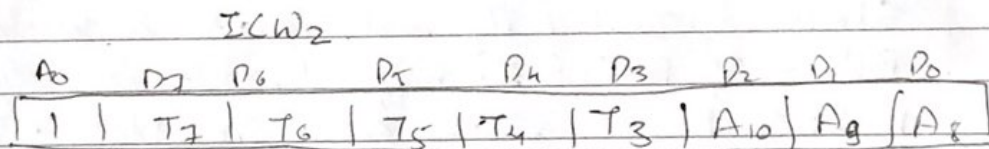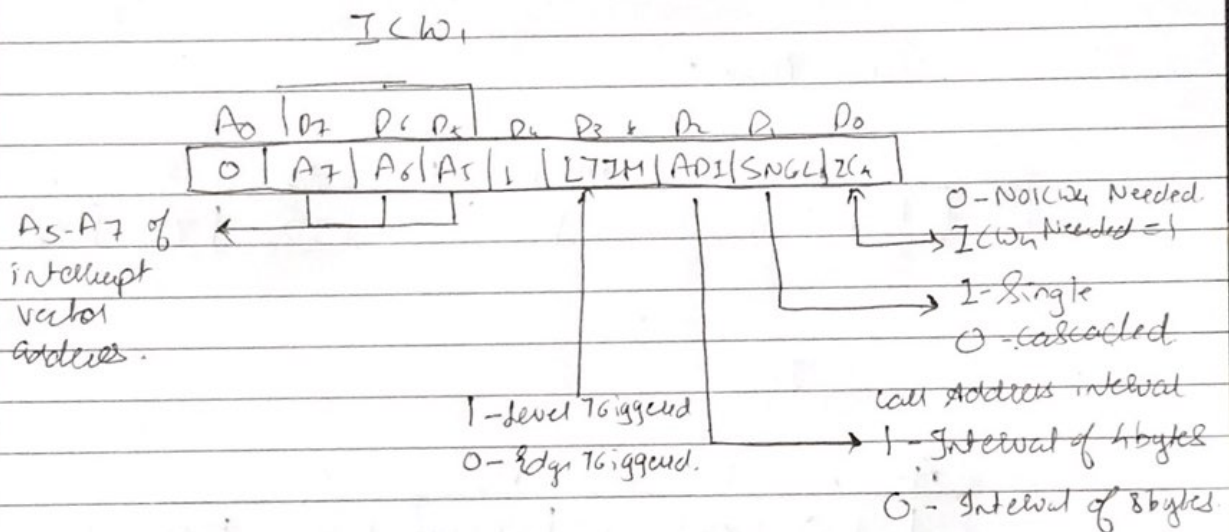## Term Test-2 MP

Q1] Initialization Command Words:

- 8259A must be initialized by writing two or four command words into the respective word registers namely ICW₁, ICW₂, ICW₃, & ICW₁, ICW₂, ICW₃, and ICW₄.

ICW_1

A₅-A₇ of interrupt vector address.

0 - NO ICW₄ Needed.
→ ICW₄ Needed =1

1 - Single
0 - Cascaded

1 - Level Triggered
0 - Edge Triggered.

call address interval
1 - Interval of 4 bytes
0 - Interval of 8 bytes

ICW_2

A₈, A₉, A₁₀ - For 8085, they are same as respective bits of vector address. And for 8086, they are 0.

T₃-T₇ - For 8085, they are filled with interrupt vector address of A₁₁-A₁₅. And for 8086, they are filled by most significant 5 bits of interrupt type.

ICW₃

Master Mode.

A₀	D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
1	S₇	S₆	S₅	S₄	S₃	S₂	S₁	S₀

Slave Mode:

A₀	D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
1	0	0	0	0	0	ID₂	ID₁	ID₀

ICW₄

A₀	D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
1	0	0	0	0	SFNM	BUF	M/S	AEOI	μPM

SFNM - Special fully nested mode is selected, if SFNM=1.

BUF - If BUF=1, the buffered mode is selected.

M/S: If M/S=1, 8259A is a master, else slave.

AEOI: If AEOI =1, the automatic end of interrupt mode is selected.

μPM: If the μPM bit is 0, the MCS-85 System operation is selected else 8086/8088 is selected.

Q2] **i]** EPROM:

Required = 64KB

Available = 32KB.

∴ No. of chips required = $\dfrac{\text{Required}}{\text{Available}}$ = $\dfrac{64\,KB}{32\,KB}$ = 2 chips

Also, 64KB = 0FFFF H.

∴ Starting address of EPROM = Ending address - Required

$$= FFFFF - 0FFFFH$$

$$= F0000\ H.$$

No. of address lines = 32KB = $2^5 \times 2^{10}B = 2^{15}$

= 15 address lines.

A_0 is a dedicated dedicated for odd/even bank Selection.

∴ Selecting $A_1 - A_{15}$ for EPROM.

∴ EPROM 1 is from F0000H to FFFFEH.

EPROM 2 is from F0001H to FFFFFH.

ii] RAM:

Required = 128KB

Available = 64KB

No. of chips required = $\dfrac{\text{Required}}{\text{Available}}$ = $\dfrac{128\,KB}{64\,KB}$ = 2 chips

No. of address lines $= 64 kB = 2^{16} = 16$ address lines

A_0 is dedicated for odd/even bank selection

$\therefore A_1 - A_{16}$ is connected to each RAM.

Starting Address from RAM = 00000 H -
RAM1 is from 00000 H - 1FFFE H.
RAM2 is from 00001 H - 1FFFF H.

Address Map:

	Address	A_{19} A_{18} A_{17} A_{16}	A_{15} A_{14} A_{13} A_{12}	A_{11} A_{10} A_9 A_8	A_7 A_6 A_5 A_4	A_3 A_2 A_1 A_0
RAM	00000 H	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
	1FFFF H	0 0 0 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1
EPROM	F0000 H	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
	FFFFF H	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Interfacing.

A_{16} —
$\vdots$
A_{19} — ⊃— ⓒ

A_{17} —
$\vdots$
A_{19} — ⊃— ⓒ'

ⓒ — ⊃— $\overline{CS_1}$

$\overline{BHE}$ —

$\overline{CS_3}$
64KB
RAM
(HB)

$A_1 - A_{16}$

$\overline{CS_4}$
64KB
RAM
(LB)

$\overline{MEMWR} \rightarrow \overline{WR}$
$\overline{MEMRD} \rightarrow \overline{RD}$

$\overline{MEMWR} \rightarrow \overline{WR}$
$\overline{MEMRD} \rightarrow \overline{RD}$

$D_8 - D_{15}$

$D_0 - D_7$

$D_0 - D_{15}$

$D_8 - D_{15}$

$D_0 - D_7$

ⓒ — ⊃— $\overline{CS_2}$
Ⓐ0 —

EPROM
32 KB
(HB)

$A_1 - A_{15}$

EPROM
32 KB
(LB)

ⓒ' — ⊃— $\overline{CS_4}$
Ⓐ0 —

$\overline{OE}$

$\overline{CS_1}$

$\overline{MEMRD}$

$\overline{OE}$

$\overline{CS_2}$

$\overline{MEMRD}$

$\overline{CS_1}$

ⓒ' — ⊃— $\overline{CS_3}$
$\overline{BHE}$ —
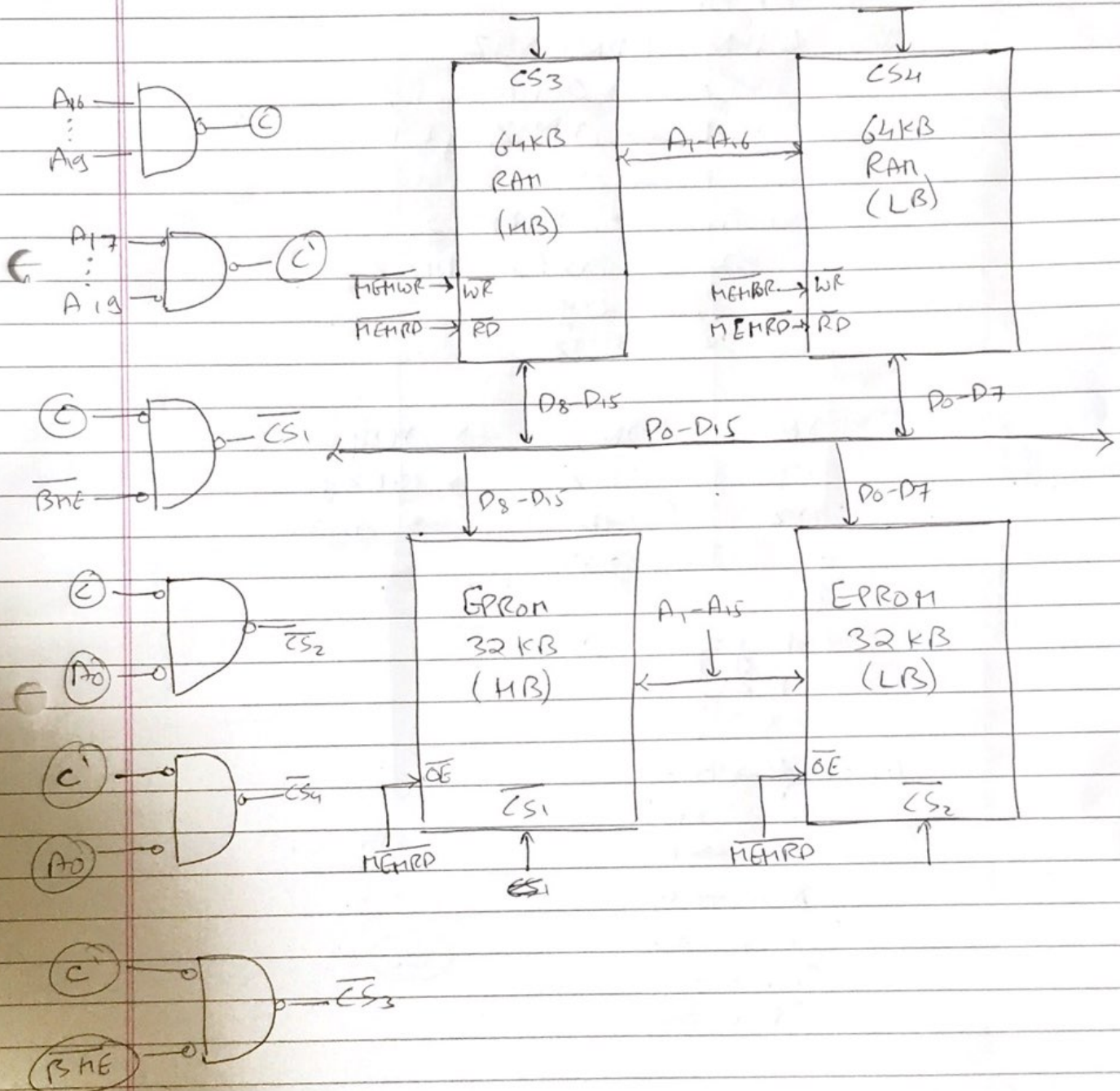
Q3] Real Mode	Protected Mode	Virtual Mode
1) Maximum memory accessible is 16 bytes (1MB + 64kB)	1] Maximum memory accessible is 4GB	1] Memory accessible is entire 4GB
2] Only one task can be executed at any given instant.	2] Multiple tasks can be executed Simultaneously	2] Only one task can be executed at any given instant.
3] Switching between real and protected mode requires complicated process.	3] Switching with virtual mode is easier compared to real mode.	3] Switching between virtual and protected mode is easy compared to that of real mode.
4] Memory addressing is similar to that of 8086	4] Memory addressing is done using descriptors and selectors	4] Memory accessing virtually seems to be similar to 8086.