ECE 506 – Architecture of Parallel Computers
Machine Problem II - Coherence Protocols
Due Date: 5th November, 2015

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The results obtained after running the cache coherence protocol simulator on various cache configurations are presented in the following section. After presenting the results, suitable graphs are plotted to illustrate the effects of changing various cache parameters on performance.

1. Varying Cache Size, with Cache Associativity and Cache Block Size fixed

Cache Sizes: 256KB, 512KB, 1MB, 2MB
Cache Associativity: 8
Block Size: 64B
Number of Processors: 4
Trace File: trace/canneal/longTrace

a) MSI Protocol

Configuration: 256 KB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5775	5805	5771	5813
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.67%	4.77%	4.57%	4.66%
6	Writebacks to Memory	254	235	278	234
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6745	6740	6774	6761
9	Interventions	68	47	81	63
10	Invalidations	2014	2034	2008	2020
11	Flushes	113	92	120	88
12	BusRdX issued	716	700	725	714

Configuration: 512 KB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5757	5792	5756	5796
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.76%	4.55%	4.65%
6	Writebacks to Memory	190	170	205	171
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6663	6662	6686	6681
9	Interventions	71	47	82	63
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	92	121	88
12	BusRdX issued	716	700	725	714

Configuration: 1 MB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5752	5781	5752	5796
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.65%
6	Writebacks to Memory	170	155	186	171
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6638	6636	6663	6661
9	Interventions	71	48	82	2020
10	Invalidations	2014	2034	2008	88
11	Flushes	116	93	121	714
12	BusRdX issued	716	700	725	714

Configuration: 2 MB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5750	5779	5751	5789
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks to Memory	166	143	176	152
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6632	6622	6652	6655
9	Interventions	71	48	82	64
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX issued	716	700	725	714

b) MESI Protocol

Configuration: 256 KB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5775	5805	5771	5813
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.67%	4.77%	4.57%	4.66%
6	Writebacks to Memory	254	235	278	234
7	Cache-to-Cache Transfers	4405	4441	4406	4411
8	Memory Transaction	1663	1640	1685	1675
9	Interventions	1468	1432	1469	1479
10	Invalidations	2014	2034	2008	2020
11	Flushes	113	92	120	88
12	BusRdX issued	39	41	42	39

Configuration: 512 KB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5757	5792	5756	5796
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.76%	4.55%	4.65%
6	Writebacks to Memory	190	170	205	171
7	Cache-to-Cache Transfers	4392	4431	4396	4400
8	Memory Transaction	1594	1572	1607	1606
9	Interventions	1466	1429	1465	1474
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	92	121	88
12	BusRdX issued	39	41	42	39

Configuration: 1 MB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5752	5781	5752	5790
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks to Memory	170	155	186	157
7	Cache-to-Cache Transfers	4389	4422	4393	4395
8	Memory Transaction	1572	1555	1587	1591
9	Interventions	1464	1428	1464	1474
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX issued	39	41	42	39

Configuration: 2 MB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5750	5779	5751	5789
3	Number of Writes	11942	11710	12383	12108

4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks to Memory	166	143	176	152
7	Cache-to-Cache Transfers	4387	4420	4392	4394
8	Memory Transaction	1586	1543	1577	1586
9	Interventions	1464	1428	1464	1474
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX issued	39	41	42	39

c) Dragon

Configuration: 256 KB, 8, 64B

Sr. No.	**Statistics**	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5635	5646	5644	5652
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	3	2	2	0
5	Total Miss Rate	4.52%	4.61%	4.43%	4.50%
6	Writebacks to Memory	226	243	232	234
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5864	5891	5878	5886
9	Interventions	1405	1396	1398	1430
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	9
12	BusRdX issued	0	0	0	0

Configuration: 512 KB, 8, 64B

Sr. No.	**Statistics**	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5601	5610	5610	5617
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	3	2	2	0
5	Total Miss Rate	4.50%	4.58%	4.41%	4.47%

6	Writebacks to Memory	128	127	135	141
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5732	5739	5747	5758
9	Interventions	1400	1388	1389	1418
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX issued	0	0	0	0

Configuration: 1 MB, 8, 64B

Sr. No.	**Statistics**	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5595	5604	5604	5611
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	3	2	2	0
5	Total Miss Rate	4.49%	4.57%	4.40%	4.47%
6	Writebacks to Memory	107	110	105	123
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5705	5716	5711	5734
9	Interventions	1398	1387	1387	1417
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX issued	0	0	0	0

Configuration: 2 MB, 8, 64B

Sr. No.	**Statistics**	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5591	5603	5601	5608
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	3	2	2	0
5	Total Miss Rate	4.49%	4.57%	4.40%	4.47%
6	Writebacks to Memory	102	105	98	121
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5696	5710	5701	5729
9	Interventions	1396	1387	1387	1416
10	Invalidations	0	0	0	0

11	Flushes	3	9	6	6
12	BusRdX issued	0	0	0	0

2. Varying Cache Associativity, with Cache Size and Block Size fixed

Cache Size: 1MB
Cache Associativity: 4-way, 8-way, 16-way
Block Size: 64B
Number of Processors: 4
Trace File: trace/canneal/longTrace

a) MSI

Configuration: 1MB, 4-Way, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5768	5797	5762	5803
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.66%	4.76%	4.56%	4.65%
6	Writebacks to Memory	239	211	239	224
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6723	6708	6726	6741
9	Interventions	69	47	81	63
10	Invalidations	2014	2034	2008	2020
11	Flushes	114	92	120	88
12	BusRdX issued	716	700	725	714

Configuration: 1MB, 8-Way, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5752	5781	5752	5790
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks to Memory	170	155	186	157
7	Cache-to-Cache Transfers	0	0	0	0

8	Memory Transaction	6638	6636	6663	6661
9	Interventions	71	48	82	64
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX issued	716	700	725	714

Configuration: 1MB, 16-Way, 64B

Sr. No.	**Statistics**	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5741	5772	5741	5780
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.64%	4.74%	4.54%	4.64%
6	Writebacks to Memory	120	101	130	98
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6577	6573	6596	6592
9	Interventions	71	48	83	64
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	122	89
12	BusRdX issued	716	700	725	714

b) MESI

Configuration: 1MB, 4-Way, 64B

Sr. No.	**Statistics**	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5768	5797	5762	5803
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.66%	4.76%	4.56%	4.65%
6	Writebacks to Memory	239	211	239	224
7	Cache-to-Cache Transfers	4402	4434	4401	4401
8	Memory Transaction	1644	1615	1642	1665
9	Interventions	1465	1431	1465	1480
10	Invalidations	2014	2034	2008	2020

11	Flushes	114	92	120	88
12	BusRdX issued	39	41	42	39

Configuration: 1MB, 8-Way, 64B

Sr. No.	**Statistics**	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5752	5781	5752	5790
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks to Memory	170	155	186	157
7	Cache-to-Cache Transfers	4389	4422	4393	4395
8	Memory Transaction	1572	1555	1587	1591
9	Interventions	1464	1428	1464	1474
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX issued	39	41	42	39

Configuration: 1MB, 16-Way, 64B

Sr. No.	**Statistics**	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5741	5772	5741	5780
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.64%	4.74%	4.54%	4.64%
6	Writebacks to Memory	120	101	130	98
7	Cache-to-Cache Transfers	4379	4415	4386	4386
8	Memory Transaction	1521	1499	1527	1531
9	Interventions	1463	1426	1461	1473
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	122	89
12	BusRdX issued	39	41	42	39

c) Dragon

Configuration: 1MB, 4-Way, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5609	5619	5619	5626
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	3	2	2	0
5	Total Miss Rate	4.50%	4.59%	4.41%	4.48%
6	Writebacks to Memory	148	149	142	158
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5760	5770	5763	5784
9	Interventions	1400	1392	1388	1424
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX issued	0	0	0	0

Configuration: 1MB, 8-Way, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5595	5604	5604	5611
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	3	2	2	0
5	Total Miss Rate	4.49%	4.57%	4.40%	4.47%
6	Writebacks to Memory	107	110	105	123
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5705	5716	5711	5734
9	Interventions	1398	1387	1387	1417
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX issued	0	0	0	0

Configuration: 1MB, 16-Way, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5576	5586	5586	5593
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	3	2	2	0
5	Total Miss Rate	4.48%	4.56%	4.39%	4.46%
6	Writebacks to Memory	47	43	62	57
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5626	5631	5650	5650
9	Interventions	1395	1382	1383	1411
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX issued	0	0	0	0

3. Varying Block Size, with Cache Size and Cache Associativity fixed

Cache Size: 1MB
Cache Associativity: 8-Way
Block Size: 64B, 128B, 256B
Number of Processors: 4
TraceFile: trace/canneal/longTrace

a) MSI

Configuration: 1MB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5752	5781	5752	5790
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks to Memory	170	155	186	157
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6638	6636	6663	6661
9	Interventions	71	48	82	64

10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX issued	716	700	725	714

Configuration: 1MB, 8, 128B

Sr. No.	**Statistics**	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5340	5386	5341	5384
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	40	42	39
5	Total Miss Rate	4.32%	4.43%	4.23%	4.32%
6	Writebacks to Memory	275	250	283	269
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6344	6347	6369	6386
9	Interventions	119	84	127	110
10	Invalidations	2066	2089	2053	2068
11	Flushes	164	129	166	135
12	BusRdX issued	729	711	745	733

Configuration: 1MB, 8, 256B

Sr. No.	**Statistics**	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5023	5070	5004	5084
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	40	42	39
5	Total Miss Rate	4.06%	4.17%	3.96%	4.08%
6	Writebacks to Memory	363	342	383	332
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6137	6147	6167	6159
9	Interventions	166	133	192	145
10	Invalidations	2132	2157	2107	2148
11	Flushes	211	178	231	170
12	BusRdX issued	751	735	780	743

b) MESI

Configuration: 1MB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5752	5781	5752	5790
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks to Memory	170	155	186	157
7	Cache-to-Cache Transfers	4389	4422	4393	4395
8	Memory Transaction	1572	1555	1587	1591
9	Interventions	1464	1428	1464	1474
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX issued	39	41	42	39

Configuration: 1MB, 8, 128B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5340	5386	5341	5384
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	3900.00%	4000.00%	4200.00%	3900.00%
5	Total Miss Rate	4.32%	4.43%	4.23%	4.32%
6	Writebacks to Memory	275	250	283	269
7	Cache-to-Cache Transfers	4124	4155	4115	4125
8	Memory Transaction	1530	1521	1551	1567
9	Interventions	1367	1337	1377	1385
10	Invalidations	2066	2089	2053	2068
11	Flushes	164	129	166	135
12	BusRdX issued	39	40	42	39

Configuration: 1MB, 8, 256B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5023	5070	5004	5084
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	3900.00%	4000.00%	4200.00%	3900.00%
5	Total Miss Rate	4.06%	4.17%	3.96%	4.08%
6	Writebacks to Memory	363	342	383	332
7	Cache-to-Cache Transfers	3938	3943	3903	3939
8	Memory Transaction	1487	1509	1526	1516
9	Interventions	1283	1284	1321	1309
10	Invalidations	2132	2157	2107	2148
11	Flushes	211	178	231	170
12	BusRdX issued	39	40	42	39

c) Dragon

Configuration: 1MB, 8, 64B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5595	5604	5604	5611
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	3	2	2	0
5	Total Miss Rate	4.49%	4.57%	4.40%	4.47%
6	Writebacks to Memory	107	110	105	123
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5705	5716	5711	5734
9	Interventions	1398	1387	1387	1417
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX issued	0	0	0	0

Configuration: 1MB, 8, 128B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	5069	5080	5080	5086
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	300.00%	100.00%	200.00%	0.00%
5	Total Miss Rate	4.07%	4.15%	3.99%	4.05%
6	Writebacks to Memory	145	149	145	160
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5217	5230	5227	5246
9	Interventions	1256	1266	1257	1287
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	9
12	BusRdX issued	0	0	0	0

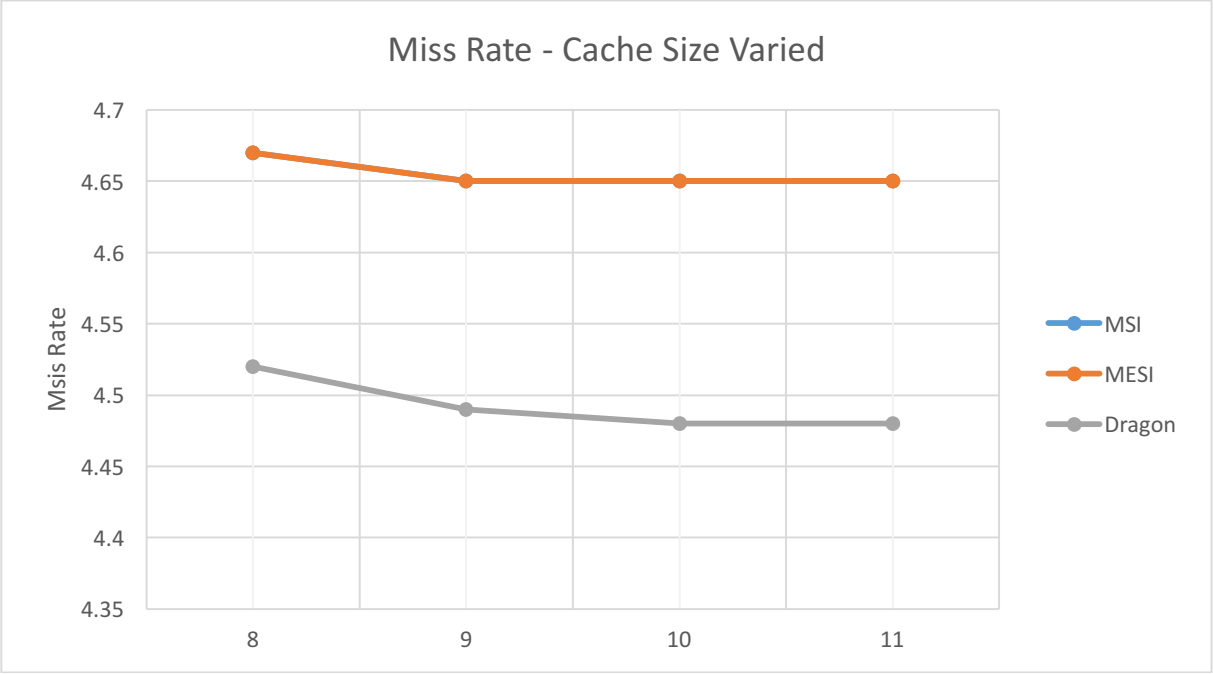
Configuration: 1MB, 8, 256B

Sr. No.	Statistics	0	1	2	3
1	Number of Reads	112661	110830	114938	113428
2	Number of Read Misses	4628	4633	4630	4640
3	Number of Writes	11942	11710	12383	12108
4	Number of Write Misses	300.00%	100.00%	200.00%	0.00%
5	Total Miss Rate	3.72%	3.78%	3.64%	3.70%
6	Writebacks to Memory	198	200	185	196
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	4829	4834	4817	4836
9	Interventions	1125	1175	1143	1176
10	Invalidations	0	0	0	0
11	Flushes	3	11	9	9
12	BusRdX issued	0	0	0	0

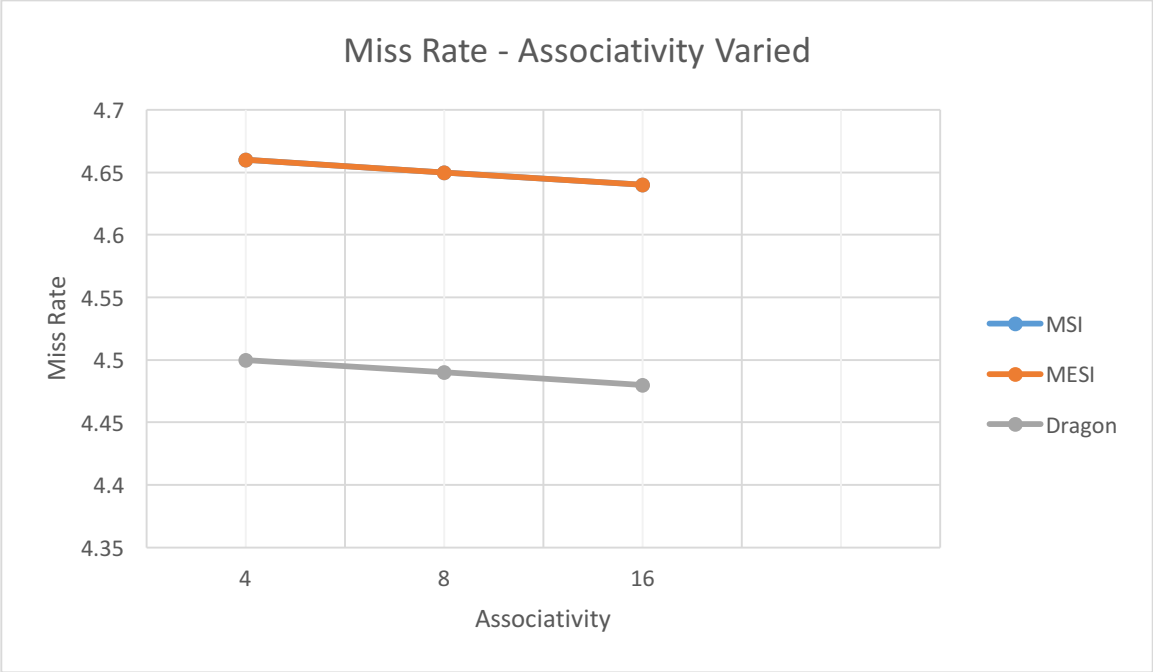
Analysis of Trends Observed:

I. Miss Rate

The miss rate for MSI, MESI and Dragon protocols is plotted against log2(cache size). The miss rate is the average of the miss rates for the 4 processor caches.



Here, the average miss rate is plotted against the associativity. Cache size and block size is kept fixed.



The block size is varied, while the cache size and associativity is kept constant. The miss rate is plotted against log2(block size).

Trends in Miss Rate:

Looking at the miss rate values observed in the graphs, we can see that the miss rate for Dragon protocol is lesser than that of MSI and MESI protocols. This observation is due the fact that Dragon is a write-update protocol, whereas the other two protocols are write-invalidate protocols. In Dragon, the caches have an updated value of the block and therefore suffer lesser number of misses.

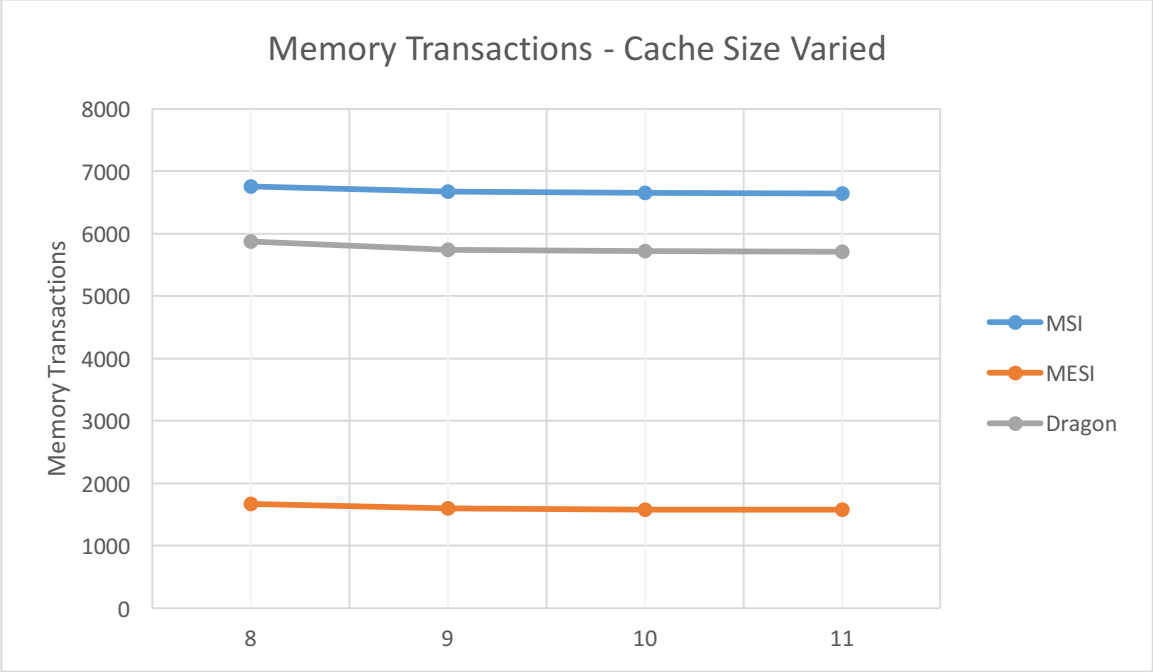
Looking at the varying cache size graph, the miss rate follows a decreasing trend with increasing cache size. As cache size is increased, the number of capacity misses decrease for same block size and associativity. This shows up in an overall decrease in the miss rate.

Miss rate also shows a decreasing trend with increasing cache associativity. Conflict misses in the cache decrease with an increase in associativity. This manifests in an overall decrease in the miss rate for multiprocessor systems as well.

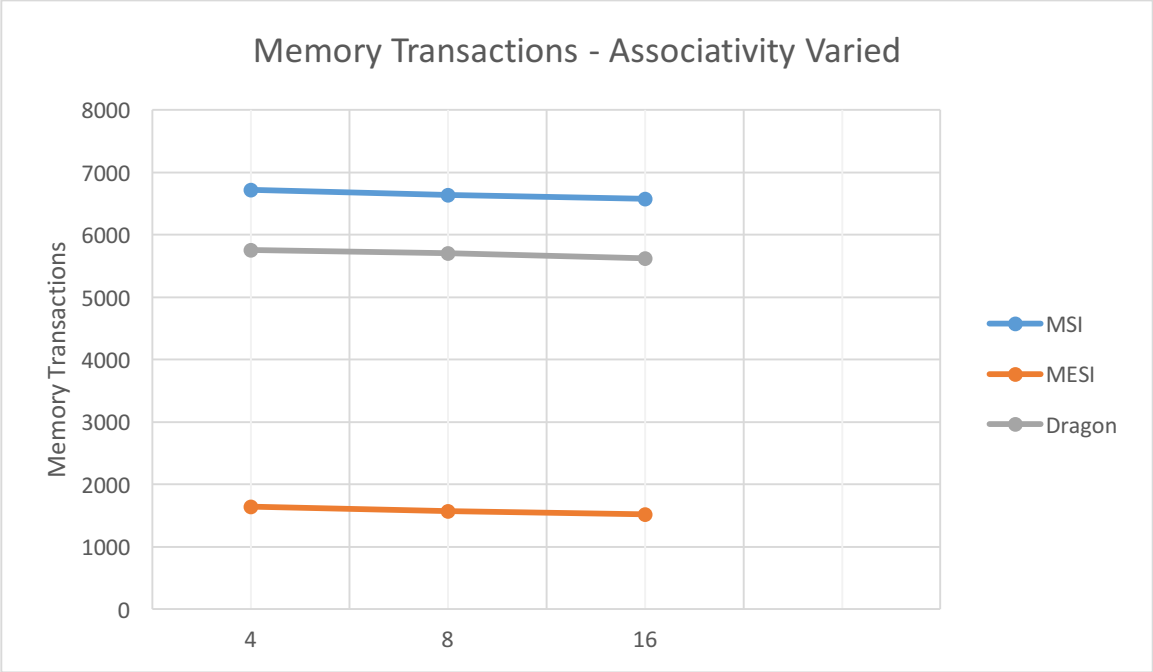
With an increase in block size, the number of compulsory misses are reduced since more number of data bytes are brought into the cache when a single cache block is fetched. This trend also continues for symmetric multiprocessor systems. Especially in the Dragon protocol, once a cache block is brought in, it stays in the cache until it is evicted; thus, a larger block size leads to a sharper decrease in the miss rate.

II. Memory Transactions

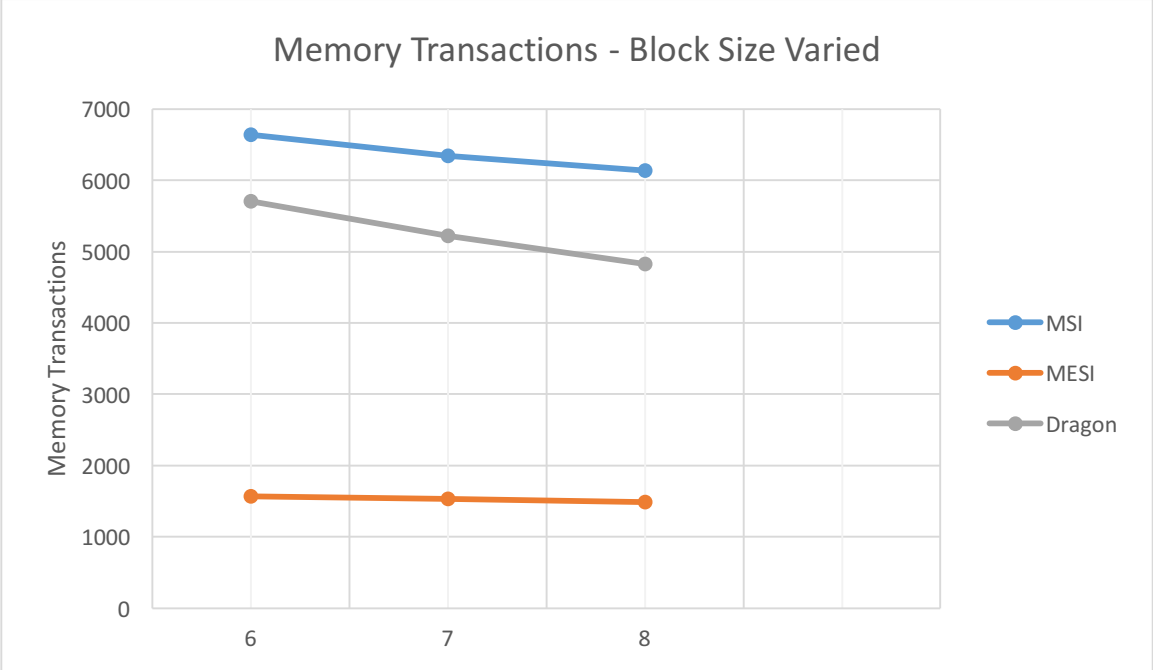
The miss rate for MSI, MESI and Dragon protocols is plotted against log2(cache size). The miss rate is the average of the miss rates for the 4 processor caches. Cache associativity and block size is kept constant in this plot.



Cache associativity is varied, while block size and cache size is kept fixed.



The cache block size is varied, keeping the associativity and total size the same.



Trends in Number of Memory Transactions:

The number of memory transactions is an important performance parameter, since memory access takes up a lot of latency. Reducing the number of memory accesses reduces the average access time for a cache configuration.

In MSI protocol, the number of memory transactions is much greater than the corresponding number for MESI and Dragon. This is because MSI accesses memory every time there is a Bus transaction request. Particularly, MSI accesses in the case of a read-write access in a sequential program, which leads to high latency.

MESI has the least number of memory transactions among the three protocols because cache-to-cache transfers are possible in MESI. Dragon does not allow cache-to-cache transfers, and thus the memory is accessed for every PrRd even if the block is present in other caches. Also, the number of memory generally decreases with increasing cache size, associativity or block size because the miss rate goes down; since there are a fewer number of misses, fewer memory accesses are required.

Trends in Number of Interventions:

From the obtained data, we observe that the number of interventions in MESI are much greater than MSI, whereas the number of interventions in Dragon are similar to that in MESI.
In MESI protocol, there are two states (M and E) from which we can downgrade to Shared. Whenever a cache block is exclusively present in one cache, the block is placed in Exclusive state. Since there is no E state in MSI protocol, all clean blocks are placed in Shared state. As a result, all downgrades from M->S and from E->S are counted in interventions As a result, observed in MESI are more than MSI.
In Dragon protocol, downgrades from either M or E to Sm or Sc are considered as interventions. Therefore, we observe larger number of interventions in Dragon protocol compared to MSI protocol.

Trends in Number of Invalidations:

Dragon protocol is a write-update protocol, and therefore there are no invalidations in Dragon.
From the data, we observe that the number of invalidations in MSI and MESI are exactly the same. This is quite expected since for a PrWr, all other cache blocks are invalidated in both MSI and MESI protocols. Thus, the number of invalidations for the same address trace will be exactly the same.

Trends in Number of Flushes:

In MSI and MESI, whenever we make transition from Modified state to either Shared or Invalid state, we Flush the block. Since these transitions are the same in both these protocols, we observe the same number of flushes.
In the case of Dragon protocol, a BusUpdate signal is also present along with Flush. Due to updates, Flushes are issued only for the transition from Modified to Sm state. Thus, very few number of Flushes are observed in Dragon protocol.

Trends in Number of BusRdX:

The number of BusRdX in MSI is much larger than MESI. This can be explained by the fact that there is no BusUpgr transaction in the MSI protocol; as a result, a BusRdX is issued even when we just want to invalidate the block in other caches. This also adds to the overall latency in MSI protocol. Presence of BusUpgr reduces the number of BusRdX issued in MESI protocol.

Since Dragon is write-update protocol, there is no BusRdX signal in Dragon. The protocol directly updates the copies of the block present in other caches rather than invalidating it whenever there is a write to the block.