Instruction set architecture

•All instructions are 30-bit wide (but padded with 2 trailing zeroes)

•Three instruction formats: R-type, I-type, and J-type

•There are 32 general purpose registers that are 32-bit wide

Instruction formats:

R-type Instructions:

Opcode	Rs	Rt	Rd	Reserved
4 bits	5 bits	5 bits	5 bits	11 bits

I-type Instructions:

Opcode	Rs	Rt	Immediate
4 bits	5 bits	5 bits	16 bits

J-type Instructions:

Opcode	Address
4 bits	26 bits

•Op^{4}: 4-bit opcode of the instruction

•Rs^{5}, Rt^{5}, Rd^{5}: 5-bit source and destination register numbers

•$Immediate^{16}$: 16-bit immediate constant or PC-relative offset

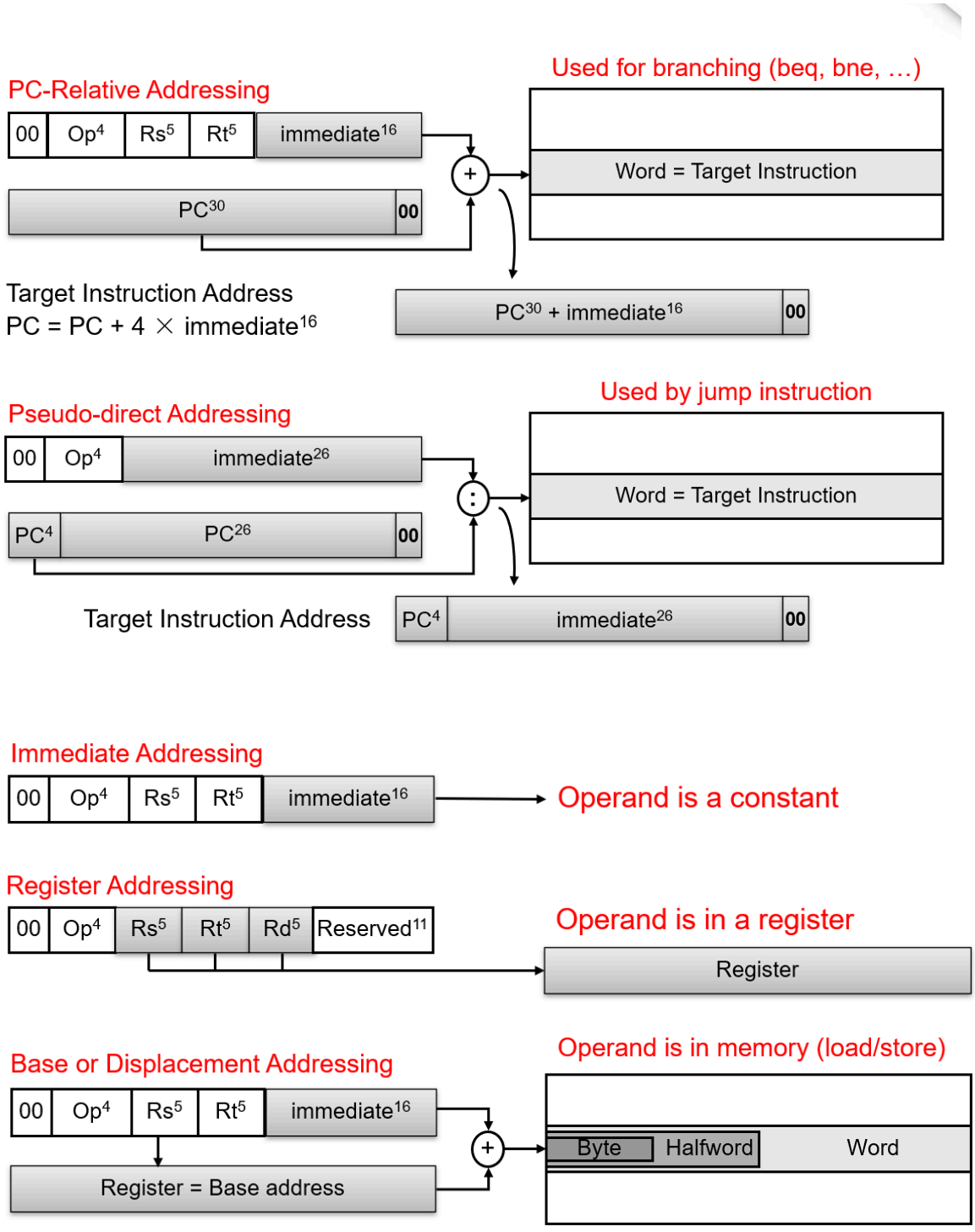
•$Address^{26}$: 26-bit target address of the jump instruction

•R-type instructions have a 11-bit reserved field that can be used for additional functionality.

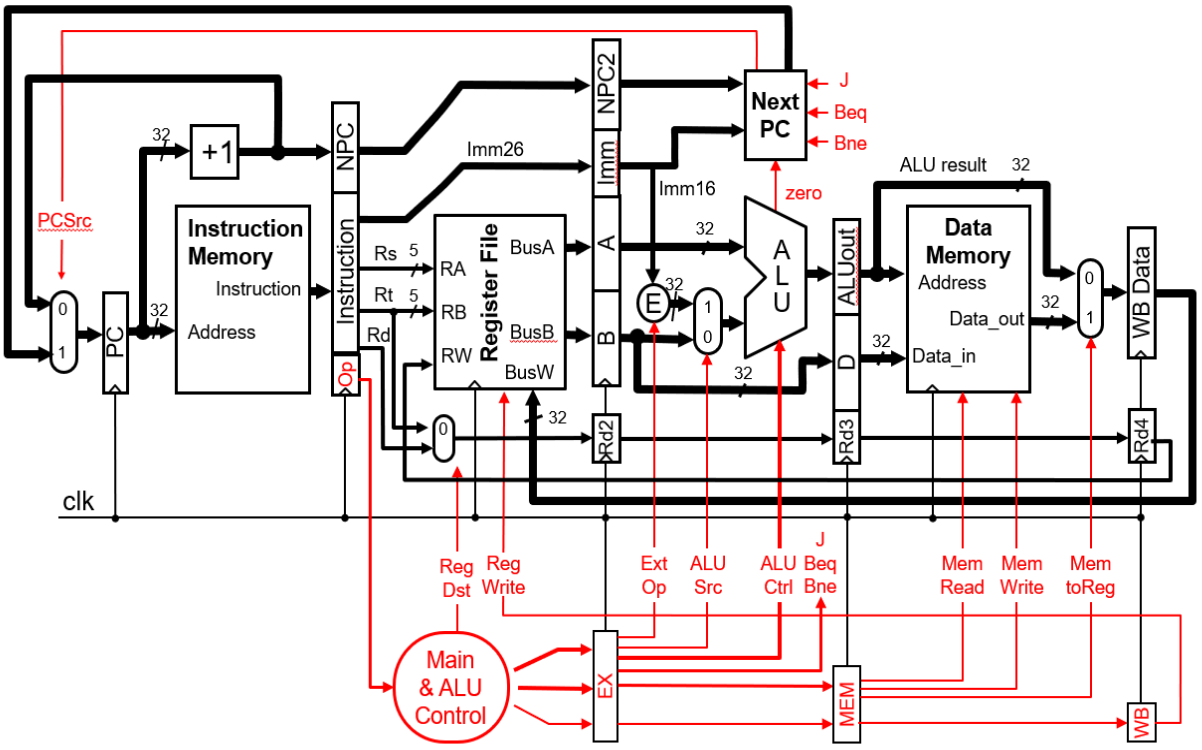
Instruction Subset:

Instruction		Meaning	Format				
add	rd, rs, rt	addition	0x00	rs^5	rt^5	rd^5	$reserved^{11}$
sub	rd, rs, rt	subtraction	0x01	rs^5	rt^5	rd^5	$reserved^{11}$
and	rd, rs, rt	bitwise and	0x02	rs^5	rt^5	rd^5	$reserved^{11}$
or	rd, rs, rt	bitwise or	0x03	rs^5	rt^5	rd^5	$reserved^{11}$
xor	rd, rs, rt	exclusive or	0x04	rs^5	rt^5	rd^5	$reserved^{11}$
slt	rd, rs, rt	set on less than	0x05	rs^5	rt^5	rd^5	$reserved^{11}$
addi	rt, rs, imm^{16}	add immediate	0x06	rs^5	rt^5	Imm^{16}	
6slti	rt, rs, imm^{16}	slt immediate	0x07	rs^5	rt^5	Imm^{16}	
andi	rt, rs, imm^{16}	and immediate	0x08	rs^5	rt^5	Imm^{16}	
ori	rt, rs, imm^{16}	or immediate	0x09	rs^5	rt^5	Imm^{16}	
xori	rt, imm^{16}	xor immediate	0x0a	rs^5	rt^5	Imm^{16}	
lw	rt, imm^{16}(rs)	load word	0x0b	rs^5	rt^5	Imm^{16}	
sw	rt, imm^{16}(rs)	store word	0x0c	rs^5	rt^5	Imm^{16}	
beq	rs, rt, $offset^{16}$	branch if equal	0x0d	rs^5	rt^5	$offset^{16}$	
bne	rs, rt, $offset^{16}$	branch not equal	0x0e	rs^5	rt^5	$offset^{16}$	
j	$address^{26}$	jump	0x0f	$Address^{26}$			

Addressing Modes:



Block Diagram:



Pipelining:

The pipeline consists of 5 stages:
Instruction fetch, Instruction decode, execution, memory, write back.