Chapter 5

Bipolar Junction Transistor

5.1 Introduction

Transistor is the solid state counterpart of vacuum triode. *It provides a number of advantages over the vacuum tube counterpart.* For example, it is smaller in size, light weight and mechanically rugged; it requires no filament heating power and time and becomes instantly available for use; it has smaller power requirement, greater efficiency and longer life. For all these it is considered to be one of the important developments in the field of electronics. The most common transistor is the bipolar junction transistor (BJT) invented by W. Shockley in 1951. It is an extension of junction diode and consists of a single crystal of semiconductor with two p-n junctions. Junction transistors can be of two types p-n-p type and n-p-n type. If a layer of n-type material is sandwiched between two p-type layers, the transistor is referred to as p-n-p type. On the other hand,

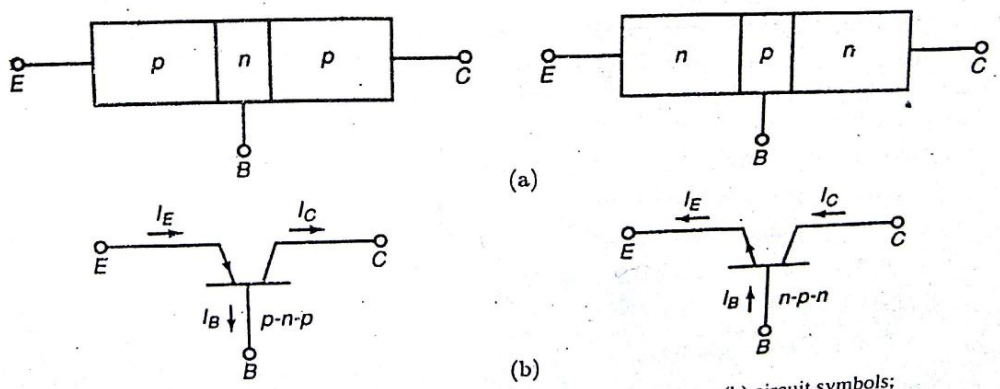

Fig. 5.1-1: (a) Schematic diagrams of a p-n-p and an n-p-n transistor (b) circuit symbols; the emitter; base and collector currents are shown in their actual conventional current directions

if a layer of p-type material is sandwiched between two n-type layers, the transistor is called n-p-n type. There are several techniques of fabricating transistors e.g., grown junction, alloy junction, diffusion and epitaxial techniques. Schematic diagrams and circuit symbols of p-n-p and n-p-n transistors are shown in Fig. 5.1-1. The central layer is made very thin and lightly doped as compared with two outer layers and is called base (B). The outer sections are called emitter (E) and collector (C). Though they appear to be identical their electrical conductivities are made different by adding different amount of impurities. The emitter layer is heavily doped and the collector only lightly doped. Moreover, in commercial transistors the area of the collector-base junction is made considerably larger than that of the emitter-base junction. This is done so because in most cases collector junction has to handle more power than the emitter. (So *if collector and emitter are interchanged normal transistor action cannot be obtained.*) The doping of base layer is also made considerably lower than that of the outer layers. The name base is related to the original method of manufacturing transistors. For normal operation emitter-base junction is forward biased and collector-base junction is reversed biased. The emitter (in p-n-p transistor) injects holes into base and these holes are finally collected by the collector. Thus the name follows. (Since the E-B junction is forward biased its dynamic resistance is small and since the C-B junction is reverse biased its dynamic resistance is large.) Due to transistor action it is found that an almost same current passes from a low resistor input circuit to a high resistor output circuit. The term transistor has been derived from the words '*transfer resistor*'. The arrow heads in the circuit symbols in Fig. 5.1-1 are in the direction of current flow when E-B junction is forward biased.

5.2 A. Manufacturing of Transistor

The first transistor invented in 1948 was of point contact type. It consists of two tungsten wires pressed against a semiconductors wafer. Because of very poor reliability and reproductibility point contact transistor has nowadays become practically obsolete. Most transistors found in the market are of junction type.

There are four basic techniques for the manufacture of transistors :

(i) **Grown junction technique :**

In this technique a single crystal is grown from a melt of Si or Ge whose impurity concentration is changed alternatively during crystal growing by adding n-type or p-type impurities. As a result alternate p-region and n-region are grown. Finally it is sliced into pieces according to the need and contacts are made to each region. Thus one can manufacture n-p-n or p-n-p transistors.

(ii) **Alloy junction technique :**

In this technique two small pellets of the same impurity element are placed on opposite sides of a thin semiconductor wafer having the opposite impurity. The assembly is heated in a furnace with carefully controlled temperature-time cycle

such that the impurity elements dissolve some of the wafer material. On cooling two p-n junctions are formed on either side of the wafer. Leads are soldered to the surplus impurity elements. The collector pellet is taken larger which makes the collector junction larger.

(iii) **Diffusion technique :**

This technique involves gaseous diffusion of impurities in a semiconductor wafer and leads to the *planar silicon transistors.* For example, let us consider the construction of an n-p-n silicon planar transistor. One starts with a wafer of n-type silicon which serves as the collector. It is put in a furnace in an atmosphere of gaseous p-type impurities. The impurities diffuse into the surface of n-type wafer through a diffusion mask and forms the p-type base. Next n-type emitter is diffused to the base through a different mask. A thin layer of SiO_2 is grown over the entire surface and photoetched to make aluminium contacts for the emitter and base leads.

(iv) **Epitaxial technique :**

The term '*epitaxial*' has been derived from Greek words '*epi*' means 'upon' and '*taxis*' means 'arrangement'. In this technique a very thin layer of p-type or n-type

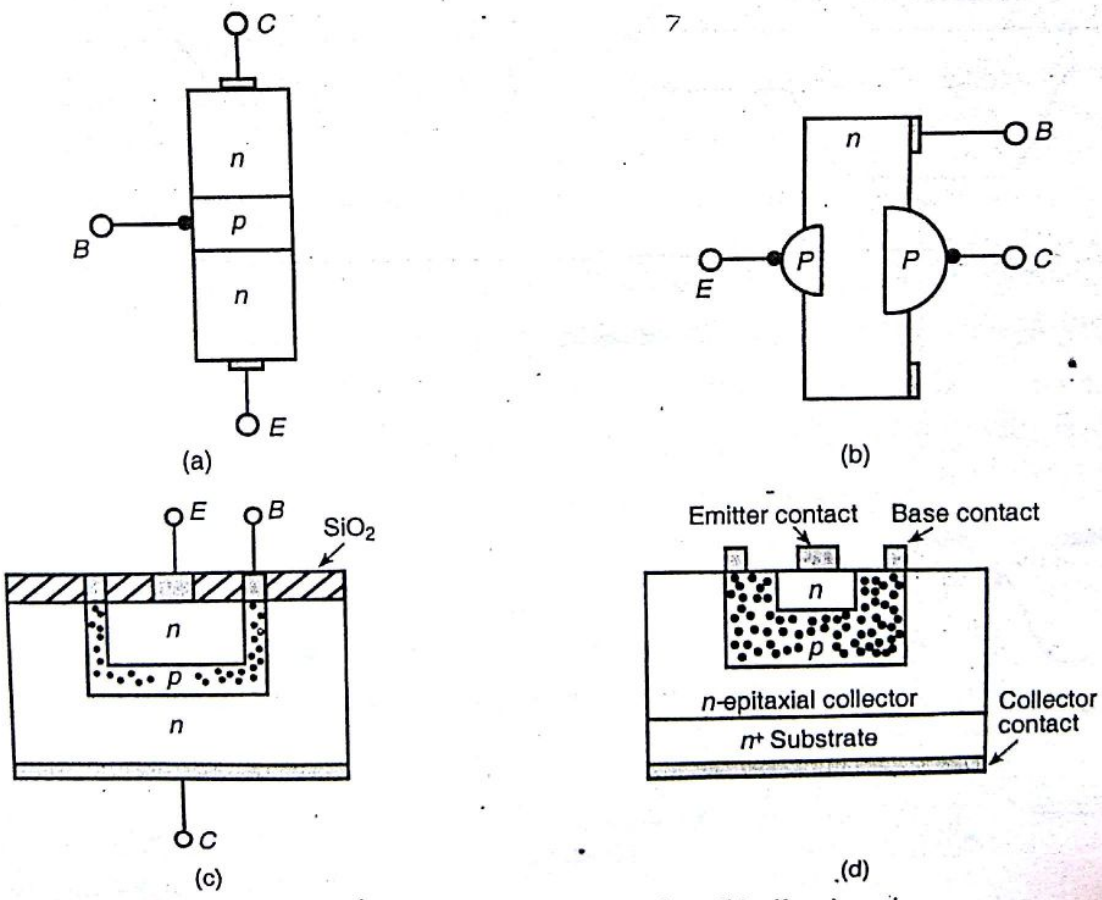

Fig. 5.2-1: Transistors : (a) Grown junction, (b) alloy junction, (c) planar diffusion and (d) planar epitaxial types

semiconductor is grown on a heavily doped substrate of the same material. The substrate is placed in a furnace containing vapour of the same material. Through proper control of temperature a thin epitaxial layer may be grown. This extended crystal forms the collector on which the base and emitter may be diffused.

B. Energy Band Diagram of a Transistor

Fig. 5.2-2(a) shows the energy band diagram of an unbiased transistor with completely symmetric p-n junctions, where V_b is the intrinsic potential barrier at the two junctions. Fig. 5.2-2(b) shows the corresponding energy band diagram with E-B junction forward biased by a voltage V_{EB} and the collector base junction reversed biased by a voltage V_{CB}. The forward biasing of E-B junction reduces the intrinsic energy barrier $|eV_b|$ to $|eV_b| = |eV_{EB}|$ and the reverse biasing of C-B junction increases the energy barrier to $|eV_b| + |eV_{CB}|$.

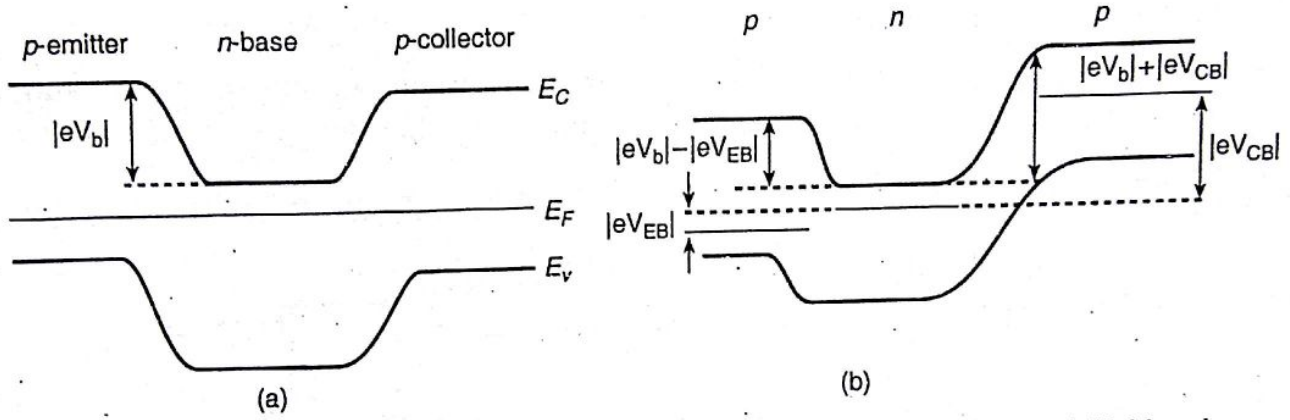

Fig. 5.2-2: Energy band diagram of a symmetric p-n-p transistor (a) unbiased (b) biased

Fig. 5.2-3(a) shows the energy band diagram of a symmetrical n-p-n transistor in an open-circuited condition and Fig. 5.2-3(b) shows the corresponding band diagram with E-B junction forward biased by a voltage V_{EB} and C-B junction reverse biased by a voltage V_{CB}.

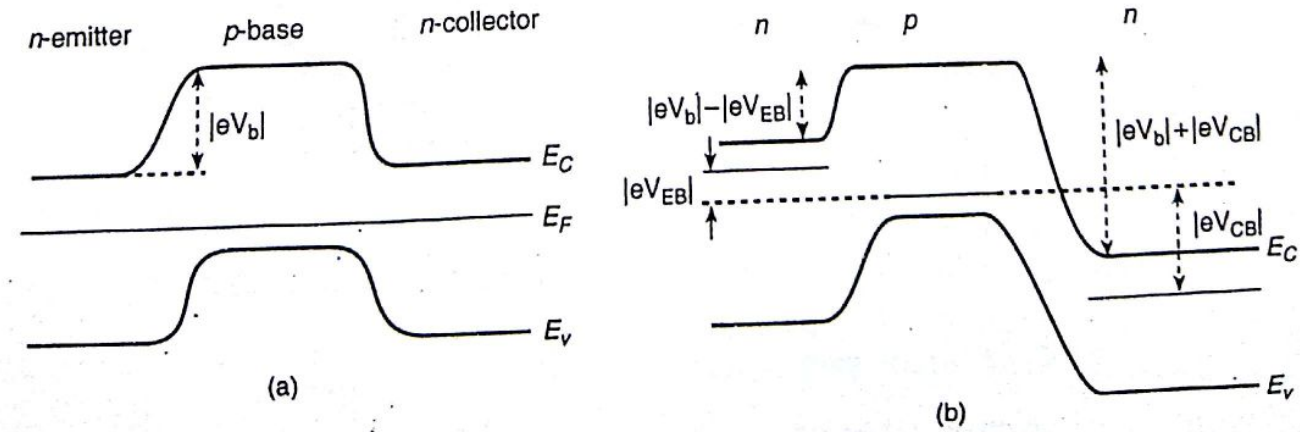

Fig. 5.2-3: Energy band diagram of a symmetric n-p-n transistor (a) unbiased (b) biased

C. Transistor Operation and Current Components

To understand the basic operation of a transistor we consider a p-n-p transistor with its E-B junction (J_E) forward biased and C-B junction (J_C) reversed biased. In the absence of any external bias all the currents through the transistor must be zero because of the development of intrinsic potential barrier across the p-n junctions. Fig. 5.2-4 shows the potential distribution in an unbiased p-n-p transistor whose junctions are assumed to be completely symmetrical. Obviously there is an intrinsic potential barrier V_b at the junctions J_E and J_C. Now the forward biasing voltage V_{EB} reduces the emitter-base potential barrier to $V_b - |V_{EB}|$ whereas the reverse biasing voltage V_{CB}

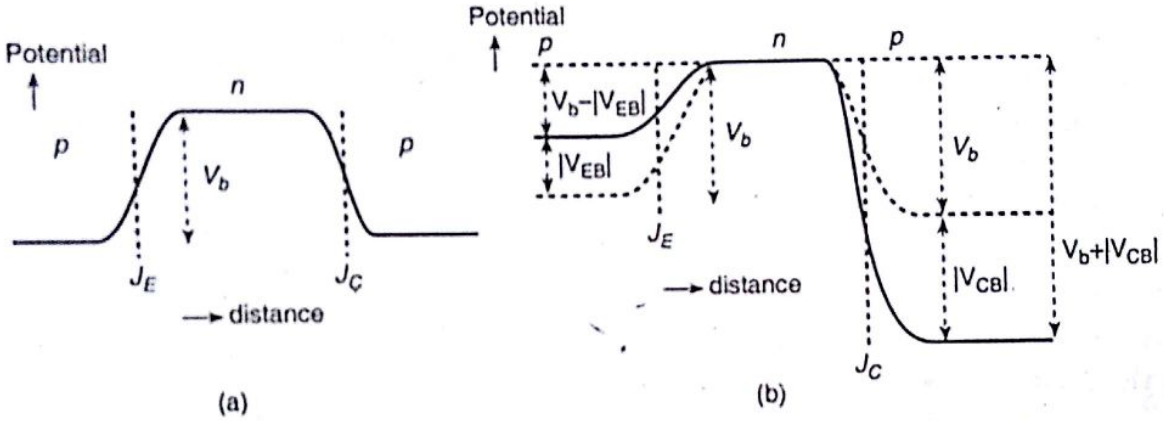

Fig. 5.2-4: Potential variation through a symmetrical p-n-p transistor (a) unbiased (b) J_E forward biased and J_C reverse biased

increases the potential barrier across collector junction J_C [Fig. 5.2.4(b)] to $V_b + |V_{CB}|$. The lowering of emitter junction barrier permits injection of holes from emitter to base and injection of electrons from base to emitter. These two flows constitute the emitter current as $I_E = I_{pE} + I_{nE}$, where I_{pE} is due to holes moving from emitter to base and

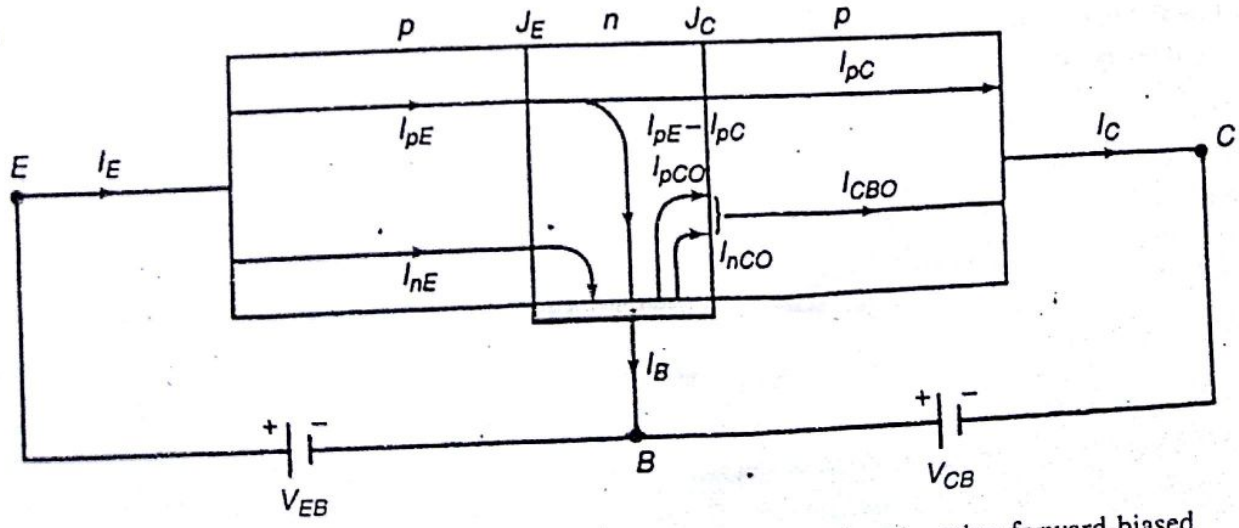

Fig. 5.2-5: Current components in a p-n-p transistor with emitter junction forward-biased and collector junction reverse-biased

I_{nE} is due to electrons going from base to emitter. In commercial transistors doping of emitter region is made much higher than that of the base. This makes $I_{pE} \gg I_{nE}$ and the emitter current is almost due to holes only. This is desirable because the current component I_{nE} does not contribute to the collector current. The injected holes diffuse through the base region towards the collector junction. While diffusing through the base a few of the injected holes (typically 1-3%) are lost due to recombination with majority electrons in the base. The holes reaching the collector junction fall down the potential barrier and are immediately collected by the collector. This gives rise to the component I_{pC} of the collector current. I_{pC} is slightly smaller than I_{pE} and the difference $(I_{pE} - I_{pC})$ constitutes a part of the base current.

The base current is due to flow of electrons from battery to the base to maintain the charge neutrality of the base region. Since the collector junction is reverse biased there is a small collector current even with emitter open. This current consists of two components: I_{nCO} due to minority electrons flowing from p-side to n-side across the collector junction J_C and I_{pCO} due to minority holes moving from n-side to p-side across J_C. The resultant $I_{nCO} + I_{pCO}$ is denoted by I_{CBO} and is called leakage current or the *reverse collector saturation current with emitter open*. It is the collector to base current with the emitter open. This component is very much temperature sensitive and is responsible for change of transistor characteristics with temperature. Here we have the relations:

$$I_C = I_{pC} + I_{CBO} \tag{5.2-1}$$

$$\text{and } I_E = I_B + I_C \tag{5.2-2}$$

The operation of an n-p-n transistor is exactly the same as above but with the roles played by the electrons and holes interchanged. The polarities of the batteries and also the directions of various currents are to be reversed as shown in Fig. 5.2-7. The potential distribution diagram for an n-p-n transistor will be similar to that of a p-n-p transistor but with the sign of potential changed (Fig. 5.2-6). Electron being a negatively charged particle likes to move from a lower potential region to a higher potential region.

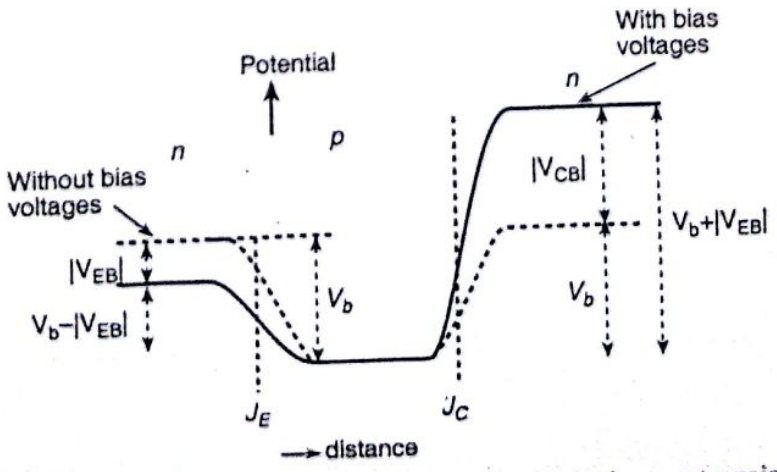

Fig. 5.2-6: Potential variation through a symmetrical *n-p-n* transistor

Here the majority electrons from emitter are injected into the base and majority holes from base are injected into emitter region. The two constitutes the emitter current as $I_E = I_{nE} + I_{pE}$. Since the doping of emitter region is much higher than that of the base, $I_{nE} \gg I_{pE}$ and we have $I_E \approx I_{nE}$. Thus here the emitter current is almost entirely due to electrons moving from emitter to base. Since electrons are negatively charged the direction of conventional current is opposite to the movement of electrons. The injected electrons diffuse through base towards the collector junction. A few of the injected electrons are lost due to recombination with majority holes in the base.

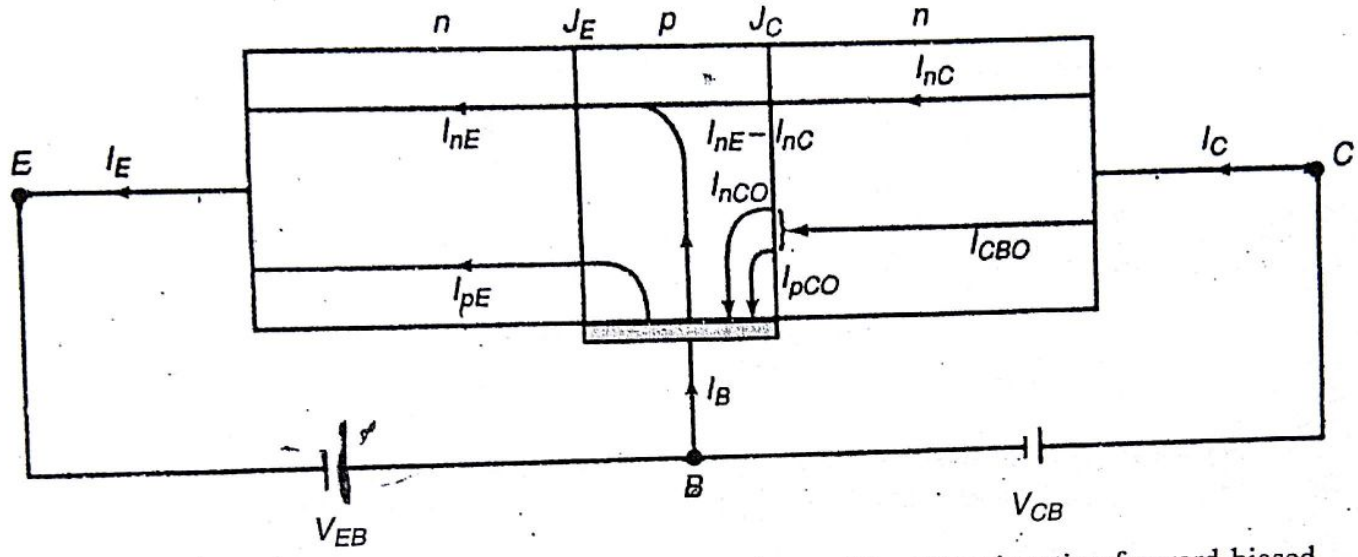

Fig. 5.2-7: Current components in an *n-p-n* transistor with emitter junction forward-biased and collector junction reverse-biased

The electrons reaching the collector junction are collected by the collector and give rise to the current component I_{nC}. The difference $I_{nE} - I_{nC}$ constitutes a part of base current. Since the collector junction is reverse biased there is also reverse saturation current through this junction even when the emitter is open. This component is denoted by I_{CBO}. It consists of two parts: I_{nCO}, due to movement of minority electrons from base to collector, I_{pCO}, due to movement of minority holes from collector to base. Here we have the relations:

$$I_C = I_{nC} + I_{CBO} \tag{5.2-3}$$

$$I_E = I_B + I_C \tag{5.2-4}$$

5.3 Three Modes of Connection of a Transistor

A junction transistor has got three terminals—base, emitter and collector and hence it can be used as a two-port network with one of the three terminals common to both input and output. Thus we have three different configurations or mode of connections as shown in Fig. 5.3-1. The configuration in which the base terminal is common to both the input and the output circuits is known as *common base* (CB) or grounded base transistor connected in CB mode is shown in Fig. 5.3-1(a). When the

Usually $I_B \gg I_{CBO}$ and hence $I_C \approx \beta I_B$. Thus $\beta_{\text{d.c.}} \approx \beta$.

Usually in commercial transistors $\beta_{d.c.}$ or h_{FE} is in the range 50 to 400. Moreover, h_{FE} depends on I_C and temperature.

For operation with a.c. one defines the small signal short circuit CE current gain $\beta_{\text{a.c.}}$ or h_{fe}. It is defined as the ratio of change in I_C to the change in I_B at a fixed collector-to-emitter voltage V_{CE}. Thus

$$\beta_{\text{a.c.}} \quad \text{or} \quad h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} \tag{5.4-8}$$

h_{fe} is found to be larger than h_{FE} for small I_C and h_{fe} is smaller than h_{FE} for large I_C. However, in most cases h_{fe} differs from h_{FE} by less than 20%.

Relationship between α and β:

$$\begin{aligned} &\text{By definition} \quad \alpha_{\text{d.c.}} = \frac{I_C}{I_E} \\ &\text{and} \qquad\qquad \beta_{\text{d.c.}} = \frac{I_C}{I_B} \\ &\text{Now} \qquad\qquad I_E = I_B + I_C \end{aligned} \tag{5.4-9}$$

Dividing by I_C, we get

$$\begin{aligned} &\frac{1}{\alpha_{\text{d.c.}}} = \frac{1}{\beta_{\text{d.c.}}} + 1 \\ &\text{or,} \qquad \beta_{\text{d.c.}} = \frac{\alpha_{\text{d.c.}}}{1 - \alpha_{\text{d.c.}}} \end{aligned} \tag{5.4-10}$$

Now, since $\alpha_{\text{d.c.}} \approx \alpha$ and $\beta_{\text{d.c.}} \approx \beta$ we can write from Eq. (5.4-10),

$$\beta = \frac{\alpha}{1 - \alpha} \tag{5.4-11}$$

5.5 Emitter Efficiency and Base Transport Factor

The value of transistor α depends on the motion of carriers through the base as well as on the processes occurring in the emitter and the collector junctions. For this α is usually represented as the product of the coefficients characterizing these processes,

$$\alpha = \gamma \cdot \beta^* \cdot M$$

where γ is the emitter injection efficiency , β^* is the base transport factor and M is the collector multiplication ratio.

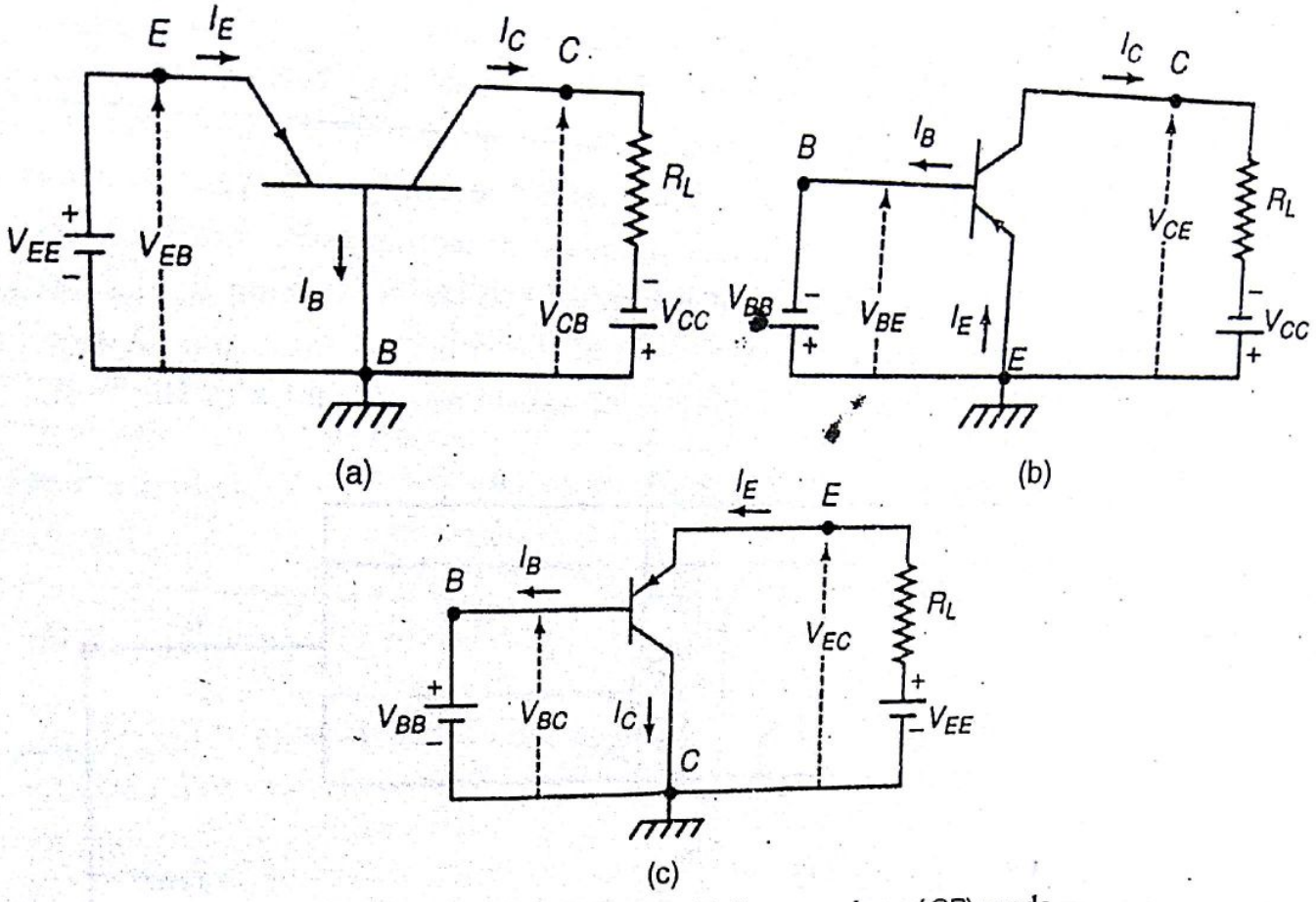

Fig. 5.3-1: *p-n-p* trasistor connected in (a) Common base (*CB*) mode (b) Common emitter (*CE*) mode (c) Common collector (*CC*) mode

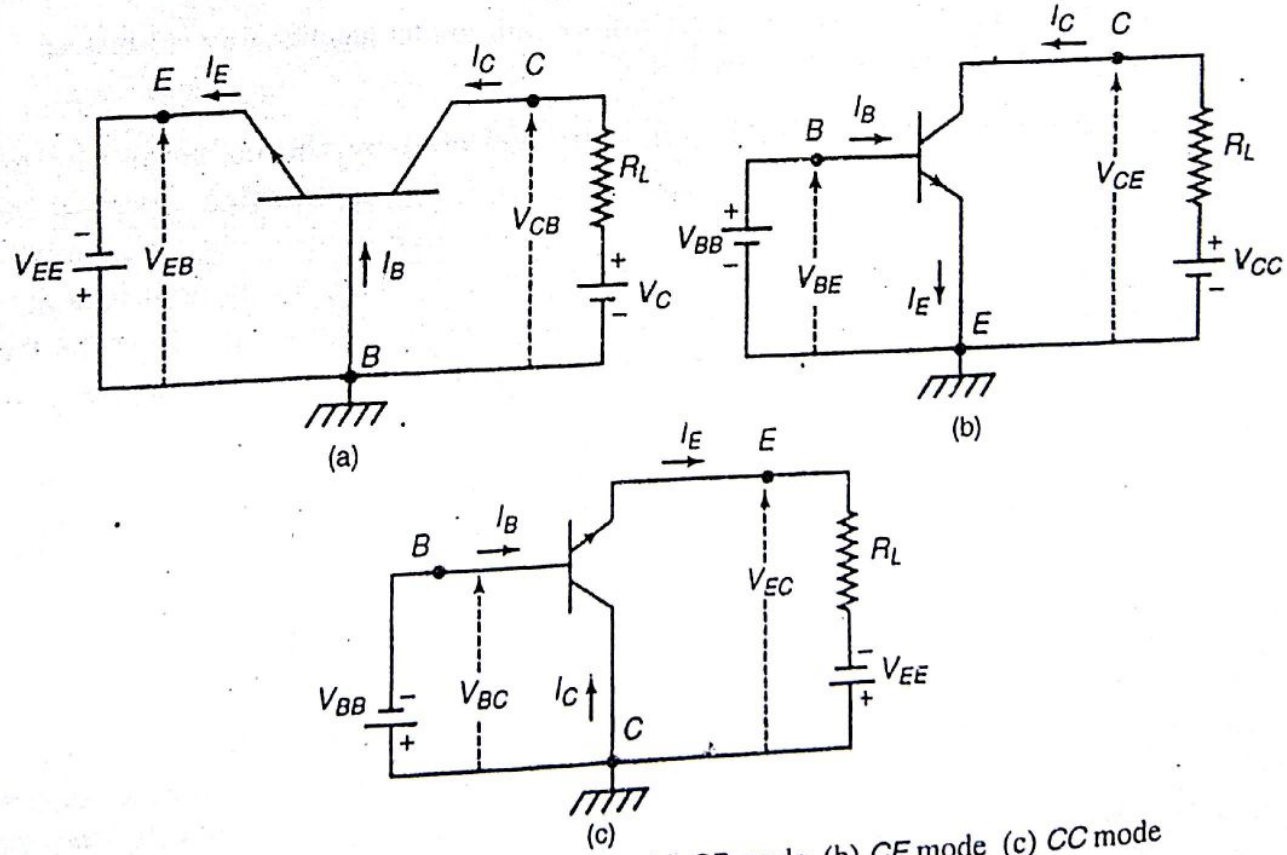

Fig. 5.3-2: *n-p-n* trasistor connected in (a) *CB* mode (b) *CE* mode (c) *CC* mode

emitter terminal is common to both the input and the output circuits, the transistor configuration is called *common emitter* (*CE*) or grounded emitter mode. Fig. 5.3-1(b)

shows a p-n-p transistor connected in CE mode. When the collector terminal is common to both the input and output circuits, the transistor is said to be connected in *common collector* (CC) mode or common collector configuration. This mode is also called grounded collector mode.

Connections of an n-p-n transistor in different modes can be obtained simply by changing polarities of the batteries in Fig. 5.3-1. These are shown in Fig. 5.3-2.

5.4 Transistor Alpha (α) and Beta (β)

The collector current I_C consists of two components, the reverse saturation current I_{CBO} and the predominant portion representing a part of the emitter current reaching the collector. Thus

$$I_C = \alpha I_E + I_{CBO} \tag{5.4-1}$$

where α is called transistor alpha. It represents the fraction of emitter current that can reach the collector. In d.c. mode of operation we define d.c. alpha, $\alpha_{\text{d.c.}}$, by the relation

$$\alpha_{\text{d.c.}} = \frac{I_C}{I_E} \tag{5.4-2}$$

Usually I_{CBO} is much smaller than I_C and we can write

$$I_C \approx \alpha I_E \tag{5.4-3}$$

Thus $\alpha \approx \alpha_{\text{d.c.}}$.

For operation with a.c. quantities one defines the small signal short-circuit common-base current gain $\alpha_{\text{a.c.}}$. It is defined as the ratio of the change in the collector current to the change in the emitter current at constant collector-to-base voltage, i.e.,

$$\alpha_{\text{a.c.}} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}} \tag{5.4-4}$$

For a good transistor $\alpha \approx \alpha_{\text{d.c.}} \approx \alpha_{\text{a.c.}}$ and all must be as close to unity as possible. Usually in good transistors α ranges from 0.98 to 0.988. However, α is not constant but varies with I_E, V_{CB} and temperature.

In a transistor connected in CE mode input current is I_B and output current is I_C. In this case the performance of the transistor is expressed in terms a parameter called transistor beta (β). Using the relation $I_E = I_B + I_C$ we get from Eq. (5.4-1),

$$\begin{aligned} I_C &= \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \\ &= \beta I_B + (1+\beta) I_{CBO} \end{aligned} \tag{5.4-5}$$

$$\text{where } \beta = \frac{\alpha}{1-\alpha} \tag{5.4-6}$$

is called transistor beta. In d.c. mode of operation we define d.c. beta by the relation

$$\beta_{\text{d.c.}} \text{ or } h_{FE} = \frac{I_C}{I_B} \tag{5.4-7}$$

In CB mode the variation of the output collector current (I_C) with output ctor-base voltage taking input emitter current (I_E) as parameter, gives the stati*utput characteristics.* A typical set of CB output characteristics, of an n-p-n tranor is shown in Fig. 5.8-4. On the curves three distinct regions of transistor operatihave been marked.

Active region : In active region emitter junction is forward biased and the ector junction is reverse biased. At the lower end of the active region $I_E = 0$ and the ector current is simply the reverse saturation current I_{CBO}. I_{CBO} is of the order a few μA for Ge and of the order of nA for Si made transistors. Now as I_E increase above zero, the collector current is given by the relation

$$I_C = \alpha I_E + I_{CBO} \approx \alpha I_E$$

Since α is close to unity, I_C is only slightly smaller than I_E. H is increased α decreases and I_C differs appreciably from I_E. In this regi current is almost independent of V_{CB}. However, because of Early effect I_C slightly with V_{CB}. Increase in V_{CB} decreases effective base width. It r probability of recombination of carriers, while diffusing through the base. increased. If V_{CB} is increased very much there may be collector junction causing sharp rise in I_C.

Saturation region : In this region both the emitter and the collector jun are forward biased. In Fig. 5.8-4 it represents the region to the left of the or $V_{CB} = 0$ and above the characteristic for $I_E = 0$. It is seen that I_C is not zer when $V_{CB} = 0$. This happens so because the injected carriers still find a potential at the collector junction due to contact potential difference. To reduce I_C to zer necessary to apply a small forward bias to the collector. In an n-p-n transistor forward biased condition electrons flow from n-collector to p-base. This is o to the flow of electrons injected from emitter and reaching the collector junc sufficient forward biasing of the collector junction these two opposite flows ma or even the direction of I_C may be reversed as indicated in Fig. 5.8-4.

Cut-off region : In this region both the emitter and the collector junc reverse biased. In Fig. 5.8-4 the region to the right of the ordinate $V_{CB} = 0$ a the characteristic for $I_E = 0$ is the cut-off region.

B. Common emitter characteristics

The circuit arrangement for drawing the CE characteristics of the *most prevale* p-n transistor is shown in Fig. 5.8-5. The variation of the input base current with input base-emitter voltage V_{BE} taking the output collector emitter vo as parameter, gives the CE *input characteristics.* Typical CE input ch shown in Fig. 5.8-6. The characteristic curves are similar to that p-n junction. For a constant V_{BE}, I_B decreases with increase

crease in

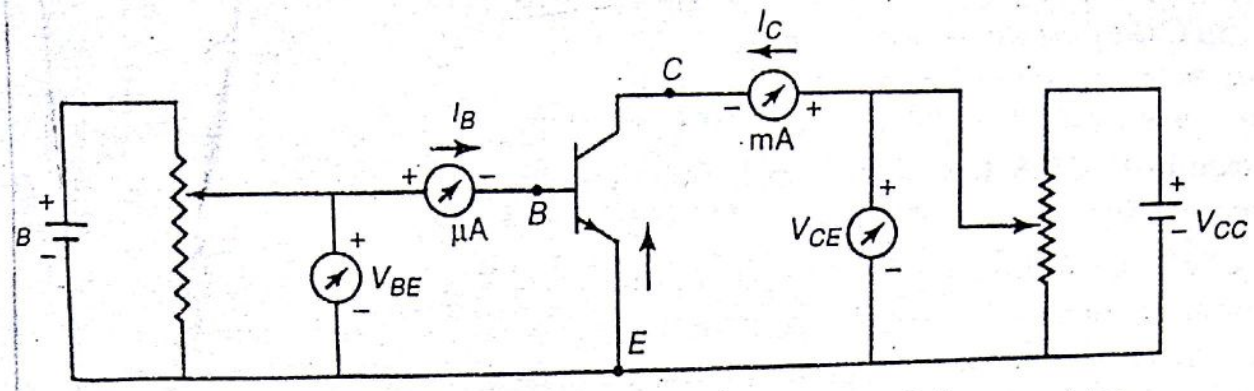

Fig. 5.8-5: Circuit arrangement to draw *CE* characteristic curves of *n-p-n* transistor. For a *p-n-p* transistor just reverse the polarities of the batteries and the meter

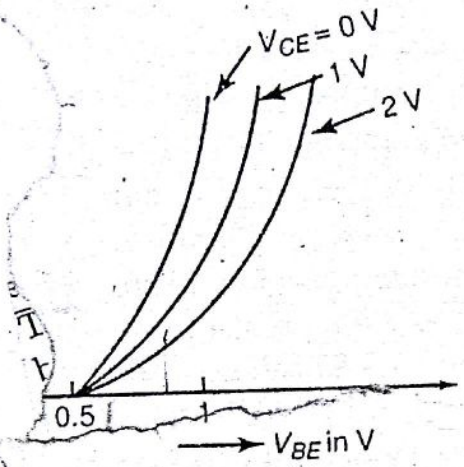

Fig. 5.8-6: *CE* input characteristics of an *n-p-n* Si transistor.

V_{CE} decreases the effective base width and hence the probability of recombination of the injected carriers in the base. As a result the recombination base current decreases.

The *CE* output characteristics are obtained by plotting output current I_C as a function of output voltage V_{CE} taking input base current I_B as parameter. Typical *CE* output characteristic curves are shown in Fig. 5.8-7. This family of curves may be divided into three regions—active, cut off and saturation regions.

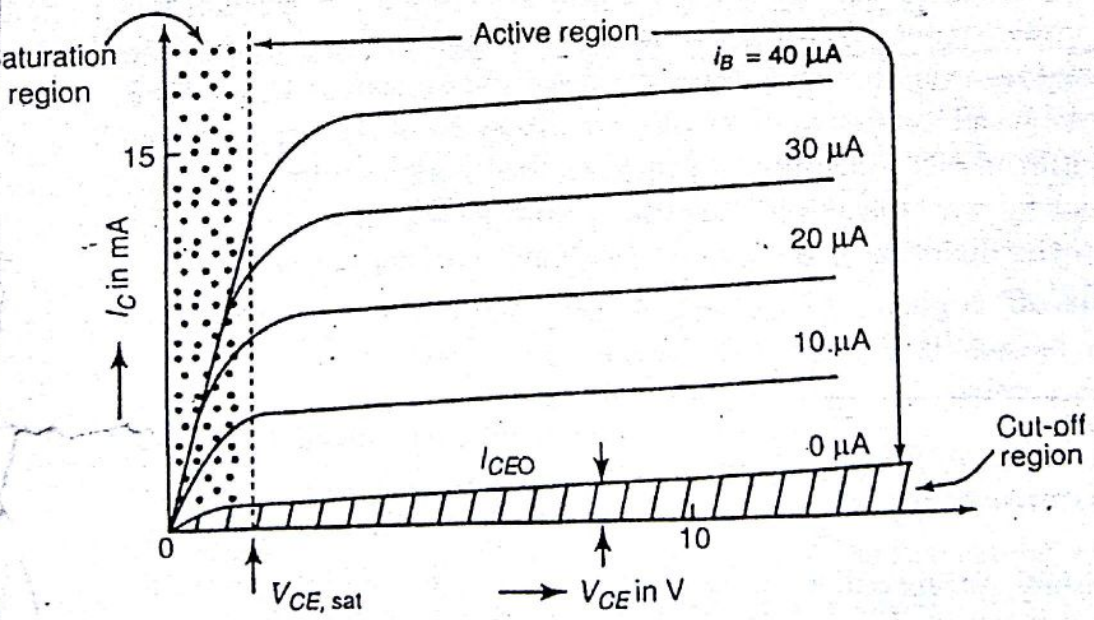

Fig. 5.8-7: Typical *CE* output characteristics curves of an *n-p-n* Si transistor.

region: In active region the emitter junction is forward biased and the junction is reverse biased. In Fig. 5.8-7 it is the region to the right of the