COL-215
ASSIGNMENT – 4
MAC Accumulator
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Design

The Multiply-Accumulate (MAC) unit is a core building block in digital systems and is used extensively in Digital Signal Processing (DSP) applications. It performs the operation:

a = a + (b × c)

In this assignment, the MAC unit takes two 8-bit operands (b and c) from the Basys3 board switches, multiplies them, and accumulates the result in a 16-bit register. The design also supports reset functionality, button debouncing, rising-edge detection for enable signals, overflow detection, and output display on both LEDs and 7-segment displays.

MECHANISM

The MAC unit multiplies two 8-bit operands (b and c) and accumulates the product into a 16-bit register.

- The **enable signal (SW12)** is edge-detected so that accumulation happens only once per rising edge.
- The **reset button (BTNC)** clears the accumulator and shows "-rSt" for 5 seconds on the 7-segment display.
- **Overflow detection** checks whether the accumulated value exceeds 16 bits. On overflow, the accumulator is cleared and "OFLO" is displayed until reset.
- The output is shown on both LEDs and 7-segment displays for better observation.

Modules

1. *mac_top*

This is the top-level module that integrates all submodules. It samples the input values of b and c
using SW10 and SW11, captures enable from SW12 through an edge detector, and connects the
multiplier and accumulator. It also drives the LEDs with the accumulated value and passes
overflow/reset signals to the display controller.

2. *debounce*

Mechanical push buttons exhibit bouncing, causing multiple transitions when pressed or released.
The debounce module filters these glitches by using a counter. The raw button input is compared
against a synchronized value, and only after a stable duration is the button state updated. This
ensures a clean reset signal.

3. *edge_detector*

The edge detector generates a one-clock-cycle pulse whenever a rising edge is detected on the
enable switch (SW12). This prevents multiple accumulations from occurring when the switch
remains in the ON position. It works by delaying the input by one clock cycle and checking the
transition.

4. *Multiplier*

The multiplier module performs an 8-bit by 8-bit multiplication to generate a 16-bit product. It is implemented using behavioral Verilog with the '*' operator for simplicity. This product is then passed
to the accumulator.

5. *accumulator*

The accumulator adds the product to the current accumulated value whenever an enable pulse is
detected. It supports parameterized initialization (default zero). Overflow detection is implemented
by extending the addition into 17 bits; if the result exceeds 16 bits, overflow is set and the accumulator is cleared. The overflow signal remains active until reset is asserted.

6. *display_ctrl*

The display controller manages the 7-segment displays. It cycles through the four digits at high
frequency using multiplexing. Upon reset, it shows '-rSt' for 5 seconds. When overflow occurs, it shows 'OFLO' until reset. Otherwise, the display remains blank. The control logic ensures proper
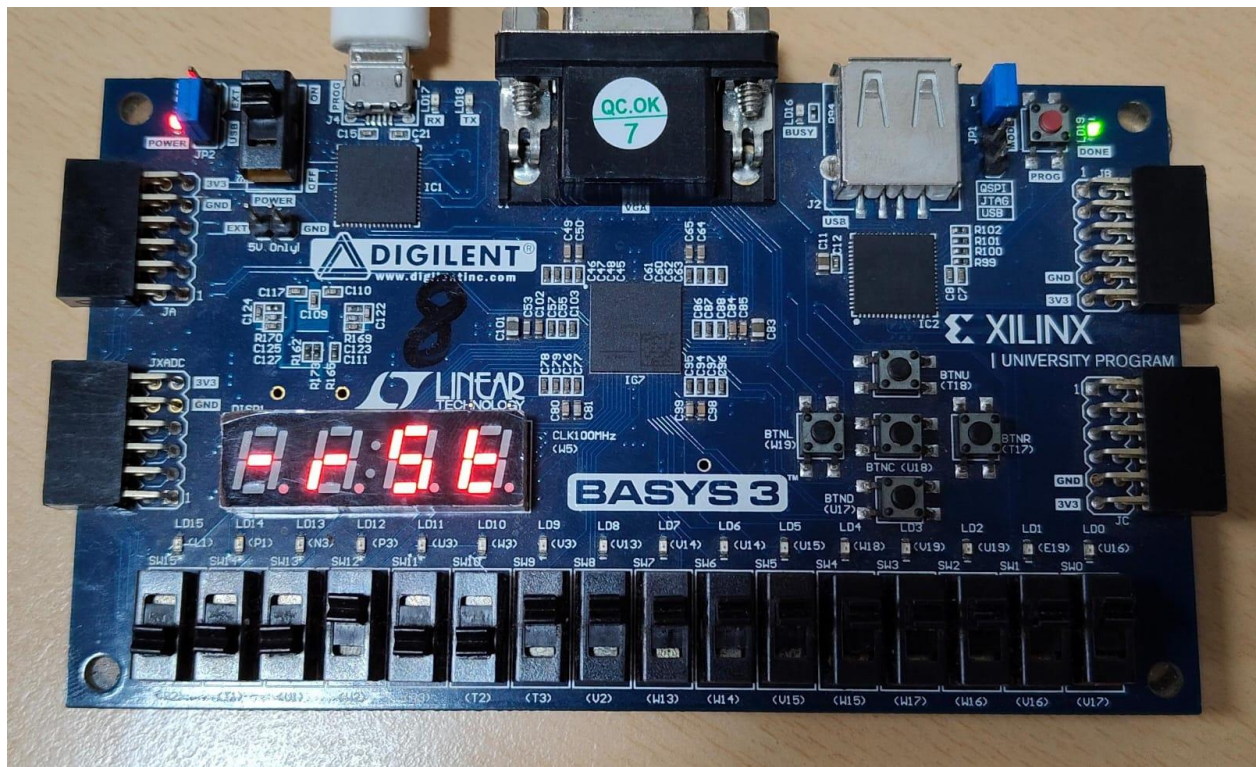left-to-right ordering for readability.

7. *ss (7-Segment Decoder)*

This module converts ASCII character codes (e.g., '-', 'r', 'S', 't', 'O', 'F', 'L') into 7-segment display
encodings. It enables textual indications on the Basys3 board for reset and overflow conditions
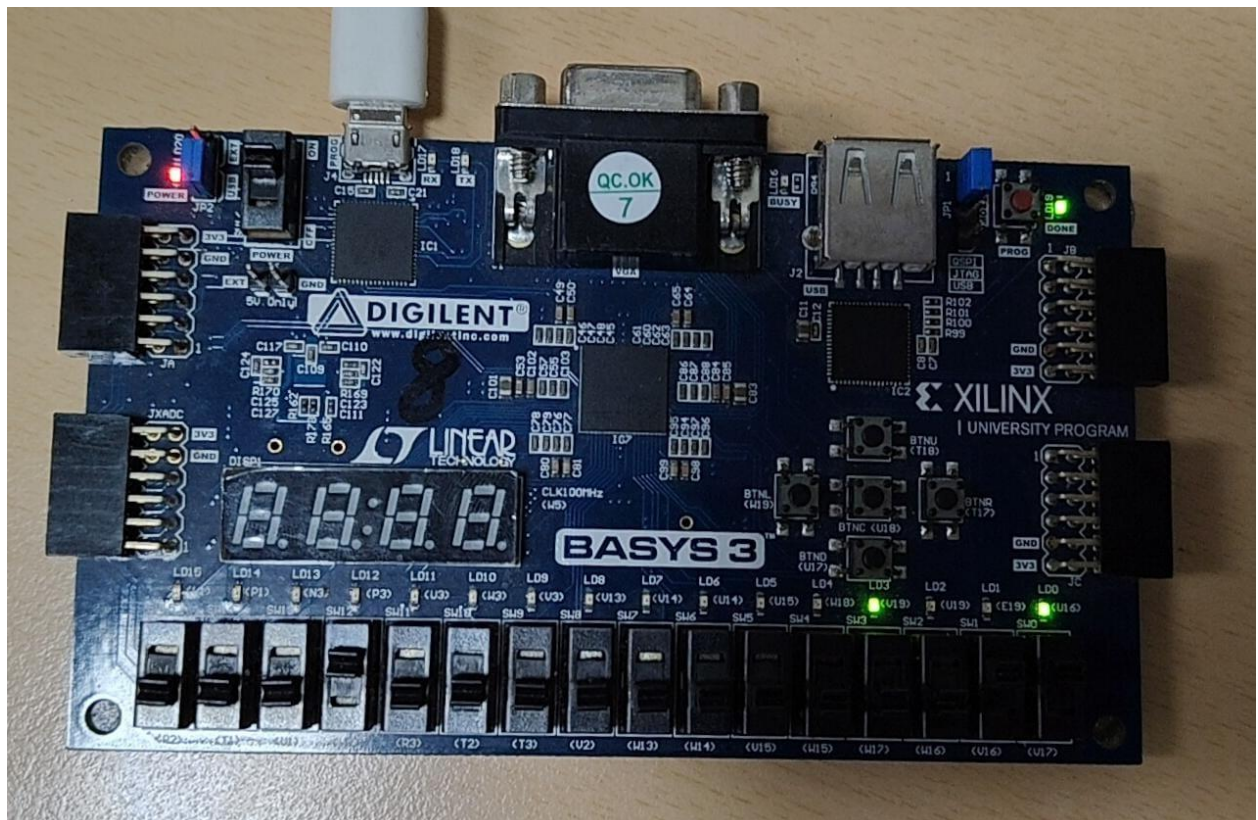
Hardware Simulation

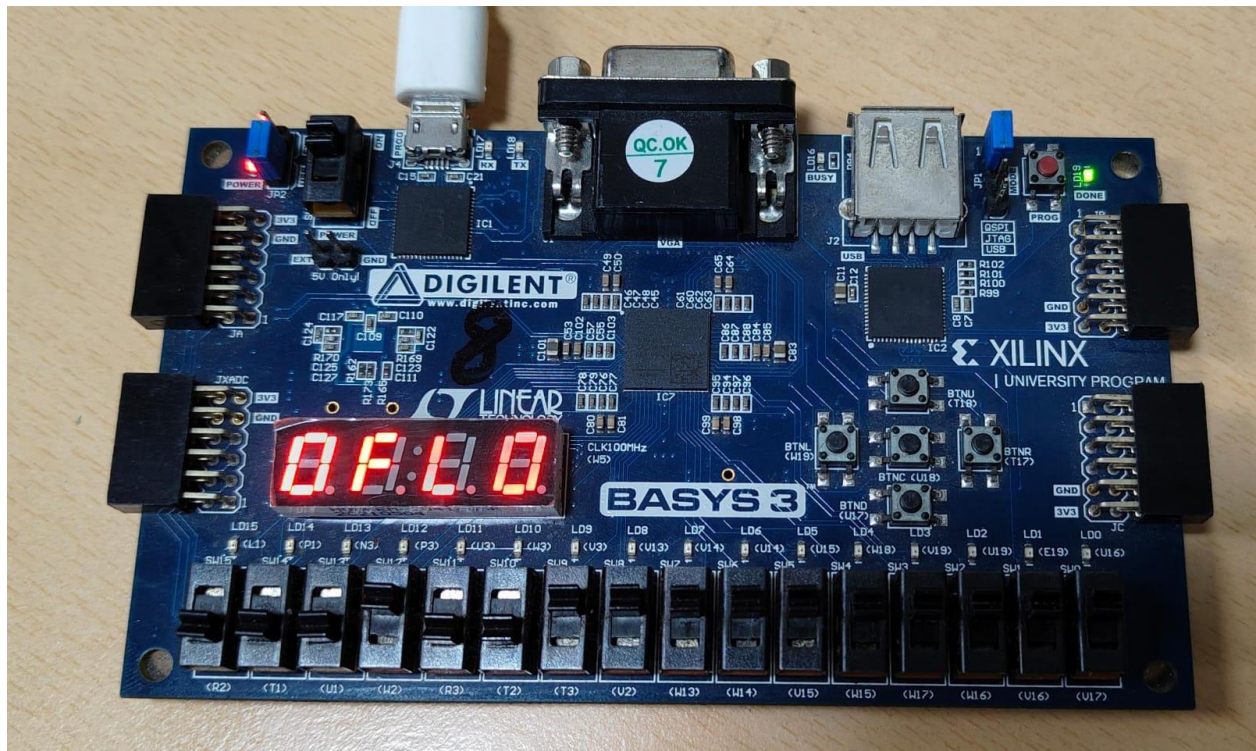During simulation, the following behaviours were verified:

1. Reset: When BTNC is pressed, the accumulator resets and the display shows '-rSt' for 5 seconds

2. Edge Detection: SW12 toggle results in a single accumulation per rising edge.

3. Overflow: When the accumulator exceeds 16 bits, overflow is set, the display shows 'OFLO', and
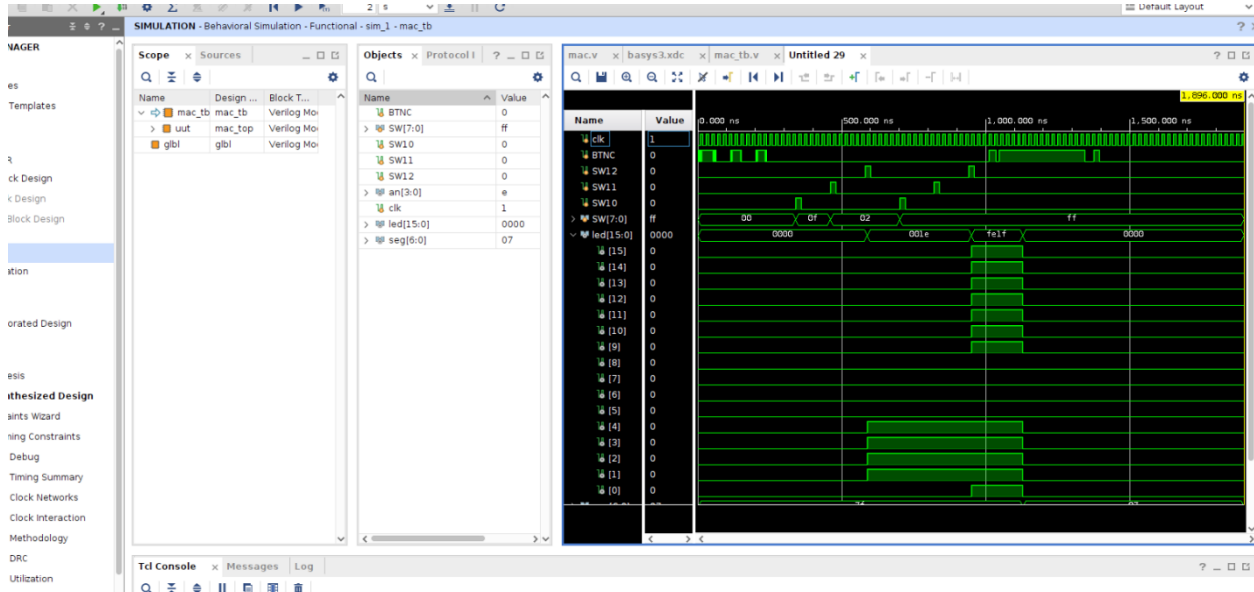accumulation halts until reset.

SIMULATION

Figure 1: Simulation waveform showing MAC function, debouncing, and accumulation.

Key observations from simulation:
• **Reset (BTNC)**: Properly initializes the accumulator and activates the reset display ("-rSt"), confirming the design returns to a known state.
• **Edge detection (SW12)**: Accumulation occurs only on the **rising edge** of SW12, preventing multiple additions during a sustained switch press.
• **Debouncer**: Correctly filters out glitches across all four specified bouncing scenarios, producing a clean reset signal as required.
• **Overflow handling**: When the accumulator exceeds 16-bit capacity, overflow is detected, the accumulator is cleared, and the display shows **"OFLO"** until the next reset.

REPORT UTILIZATION

The design was synthesized using **Vivado v2016.4** for the **Basys3 FPGA**

Resource	Used	Available	Utilization (%)
Slice LUTs	183	20,800	0.99 %
Slice Registers	111	41,600	0.27 %
Flip Flop	111	33,280	0.33%
Block RAM Tiles	0	50	0.00 %
DSP Slices	0	90	0.00 %
Bonded IOBs	40	106	37.74 %
BUFGCTRL (Clock Buff)	1	32	3.13 %

Analysis
- The design is **lightweight**, using <1% of LUTs and registers.
- **I/O utilization (37.7%)** is the highest, due to switches, LEDs, and 7-segment displays.
- No DSP or Block RAM usage → confirms multiplier used LUT-based implementation.
- Timing constraints met at **100 MHz**, making the design suitable for FPGA deployment.
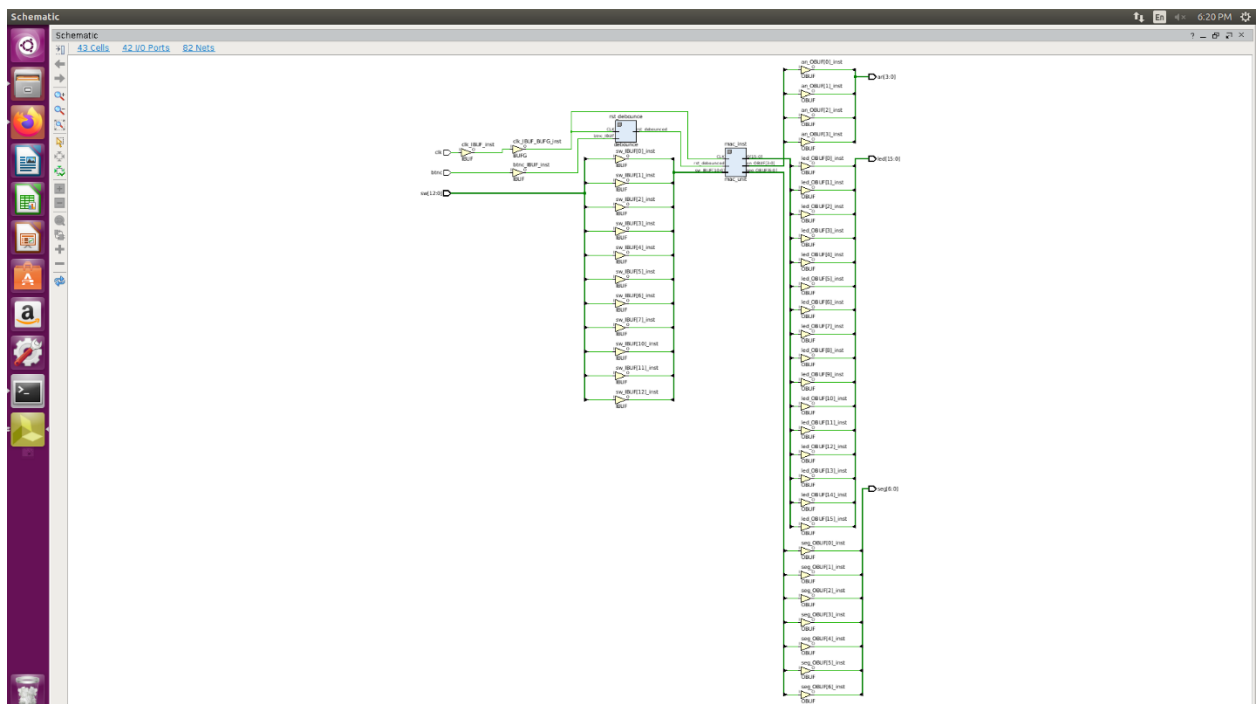
SCHEMATICS

The synthesized schematic of the MAC unit shows the interconnection of all submodules:
- **Multiplier**: Performs 8-bit × 8-bit multiplication using LUT-based implementation.
- **Accumulator**: A 16-bit register that stores accumulated values and includes overflow detection logic.
- **Debounce Circuit**: Filters glitches from the reset button to ensure stable reset behavior.
- **Edge Detector**: Ensures accumulation occurs only once per rising edge of the enable signal (SW12).
- **Display Controller**: Controls the 7-segment displays, showing "-rSt" on reset and "OFLO" on overflow.

- **Top-level Module (mac_top)**: Integrates all submodules, handles input from switches, and output to LEDs/7-segment displays.

The schematic confirms that:

- Data flows from switches (SW0–SW11) into the multiplier, then into the accumulator.
- Control signals (SW12 for enable, BTNC for reset) are passed through debounce and edge detection before reaching the accumulator.
- Outputs are directed both to **LEDs (16-bit accumulated value)** and **7-segment displays (reset/overflow status)**.

Design Decisions

Several key design decisions were made:

1. **Debouncing**: Implemented via counter instead of shift-register for robustness and simplicity.

2. **Edge Detection**: Rising-edge only detection ensures no multiple accumulations for SW12 state.

3. **Overflow Handling**: Chose to latch overflow until reset to make debugging and user interaction

easier.

4. **Display Encoding**: Characters were chosen to clearly represent states ('-rSt' and 'OFLO') and

tested for readability.

5. **Parameterization**: The accumulator was parameterized for initialization value for flexibility in

Testing.

Conclusion

The MAC unit was successfully designed and implemented on the Basys3 FPGA board. It

demonstrates clean reset behaviour, proper accumulation with edge detection, overflow handling,

and textual status display on the 7-segment displays. This project provided hands-on experience

with digital design principles such as debouncing, timing, and modular design.