COL 215

DIGITAL LOGIC AND SYSTEM DESIGN

LAB 2 REPORT

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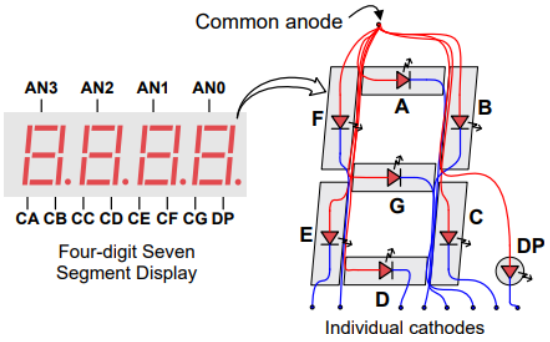
INTRODUTION

- The primary objective of the Lab Assignment 2 was to display the digits from 0 to 9 on the seven segment display on Field Programmable Gate Array (FPGA) board.
- The inputs were the 10 slide switches (SW0 TO SW9) which indicated the given decimal number and the outputs corresponded to 7 cathode pins.
- We then implanted our design on the board and created testbench files to check and run the simulation.



Anode and Cathode design in Seven Segment Display

DESIGN OVERVIEW

- We took the 9 slide switches (SW0 TO SW9) as the input and returned the outputs corresponding to the 4 anodes ([3:0] anode) and the 7 cathodes ([6:0] cat) based on the switch position.
- The design was implemented in a way that a priority order was maintained. This means that even if two switches were tuned on; the higher digit would be displayed.
- The “always” block made sure that any change in the switch position would trigger the computation again.
- We triggered all the 4 anodes but used only one (an[0]). Rest anodes were turned off (high).

SWITCH	PIN
sw[0]	V17
sw[1]	V16
sw[2]	W16
sw[3]	W17
sw[4]	W15
sw[5]	V15
sw[6]	W14
sw[7]	W13
sw[8]	V2
sw[9]	T3

CATHODE	PIN
cat[6]	W7
cat[5]	W6
cat[4]	U8
cat[3]	V8
cat[2]	U5
cat[1]	V5
cat[0]	U7

ANODE	PIN
an[0]	U2
an[1]	U4
an[2]	V4
an[3]	W4

The Pin Mapping as per the constraints in the Basys file.

SIMULATION

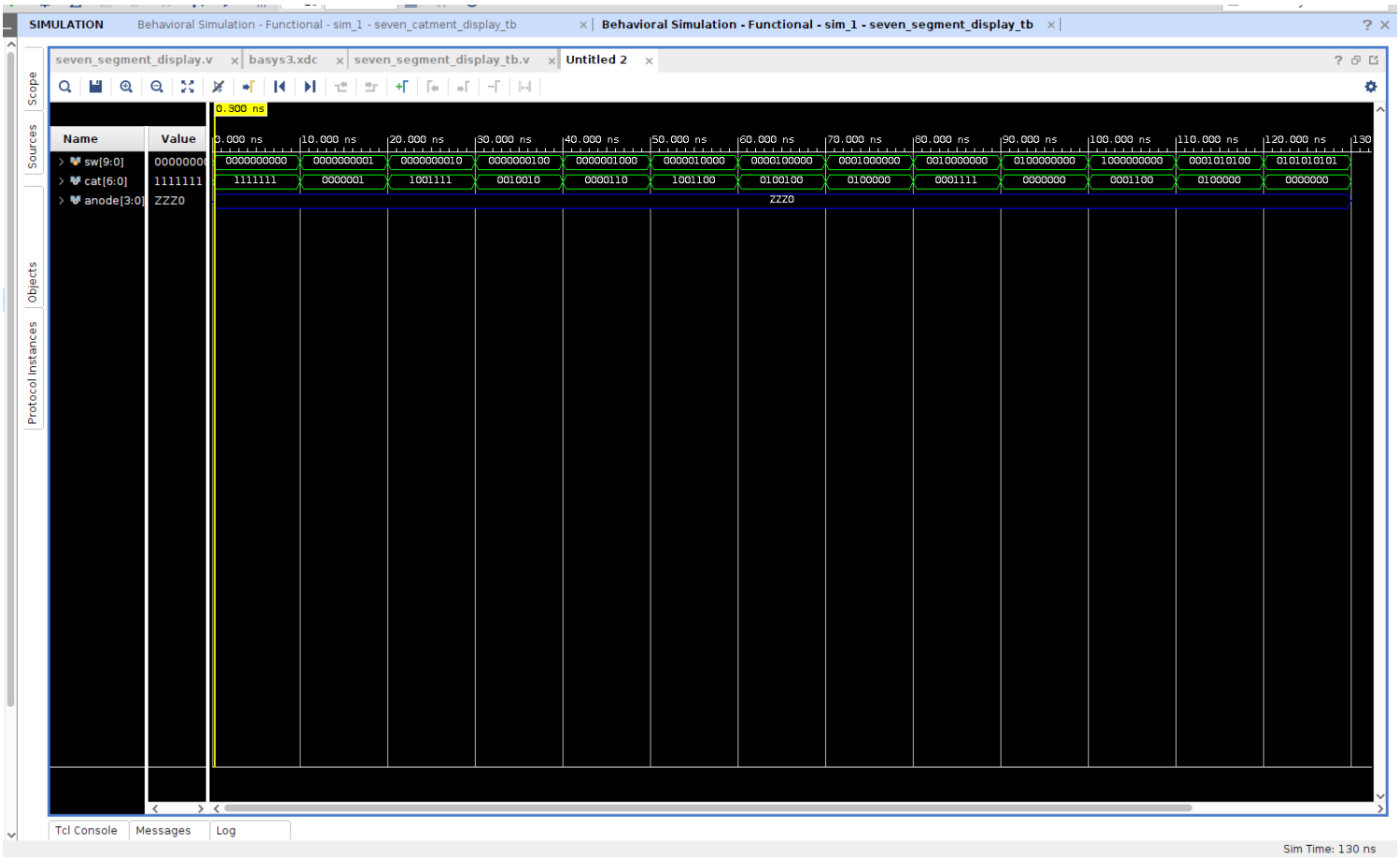


Figure 1 Simulation showing switches and cathode outputs

Based on the switch that is turned on, the corresponding cathode bitstring is received. The bitstring is in the “abcdefg” format which represent the seven segments of the cathode. Also cathode is active low, which means that 1 corresponds to OFF and 0 corresponds to ON. Only an[0] is used to display the digit.

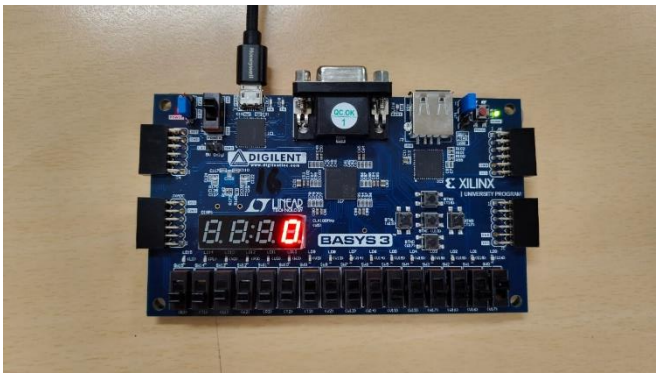
DESIGN DECISIONS

- Used combinational logic (always @(*)) for immediate output updates without a clock.
- Activated only one anode (4'b1110) to display a single digit.
- Used active-low logic for anodes and cathodes as per Basys3 manual.

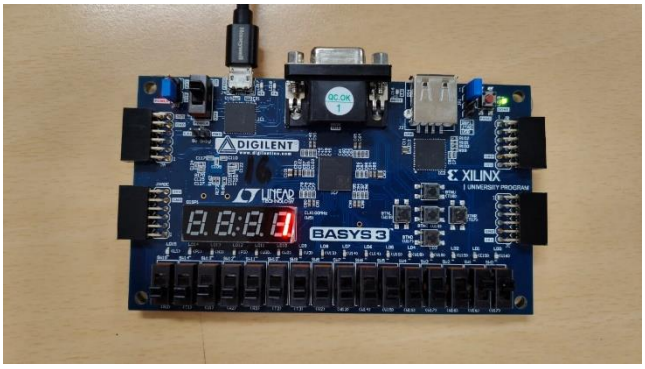
- Implemented priority logic using the else if ladder: sw[9] has the highest priority, sw[0] lowest.
- Default output (1111111) turns all segments off when no switch is active.

HARDWARE

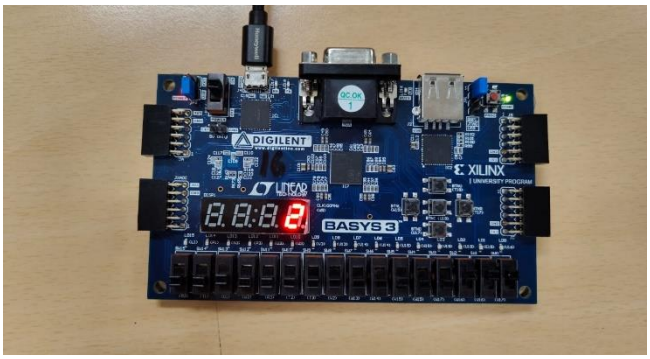
The figures shows the hardware implementation of the seven segment display.



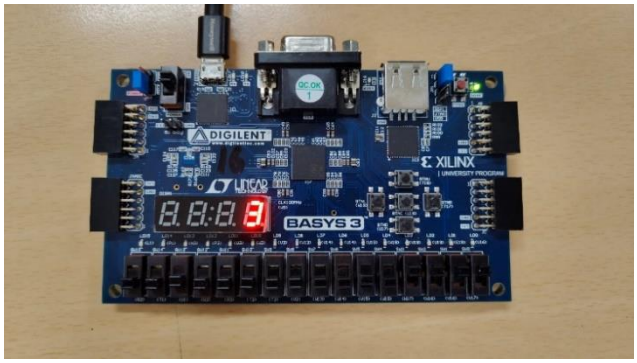
Digit 0



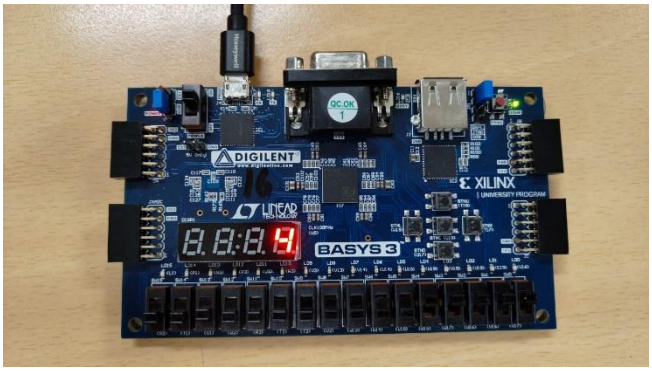
Digit 1



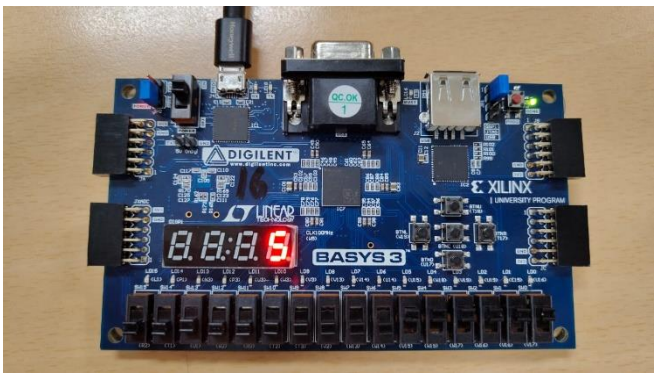
Digit 2



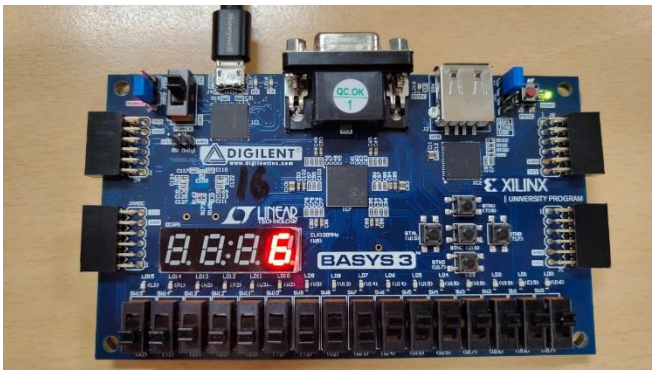
Digit 3



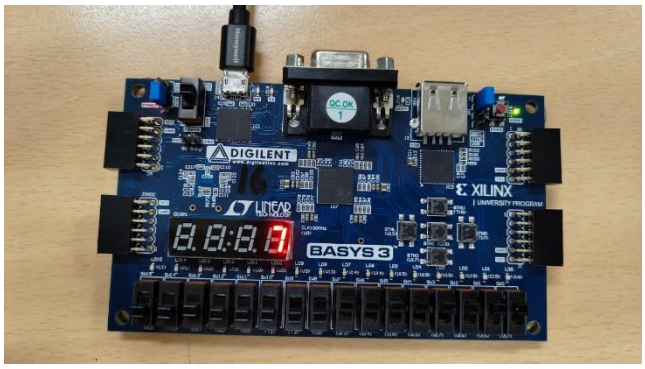
Digit4



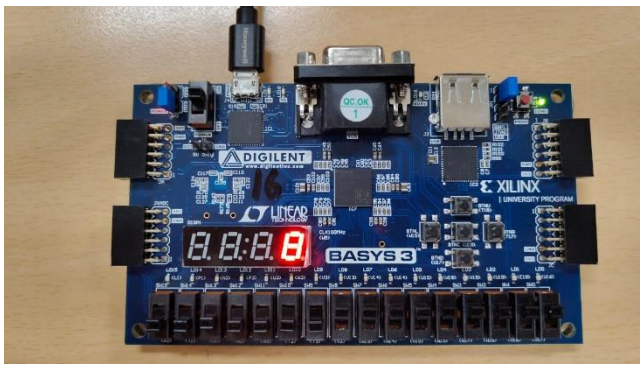
Digit 5



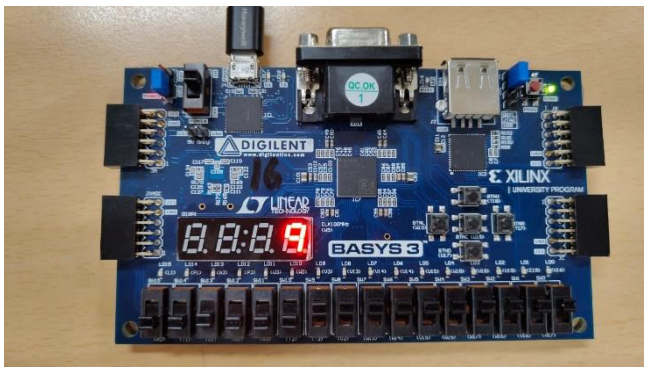
Digit 6



Digit 7



Digit 8



Digit 9

SYNTHESIS REPORT

The design was synthesized successfully with no critical warnings. Utilization summary:

LUTs: 12

Flip Flops: 0

BRAMs and URAMs : 0

LUT	FF	BRAM	URAM	DSP
12	0	0	0	0
12	0	0	0	0

Generated Schematics

The schematics shown below shows the internal conncetivity of the synthesized design. It shows the input, the logic implementation and the output.

Switches → Input Buffers → LUT decoding logic → Output Buffers → Seven-segment pins.

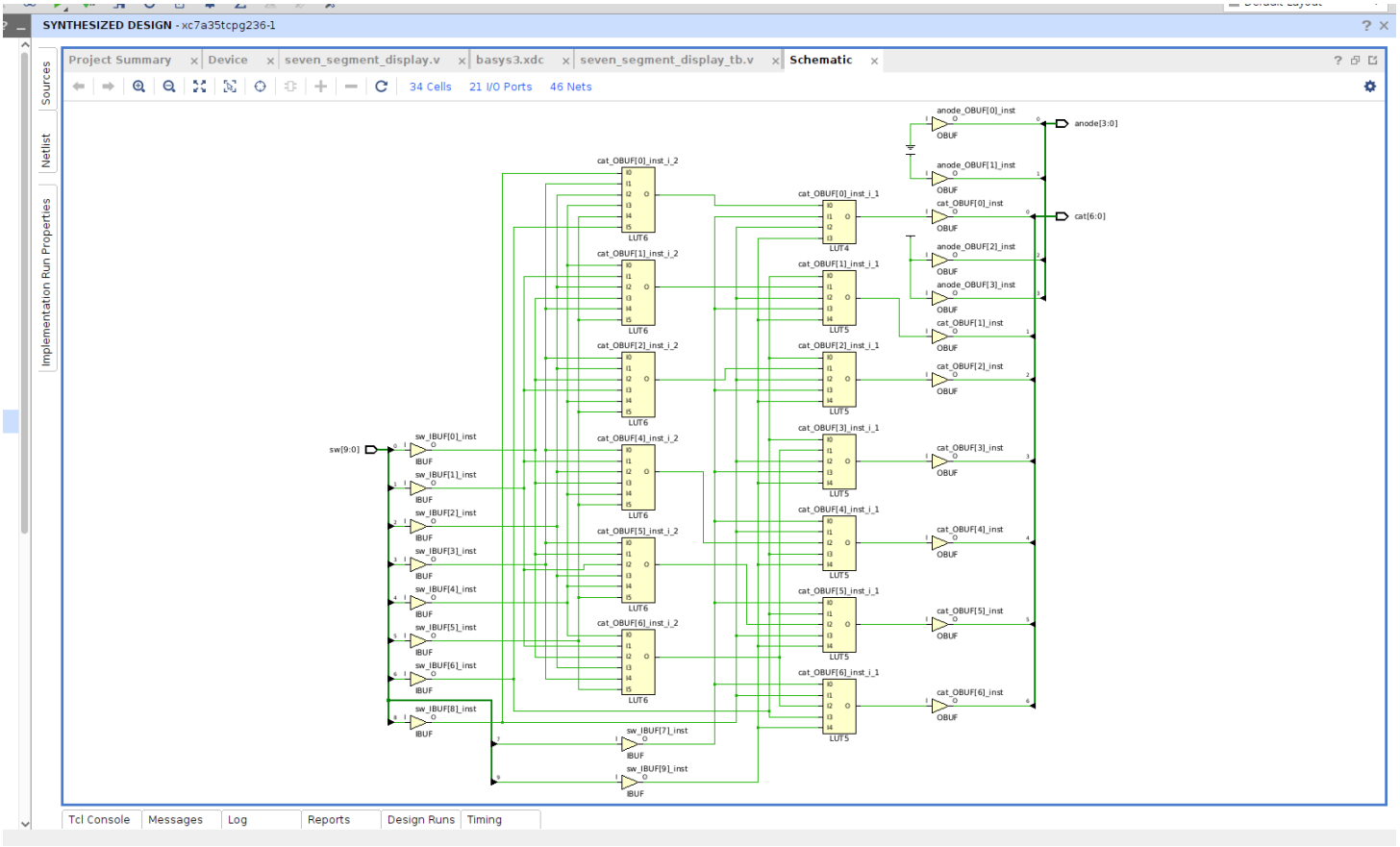


Figure 2 the schematics showing internal working

Conclusion

This lab demonstrated the use of Verilog HDL to interface with real FPGA hardware, specifically the Basys3 board's slide switches and seven-segment display. By implementing combinational logic, the system successfully captured the binary value from the slide switches and decoded it to drive the corresponding segments, displaying digits from 0 to 9.