COL215
Lab Assignment – 1

PARTH ARVIND RATHI 2024CS50875

HARSH VERMA 2024CS10499

DISCUSSION

- The primary objective of Lab Assignment 1 of our COL215 course was to implement basic logic gates (AND, OR, and NOT), simulate their behaviour, and realise them on the BASYS 3 Field Programmable Gate Array (FPGA) board. During the simulation phase, we used the “testbench” feature to test the functionality of our gates. Each gate produced the expected output combinations in response to various input signals. The output observed was consistent with the truth table of the corresponding operations.
- We also learned to execute basic Linux commands like ls, touch, gedit, rm and cd, and could utilise these commands to set up Vivado on our GCL account.
- Then we started a new project that consisted of AND, OR, and NOT gates in the same module in Verilog (for both Target and Simulation).

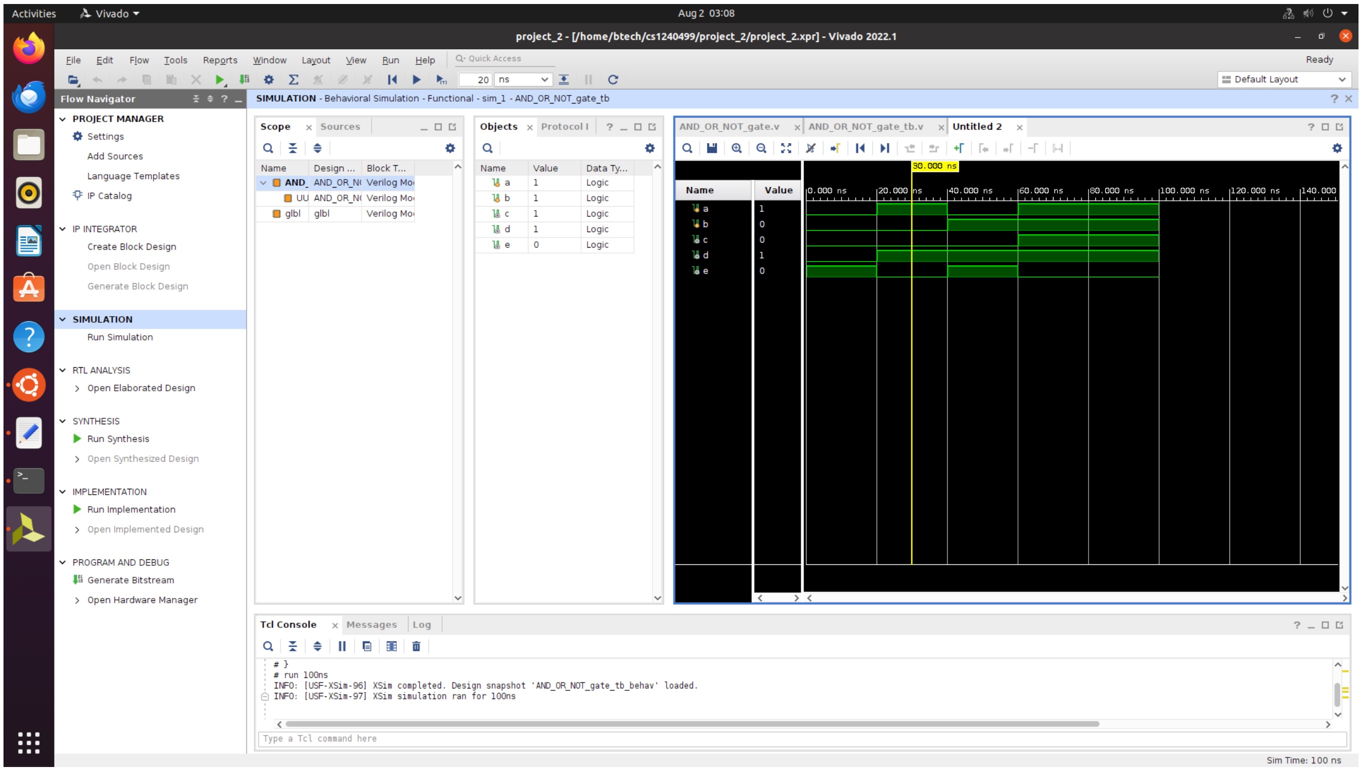
Truth Tables

a	b	c=a&b	d=a|b	e=~a
0	0	0	0	1
0	1	0	1	1
1	0	0	1	0
1	1	1	1	0

VERILOG DESIGN

- *We operated on 2 inputs and returned 3 outputs(corresponding to the gates).*
- *Constrains used*
    - *Mapped switches and LEDs corresponding to each gate, on the BASYS3 board*
    - *Switch V17 with input 'a'*
    - *Switch V16 with input 'b'*
    - *Led U19 with output 'c=a&b'*
    - *Led E19 with output 'd=a|b'*
    - *Led U16 with output 'e=~a'*

SIMULATION



project_2 - [/home/btech/cs1240499/project_2/project_2.xpr] - Vivado 2022.1

SIMULATION - Behavioral Simulation - Functional - sim_1 - AND_OR_NOT_gate_tb

Name	Design ...	Block T...
AND_	AND_OR_N(	Verilog Mo(
UU	AND_OR_N(	Verilog Mo(
glbl	glbl	Verilog Mo(

Name	Value	Data Ty...
a	1	Logic
b	1	Logic
c	1	Logic
d	1	Logic
e	0	Logic

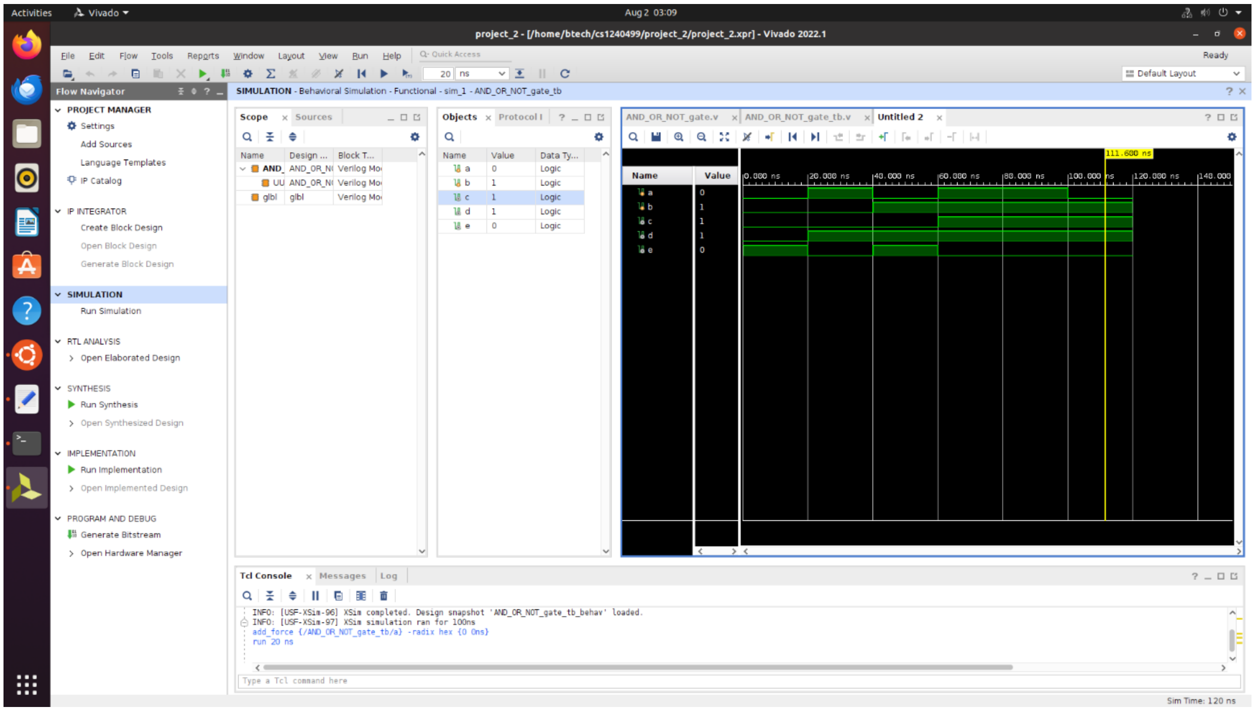
Name	Value
a	1
b	0
c	0
d	1
e	0

```
# }
# run 100ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'AND_OR_NOT_gate_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 100ns
```

- ***AND Gate**: The waveform showed that the output c was high only when both inputs a and b were high, as expected from truth table.*
- ***OR Gate**: The simulation confirmed that the output d was high whenever at least one input was high.*
- ***NOT Gate**: Simulation confirms high output e for low input and low output for high input.*

Forced Simulation:

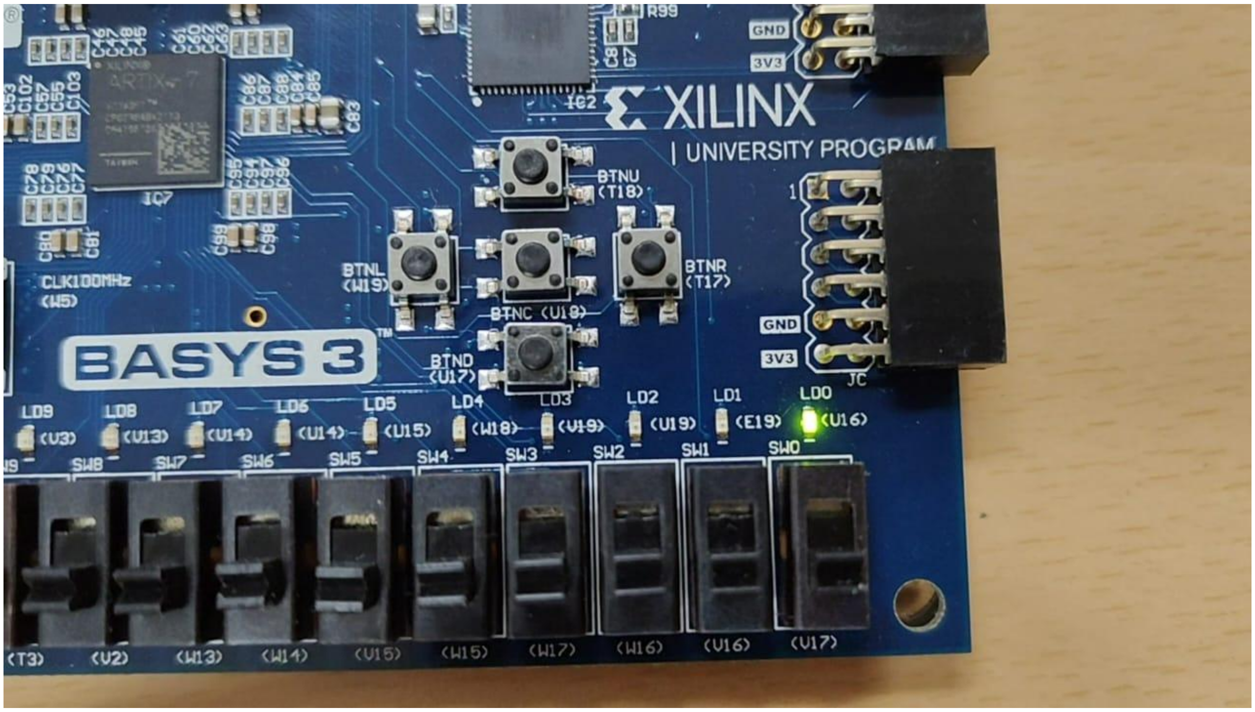
We used forced constant on a and set its value as 0



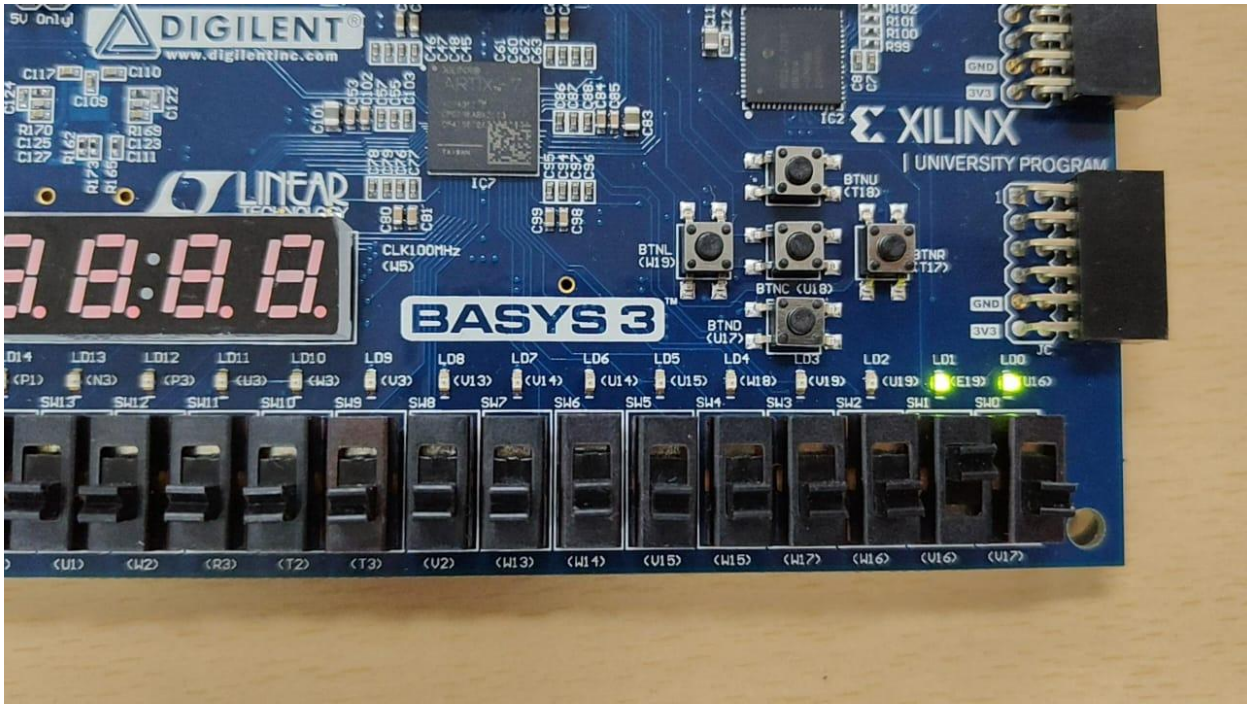
Name	Value	Data Ty...
a	0	Logic
b	1	Logic
c	1	Logic
d	1	Logic
e	0	Logic

```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'AND_OR_NOT_gate_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 100ns
add_force {/AND_OR_NOT_gate_tb/a} -radix hex {0 0ns}
run 20 ns
```

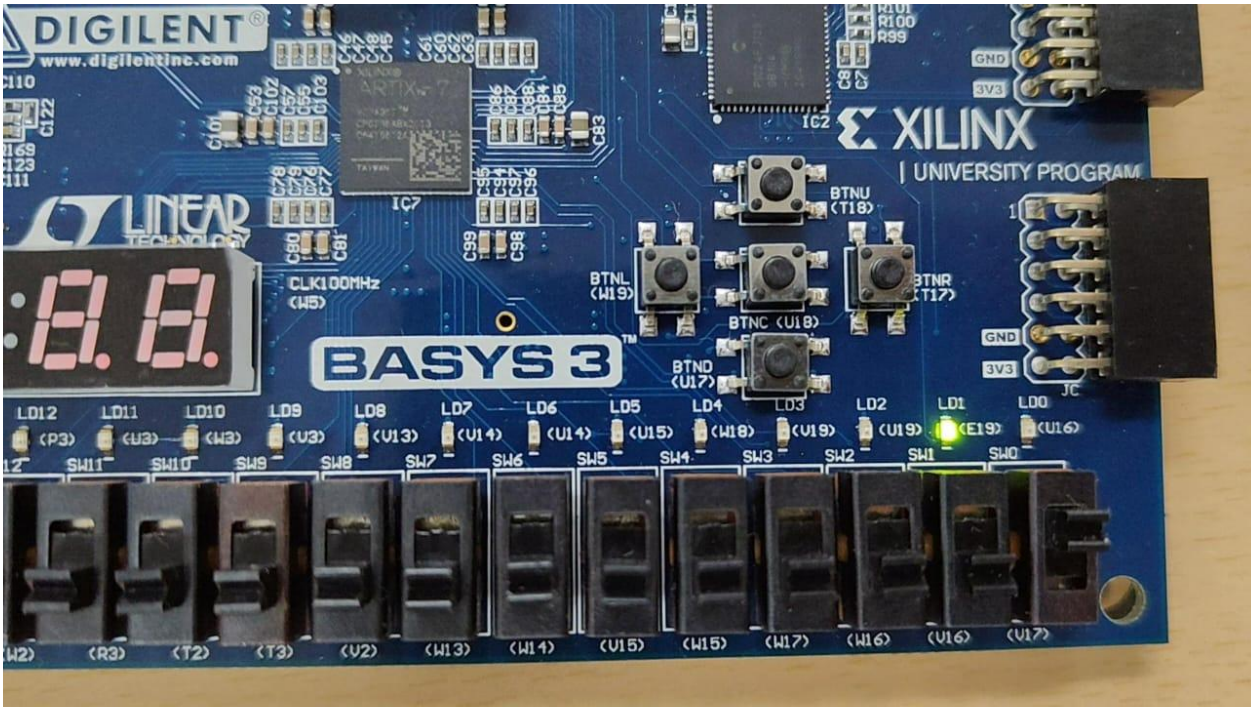
HARDWARE



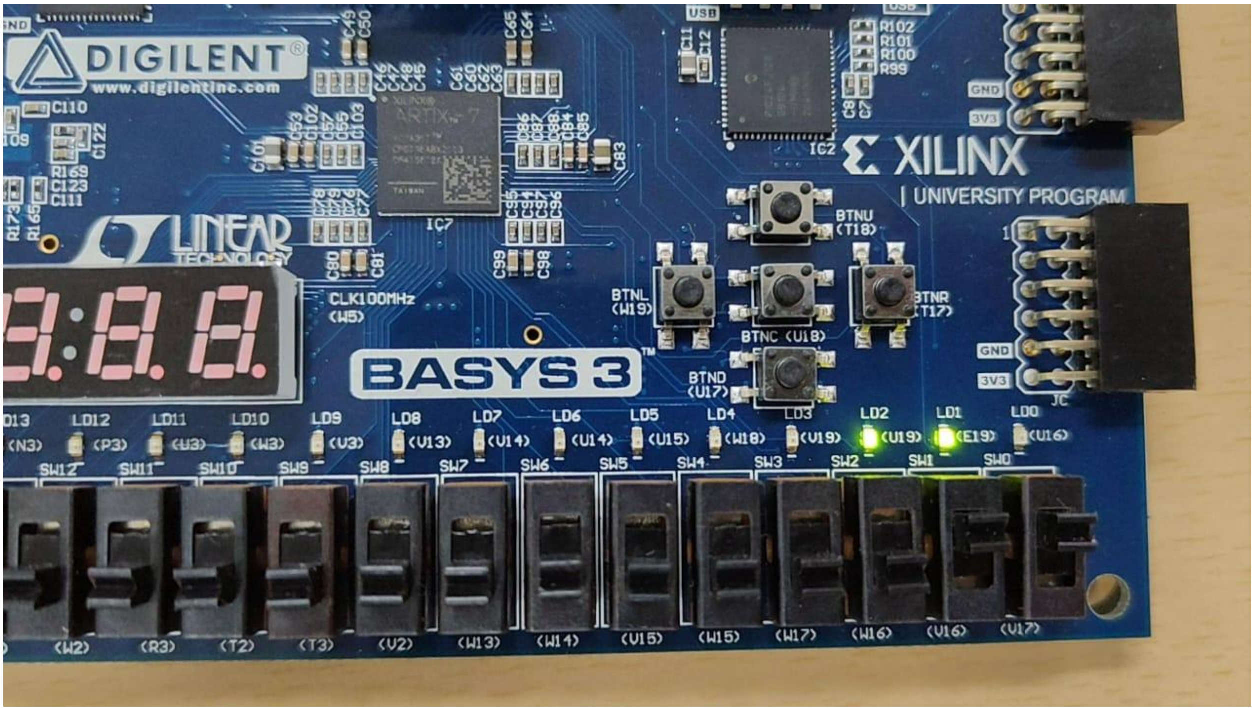
Input: a=0,b=0   Output: c=0,d=0,e=1



Input: a=0,b=1   Output: c=0,d=1,e=1



Input: a=1,b=0   Output: c=0,d=1,e=0

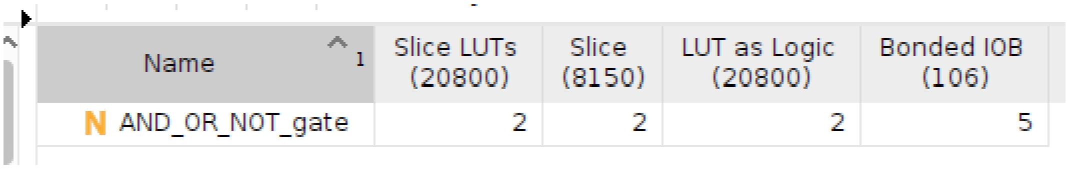


Input: a=1,b=1   Output: c=1,d=1,e=0

SYNTHESIS REPORT

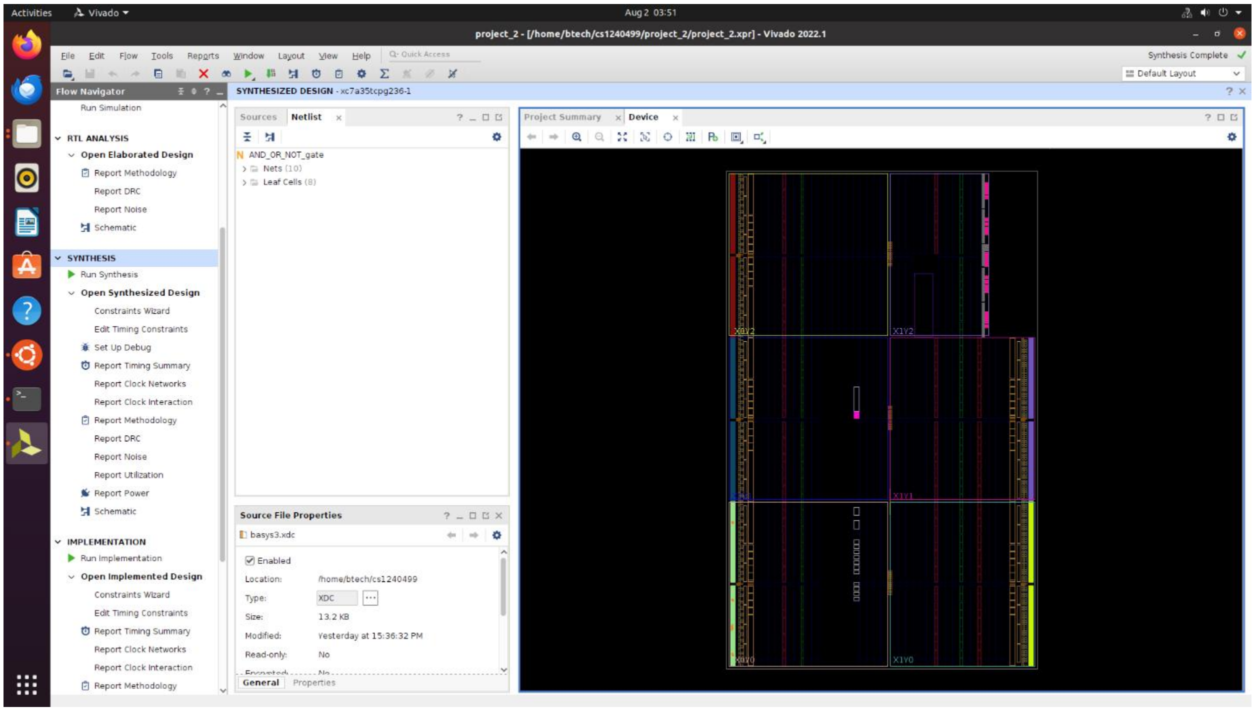
The resource utilization as per Vivado's synthesis report was minimal, consistent with the simplicity of the gates:

- *Flip-Flops: 0 (not needed for purely combinational logic)*
- *LUTs: 2*
- *BRAMs & DSPs: 0*



Name	Slice LUTs (20800)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)
N AND_OR_NOT_gate	2	2	2	5

Device blueprint



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project_2 - [/home/btech/cs1240499/project_2/project_2.xpr] - Vivado 2022.1

Synthesis Complete ✓

SYNTHESIZED DESIGN - xc7a35tcpg236-1

Netlist:

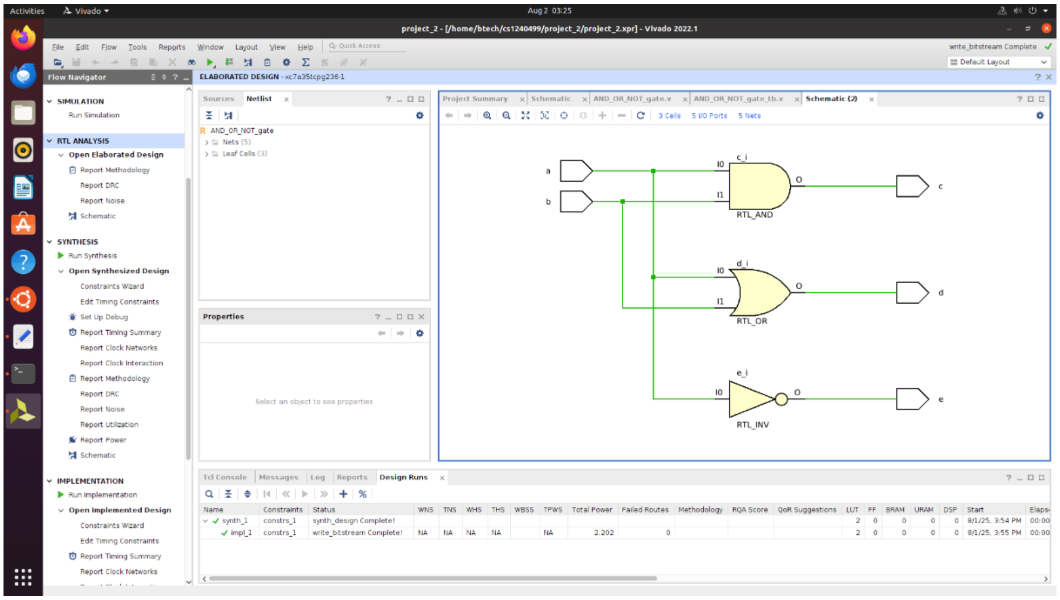
- AND_OR_NOT_gate
  - Nets (10)
  - Leaf Cells (8)

Source File Properties: basys3.xdc

☑ Enabled

Location:	/home/btech/cs1240499
Type:	XDC
Size:	13.2 KB
Modified:	Yesterday at 15:36:32 PM
Read-only:	No
Encrypted:	No

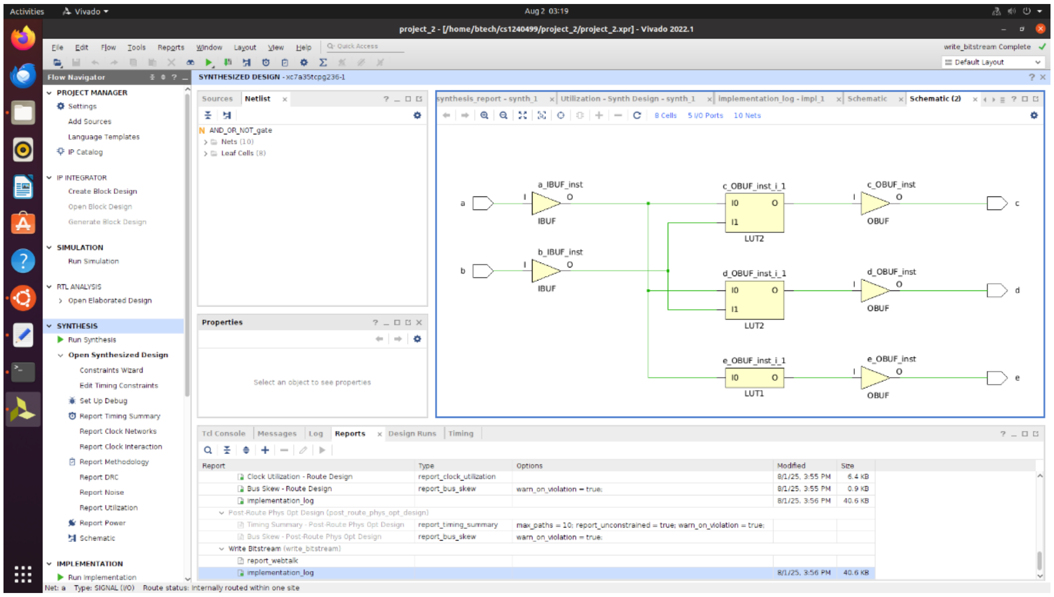
GENERATED SCHEMATICS



project_2 - [/home/btech/cs1240499/project_2/project_2.xpr] - Vivado 2022.1

ELABORATED DESIGN - xc7a35tcpg236-1

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elaps
✓ synth_1	constrs_1	synth_design Complete!												2	0	0	0	0	8/1/25, 3:54 PM	00:00
✓ impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA		NA	2.202	0				2	0	0	0	0	8/1/25, 3:55 PM	00:00



project_2 - [/home/btech/cs1240499/project_2/project_2.xpr] - Vivado 2022.1

SYNTHESIZED DESIGN - xc7a35tcpg236-1

Report	Type	Options	Modified	Size
Clock Utilization - Route Design	report_clock_utilization		8/1/25, 3:55 PM	6.4 KB
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;	8/1/25, 3:55 PM	0.9 KB
implementation_log			8/1/25, 3:56 PM	40.6 KB
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log			8/1/25, 3:56 PM	40.6 KB

Net: a   Type: SIGNAL (I/O)   Route status: Internally routed within one site

CONCLUSION

This lab successfully demonstrated the complete digital design flow using Vivado—from writing Verilog modules and simulating them using testbenches, to synthesizing and implementing them on real FPGA hardware. The behavior of all three gates (AND, OR, and NOT) was verified both through simulation and on the Basys 3 board, with results matching theoretical expectations precisely. Key takeaways include:

- *Understanding of Verilog coding style for combinational logic.*
- *The importance of simulation for verifying logical correctness. Practical experience in synthesis, bitstream generation, and hardware testing using FPGA.*
- *Working knowledge of Vivado and the associated Linux environment setup. This assignment laid a solid foundation for more complex sequential and combinational digital designs in future labs.*