COL215- ASSIGNMENT 5

COL- 215

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1. *AIM*

Develop and implement a Dot Product Controller utilizing a pre-designed Multiply-Accumulate (MAC) unit to efficiently compute the dot product of two vectors. The computed result is displayed on LEDs and 7-segment displays, highlighting principles of modular hardware design and component reuse.

2. *Design and Implementation*

2.1. Top Module: Dot_product_top

Functionality:

It connects the input switches, reset button, clock, storage for vectors A and B, the Multiply-Accumulate (MAC) unit, and the seven-segment display controller.

Submodules Used:

1. btn_debounce_onepulse – Cleans the raw reset button input and generates a one-cycle pulse
2. mac_core - Perfroms sequential multiply-accumulate operations to compute the dot product of the two vectors
3. sevenseg_controller – Scans and updates the 7-segment display.

Implementation Notes:

- led shows the final dot product value.
- Reset ensures stable system initialization.
- Vector elements (a0-a3, b0-b3) are shared with the display logic for visual verification.
- Overflow Handling: An overflow detection flag (oflo) is integrated into the MAC core to handle cases where the result exceeds accumulator width.
- Resource Efficiency: The design prioritizes low LUT/register usage, leaving space for scalability (e.g., larger vectors or extended functionality).
- Dual Output Representation: Results are displayed both on LEDs (for raw binary values) and on the 7-segment display (for human-readable output).

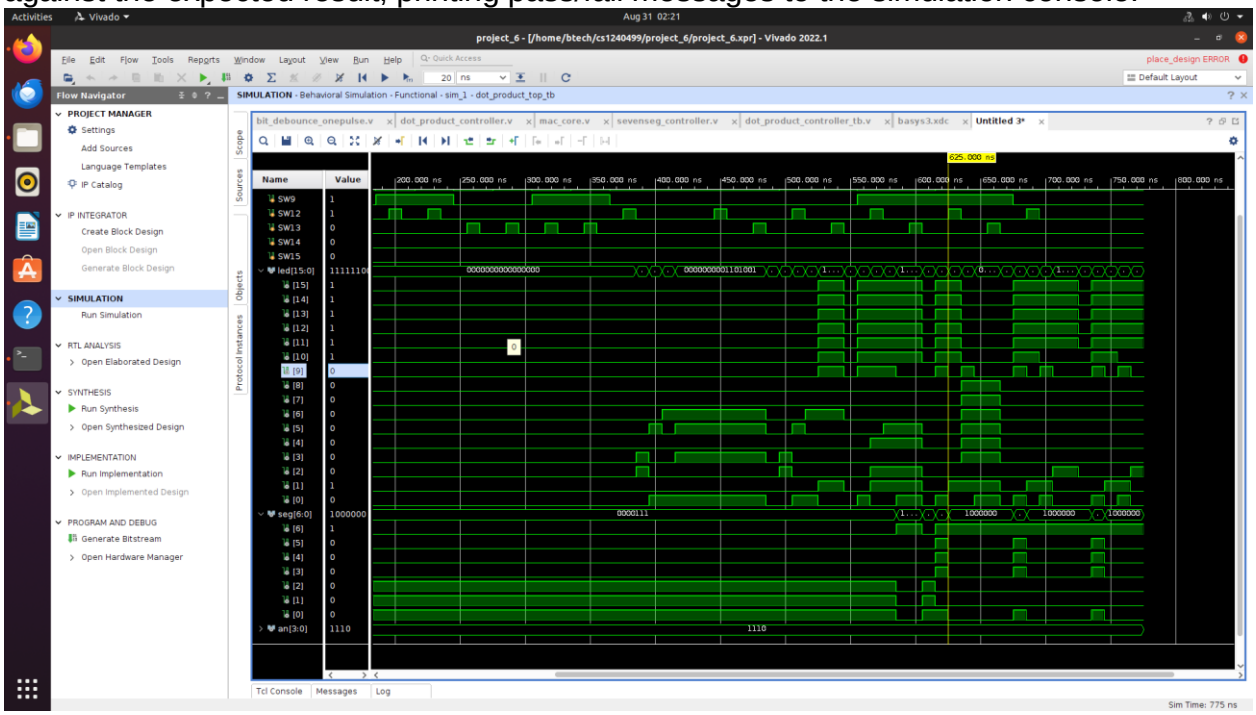
Design Decisions

- Switch-based Input: Vector elements are entered through board switches, allowing manual control and step-by-step debugging during hardware testing
- Debounced Reset: A debouncer was used to ensure a clean, synchronous reset

pulse, preventing metastability from the mechanical push-button.

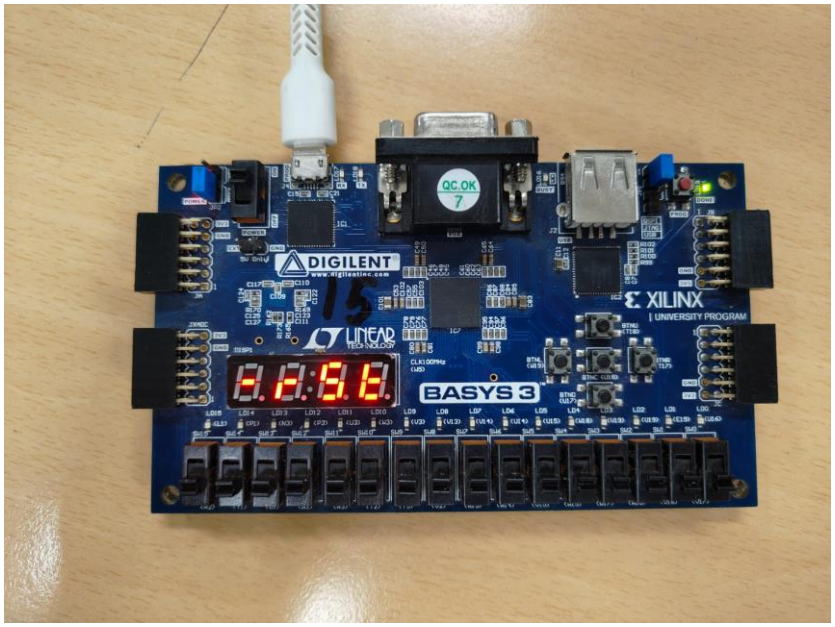
3. *Testbench and Simulation*

The Vector_Dot_tb testbench is designed to verify the functionality of the dot_product_top module. It generates a 100 MHz system clock and applies a clean, debounced reset using the simulated push-button input (BTNC). The testbench then drives the input switches to sequentially load vector elements into registers A[0–3] and B[0–3], overwrites vector **B** with new values, and allows the state machine with the MAC core to compute the dot product. Once computation is complete, the resulting value is observed on the LED output (led). The testbench automatically compares the computed dot product against the expected result, printing pass/fail messages to the simulation console.



4. *Constraints and Hardware Testing*

Snapshots of Board Testing:



Reset button pressed

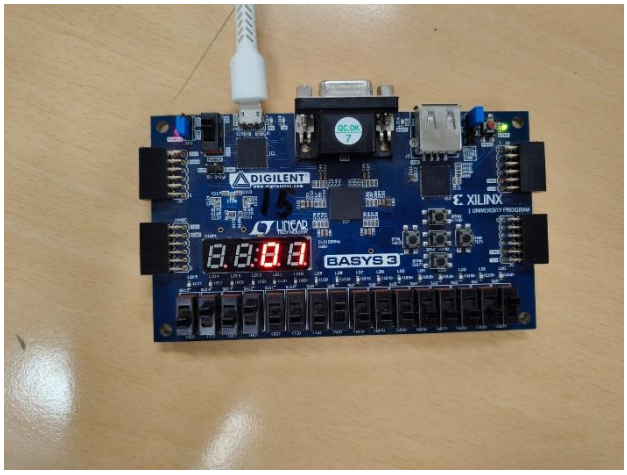


Figure 2 A[1]=1

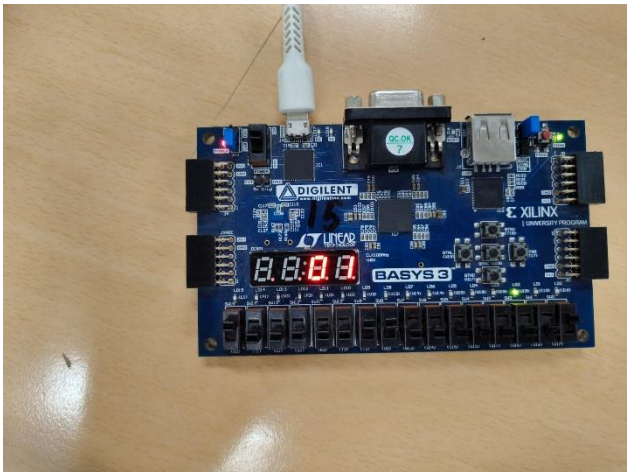


Figure 1 B[3]=1

Input: A = (1,1,1,1)
Input B = (1,1,1,1)
Output C = 0004 (in hexadecimal)

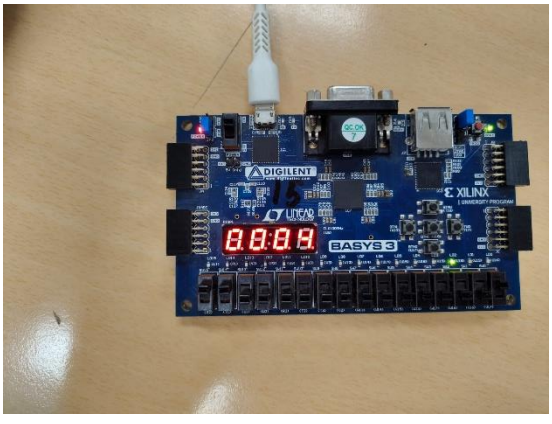


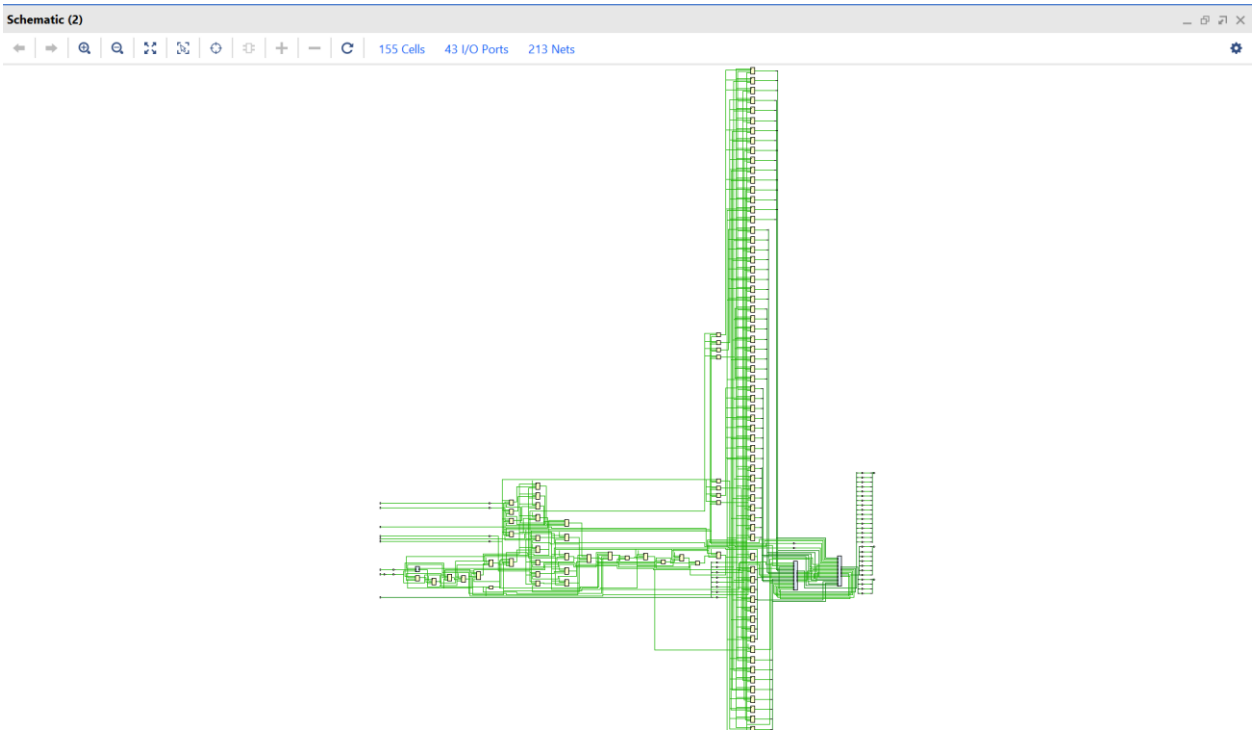
Figure 3 Output 0004

c. Resource Utilization Report

Resource Type	Used	Available	Utilization %
Slice LUTs	225	20800	1.08%
LUT as Logic	225	20800	1.08%
LUT as Memory	0	9600	0.00%
Slice Register	185	41600	0.44%
Flip-Flops	185	41600	0.44%
Latches	0	41600	0.00%
F7 Muxes	3	16300	0.02%
F8 Muxes	0	8150	0.00%
DSPs	0	90	0.00%
Block RAMs (BRAM)	0	50	0.00%

LUT	FF	BRAM	URAM	DSP
225	185	0	0	0
222	185	0	0	0

Schematic of Synthesized Design



Explanation: The schematic of the **Dot_product_top** is divided into four main functional blocks: the input interface, the debounced reset unit, the accumulator (MAC core with control FSM), and the display/output module

7. Conclusion:

- The design was successfully implemented on the FPGA and consistently produced correct dot product results for the given input vectors.
- A debouncer and synchronous reset mechanism were incorporated to ensure stable system initialization, effectively preventing metastability and undefined behavior.
- The accumulator module demonstrated reliable performance, handling sequential multiply-accumulate operations accurately while also providing proper overflow detection.
- The display controller enhanced system usability by allowing vector elements and the computed dot product to be clearly visualized on the 7-segment LEDs through simple switch-based control.
- Furthermore, the design was shown to be resource-efficient, utilizing minimal LUTs and registers, which leaves ample room for scalability to support larger vector sizes or the integration of additional functionality..