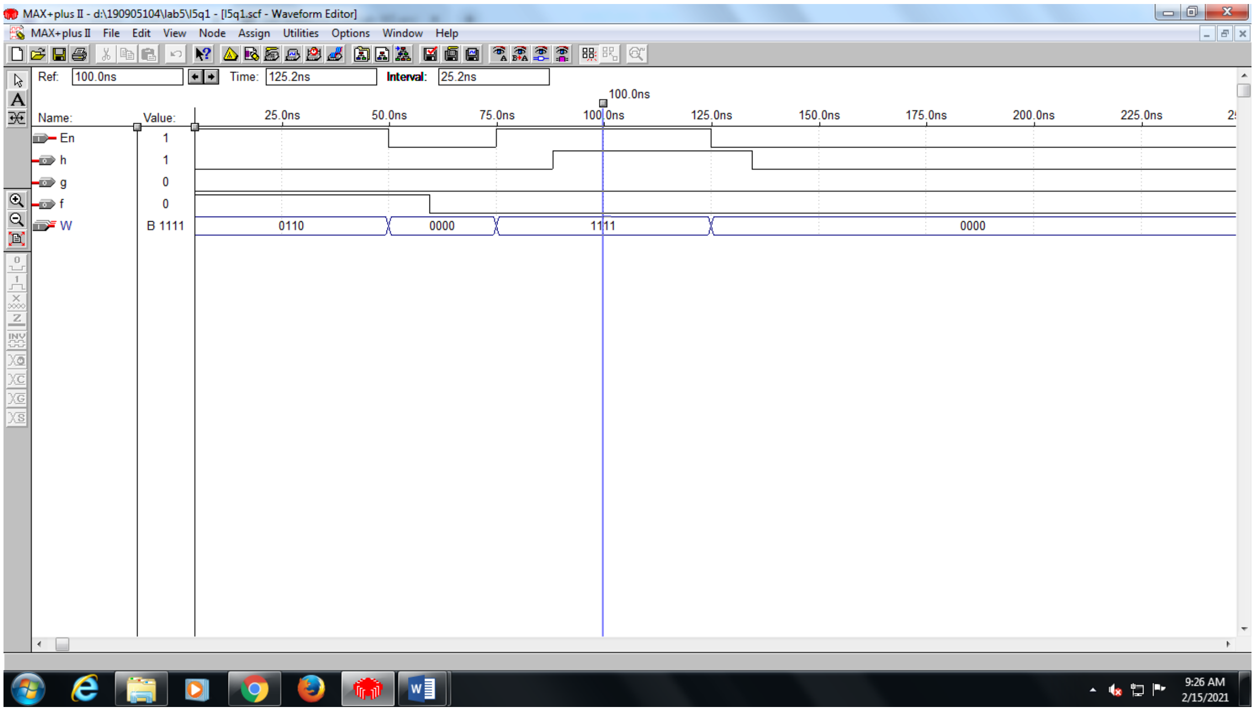
Week 5

1)

```
// Design and simulate a combinational circuit with external gates and a 4 to 16 decoder built
// using a decoder tree of 2 to 4 decoders to implement the functions below.
// F= ab’c + a’cd + bcd’ , G=acd’ + a’b’c and H=a’b’c’ + abc + a’cd

module dec2to4(W,En,Y);
input[1:0]W;
input En;
output [0:3]Y;
reg [0:3]Y;
always@(W or En)
begin
if(En==1)
case(W)
0: Y=4'b1000;
1: Y=4'b0100;
2: Y=4'b0010;
3: Y=4'b0001;
endcase
else
Y=4'b0000;
end
endmodule

module dec4to16(W,En,Y);
input [3:0]W;
input En;
output [0:15]Y;
```

```
wire[0:3]M;

dec2to4 dec1(W[3:2],En,M[0:3]);
dec2to4 dec2(W[1:0],M[0],Y[0:3]);
dec2to4 dec3(W[1:0],M[1],Y[4:7]);
dec2to4 dec4(W[1:0],M[2],Y[8:11]);
dec2to4 dec5(W[1:0],M[3],Y[12:15]);
endmodule


module l5q1(W, En, f, g, h);
input [3:0]W;
input En;
output f, g, h;
wire [0:15]Y;

dec4to16 dec1(W[3:0], En, Y);
or(f, Y[3], Y[6], Y[7], Y[10], Y[11], Y[14]);
or(g, Y[2], Y[3], Y[10], Y[14]);
or(h, Y[0], Y[1], Y[3], Y[7], Y[14], Y[15]);
endmodule
```


MAX+plus II - d:\190905104\lab5\l5q1 - [l5q1.scf - Waveform Editor]
MAX+plus II File Edit View Node Assign Utilities Options Window Help
100.0ns
25.0ns
50.0ns
75.0ns
100.0ns
125.0ns
150.0ns
175.0ns
200.0ns
225.0ns
0110
0000
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9:26 AM
2/15/2021

Ref: 100.0ns Time: 125.2ns Interval: 25.2ns

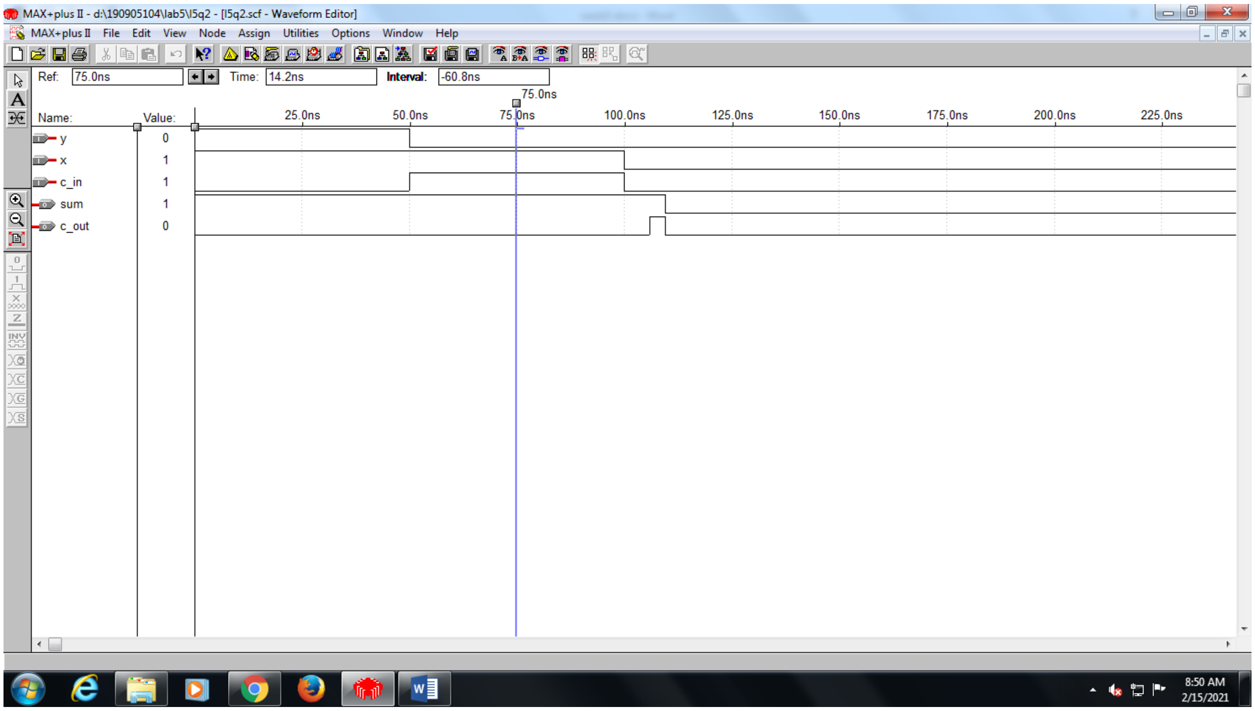
Name:	Value:
En	1
h	1
g	0
f	0
W	B 1111

2)

// Design and implement a full adder using 2 to 4 decoder(s) and other gates.

```
module dec2to4(W, En, Y);
input [1:0]W;
input En;
output [0:3]Y;
reg [0:3]Y;
always @(W or En)
begin
if(En==0)
Y=4'b0000;
else
case(W)
0:Y=4'b1000;
1:Y=4'b0100;
2:Y=4'b0010;
```

```
3:Y=4'b0001;
endcase
end
endmodule

module l5q2(x, y, c_in, sum, c_out);
input x, y, c_in;
output sum, c_out;
wire [0:3] dec0w;
wire [0:3] dec1w;
wire [0:3] dec2w;
dec2to4 d0({1'b0, x}, 1'b1, dec0w);
dec2to4 d1({c_in, y}, dec0w[1], dec1w);
dec2to4 d2({c_in, y}, dec0w[0], dec2w);
or(sum, dec2w[3], dec1w[1], dec1w[2], dec1w[3]);
or(c_out, dec2w[1], dec2w[2], dec1w[0], dec1w[3]);
endmodule
```



MAX+plus II - d:\190905104\lab5\l5q2 - [l5q2.scf - Waveform Editor]

Ref: 75.0ns Time: 14.2ns Interval: -60.8ns

Name:	Value:
y	0
x	1
c_in	1
sum	1
c_out	0

3)

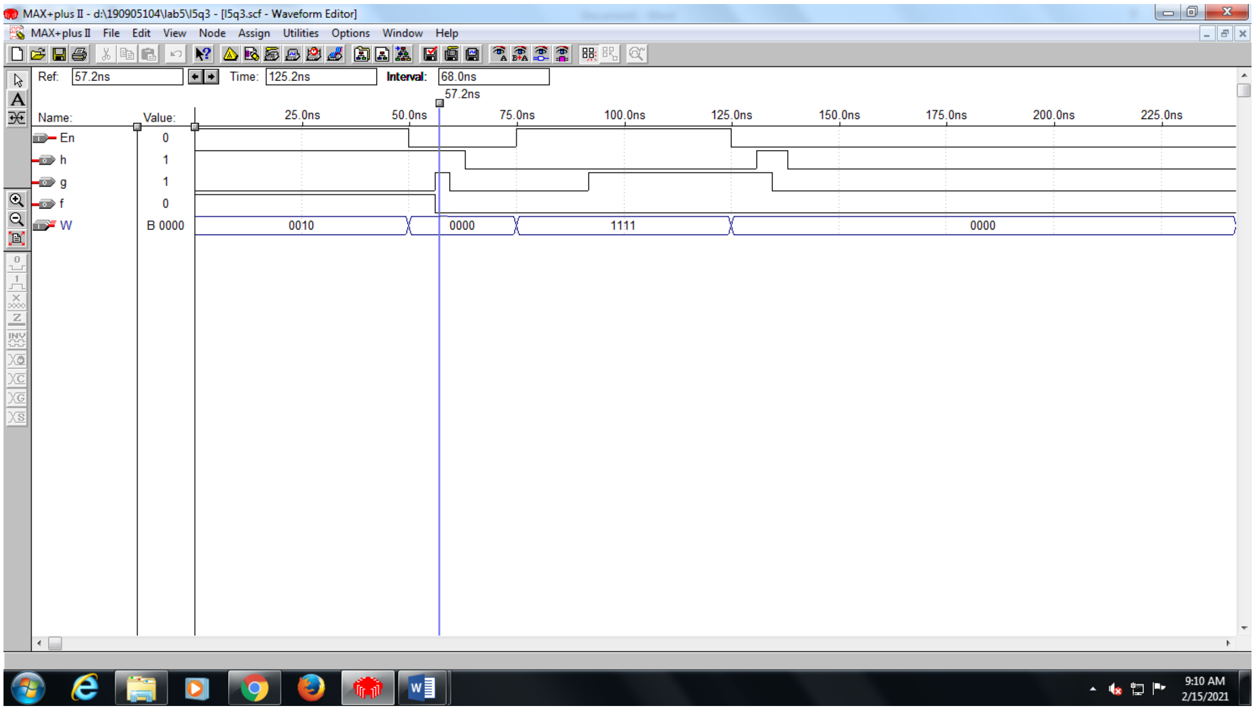
// Design and simulate the circuit with 3 to 8 decoder(s) and external gates to implement the functions below.

// F(a, b, c, d)= Sm(2,4,7,9) G (a, b, c, d)= Sm (0,3,15) H(a, b, c, d)= Sm(0,2,10,12)

```
module dec2to4(W, En, Y);

input [1:0]W;

input En;

output [0:3]Y;

reg [0:3]Y;

always @(W or En)

begin

if(En==0)

Y=4'b0000;

else

case(W)
```

```
0:Y=4'b1000;

1:Y=4'b0100;

2:Y=4'b0010;

3:Y=4'b0001;

endcase

end

endmodule


module dec3to8(W,En,Y);

input [2:0]W;

input En;

output [0:7]Y;

wire[0:3]M;


dec2to4 dec1({1'b0, W[2]},En,M);

dec2to4 dec2(W[1:0],M[0],Y[0:3]);

dec2to4 dec3(W[1:0],M[1],Y[4:7]);

endmodule


module l5q3(W, En, f, g, h);

input [3:0]W;

input En;

output f, g, h;

wire [0:7] temp0;

wire [0:7] temp1;

wire [0:7] temp2;

wire [0:7] temp3;

wire [0:7] temp4;

dec3to8 dec0({1'b0, W[3], W[2]}, En, temp0);
```

```
dec3to8 dec1({1'b0, W[1], W[0]}, temp0[0], temp1);
dec3to8 dec2({1'b0, W[1], W[0]}, temp0[1], temp2);


dec3to8 dec3({1'b0, W[1], W[0]}, temp0[2], temp3);
dec3to8 dec4({1'b0, W[1], W[0]}, temp0[3], temp4);


or(f, temp1[2], temp2[0], temp2[3], temp3[1]);
or(g, temp1[0], temp1[3], temp4[3]);
or(h, temp1[0], temp1[2], temp3[2], temp4[0]);
endmodule
```



MAX+plus II - d:\190905104\lab5\l5q3 - [l5q3.scf - Waveform Editor]

Ref: 57.2ns Time: 125.2ns Interval: 68.0ns

Name:	Value:
En	0
h	1
g	1
f	0
W	B 0000