X86 PROCESSOR ARCHITECTURE

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General Concepts

1. Basic Microcomputer Design

- The central processor unit (CPU), where calculations and logic operations take place.
- CPU contains:
  - a limited number of storage locations, called Registers,
  - a high-frequency clock,
  - a control unit (CU),
  - and an arithmetic logic unit (ALU).

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- The clock synchronizes the internal operations of the CPU with other system components.
- The control unit (CU) coordinates the sequencing of steps involved in executing machine instructions.
- The arithmetic logic unit (ALU) performs arithmetic operations such as addition and subtraction and logical operations such as AND, OR, and NOT.

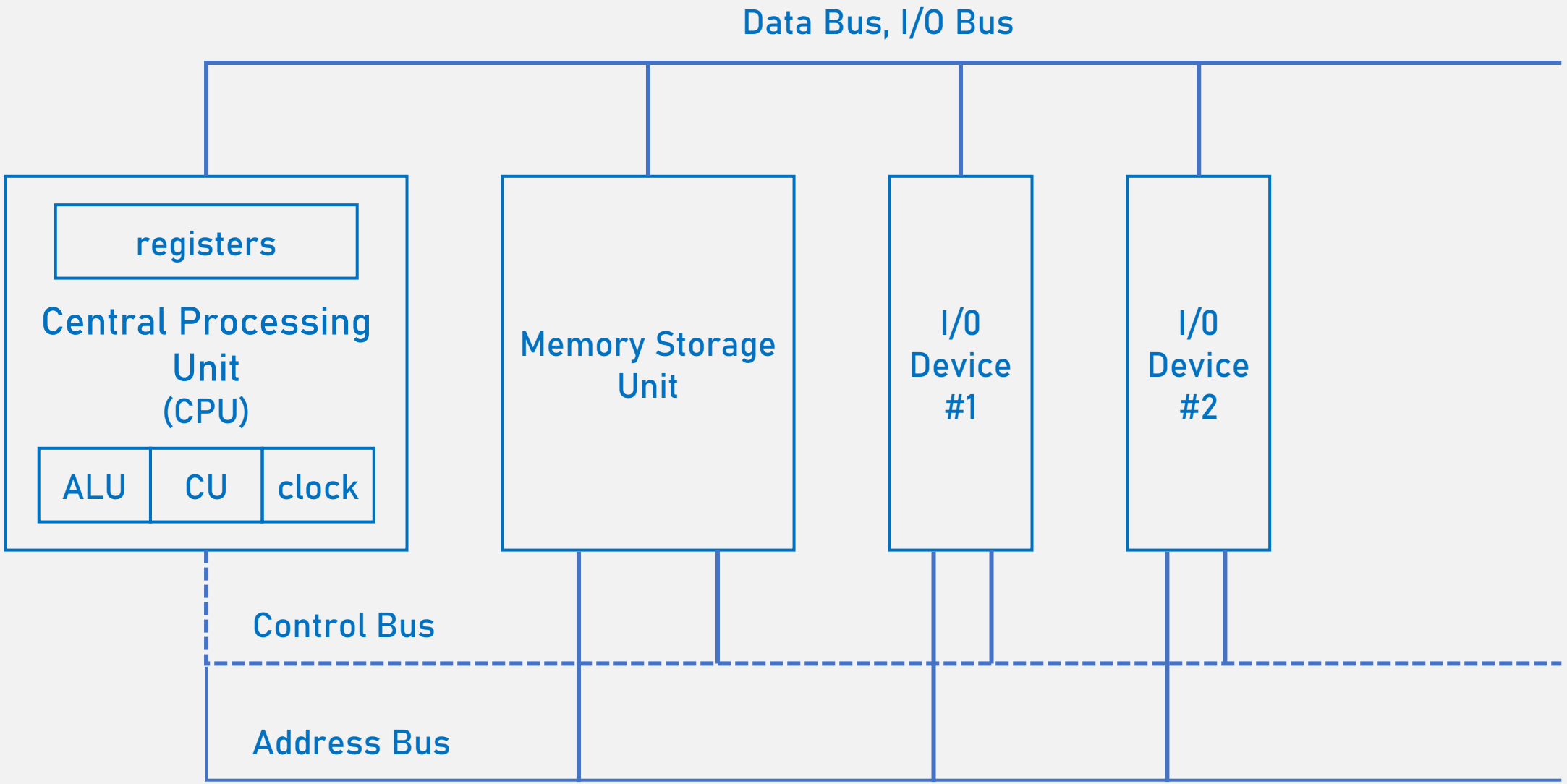
Memory Storage Unit

- The memory storage unit is where instructions and data are held while a computer program is running.
- The storage unit receives requests for data from the CPU,
  - transfers data from random access memory (RAM) to the CPU,
  - and transfers data from the CPU into memory.

"All processing of data takes place within the CPU, so programs residing in **memory must be copied into the CPU** before they can execute."

Bus

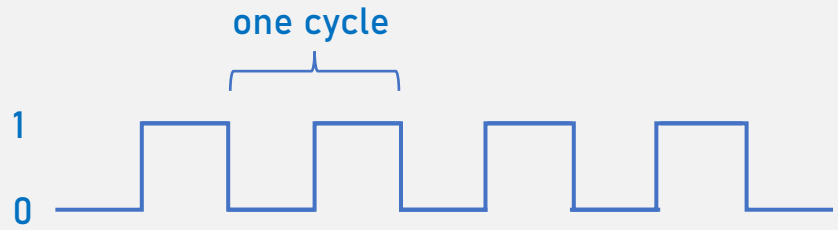
- A bus is a group of parallel wires that transfer data from one part of the computer to another.
  - Data Bus: transfers instructions and data between the CPU and memory.
  - I/O Bus: transfers data between the CPU and the system input/output devices.
  - Control Bus: uses binary signals to synchronize actions of all devices attached to the system bus.
  - Address Bus: holds the addresses of instructions and data when the currently executing instruction transfers data between the CPU and memory.



Block Diagram of a Microcomputer

Clock

- Each operation involving the CPU and the system bus is synchronized by an internal clock pulsing at a constant rate.
- The basic unit of time for machine instructions is a machine cycle (or clock cycle).
- The length of a clock cycle is the time required for one complete clock pulse.



- A machine instruction requires at least one clock cycle to execute.
- Instructions requiring memory access often have empty clock cycles called wait states because of the differences in the speeds of the CPU, the system bus, and memory circuits.

2. Instruction Execution Cycle

- The execution of a single machine instruction can be divided into a sequence of individual operations called the instruction execution cycle.
- Before executing, a program is loaded into memory.
- The instruction pointer contains the address of the next instruction.
- The instruction queue holds a group of instructions about to be executed.

"Executing a machine instruction requires three basic steps: fetch, decode, and execute."

Fetch

- The control unit fetches the next instruction from the instruction queue and increments the instruction pointer (IP). The IP is also known as the program counter.

Decode

- The control unit decodes the instruction's function to determine what the instruction will do.
- The instruction's input operands are passed to the ALU, and signals are sent to the ALU indicating the operation to be performed.

Execute

- The ALU executes the instruction using the named registers and internal registers as operands and sends the output to named registers and/or memory.
- The ALU updates status flags providing information about the processor state.

"Two more steps are required when the instruction uses a memory operand: fetch operand and store output operand."

Fetch Operands

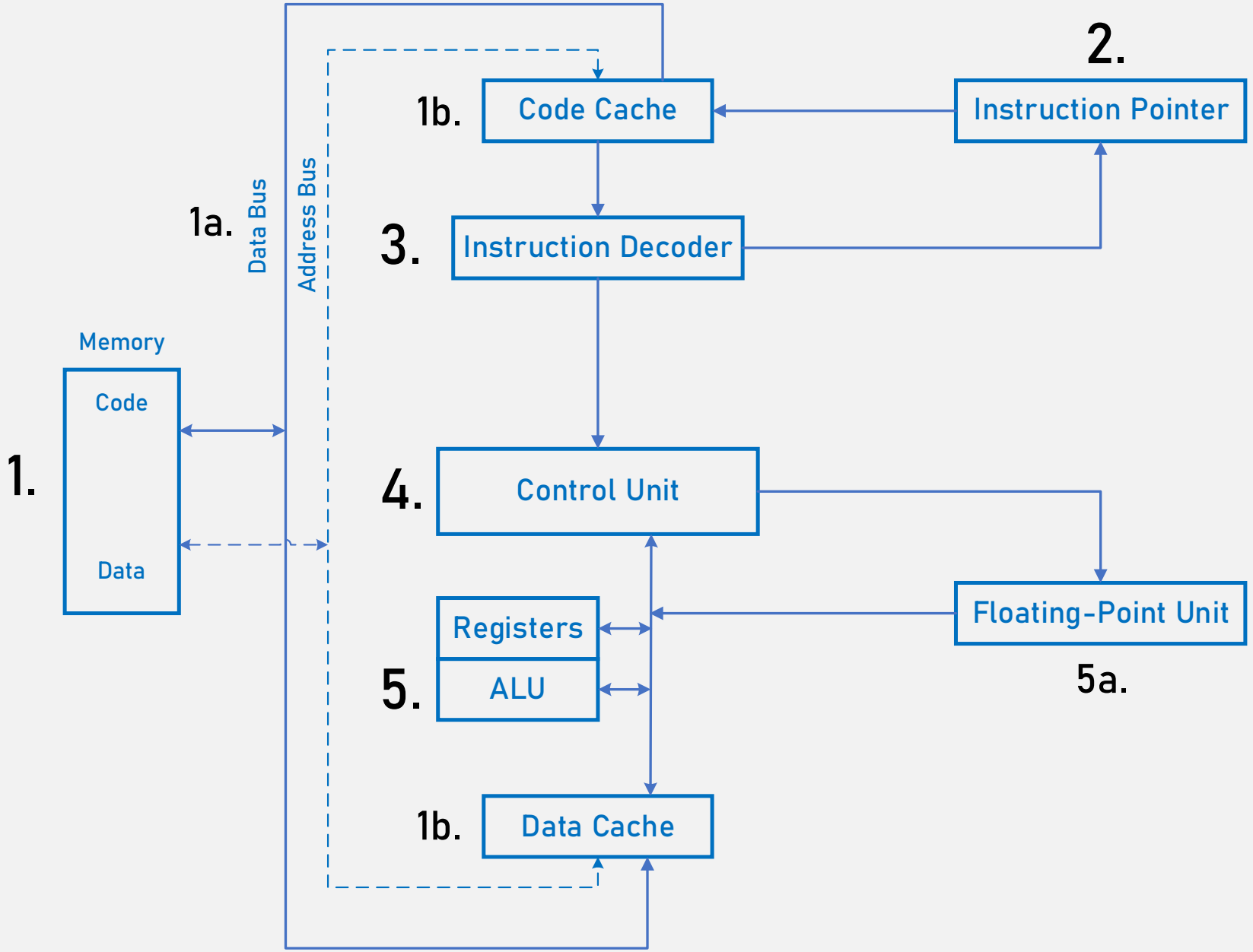
- If the instruction uses an input operand located in memory, the control unit uses a read operation to retrieve the operand and copy it into internal registers.

Store Output Operands

- If the output operand is in memory, the control unit uses a write operation to store the data.

Steps of Instruction Execution Cycle as Pseudocode

```
loop
•     fetch next instruction
•     advance the instruction pointer (IP)
•     decode the instruction
•     if memory operand needed, read value from memory
      ,execute the instruction
•     if result is memory operand, write result to memory
continue loop
```



Simplified CPU Block Diagram