Design and Implementation of Level Triggered D Flip Flop

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ABSTRACT

The most important memory element in a sequential logic circuit is Flip-Flop. A flip flop is a bistable multivibrator which has two stable states. It can have one or more inputs, which helps the device to flip and flop between the possible output states. It can store one bit of data either 0 or a 1. They are classified as SR Flip-Flop, D Flip-Flop, JK Flip-Flop and T Flip-Flop. These flip flops are used in building registers and counters. The proposed paper shows the implementation of level triggered D Flip-Flop using CMOS with 130nm SkyWater technology.

CIRCUIT DETAILS

In an SR flip flop, the condition S=R=1 generating invalid state is undesirable. To avoid this condition, a not gate is placed between the S and R inputs. The result is SR flip flop is converted into a D flip-flop (data flip-flop or delay flip-flop). Here, the data is fed at the D input. The circuit consists of 5 PMOS and 5 NMOS transistors. In this reference circuit diagram, M1,M2,M5,M7 and M8 are PMOS transistors and M3,M4,M6,M9 and M10 are NMOS transistors. D input is fed simultaneously to both M1 and M4.M5 and M6 forms CMOS inverter. Output of second stage is Q, output of last stage is Qbar. When CLK=0, output Q remains in its previous state. When CLK=1 and D=1 ,Q=1.In the same lines when CLK=1 and D=0, Q=0.

CIRCUIT DIAGRAM

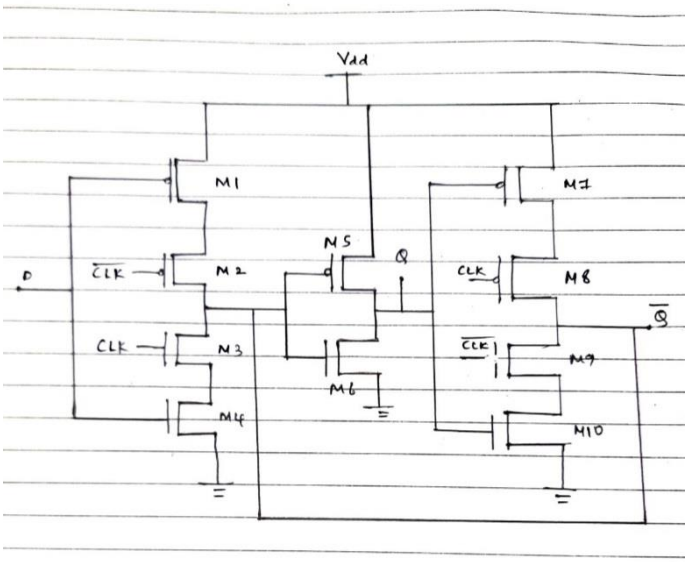

Fig-1 : Reference Circuit Diagram

WAVEFORMS

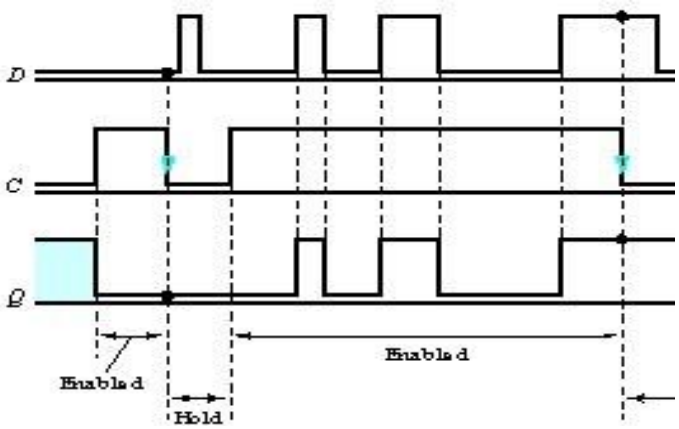

Fig-2 : Reference Waveforms

REFERENCE

https://www.ques10.com/p/36422/implement-d-flip-flop-using-static-cmos-what-are-o/